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# CMOS single-chip 8-bit MCU with 12-bit A/D converter and LCD driver



## Main features

- **8-bit Microcontroller With High Speed 8051 CPU**
- **Basic MCU Function**
  - 32 Kbytes Flash Code Memory
  - 1024 bytes SRAM
- **Built-in Analog Function**
  - Power-On Reset and Low Voltage Detect Reset
  - Internal 16MHz RC Oscillator ( $\pm 1.5\%$ ,  $T_A = 0 \sim +50^\circ\text{C}$ )
  - Watchdog Timer RC Oscillator (5kHz)
- **Peripheral Features**
  - 12-bit Analog to Digital Converter (16 inputs)
  - USI (USART + SPI + I2C) 2 sets
  - LCD Driver (21 segments x 8 commons)
- **I/O and Packages**
  - Up to 42 programmable I/O lines with 48/44-pin package
  - 48 QFN, 44 MQFP, 32 LQFP, 32/28 SOP, 24 QFN
- **Operating Conditions**
  - 2.2V to 5.5V Wide Voltage Range
  - $-40^\circ\text{C}$  to  $85^\circ\text{C}$  Temperature Range
- **Application**
  - Small Home Appliance
  - BLDC Motor Controller

## MC96F6432A

## MC96F6332A

### User's manual

### V 2.00

Revised 08 May, 2023

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## Revision history

Version	Date	Revision list
0.0	2015.09.18	Published this book.
0.1	2015.12.16	Change symbol name from ILE, DLE, FSE, $t_{CON}$ , $V_{AN}$ , $I_{AN}$ to INL, DNL, TOE, $t_{CONV}$ , $V_{AIN}$ , $I_{AIN}$ in 7.3 A/D Converter Characteristics Fix typos.
1.0	2016.02.03	Add a "MC96F6432AU" 48 QFN package. Add IRC Max 16MHz in 7.6 High Internal RC Oscillator Characteristics. Add a note about IRC frequency in 11.1 Clock Generator.
1.1	2016.03.25	Modify 48-Pin QFN Package Diagram
1.2	2016.04.08	Add a "Full-flash erase mode method" in different table. Remove the note about "direct bit test and branch instructions", Modify the program tips in Chapter 15. Flash Memory. Add an appendix about "Flash Protection for invalid Erase/Write"
1.3	2016.05.26	Change '8.5MHz (Max)' to "Main X-TAL Operating Frequency" in Electrical Characteristics.
1.4	2016.05.30	Add a "MC96F6332AL" 32LQFP package.
1.5	2016.07.06	Remove the 28TSSOP package. Change Gang programmer from StandAlone GANG8 to E-GANG4/E-GANG6. Fixed typos of I2C Status Register.
1.6	2017.02.09	Updated Package diagrams in Chapter 4. Package Diagram. Added the note on the flash memory erase and write in Chapter 15. Flash Memory. Updated OCD dongle image in Chapter 1.3 Development tools.
1.7	2018.06.22	Fixed typos. Updated All Package Diagram.
1.8	2022.02.24	Add a "MC96F6232AU" 24 QFN package.
1.9	2022.10.26	Revised this book. Modify a font. Added Figure 1.1 Device Nomenclature.
2.0	2022.11.09	Fixed the typo in Chapter 15. Flash memory
2.00	2023.05.08	Changed the format of the revision number to "X.YY" according to internal policy.

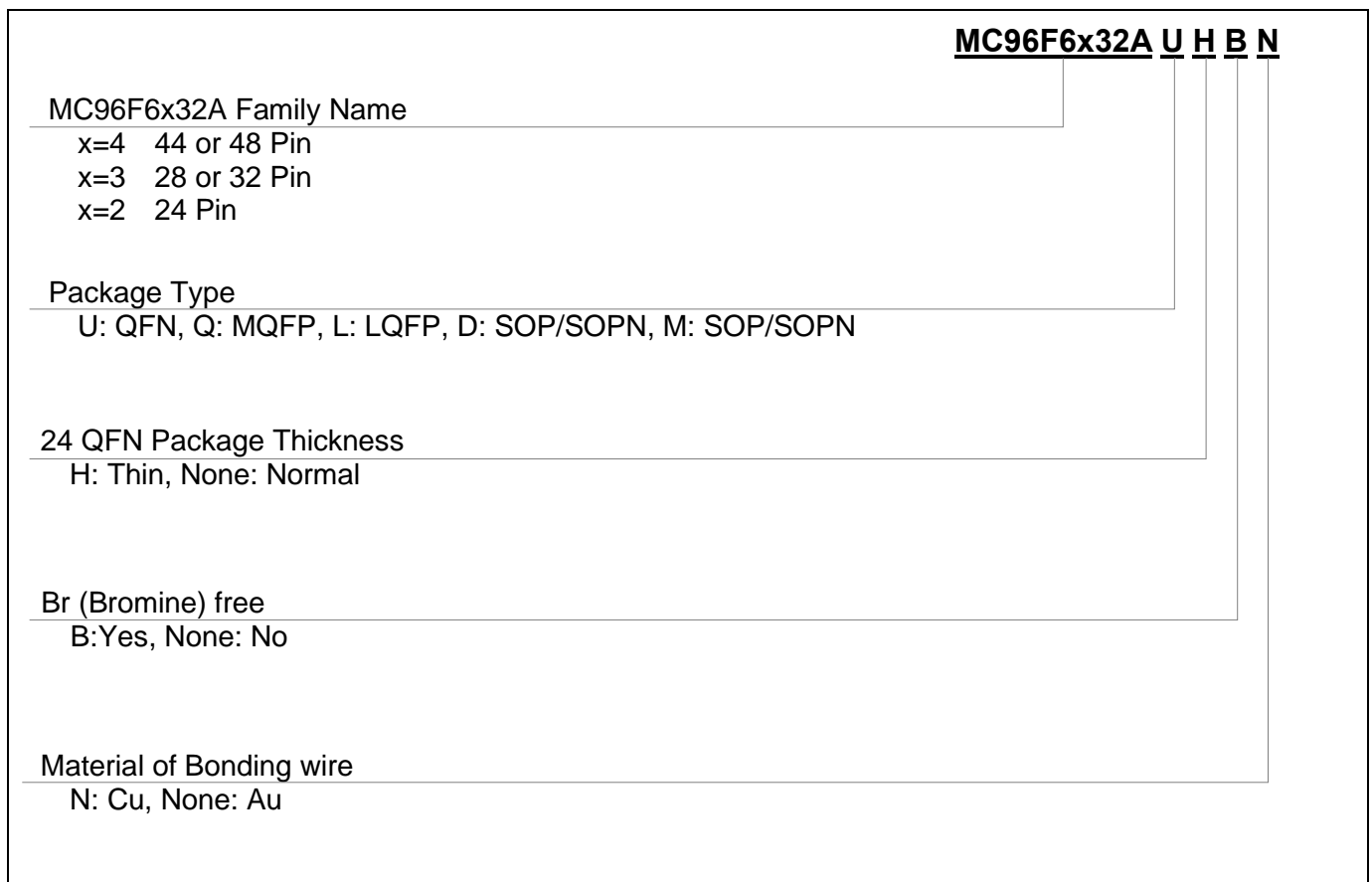
# 1 Overview

## 1.1 Description

The MC96F6432A is an advanced CMOS 8-bit microcontroller with 32 Kbytes of FLASH. This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This offers the following features: 32 Kbytes of FLASH, 256 bytes of IRAM, 768 bytes of XRAM, general purpose I/O, basic interval timer, watchdog timer, 8/16-bit timer/counter, 16-bit PPG output, 8-bit PWM output, 10-bit PWM output, watch timer, buzzer driving port, SPI, USI, 12-bit A/D converter, LCD driver, on-chip POR, LVR, LVI, on-chip oscillator and clock circuitry. The MC96F6432A also supports power saving modes to reduce power consumption.

Device Name	FLASH	XRAM	IRAM	ADC	I/O PORT	Package
MC96F6432AU	32Kbytes	768bytes	256bytes	16 inputs	42	48 QFN
MC96F6432AQ				16 inputs	42	44 MQFP
MC96F6332AL				12 inputs	30	32 LQFP
MC96F6332AD				12 inputs	30	32 SOP
MC96F6332AM				11 inputs	26	28 SOP
MC96F6232AU				8 inputs	22	24 QFN

**Table 1.1** Ordering Information of MC96F6432A



**Figure 1.1** Device Nomenclature

## 1.2 Features

- **CPU**
  - 8-bit CISC core (M8051, 2 clocks per cycle)
- **ROM (FLASH) Capacity**
  - 32Kbytes Flash with self-read and write capability
  - In-System Programming (ISP)
  - Endurance : 10,000 times (Sector 0~507)  
100,000 times (Sector 508~511)
  - Retention : 10 years
- **256bytes IRAM**
- **768bytes XRAM**
  - (27bytes including LCD display RAM)
- **General Purpose I/O (GPIO)**
  - Normal I/O : 9ports (P0[2:0], P5[5:0])
  - LCD shared I/O : 33ports (P0[7:3], P1, P2, P3, P4)
- **Timer/Counter**
  - Basic Interval Timer (BIT) 8-bit × 1-ch
  - Watch Dog Timer (WDT) 8-bit × 1-ch  
5kHz internal RC oscillator for WDT
  - 8-bit × 1-ch (T0), 16-bit × 2-ch (T1/T2)
  - 8-bit × 2-ch (T3/T4) or 16-bit × 1-ch (T3)
- **Programmable Pulse Generation**
  - Pulse generation (by T1/T2)
  - 8-bit PWM (by T0)
  - 6-ch 10-bit PWM for Motor (by T4)
- **Watch Timer (WT)**
  - 3.91ms/0.25s/0.5s/1s /1min interval at 32.768kHz
- **Buzzer**
  - 8-bit × 1-ch
- **SPI 2**
  - 8-bit × 1-ch
- **USI0/1 (UART + SPI + I2C)**
  - 8-bit UART × 2-ch, 8-bit SPI × 2-ch and I2C × 2-ch
- **12-bit A/D Converter**
  - 16 Input channels
- **LCD Driver**
  - 21segments and 8common terminals
  - Internal or external resistor bias
  - Two Internal Resistors Selectable
  - 1/2, 1/3, 1/4, 1/5, 1/6 and 1/8 duty selectable
  - Resistor Bias and 16-step contrast control
- **Power On Reset**
  - Reset release level (1.4V)
- **Low Voltage Reset**
  - 12 levels detect  
(1.85/ 2.20/ 2.32/ 2.44/ 2.59/ 2.75/ 2.93/ 3.14/ 3.38/  
3.67/ 4.00/ 4.40V)
- **Low Voltage Indicator**
  - 11 levels detect  
(2.20/ 2.32/ 2.44/ 2.59/ 2.75/ 2.93/ 3.14/ 3.38/ 3.67/  
4.00/ 4.40V)
- **Interrupt Sources**
  - External Interrupts  
(EINT0~7, EINT8, EINT10, EINT11, EINT12) (12)
  - Timer(0/1/2/3/4) (5)
  - WDT (1)
  - BIT (1)
  - WT (1)
  - SPI 2 (1)
  - USI0/1 (6)
  - ADC (1)
- **Internal RC Oscillator**
  - Internal RC frequency: 16MHz ±1.5% (TA= 0 ~ +50°C)
- **Power Down Mode**
  - STOP, IDLE mode
- **Operating Voltage and Frequency**
  - 2.2V~ 5.5V (@32 ~ 38kHz with Crystal)
  - 2.2V~ 5.5V (@0.4 ~ 4.2MHz with Crystal)
  - 2.7V~ 5.5V (@0.4 ~ 8.5MHz with Crystal)
  - 2.2V~ 5.5V (@0.5 ~ 16.0MHz with Internal RC)
  - Voltage dropout converter included for core
- **Minimum Instruction Execution Time**
  - 235ns (@8.5MHz main clock)
  - 61us (@ 32.768kHz sub clock)
- **Operating Temperature**
  - -40 ~ +85°C
- **Oscillator Type**
  - 0.4 – 8.5MHz Crystal or Ceramic for main clock
  - 32.768kHz Crystal for sub clock
- **Package Type**
  - 48 QFN
  - 44 MQFP-1010
  - 32 LQFP, 32 SOP
  - 28 SOP
  - 24 QFN
  - Pb-free package

### 1.3 Development tools

#### 1.3.1 Compiler

ABOV Semiconductor does not provide compiler. It is recommended that you consult a compiler provider. The MC96F6432A core is Mentor 8051 and the ROM size is smaller than 64 Kbytes. Therefore, developer can use the standard 8051 compiler from other providers.

#### 1.3.2 OCD(On-chip debugger) emulator and debugger

The OCD (On Chip Debug) emulator supports ABOV Semiconductor’s 8051 series MCU emulation. The OCD interface uses two-wire connection between PC and MCU which is attached to user’s system. The OCD can read or change the value of MCU internal memory and I/O peripherals. And the OCD also controls MCU internal debugging logic, it means OCD controls emulation, step run, monitoring, etc.

The OCD debugger program works on Microsoft-Windows NT, 2000, XP, Vista (32-bit) operating system. If you want to see more details, please refer to OCD debugger manual. You can download debugger S/W and manual from our web-site (<http://www.abov.co.kr>).

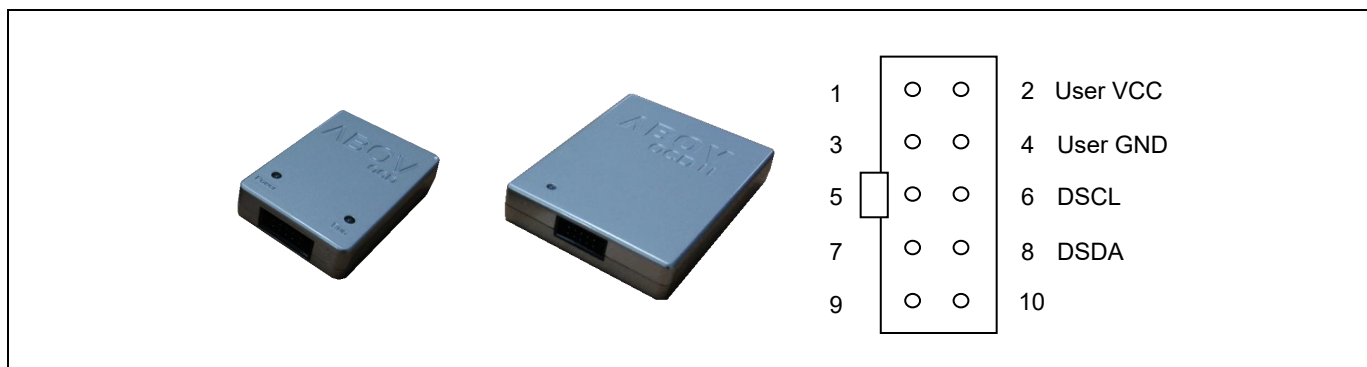
Connection:

- DSCL (MC96F6432 P01 port)
- DSDA (MC96F6432 P00 port)

**NOTE)**

1. MC96F6432A does not support the OCD function. MC96F6432 should be used for debugging.
2. Do not access to P0, P1, P2, P3, P4, P5 and EIFLAG0 registers through the “direct bit test and branch instructions” in the MC96F6432. Refer to the “MC96F6432 User’s Manual”.

OCD connector diagram: Connect OCD with user system



**Figure 1.2** Debugger(OCD1/OCD2) and Pin description

Subject	MC96F6432A	MC96F6432S	MC96F6432
On Chip Debugger (OCD)	Not supported	Not supported	Supported
Internal RC frequency (IRC)	Tolerance TA= 0°Cto+50°C : ±1.5% TA= -20°Cto+85°C : ±2.5% TA= -40°Cto+85°C : ±3.5%	Tolerance TA= 0°Cto+50°C : ±1.5% TA= -20°Cto+85°C : ±2.5% TA= -40°Cto+85°C : ±3.5%	Tolerance TA= 0°Cto+50°C : ±1.0% TA= -20°Cto+85°C : ±2.0% TA= -40°Cto+85°C : ±3.0%
x-tal filter selectable (XTFLSR Register)	x-tal filter selection register for noise immunity - 4.2MHz < x-tal ≤ 8.5MHz - x-tal ≤ 4.2MHz	Not supported	Not supported
LVR/LVI	12 Level Selectable - 1.85V, 2.2V,,,,, 4.4V	14 Level Selectable - 1.6V, 2.0V, 2.1V,,,,, 4.4V	14 Level Selectable - 1.6V, 2.0V, 2.1V,,,,, 4.4V
	11 Level Selectable - 2.2V,,,,, 4.4V	13 Level Selectable - 2.0V, 2.1V,,,,, 4.4V	13 Level Selectable - 2.0V, 2.1V,,,,, 4.4V
	LVR and LVI Current Both : 14.0(TYP)/24.0(MAX) uA One: 10.0(TYP)/18.0(MAX) uA	LVR and LVI Current Both : 14.0(TYP)/24.0(MAX) uA One: 10.0(TYP)/18.0(MAX) uA	LVR and LVI Current Both : 10.0(TYP)/15.0(MAX) uA One: 8.0(TYP)/12.0(MAX) uA
LCD	Internal LCD Bias Dividing Resistor Select - RLCD1 = 60kΩ - RLCD2 = 120kΩ	Internal LCD Bias Dividing Resistor Select - RLCD1 = 60kΩ - RLCD2 = 120kΩ	Internal LCD Bias Dividing Resistor - RLCD = 60kΩ
	RLCD1 - 40(MIN)/60(TYP)/80(MAX) kΩ RLCD2 - 80(MIN)/120(TYP)/160(MAX) kΩ	RLCD1 - 40(MIN)/60(TYP)/80(MAX) kΩ RLCD2 - 80(MIN)/120(TYP)/160(MAX) kΩ	RLCD - 40(MIN)/60(TYP)/80(MAX) kΩ
Vector Area Protection	En/Disable Vector Area(00H – FFH) Protection	Not supported	Not supported
Specific Area for Write Protection	8 kinds of protection size selectable - Address 0100H – 03FFH - Address 0100H – 07FFH - Address 0100H – 0BFFH - Address 0100H – 0FFFH - Address 0100H – 77FFH - Address 0100H – 7BFFH - Address 0100H – 7DFFH - Address 0100H – 7EFFH	4 kinds of protection size selectable - Address 0100H – 0FFFH - Address 0100H – 07FFH - Address 0100H – 03FFH - Address 0100H – 01FFH	4 kinds of protection size selectable - Address 0100H – 0FFFH - Address 0100H – 07FFH - Address 0100H – 03FFH - Address 0100H – 01FFH
ADC	A/D Converter INL : ±6LSB DNL : ±1 LSB TOE : ±5 LSB ZOE : ±5 LSB	A/D Converter INL : ±6LSB DNL : ±1 LSB TOE : ±5 LSB ZOE : ±5 LSB	A/D Converter INL : ±4LSB DNL : ±1 LSB TOE : ±3 LSB ZOE : ±3 LSB
Supply Current IDD3 (Sub operation)	Typ/Max : 90/180 [uA] - 32.768kHz, VDD=3V±10%, TA=25°C	Typ/Max : 60/90 [uA] - 32.768kHz, VDD=3V±10%, TA=25°C	Typ/Max : 50/80 [uA] - 32.768kHz, VDD=3V±10%, TA=25°C
Operating Voltage and Frequency	VDD: 2.2V to 5.5V, Freq.: Up to 16MHz - 2.2V to 5.5V @ 32 to 38kHz with x-tal - 2.2V to 5.5V @ 0.4 to 4.2MHz with x-tal - 2.7V to 5.5V @ 0.4 to 8.5MHz with x-tal - 2.2V to 5.5V @ 0.5 to 16MHz with IRC	VDD: 1.8V to 5.5V, Freq.: Up to 16MHz - 1.8V to 5.5V @ 32 to 38kHz with x-tal - 1.8V to 5.5V @ 0.4 to 4.2MHz with x-tal - 2.7V to 5.5V @ 0.4 to 10MHz with x-tal - 3.0V to 5.5V @ 0.4 to 12MHz with x-tal - 1.8V to 5.5V @ 0.5 to 8MHz with IRC - 2.0V to 5.5V @ 0.5 to 16MHz with IRC	VDD: 1.8V to 5.5V, Freq.: Up to 16MHz - 1.8V to 5.5V @ 32 to 38kHz with x-tal - 1.8V to 5.5V @ 0.4 to 4.2MHz with x-tal - 2.7V to 5.5V @ 0.4 to 10MHz with x-tal - 3.0V to 5.5V @ 0.4 to 12MHz with x-tal - 1.8V to 5.5V @ 0.5 to 8MHz with IRC - 2.0V to 5.5V @ 0.5 to 16MHz with IRC
Power-On Reset Characteristics	VDD Voltage Rising Time Min/Max : 0.05/30.0[V/ms]	VDD Voltage Rising Time Min/Max : 0.05/30.0[V/ms]	VDD Voltage Rising Time Min/Max : 0.05/5.0[V/ms]
Full-flash erase mode method	Sector erase mode	Sector erase mode	Sector and byte erase mode

Table 1.2 Difference among MC96F6432A, MC96F6432S and MC96F6432

### 1.3.3 Programmer

Single programmer:

E-PGM+ : It programs MCU device directly.

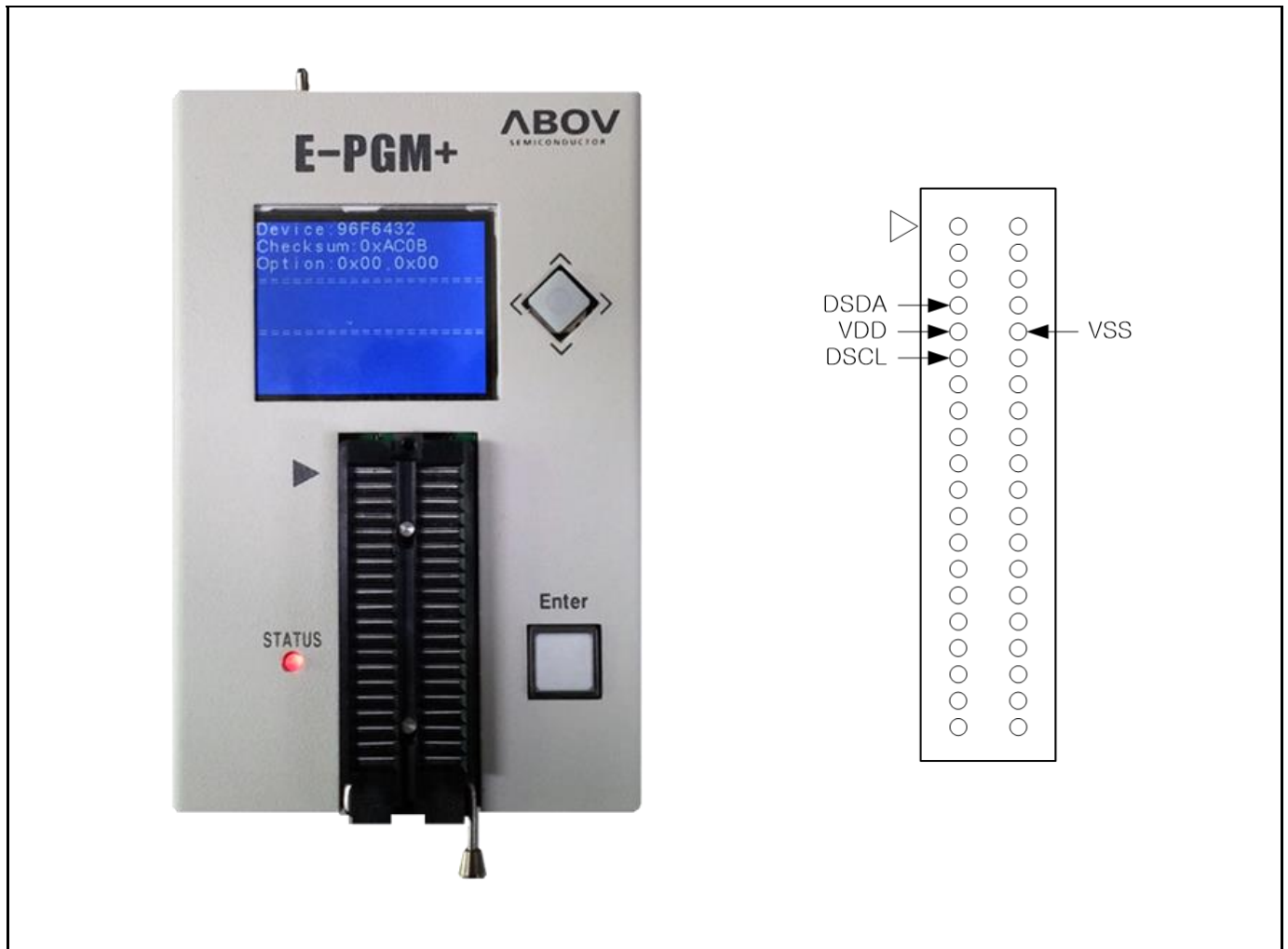
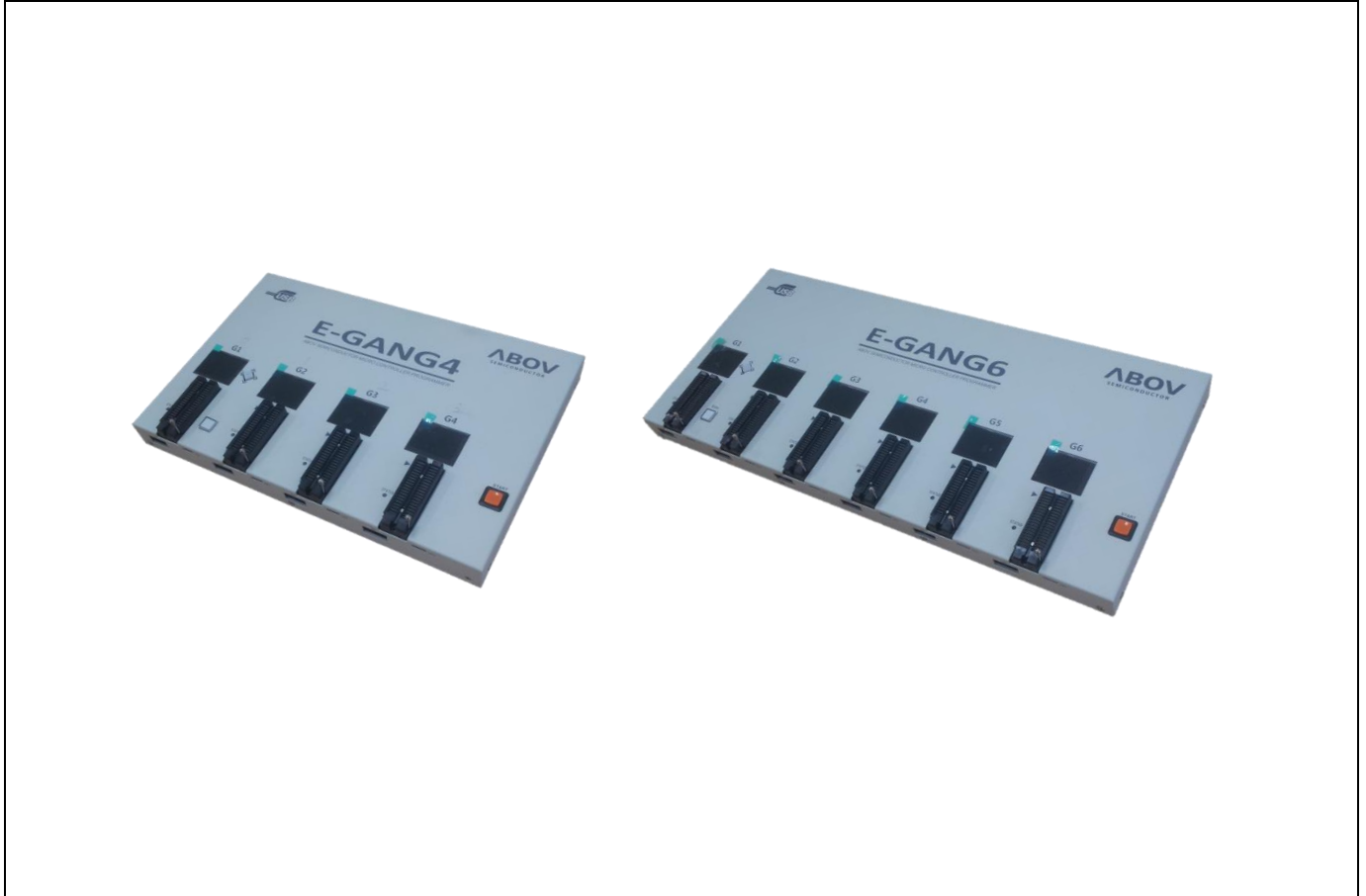


Figure 1.3 E-PGM+(Single writer)

Gang programmer: E-GANG4 and E-GANG6

- It can run PC controlled mode.
- It can run standalone without PC control too.
- USB interface is supported.
- Easy to connect to the handler.



**Figure 1.4** E-GANG4 and E-GANG6 (for Mass Production)



## 1.4 MTP programming

### 1.4.1 Overview

The program memory of MC96F6432A is MTP Type. This flash is accessed by serial data format. There are four pins(DSCL, DSDA, VDD and VSS) for programming/reading the flash.

Pin name	Main chip pin name	During programming	
		I/O	Description
DSCL	P01	I	Serial clock pin. Input only pin.
DSDA	P00	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	-	Logic power supply pin.

**Table 1.3** Descriptions of pins which are used to programming/reading the Flash

### 1.4.2 On-Board programming

The MC96F6432A needs only four signal lines including VDD and VSS pins for programming FLASH with serial communication protocol. Therefore the on-board programming is possible if the programming signal lines are ready at the PCB of application board is designed.

#### 1.4.2.1 Circuit Design Guide

At the FLASH programming, the programming tool needs 4 signal lines that are DSCL, DSDA, VDD and VSS. When you design the PCB circuits, you should consider the usage of these signal lines for the on-board programming.

Please be careful to design the related circuit of these signal pins because rising/falling timing of DSCL and DSDA is very important for proper programming.

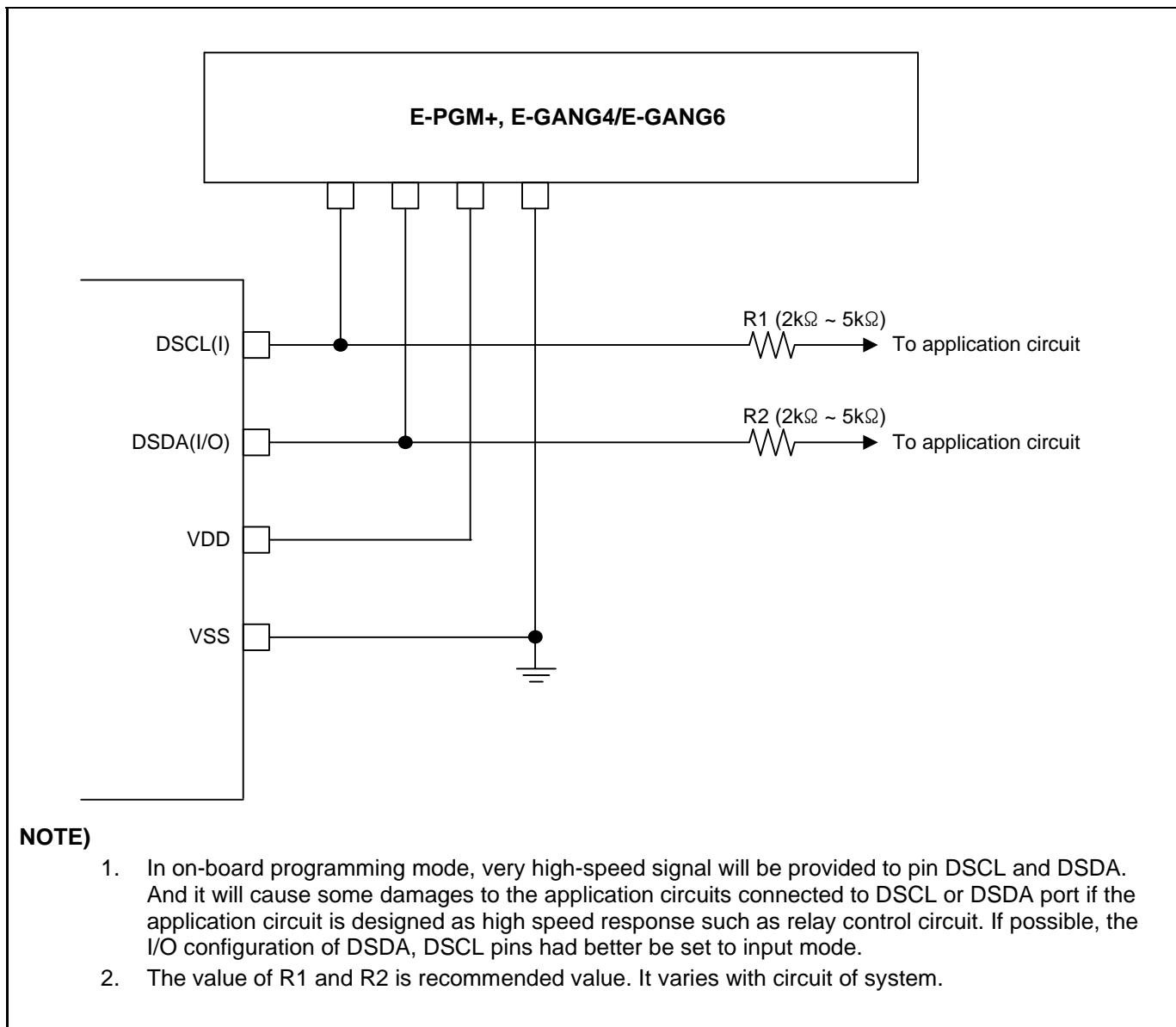


Figure 1.5 PCB design guide for on board programming

## 2 Block diagram

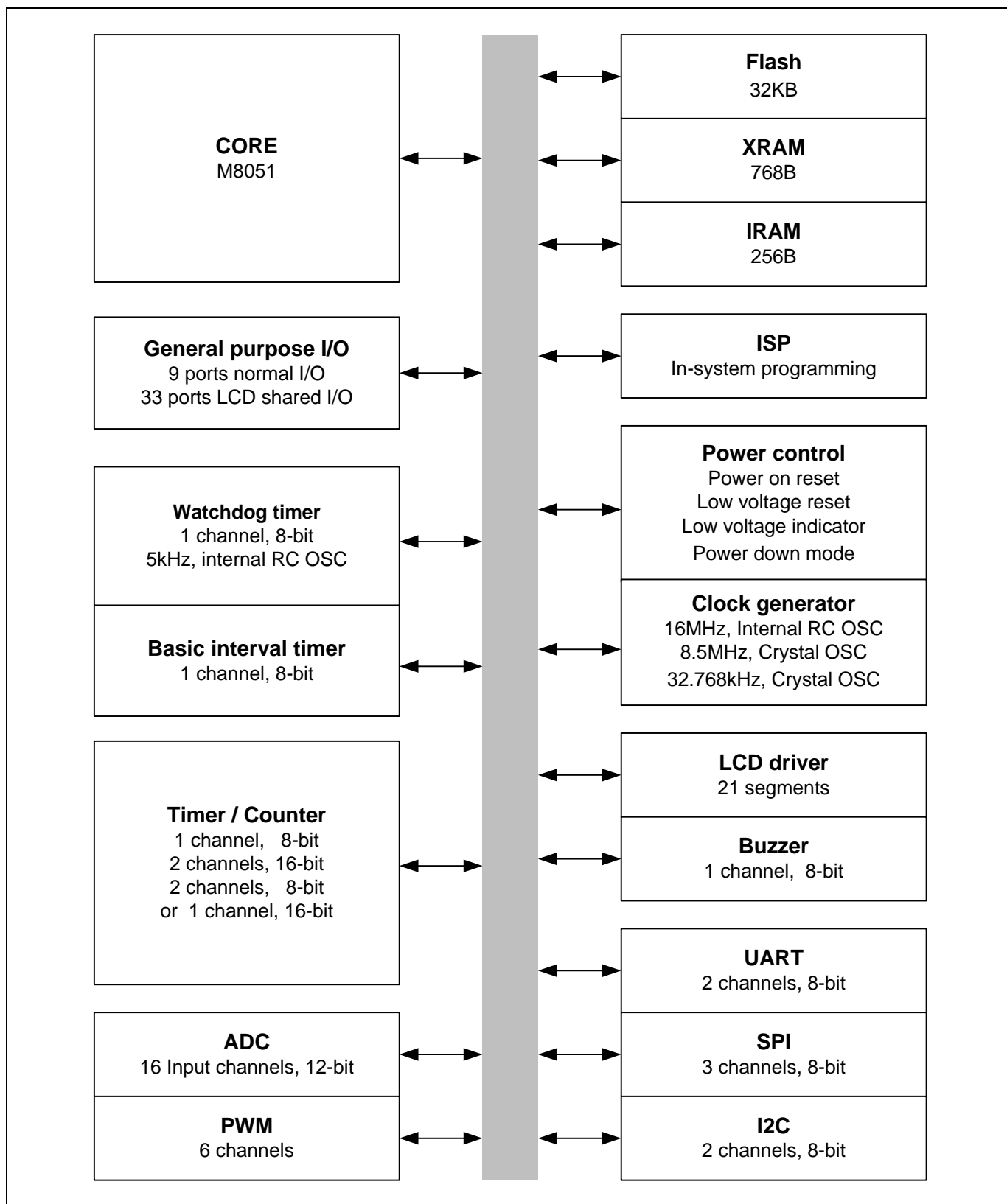
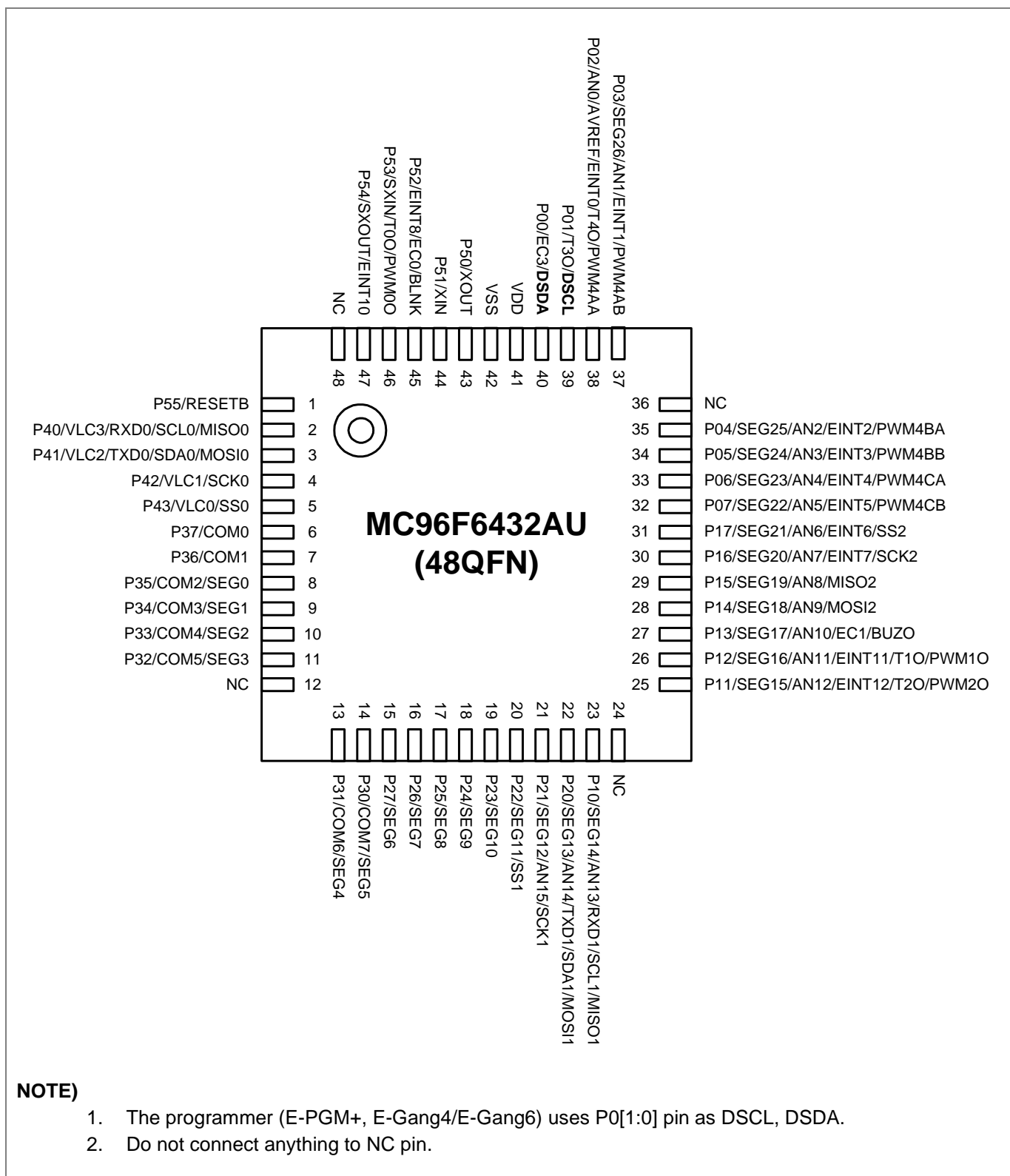


Figure 2.1 Block diagram of MC96F6432A

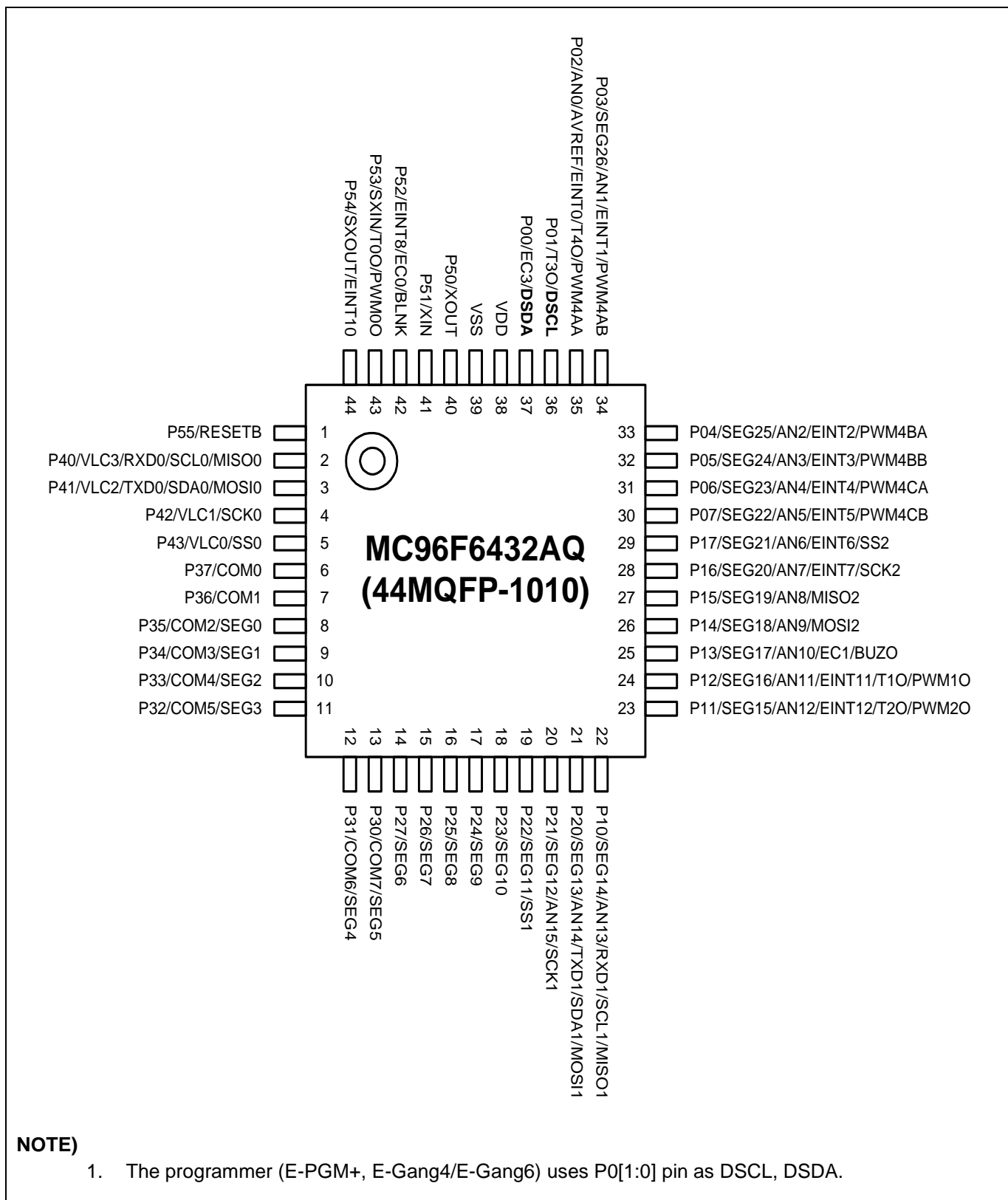
### 3 Pin assignment



**NOTE)**

1. The programmer (E-PGM+, E-Gang4/E-Gang6) uses P0[1:0] pin as DSCL, DSDA.
2. Do not connect anything to NC pin.

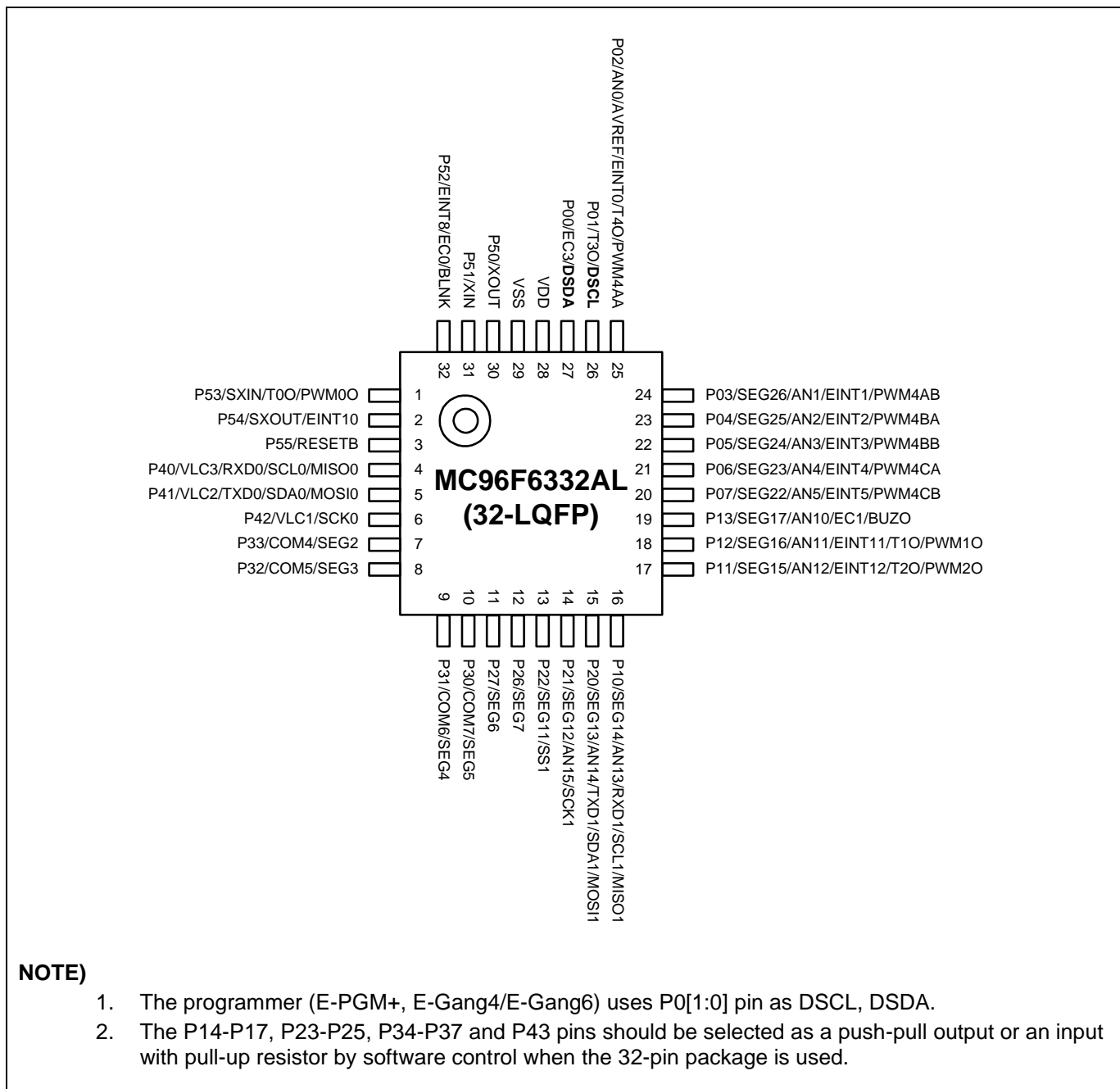
Figure 3.1 MC96F6432AU 48QFN pin assignment



**NOTE)**

1. The programmer (E-PGM+, E-Gang4/E-Gang6) uses P0[1:0] pin as DSCL, DSDA.

**Figure 3.2** MC96F6432AQ 44MQFP-1010 pin assignment



**NOTE)**

1. The programmer (E-PGM+, E-Gang4/E-Gang6) uses P0[1:0] pin as DSCL, DSDA.
2. The P14-P17, P23-P25, P34-P37 and P43 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 32-pin package is used.

**Figure 3.3** MC96F6432AL 32LQFP-0707 pin assignment

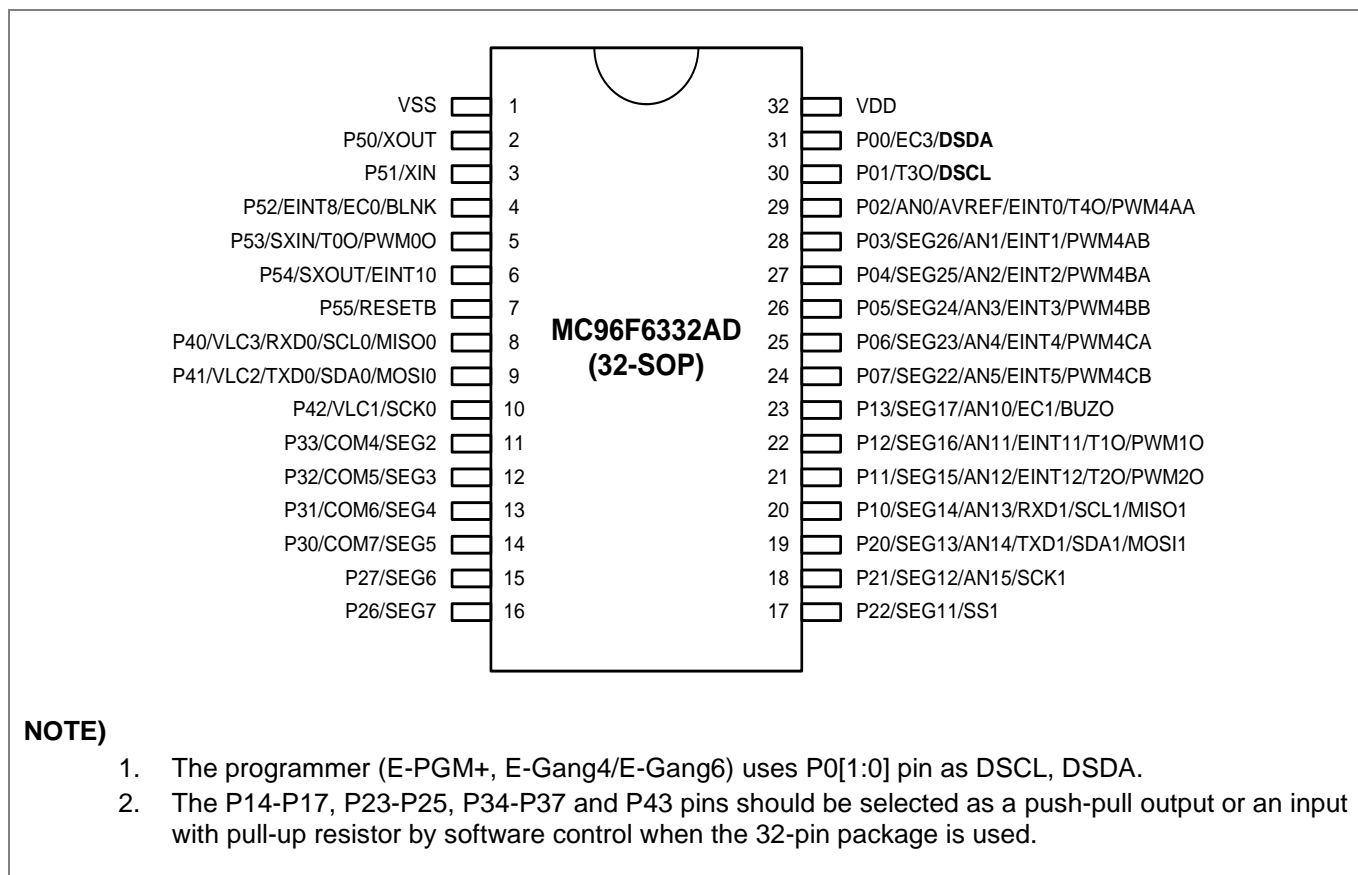


Figure 3.4 MC96F6332AD 32SOP pin assignment

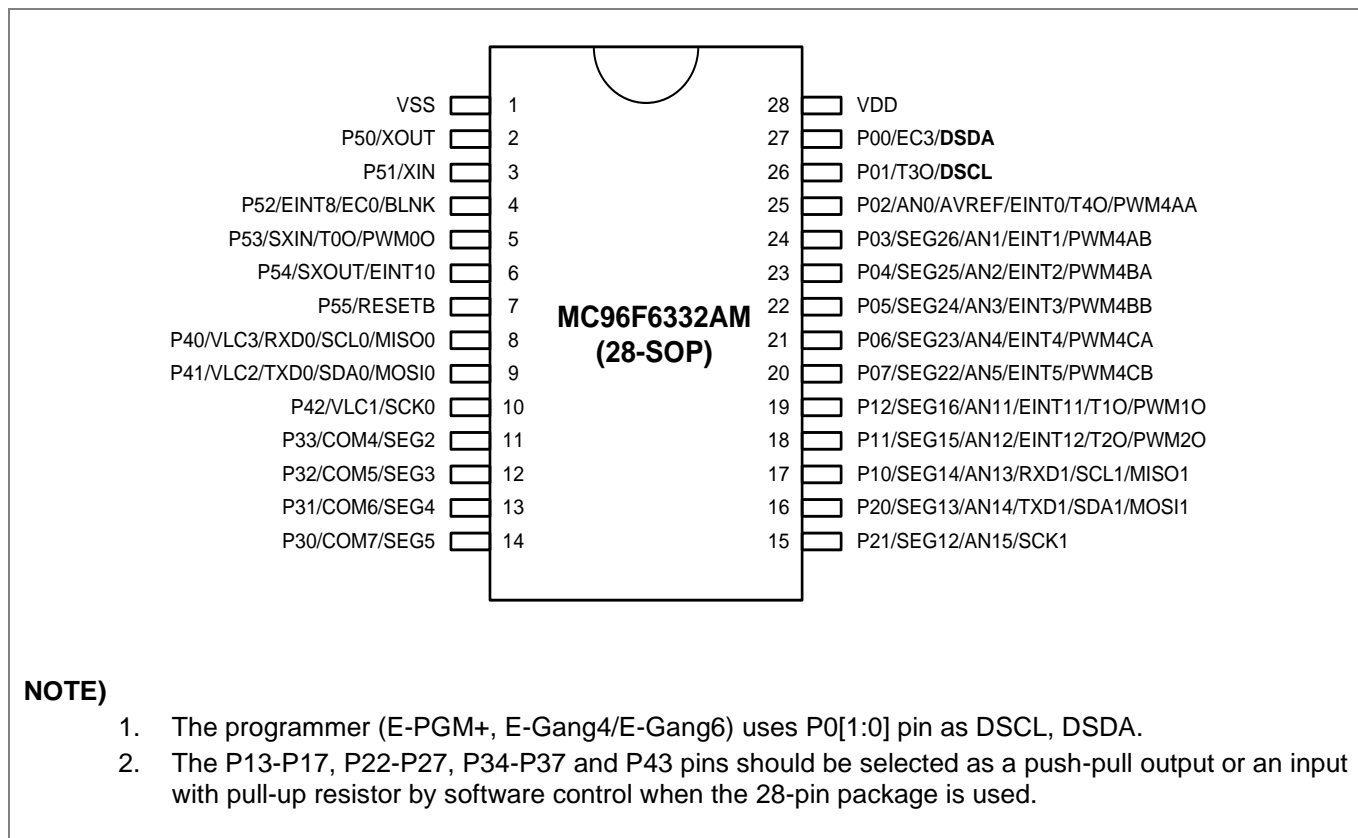


Figure 3.5 MC96F6332AM 28SOP pinassignment

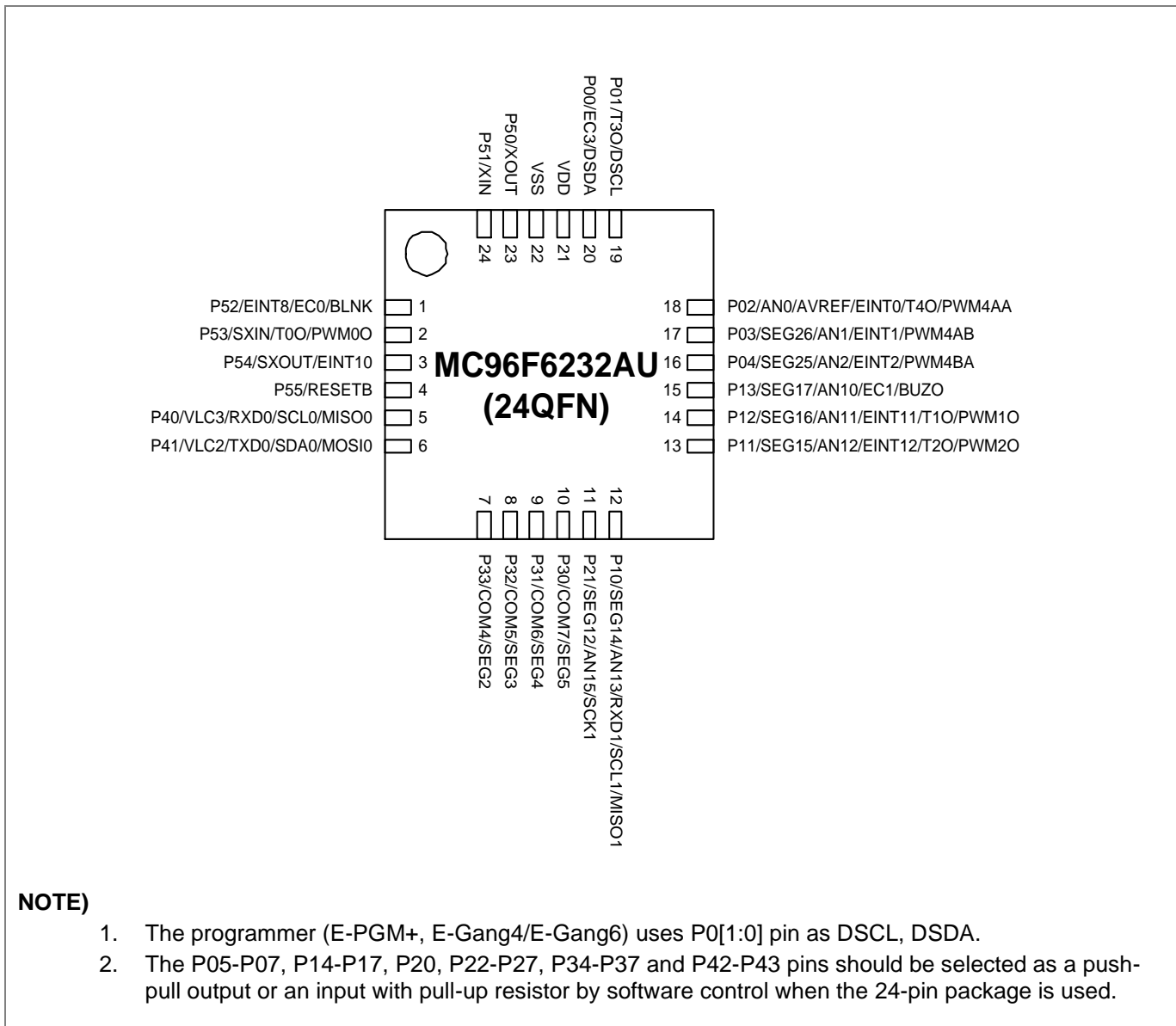
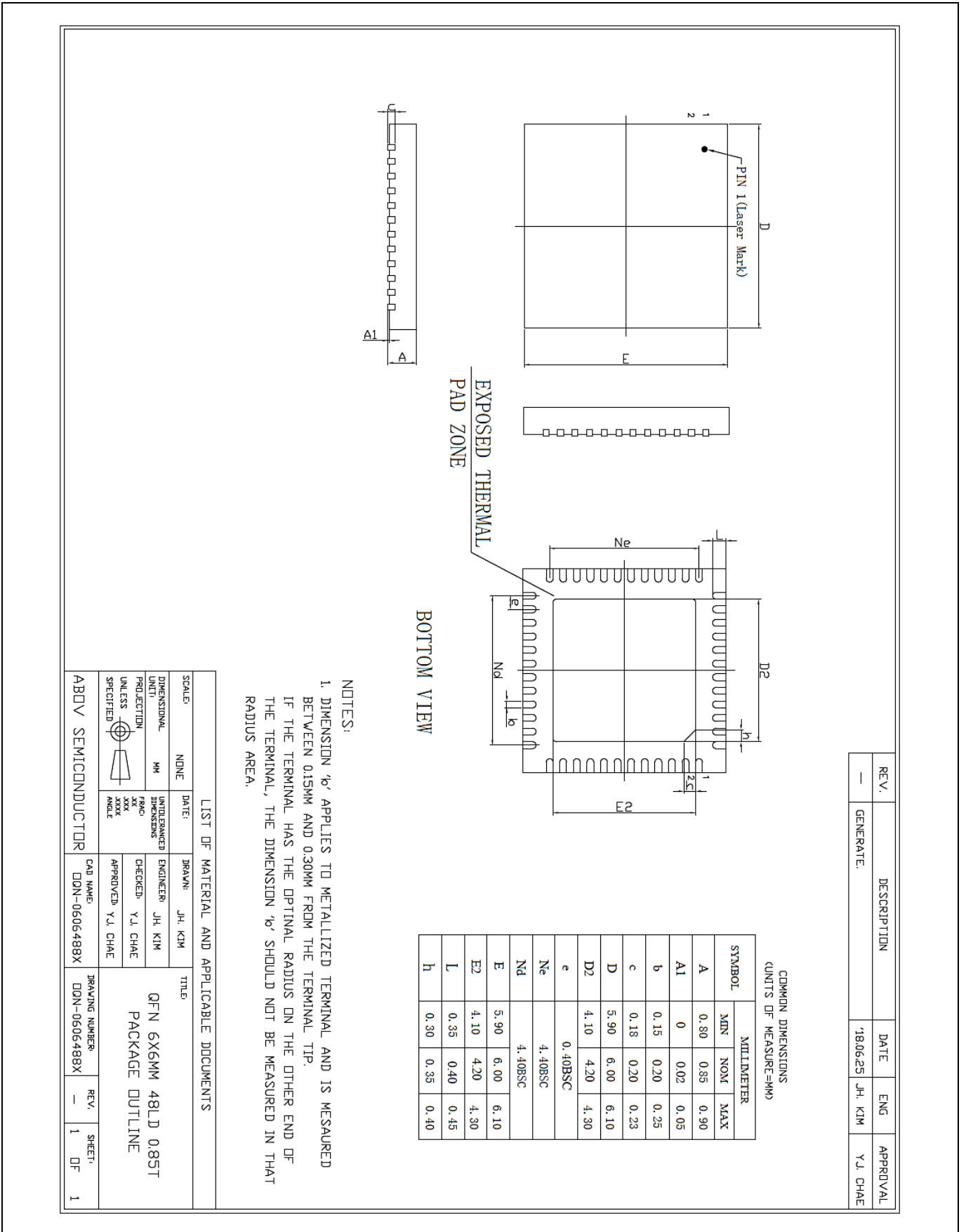


Figure 3.6 MC96F6232AU 24QFN pin assignment



# 4 Package Diagram



REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	'1806.25	JH. KIM	Y.J. CHAE

COMMON DIMENSIONS  
(UNITS OF MEASURE=MM)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.23
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.40BSC		
Ne	4.40BSC		
Nd	4.40BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40

BOTTOM VIEW

EXPOSED THERMAL PAD ZONE

NOTES:

1. DIMENSION 'b' APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIMAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION 'b' SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE	NONE	DATE	DRAWN	JH. KIM	TITLE
DIMENSIONAL UNIT	MM	INTOLERANCES	ENGINEER	JH. KIM	QFN 6X6MM 48LD 08ST PACKAGE OUTLINE
PROJECTION	1ST ANGLE	FRAC. DIMENSIONS	CHECKED	Y.J. CHAE	
UNLESS SPECIFIED	AS SHOWN	ANGLE	APPROVED	Y.J. CHAE	
ABOV SEMICONDUCTOR		CAD NAME	QFN-0606488X	DRAWING NUMBER	
				REV.	—
				SHEET	1 OF 1

Figure 4.1 48-Pin QFN Package

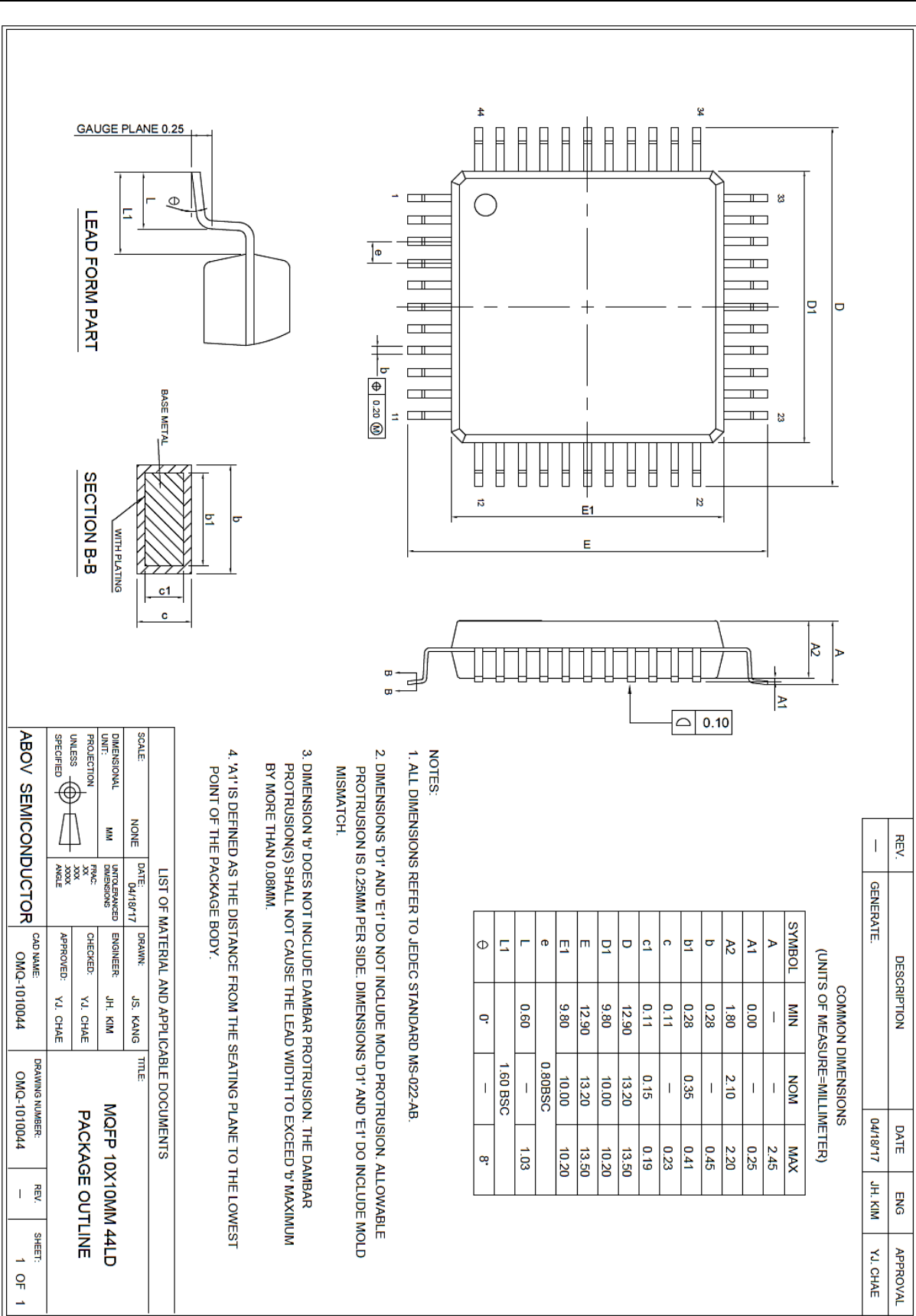


Figure 4.2 44-Pin MQFP Package

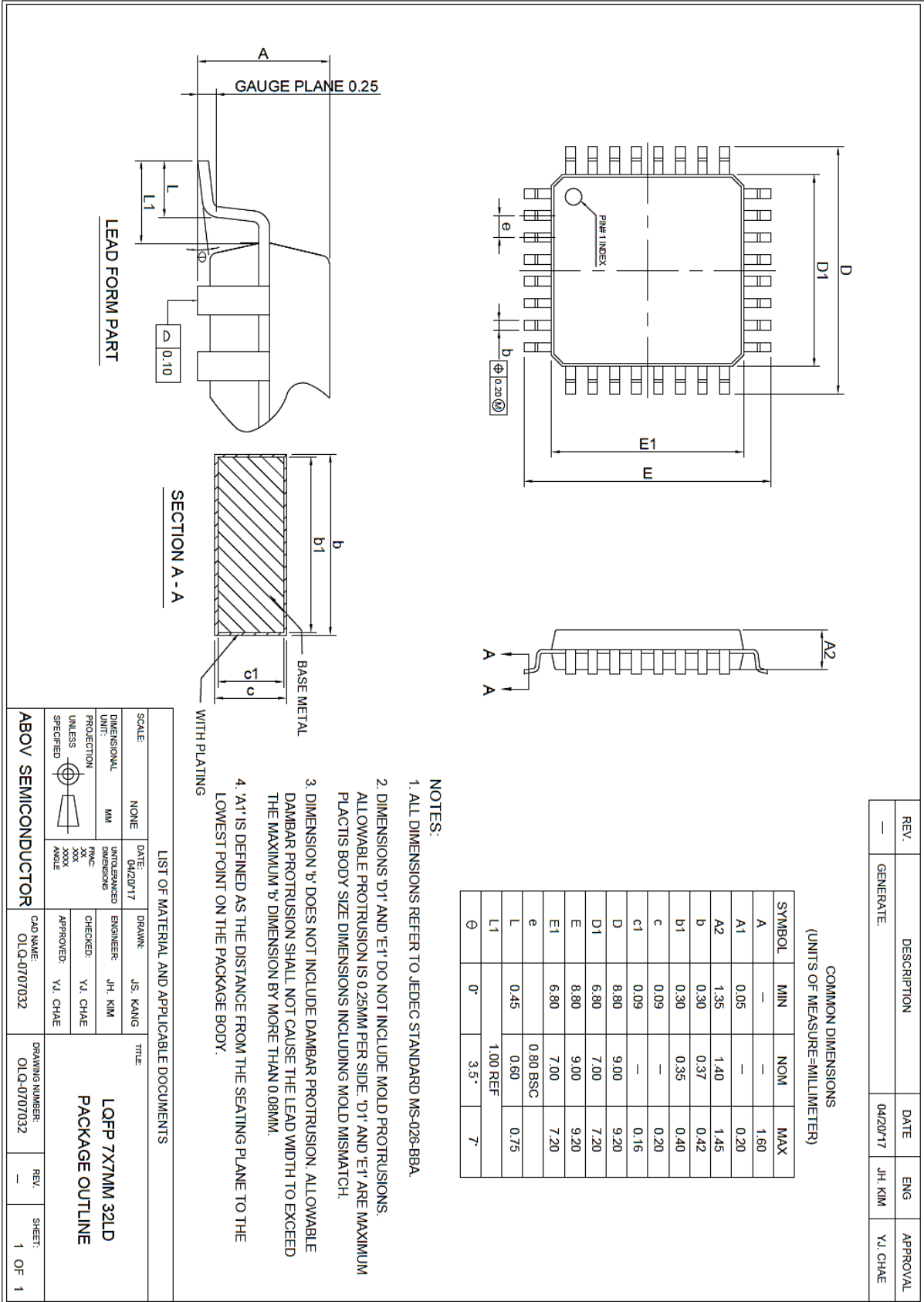


Figure 4.3 32-Pin LQFP Package

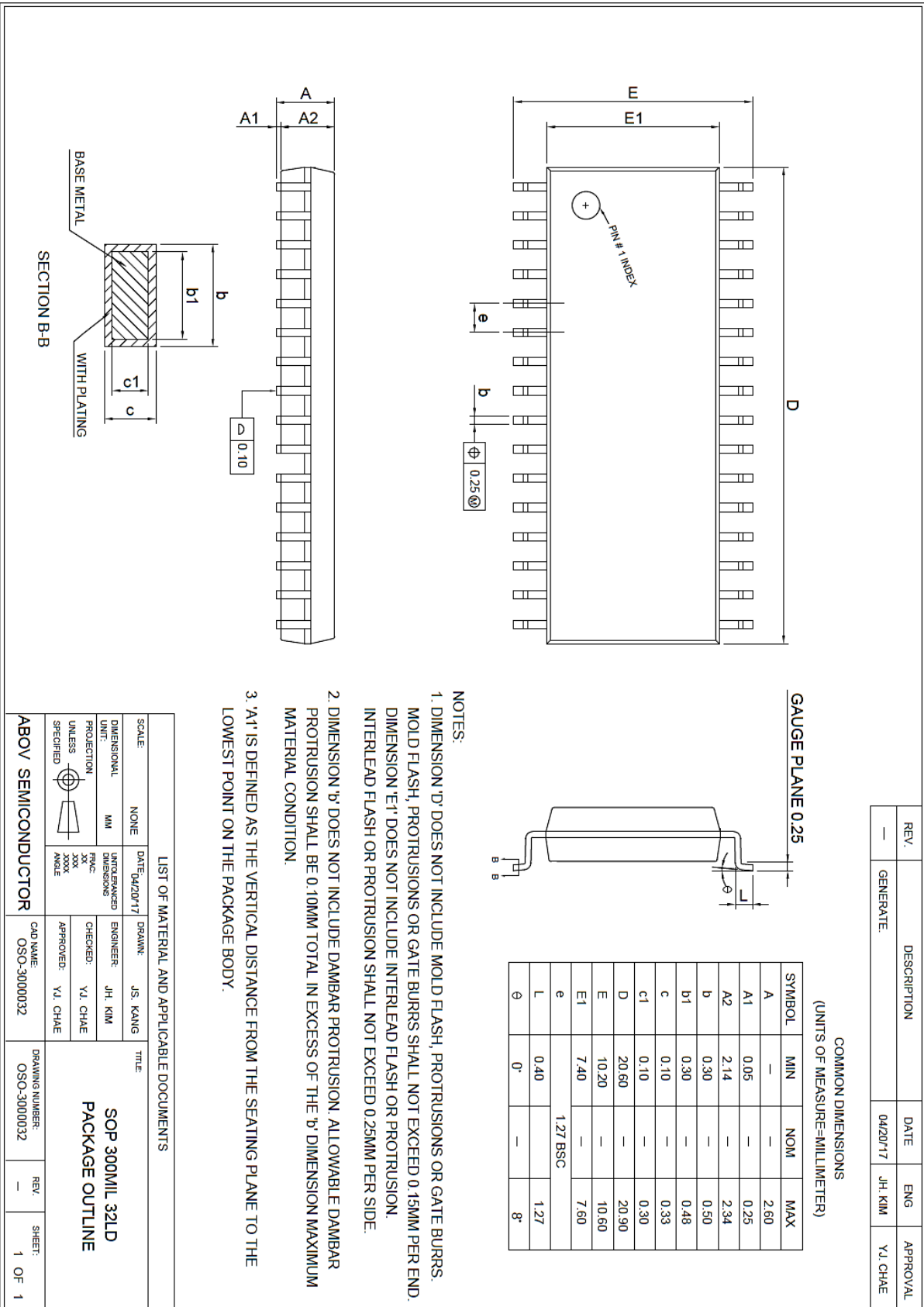


Figure 4.4 32-Pin SOP Package

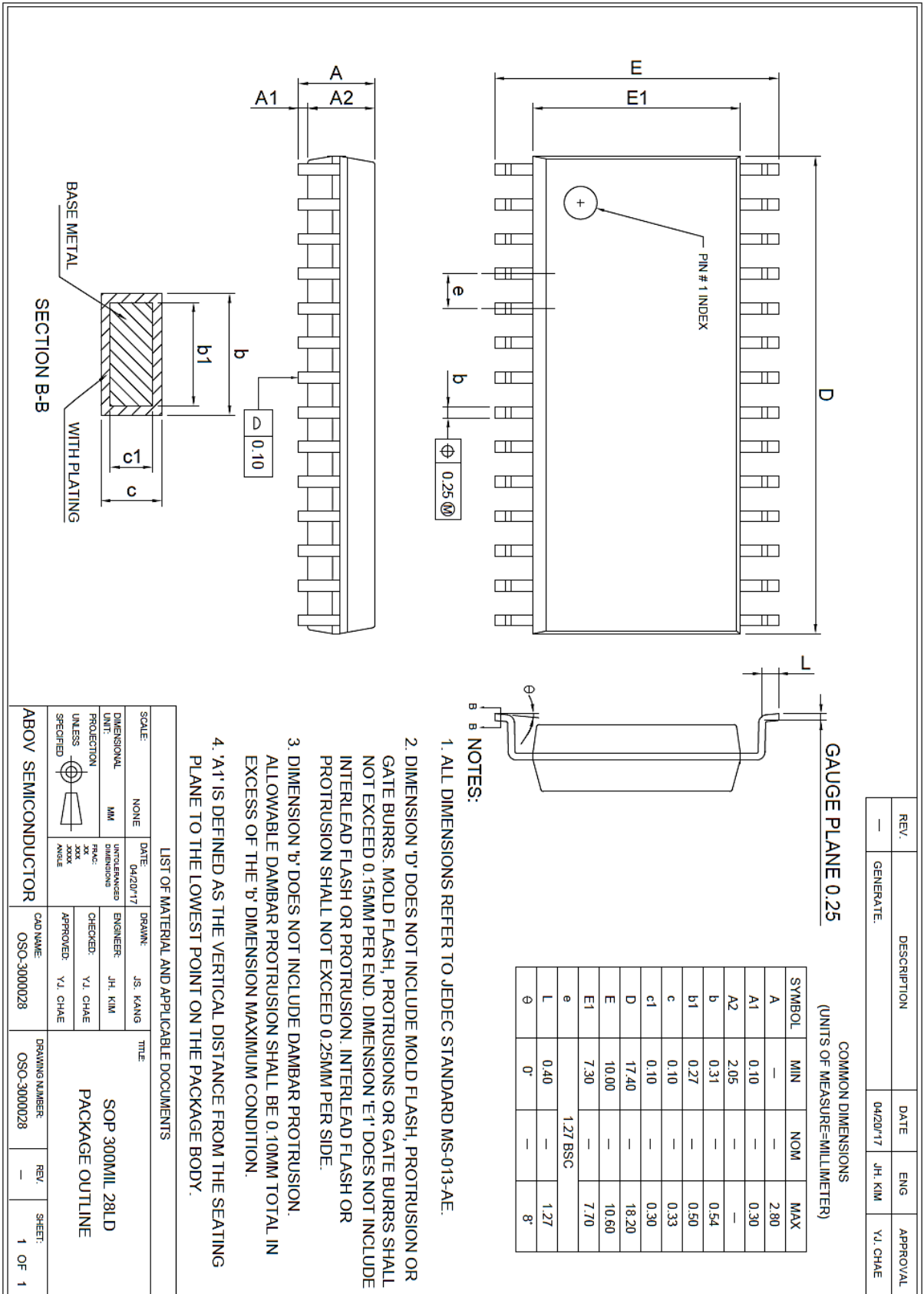


Figure 4.5 28-Pin SOP Package

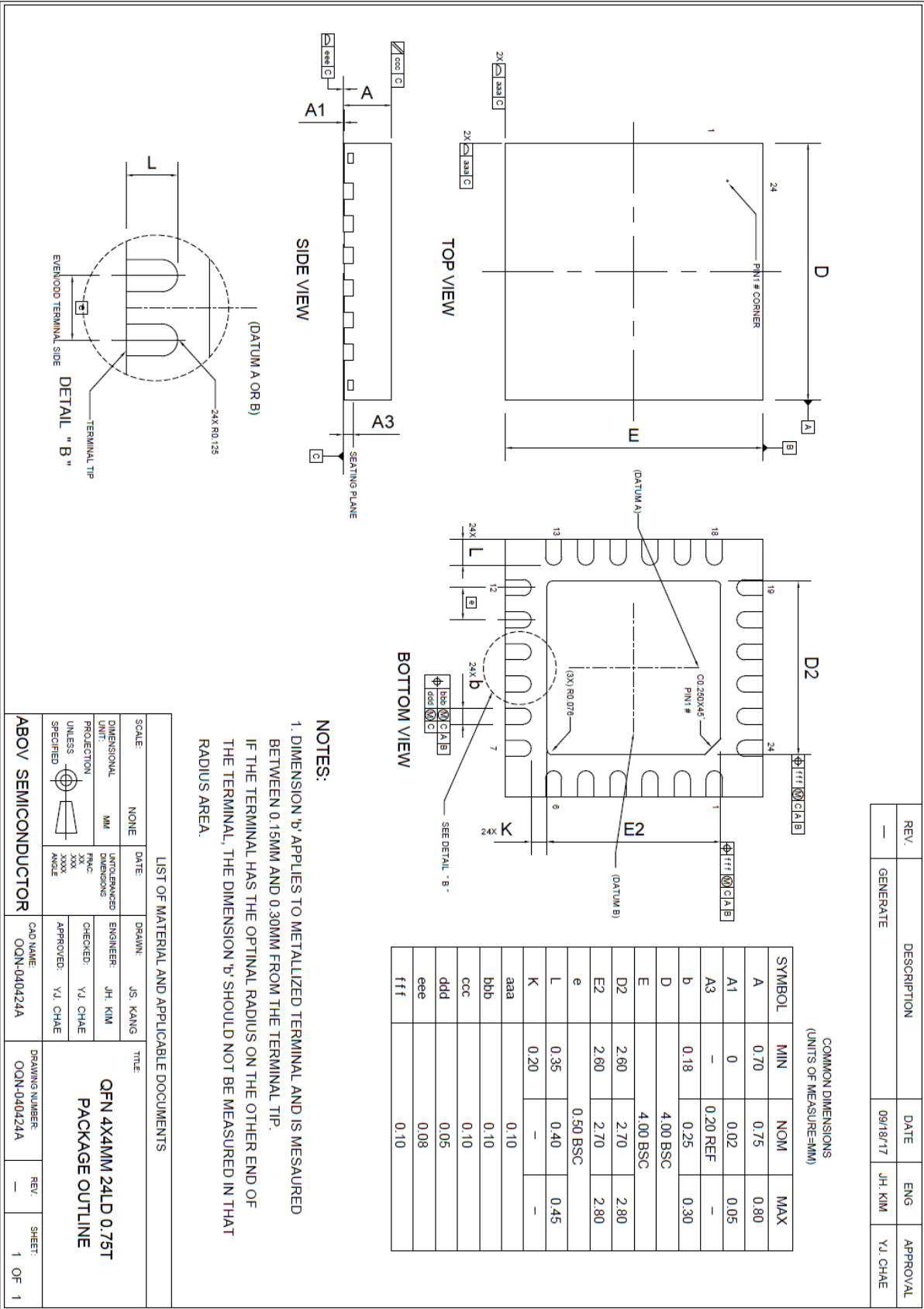


Figure 4.6 24-Pin QFN Package

## 5 Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	Port 0 is a bit-programmable I/O port which can be configured as a Schmitt-trigger input, a push-pull output or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P05 – P07 are not in the 24-pin package.	Input	EC3/DSDA
P01				T30/DSCL
P02				AN0/AVREF/EINT0/T4O/PWM4AA
P03				SEG26/AN1/EINT1/PWM4AB
P04				SEG25/AN2/EINT2/PWM4BA
P05				SEG24/AN3/EINT3/PWM4BB
P06				SEG23/AN4/EINT4/PWM4CA
P07				SEG22/AN5/EINT5/PWM4CB
P10	I/O	Port 1 is a bit-programmable I/O port which can be configured as a Schmitt-trigger input, a push-pull output or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P14 – P17 are not in the 32-pin package. The P13 – P17 are not in the 28-pin package. The P14 – P17 are not in the 24-pin package.	Input	SEG14/AN13/RXD1/SCL1/MISO1
P11				SEG15/AN12/EINT12/T2O/PWM2O
P12				SEG16/AN11/EINT11/T1O/PWM1O
P13				SEG17/AN10/EC1/BUZO
P14				SEG18/AN9/MOSI2
P15				SEG19/AN8/MISO2
P16				SEG20/AN7/EINT7/SCK2
P17				SEG21/AN6/EINT6/SS2
P20	I/O	Port 2 is a bit-programmable I/O port which can be configured as an input, a push-pull output or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P23 – P25 are not in the 32-pin package. The P22 – P27 are not in the 28-pin package. The P20, P22 – P27 are not in the 24-pin package.	Input	SEG13/AN14/TXD1/SDA1/MOSI1
P21				SEG12/AN15/SCK1
P22				SEG11/SS1
P23				SEG10
P24				SEG9
P25				SEG8
P26				SEG7
P27				SEG6
P30	I/O	Port 3 is a bit-programmable I/O port which can be configured as an input, a push-pull output. A pull-up resistor can be specified in 1-bit unit. The P34 – P37 are only in the 32-pin package. The P34 – P37 are not in the 28-pin package. The P34 – P37 are not in the 24-pin package.	Input	COM7/SEG5
P31				COM6/SEG4
P32				COM5/SEG3
P33				COM4/SEG2
P34				COM3/SEG1
P35				COM2/SEG0
P36				COM1
P37				COM0
P40	I/O	Port 4 is a bit-programmable I/O port which can be configured as an input, a push-pull output or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P43 is not in the 32-pin package. The P43 is not in the 28-pin package. The P42 – P43 are not in the 24-pin package.	Input	VLC3/RXD0/SCL0/MISO0
P41				VLC2/TXD0/SDA0/MOSI0
P42				VLC1/SCK0
P43				VLC0/SS0

**Table 5.1** Normal Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P50	I/O	Port 5 is a bit-programmable I/O port which can be configured as a Schmitt-trigger input or a push-pull output. A pull-up resistor can be specified in 1-bit unit.	Input	XOUT
P51				XIN
P52				EINT8/EC0/BLNK
P53				SXIN/T0O/PWM0O
P54				SXOUT/EINT10
P55				RESETB
EINT0	I/O	External interrupt input and Timer 3 capture input	Input	P02/AN0/AVREF/T4O/PWM4AA
EINT1	I/O	External interrupt input and Timer 4 capture input	Input	P03/SEG26/AN1/PWM4AB
EINT2	I/O	External interrupt inputs	Input	P04/SEG25/AN2/PWM4BA
EINT3				P05/SEG24/AN3/PWM4BB
EINT4				P06/SEG23/AN4/PWM4CA
EINT5				P07/SEG22/AN5/PWM4CB
EINT6				P17/SEG21/AN6/SS2
EINT7				P16/SEG20/AN7/SCK2
EINT8				P52/EC0/BLNK
EINT10	I/O	External interrupt input and Timer 0 capture input	Input	P54/SXOUT
EINT11	I/O	External interrupt input and Timer 1 capture input	Input	P12/SEG16/AN11/T1O/PWM1O
EINT12	I/O	External interrupt input and Timer 2 capture input	Input	P11/SEG15/AN12/T2O/PWM2O
T0O	I/O	Timer 0 interval output	Input	P53/SXIN/PWM0O
T1O	I/O	Timer 1 interval output	Input	P12/SEG16/AN11/EINT11/PWM1O
T2O	I/O	Timer 2 interval output	Input	P11/SEG15/AN12/EINT12/PWM2O
T3O	I/O	Timer 3 interval output	Input	P01/DSCL
T4O	I/O	Timer 4 interval output	Input	P02/AN0/AVREF/EINT0/PWM4AA
PWM0O	I/O	Timer 0 PWM output	Input	P53/SXIN/T0O
PWM1O	I/O	Timer 1 PWM output	Input	P12/SEG16/AN11/EINT11/T1O
PWM2O	I/O	Timer 2 PWM output	Input	P11/SEG15/AN12/EINT12/T2O
PWM4AA	I/O	Timer 4 PWM outputs	Input	P02/AN0/AVREF/EINT0/T4O
PWM4AB				P03/SEG26/AN1/EINT1
PWM4BA				P04/SEG25/AN2/EINT2
PWM4BB				P05/SEG24/AN3/EINT3
PWM4CA				P06/SEG23/AN4/EINT4
PWM4CB				P07/SEG22/AN5/EINT5
BLNK	I/O	External sync signal input for 6-ch PWMs	Input	P52/EINT8/EC0
EC0	I/O	Timer 0 event count input	Input	P52/EINT8/BLNK
EC1	I/O	Timer 1 event count input	Input	P13/SEG17/AN10
EC3	I/O	Timer 3 event count input	Input	P00/DSDA

Table 5.2 Normal Pin Description (continue)



PIN Name	I/O	Function	@RESET	Shared with
BUZO	I/O	Buzzer signal output	Input	P13/SEG17/AN10/EC1
SCK0	I/O	Serial 0 clock input/output	Input	P42/VLC1
SCK1	I/O	Serial 1 clock input/output	Input	P21/SEG12/AN15
SCK2	I/O	Serial 2 clock input/output	Input	P16/SEG20/AN7/EINT7
MOSI0	I/O	SPI 0 master output, slave input	Input	P41/VLC2/TXD0/SDA0
MOSI1	I/O	SPI 1 master output, slave input	Input	P20/SEG13/AN14/TXD1/SDA1
MOSI2	I/O	SPI 2 master output, slave input	Input	P14/SEG18/AN9
MISO0	I/O	SPI 0 master input, slave output	Input	P40/VLC3/RXD0/SCL0
MISO1	I/O	SPI 1 master input, slave output	Input	P10/SEG14/AN13/RXD1/SCL1
MISO2	I/O	SPI 2 master input, slave output	Input	P15/SEG19/AN8
SS0	I/O	SPI 0 slave select input	Input	P43/VLC0
SS1	I/O	SPI 1 slave select input	Input	P22/SEG11
SS2	I/O	SPI 2 slave select input	Input	P17/SEG21/AN6/EINT6
TXD0	I/O	UART 0 data output	Input	P41/VLC2/SDA0/MOSI0
TXD1	I/O	UART 1 data output	Input	P20/SEG13/AN14/SDA1/MOSI1
RXD0	I/O	UART 0 data input	Input	P40/VLC3/SCL0/MISO0
RXD1	I/O	UART 1 data input	Input	P10/SEG14/AN13/SCL1/MISO1
SCL0	I/O	I2C 0 clock input/output	Input	P40/VLC3/RXD0/MISO0
SCL1	I/O	I2C 1 clock input/output	Input	P10/SEG14/AN13/RXD1/MISO1
SDA0	I/O	I2C 0 data input/output	Input	P41/VLC2/TXD0/MOSI0
SDA1	I/O	I2C 1 data input/output	Input	P20/SEG13/AN14/TXD1/MOSI1
AVREF	I/O	A/D converter reference voltage	Input	P02/AN0/EINT0/T4O/PWM4AA
AN0	I/O	A/D converter analog input channels	Input	P02/AVREF/EINT0/T4O/PWM4AA
AN1				P03/SEG26/EINT1/PWM4AB
AN2				P04/SEG25/EINT2/PWM4BA
AN3				P05/SEG24/EINT3/PWM4BB
AN4				P06/SEG23/EINT4/PWM4CA
AN5				P07/SEG22/EINT5/PWM4CB
AN6				P17/SEG21/EINT6/SS2
AN7				P16/SEG20/EINT7/SCK2
AN8				P15/SEG19/MISO2
AN9				P14/SEG18/MOSI2
AN10				P13/SEG17/EC1
AN11				P12/SEG16/EINT11/T10/PWM1O
AN12				P11/SEG15/EINT12/T2O/PWM2O
AN13				P10/SEG14/RXD1/SCL1/MISO1
AN14				P20/SEG13/TXD1/SDA1/MOSI1
AN15	P21/SEG12/SCK1			

Table 5.3 Normal Pin Description (continue)

PIN Name	I/O	Function	@RESET	Shared with
VLC0	I/O	LCD bias voltage pins	Input	P43/SS0
VLC1				P42/SCK0
VLC2				P41/TXD0/SDA0/MOSI0
VLC3				P40/RXD0/SCL0/MISO0
COM0 COM1	I/O	LCD common signal outputs	Input	P37–P36
COM2– COM3				P35–P34/SEG0–SEG1
COM4– COM7				P33–P30/SEG2–SEG5
SEG0– SEG1	I/O	LCD segment signal outputs	Input	P35–P34/COM2–COM3
SEG2– SEG5				P33–P30/COM4–COM7
SEG6– SEG10				P27–P23
SEG11				P22/SS1
SEG12				P21/SCK1/AN15
SEG13				P20/AN14/TXD1/SDA1/MOSI1
SEG14				P10/AN13/RXD1/SCL1/MISO1
SEG15				P11/AN12/EINT12/T2O/PWM2O
SEG16				P12/AN11/EINT11/T1O/PWM1O
SEG17				P13/AN10/EC1
SEG18				P14/AN9/MOSI2
SEG19				P15/AN8/MISO2
SEG20				P16/AN7/EINT7/SCK2
SEG21				P17/AN6/EINT6/SS2
SEG22				P07/AN5/EINT5/PWM4CB
SEG23				P06/AN4/EINT4/PWM4CA
SEG24				P05/AN3/EINT3/PWM4BB
SEG25				P04/AN2/EINT2/PWM4BA
SEG26				P03/AN1/EINT1/PWM4AB

**Table 5.4** Normal Pin Description (continue)

PIN Name	I/O	Function	@RESET	Shared with
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by CONFIGURE OPTION	Input	P55
DSDA	I/O	In-system programming data input/output	Input	P00/EC3
DSCL	I/O	In-system programming clock input	Input	P01/T3O
XIN	I/O	Main oscillator pins	Input	P51
XOUT				P50
SXIN	I/O	Sub oscillator pins	Input	P53/T0O/PWM0O
SXOUT				P54/EINT10
VDD, VSS	–	Power input pins	–	–

**Table 5.5** Normal Pin Description (conclude)

**NOTE)**

1. The P14–P17, P23–P25, P34–P37 and P43 are not in the 32-pin package.
2. The P13–P17, P22–P27, P34–P37 and P43 are not in the 28-pin package.
3. The P05–P07, P14–P17, P20, P22–P27, P34–P37 and P42-P43 are not in the 24-pin package.
4. The P55/RESETB pin is configured as one of the P55 and RESETB pin by the “CONFIGURE OPTION.”
5. If the P00/EC3/DSDA and P01/T3O/DSCL pins are connected to the programmer during power-on reset, the pins are automatically configured as In-system programming pins.
6. The P00/EC3/DSDA and P01/T3O/DSCL pins are configured as inputs with internal pull-up resistor only during the reset or power-on reset.
7. The P50/XOUT, P51/XIN, P53/SXIN/T0O/PWM0O and P54/SXOUT/EINT10 pins are configured as a function pin by software control.

## 6 Port Structures

### 6.1 General Purpose I/O Port

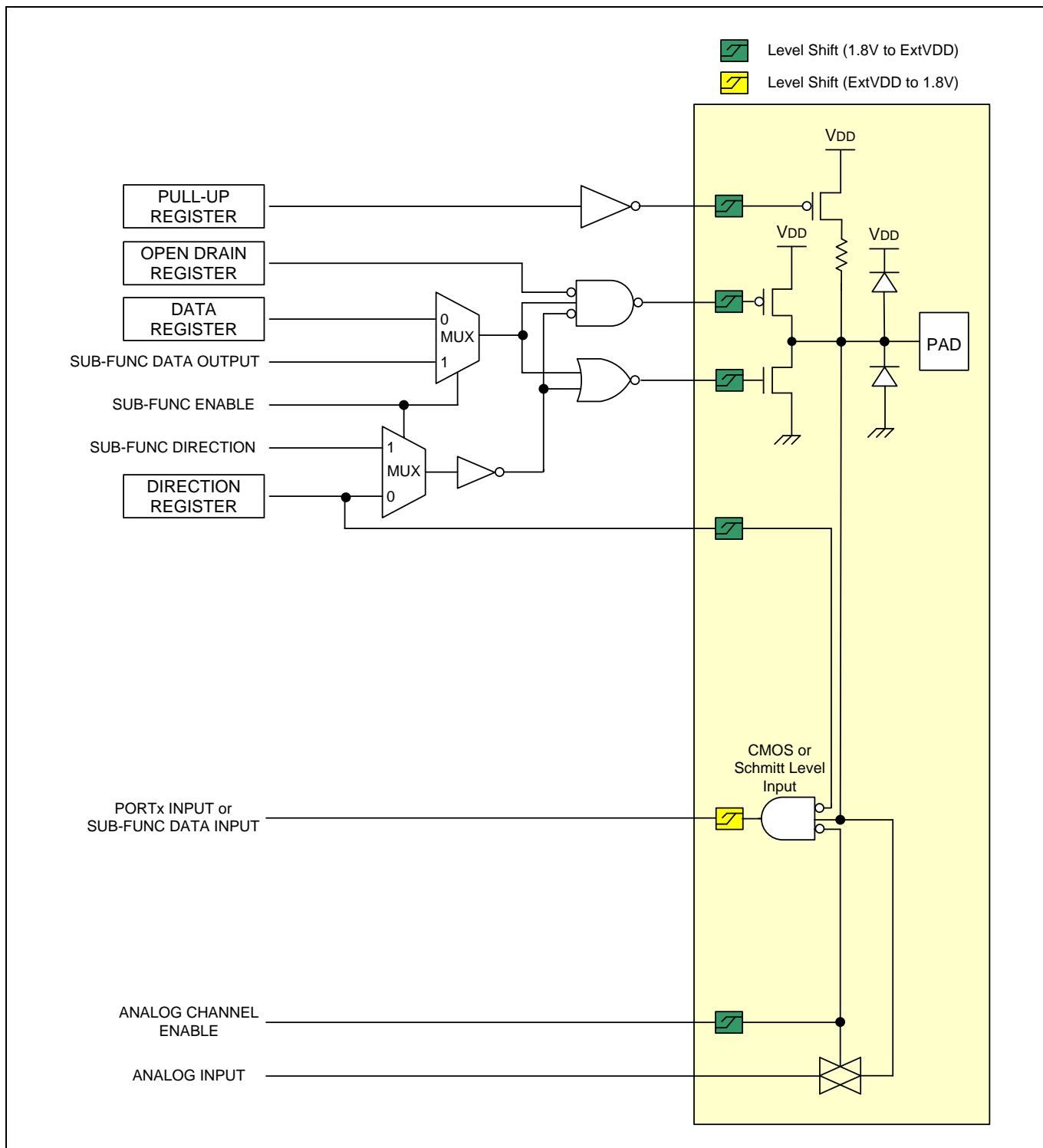


Figure 6.1 General Purpose I/O Port

### 6.2 External Interrupt I/O Port

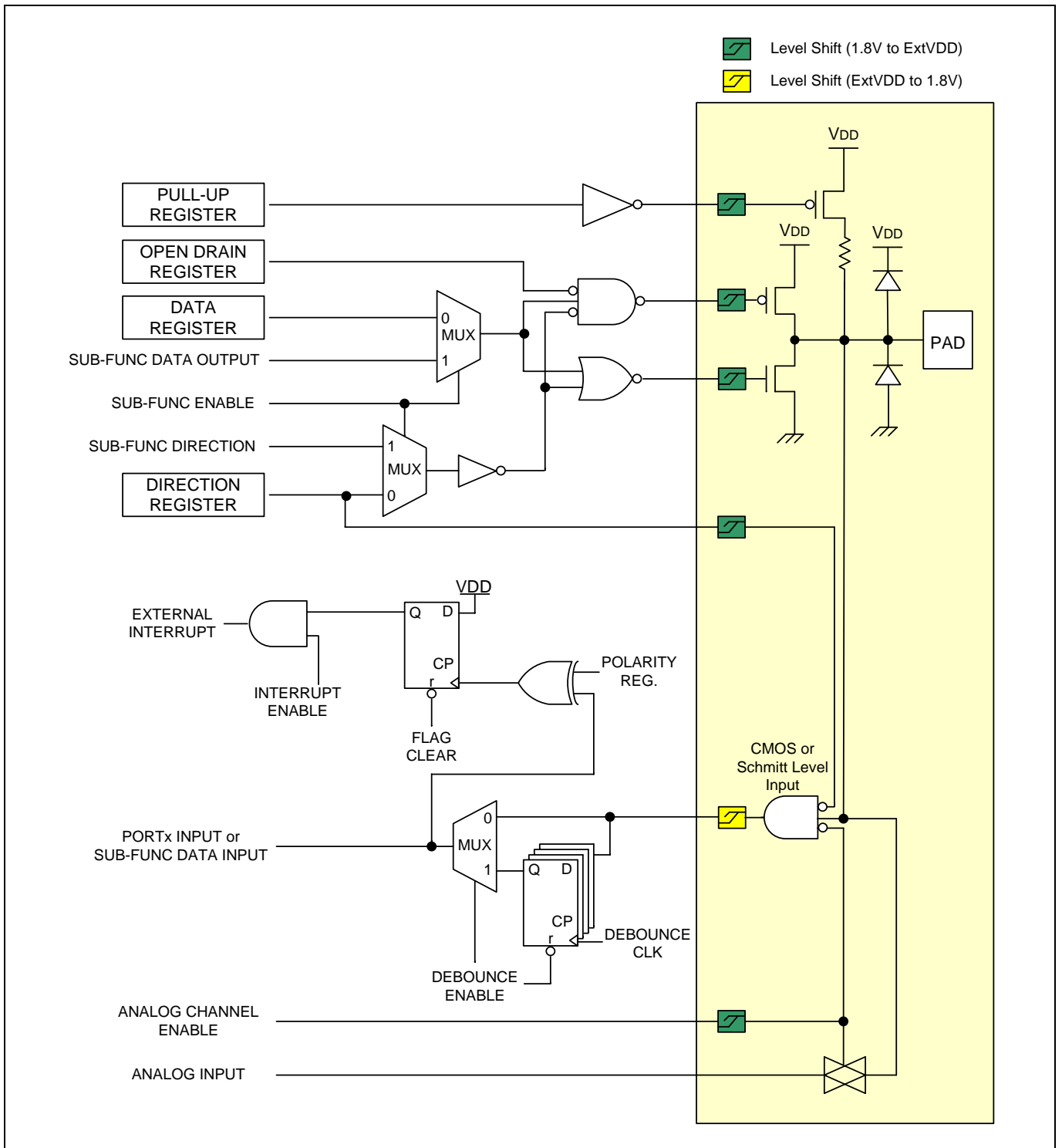


Figure 6.2 External Interrupt I/O Port

## 7 Electrical Characteristics

### 7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply Voltage	VDD	-0.3~+6.5	V	–
Normal Voltage Pin	V <sub>I</sub>	-0.3~VDD+0.3	V	Voltage on any pin with respect to VSS
	V <sub>O</sub>	-0.3~VDD+0.3	V	
	I <sub>OH</sub>	-10	mA	Maximum current output sourced by (I <sub>OH</sub> per I/O pin)
	ΣI <sub>OH</sub>	-80	mA	Maximum current (ΣI <sub>OH</sub> )
	I <sub>OL</sub>	60	mA	Maximum current sunk by (I <sub>OL</sub> per I/O pin)
	ΣI <sub>OL</sub>	120	mA	Maximum current (ΣI <sub>OL</sub> )
Total Power Dissipation	P <sub>T</sub>	600	mW	–
Storage Temperature	T <sub>STG</sub>	-65~+150	°C	–

Table 7.1 Absolute Maximum Ratings

**NOTE)**

- Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### 7.2 Recommended Operating Conditions

(T<sub>A</sub> = -40°C ~ +85°C)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Operating Voltage	VDD	f <sub>x</sub> = 32 ~ 38kHz	Sub Crystal	2.2	–	5.5	V
		f <sub>x</sub> = 0.4 ~ 4.2MHz	Main Crystal	2.2	–	5.5	
		f <sub>x</sub> = 0.4 ~ 8.5MHz		2.7	–	5.5	
		f <sub>x</sub> = 0.5 ~ 16MHz	Internal RC	2.2	–	5.5	
Operating Temperature	T <sub>OPR</sub>	VDD=2.2~5.5V		-40	–	85	°C

Table 7.2 Recommended Operating Conditions

### 7.3 A/D Converter Characteristics

(T<sub>A</sub> = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V, VSS = 0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Resolution	–	–	–	12	–	bit
Integral Non-Linear	INL	AVREF= 2.7V – 5.5V fx= 8MHz	–	–	±6	LSB
Differential Non-Linearity	DNL		–	–	±1	
Top Offset Error	TOE		–	–	±5	
Zero Offset Error	ZOE		–	–	±5	
Conversion Time	t <sub>CONV</sub>	12-bit resolution, 8MHz	20	–	–	us
Analog Input Voltage	V <sub>AIN</sub>	–	VSS	–	AVREF	V
Analog Reference Voltage	AVREF	*Note 3	2.2	–	VDD	
Analog Input Leakage Current	I <sub>AIN</sub>	AVREF=5.12V	–	–	2	uA
ADC Operating Current	I <sub>ADC</sub>	Enable	–	1	2	mA
		Disable	–	–	0.1	uA

**Table 7.3** A/D Converter Characteristics

#### NOTE)

1. Zero offset error is the difference between 000000000000 and the converted output for zero input voltage (VSS).
2. Full scale error is the difference between 111111111111 and the converted output for full-scale input voltage (AVREF).
3. When AVREF is lower than 2.7V, the ADC resolution is worse.

### 7.4 Power-On Reset Characteristics

(T<sub>A</sub> = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V, VSS = 0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	V <sub>POR</sub>	–	–	1.4	–	V
VDD Voltage Rising Time	t <sub>R</sub>	–	0.05	–	30.0	V/ms
POR Current	I <sub>POR</sub>	–	–	0.2	–	uA

**Table 7.4** Power-on Reset Characteristics

### 7.5 Low Voltage Reset and Low Voltage Indicator Characteristics

(T<sub>A</sub> = -40°C ~ +85°C, V<sub>DD</sub> = 2.2V ~ 5.5V, V<sub>SS</sub> = 0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	
Detection Level	V <sub>LVR</sub> V <sub>LVI</sub>	The LVR can select all levels but LVI can select other levels except 1.85V	-	1.85	2.15	V	
			2.05	2.20	2.35		
			2.17	2.32	2.47		
			2.29	2.44	2.59		
			2.39	2.59	2.79		
			2.55	2.75	2.95		
			2.73	2.93	3.13		
			2.94	3.14	3.34		
			3.18	3.38	3.58		
			3.37	3.67	3.97		
			3.70	4.00	4.30		
4.10	4.40	4.70					
Hysteresis	ΔV	-	-	50	150	mV	
Minimum Pulse Width	t <sub>lw</sub>	-	100	-	-	us	
LVR and LVI Current	I <sub>BL</sub>	Enable (Both)	V <sub>DD</sub> = 3V, RUN Mode	-	14.0	24.0	uA
		Enable (One of two)		-	10.0	18.0	
		Disable (Both)		V <sub>DD</sub> = 3V	-	-	

Table 7.5 LVR and LVI Characteristics

### 7.6 High Internal RC Oscillator Characteristics

(T<sub>A</sub> = -40°C ~ +85°C, V<sub>DD</sub> = 2.2V ~ 5.5V, V<sub>SS</sub> = 0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	
Frequency	f <sub>IRC</sub>	V <sub>DD</sub> = 2.2 – 5.5V	-	16	-	MHz	
Tolerance	-	T <sub>A</sub> = 0°C to +50°C	With 0.1uF Bypass capacitor	-	-	±1.5	%
		T <sub>A</sub> = -20°C to +85°C				±2.5	
		T <sub>A</sub> = -40°C to +85°C				±3.5	
Clock Duty Ratio	T <sub>OD</sub>	-	40	50	60	%	
Stabilization Time	T <sub>HFS</sub>	-	-	-	100	us	
IRC Current	I <sub>IRC</sub>	Enable	-	0.2	-	mA	
		Disable	-	-	0.1	uA	

Table 7.6 High Internal RC Oscillator Characteristics

**NOTE)**

1. A 0.1uF bypass capacitor should be connected to V<sub>DD</sub> and V<sub>SS</sub>.



## 7.7 Internal Watch-Dog Timer RC Oscillator Characteristics

(T<sub>A</sub> = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V, VSS = 0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	f <sub>WDTRC</sub>	–	2	5	10	kHz
Stabilization Time	t <sub>WDTS</sub>	–	–	–	1	ms
WDTRC Current	I <sub>WDTRC</sub>	Enable	–	1	–	uA
		Disable	–	–	0.1	

Table 7.7 Internal WDTRC Oscillator Characteristics

## 7.8 LCD Voltage Characteristics

(T<sub>A</sub> = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V, VSS = 0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	
LCD Voltage	V <sub>LC0</sub>	LCD contrast disabled, 1/4 bias	Typx0.95	VDD	Typx1.05	V	
		LCD contrast enabled, 1/4 bias, RLCD1, No panel load	LCDCR=00H	Typx0.9	VDDx16/31	Typx1.1	V
			LCDCR=01H		VDDx16/30		
			LCDCR=02H		VDDx16/29		
			LCDCR=03H		VDDx16/28		
			LCDCR=04H		VDDx16/27		
			LCDCR=05H		VDDx16/26		
			LCDCR=06H		VDDx16/25		
			LCDCR=07H		VDDx16/24		
			LCDCR=08H		VDDx16/23		
			LCDCR=09H		VDDx16/22		
			LCDCR=0AH		VDDx16/21		
			LCDCR=0BH		VDDx16/20		
			LCDCR=0CH		VDDx16/19		
			LCDCR=0DH		VDDx16/18		
LCDCR=0EH	VDDx16/17						
LCDCR=0FH	VDDx16/16						
LCD Mid Bias Voltage(note)	V <sub>LC1</sub>	VDD=2.7V to 5.5V, LCD clock = 0Hz, 1/4 bias, No panel load	Typx0.9	3/4xVLC0	Typx1.1	V	
	V <sub>LC2</sub>		Typx0.9	2/4xVLC0	Typx1.1		
	V <sub>LC3</sub>		Typx0.9	1/4xVLC0	Typx1.1		
LCD Driver Output Impedance	R <sub>LO</sub>	VLCD=3V, ILOAD=±10uA	–	5	10	kΩ	
LCD Bias Dividing Resistor	R <sub>LCD1</sub>	T <sub>A</sub> = 25°C	40	60	80		
	R <sub>LCD2</sub>		80	120	160		

Table 7.8 LCD Voltage Characteristics

### NOTE)

1. It is middle output voltage when the VDD and the V<sub>LC0</sub> node are connected.

7.9 DC Characteristics

(T<sub>A</sub> = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V, VSS = 0V, f<sub>XIN</sub> = 8.0MHz)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit	
Input High Voltage	V <sub>IH1</sub>	P0, P1,P5, RESETB		0.8VDD	–	VDD	V	
	V <sub>IH2</sub>	All input pins except V <sub>IH1</sub>		0.7VDD	–	VDD	V	
Input Low Voltage	V <sub>IL1</sub>	P0, P1,P5, RESETB		–	–	0.2VDD	V	
	V <sub>IL2</sub>	All input pins except V <sub>IL1</sub>		–	–	0.3VDD	V	
Output High Voltage	V <sub>OH</sub>	VDD=4.5V, I <sub>OH</sub> =-2mA, All output ports;		VDD-1.0	–	–	V	
Output Low Voltage	V <sub>OL1</sub>	VDD=4.5V, I <sub>OL</sub> = 10mA; All output ports except V <sub>OL2</sub>		–	–	1.0		
	V <sub>OL2</sub>	VDD=4.5V, I <sub>OL</sub> = 15mA; P1		–	–	1.0	V	
Input High Leakage Current	I <sub>IH</sub>	All input ports		–	–	1	uA	
Input Low Leakage Current	I <sub>IL</sub>	All input ports		-1	–	–	uA	
Pull-Up Resistor	R <sub>PU1</sub>	V <sub>I</sub> =0V, T <sub>A</sub> = 25°C All Input ports	VDD=5.0V	25	50	100	kΩ	
			VDD=3.0V	50	100	200		
	R <sub>PU2</sub>	V <sub>I</sub> =0V, T <sub>A</sub> = 25°C RESETB	VDD=5.0V	150	250	400	kΩ	
			VDD=3.0V	300	500	700		
OSC feedback resistor	R <sub>X1</sub>	XIN= VDD, XOUT= VSS T <sub>A</sub> = 25°C, VDD= 5V		600	1200	2000	kΩ	
	R <sub>X2</sub>	SXIN=VDD, SXOUT=VSS T <sub>A</sub> = 25°C, VDD=5V		2500	5000	10000		
Supply Current	I <sub>DD1</sub> (RUN)	f <sub>XIN</sub> = 8MHz	VDD= 5V±10%	–	2.6	5.2	mA	
		f <sub>XIN</sub> = 4MHz	VDD= 3V±10%	–	1.2	2.4		
		f <sub>IRC</sub> = 16MHz	VDD= 5V±10%	–	3.0	6.0		
	I <sub>DD2</sub> (IDLE)	f <sub>XIN</sub> = 8MHz	VDD= 5V±10%	–	1.8	3.6	mA	
		f <sub>XIN</sub> = 4MHz	VDD= 3V±10%	–	0.8	1.6		
		f <sub>IRC</sub> = 16MHz	VDD= 5V±10%	–	1.5	3.0		
	I <sub>DD3</sub>	f <sub>XIN</sub> =32.768kHz VDD= 3V±10% T <sub>A</sub> = 25°C	Sub RUN		–	90.0	180.0	uA
	I <sub>DD4</sub>		Sub IDLE		–	8.0	16.0	uA
I <sub>DD5</sub>	STOP, VDD= 5V±10%, T <sub>A</sub> = 25°C		–	0.5	3.0	uA		

Table 7.9 DC Characteristics

NOTE)

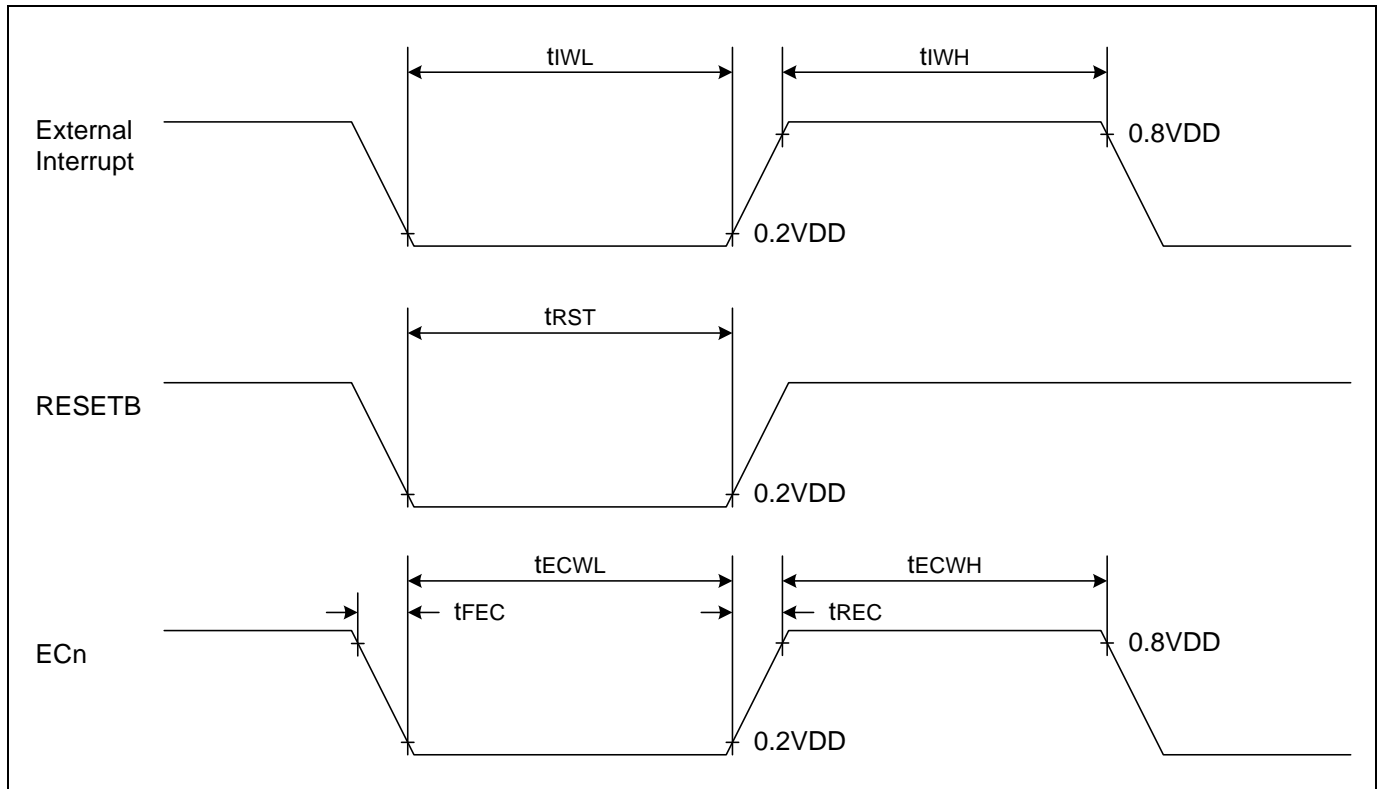
1. Where the f<sub>XIN</sub> is an external main oscillator, f<sub>SUB</sub> is an external sub oscillator, the f<sub>IRC</sub> is an internal RC oscillator and the fx is the selected system clock.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current items include the current of the power-on reset (POR) block.

### 7.10 AC Characteristics

( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 2.2\text{V} \sim 5.5\text{V}$ )

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESETB Input Low Width	$t_{RST}$	Input, $V_{DD} = 5\text{V}$	10	–	–	us
Interrupt Input High, Low Width	$t_{IWH}$ , $t_{IWL}$	All interrupt, $V_{DD} = 5\text{V}$	200	–	–	ns
External Counter Input High, Low Pulse Width	$t_{ECWH}$ , $t_{ECWL}$	$EC_n$ , $V_{DD} = 5\text{V}$ ( $n = 0, 1, 3$ )	200	–	–	
External Counter Transition Time	$t_{REC}$ , $t_{FEC}$	$EC_n$ , $V_{DD} = 5\text{V}$ ( $n = 0, 1, 3$ )	20	–	–	

**Table 7.10** AC Characteristics



**Figure 7.1** AC Timing

### 7.11 SPI0/1/2 Characteristics

( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 2.2\text{V} \sim 5.5\text{V}$ )

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Clock Pulse Period	$t_{\text{SCK}}$	Internal SCK source	200	–	–	ns
Input Clock Pulse Period		External SCK source	200	–	–	
Output Clock High, Low Pulse Width	$t_{\text{SCKH}}$ , $t_{\text{SCKL}}$	Internal SCK source	70	–	–	
Input Clock High, Low Pulse Width		External SCK source	70	–	–	
First Output Clock Delay Time	$t_{\text{FOD}}$	Internal/External SCK source	100	–	–	
Output Clock Delay Time	$t_{\text{DS}}$	–	–	–	50	
Input Setup Time	$t_{\text{DIS}}$	–	100	–	–	
Input Hold Time	$t_{\text{DIH}}$	–	150	–	–	

Table 7.11 SPI0/1/2 Characteristics

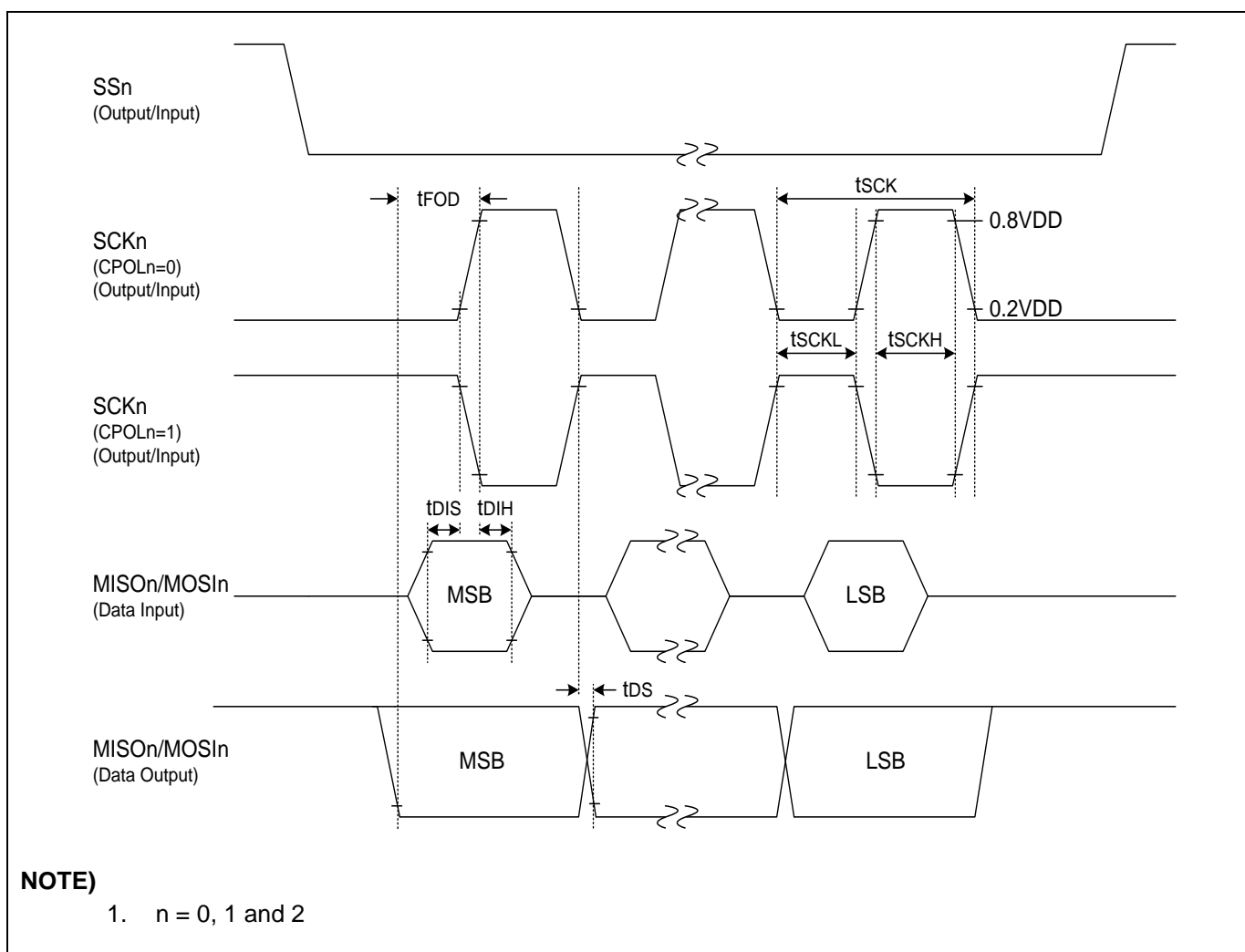


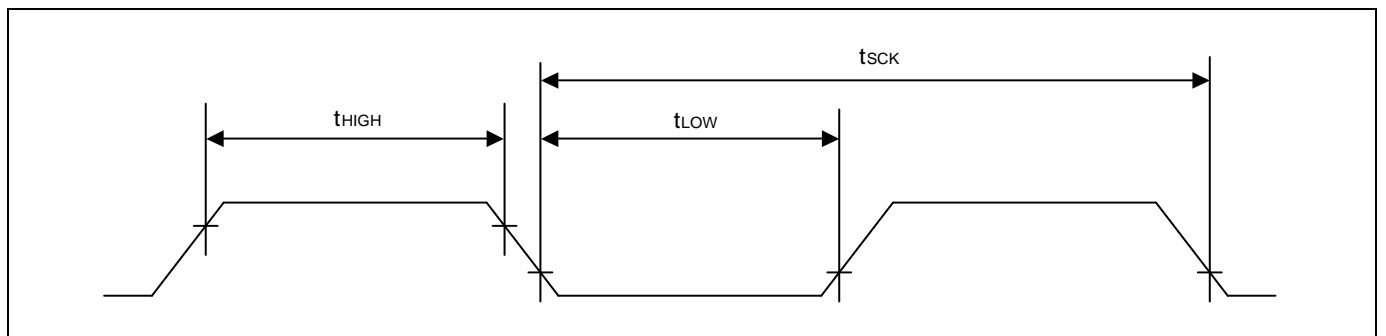
Figure 7.2 SPI0/1/2 Timing

### 7.12 UART0/1 Characteristics

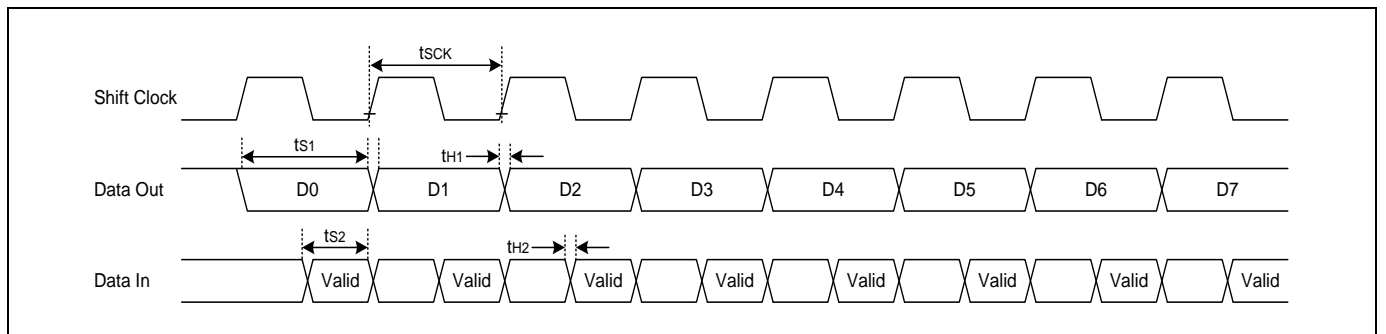
( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 2.2\text{V} \sim 5.5\text{V}$ ,  $f_{XIN} = 8\text{MHz}$ )

Parameter	Symbol	MIN	TYP	MAX	Unit
Serial port clock cycle time	$t_{SCK}$	1800	$t_{CPU} \times 16$	2200	ns
Output data setup to clock rising edge	$t_{S1}$	810	$t_{CPU} \times 13$	—	
Clock rising edge to input data valid	$t_{S2}$	—	—	590	
Output data hold after clock rising edge	$t_{H1}$	$t_{CPU} - 50$	$t_{CPU}$	—	
Input data hold after clock rising edge	$t_{H2}$	0	—	—	
Serial port clock High, Low level width	$t_{HIGH}, t_{LOW}$	720	$t_{CPU} \times 8$	1280	

**Table 7.12** UART0/1 Characteristics



**Figure 7.3** Waveform for UART0/1 Timing Characteristics



**Figure 7.4** Timing Waveform for the UART0/1 Module

### 7.13 I2C0/1 Characteristics

( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 2.2\text{V} \sim 5.5\text{V}$ )

Parameter	Symbol	Standard Mode		High-Speed Mode		Unit
		MIN	MAX	MIN	MAX	
Clock frequency	$t_{SCL}$	0	100	0	400	kHz
Clock High Pulse Width	$t_{SCLH}$	4.0	—	0.6	—	
Clock Low Pulse Width	$t_{SCLL}$	4.7	—	1.3	—	
Bus Free Time	$t_{BF}$	4.7	—	1.3	—	
Start Condition Setup Time	$t_{STSU}$	4.7	—	0.6	—	
Start Condition Hold Time	$t_{STHD}$	4.0	—	0.6	—	
Stop Condition Setup Time	$t_{SPSU}$	4.0	—	0.6	—	
Stop Condition Hold Time	$t_{SPHD}$	4.0	—	0.6	—	
Output Valid from Clock	$t_{VD}$	0	—	0	—	
Data Input Hold Time	$t_{DIH}$	0	—	0	1.0	
Data Input Setup Time	$t_{DIS}$	250	—	100	—	
						ns

Table 7.13 I2C0/1 Characteristics

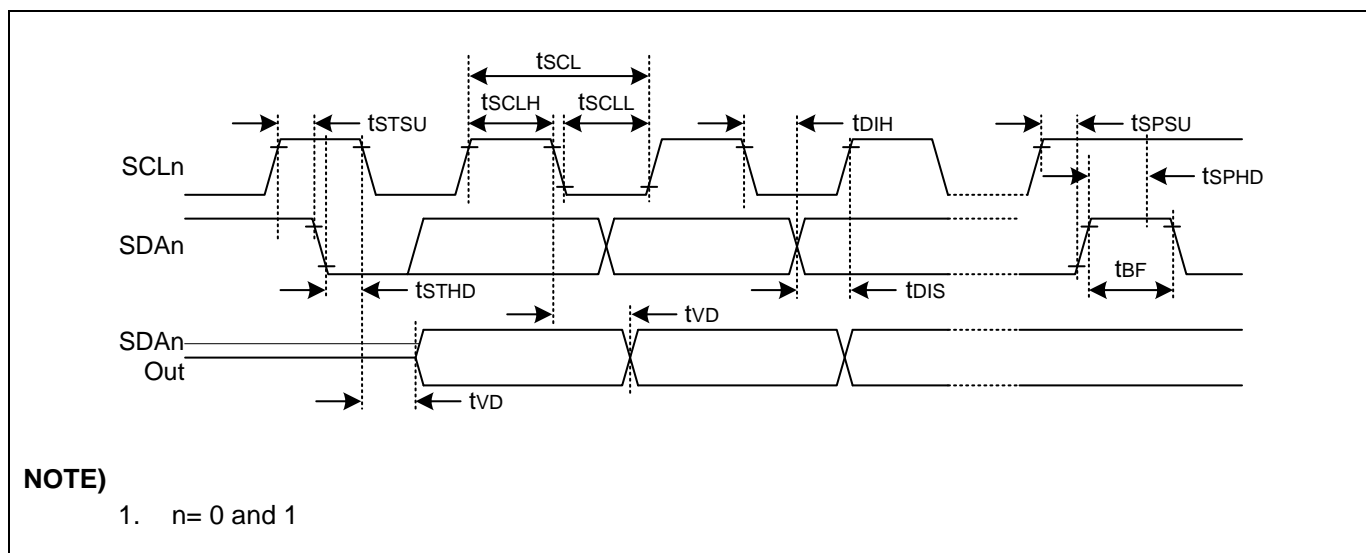


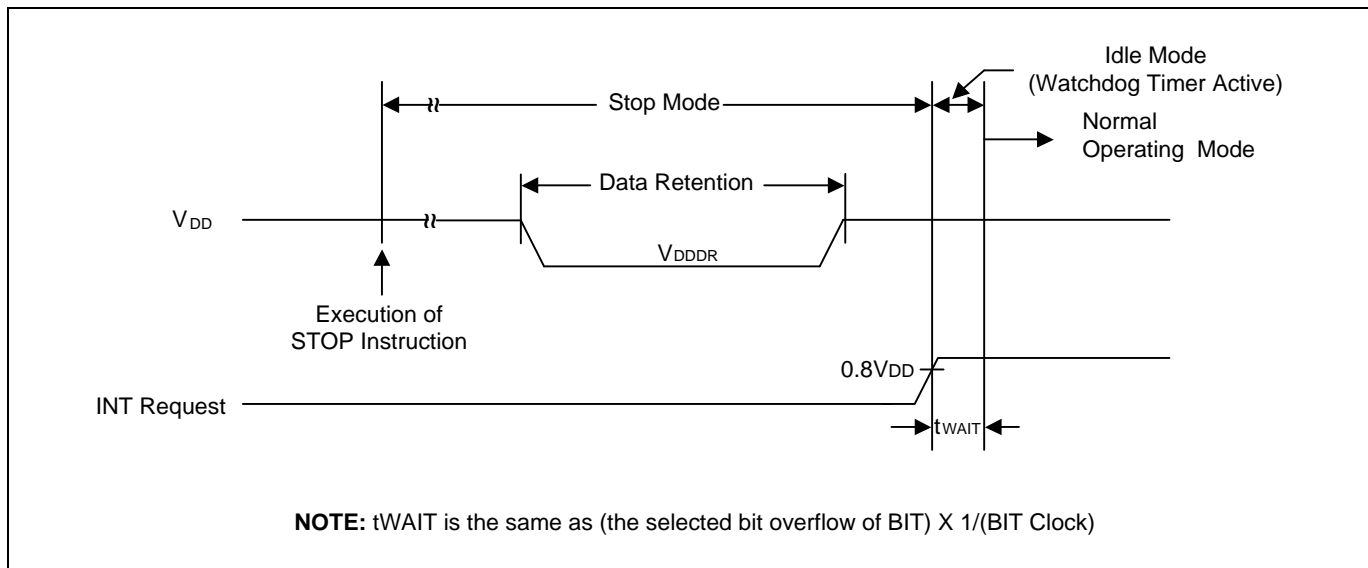
Figure 7.5 I2C0/1 Timing

### 7.14 Data Retention Voltage in Stop Mode

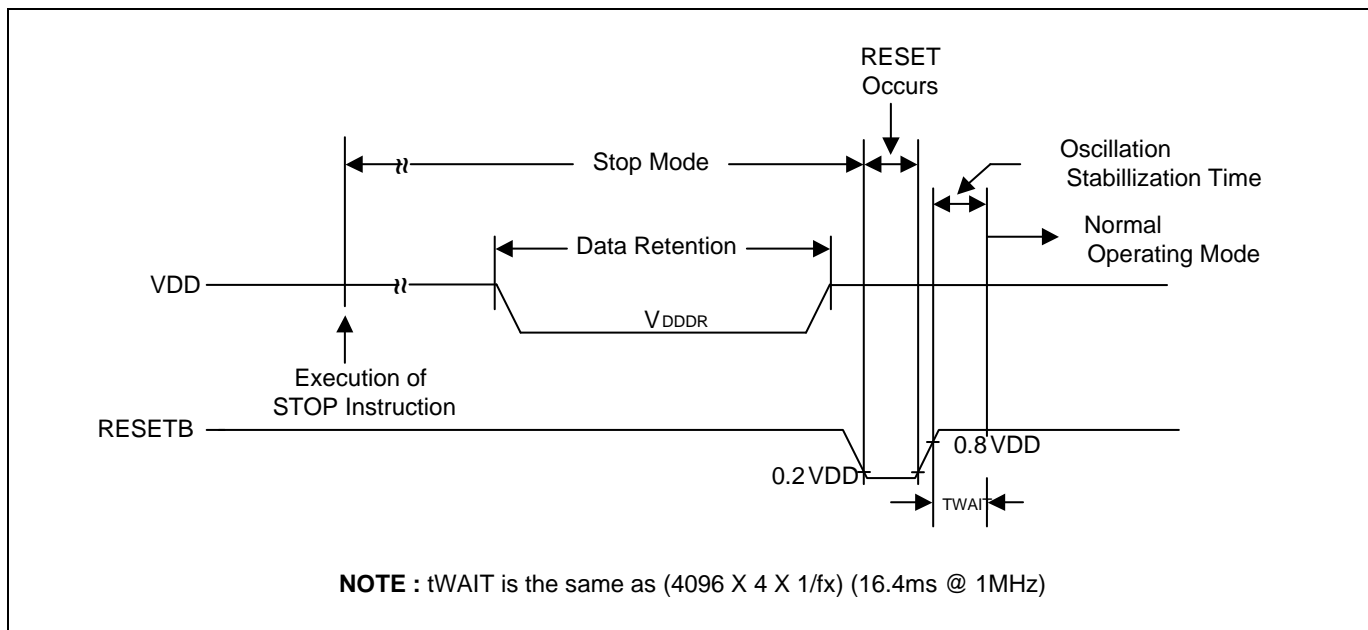
( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 2.2\text{V} \sim 5.5\text{V}$ )

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data retention supply voltage	$V_{DDDR}$	–	2.2	–	5.5	V
Data retention supply current	$I_{DDDR}$	$V_{DDR} = 2.2\text{V}(T_A = 25^{\circ}\text{C})$ , Stop mode	–	–	1	$\mu\text{A}$

**Table 7.14** Data Retention Voltage in Stop Mode



**Figure 7.6** Stop Mode Release Timing when Initiated by an Interrupt



**Figure 7.7** Stop Mode Release Timing when Initiated by RESETB

### 7.15 Internal Flash Rom Characteristics

(T<sub>A</sub> = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V, VSS = 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Sector Write Time	t <sub>FSW</sub>	–	–	2.5	2.7	ms
Sector Erase Time	t <sub>FSE</sub>	–	–	2.5	2.7	
Code Write Protection Time	t <sub>FHL</sub>	–	–	2.5	2.7	
Page Buffer Reset Time	t <sub>FBR</sub>	–	–	–	5	us
Flash Programming Frequency	f <sub>PGM</sub>	–	0.4	–	–	MHz
Endurance of Write/Erase	N <sub>FWE</sub>	Sector 0 to 507	–	–	10,000	times
		Sector 508 to 511(256 bytes)	–	–	100,000	
Flash Data Retention Time	t <sub>RT</sub>	–	10	–	–	years

Table 7.15 Internal Flash Rom Characteristics

**NOTE)**

1. During a flash operation, SCLK[1:0] of SCCR must be set to “00” or “01” (INT-RC OSC or Main X-TAL for system clock).

### 7.16 Input/Output Capacitance

(T<sub>A</sub> = -40°C ~ +85°C, VDD = 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Capacitance	C <sub>IN</sub>	f <sub>x</sub> = 1MHz Unmeasured pins are connected to VSS	–	–	10	pF
Output Capacitance	C <sub>OUT</sub>					
I/O Capacitance	C <sub>IO</sub>					

Table 7.16 Input/Output Capacitance

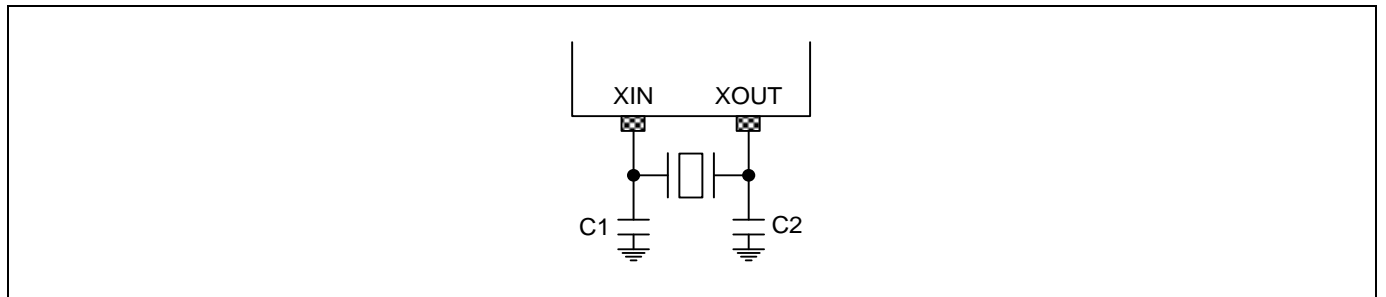


### 7.17 Main Clock Oscillator Characteristics

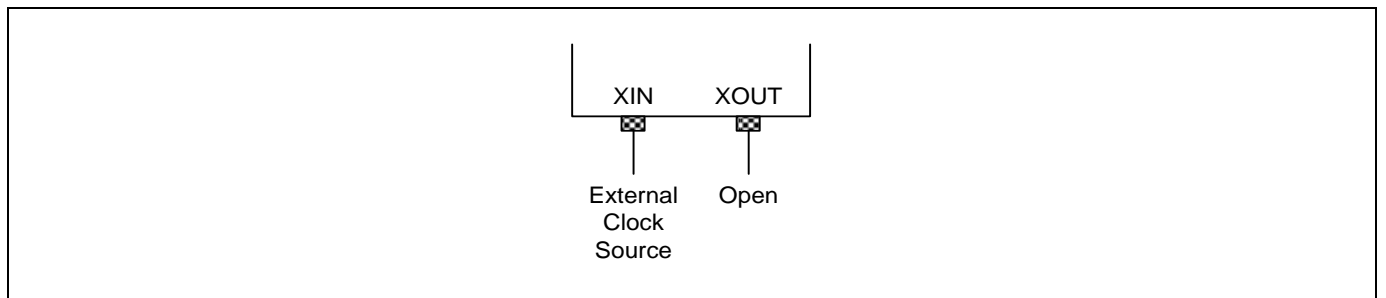
( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 2.2\text{V} \sim 5.5\text{V}$ )

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Main oscillation frequency	2.2V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	8.5	
Ceramic Oscillator	Main oscillation frequency	2.2V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	8.5	
External Clock	XIN input frequency	2.2V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	8.5	

**Table 7.17** Main Clock Oscillator Characteristics



**Figure 7.8** Crystal/Ceramic Oscillator



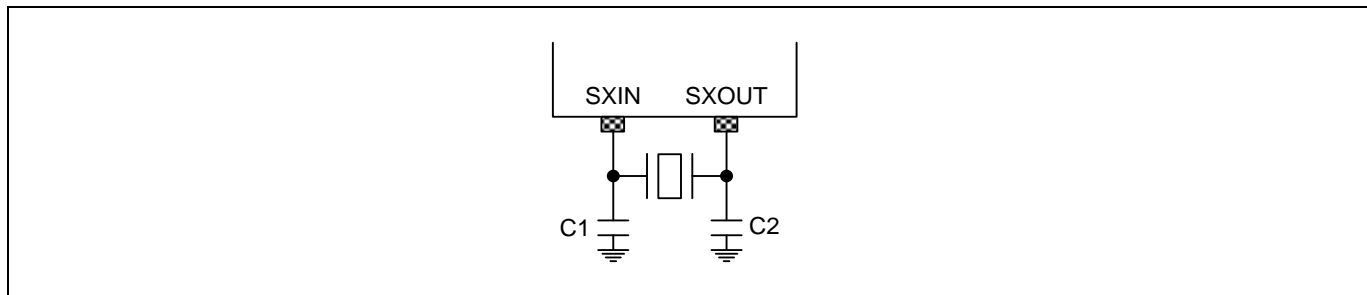
**Figure 7.9** External Clock

### 7.18 Sub Clock Oscillator Characteristics

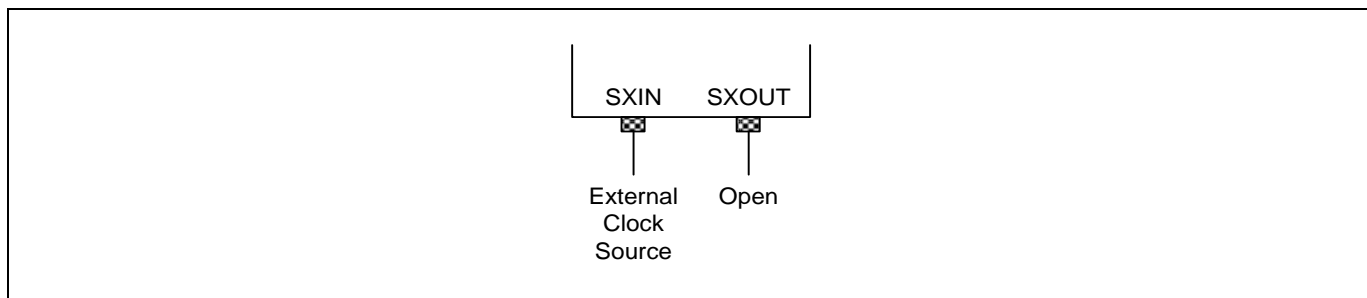
( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 2.2\text{V} \sim 5.5\text{V}$ )

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Sub oscillation frequency	2.2V – 5.5V	32	32.768	38	kHz
External Clock	SXIN input frequency		32	–	100	kHz

**Table 7.18** Sub Clock Oscillator Characteristics



**Figure 7.10** Crystal Oscillator



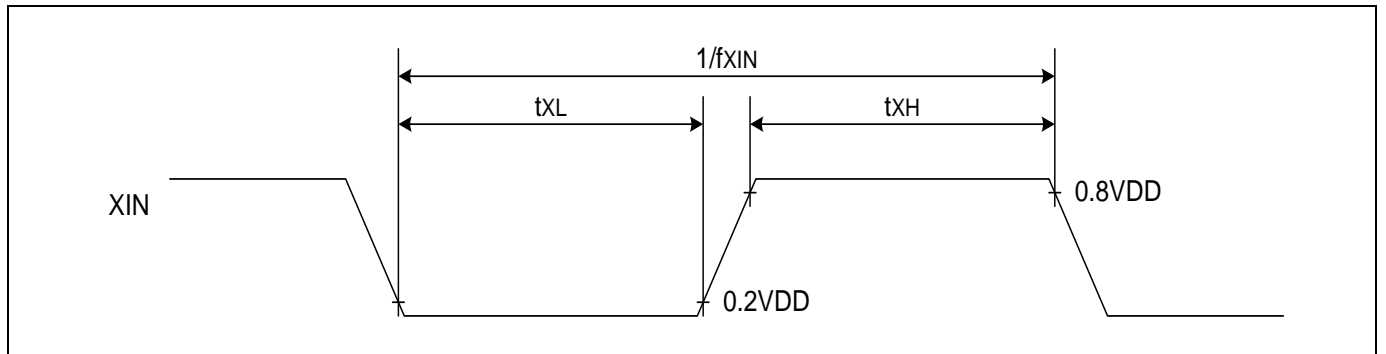
**Figure 7.11** External Clock

### 7.19 Main Oscillation Stabilization Characteristics

( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 2.2\text{V} \sim 5.5\text{V}$ )

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	$f_x > 4\text{MHz}$ , $V_{DD} = 2.7\text{V} \sim 5.5\text{V}$ ,	-	-	15	ms
	$f_x > 1\text{MHz}$ , $V_{DD} = 2.2\text{V}$ , $T_A = -40^{\circ}\text{C}$			60	
Ceramic	-	-	-	10	ms
External Clock	$f_{XIN} = 0.4$ to $8.5\text{MHz}$ XIN input high and low width ( $t_{XH}$ , $t_{XL}$ )	58	-	1250	ns

**Table 7.19** Main Oscillation Stabilization Characteristics



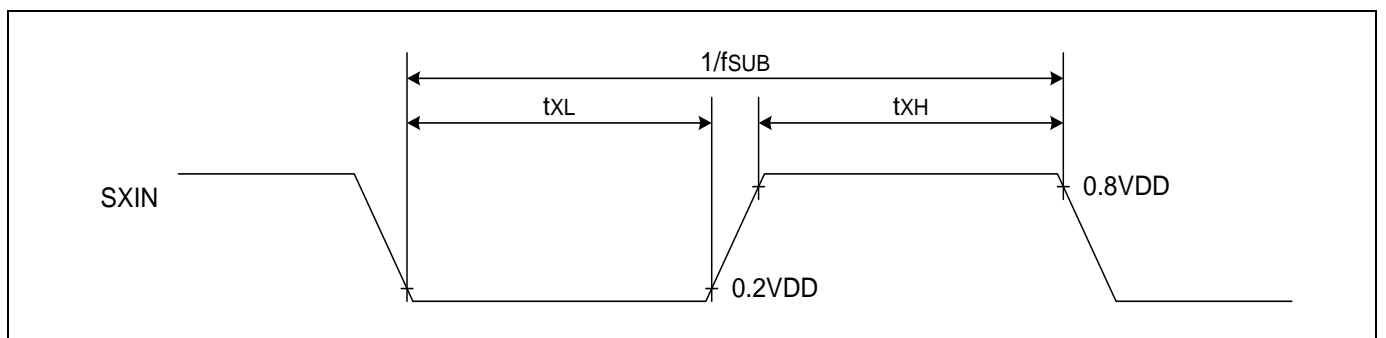
**Figure 7.12** Clock Timing Measurement at XIN

### 7.20 Sub Oscillation Characteristics

( $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ ,  $V_{DD} = 2.2\text{V} \sim 5.5\text{V}$ )

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	-	-	-	10	s
External Clock	SXIN input high and low width ( $t_{XH}$ , $t_{XL}$ )	5	-	15	us

**Table 7.20** Sub Oscillation Stabilization Characteristics



**Figure 7.13** Clock Timing Measurement at SXIN

### 7.21 Operating Voltage Range

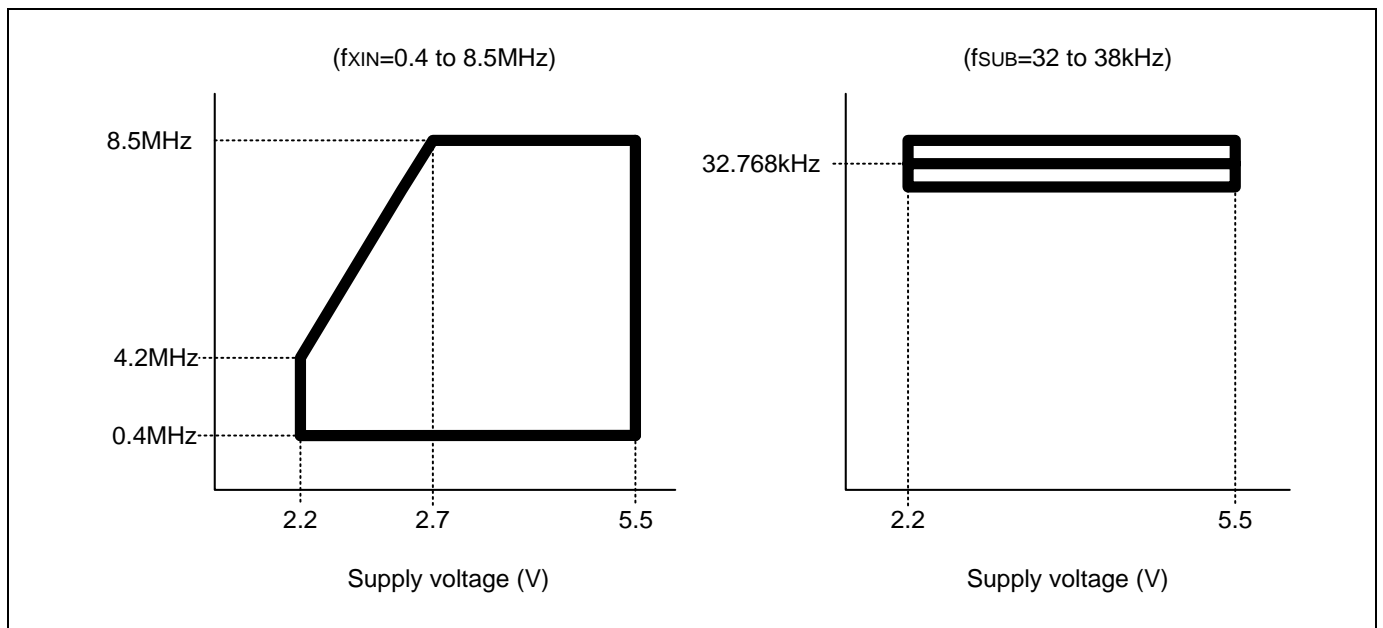


Figure 7.14 Operating Voltage Range

## 7.22 Recommended Circuit and Layout

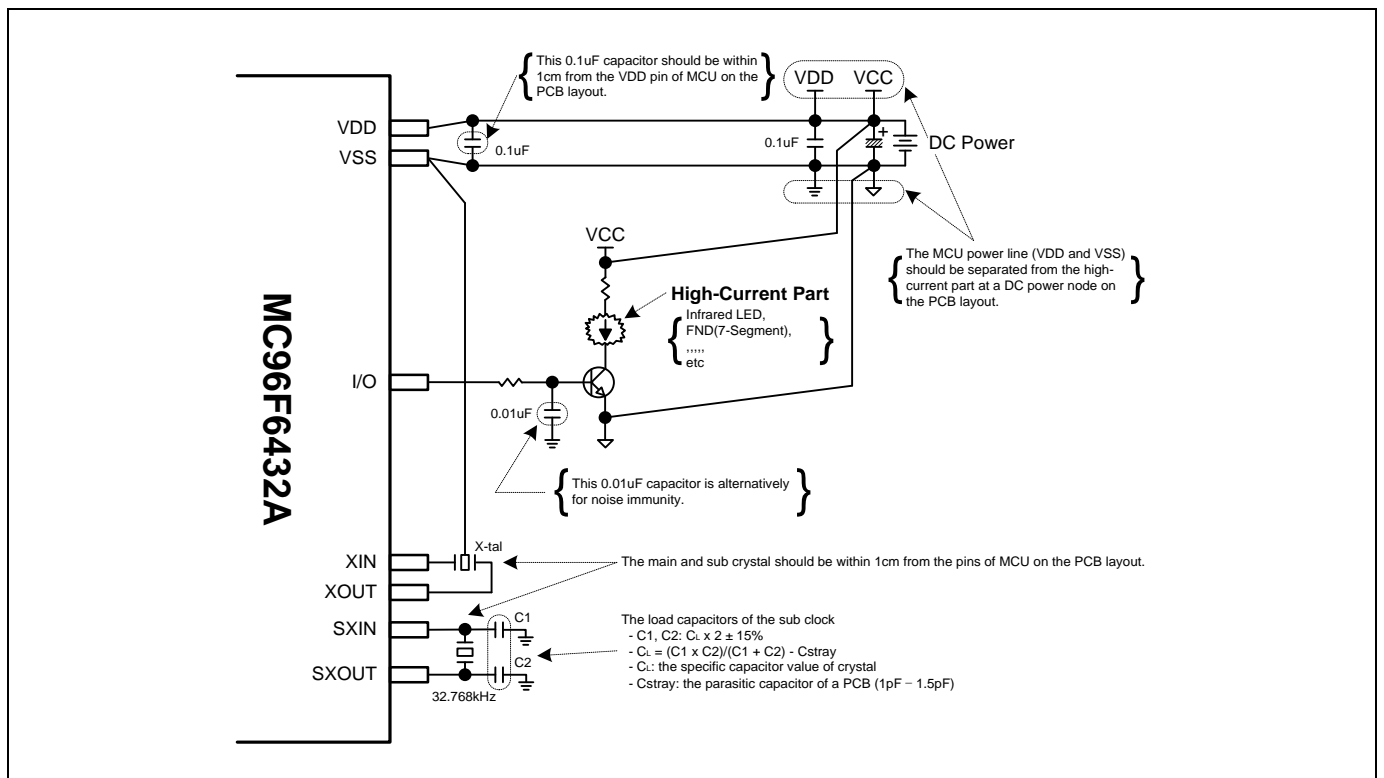


Figure 7.15 Recommended Circuit and Layout

### 7.23 Recommended Circuit and Layout with SMPS Power

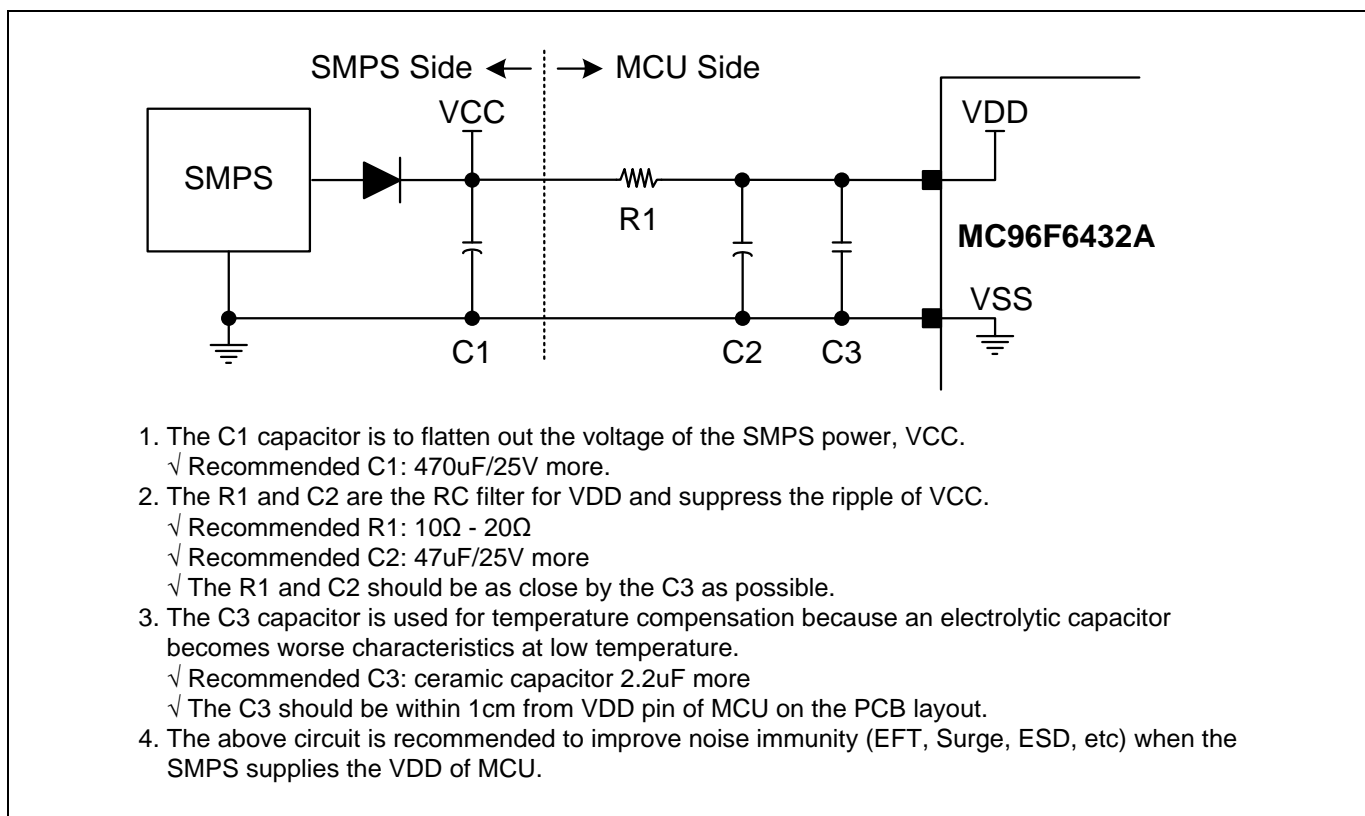


Figure 7.16 Recommended Circuit and Layout with SMPS Power

### 7.24 Typical Characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3 $\sigma$ ) and (mean - 3 $\sigma$ ) respectively where  $\sigma$  is standard deviation.

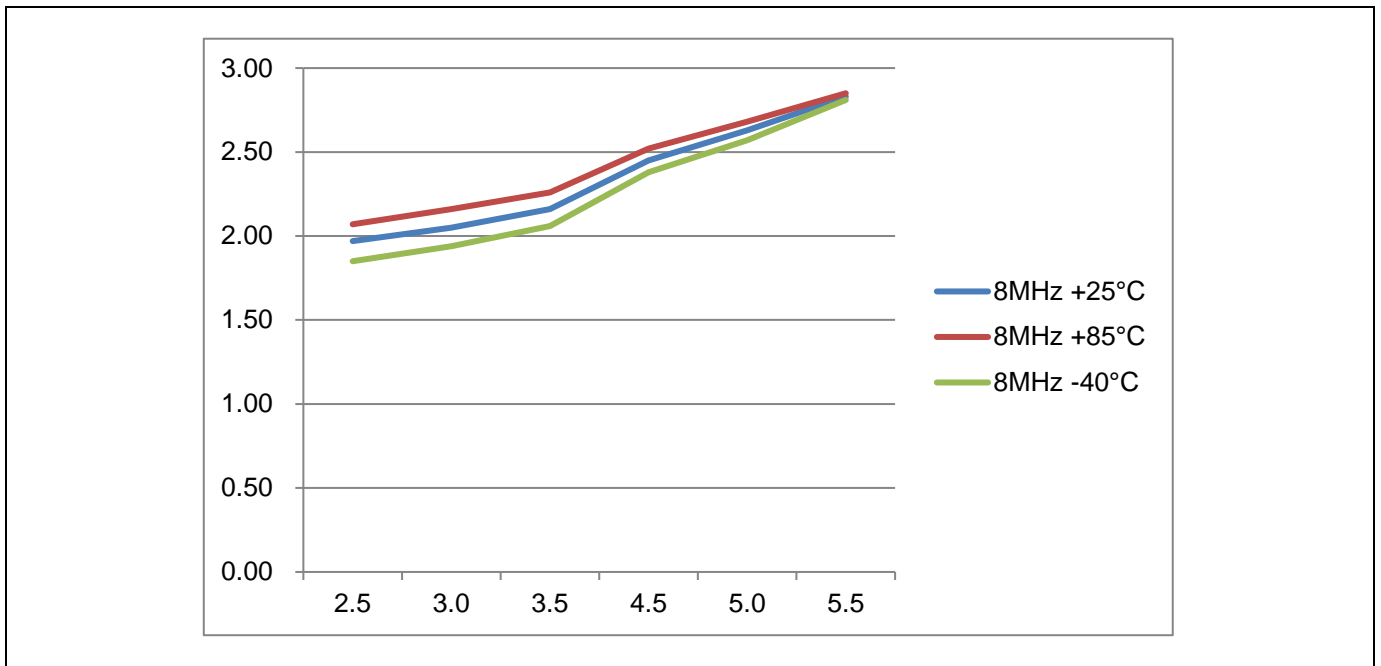


Figure 7.17 RUN (IDD1) Current

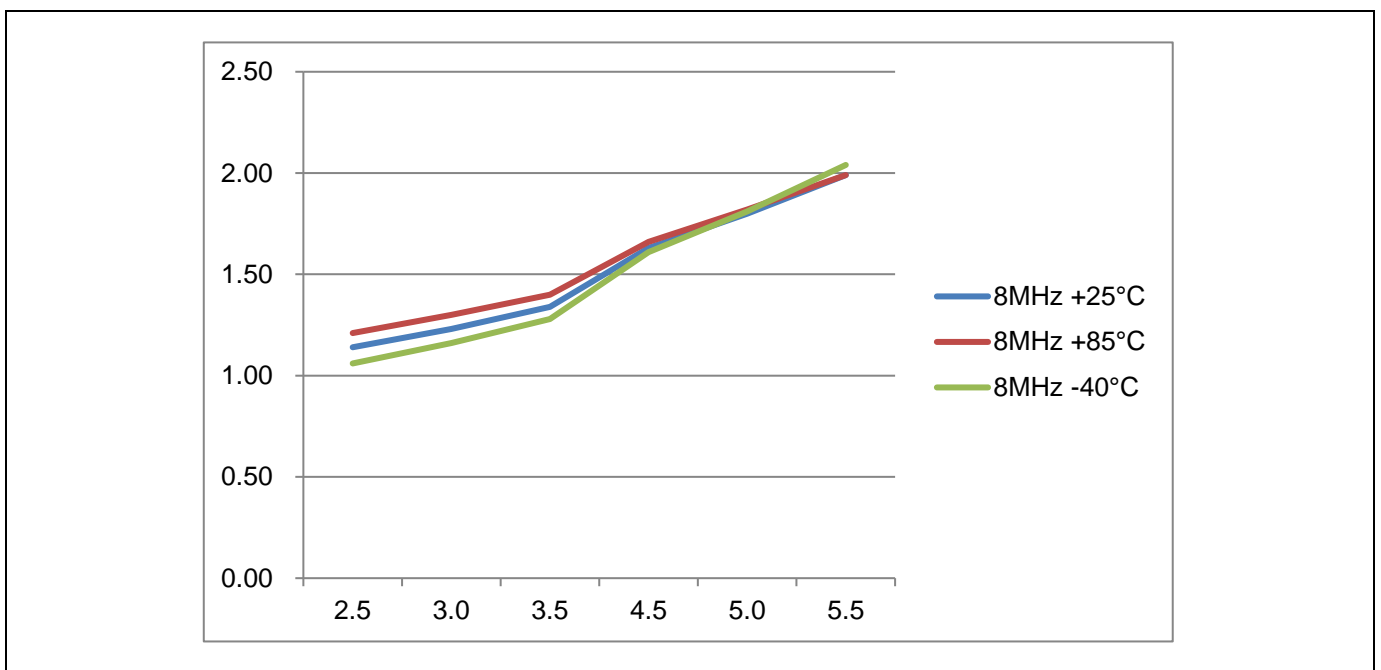


Figure 7.18 IDLE (IDD2) Current

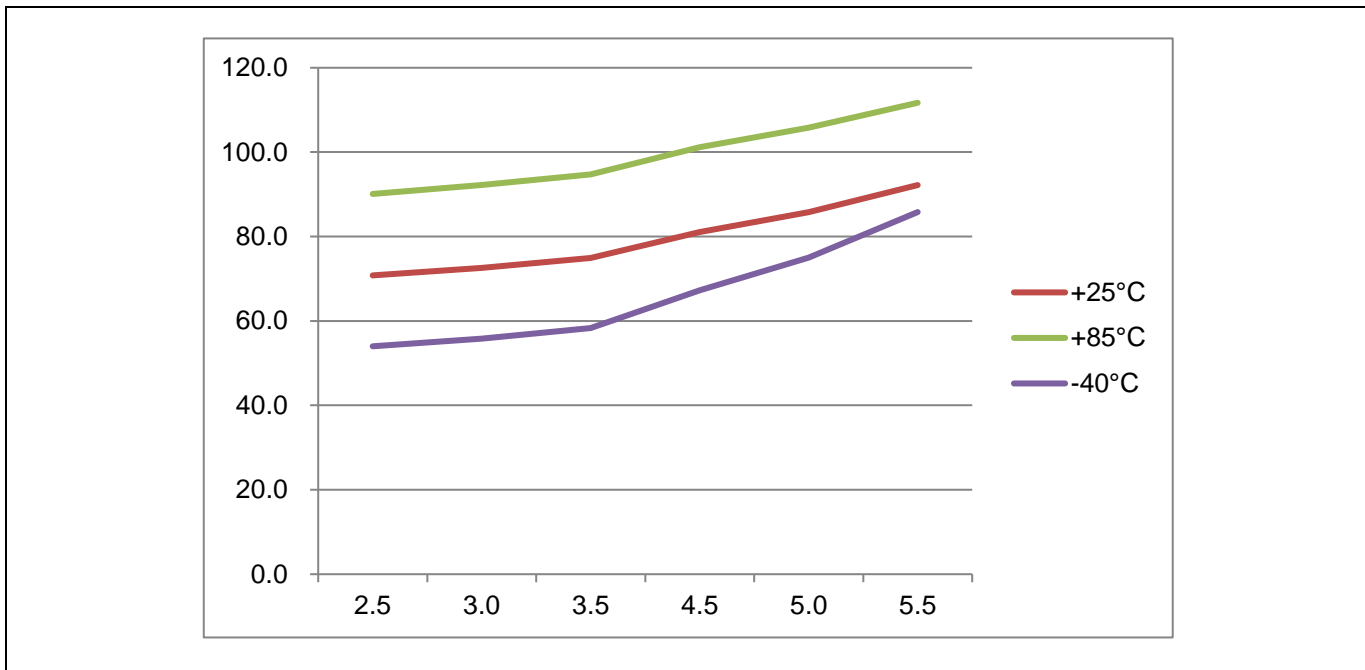


Figure 7.19 SUB RUN (IDD3) Current

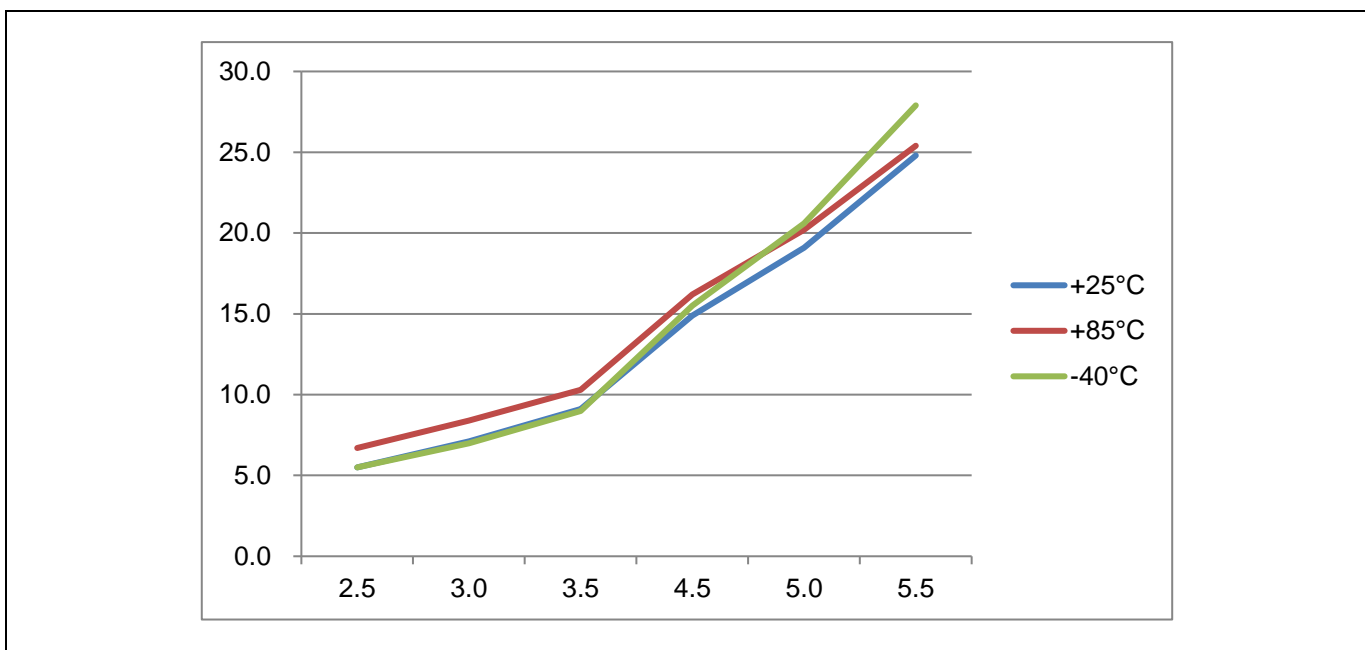


Figure 7.20 SUB IDLE (IDD4) Current



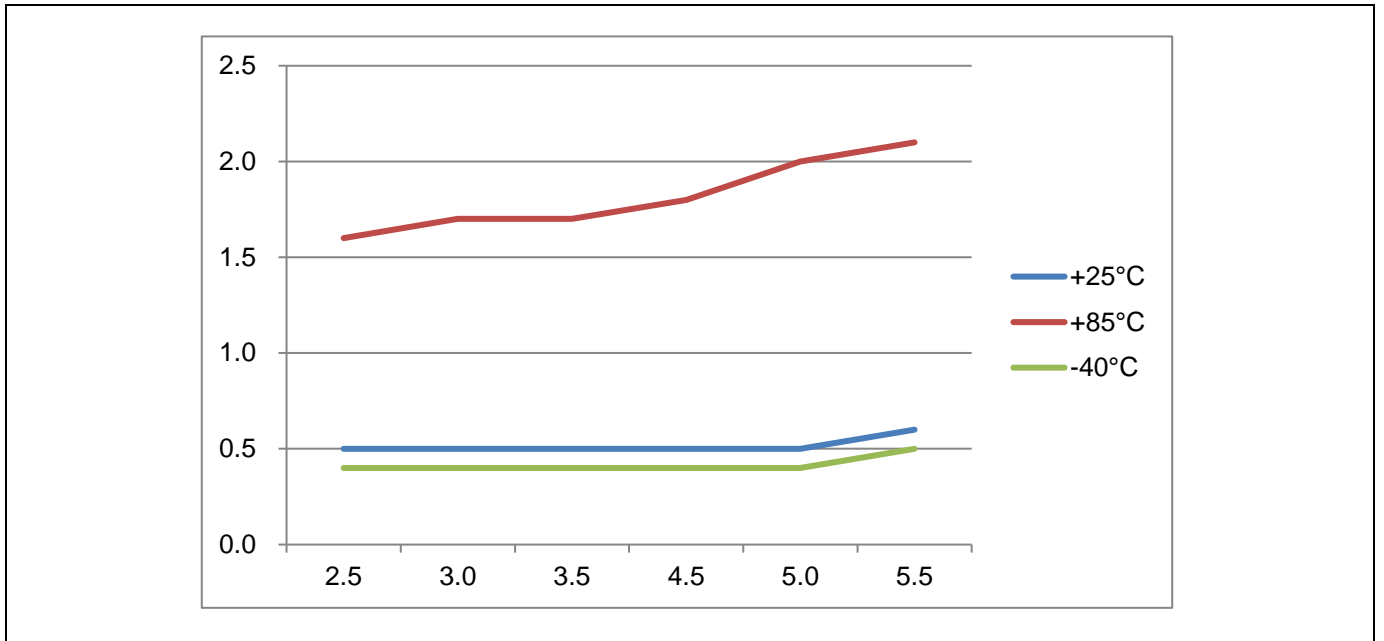


Figure 7.21 STOP (IDD5) Current

## 8 Memory

The MC96F6432A addresses two separate address memory stores: Program memory and Data memory. The logical separation of Program and Data memory allows Data memory to be accessed by 8-bit addresses, which makes the 8-bit CPU access the data memory more rapidly. Nevertheless, 16-bit Data memory addresses can also be generated through the DPTR register.

MC96F6432A provides on-chip 32 Kbytes of the ISP type flash program memory, which can be read and written to. Internal data memory (IRAM) is 256 bytes and it includes the stack area. External data memory (XRAM) is 768 bytes and it includes 27 bytes of LCD display RAM.

### 8.1 Program Memory

A 16-bit program counter is capable of addressing up to 64 Kbytes, but this device has just 32 Kbytes as program memory space.

Figure 8.1 shows the map of the lower part of the program memory. After reset, the CPU begins execution from address 0000H. Each interrupt is assigned to a fixed address in program memory. The interrupt causes the CPU to jump to that address, where it commences execution of the service routine. External interrupt 11, for example, is assigned to address 000BH. If external interrupt 11 would be requested, its service routine must begin at location 000BH. When the interrupt is not used, the Rom address is used as general purpose program memory. If an interrupt service routine is short enough (as is often case in S/W), it can reside entirely within that 8 bytes interval. Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.

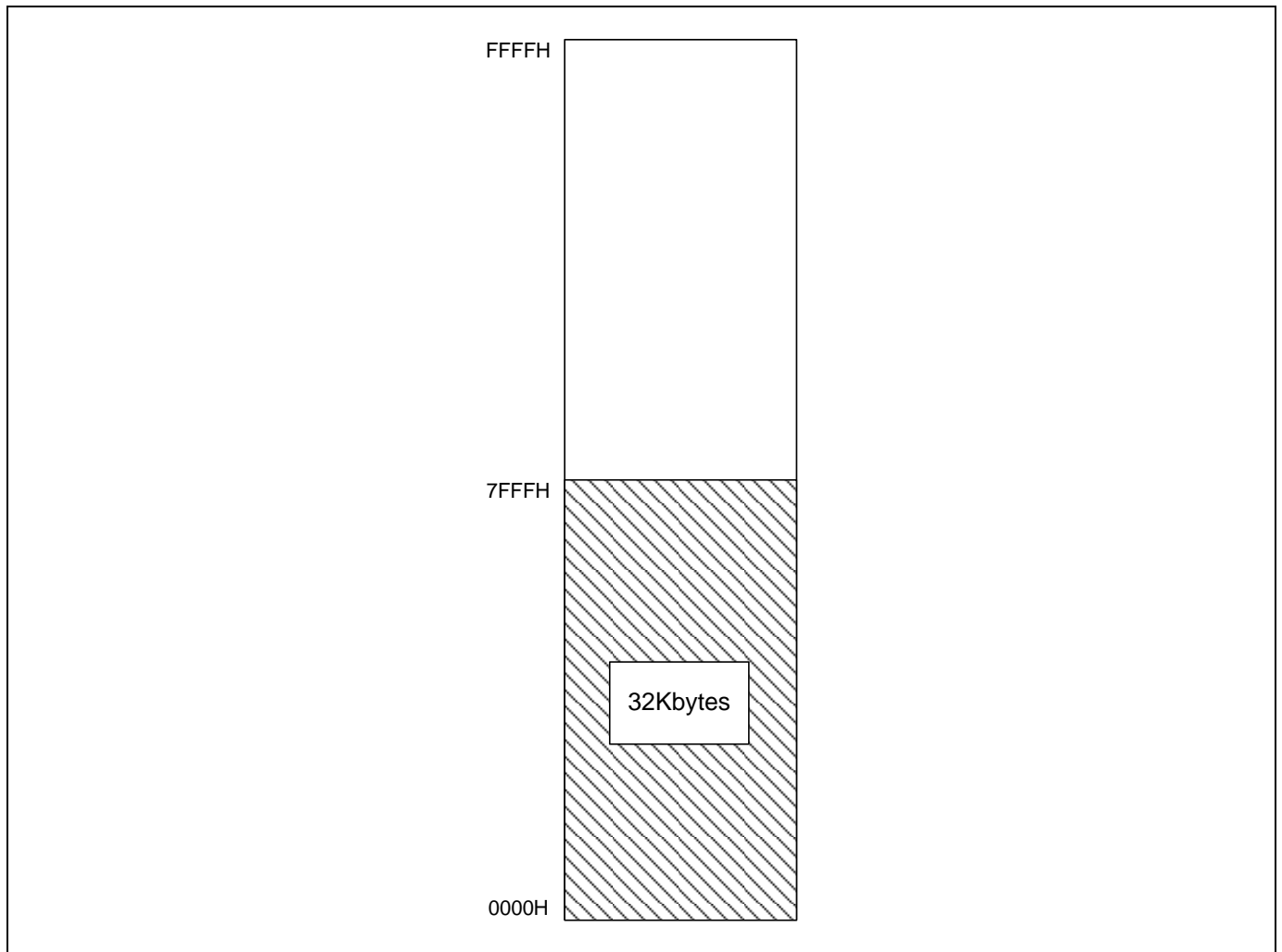
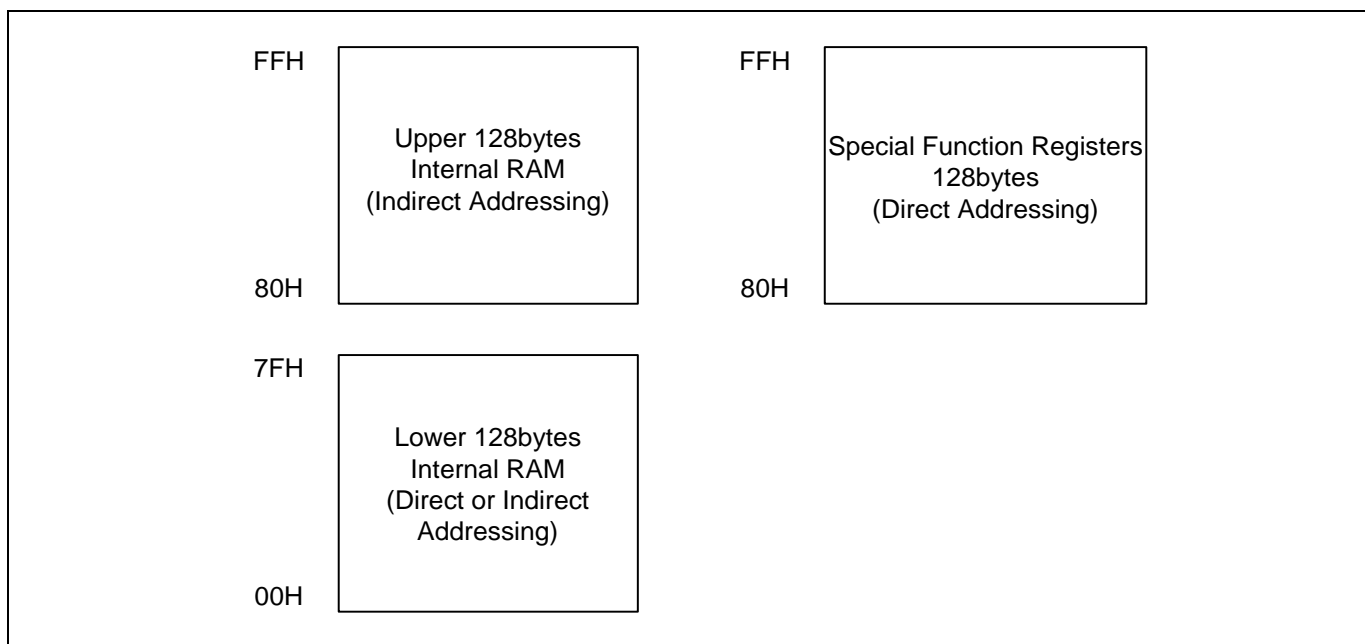


Figure 8.1 Program Memory

NOTE)

- 1. 32Kbytes Including Interrupt Vector address

## 8.2 Data Memory



**Figure 8.2** Data Memory Map

The internal data memory space is divided into three blocks, which are generally referred to as the lower 128 bytes, upper 128 bytes and SFR space.

Internal data memory address is one byte wide, which implies an address space of only 256bytes. However, in fact the addressing modes for internal RAM can accommodate up to 384 bytes by using a simple trick. Direct addresses higher than 7FH access one memory space and indirect addresses higher than 7FH access a different memory space. Thus Figure 8.2 shows the upper 128 bytes and SFR space occupying the same block of addresses, 80H through FFH, although they are physically separate entities.

The lower 128 bytes of RAM are present in all 8051 devices as mapped in Figure 8.3. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient usage of code space, since register instructions needs less bytes than direct addressing instructions.

The next 16 bytes above the register banks form a block of bit-addressable memory space. The 8051 instruction set includes a wide selection of single-bit instructions and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All of the bytes in the lower 128 bytes can be accessed by either direct or indirect addressing. The upper 128 bytes RAM can only be accessed by indirect addressing. These spaces are used for data RAM and stack.

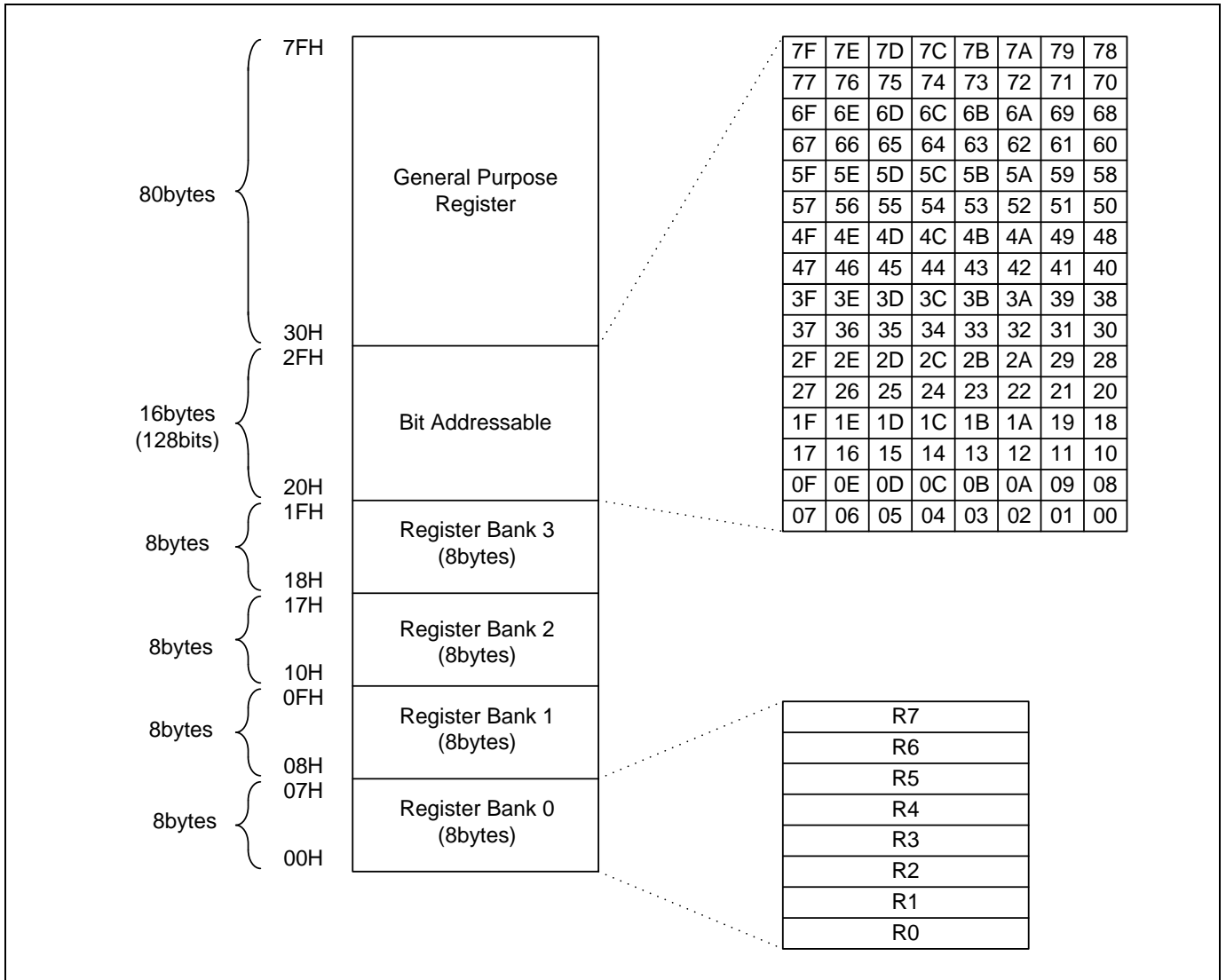


Figure 8.3 Lower 128bytes RAM

### 8.3 External Data Memory

MC96F6432A has 768 bytes XRAM and XSFR. This area has no relation with RAM/FLASH. It can be read and written to through SFR with 8-bit unit.

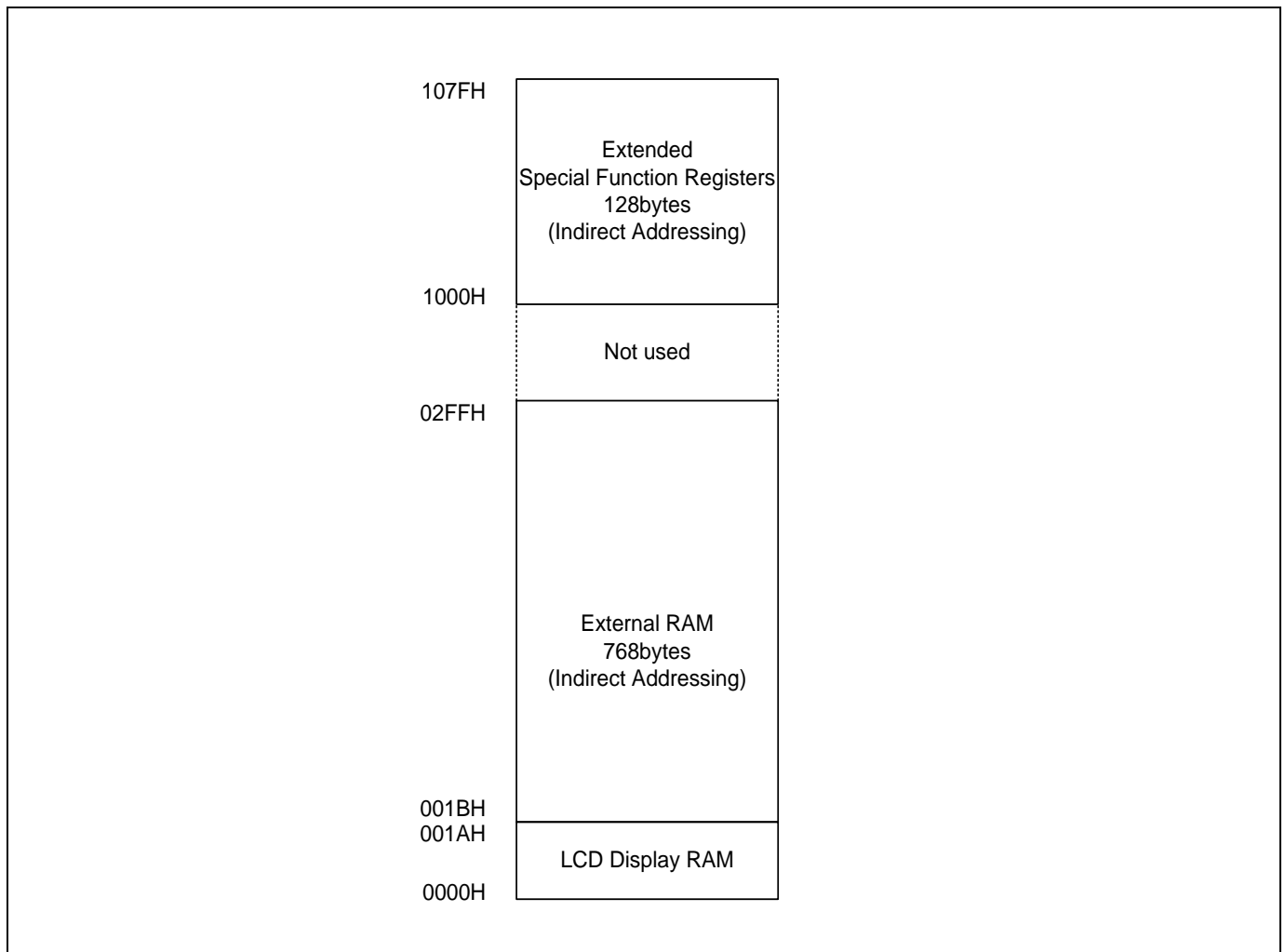


Figure 8.4 XDATA Memory Area

## 8.4 SFR Map

### 8.4.1 SFR Map Summary

-	Reserved
	M8051 compatible

	00H/8H <sup>(1)</sup>	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
0F8H	IP1	-	FSADRH	FSADRM	FSADRL	FIDR	FMCR	P5FSR
0F0H	B	USI1ST1	USI1ST2	USI1BD	USI1SDHR	USI1DR	USI1SCLR	USI1SCHR
0E8H	RSTFR	USI1CR1	USI1CR2	USI1CR3	USI1CR4	USI1SAR	P3FSR	P4FSR
0E0H	ACC	USI0ST1	USI0ST2	USI0BD	USI0SDHR	USI0DR	USI0SCLR	USI0SCHR
0D8H	LVRCR	USI0CR1	USI0CR2	USI0CR3	USI0CR4	USI0SAR	P0DB	P15DB
0D0H	PSW	P5IO	P0FSRL	P0FSRH	P1FSRL	P1FSRH	P2FSRL	P2FSRH
0C8H	OSCCR	P4IO	-	-	-	-	-	-
0C0H	EIFLAG0	P3IO	T2CRL	T2CRH	T2ADRL	T2ADRH	T2BDRL	T2BDRH
0B8H	IP	P2IO	T1CRL	T1CRH	T1ADRL	T1ADRH	T1BDRL	T1BDRH
0B0H	P5	P1IO	T0CR	T0CNT	T0DR/ T0CDR	SPICR	SPIDR	SPISR
0A8H	IE	IE1	IE2	IE3	P0PU	P1PU	P2PU	P3PU
0A0H	P4	P0IO	EO	P4PU	EIPOL0L	EIPOL0H	EIFLAG1	EIPOL1
98H	P3	LCDCRL	LCDCRH	LCDCCR	ADCCRL	ADCCRH	ADCDRL	ADCDRH
90H	P2	P0OD	P1OD	P2OD	P4OD	P5PU	WTCR	BUZCR
88H	P1	WTDR/ WTCNT	SCCR	BITCR	BITCNT	WDTCR	WDTDR/ WDCNT	BUZDR
80H	P0	SP	DPL	DPH	DPL1	DPH1	LVICR	PCON

Table 8.1 SFR Map Summary

#### NOTE)

- 00H/8H, These registers are bit-addressable.

	00H/8H <sup>(1)</sup>	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
1078H	-	-	-	-	-	-	-	-
1070H	-	-	-	-	-	-	-	-
1068H	-	-	-	-	-	-	-	-
1060H	-	-	-	-	-	-	-	-
1058H	-	-	-	-	-	-	-	-
1050H	-	-	-	-	-	-	-	-
1048H	-	-	-	-	-	-	-	-
1040H	-	-	-	-	-	-	-	-
1038H	XTFLSR	-	-	-	-	-	-	-
1030H	-	-	-	-	-	-	-	-
1028H	-	-	-	-	-	-	-	-
1020H	-	-	-	-	-	-	-	-
1018H	-	-	-	-	-	-	-	-
1010H	T4DLYA	T4DLYB	T4DLYC	T4DR	T4CAPR	T4CNT	-	-
1008H	T4PPRL	T4PPRH	T4ADRL	T4ADRH	T4BDRL	T4BDRH	T4CDRL	T4CDRH
1000H	T3CR	T3CNT/ T3DR/ T3CAPR	T4CR	T4PCR1	T4PCR2	T4PCR3	T4ISR	T4IMSK

Table 8.2 XSFR Map Summary



## 8.4.2 SFR Map

Address	Function	Symbol	R/W	@Reset								
				7	6	5	4	3	2	1	0	
80H	P0 Data Register	P0	R/W	0	0	0	0	0	0	0	0	0
81H	Stack Pointer	SP	R/W	0	0	0	0	0	1	1	1	1
82H	Data Pointer Register Low	DPL	R/W	0	0	0	0	0	0	0	0	0
83H	Data Pointer Register High	DPH	R/W	0	0	0	0	0	0	0	0	0
84H	Data Pointer Register Low 1	DPL1	R/W	0	0	0	0	0	0	0	0	0
85H	Data Pointer Register High 1	DPH1	R/W	0	0	0	0	0	0	0	0	0
86H	Low Voltage Indicator Control Register	LVICR	R/W	–	–	0	0	0	0	0	0	0
87H	Power Control Register	PCON	R/W	0	–	–	–	0	0	0	0	0
88H	P1 Data Register	P1	R/W	0	0	0	0	0	0	0	0	0
89H	Watch Timer Data Register	WTDR	W	0	1	1	1	1	1	1	1	1
	Watch Timer Counter Register	WTCNT	R	–	0	0	0	0	0	0	0	0
8AH	System and Clock Control Register	SCCR	R/W	–	–	–	–	–	–	0	0	0
8BH	BIT Control Register	BITCR	R/W	0	0	0	–	0	0	0	0	1
8CH	Basic Interval Timer Counter Register	BITCNT	R	0	0	0	0	0	0	0	0	0
8DH	Watch Dog Timer Control Register	WDTCR	R/W	0	0	0	–	–	–	0	0	0
8EH	Watch Dog Timer Data Register	WDTDR	W	1	1	1	1	1	1	1	1	1
	Watch Dog Timer Counter Register	WDCNT	R	0	0	0	0	0	0	0	0	0
8FH	BUZZER Data Register	BUZDR	R/W	1	1	1	1	1	1	1	1	1
90H	P2 Data Register	P2	R/W	0	0	0	0	0	0	0	0	0
91H	P0 Open-drain Selection Register	P0OD	R/W	0	0	0	0	0	0	0	0	0
92H	P1 Open-drain Selection Register	P1OD	R/W	0	0	0	0	0	0	0	0	0
93H	P2 Open-drain Selection Register	P2OD	R/W	0	0	0	0	0	0	0	0	0
94H	P4 Open-drain Selection Register	P4OD	R/W	–	–	–	–	0	0	0	0	0
95H	P5 Pull-up Resistor Selection Register	P5PU	R/W	–	–	0	0	0	0	0	0	0
96H	Watch Timer Control Register	WTCR	R/W	0	–	–	0	0	0	0	0	0
97H	BUZZER Control Register	BUZCR	R/W	–	–	–	–	–	0	0	0	0
98H	P3 Data Register	P3	R/W	0	0	0	0	0	0	0	0	0
99H	LCD Driver Control Low Register	LCDCRL	R/W	–	–	0	0	0	0	0	0	0
9AH	LCD Driver Control High Register	LCDCRH	R/W	–	–	–	0	–	–	0	0	0
9BH	LCD Contrast Control Register	LCDCCR	R/W	0	–	–	–	0	0	0	0	0
9CH	A/D Converter Control Low Register	ADCCRL	R/W	0	0	0	0	0	0	0	0	0
9DH	A/D Converter Control High Register	ADCCRH	R/W	0	–	0	0	0	0	0	0	0
9EH	A/D Converter Data Low Register	ADCDRL	R	x	x	x	x	x	x	x	x	x
9FH	A/D Converter Data High Register	ADCDRH	R	x	x	x	x	x	x	x	x	x

Table 8.3 SFR Map

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
A0H	P4 Data Register	P4	R/W	-	-	-	-	0	0	0	0
A1H	P0 Direction Register	P0IO	R/W	0	0	0	0	0	0	0	0
A2H	Extended Operation Register	EO	R/W	-	-	-	0	-	0	0	0
A3H	P4 Pull-up Resistor Selection Register	P4PU	R/W	-	-	-	-	0	0	0	0
A4H	External Interrupt Polarity 0 Low Register	EIPOL0L	R/W	0	0	0	0	0	0	0	0
A5H	External Interrupt Polarity 0 High Register	EIPOL0H	R/W	0	0	0	0	0	0	0	0
A6H	External Interrupt Flag 1 Register	EIFLAG1	R/W	0	0	0	0	0	0	0	0
A7H	External Interrupt Polarity 1 Register	EIPOL1	R/W	0	0	0	0	0	0	0	0
A8H	Interrupt Enable Register	IE	R/W	0	-	0	0	0	0	0	0
A9H	Interrupt Enable Register 1	IE1	R/W	-	-	0	0	0	0	-	0
AAH	Interrupt Enable Register 2	IE2	R/W	-	-	0	0	0	0	0	0
ABH	Interrupt Enable Register 3	IE3	R/W	-	-	0	0	0	0	0	0
ACH	P0 Pull-up Resistor Selection Register	P0PU	R/W	0	0	0	0	0	0	0	0
ADH	P1 Pull-up Resistor Selection Register	P1PU	R/W	0	0	0	0	0	0	0	0
AEH	P2 Pull-up Resistor Selection Register	P2PU	R/W	0	0	0	0	0	0	0	0
AFH	P3 Pull-up Resistor Selection Register	P3PU	R/W	0	0	0	0	0	0	0	0
B0H	P5 Data Register	P5	R/W	-	-	0	0	0	0	0	0
B1H	P1 Direction Register	P1IO	R/W	0	0	0	0	0	0	0	0
B2H	Timer 0 Control Register	T0CR	R/W	0	-	0	0	0	0	0	0
B3H	Timer 0 Counter Register	T0CNT	R	0	0	0	0	0	0	0	0
B4H	Timer 0 Data Register	T0DR	R/W	1	1	1	1	1	1	1	1
	Timer 0 Capture Data Register	T0CDR	R	0	0	0	0	0	0	0	0
B5H	SPI 2 Control Register	SPICR	R/W	0	0	0	0	0	0	0	0
B6H	SPI 2 Data Register	SPIDR	R/W	0	0	0	0	0	0	0	0
B7H	SPI 2 Status Register	SPISR	R/W	0	0	0	-	0	0	-	-
B8H	Interrupt Priority Register	IP	R/W	-	-	0	0	0	0	0	0
B9H	P2 Direction Register	P2IO	R/W	0	0	0	0	0	0	0	0
BAH	Timer 1 Control Low Register	T1CRL	R/W	0	0	0	0	-	0	0	0
BBH	Timer 1 Control High Register	T1CRH	R/W	0	-	0	0	-	-	-	0
BCH	Timer 1 A Data Low Register	T1ADRL	R/W	1	1	1	1	1	1	1	1
BDH	Timer 1 A Data High Register	T1ADRH	R/W	1	1	1	1	1	1	1	1
BEH	Timer 1 B Data Low Register	T1BDRL	R/W	1	1	1	1	1	1	1	1
BFH	Timer 1 B Data High Register	T1BDRH	R/W	1	1	1	1	1	1	1	1

Table 8.4 SFR Map (Continued)

Address	Function	Symbol	R/W	@Reset								
				7	6	5	4	3	2	1	0	
C0H	External Interrupt Flag 0 Register	EIFLAG0	R/W	0	0	0	0	0	0	0	0	0
C1H	P3 Direction Register	P3IO	R/W	0	0	0	0	0	0	0	0	0
C2H	Timer 2 Control Low Register	T2CRL	R/W	0	0	0	0	–	0	–	0	0
C3H	Timer 2 Control High Register	T2CRH	R/W	0	–	0	0	–	–	–	–	0
C4H	Timer 2 A Data Low Register	T2ADRL	R/W	1	1	1	1	1	1	1	1	1
C5H	Timer 2 A Data High Register	T2ADRH	R/W	1	1	1	1	1	1	1	1	1
C6H	Timer 2 B Data Low Register	T2BDRL	R/W	1	1	1	1	1	1	1	1	1
C7H	Timer 2 B Data High Register	T2BDRH	R/W	1	1	1	1	1	1	1	1	1
C8H	Oscillator Control Register	OSCCR	R/W	–	–	0	0	1	0	0	0	0
C9H	P4 Direction Register	P4IO	R/W	–	–	–	–	0	0	0	0	0
CAH	Reserved	–	–	–								
CBH	Reserved	–	–	–								
CCH	Reserved	–	–	–								
CDH	Reserved	–	–	–								
CEH	Reserved	–	–	–								
CFH	Reserved	–	–	–								
D0H	Program Status Word Register	PSW	R/W	0	0	0	0	0	0	0	0	0
D1H	P5 Direction Register	P5IO	R/W	–	–	0	0	0	0	0	0	0
D2H	P0 Function Selection Low Register	P0FSRL	R/W	–	0	0	0	0	0	0	0	0
D3H	P0 Function Selection High Register	P0FSRH	R/W	–	–	0	0	0	0	0	0	0
D4H	P1 Function Selection Low Register	P1FSRL	R/W	0	0	0	0	0	0	0	0	0
D5H	P1 Function Selection High Register	P1FSRH	R/W	0	0	0	0	0	0	0	0	0
D6H	P2 Function Selection Low Register	P2FSRL	R/W	–	–	0	0	0	0	0	0	0
D7H	P2 Function Selection High Register	P2FSRH	R/W	–	–	–	–	0	0	0	0	0
D8H	Low Voltage Reset Control Register	LVRCCR	R/W	0	–	–	0	0	0	0	0	0
D9H	USI0 Control Register 1	USI0CR1	R/W	0	0	0	0	0	0	0	0	0
DAH	USI0 Control Register 2	USI0CR2	R/W	0	0	0	0	0	0	0	0	0
DBH	USI0 Control Register 3	USI0CR3	R/W	0	0	0	0	0	0	0	0	0
DCH	USI0 Control Register 4	USI0CR4	R/W	0	–	–	0	0	–	0	0	0
DDH	USI0 Slave Address Register	USI0SAR	R/W	0	0	0	0	0	0	0	0	0
DEH	P0 Debounce Enable Register	P0DB	R/W	0	0	0	0	0	0	0	0	0
DFH	P1/P5 Debounce Enable Register	P15DB	R/W	–	–	0	0	0	0	0	0	0

Table 8.5 SFR Map (Continued)

Address	Function	Symbol	R/W	@Reset								
				7	6	5	4	3	2	1	0	
E0H	Accumulator Register	ACC	R/W	0	0	0	0	0	0	0	0	0
E1H	USI0 Status Register 1	USI0ST1	R/W	1	0	0	0	–	0	0	0	0
E2H	USI0 Status Register 2	USI0ST2	R	0	0	0	0	0	0	0	0	0
E3H	USI0 Baud Rate Generation Register	USI0BD	R/W	1	1	1	1	1	1	1	1	1
E4H	USI0 SDA Hold Time Register	USI0SDHR	R/W	0	0	0	0	0	0	0	0	1
E5H	USI0 Data Register	USI0DR	R/W	0	0	0	0	0	0	0	0	0
E6H	USI0 SCL Low Period Register	USI0SCLR	R/W	0	0	1	1	1	1	1	1	1
E7H	USI0 SCL High Period Register	USI0SCHR	R/W	0	0	1	1	1	1	1	1	1
E8H	Reset Flag Register	RSTFR	R/W	1	x	0	0	x	–	–	–	–
E9H	USI1 Control Register 1	USI1CR1	R/W	0	0	0	0	0	0	0	0	0
EAH	USI1 Control Register 2	USI1CR2	R/W	0	0	0	0	0	0	0	0	0
EBH	USI1 Control Register 3	USI1CR3	R/W	0	0	0	0	0	0	0	0	0
ECH	USI1 Control Register 4	USI1CR4	R/W	0	–	–	0	0	–	0	0	0
EDH	USI1 Slave Address Register	USI1SAR	R/W	0	0	0	0	0	0	0	0	0
EEH	P3 Function Selection Register	P3FSR	R/W	0	0	0	0	0	0	0	0	0
EFH	P4 Function Selection Register	P4FSR	R/W	–	0	0	0	0	0	0	0	0
F0H	B Register	B	R/W	0	0	0	0	0	0	0	0	0
F1H	USI1 Status Register 1	USI1ST1	R/W	1	0	0	0	–	0	0	0	0
F2H	USI1 Status Register 2	USI1ST2	R	0	0	0	0	0	0	0	0	0
F3H	USI1 Baud Rate Generation Register	USI1BD	R/W	1	1	1	1	1	1	1	1	1
F4H	USI1 SDA Hold Time Register	USI1SDHR	R/W	0	0	0	0	0	0	0	0	1
F5H	USI1 Data Register	USI1DR	R/W	0	0	0	0	0	0	0	0	0
F6H	USI1 SCL Low Period Register	USI1SCLR	R/W	0	0	1	1	1	1	1	1	1
F7H	USI1 SCL High Period Register	USI1SCHR	R/W	0	0	1	1	1	1	1	1	1
F8H	Interrupt Priority Register 1	IP1	R/W	–	–	0	0	0	0	0	0	0
F9H	Reserved	–	–	–								
FAH	Flash Sector Address High Register	FSADRH	R/W	–	–	–	–	0	0	0	0	0
FBH	Flash Sector Address Middle Register	FSADRM	R/W	0	0	0	0	0	0	0	0	0
FCH	Flash Sector Address Low Register	FSADRL	R/W	0	0	0	0	0	0	0	0	0
FDH	Flash Identification Register	FIDR	R/W	0	0	0	0	0	0	0	0	0
FEH	Flash Mode Control Register	FMCR	R/W	0	–	–	–	–	0	0	0	0
FFH	P5 Function Selection Register	P5FSR	R/W	–	–	0	0	0	0	0	0	0

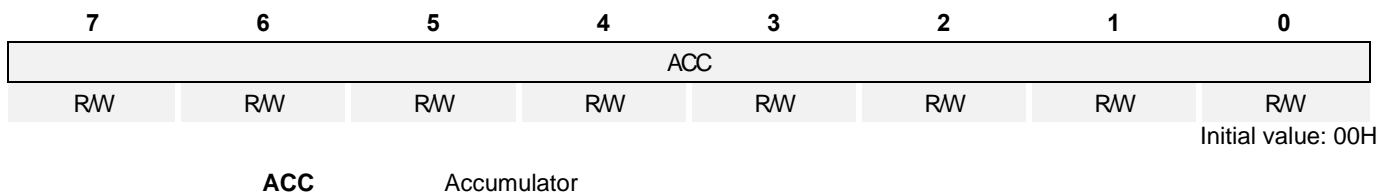
Table 8.6 SFR Map (Continued)

Address	Function	Symbol	R/W	@Reset								
				7	6	5	4	3	2	1	0	
1000H	Timer 3 Control Register	T3CR	R/W	0	–	0	0	0	0	0	0	0
1001H	Timer 3 Counter Register	T3CNT	R	0	0	0	0	0	0	0	0	0
	Timer 3 Data Register	T3DR	W	1	1	1	1	1	1	1	1	1
	Timer 3 Capture Data Register	T3CAPR	R	0	0	0	0	0	0	0	0	0
1002H	Timer 4 Control Register	T4CR	R/W	0	0	0	0	0	0	0	0	0
1003H	Timer 4 PWM Control Register 1	T4PCR1	R/W	0	0	0	0	0	0	0	0	0
1004H	Timer 4 PWM Control Register 2	T4PCR2	R/W	0	0	0	0	0	0	0	0	0
1005H	Timer 4 PWM Control Register 3	T4PCR3	R/W	–	0	0	0	–	–	–	–	–
1006H	Timer 4 Interrupt Status Register	T4ISR	R/W	0	0	0	0	0	–	–	–	–
1007H	Timer 4 Interrupt Mask Register	T4MSK	R/W	0	0	0	0	0	–	–	–	–
1008H	Timer 4 PWM Period Low Register	T4PPRL	R/W	1	1	1	1	1	1	1	1	1
1009H	Timer 4 PWM Period High Register	T4PPRH	R/W	–	–	–	–	–	–	–	0	0
100AH	Timer 4 PWM A Duty Low Register	T4ADRL	R/W	0	1	1	1	1	1	1	1	1
100BH	Timer 4 PWM A Duty High Register	T4ADRH	R/W	–	–	–	–	–	–	–	0	0
100CH	Timer 4 PWM B Duty Low Register	T4BDRL	R/W	0	1	1	1	1	1	1	1	1
100DH	Timer 4 PWM B Duty High Register	T4BDRH	R/W	–	–	–	–	–	–	–	0	0
100EH	Timer 4 PWM C Duty Low Register	T4CDRL	R/W	0	1	1	1	1	1	1	1	1
100FH	Timer 4 PWM C Duty High Register	T4CDRH	R/W	–	–	–	–	–	–	–	0	0
1010H	Timer 4 PWM A Delay Register	T4DLYA	R/W	0	0	0	0	0	0	0	0	0
1011H	Timer 4 PWM B Delay Register	T4DLYB	R/W	0	0	0	0	0	0	0	0	0
1012H	Timer 4 PWM C Delay Register	T4DLYC	R/W	0	0	0	0	0	0	0	0	0
1013H	Timer 4 Data Register	T4DR	R/W	1	1	1	1	1	1	1	1	1
1014H	Timer 4 Capture Data Register	T4CAPR	R	0	0	0	0	0	0	0	0	0
1015H	Timer 4 Counter Register	T4CNT	R	0	0	0	0	0	0	0	0	0
.....												
1038H	X-tal Filter Selection Register	XTFLSR	R/W	0	0	0	0	0	–	–	–	0
.....												
107FH	Reserved	–	–	–								

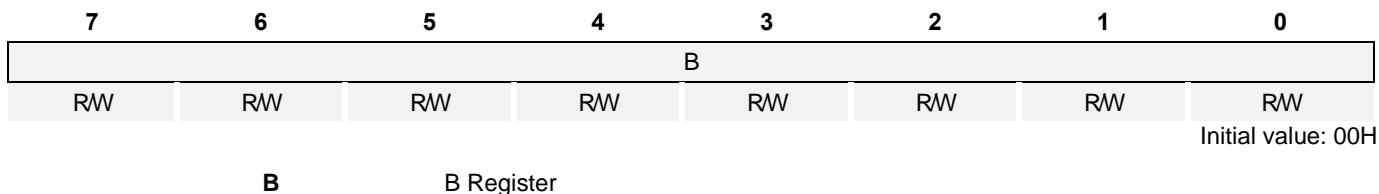
Table 8.7 XSFR Map (Conclude)

8.4.3 SFR Map

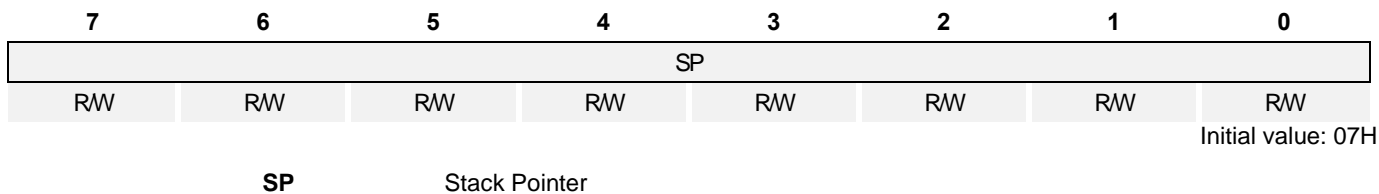
**ACC (Accumulator Register): E0H**



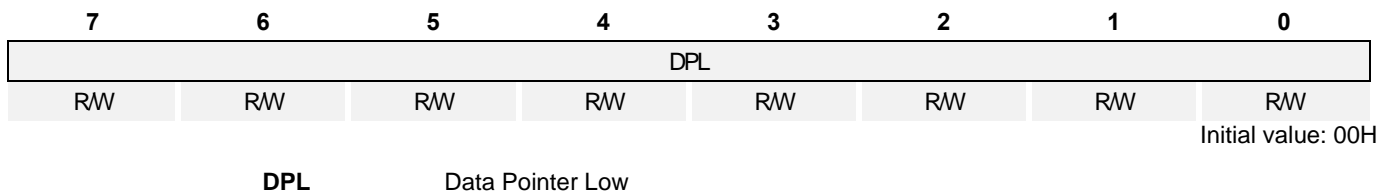
**B (B Register): F0H**



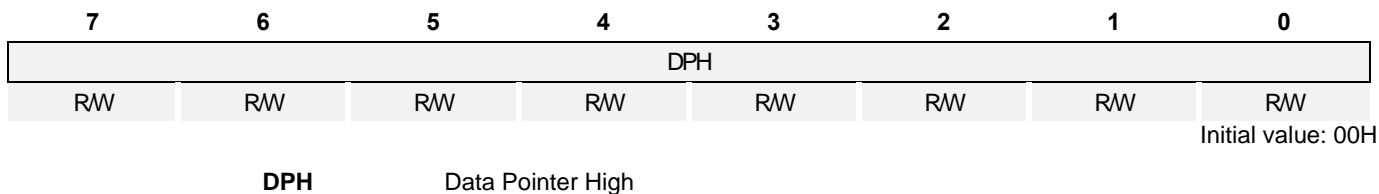
**SP (Stack Pointer): 81H**



**DPL (Data Pointer Register Low): 82H**



**DPH (Data Pointer Register High): 83H**



**DPL1 (Data Pointer Register Low 1): 84H**

7	6	5	4	3	2	1	0
DPL1							
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**DPL1**            Data Pointer Low 1

**DPH1 (Data Pointer Register High 1): 85H**

7	6	5	4	3	2	1	0
DPH1							
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**DPH1**            Data Pointer High 1

**PSW (Program Status Word Register): D0H**

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	F1	P
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

- CY**            Carry Flag
- AC**            Auxiliary Carry Flag
- F0**            General Purpose User-Definable Flag
- RS1**          Register Bank Select bit 1
- RS0**          Register Bank Select bit 0
- OV**            Overflow Flag
- F1**            User-Definable Flag
- P**             Parity Flag. Set/Cleared by hardware each instruction cycle to indicate an odd/even number of '1' bits in the accumulator

**EO (Extended Operation Register): A2H**

7	6	5	4	3	2	1	0
-	-	-	TRAP_EN	-	DPSEL2	DPSEL1	DPSEL0
-	-	-	RW	-	RW	RW	RW

Initial value: 00H

- TRAP\_EN**      Select the Instruction (**Keep always '0'**).
  - 0            Select MOV<sub>C</sub> @(DPTR++), A
  - 1            Select Software TRAP Instruction
- DPSEL[2:0]**    Select Banked Data Pointer Register
 

DPSEL2	DPSEL1	DPSEL0	Description
0	0	0	DPTR0
0	0	1	DPTR1
Reserved			

## 9 I/O Ports

### 9.1 I/O Ports

The MC96F6432A has six groups of I/O ports (P0 ~ P5). Each port can be easily configured by software as I/O pin, internal pull up and open-drain pin to meet various system configurations and design requirements. Also P0 includes function that can generate interrupt according to change of state of the pin.

### 9.2 Port Register

#### 9.2.1 Data Register (Px)

Data Register is a bidirectional I/O port. If ports are configured as output ports, data can be written to the corresponding bit of the Px. If ports are configured as input ports, the data can be read from the corresponding bit of the Px.

#### 9.2.2 Direction Register (PxIO)

Each I/O pin can be independently used as an input or an output through the PxIO register. Clearing bits in this register will make the corresponding pin of Px as an input mode. Set bits of this register will make the pin to output mode. Almost bits are cleared by a system reset, but some bits are set by a system reset.

#### 9.2.3 Pull-up Resistor Selection Register (PxPU)

The on-chip pull-up resistor can be connected to I/O ports individually with a pull-up resistor selection register (PxPU). The pull-up register selection controls the pull-up resistor enable/disable of each port. When the corresponding bit is 1, the pull-up resistor of the pin is enabled. When 0, the pull-up resistor is disabled. All bits are cleared by a system reset.

#### 9.2.4 Open-drain Selection Register (PxOD)

There are internally open-drain selection registers (PxOD) for P0 ~ P4 and a bit for P5. The open-drain selection register controls the open-drain enable/disable of each port. Almost ports become push-pull by a system reset, but some ports become open-drain by a system reset.

#### 9.2.5 De-bounce Enable Register (PxDB)

P0[7:2], P1[2:1], P1[7:6], P52 and P54 support debounce function. De-bounce clocks of each ports are  $fx/1$ ,  $fx/4$  and  $fx/4096$ .



## 9.2.6 Port Function Selection Register (PxFSR)

These registers define alternative functions of ports. Please remember that these registers should be set properly for alternative port function. A reset clears the PxFSR register to '00H', which makes all pins to normal I/O ports.

## 9.2.7 Register Map

Name	Address	Direction	Default	Description
P0	80H	R/W	00H	P0 Data Register
P0IO	A1H	R/W	00H	P0 Direction Register
P0PU	ACH	R/W	00H	P0 Pull-up Resistor Selection Register
P0OD	91H	R/W	00H	P0 Open-drain Selection Register
P0DB	DEH	R/W	00H	P0 De-bounce Enable Register
P0FSRH	D3H	R/W	00H	P0 Function Selection High Register
P0FSRL	D2H	R/W	00H	P0 Function Selection Low Register
P1	88H	R/W	00H	P1 Data Register
P1IO	B1H	R/W	00H	P1 Direction Register
P1PU	ADH	R/W	00H	P1 Pull-up Resistor Selection Register
P1OD	92H	R/W	00H	P1 Open-drain Selection Register
P15DB	DFH	R/W	00H	P1/P5 Debounce Enable Register
P1FSRH	D5H	R/W	00H	P1 Function Selection High Register
P1FSRL	D4H	R/W	00H	P1 Function Selection Low Register
P2	90H	R/W	00H	P2 Data Register
P2IO	B9H	R/W	00H	P2 Direction Register
P2PU	AEH	R/W	00H	P2 Pull-up Resistor Selection Register
P2OD	93H	R/W	00H	P2 Open-drain Selection Register
P2FSRH	D7H	R/W	00H	P2 Function Selection High Register
P2FSRL	D6H	R/W	00H	P2 Function Selection Low Register
P3	98H	R/W	00H	P3 Data Register
P3IO	C1H	R/W	00H	P3 Direction Register
P3PU	AFH	R/W	00H	P3 Pull-up Resistor Selection Register
P3FSR	EEH	R/W	00H	P3 Function Selection Register
P4	A0H	R/W	00H	P4 Data Register
P4IO	C9H	R/W	00H	P4 Direction Register
P4PU	A3H	R/W	00H	P4 Pull-up Resistor Selection Register
P4OD	94H	R/W	00H	P4 Open-drain Selection Register
P4FSR	EFH	R/W	00H	P4 Function Selection Register
P5	B0H	R/W	00H	P5 Data Register
P5IO	D1H	R/W	00H	P5 Direction Register
P5PU	95H	R/W	00H	P5 Pull-up Resistor Selection Register
P5FSR	FFH	R/W	00H	P5 Function Selection Register

**Table 9.1** Port Register Map

### 9.3 P0 Port

#### 9.3.1 P0 Port Description

P0 is 8-bit I/O port. P0 control registers consist of P0 data register (P0), P0 direction register (P0IO), debounce enable register (P0DB), P0 pull-up resistor selection register (P0PU) and P0 open-drain selection register (P0OD). Refer to the port function selection registers for the P0 function selection.

#### 9.3.2 Register description for P0

##### P0 (P0 Data Register): 80H

7	6	5	4	3	2	1	0
P07	P06	P05	P04	P03	P02	P01	P00
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**P0[7:0]** I/O Data

##### P0IO (P0 Direction Register): A1H

7	6	5	4	3	2	1	0
P07IO	P06IO	P05IO	P04IO	P03IO	P02IO	P01IO	P00IO
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**P0IO[7:0]** P0 Data I/O Direction.

- 0 Input
- 1 Output

**NOTE)**

1. EC3/EINT0 ~ EINT5 function possible when input

##### P0PU (P0 Pull-up Resistor Selection Register): ACH

7	6	5	4	3	2	1	0
P07PU	P06PU	P05PU	P04PU	P03PU	P02PU	P01PU	P00PU
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**P0PU[7:0]** Configure Pull-up Resistor of P0 Port

- 0 Disable
- 1 Enable

**P0OD (P0 Open-drain Selection Register): 91H**

7	6	5	4	3	2	1	0
P07OD	P06OD	P05OD	P04OD	P03OD	P02OD	P01OD	P00OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

**P0OD[7:0]** Configure Open-drain of P0 Port  
 0 Push-pull output  
 1 Open-drain output

**P0DB (P0 De-bounce Enable Register): DEH**

7	6	5	4	3	2	1	0
DBCLK1	DBCLK0	P07DB	P06DB	P05DB	P04DB	P03DB	P02DB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

**DBCLK[1:0]** Configure De-bounce Clock of Port  
 DBCLK1 DBCLK0 Description  
 0 0 fx/1  
 0 1 fx/4  
 1 0 fx/4096  
 1 1 Reserved

**P07DB** Configure De-bounce of P07 Port  
 0 Disable  
 1 Enable

**P06DB** Configure De-bounce of P06 Port  
 0 Disable  
 1 Enable

**P05DB** Configure De-bounce of P05 Port  
 0 Disable  
 1 Enable

**P04DB** Configure De-bounce of P04 Port  
 0 Disable  
 1 Enable

**P03DB** Configure De-bounce of P03 Port  
 0 Disable  
 1 Enable

**P02DB** Configure De-bounce of P02 Port  
 0 Disable  
 1 Enable

**NOTE)**

1. If the same level is not detected on enabled pin three or four times in a row at the sampling clock, the signal is eliminated as noise.
2. A pulse level should be input for the duration of 3 clock or more to be actually detected as a valid edge.
3. The port de-bounce is automatically disabled at stop mode and recovered after stop mode release.

**P0FSRH (Port 0 Function Selection High Register): D3H**

7	6	5	4	3	2	1	0
–	–	P0FSRH5	P0FSRH4	P0FSRH3	P0FSRH2	P0FSRH1	P0FSRH0
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

- P0FSRH[5:4]** P07 Function Select
 

P0FSRH5	P0FSRH4	Description
0	0	I/O Port (EINT5 function possible when input)
0	1	SEG22 Function
1	0	AN5 Function
1	1	PWM4CB Function
  
- P0FSRH[3:2]** P06 Function Select
 

P0FSRH3	P0FSRH2	Description
0	0	I/O Port (EINT4 function possible when input)
0	1	SEG23 Function
1	0	AN4 Function
1	1	PWM4CA Function
  
- P0FSRH[1:0]** P05 Function Select
 

P0FSRH1	P0FSRH0	Description
0	0	I/O Port (EINT3 function possible when input)
0	1	SEG24 Function
1	0	AN3 Function
1	1	PWM4BB Function

**P0FSRL (Port 0 Function Selection Low Register): D2H**

7	6	5	4	3	2	1	0
–	P0FSRL6	P0FSRL5	P0FSRL4	P0FSRL3	P0FSRL2	P0FSRL1	P0FSRL0
–	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

<b>P0FSRL[6:5]</b>	P04 Function Select	
	P0FSRL6	P0FSRL5
	Description	
	0	0
	I/O Port(EINT2 function possible when input)	
	0	1
	SEG25 Function	
	1	0
	AN2 Function	
	1	1
	PWM4BA Function	
<b>P0FSRL[4:3]</b>	P03 Function Select	
	P0FSRL4	P0FSRL3
	Description	
	0	0
	I/O Port(EINT1 function possible when input)	
	0	1
	SEG26 Function	
	1	0
	AN1 Function	
	1	1
	PWM4AB Function	
<b>P0FSRL[2:1]</b>	P02 Function Select	
	P0FSRL2	P0FSRL1
	Description	
	0	0
	I/O Port (EINT0 function possible when input)	
	0	1
	AVREF Function	
	1	0
	AN0 Function	
	1	1
	T4O/PWM4A Function	
<b>P0FSRL0</b>	P01 Function Select	
	0	I/O Port
	1	T3O Function

## 9.4 P1 Port

### 9.4.1 P1 Port Description

P1 is 8-bit I/O port. P1 control registers consist of P1 data register (P1), P1 direction register (P1IO), debounce enable register (P15DB), P1 pull-up resistor selection register (P1PU) and P1 open-drain selection register (P1OD). Refer to the port function selection registers for the P1 function selection.

### 9.4.2 Register description for P1

#### P1 (P1 Data Register): 88H

7	6	5	4	3	2	1	0
P17	P16	P15	P14	P13	P12	P11	P10
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

P1[7:0] I/O Data

#### P1IO (P1 Direction Register): B1H

7	6	5	4	3	2	1	0
P17IO	P16IO	P15IO	P14IO	P13IO	P12IO	P11IO	P10IO
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

P1IO[7:0] P1 Data I/O Direction  
 0 Input  
 1 Output

**NOTE)**

1. EINT6/ENINT7/EINT11/EINT12/SS2/EC1 function possible when input

#### P1PU (P1 Pull-up Resistor Selection Register): ADH

7	6	5	4	3	2	1	0
P17PU	P16PU	P15PU	P14PU	P13PU	P12PU	P11PU	P10PU
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

P1PU[7:0] Configure Pull-up Resistor of P1 Port  
 0 Disable  
 1 Enable

**P1OD (P1 Open-drain Selection Register): 92H**

7	6	5	4	3	2	1	0
P17OD	P16OD	P15OD	P14OD	P13OD	P12OD	P11OD	P10OD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 08H

**P1OD[7:0]** Configure Open-drain of P1 Port  
 0 Push-pull output  
 1 Open-drain output

**P15DB (P1/P5 De-bounce Enable Register): DFH**

7	6	5	4	3	2	1	0
–	–	P54DB	P52DB	P17DB	P16DB	P12DB	P11DB
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

**P54DB** Configure De-bounce of P54 Port  
 0 Disable  
 1 Enable

**P52DB** Configure De-bounce of P52 Port  
 0 Disable  
 1 Enable

**P17DB** Configure De-bounce of P17 Port  
 0 Disable  
 1 Enable

**P16DB** Configure De-bounce of P16 Port  
 0 Disable  
 1 Enable

**P12DB** Configure De-bounce of P12 Port  
 0 Disable  
 1 Enable

**P11DB** Configure De-bounce of P11 Port  
 0 Disable  
 1 Enable

**NOTE)**

1. If the same level is not detected on enabled pin three or four times in a row at the sampling clock, the signal is eliminated as noise.
2. A pulse level should be input for the duration of 3 clock or more to be actually detected as a valid edge.
3. The port de-bounce is automatically disabled at stop mode and recovered after stop mode release.
4. Refer to the port 0 de-bounce enable register (P0DB) for the de-bounce clock of port 1 and port 5.

**P1FSRH (Port 1 Function Selection High Register): D5H**

7	6	5	4	3	2	1	0
P1FSRH7	P1FSRH6	P1FSRH5	P1FSRH4	P1FSRH3	P1FSRH2	P1FSRH1	P1FSRH0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

- P1FSRH[7:6]** P17 Function Select
 

P1FSRH7	P1FSRH6	Description
0	0	I/O Port(EINT6/SS2 function possible when input)
0	1	SEG21 Function
1	0	AN6 Function
1	1	Not used
  
- P1FSRH[5:4]** P16 Function Select
 

P1FSRH5	P1FSRH4	Description
0	0	I/O Port (EINT7 function possible when input)
0	1	SEG20 Function
1	0	AN7 Function
1	1	SCK2 Function
  
- P1FSRH[3:2]** P15 Function Select
 

P1FSRH3	P1FSRH2	Description
0	0	I/O Port
0	1	SEG19 Function
1	0	AN8 Function
1	1	MISO2 Function
  
- P1FSRH[1:0]** P14 Function Select
 

P1FSRH1	P0FSRH0	Description
0	0	I/O Port
0	1	SEG18 Function
1	0	AN9 Function
1	1	MOSI2 Function



**P1FSRL (Port 1 Function Selection Low Register): D4H**

7	6	5	4	3	2	1	0
P1FSRL7	P1FSRL6	P1FSRL5	P1FSRL4	P1FSRL3	P1FSRL2	P1FSRL1	P1FSRL0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**P1FSRL[7:6]** P13 Function Select

P1FSRL7	P1FSRL6	Description
0	0	I/O Port(EC1 function possible when input)
0	1	SEG17 Function
1	0	AN10 Function
1	1	BUZO Function

**P1FSRL[5:4]** P12 Function Select

P1FSRL5	P1FSRL4	Description
0	0	I/O Port(EINT11 function possible when input)
0	1	SEG16 Function
1	0	AN11 Function
1	1	T10/PWM1O Function

**P1FSRL[3:2]** P11 Function Select

P1FSRL3	P1FSRL2	Description
0	0	I/O Port(EINT12 function possible when input)
0	1	SEG15 Function
1	0	AN12 Function
1	1	T20/PWM2O Function

**P1FSRL[1:0]** P10 Function Select

P1FSRL1	P1FSRL0	Description
0	0	I/O Port
0	1	SEG14 Function
1	0	AN13 Function
1	1	RXD1/SCL1/MISO1 Function

## 9.5 P2 Port

### 9.5.1 P2 Port Description

P2 is 8-bit I/O port. P2 control registers consist of P2 data register (P2), P2 direction register (P2IO), P2 pull-up resistor selection register (P2PU) and P2 open-drain selection register (P2OD). Refer to the port function selection registers for the P2 function selection.

### 9.5.2 Register description for P2

#### P2 (P2 Data Register): 90H

7	6	5	4	3	2	1	0
P27	P26	P25	P24	P23	P22	P21	P20
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

P2[7:0] I/O Data

#### P2IO (P2 Direction Register): B9H

7	6	5	4	3	2	1	0
P27IO	P26IO	P25IO	P24IO	P23IO	P22IO	P21IO	P20IO
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

P2IO[7:0] P2 Data I/O Direction  
 0 Input  
 1 Output

**NOTE)**

1. SS1 function possible when input

**P2PU (P2 Pull-up Resistor Selection Register): AEH**

7	6	5	4	3	2	1	0
P27PU	P26PU	P25PU	P24PU	P23PU	P22PU	P21PU	P20PU
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**P2PU[7:0]**      Configure Pull-up Resistor of P2 Port  
 0      Disable  
 1      Enable

**P2OD (P2 Open-drain Selection Register): 93H**

7	6	5	4	3	2	1	0
P27OD	P26OD	P25OD	P24OD	P23OD	P22OD	P21OD	P20OD
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**P2OD[7:0]**      Configure Open-drain of P2 Port  
 0      Push-pull output  
 1      Open-drain output

**P2FSRH (Port 2 Function Selection High Register): D7H**

7	6	5	4	3	2	1	0
–	–	–	–	P2FSRH3	P2FSRH2	P2FSRH1	P2FSRH0
–	–	–	–	RW	RW	RW	RW

Initial value: 00H

- P2FSRH3** P27 Function select
  - 0 I/O Port
  - 1 SEG6 Function
- P2FSRH2** P26 Function Select
  - 0 I/O Port
  - 1 SEG7 Function
- P2FSRH1** P25 Function select
  - 0 I/O Port
  - 1 SEG8 Function
- P2FSRH0** P24 Function Select
  - 0 I/O Port
  - 1 SEG9 Function

**P2FSRL (Port 2 Function Selection Low Register): D6H**

7	6	5	4	3	2	1	0
–	–	P2FSRL5	P2FSRL4	P2FSRL3	P2FSRL2	P2FSRL1	P2FSRL0
–	–	RW	RW	RW	RW	RW	RW

Initial value: 00H

- P2FSRL5** P23 Function Select
  - 0 I/O Port
  - 1 SEG10 Function
- P2FSRL4** P22 Function Select
  - 0 I/O Port(SS1 function possible when input)
  - 1 SEG11 Function
- P2FSRL[3:2]** P21 Function Select
 

P2FSRL3	P2FSRL2	Description
0	0	I/O Port
0	1	SEG12 Function
1	0	AN15 Function
1	1	SCK1 Function
- P2FSRL[1:0]** P20 Function Select
 

P2FSRL1	P1FSRL0	Description
0	0	I/O Port
0	1	SEG13 Function
1	0	AN14 Function
1	1	TXD1/SDA1/MOSI1 Function

## 9.6 P3 Port

### 9.6.1 P3 Port Description

P3 is 8-bit I/O port. P3 control registers consist of P3 data register (P3), P3 direction register (P3IO) and P3 pull-up resistor selection register (P3PU). Refer to the port function selection registers for the P3 function selection.

### 9.6.2 Register description for P3

#### P3 (P3 Data Register): 98H

7	6	5	4	3	2	1	0
P37	P36	P35	P34	P33	P32	P31	P30
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**P3[7:0]** I/O Data

#### P3IO (P3 Direction Register): C1H

7	6	5	4	3	2	1	0
P37IO	P36IO	P35IO	P34IO	P33IO	P32IO	P31IO	P30IO
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**P3IO[7:0]** P3 Data I/O Direction  
 0 Input  
 1 Output

#### P3PU (P3 Pull-up Resistor Selection Register): AFH

7	6	5	4	3	2	1	0
P37PU	P36PU	P35PU	P34PU	P33PU	P32PU	P31PU	P30PU
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**P3PU[7:0]** Configure Pull-up Resistor of P3 Port  
 0 Disable  
 1 Enable

**P3FSR (Port 3 Function Selection Register): EEH**

7	6	5	4	3	2	1	0
P3FSR7	P3FSR6	P3FSR5	P3FSR4	P3FSR3	P3FSR2	P3FSR1	P3FSR0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

- P3FSR7** P37 Function select
  - 0 I/O Port
  - 1 COM0 Function
- P3FSR6** P36 Function Select
  - 0 I/O Port
  - 1 COM1 Function
- P3FSR5** P35 Function select
  - 0 I/O Port
  - 1 COM2/SEG0 Function
- P3FSR4** P34 Function Select
  - 0 I/O Port
  - 1 COM3/SEG1 Function
- P3FSR3** P33 Function select
  - 0 I/O Port
  - 1 COM4/SEG2 or COM0 Function
- P3FSR2** P32 Function Select
  - 0 I/O Port
  - 1 COM5/SEG3 or COM1 Function
- P3FSR1** P31 Function select
  - 0 I/O Port
  - 1 COM6/SEG4 or COM2/SEG4 Function
- P3FSR0** P30 Function Select
  - 0 I/O Port
  - 1 COM7/SEG5 or COM3/SEG5 Function

**NOTE)**

1. The P30-P35 is automatically configured as common or segment signal according to the duty in the LCDCTRL register when the pin is selected as the sub-function for common/segment.
2. The COM0-COM3 signals can be outputted through the P33-P30 pins. Refer to the LCD drive control high register (LCDCRH).

## 9.7 P4 Port

### 9.7.1 P4 Port Description

P4 is 4-bit I/O port. P4 control registers consist of P4 data register (P4), P4 direction register (P4IO), P4 pull-up resistor selection register (P4PU) and P4 open-drain selection register (P4OD). Refer to the port function selection registers for the P4 function selection.

### 9.7.2 Register description for P4

#### P4 (P4 Data Register): A0H

7	6	5	4	3	2	1	0
–	–	–	–	P43	P42	P41	P40
–	–	–	–	RW	RW	RW	RW

Initial value: 00H

P4[3:0] I/O Data

#### P4IO (P4 Direction Register): C9H

7	6	5	4	3	2	1	0
–	–	–	–	P43IO	P42IO	P41IO	P40IO
–	–	–	–	RW	RW	RW	RW

Initial value: 00H

P4IO[3:0] P4 Data I/O Direction  
 0 Input  
 1 Output

**NOTE)**

1. SS0 function possible when input

#### P4PU (P4 Pull-up Resistor Selection Register): A3H

7	6	5	4	3	2	1	0
–	–	–	–	P43PU	P42PU	P41PU	P40PU
–	–	–	–	RW	RW	RW	RW

Initial value: 00H

P4PU[3:0] Configure Pull-up Resistor of P4 Port  
 0 Disable  
 1 Enable

**P4OD (P4 Open-drain Selection Register): 94H**

7	6	5	4	3	2	1	0
–	–	–	–	P43OD	P42OD	P41OD	P40OD
–	–	–	–	RW	RW	RW	RW

Initial value: 00H

**P4OD[3:0]** Configure Open-drain of P4 Port  
 0 Push-pull output  
 1 Open-drain output

**P4FSR (Port 4 Function Selection Register): EFH**

7	6	5	4	3	2	1	0
–	P4FSR6	P4FSR5	P4FSR4	P4FSR3	P4FSR2	P4FSR1	P4FSR0
–	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

**P4FSR6** P43 Function Select  
 0 I/O Port(SS0 function possible when input)  
 1 VLC0 Function

**P4FSR[5:4]** P42 Function Select

P4FSR5	P4FSR4	Description
0	0	I/O Port
0	1	VLC1 Function
1	0	SCK0 Function
1	1	Not used

**P4FSR[3:2]** P41 Function Select

P4FSR3	P4FSR2	Description
0	0	I/O Port
0	1	VLC2 Function
1	0	TXD0/SDA0/MOSI0 Function
1	1	Not used

**P4FSR6[1:0]** P40 Function Select

P4FSR1	P4FSR0	Description
0	0	I/O Port
0	1	VLC3 Function
1	0	RXD0/SCL0/MISO0 Function
1	1	Not used



## 9.8 P5 Port

### 9.8.1 P5 Port Description

P5 is 6-bit I/O port. P5 control registers consist of P5 data register (P5), P5 direction register (P5IO) and P5 pull-up resistor selection register (P5PU). Refer to the port function selection registers for the P5 function selection.

### 9.8.2 Register description for P5

#### P5 (P5 Data Register): B0H

7	6	5	4	3	2	1	0
–	–	P55	P54	P53	P52	P51	P50
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

**P5[5:0]** I/O Data

#### P5IO (P5 Direction Register): D1H

7	6	5	4	3	2	1	0
–	–	P55IO	P54IO	P53IO	P52IO	P51IO	P50IO
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

**P5IO[5:0]** P5 Data I/O Direction  
 0 Input  
 1 Output

**NOTE)**

1. EC0/EINT8/EINT10/BLNK function possible when input

#### P5PU (P5 Pull-up Resistor Selection Register): 95H

7	6	5	4	3	2	1	0
–	–	P55PU	P54PU	P53PU	P52PU	P51PU	P50PU
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

**P5PU[5:0]** Configure Pull-up Resistor of P5 Port  
 0 Disable  
 1 Enable

**P5FSR (Port 5 Function Selection Register): FFH**

7	6	5	4	3	2	1	0
–	–	P5FSR5	P5FSR4	P5FSR3	P5FSR2	P5FSR1	P5FSR0
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

<b>P5FSR5</b>	P54 Function Select		
0	I/O Port(EINT10 function possible when input)		
1	SXOUT Function		
<b>P5FSR[4:3]</b>	P53 Function Select		
P5FSR4	P5FSR3	Description	
0	0	I/O Port	
0	1	SXIN Function	
1	0	T00/PWM00 Function	
1	1	Not used	
<b>P5FSR2</b>	P51 Function Select		
0	I/O Port		
1	XIN Function		
<b>P5FSR[1:0]</b>	P50 Function Select		
P5FSR1	P5FSR0	Description	
0	0	I/O Port	
0	1	XOUT Function	
1	0	Not used	
1	1	Not used	

**NOTE)**

1. Refer to the configure option for the P55/RESETB.

## 10 Interrupt Controller

### 10.1 Overview

The MC96F6432A supports up to 23 interrupt sources. The interrupts have separate enable register bits and allows software control. They can also have four levels of priority assigned to them. The non-maskable interrupt source is always enabled with a higher priority than any other interrupt source and is not controllable by software. The interrupt controller has following features:

- The request from 23 interrupt source
- 6 group priority
- 4 priority levels
- Multi Interrupt possibility
- If the requests of different priority levels are received simultaneously, the request of higher priority level is served first.
- Each interrupt source can be controlled by EA bit and each IEx bit
- Interrupt latency: 3~9 machine cycles in single interrupt system

The maskable interrupts are enabled through four pair of interrupt enable registers (IE, IE1, IE2, IE3). Bits of IE, IE1, IE2, IE3 register individually enable/disable a particular interrupt source. Overall interrupts are controlled by EA (bit 7 of IE). When EA is set to '0', all interrupts are disabled: when EA is set to '1', interrupts are individually enabled or disabled through the other bits of the interrupt enable registers. The EA bit is always cleared to '0' jumping to an interrupt service vector and set to '1' executing the [RETI] instruction. The MC96F6432A supports a four-level priority scheme. Each maskable interrupt is individually assigned to one of four priority levels according to IP and IP1.

Default interrupt mode is level-trigger mode basically, but if needed, it is possible to change to edge-trigger mode. Table 10.1 shows the Interrupt Group Priority Level that is available for sharing interrupt priority. Priority of a group is set by two bits of interrupt priority registers (one bit from IP, another one from IP1). Interrupt service routine serves higher priority interrupt first. If two requests of different priority levels are received simultaneously, the request of higher priority level is served prior to the lower one.

Interrupt Group	Highest <span style="float: right;">Lowest</span>				
	→				
0 (Bit0)	Interrupt 0	Interrupt 6	Interrupt 12	Interrupt 18	Highest      Lowest
1 (Bit1)	Interrupt 1	Interrupt 7	Interrupt 13	Interrupt 19	
2 (Bit2)	Interrupt 2	Interrupt 8	Interrupt 14	Interrupt 20	
3 (Bit3)	Interrupt 3	Interrupt 9	Interrupt 15	Interrupt 21	
4 (Bit4)	Interrupt 4	Interrupt 10	Interrupt 16	Interrupt 22	
5 (Bit5)	Interrupt 5	Interrupt 11	Interrupt 17	Interrupt 23	

Table 10.1 Interrupt Group Priority Level

## 10.2 External Interrupt

The external interrupt on INT0, INT1, INT5, INT6 and INT11 pins receive various interrupt request depending on the external interrupt polarity 0 high/low register (EIPOL0H/L) and external interrupt polarity 1 register (EIPOL1) as shown in Figure 10.1. Also each external interrupt source has enable/disable bits. The External interrupt flag 0 register (EIFLAG0) and external interrupt flag 1 register 1 (EIFLAG1) provides the status of external interrupts.

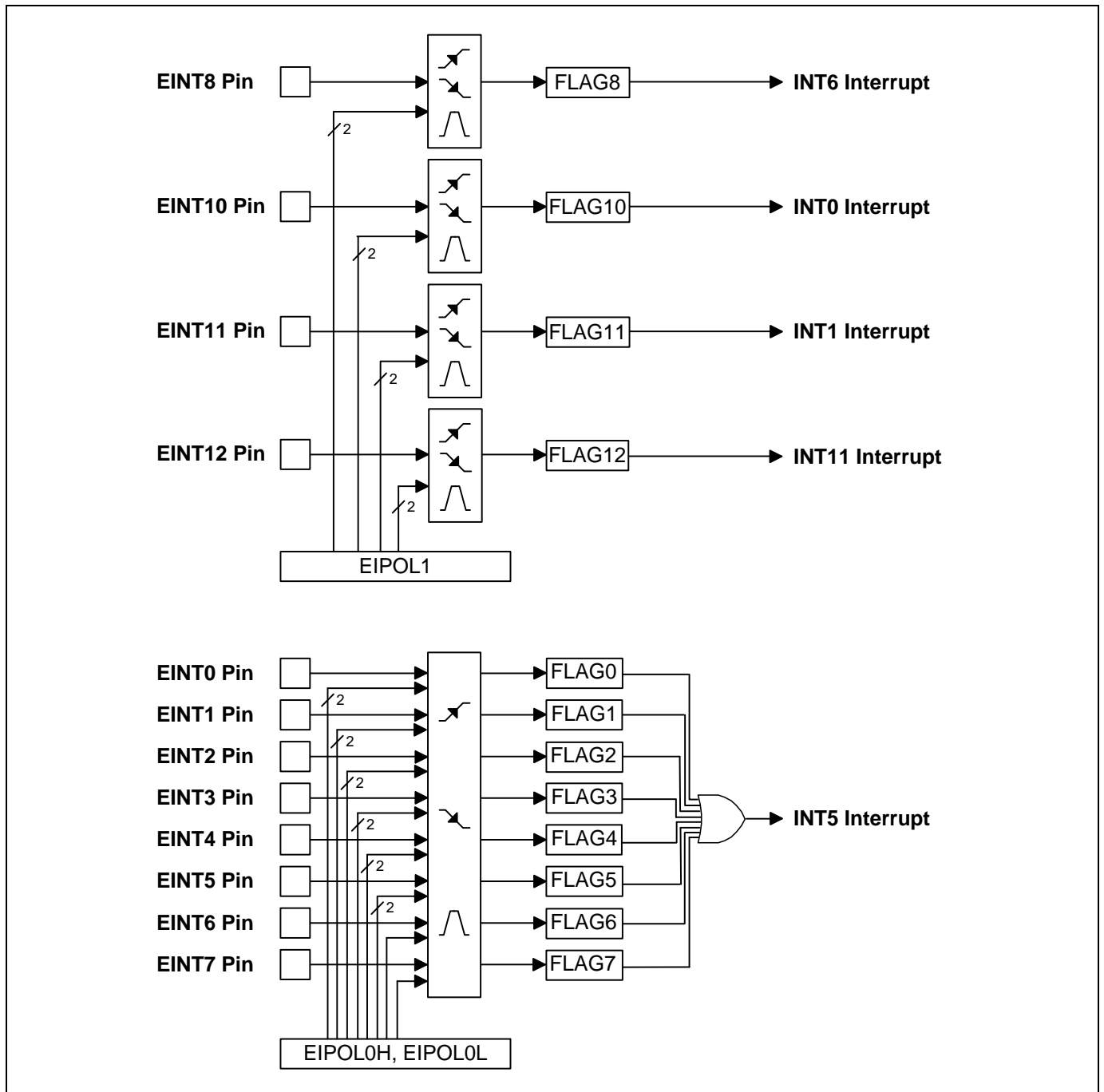


Figure 10.1 External Interrupt Description

### 10.3 Block Diagram

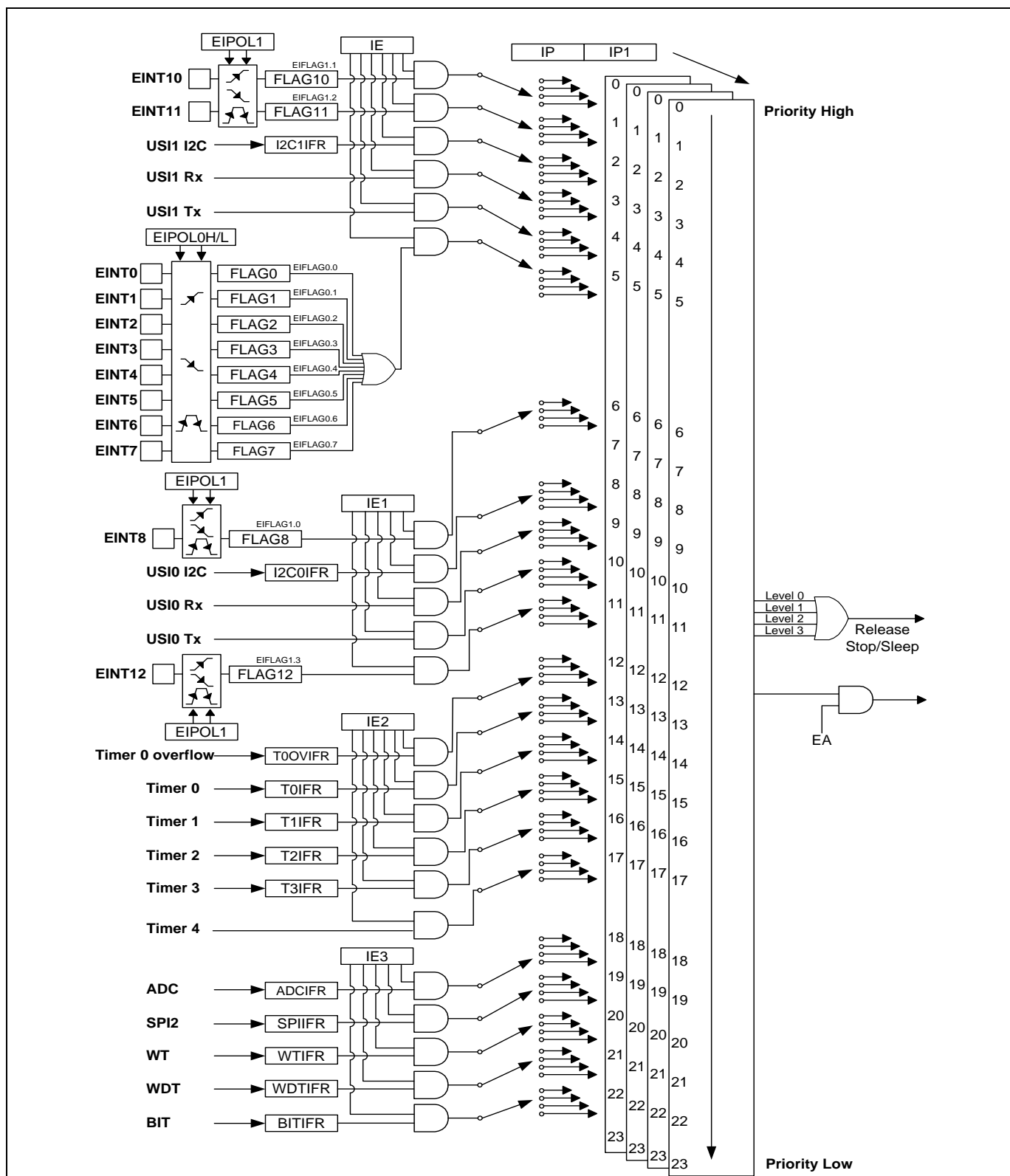


Figure 10.2 Block Diagram of Interrupt

NOTE)

1. The release signal for stop/idle mode may be generated by all interrupt sources which are enabled without reference to the priority level.
2. An interrupt request is delayed while data are written to IE, IE1, IE2, IE3, IP, IP1 and PCON register.

## 10.4 Interrupt Vector Table

The interrupt controller supports 24 interrupt sources as shown in the Table 10.2. When interrupt is served, long call instruction (LCALL) is executed and program counter jumps to the vector address. All interrupt requests have a decided priority order.

Interrupt Source	Symbol	Interrupt Enable Bit	Priority	Mask	Vector Address
Hardware Reset	RESETB	-	0	Non-Maskable	0000H
External Interrupt 10	INT0	IE.0	1	Maskable	0003H
External Interrupt 11	INT1	IE.1	2	Maskable	000BH
USI1 I2C Interrupt	INT2	IE.2	3	Maskable	0013H
USI1 Rx Interrupt	INT3	IE.3	4	Maskable	001BH
USI1 Tx Interrupt	INT4	IE.4	5	Maskable	0023H
External Interrupt 0 - 7	INT5	IE.5	6	Maskable	002BH
External Interrupt 8	INT6	IE1.0	7	Maskable	0033H
-	INT7	IE1.1	8	Maskable	003BH
USI0 I2C Interrupt	INT8	IE1.2	9	Maskable	0043H
USI0 Rx Interrupt	INT9	IE1.3	10	Maskable	004BH
USI0 Tx Interrupt	INT10	IE1.4	11	Maskable	0053H
External Interrupt 12	INT11	IE1.5	12	Maskable	005BH
T0 Overflow Interrupt	INT12	IE2.0	13	Maskable	0063H
T0 Match Interrupt	INT13	IE2.1	14	Maskable	006BH
T1 Match Interrupt	INT14	IE2.2	15	Maskable	0073H
T2 Match Interrupt	INT15	IE2.3	16	Maskable	007BH
T3 Match Interrupt	INT16	IE2.4	17	Maskable	0083H
T4 Interrupt	INT17	IE2.5	18	Maskable	008BH
ADC Interrupt	INT18	IE3.0	19	Maskable	0093H
SPI 2 Interrupt	INT19	IE3.1	20	Maskable	009BH
WT Interrupt	INT20	IE3.2	21	Maskable	00A3H
WDT Interrupt	INT21	IE3.3	22	Maskable	00ABH
BIT Interrupt	INT22	IE3.4	23	Maskable	00B3H
-	INT23	IE3.5	24	Maskable	00BBH

**Table 10.2** Interrupt Vector Address Table

For executing maskable interrupt, specific interrupt source must set '1' by writing a '1' to associated bit in the IEx and EA bit must set '1'. If interrupt request is received, specific interrupt request flag set '1'. And it remains '1' until CPU accepts interrupt. After then, interrupt request flag will be cleared automatically.

### 10.5 Interrupt Sequence

An interrupt request is held until the interrupt is accepted or the interrupt latch is cleared to '0' by a reset or an instruction. Interrupt acceptance always generates at last cycle of the instruction. So instead of fetching the current instruction, CPU executes internally LCALL instruction and saves the PC at stack. For the interrupt service routine, the interrupt controller gives the address of LJMP instruction to CPU. Since the end of the execution of current instruction, it needs 3~9 machine cycles to go to the interrupt service routine. The interrupt service task is terminated by the interrupt return instruction [RETI]. The following process is the flow of whole interrupt service routine.

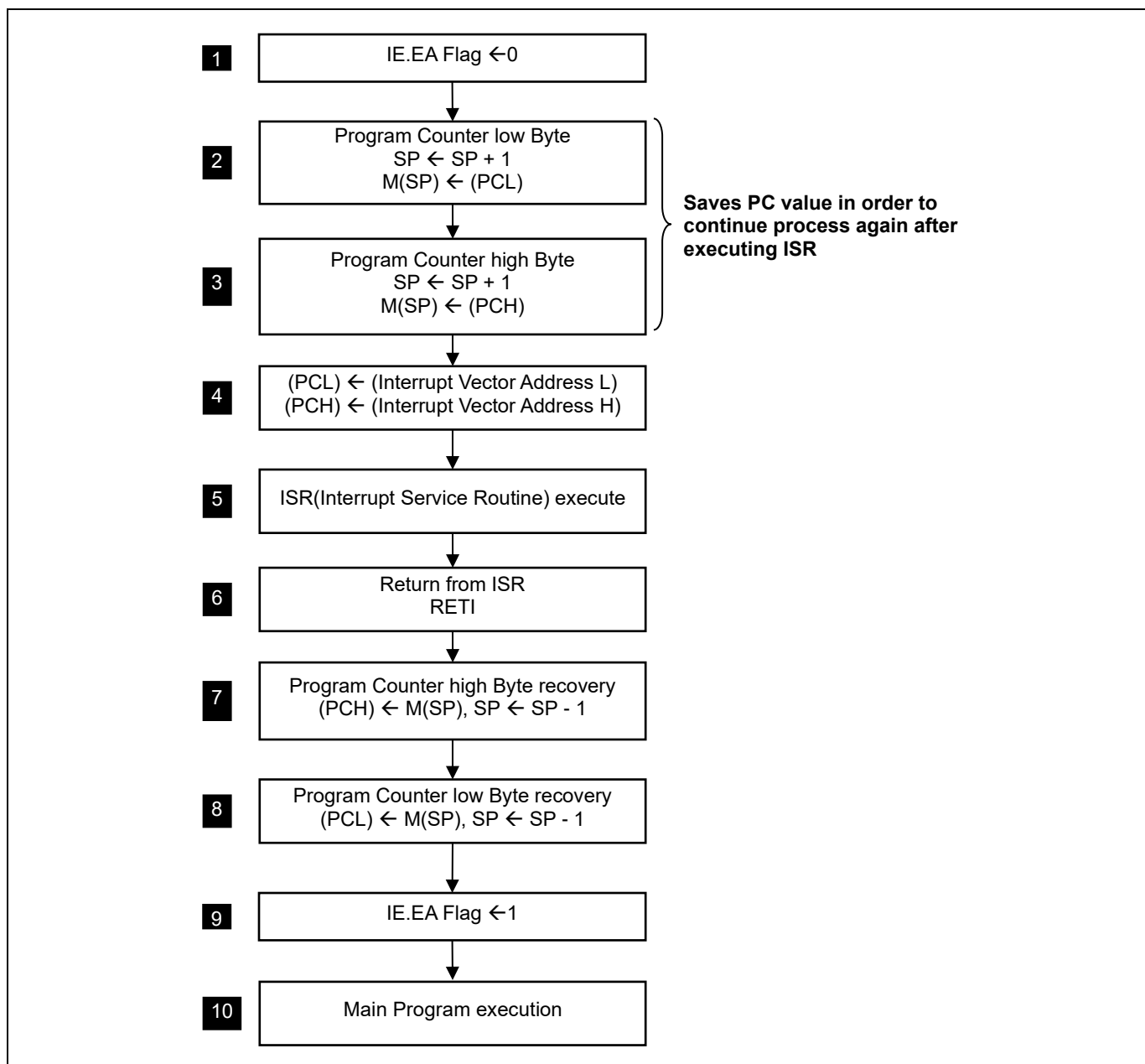


Figure 10.3 Interrupt Sequence Flow



### 10.6 Effective Timing after Controlling Interrupt Bit

Case a) Control Interrupt Enable Register (IE, IE1, IE2, IE3)

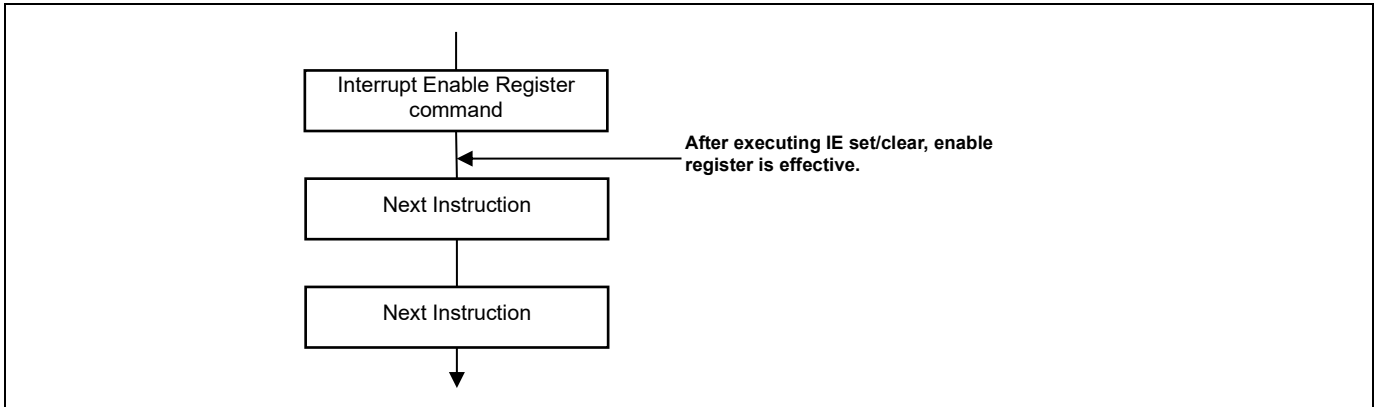


Figure 10.4 Effective Timing of Interrupt Enable Register

Case b) Interrupt flag Register

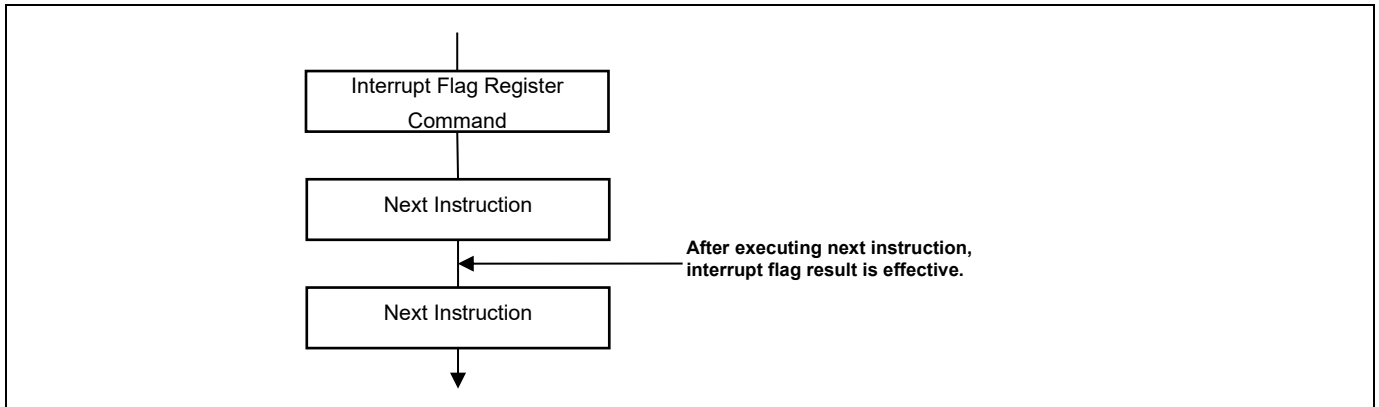
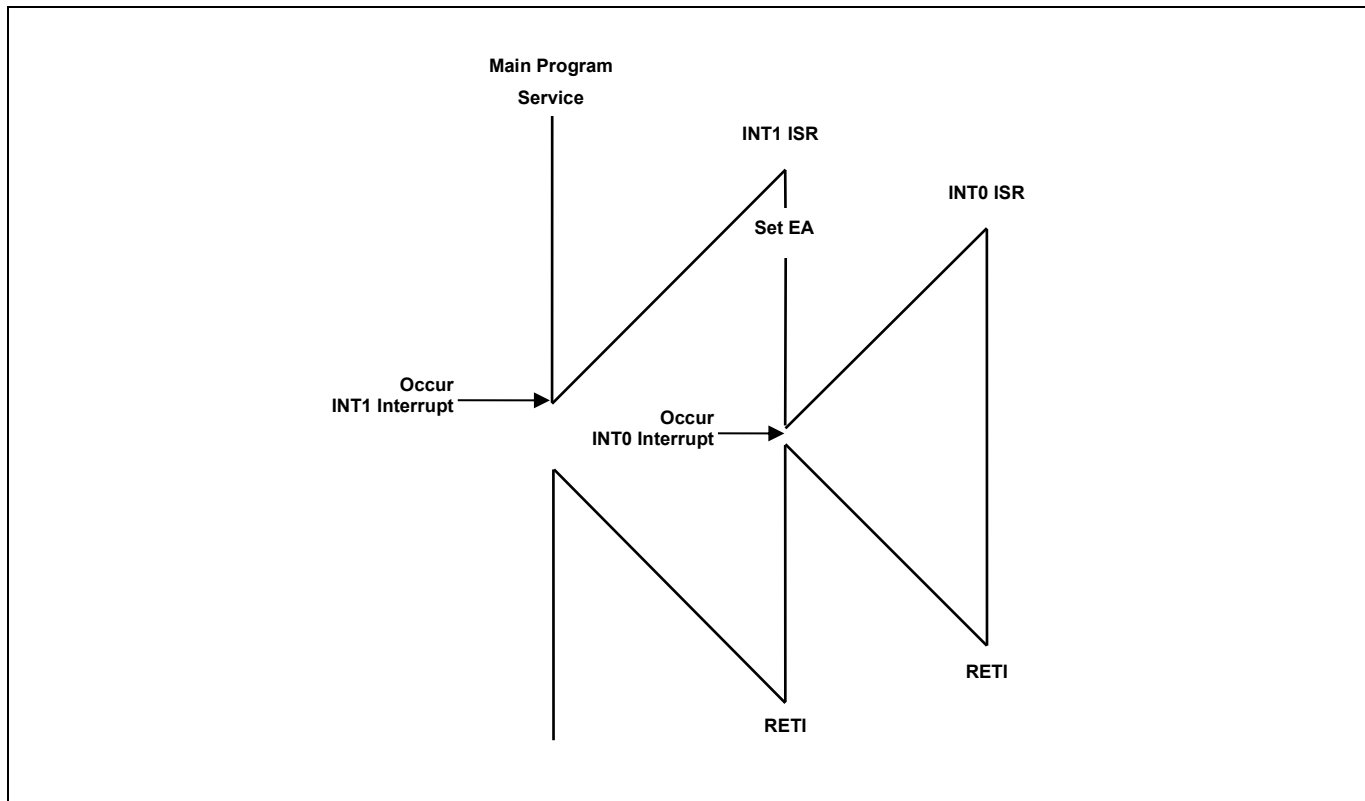


Figure 10.5 Effective Timing of Interrupt Flag Register

### 10.7 Multi Interrupt

If two different priority level requests are received simultaneously, the higher priority level request is serviced. If requests of the interrupt are received at the same time, an interrupt polling sequence determines by hardware which request is serviced. However, multiple processing is possible through software for special features.



**Figure 10.6** Effective Timing of Multi-Interrupt

Figure 10.6 shows an example of multi-interrupt processing. While INT1 is served, INT0 which has higher priority than INT1 is occurred. Then INT0 is served immediately and then the remain part of INT1 service routine is executed. If the priority level of INT0 is same or lower than INT1, INT0 will be served after the INT1 service has completed.

An interrupt service routine may be only interrupted by an interrupt of higher priority and, if two interrupts of different priority occur at the same time, the higher level interrupt will be served first. An interrupt cannot be interrupted by another interrupt of the same or a lower priority level. If two interrupts of the same priority level occur simultaneously, the service order for those interrupts is determined by the scan order.

### 10.8 Interrupt Enable Accept Timing

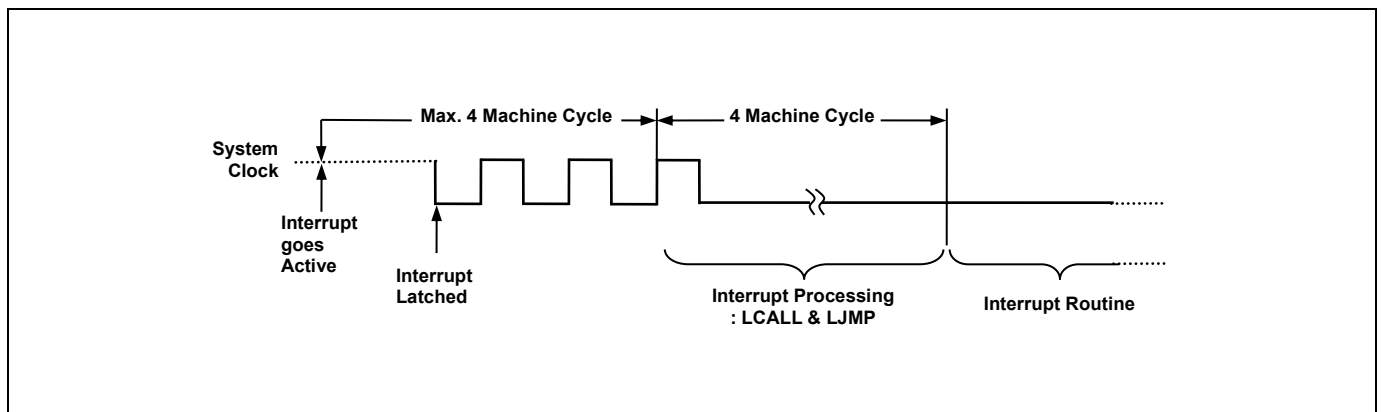


Figure 10.7 Interrupt Response Timing Diagram

### 10.9 Interrupt Service Routine Address

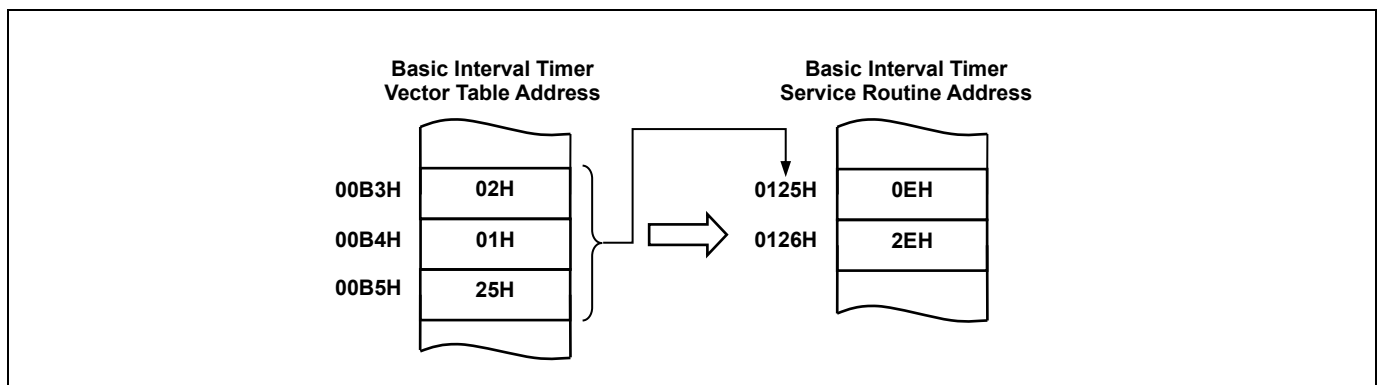


Figure 10.8 Correspondence between Vector Table Address and the Entry Address of ISR

### 10.10 Saving/Restore General-Purpose Registers

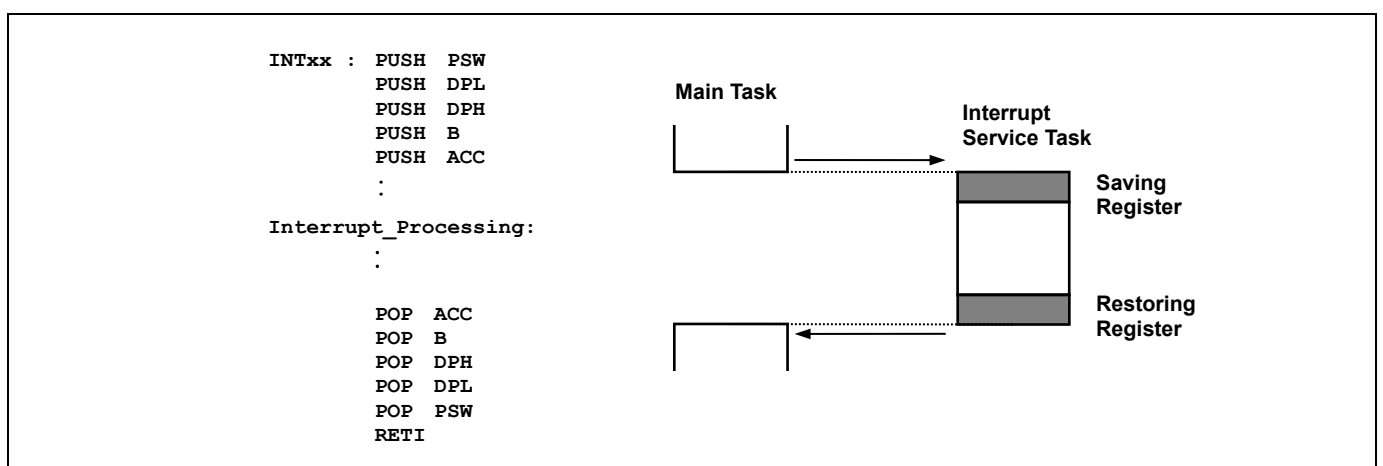
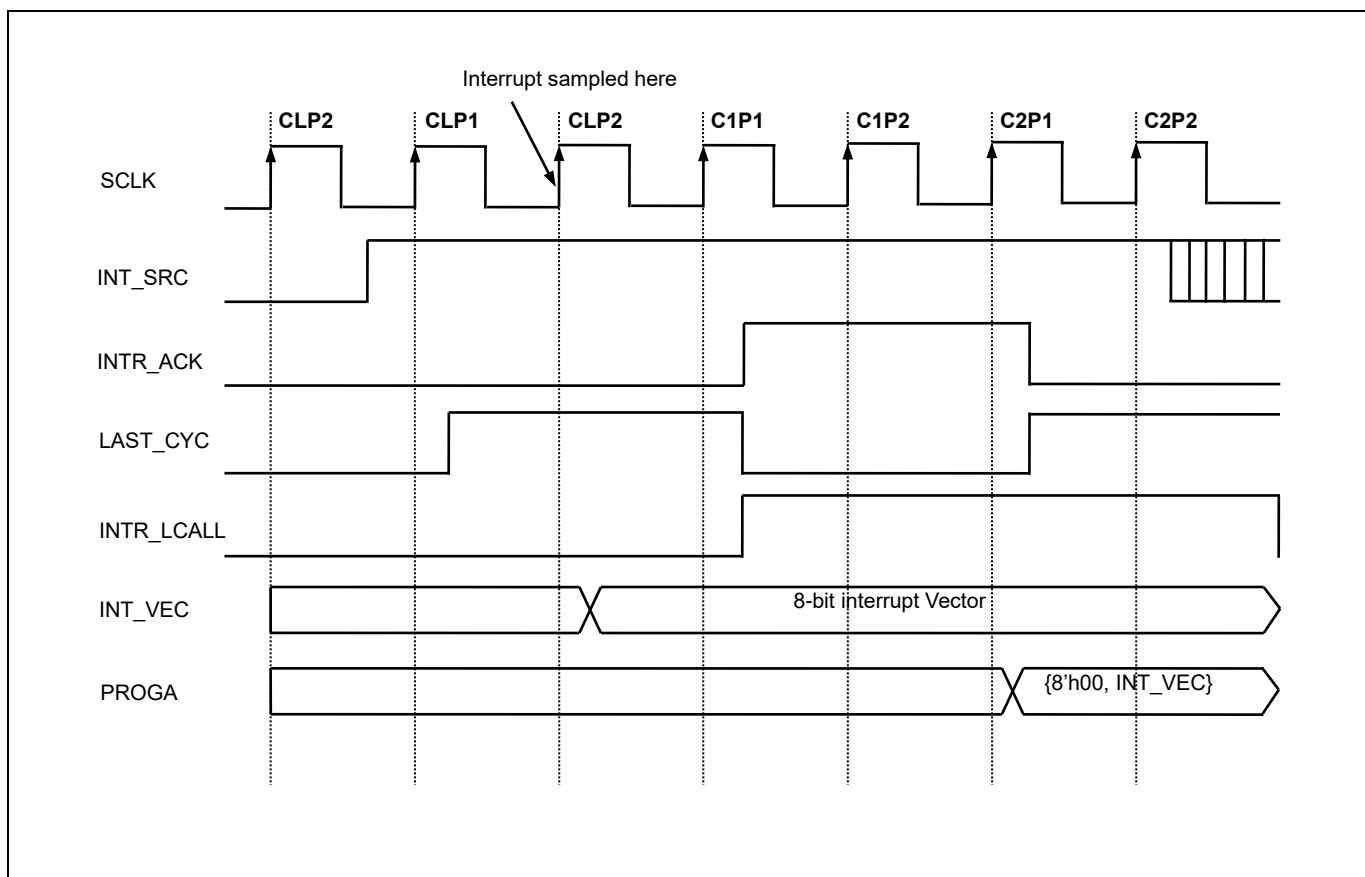


Figure 10.9 Saving/Restore Process Diagram and Sample Source

## 10.11 Interrupt Timing



**Figure 10.10** Timing Chart of Interrupt Acceptance and Interrupt Return Instruction

Interrupt sources are sampled at the last cycle of a command. If an interrupt source is detected the lower 8-bit of interrupt vector (INT\_VEC) is decided. M8051W core makes interrupt acknowledge at the first cycle of a command and executes long call to jump to interrupt service routine.

**NOTE)**

1. command cycle CLPx: L=Last cycle, 1=1<sup>st</sup> cycle or 1<sup>st</sup> phase, 2=2<sup>nd</sup> cycle or 2<sup>nd</sup> phase

## 10.12 Interrupt Register Overview

### 10.12.1 Interrupt Enable Register (IE, IE1, IE2, IE3)

Interrupt enable register consists of global interrupt control bit (EA) and peripheral interrupt control bits. Total 24 peripherals are able to control interrupt.

### 10.12.2 Interrupt Priority Register (IP, IP1)

The 24 interrupts are divided into 6 groups which have each 4 interrupt sources. A group can be assigned 4 levels interrupt priority using interrupt priority register. Level 3 is the highest priority, while level 0 is the lowest priority. After a reset IP and IP1 are cleared to '00H'. If interrupts have the same priority level, lower number interrupt is served first.

### 10.12.3 External Interrupt Flag Register (EIFLAG0, EIFLAG1)

The external interrupt flag 0 register (EIFLAG0) and external interrupt flag 1 register (EIFLAG1) are set to '1' when the external interrupt generating condition is satisfied. The flag is cleared when the interrupt service routine is executed. Alternatively, the flag can be cleared by writing '0' to it.

### 10.12.4 External Interrupt Polarity Register (EIPOL0L, EIPOL0H, EIPOL1)

The external interrupt polarity 0 high/low register (EIPOL0H/L) and external interrupt polarity 1 register (EIPOL1) determines which type of rising/falling/both edge interrupt. Initially, default value is no interrupt at any edge.

### 10.12.5 Register Map

Name	Address	Direction	Default	Description
IE	A8H	R/W	00H	Interrupt Enable Register
IE1	A9H	R/W	00H	Interrupt Enable Register 1
IE2	AAH	R/W	00H	Interrupt Enable Register 2
IE3	ABH	R/W	00H	Interrupt Enable Register 3
IP	B8H	R/W	00H	Interrupt Priority Register
IP1	F8H	R/W	00H	Interrupt Priority Register 1
EIFLAG0	C0H	R/W	00H	External Interrupt Flag 0 Register
EIPOL0L	A4H	R/W	00H	External Interrupt Polarity 0 Low Register
EIPOL0H	A5H	R/W	00H	External Interrupt Polarity 0 High Register
EIFLAG1	A6H	R/W	00H	External Interrupt Flag 1 Register
EIPOL1	A7H	R/W	00H	External Interrupt Polarity 1 Register

**Table 10.3** Interrupt Register Map

### 10.12.6 Interrupt Register Description

The interrupt register is used for controlling interrupt functions. Also it has external interrupt control registers. The interrupt register consists of interrupt enable register (IE), interrupt enable register 1 (IE1), interrupt enable register 2 (IE2) and interrupt enable register 3 (IE3). For external interrupt, it consists of external interrupt flag 0 register (EIFLAG0), external interrupt polarity 0 high/low register (EIPOL0H/L), external interrupt flag 1 register (EIFLAG1) and external interrupt polarity 1 register (EIPOL1).

10.12.7 Register Description for Interrupt

IE (Interrupt Enable Register): A8H

7	6	5	4	3	2	1	0
EA	–	INT5E	INT4E	INT3E	INT2E	INT1E	INT0E
RW	–	RW	RW	RW	RW	RW	RW

Initial value: 00H

- EA** Enable or Disable All Interrupt bits
  - 0 All Interrupt disable
  - 1 All Interrupt enable
- INT5E** Enable or Disable External Interrupt 0 ~ 7 (EINT0 ~ EINT7)
  - 0 Disable
  - 1 Enable
- INT4E** Enable or Disable USI1 Tx Interrupt
  - 0 Disable
  - 1 Enable
- INT3E** Enable or Disable USI1 Rx Interrupt
  - 0 Disable
  - 1 Enable
- INT2E** Enable or Disable USI1 I2C Interrupt
  - 0 Disable
  - 1 Enable
- INT1E** Enable or Disable External Interrupt 11(EINT11)
  - 0 Disable
  - 1 Enable
- INT0E** Enable or Disable External Interrupt 10 (EINT10)
  - 0 Disable
  - 1 Enable

**IE1 (Interrupt Enable Register 1): A9H**

7	6	5	4	3	2	1	0
–	–	INT11E	INT10E	INT9E	INT8E	–	INT6E
–	–	RW	RW	RW	RW	–	RW

Initial value: 00H

<b>INT11E</b>	Enable or Disable External Interrupt 12 (EINT12)
0	Disable
1	Enable
<b>INT10E</b>	Enable or Disable USI0 Tx Interrupt
0	Disable
1	Enable
<b>INT9E</b>	Enable or Disable USI0 Rx Interrupt
0	Disable
1	Enable
<b>INT8E</b>	Enable or Disable USI0 I2C Interrupt
0	Disable
1	Enable
<b>INT6E</b>	Enable or Disable External Interrupt 8 (EINT8)
0	Disable
1	Enable

**IE2 (Interrupt Enable Register 2): AAH**

7	6	5	4	3	2	1	0
—	—	INT17E	INT16E	INT15E	INT14E	INT13E	INT12E
—	—	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

- INT17E** Enable or Disable Timer 4 Interrupt  
0 Disable  
1 Enable
- INT16E** Enable or Disable Timer 3 Match Interrupt  
0 Disable  
1 Enable
- INT15E** Enable or Disable Timer 2 Match Interrupt  
0 Disable  
1 Enable
- INT14E** Enable or Disable Timer 1 Match Interrupt  
0 Disable  
1 Enable
- INT13E** Enable or Disable Timer 0 Match Interrupt  
0 Disable  
1 Enable
- INT12E** Enable or Disable Timer 0 Overflow Interrupt  
0 Disable  
1 Enable

**IE3 (Interrupt Enable Register 3): ABH**

7	6	5	4	3	2	1	0
—	—	—	INT22E	INT21E	INT20E	INT19E	INT18E
—	—	—	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

- INT22E** Enable or Disable BIT Interrupt  
0 Disable  
1 Enable
- INT21E** Enable or Disable WDT Interrupt  
0 Disable  
1 Enable
- INT20E** Enable or Disable WT Interrupt  
0 Disable  
1 Enable
- INT19E** Enable or Disable SPI 2 Interrupt  
0 Disable  
1 Enable
- INT18E** Enable or Disable ADC Interrupt  
0 Disable  
1 Enable



**IP (Interrupt Priority Register): B8H**

7	6	5	4	3	2	1	0
–	–	IP5	IP4	IP3	IP2	IP1	IP0
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

**IP1 (Interrupt Priority Register 1): F8H**

7	6	5	4	3	2	1	0
–	–	IP15	IP14	IP13	IP12	IP11	IP10
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

<b>IP[5:0], IP1[5:0]</b>	Select Interrupt Group Priority		
	IP1x	IPx	Description
	0	0	level 0 (lowest)
	0	1	level 1
	1	0	level 2
	1	1	level 3 (highest)

**EIFLAG0 (External Interrupt Flag 0 Register): C0H**

7	6	5	4	3	2	1	0
FLAG7	FLAG6	FLAG5	FLAG4	FLAG3	FLAG2	FLAG1	FLAG0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**EIFLAG0[7:0]** When an External Interrupt 0-7 is occurred, the flag becomes '1'. The flag is cleared only by writing '0' to the bit. So, the flag should be cleared by software.

- 0 External Interrupt0 ~ 7 not occurred
- 1 External Interrupt0 ~ 7 occurred

**EIPOL0H (External Interrupt Polarity 0 High Register): A5H**

7	6	5	4	3	2	1	0
POL7		POL6		POL5		POL4	
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**EIPOL0H[7:0]** External interrupt (EINT7, EINT6, EINT5, EINT4) polarity selection

- |           |  |
|-----------|--|
| POLn[1:0] | Description                                  |
| 0 0       | No interrupt at any edge                     |
| 0 1       | Interrupt on rising edge                     |
| 1 0       | Interrupt on falling edge                    |
| 1 1       | Interrupt on both of rising and falling edge |

Where n =4, 5, 6 and 7

**EIPOL0L (External Interrupt Polarity 0 Low Register): A4H**

7	6	5	4	3	2	1	0
POL3		POL2		POL1		POL0	
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**EIPOL0L[7:0]** External interrupt (EINT0, EINT1, EINT2, EINT3) polarity selection

- |           |  |
|-----------|--|
| POLn[1:0] | Description                                  |
| 0 0       | No interrupt at any edge                     |
| 0 1       | Interrupt on rising edge                     |
| 1 0       | Interrupt on falling edge                    |
| 1 1       | Interrupt on both of rising and falling edge |

Where n =0, 1, 2 and 3

**EIFLAG1 (External Interrupt Flag 1 Register): A6H**

7	6	5	4	3	2	1	0
TOOVIFR	T0IFR	T3IFR	–	FLAG12	FLAG11	FLAG10	FLAG8
RW	RW	RW	–	RW	RW	RW	RW

Initial value: 00H

- TOOVIFR** When T0 overflow interrupt occurs, this bit becomes '1'. For clearing bit, write '0' to this bit or automatically clear by INT\_ACK signal. Writing "1" has no effect.
- 0 T0 overflow Interrupt no generation  
1 T0 overflow Interrupt generation
- T0IFR** When T0 interrupt occurs, this bit becomes '1'. For clearing bit, write '0' to this bit or automatically clear by INT\_ACK signal. Writing "1" has no effect.
- 0 T0 Interrupt no generation  
1 T0 Interrupt generation
- T3IFR** When T3 interrupt occurs, this bit becomes '1'. For clearing bit, write '0' to this bit or automatically clear by INT\_ACK signal. Writing "1" has no effect.
- 0 T3 Interrupt no generation  
1 T3 Interrupt generation
- EIFLAG1[3:0]** When an External Interrupt (EINT8, EINT10-EINT12) is occurred, the flag becomes '1'. The flag is cleared by writing '0' to the bit or automatically cleared by INT\_ACK signal. Writing "1" has no effect.
- 0 External Interrupt not occurred  
1 External Interrupt occurred

**EIPOL1 (External Interrupt Polarity 1 Register): A7H**

7	6	5	4	3	2	1	0
POL12		POL11		POL10		POL8	
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

- EIPOL1[7:0]** External interrupt (EINT8,EINT10,EINT11,EINT12) polarity selection
- | POLn[1:0] | Description                                  |
|-----------|--|
| 0 0       | No interrupt at any edge                     |
| 0 1       | Interrupt on rising edge                     |
| 1 0       | Interrupt on falling edge                    |
| 1 1       | Interrupt on both of rising and falling edge |
- Where n =8, 10, 11 and 12

## 11 Peripheral Hardware

### 11.1 Clock Generator

#### 11.1.1 Overview

As shown in Figure 11.1, the clock generator produces the basic clock pulses which provide the system clock to be supplied to the CPU and the peripheral hardware. It contains main/sub-frequency clock oscillator. The main/sub clock operation can be easily obtained by attaching a crystal between the XIN/SXIN and XOUT/SXOUT pin, respectively. The main/sub clock can be also obtained from the external oscillator. In this case, it is necessary to put the external clock signal into the XIN/SXIN pin and open the XOUT/SXOUT pin. The default system clock is 1MHz INT-RC Oscillator and the default division rate is eight. In order to stabilize system internally, it is used 1MHz INT-RC oscillator on POR.

- Calibrated Internal RC Oscillator (16MHz )
  - INT-RC OSC/1 (16MHz)
  - INT-RC OSC/2 (8MHz)
  - INT-RC OSC/4 (4MHz)
  - INT-RC OSC/8 (2MHz)
  - INT-RC OSC/16 (1MHz, Default system clock)
  - INT-RC OSC/32 (0.5MHz)
- Main Crystal Oscillator (0.4~8.5MHz)
- Sub Crystal Oscillator (32.768kHz)
- Internal WDTRC Oscillator (5kHz)

11.1.2 Block Diagram

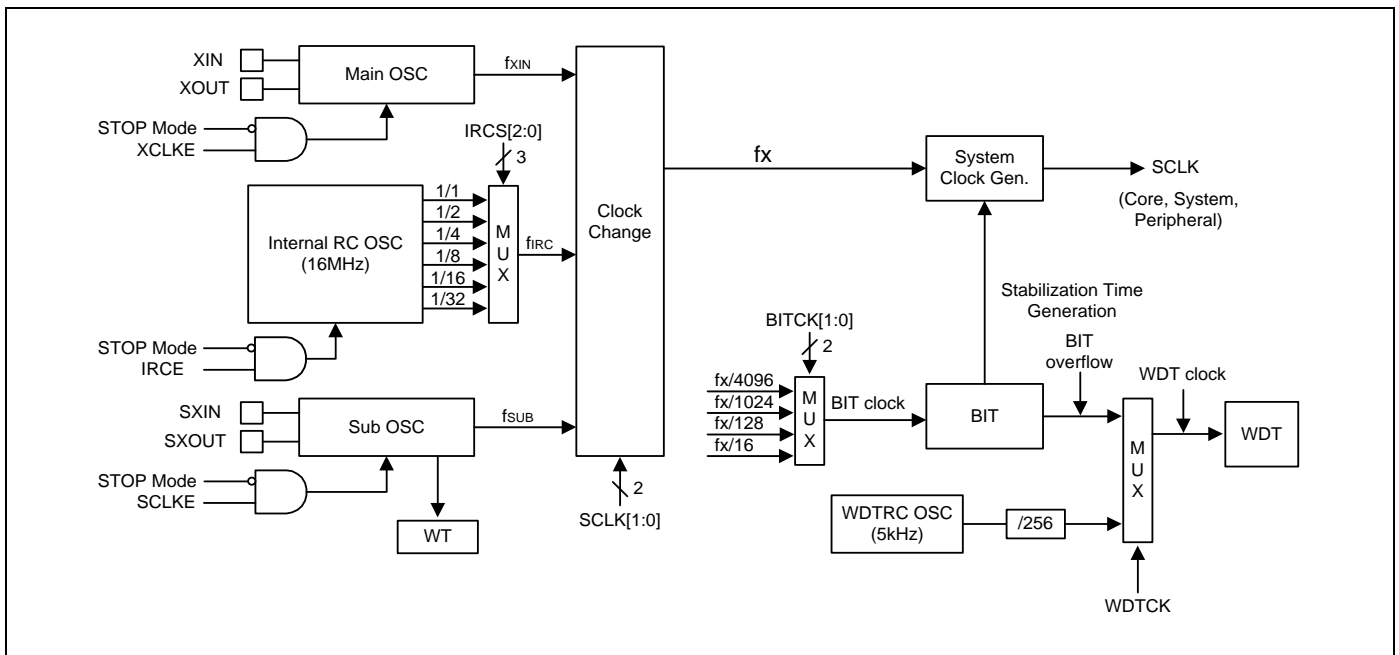


Figure 11.1 Clock Generator Block Diagram

### 11.1.3 Register Map

Name	Address	Direction	Default	Description
SCCR	8AH	R/W	00H	System and Clock Control Register
OSCCR	C8H	R/W	20H	Oscillator Control Register
XTFLSR	1038H	R/W	00H	X-tal Filter Selection Register

Table 11.1 Clock Generator Register Map

### 11.1.4 Clock Generator Register Description

The clock generator register uses clock control for system operation. The clock generation consists of System and clock control register and oscillator control register.

### 11.1.5 Register Description for Clock Generator

#### SCCR (System and Clock Control Register): 8AH

7	6	5	4	3	2	1	0
–	–	–	–	–	–	SCLK1	SCLK0
–	–	–	–	–	–	RW	RW

Initial value: 00H

<b>SCLK [1:0]</b>	System Clock Selection Bit	
	SCLK1	SCLK0
	Description	
	0	0
	INT RC OSC ( $f_{IRC}$ ) for system clock	
	0	1
	External Main OSC ( $f_{XIN}$ ) for system clock	
	1	0
	External Sub OSC ( $f_{SUB}$ ) for system clock	
	1	1
	Not used	

## OSCCR (Oscillator Control Register): C8H

7	6	5	4	3	2	1	0
–	–	IRCS2	IRCS1	IRCS0	IRCE	XCLKE	SCLKE
–	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 08H

<b>IRCS[2:0]</b>	Internal RC Oscillator Post-divider Selection			
	IRCS2	IRCS1	IRCS0	Description
	0	0	0	INT-RC/32 (0.5MHz)
	0	0	1	INT-RC/16 (1MHz)
	0	1	0	INT-RC/8 (2MHz)
	0	1	1	INT-RC/4 (4MHz)
	1	0	0	INT-RC/2 (8MHz)
	1	0	1	INT-RC/1 (16MHz)
	Other values			Not used
<b>IRCE</b>	Control the Operation of the Internal RC Oscillator			
	0	Enable operation of INT-RC OSC		
	1	Disable operation of INT-RC OSC		
<b>XCLKE</b>	Control the Operation of the External Main Oscillator			
	0	Disable operation of X-TAL		
	1	Enable operation of X-TAL		
<b>SCLKE</b>	Control the Operation of the External Sub Oscillator			
	0	Disable operation of SX-TAL		
	1	Enable operation of SX-TAL		

**NOTE)**

1. IRC 8MHz or under frequencies are recommended in a noisy environment

**XTFLSR (X-tal Filter Selection Register): 1038H (ESFR)**

7	6	5	4	3	2	1	0
WTP4	WTP3	WTP2	WTP1	WTP0	–	–	XRNS
W	W	W	W	W	–	–	R/W

Initial value: 00H

- WTP[4:0]** Write Identification bits. These bits are automatically cleared to “00000b” immediately after XTFLSR write. 0x00 on read.  
 10101b Write 0x15 to these bits with valid XRNS[2:0]  
 Other values Write is ignored.
- XRNS** External Main Oscillator Range selection. This bit is effective only when the fXIN is selected for system clock.  
 XRNS Description  
 0 4.2MHz < x-tal ≤ 8.5MHz  
 1 x-tal ≤ 4.2MHz

**NOTE)**

1. The External Main Oscillator Range(XRNS) should be changed while the system clock is selected as IRC.



## 11.2 Basic Interval Timer

### 11.2.1 Overview

The MC96F6432A has one 8-bit basic interval timer that is free-run and can't stop. Block diagram is shown in Figure 11.2. In addition, the basic interval timer generates the time base for watchdog timer counting. It also provides a basic interval timer interrupt (BITIFR).

The MC96F6432A has these basic interval timer (BIT) features:

- During Power On, BIT gives a stable clock generation time
- On exiting Stop mode, BIT gives a stable clock generation time
- As timer function, timer interrupt occurrence

### 11.2.2 Block Diagram

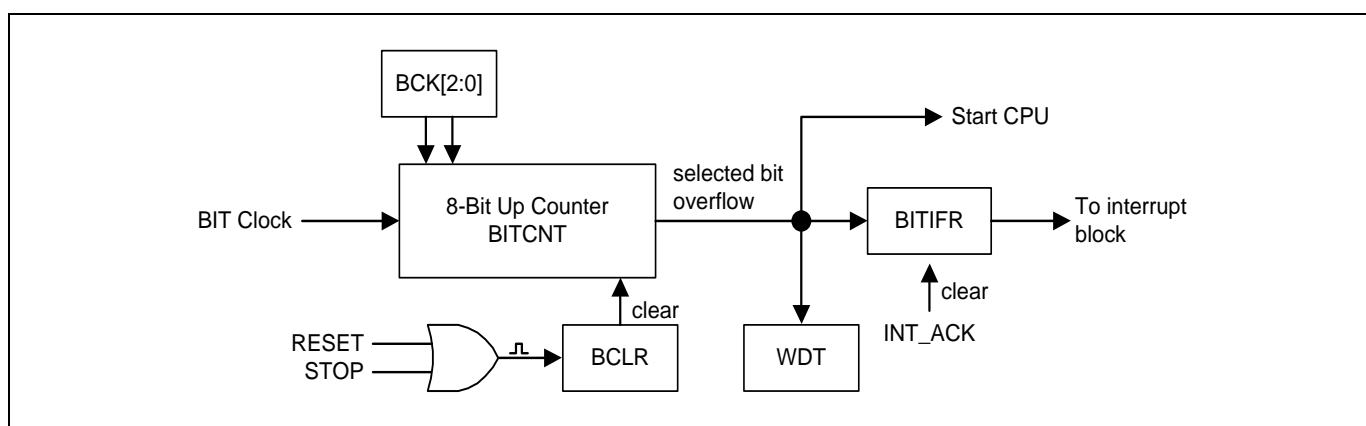


Figure 11.2 Basic Interval Timer Block Diagram

### 11.2.3 Register Map

Name	Address	Direction	Default	Description
BITCNT	8CH	R	00H	Basic Interval Timer Counter Register
BITCR	8BH	R/W	01H	Basic Interval Timer Control Register

Table 11.2 Basic Interval Timer Register Map

### 11.2.4 Basic Interval Timer Register Description

The basic interval timer register consists of basic interval timer counter register (BITCNT) and basic interval timer control register (BITCR). If BCLR bit is set to '1', BITCNT becomes '0' and then counts up. After 1 machine cycle, BCLR bit is cleared to '0' automatically.

### 11.2.5 Register Description for Basic Interval Timer

#### BITCNT (Basic Interval Timer Counter Register): 8CH

7	6	5	4	3	2	1	0
BITCNT7	BITCNT6	BITCNT5	BITCNT4	BITCNT3	BITCNT2	BITCNT1	BITCNT0
R	R	R	R	R	R	R	R

Initial value: 00H

**BITCNT[7:0]** BIT Counter

#### BITCR (Basic Interval Timer Control Register): 8BH

7	6	5	4	3	2	1	0
BITIFR	BITCK1	BITCK0	-	BCLR	BCK2	BCK1	BCK0
RW	RW	RW	-	RW	RW	RW	RW

Initial value: 01H

**BITIFR** When BIT Interrupt occurs, this bit becomes '1'. For clearing bit, write '0' to this bit or auto clear by INT\_ACK signal. Writing "1" has no effect.

- 0 BIT interrupt no generation
- 1 BIT interrupt generation

**BITCK[1:0]** Select BIT clock source

BITCK1	BITCK0	Description
0	0	fx/4096
0	1	fx/1024
1	0	fx/128
1	1	fx/16

**BCLR** If this bit is written to '1', BIT Counter is cleared to '0'

- 0 Free Running
- 1 Clear Counter

**BCK[2:0]** Select BIT overflow period

BCK2	BCK1	BCK0	Description
0	0	0	Bit 0 overflow (BIT Clock * 2)
0	0	1	Bit 1 overflow (BIT Clock * 4) (default)
0	1	0	Bit 2 overflow (BIT Clock * 8)
0	1	1	Bit 3 overflow (BIT Clock * 16)
1	0	0	Bit 4 overflow (BIT Clock * 32)
1	0	1	Bit 5 overflow (BIT Clock * 64)
1	1	0	Bit 6 overflow (BIT Clock * 128)
1	1	1	Bit 7 overflow (BIT Clock * 256)

### 11.3 Watch Dog Timer

#### 11.3.1 Overview

The watchdog timer rapidly detects the CPU malfunction such as endless looping caused by noise or something like that and resumes the CPU to the normal state. The watchdog timer signal for malfunction detection can be used as either a CPU reset or an interrupt request. When the watchdog timer is not being used for malfunction detection, it can be used as a timer to generate an interrupt at fixed intervals. It is possible to use free running 8-bit timer mode (WDTRSON='0') or watch dog timer mode (WDTRSON='1') as setting WDTCR[6] bit. If WDTCR[5] is written to '1', WDT counter value is cleared and counts up. After 1 machine cycle, this bit is cleared to '0' automatically. The watchdog timer consists of 8-bit binary counter and the watchdog timer data register. When the value of 8-bit binary counter is equal to the 8 bits of WDCNT, the interrupt request flag is generated. This can be used as Watchdog timer interrupt or reset of CPU in accordance with the bit WDTRSON.

The input clock source of watch dog timer is the BIT overflow. The interval of watchdog timer interrupt is decided by BIT overflow period and WDTDR set value. The equation can be described as

$$\text{WDT Interrupt Interval} = (\text{BIT Interrupt Interval}) \times (\text{WDTDR Value} + 1)$$

#### 11.3.2 WDT Interrupt Timing Waveform

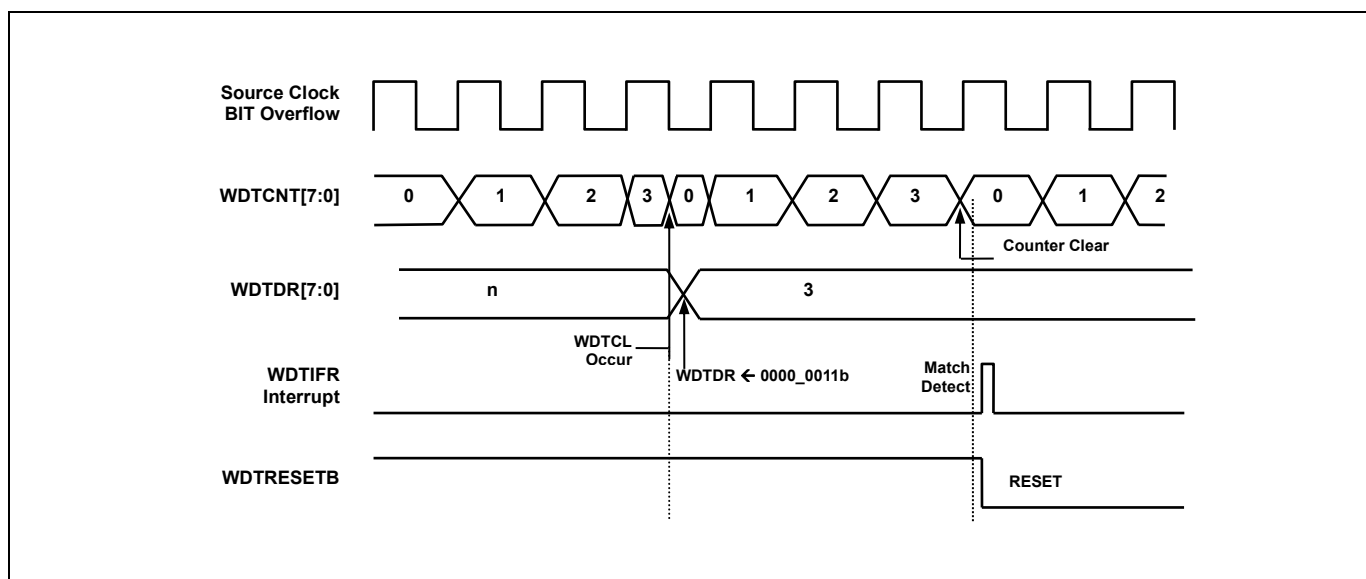


Figure 11.3 Watch Dog Timer Interrupt Timing Waveform

### 11.3.3 Block Diagram

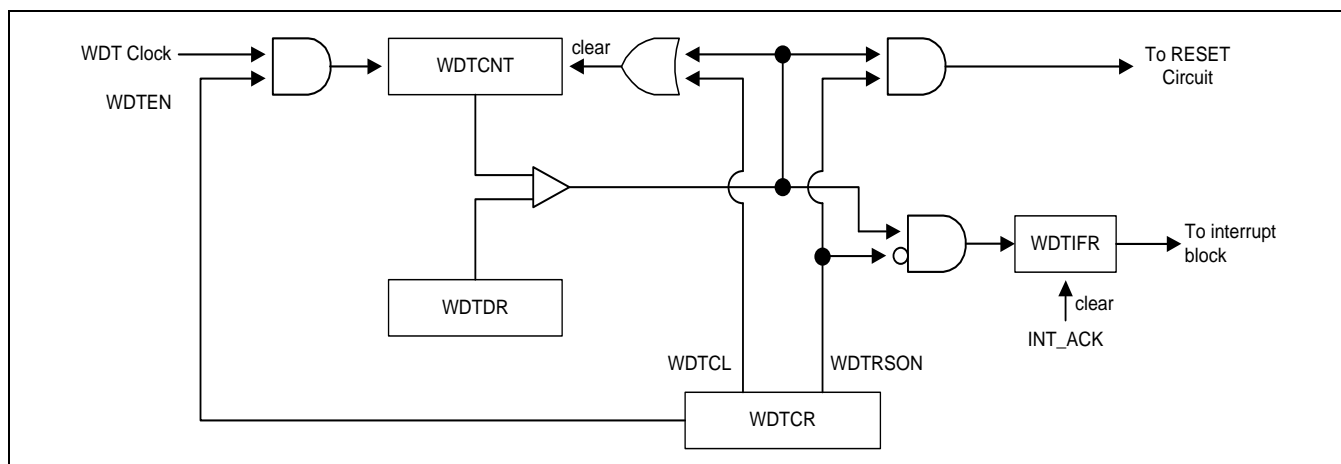


Figure 11.4 Watch Dog Timer Block Diagram

### 11.3.4 Register Map

Name	Address	Direction	Default	Description
WDCNT	8EH	R	00H	Watch Dog Timer Counter Register
WDTDR	8EH	W	FFH	Watch Dog Timer Data Register
WDTCR	8DH	R/W	00H	Watch Dog Timer Control Register

Table 11.3 Watch Dog Timer Register Map

### 11.3.5 Watch Dog Timer Register Description

The watch dog timer register consists of watch dog timer counter register (WDCNT), watch dog timer data register (WDTDR) and watch dog timer control register (WDTCR).

### 11.3.6 Register Description for Watch Dog Timer

#### WDTCNT (Watch Dog Timer Counter Register: Read Case): 8EH

7	6	5	4	3	2	1	0
WDTCNT7	WDTCNT6	WDTCNT5	WDTCNT4	WDTCNT3	WDTCNT2	WDTCNT1	WDTCNT0
R	R	R	R	R	R	R	R

Initial value: 00H

**WDTCNT[7:0]** WDT Counter

#### WDTDR (Watch Dog Timer Data Register: Write Case): 8EH

7	6	5	4	3	2	1	0
WDTDR7	WDTDR6	WDTDR5	WDTDR4	WDTDR3	WDTDR2	WDTDR1	WDTDR0
W	W	W	W	W	W	W	W

Initial value: FFH

**WDTDR[7:0]** Set a period  
 $WDT\ Interrupt\ Interval = (BIT\ Interrupt\ Interval) \times (WDTDR\ Value + 1)$

**NOTE)**

1. Do not write "0" in the WDTDR register.

#### WDTCR (Watch Dog Timer Control Register): 8DH

7	6	5	4	3	2	1	0
WDTEN	WDRSON	WDTCL	-	-	-	WDTCK	WDTIFR
RW	RW	RW	-	-	-	RW	RW

Initial value: 00H

- WDTEN** Control WDT Operation
  - 0 Disable
  - 1 Enable
- WDRSON** Control WDT RESET Operation
  - 0 Free Running 8-bit timer
  - 1 Watch Dog Timer RESET ON
- WDTCL** Clear WDT Counter
  - 0 Free Run
  - 1 Clear WDT Counter (auto clear after 1 Cycle)
- WDTCK** Control WDT Clock Selection Bit
  - 0 BIT overflow for WDT clock (WDTRC disable)
  - 1 WDTRC for WDT clock (WDTRC enable)
- WDTIFR** When WDT Interrupt occurs, this bit becomes '1'. For clearing bit, write '0' to this bit or auto clear by INT\_ACK signal. Writing "1" has no effect.
  - 0 WDT Interrupt no generation
  - 1 WDT Interrupt generation

## 11.4 Watch Timer

### 11.4.1 Overview

The watch timer has the function for RTC (Real Time Clock) operation. It is generally used for RTC design. The internal structure of the watch timer consists of the clock source select circuit, timer counter circuit, output select circuit and watch timer control register. To operate the watch timer, determine the input clock source, output interval and set WTEN as '1' in watch timer control register (WTCR). It is able to execute simultaneously or individually. To stop or reset WT, clear the WTEN bit in WTCR register. Even if CPU is STOP mode, sub clock is able to be alive and so WT can continue the operation. The watch timer counter circuits is composed of 21-bit counter. Low 14-bit is binary counter and high 7-bit is auto reload counter in order to raise resolution. In WTR, it can control WT clear and set Interval value at write time, and it can read 7-bit WT counter value at read time.

The watch timer supplies the clock frequency for the LCD driver ( $f_{LCD}$ ). Therefore, if the watch timer is disabled, the LCD driver controller does not operate.

### 11.4.2 Block Diagram

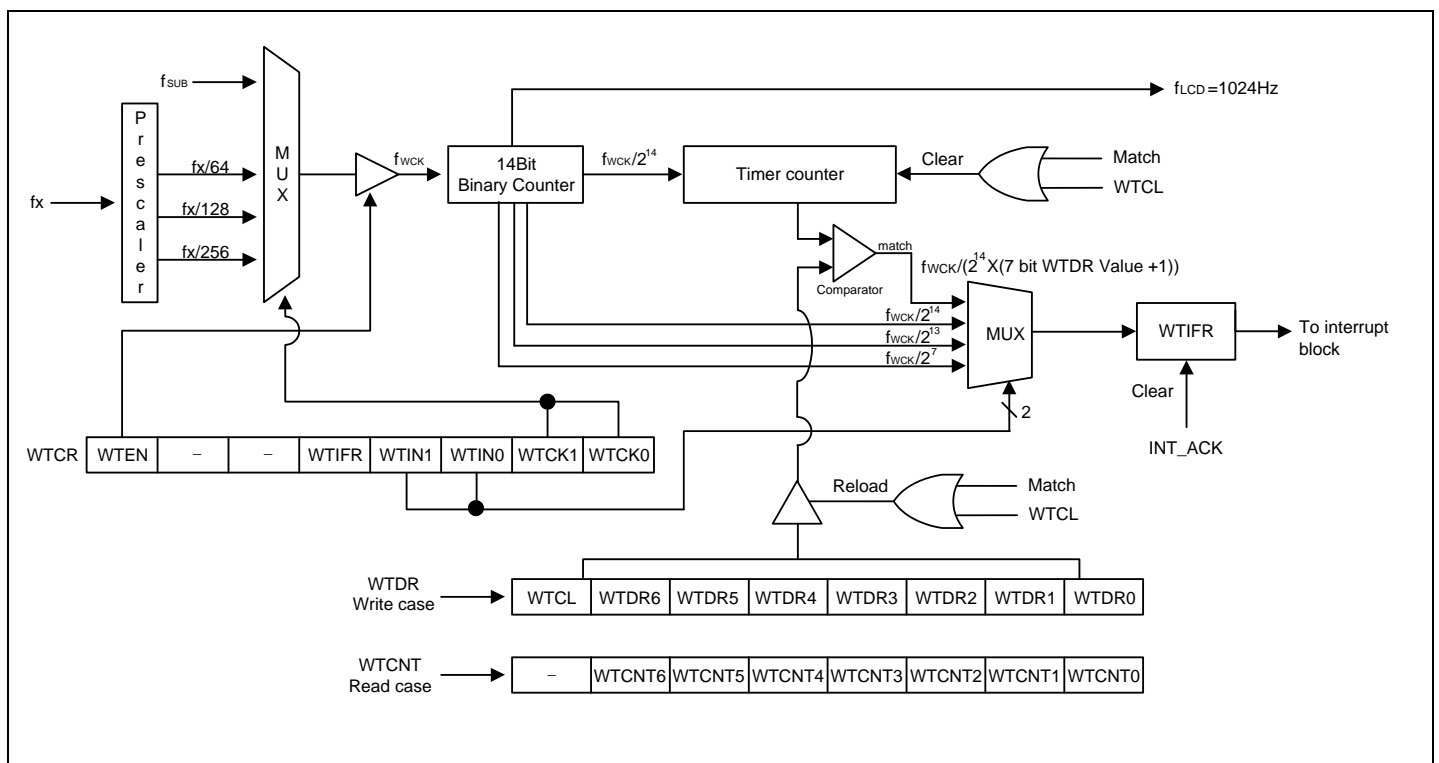


Figure 11.5 Watch Timer Block Diagram

### 11.4.3 Register Map

Name	Address	Direction	Default	Description
WTCNT	89H	R	00H	Watch Timer Counter Register
WTDR	89H	W	7FH	Watch Timer Data Register
WTCR	96H	R/W	00H	Watch Timer Control Register

Table 11.4 Watch Timer Register Map

### 11.4.4 Watch Timer Register Description

The watch timer register consists of watch timer counter register (WTCNT), watch timer data register (WTDR) and watch timer control register (WTCR). As WTCR is 6-bit writable/ readable register, WTCR can control the clock source (WTCK[1:0]), interrupt interval (WTIN[1:0]) and function enable/disable (WTEN). Also there is WT interrupt flag bit (WTIFR).

### 11.4.5 Register Description for Watch Timer

#### WTCNT (Watch Timer Counter Register: Read Case): 89H

7	6	5	4	3	2	1	0
–	WTCNT6	WTCNT5	WTCNT4	WTCNT3	WTCNT2	WTCNT1	WTCNT0
–	R	R	R	R	R	R	R

Initial value: 00H

**WTCNT[6:0]** WT Counter

#### WTDR (Watch Timer Data Register: Write Case): 89H

7	6	5	4	3	2	1	0
WTCL	WTDR6	WTDR5	WTDR4	WTDR3	WTDR2	WTDR1	WTDR0
RW	W	W	W	W	W	W	W

Initial value: 7FH

**WTCL** Clear WT Counter  
 0 Free Run  
 1 Clear WT Counter (auto clear after 1 Cycle)

**WTDR[6:0]** Set WT period  
 WT Interrupt Interval =  $fwck / (2^{14} \times (7\text{bit WTDR Value} + 1))$

**NOTE)**

- Do not write "0" in the WTDR register.

**WTCR (Watch Timer Control Register): 96H**

7	6	5	4	3	2	1	0
WTEN	–	–	WTIFR	WTIN1	WTIN0	WTCK1	WTCK0
RW	–	–	RW	RW	RW	RW	RW

Initial value: 00H

<b>WTEN</b>	Control Watch Timer		
	0	Disable	
	1	Enable	
<b>WTIFR</b>	When WT Interrupt occurs, this bit becomes '1'. For clearing bit, write '0' to this bit or automatically clear by INT_ACK signal. Writing "1" has no effect.		
	0	WT Interrupt no generation	
	1	WT Interrupt generation	
<b>WTIN[1:0]</b>	Determine interrupt interval		
	WTIN1	WTIN0	Description
	0	0	$f_{wck}/2^7$
	0	1	$f_{wck}/2^{13}$
	1	0	$f_{wck}/2^{14}$
	1	1	$f_{wck}/(2^{14} \times (7\text{bit WTDR Value}+1))$
<b>WTCK[1:0]</b>	Determine Source Clock		
	WTCK1	WTCK0	Description
	0	0	$f_{SUB}$
	0	1	$f_x/256$
	1	0	$f_x/128$
	1	1	$f_x/64$

**NOTE)**

1.  $f_x$ – System clock frequency (Where  $f_x= 4.19\text{MHz}$ )
2.  $f_{SUB}$ – Sub clock oscillator frequency (32.768kHz)
3.  $f_{wck}$ – Selected Watch timer clock
4.  $f_{LCD}$  – LCD frequency (Where  $f_x= 4.19\text{MHz}$ ,  $WTCK[1:0]='10'$ ;  $f_{LCD}= 1024\text{Hz}$ )



## 11.5 Timer 0

### 11.5.1 Overview

The 8-bit timer 0 consists of multiplexer, timer 0 counter register, timer 0 data register, timer 0 capture data register and timer 0 control register (T0CNT, T0DR, T0CDR, T0CR).

It has three operating modes:

- 8-bit timer/counter mode
- 8-bit PWM output mode
- 8-bit capture mode

The timer/counter 0 can be clocked by an internal or an external clock source (EC0). The clock source is selected by clock selection logic which is controlled by the clock selection bits (T0CK[2:0]).

- TIMER0 clock source:  $f_x/(2, 4, 8, 32, 128, 512, 2048)$ , EC0

In the capture mode, by EINT10, the data is captured into input capture data register (T0CDR). In timer/counter mode, whenever counter value is equal to T0DR, T0O port toggles. Also the timer 0 outputs PWM waveform through PWM0O port in the PWM mode.

T0EN	T0MS[1:0]	T0CK[2:0]	Timer 0
1	00	XXX	8-bit Timer/Counter Mode
1	01	XXX	8-bit PWM Mode
1	1X	XXX	8-bit Capture Mode

**Table 11.5** Timer 0 Operating Modes

### 11.5.2 8-bit Timer/Counter Mode

The 8-bit timer/counter mode is selected by control register as shown in Figure 11.6.

The 8-bit timer has counter and data register. The counter register is increased by internal or external clock input. The timer 0 can use the input clock with one of 2, 4, 8, 32, 128, 512 and 2048 prescaler division rates (T0CK[2:0]). When the value of T0CNT and T0DR is identical in timer 0, a match signal is generated and the interrupt of Timer 0 occurs. T0CNT value is automatically cleared by match signal. It can be also cleared by software (T0CC).

The external clock (EC0) counts up the timer at the rising edge. If the EC0 is selected as a clock source by T0CK[2:0], EC0 port should be set to the input port by P52IO bit.

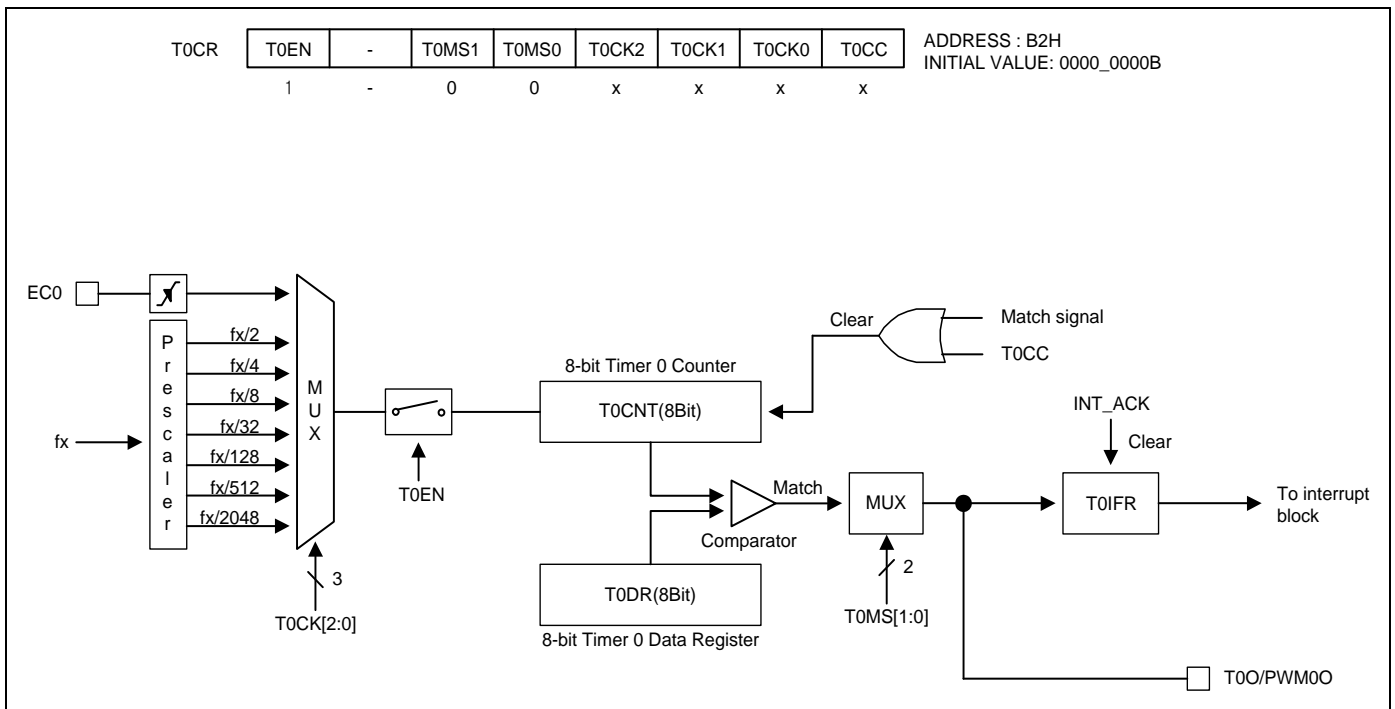


Figure 11.6 8-bit Timer/Counter Mode for Timer 0

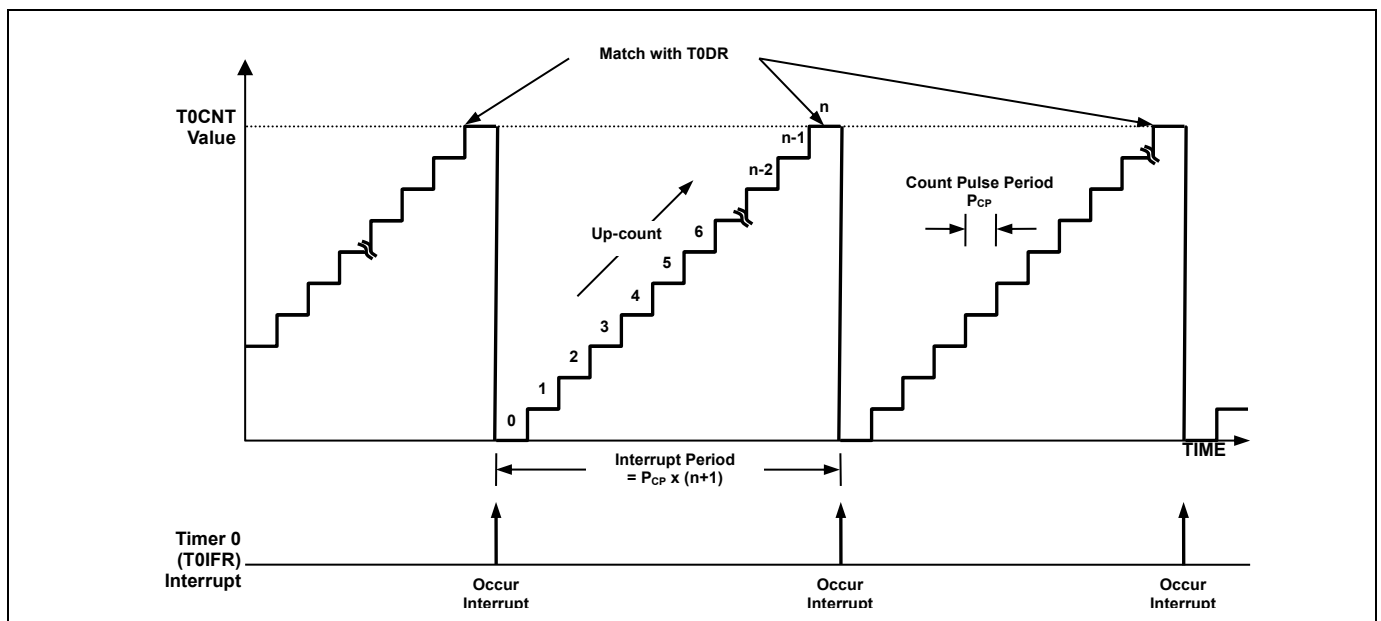


Figure 11.7 8-bit Timer/Counter 0 Example

### 11.5.3 8-bit PWM Mode

The timer 0 has a high speed PWM (Pulse Width Modulation) function. In PWM mode, T0O/PWM00 pin outputs up to 8-bit resolution PWM output. This pin should be configured as a PWM output by setting the T0O/PWM00 function by P5FSR[4:3] bits. In the 8-bit timer/counter mode, a match signal is generated when the counter value is identical to the value of T0DR. When the value of T0CNT and T0DR is identical in timer 0, a match signal is generated and the interrupt of timer 0 occurs. In PWM mode, the match signal does not clear the counter. Instead, it runs continuously, overflowing at “FFH” and then continues incrementing from “00H”. The timer 0 overflow interrupt is generated whenever a counter overflow occurs. T0CNT value is cleared by software (T0CC) bit.

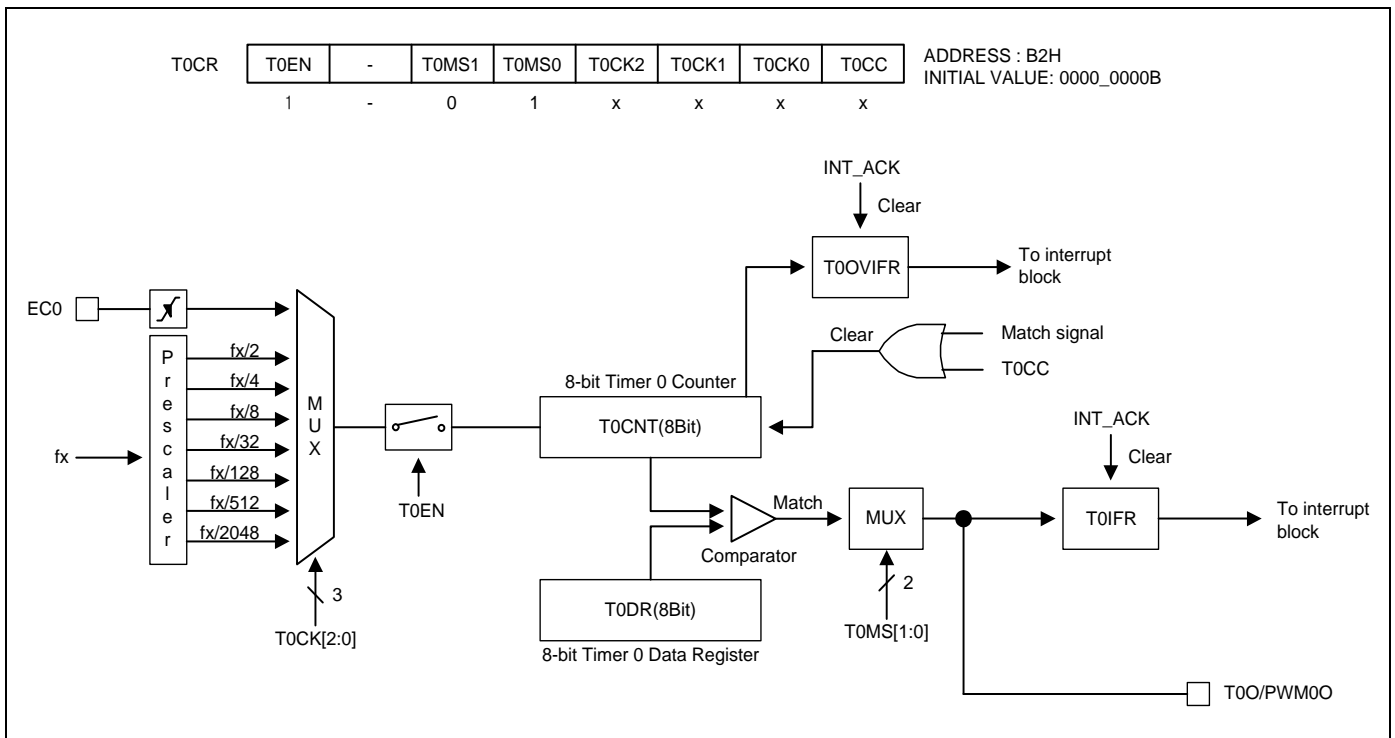


Figure 11.8 8-bit PWM Mode for Timer 0

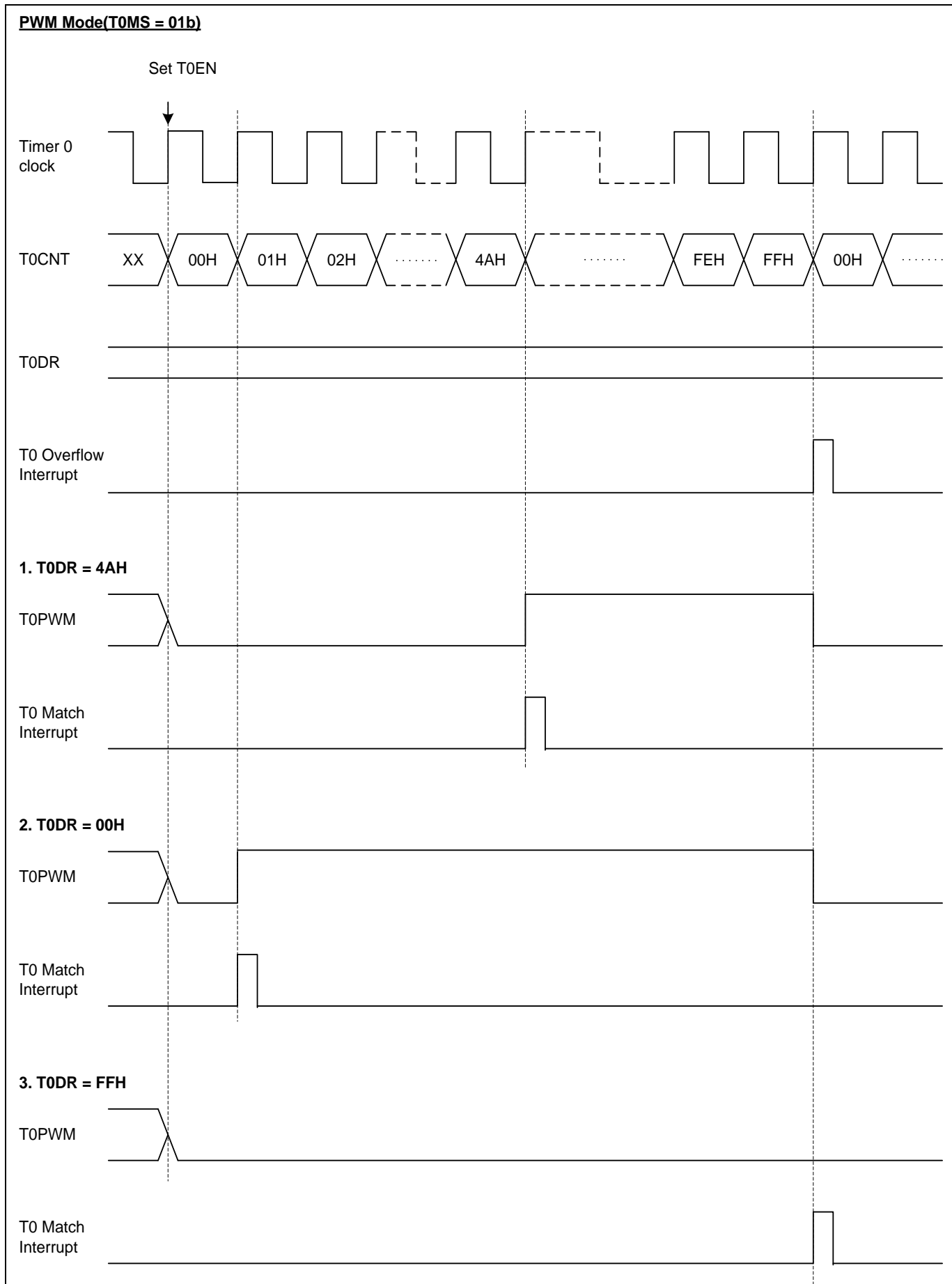


Figure 11.9 PWM Output Waveforms in PWM Mode for Timer 0

### 11.5.4 8-bit Capture Mode

The timer 0 capture mode is evoked by setting T0MS[1:0] as '1x'. The clock source can use the internal/external clock. Basically, it has the same function as the 8-bit timer/counter mode and the interrupt occurs when T0CNT is equal to T0DR. T0CNT value is automatically cleared by match signal and it can be also cleared by software (TOCC).

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

The capture result is loaded into T0CDR. In the timer 0 capture mode, timer 0 output (T0O) waveform is not available. According to EIPOL1 registers setting, the external interrupt EINT10 function is chosen. Of course, the EINT10 pin must be set to an input port.

T0CDR and T0DR are in the same address. In the capture mode, reading operation reads T0CDR, not T0DR and writing operation will update T0DR.

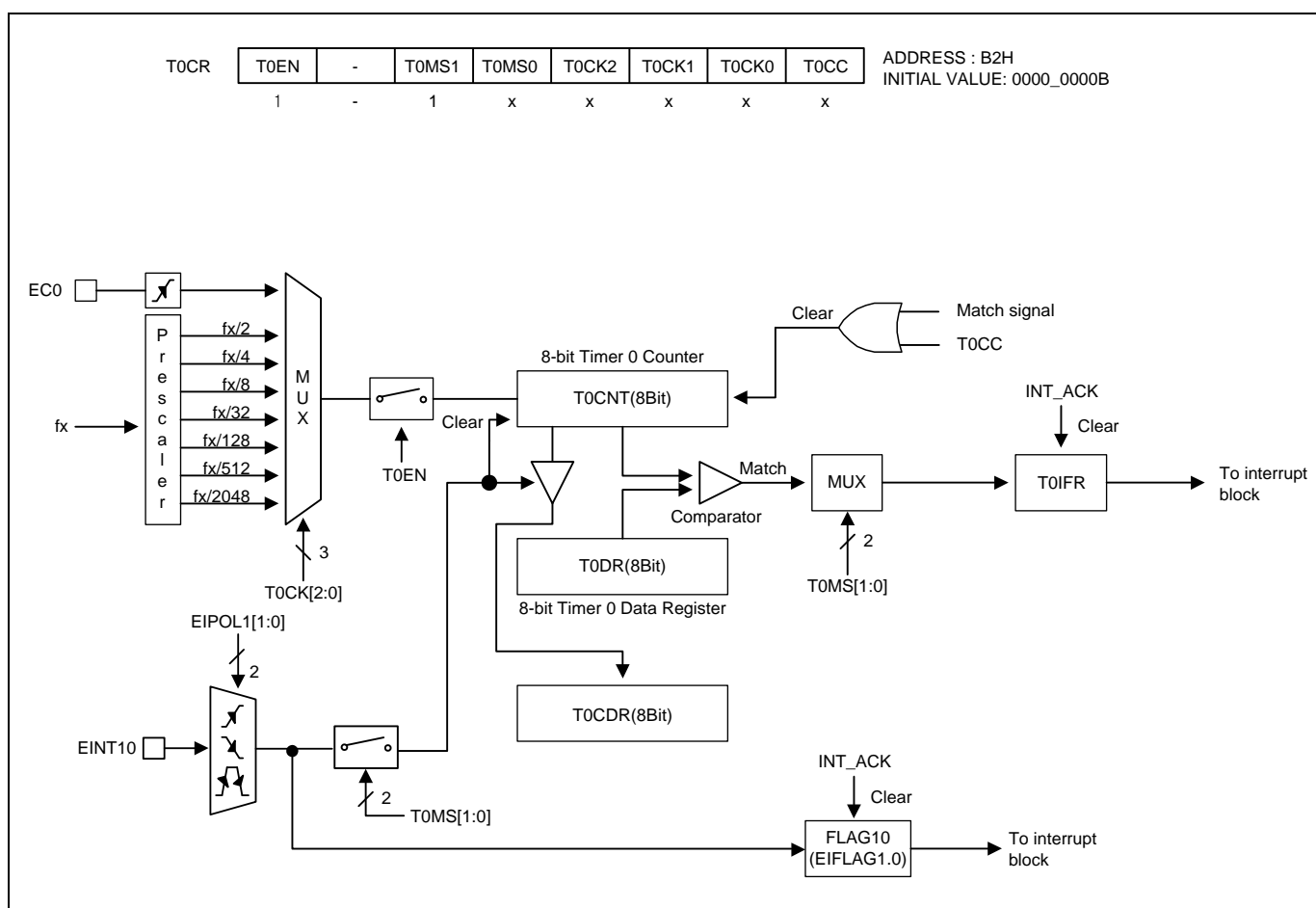


Figure 11.10 8-bit Capture Mode for Timer 0

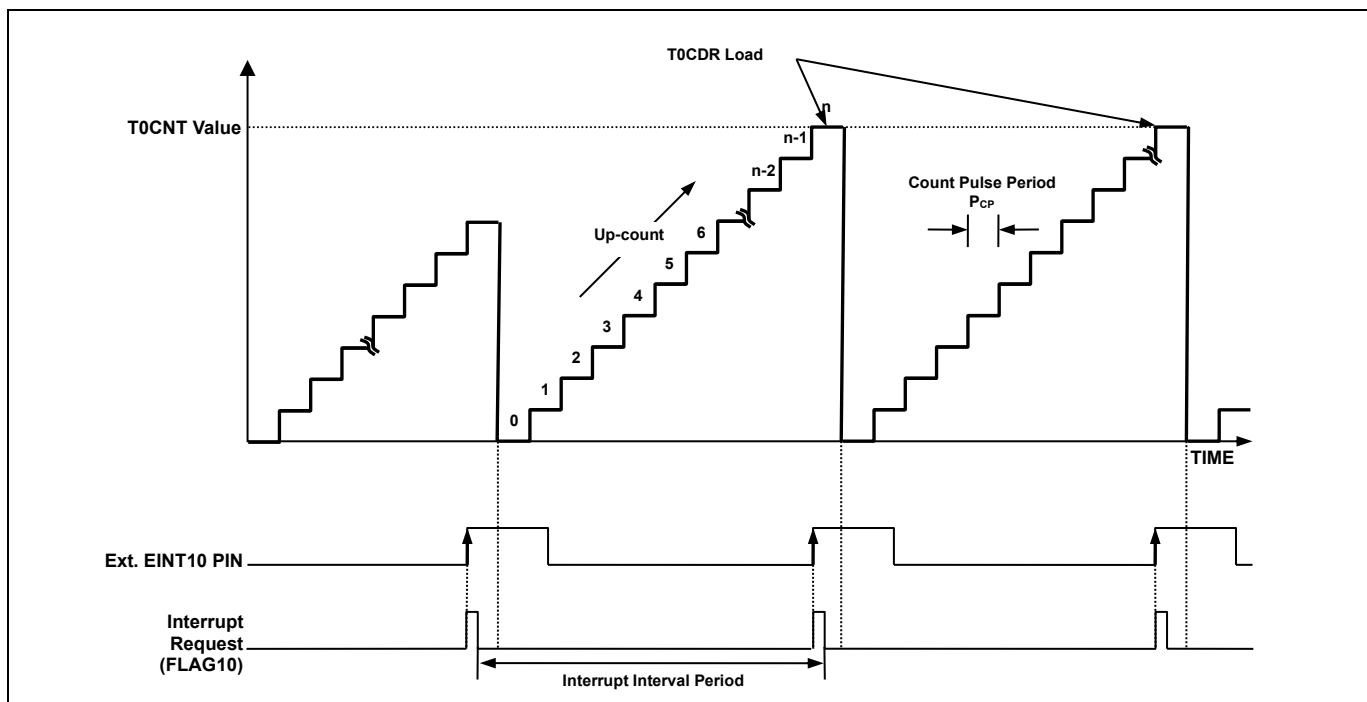


Figure 11.11 Input Capture Mode Operation for Timer 0

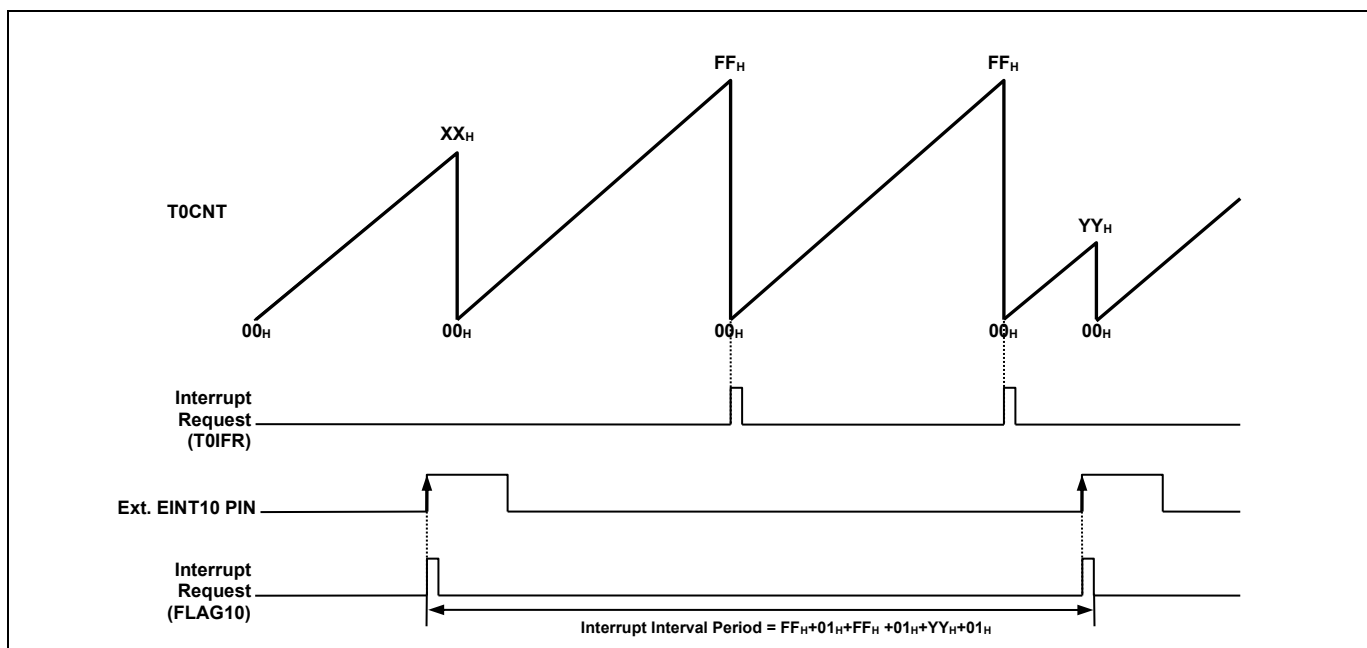


Figure 11.12 Express Timer Overflow in Capture Mode

### 11.5.5 Block Diagram

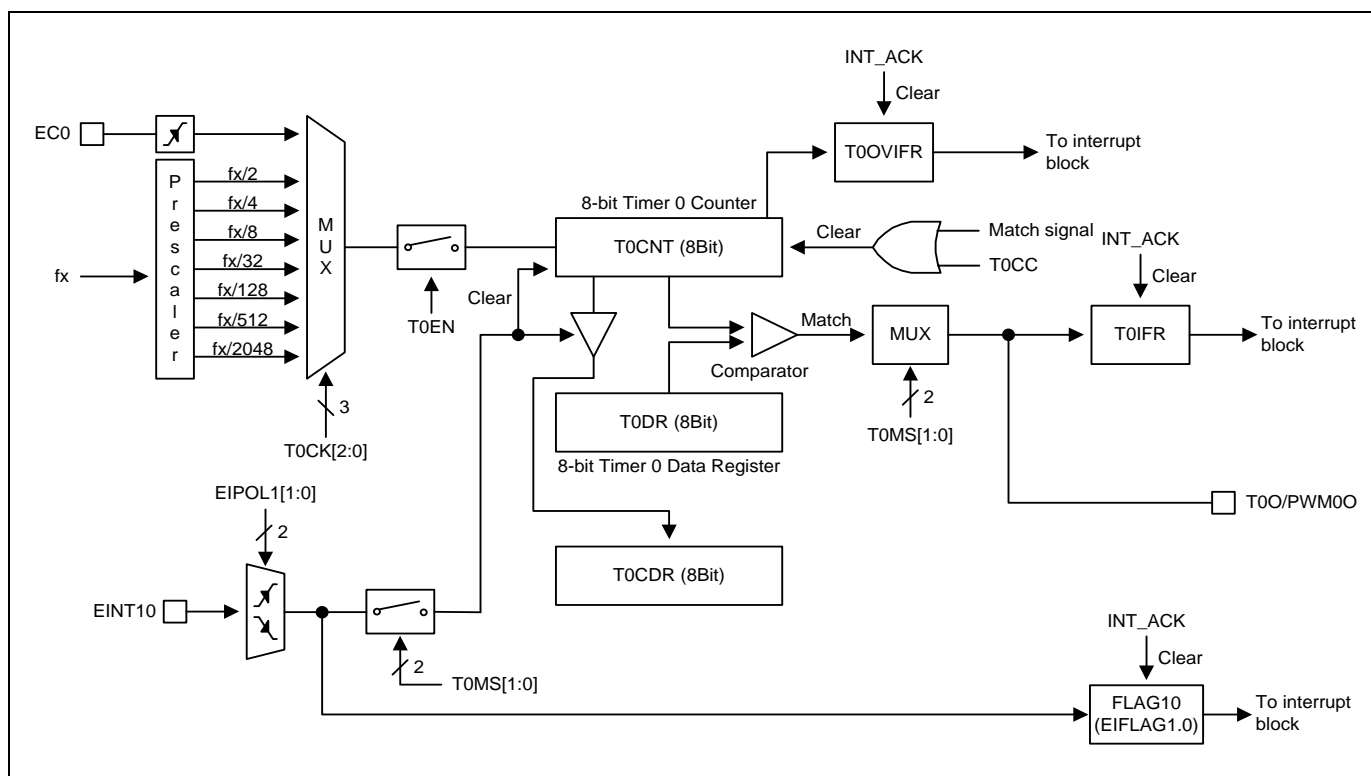


Figure 11.13 8-bit Timer 0 Block Diagram

### 11.5.6 Register Map

Name	Address	Direction	Default	Description
T0CNT	B3H	R	00H	Timer 0 Counter Register
T0DR	B4H	R/W	FFH	Timer 0 Data Register
T0CDR	B4H	R	00H	Timer 0 Capture Data Register
T0CR	B2H	R/W	00H	Timer 0 Control Register

Table 11.6 Timer 0 Register Map

### 11.5.7 Timer/Counter 0 Register Description

The timer/counter 0 register consists of timer 0 counter register ( $T0CNT$ ), timer 0 data register ( $T0DR$ ), timer 0 capture data register ( $T0CDR$ ) and timer 0 control register ( $T0CR$ ).  $T0IFR$  and  $T0OVI$  bits are in the external interrupt flag 1 register (EIFLAG1).

11.5.8 Register Description for Timer/Counter 0

**T0CNT (Timer 0 Counter Register): B3H**

7	6	5	4	3	2	1	0
T0CNT7	T0CNT6	T0CNT5	T0CNT4	T0CNT3	T0CNT2	T0CNT1	T0CNT0
R	R	R	R	R	R	R	R

Initial value: 00H

**T0CNT[7:0]** T0 Counter

**T0DR (Timer 0 Data Register): B4H**

7	6	5	4	3	2	1	0
T0DR7	T0DR6	T0DR5	T0DR4	T0DR3	T0DR2	T0DR1	T0DR0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: FFH

**T0DR[7:0]** T0 Data

**T0CDR (Timer 0 Capture Data Register: Read Case, Capture mode only): B4H**

7	6	5	4	3	2	1	0
T0CDR7	T0CDR6	T0CDR5	T0CDR4	T0CDR3	T0CDR2	T0CDR1	T0CDR0
R	R	R	R	R	R	R	R

Initial value: 00H

**T0CDR[7:0]** T0 Capture Data



## T0CR (Timer 0 Control Register): B2H

7	6	5	4	3	2	1	0
T0EN	–	T0MS1	T0MS0	T0CK2	T0CK1	T0CK0	T0CC
RW	–	RW	RW	RW	RW	RW	RW

Initial value: 00H

<b>T0EN</b>	Control Timer 0			
	0	Timer 0 disable		
	1	Timer 0 enable		
<b>T0MS[1:0]</b>	Control Timer 0 Operation Mode			
	T0MS1	T0MS0	Description	
	0	0	Timer/counter mode	
	0	1	PWM mode	
	1	x	Capture mode	
<b>T0CK[2:0]</b>	Select Timer 0 clock source. fx is a system clock frequency			
	T0CK2	T0CK1	T0CK0	Description
	0	0	0	fx/2
	0	0	1	fx/4
	0	1	0	fx/8
	0	1	1	fx/32
	1	0	0	fx/128
	1	0	1	fx/512
	1	1	0	fx/2048
	1	1	1	External Clock (EC0)
<b>T0CC</b>	Clear timer 0 Counter			
	0	No effect		
	1	Clear the Timer 0 counter (When write, automatically cleared "0" after being cleared counter)		

## NOTE)

1. Match Interrupt is generated in Capture mode.
2. Refer to the external interrupt flag 1 register (EIFLAG1) for the T0 interrupt flags.

## 11.6 Timer 1

### 11.6.1 Overview

The 16-bit timer 1 consists of multiplexer, timer 1 A data register high/low, timer 1 B data register high/low and timer 1 control register high/low (T1ADRH, T1ADRL, T1BDRH, T1BDRL, T1CRH, T1CRL).

It has four operating modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 1 can be clocked by an internal or an external clock source (EC1). The clock source is selected by clock selection logic which is controlled by the clock selection bits (T1CK[2:0]).

- TIMER 1 clock source:  $f_x/(1, 2, 4, 8, 64, 512, 2048)$ , EC1

In the capture mode, by EINT11, the data is captured into input capture data register (T1BDRH/T1BDRL). Timer 1 outputs the comparison result between counter and data register through T1O port in timer/counter mode. Also Timer 1 outputs PWM wave form through PWM1O port in the PPG mode.

T1EN	P1FSRL[5:4]	T1MS[1:0]	T1CK[2:0]	Timer 1
1	11	00	XXX	16-bit Timer/Counter Mode
1	00	01	XXX	16-bit Capture Mode
1	11	10	XXX	16-bit PPG Mode(one-shot mode)
1	11	11	XXX	16-bit PPG Mode(repeat mode)

**Table 11.7** Timer 1 Operating Modes

### 11.6.2 16-bit Timer/Counter Mode

The 16-bit timer/counter mode is selected by control register as shown in Figure 11.14.

The 16-bit timer has counter and data register. The counter register is increased by internal or external clock input. Timer 1 can use the input clock with one of 1, 2, 4, 8, 64, 512 and 2048 prescaler division rates (T1CK[2:0]). When the value of T1CNTH, T1CNTL and the value of T1ADRH, T1ADRL are identical in Timer 1 respectively, a match signal is generated and the interrupt of Timer 1 occurs. The T1CNTH, T1CNTL value is automatically cleared by match signal. It can be also cleared by software (T1CC).

The external clock (EC1) counts up the timer at the rising edge. If the EC1 is selected as a clock source by T1CK[2:0], EC1 port should be set to the input port by P13IO bit.

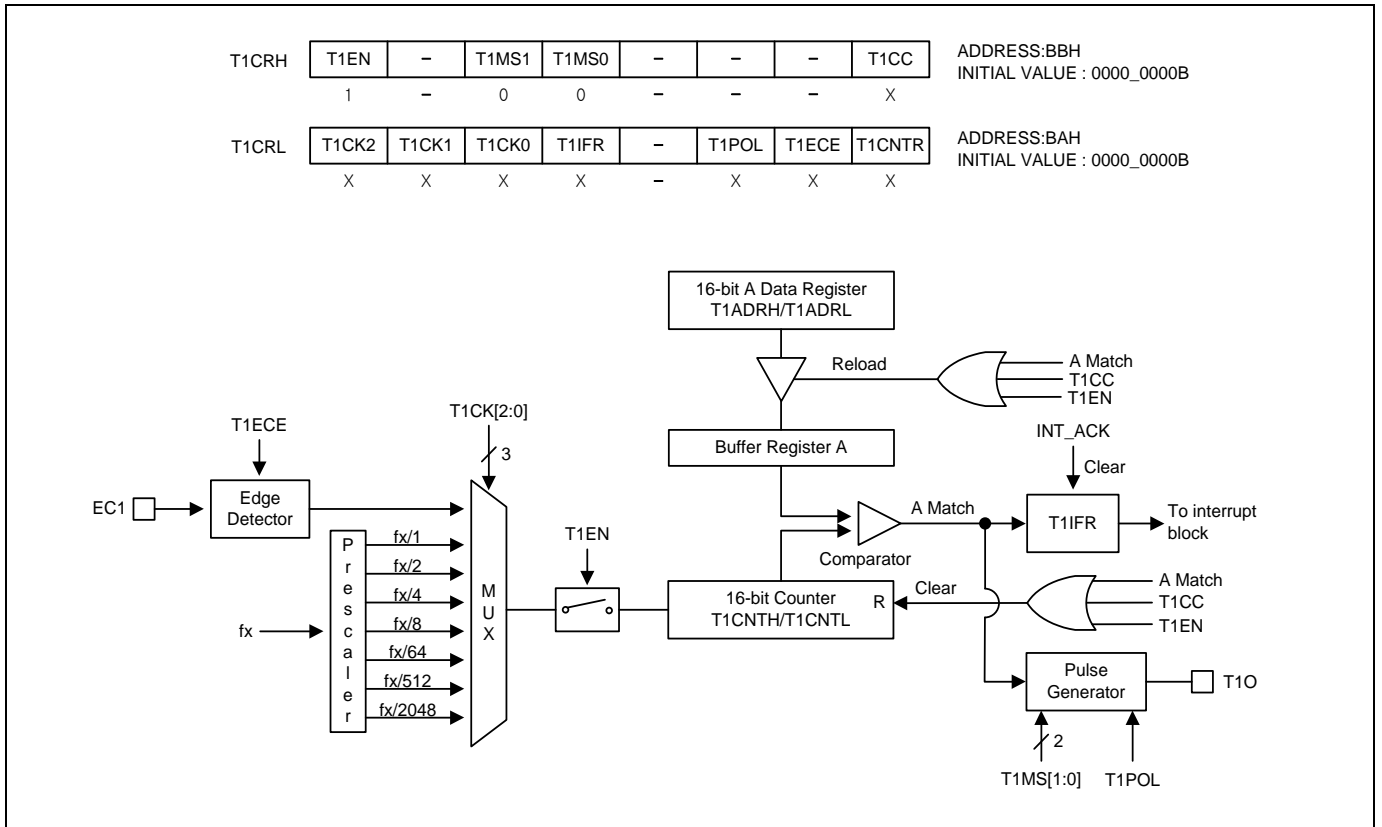


Figure 11.14 16-bit Timer/Counter Mode for Timer 1

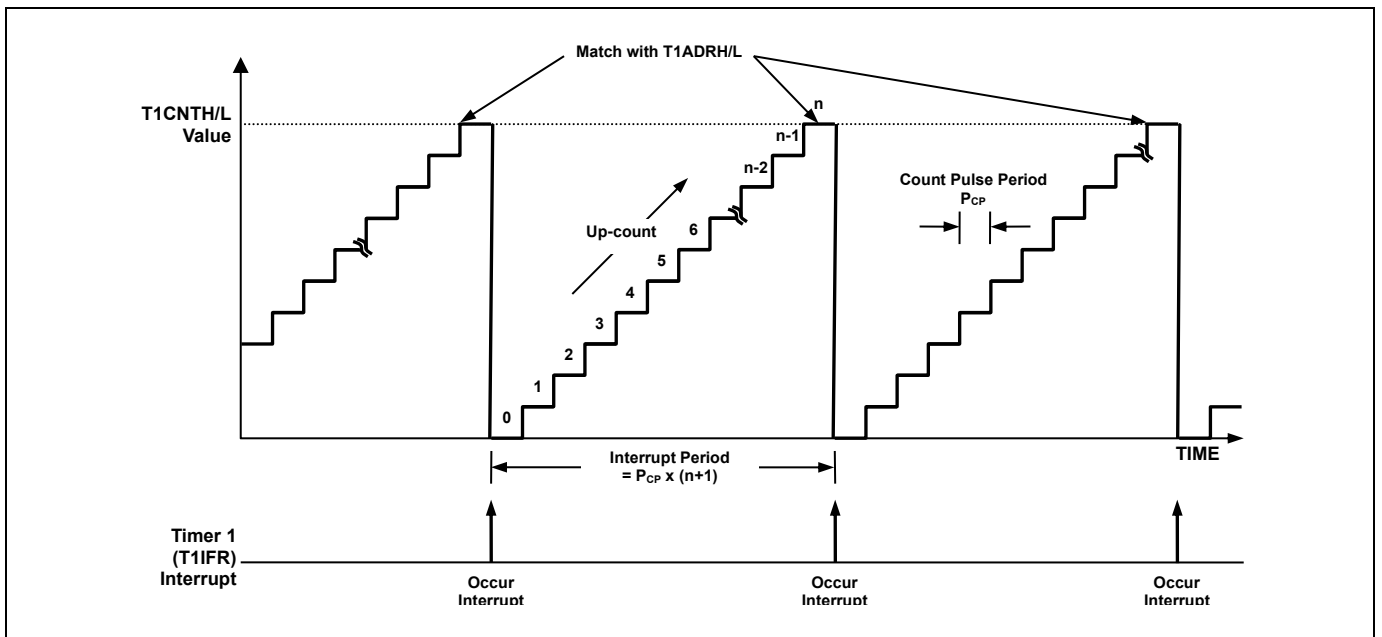


Figure 11.15 16-bit Timer/Counter 1 Example

### 11.6.3 16-bit Capture Mode

The 16-bit timer 1 capture mode is evoked by setting T1MS[1:0] as '01'. The clock source can use the internal/external clock. Basically, it has the same function as the 16-bit timer/counter mode and the interrupt occurs when T1CNTH/T1CNTL is equal to T1ADRH/T1ADRL. The T1CNTH, T1CNTL values are automatically cleared by match signal. It can be also cleared by software (T1CC).

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

The capture result is loaded into T1BDRH/T1BDRL.

According to EIPOL1 registers setting, the external interrupt EINT11 function is chosen. Of course, the EINT11 pin must be set as an input port.

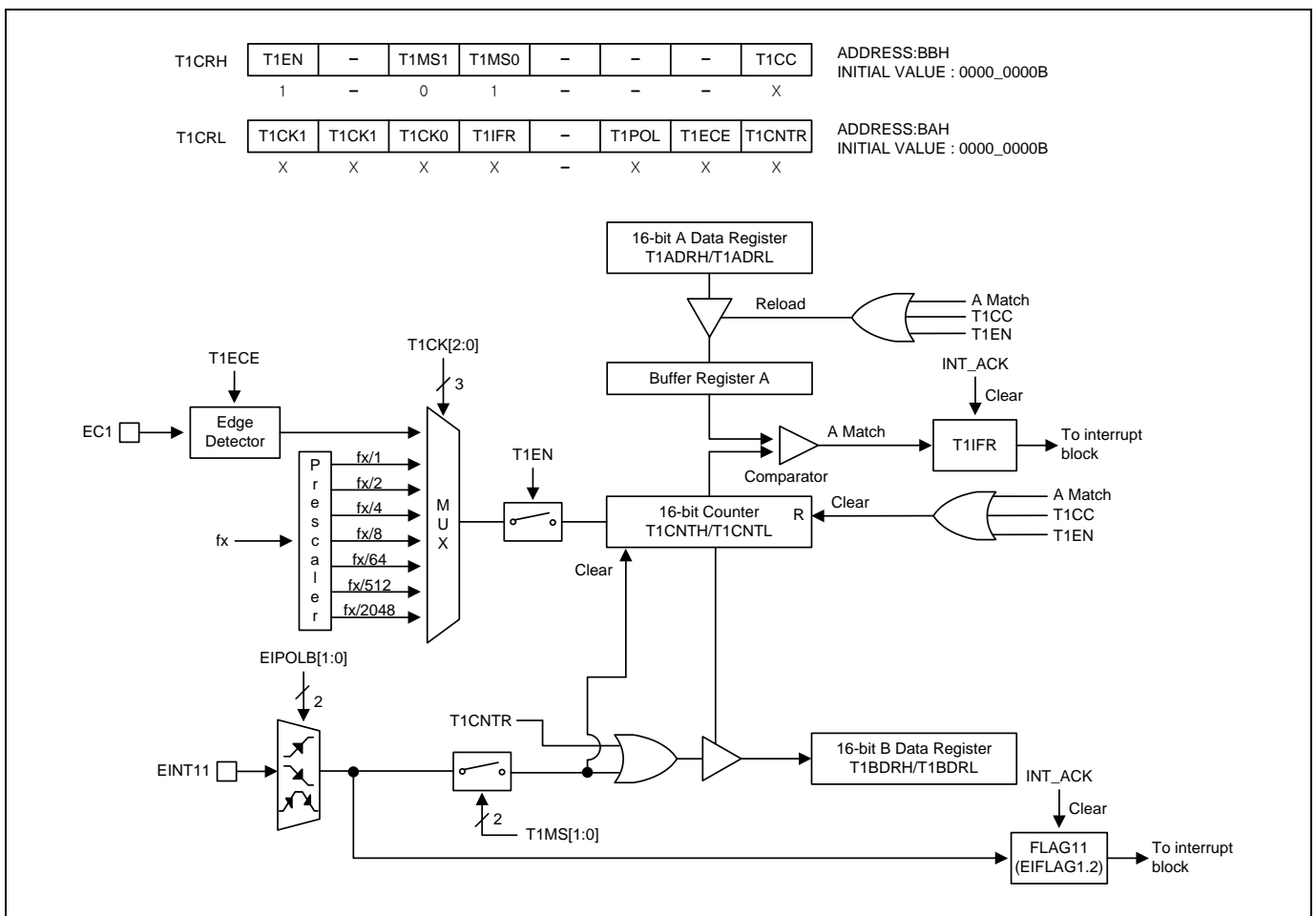


Figure 11.16 16-bit Capture Mode for Timer 1

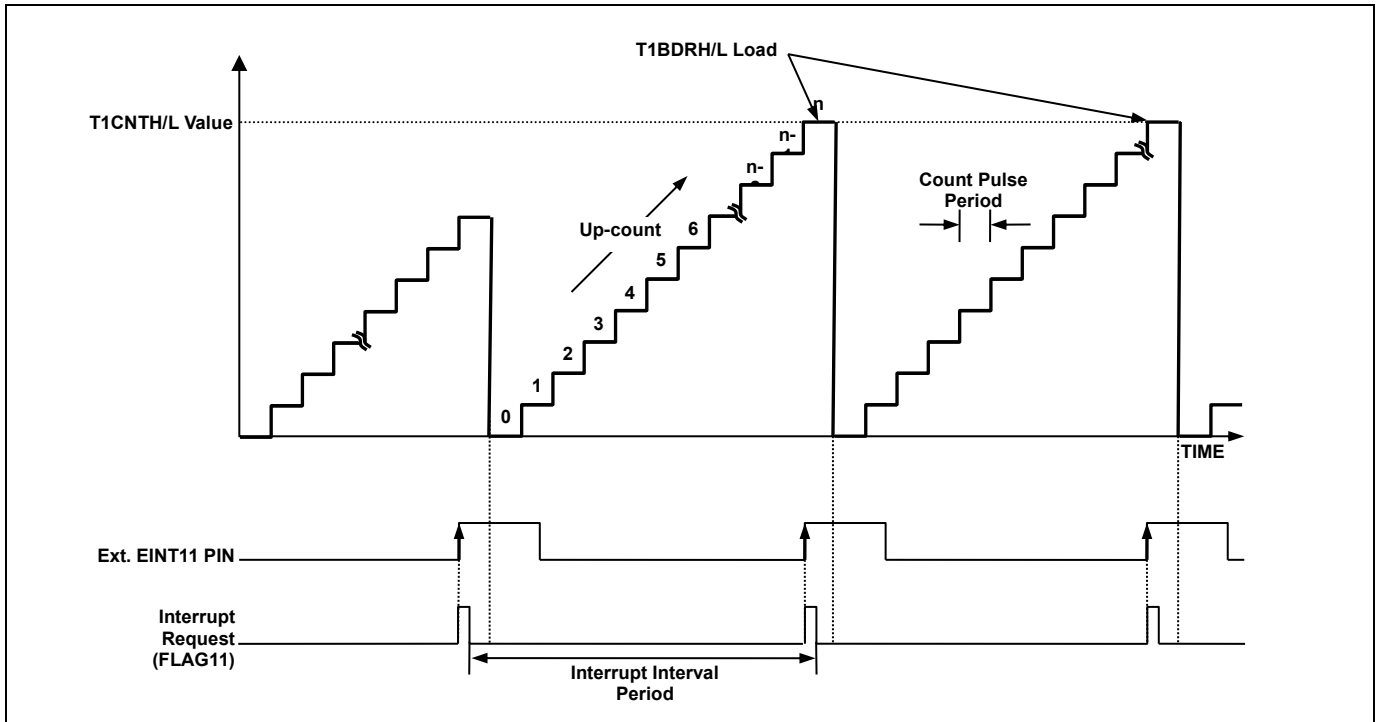


Figure 11.17 Input Capture Mode Operation for Timer 1

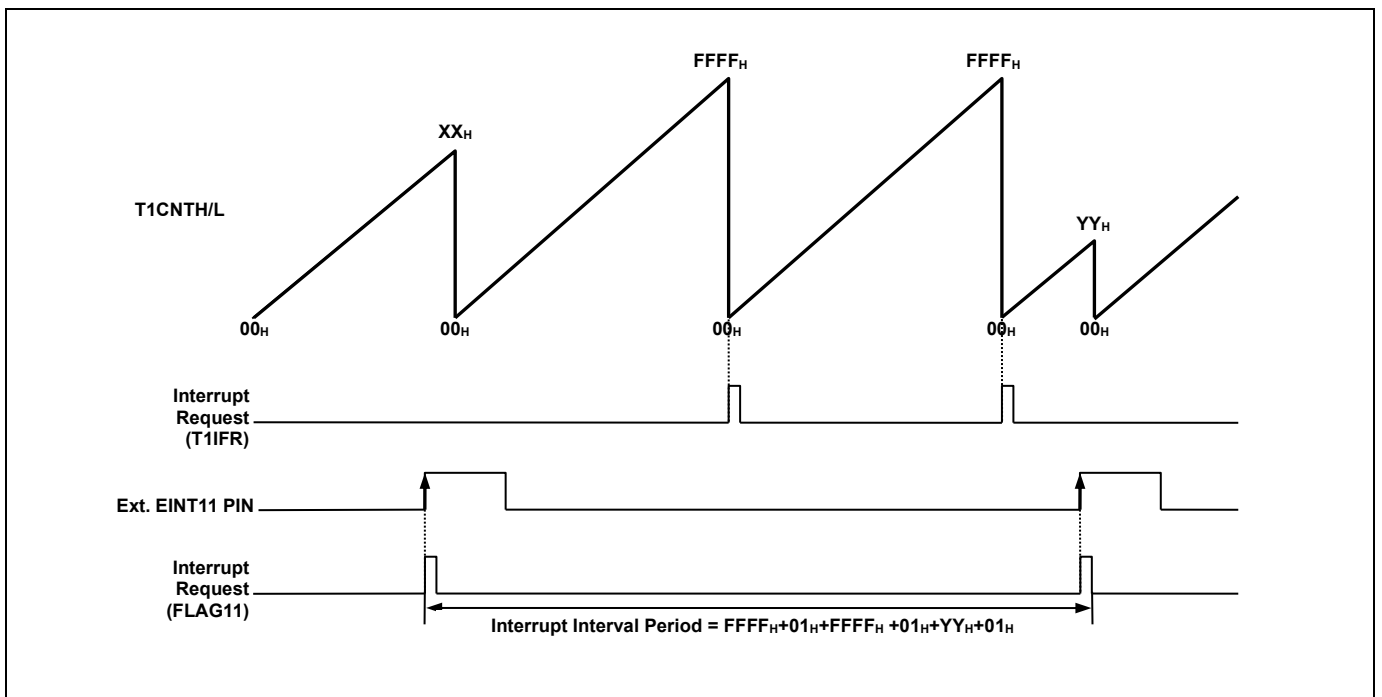


Figure 11.18 Express Timer Overflow in Capture Mode

11.6.4 16-bit PPG Mode

The timer 1 has a PPG (Programmable Pulse Generation) function. In PPG mode, T1O/PWM1O pin outputs up to 16-bit resolution PWM output. This pin should be configured as a PWM output by setting P1FSRL[5:4] to '11'. The period of the PWM output is determined by the T1ADRH/T1ADRL. And the duty of the PWM output is determined by the T1BDRH/T1BDRL.

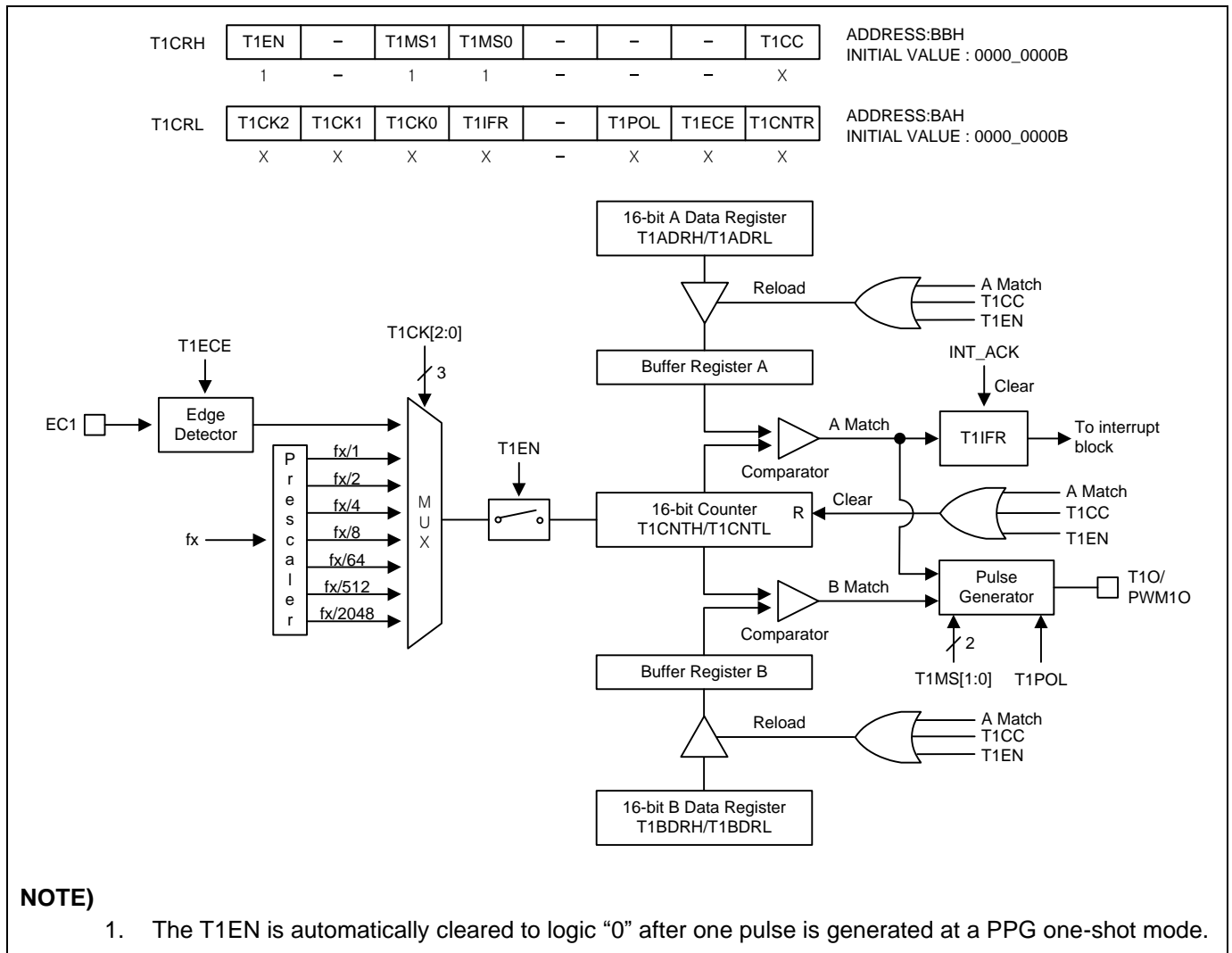


Figure 11.19 16-bit PPG Mode for Timer 1

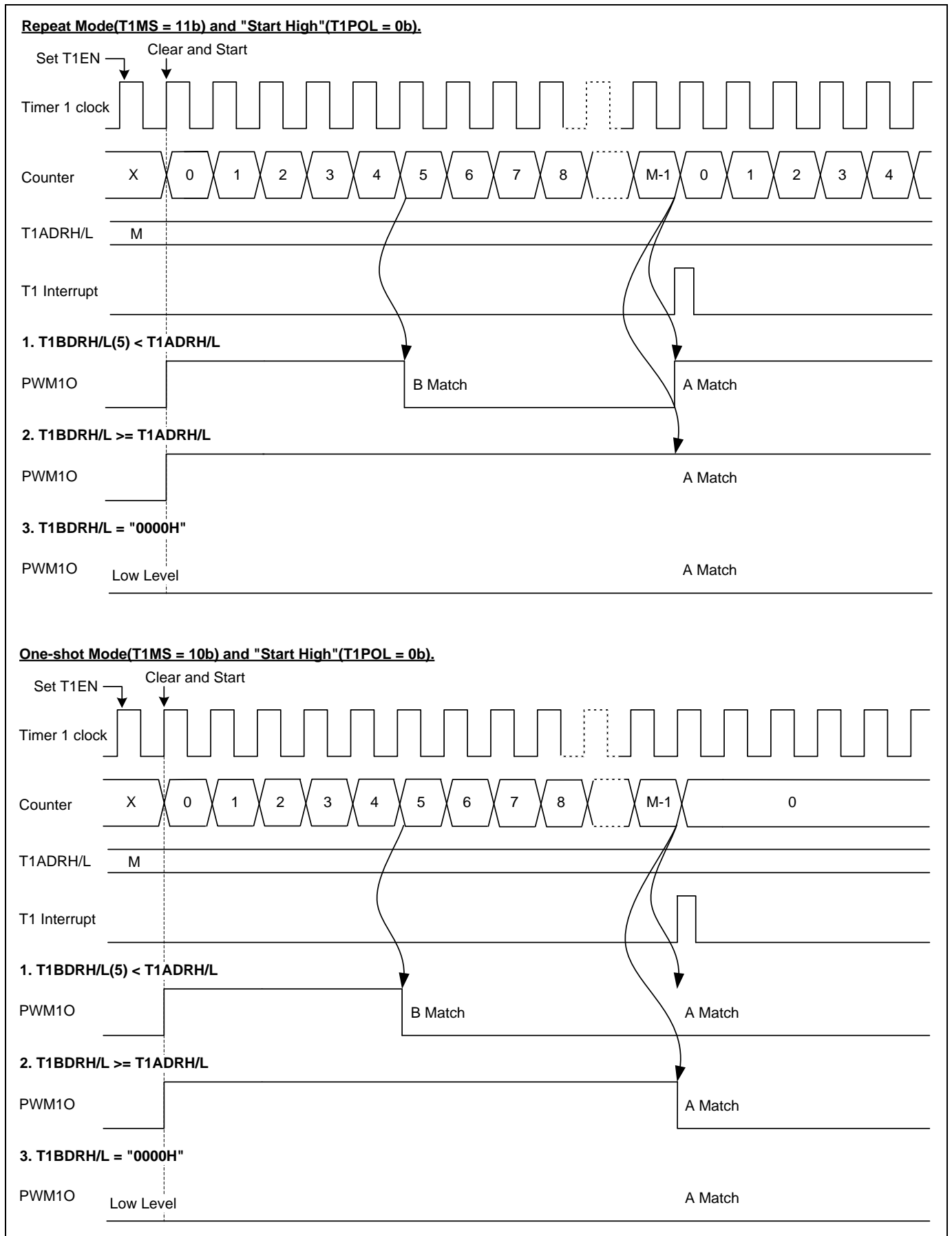


Figure 11.20 16-bit PPG Mode Timing chart for Timer 1

### 11.6.5 Block Diagram

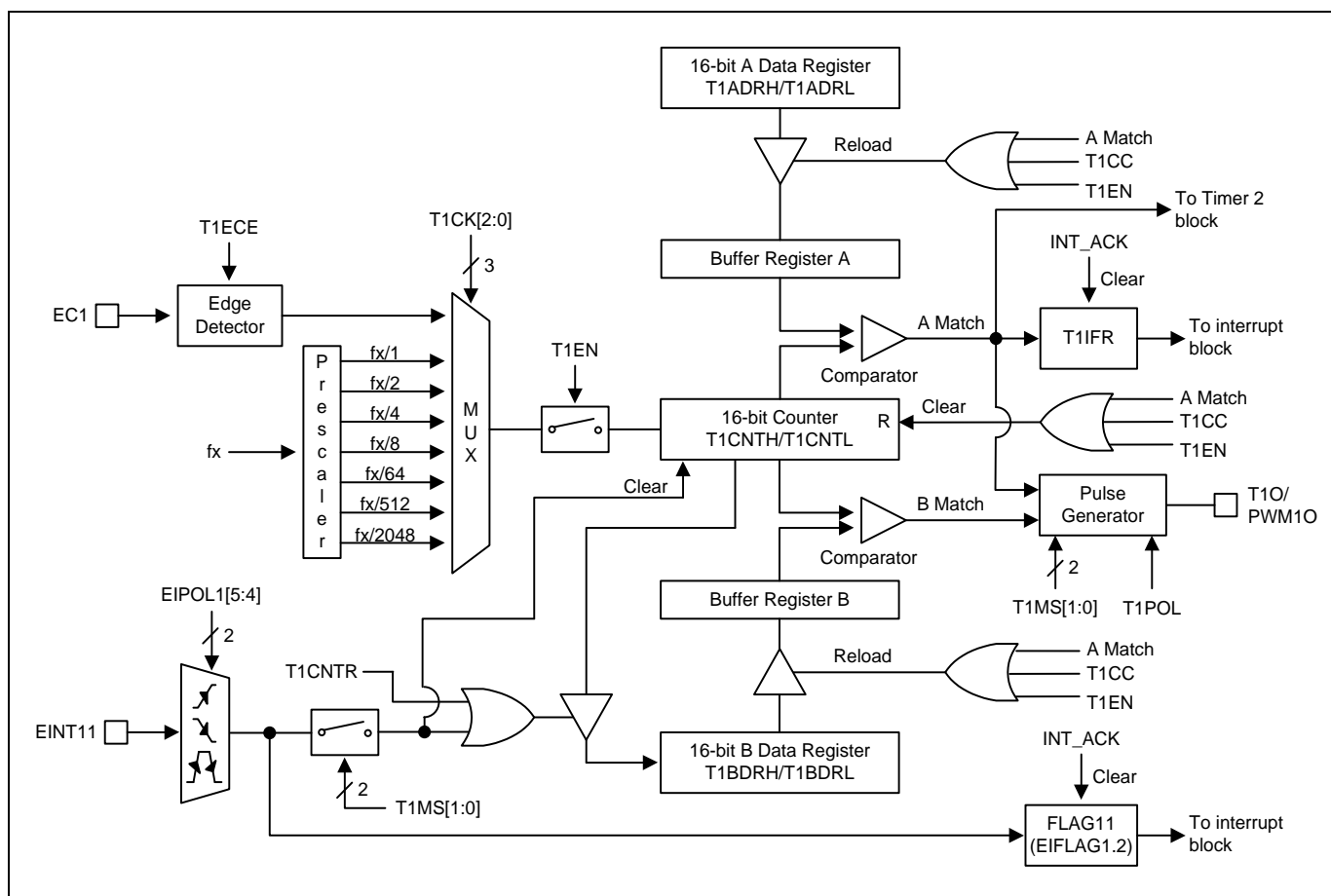


Figure 11.21 16-bit Timer 1 Block Diagram

### 11.6.6 Register Map

Name	Address	Direction	Default	Description
T1ADRH	BDH	R/W	FFH	Timer 1 A Data High Register
T1ADRL	BCH	R/W	FFH	Timer 1 A Data Low Register
T1BDRH	BFH	R/W	FFH	Timer 1 B Data High Register
T1BDRL	BEH	R/W	FFH	Timer 1 B Data Low Register
T1CRH	BBH	R/W	00H	Timer 1 Control High Register
T1CRL	BAH	R/W	00H	Timer 1 Control Low Register

Table 11.8 Timer 2 Register Map



### 11.6.7 Timer/Counter 1 Register Description

The timer/counter 1 register consists of timer 1 A data high register (T1ADRH), timer 1 A data low register (T1ADRL), timer 1 B data high register (T1BDRH), timer 1 B data low register (T1BDRL), timer 1 control high register (T1CRH) and timer 1 control low register (T1CRL).

### 11.6.8 Register Description for Timer/Counter 1

#### T1ADRH (Timer 1 A data High Register): BDH

7	6	5	4	3	2	1	0
T1ADRH7	T1ADRH6	T1ADRH5	T1ADRH4	T1ADRH3	T1ADRH2	T1ADRH1	T1ADRH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

**T1ADRH[7:0]** T1 A Data High Byte

#### T1ADRL (Timer 1 A Data Low Register): BCH

7	6	5	4	3	2	1	0
T1ADRL7	T1ADRL6	T1ADRL5	T1ADRL4	T1ADRL3	T1ADRL2	T1ADRL1	T1ADRL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

**T1ADRL[7:0]** T1 A Data Low Byte

#### NOTE)

- Do not write "0000H" in the T1ADRH/T1ADRL register when PPG mode

#### T1BDRH (Timer 1 B Data High Register): BFH

7	6	5	4	3	2	1	0
T1BDRH7	T1BDRH6	T1BDRH5	T1BDRH4	T1BDRH3	T1BDRH2	T1BDRH1	T1BDRH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

**T1BDRH[7:0]** T1 B Data High Byte

#### T1BDRL (Timer 1 B Data Low Register): BEH

7	6	5	4	3	2	1	0
T1BDRL7	T1BDRL6	T1BDRL5	T1BDRL4	T1BDRL3	T1BDRL2	T1BDRL1	T1BDRL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

**T1BDRL[7:0]** T1 B Data Low Byte

**T1CRH (Timer 1 Control High Register): BBH**

7	6	5	4	3	2	1	0
T1EN	–	T1MS1	T1MS0	–	–	–	T1CC
RW	–	R/W	R/W	–	–	–	R/W

Initial value: 00H

- T1EN** Control Timer 1
  - 0 Timer 1 disable
  - 1 Timer 1 enable (Counter clear and start)
- T1MS[1:0]** Control Timer 1 Operation Mode
 

T1MS1	T1MS0	Description
0	0	Timer/counter mode (T1O: toggle at A match)
0	1	Capture mode (The A match interrupt can occur)
1	0	PPG one-shot mode (PWM1O)
1	1	PPG repeat mode (PWM1O)
- T1CC** Clear Timer 1 Counter
  - 0 No effect
  - 1 Clear the Timer 1 counter (When write, automatically cleared "0" after being cleared counter)

**T1CRL (Timer 1 Control Low Register): BAH**

7	6	5	4	3	2	1	0
T1CK2	T1CK1	T1CK0	T1IFR	–	T1POL	T1ECE	T1CNTR
R/W	R/W	R/W	R/W	–	RW	RW	RW

Initial value: 00H

**T1CK[2:0]** Select Timer 1 clock source. fx is main system clock frequency

T1CK2	T1CK1	T1CK0	Description
0	0	0	fx/2048
0	0	1	fx/512
0	1	0	fx/64
0	1	1	fx/8
1	0	0	fx/4
1	0	1	fx/2
1	1	0	fx/1
1	1	1	External clock (EC1)

**T1IFR** When T1 Interrupt occurs, this bit becomes '1'. For clearing bit, write '0' to this bit or auto clear by INT\_ACK signal. Writing "1" has no effect.

0 T1 Interrupt no generation

1 T1 Interrupt generation

**T1POL** T1O/PWM1O Polarity Selection

0 Start High (T1O/PWM1O is low level at disable)

1 Start Low (T1O/PWM1O is high level at disable)

**T1ECE** Timer 1 External Clock Edge Selection

0 External clock falling edge

1 External clock rising edge

**T1CNTR** Timer 1 Counter Read Control

0 No effect

1 Load the counter value to the B data register (When write, automatically cleared "0" after being loaded)

## 11.7 Timer 2

### 11.7.1 Overview

The 16-bit timer 2 consists of multiplexer, timer 2 A data high/low register, timer 2 B data high/low register and timer 2 control high/low register (T2ADRH, T2ADRL, T2BDRH, T2BDRL, T2CRH and T2CRL).

It has four operating modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 2 can be divided clock of the system clock selected from prescaler output and T1 A Match (timer 1 A match signal). The clock source is selected by clock selection logic which is controlled by the clock selection bits (T2CK[2:0]).

- TIMER 2 clock source:  $f_x/(1, 2, 4, 8, 32, 128, 512)$ , T1 A Match

In the capture mode, by EINT12, the data is captured into input capture data register (T2BDRH/T2BDRL). In timer/counter mode, whenever counter value is equal to T2ADRH/L, T2O port toggles. Also the timer 2 outputs PWM wave form to PWM2O port in the PPG mode.

T2EN	P1FSRL[3:2]	T2MS[1:0]	T2CK[2:0]	Timer 2
1	11	00	XXX	16-bit Timer/Counter Mode
1	00	01	XXX	16-bit Capture Mode
1	11	10	XXX	16-bit PPG Mode (one-shot mode)
1	11	11	XXX	16-bit PPG Mode (repeat mode)

**Table 11.9** Timer 2 Operating Modes

### 11.7.2 16-bit Timer/Counter Mode

The 16-bit timer/counter mode is selected by control register as shown in Figure 11.22.

The 16-bit timer have counter and data register. The counter register is increased by internal or timer 1 A match clock input. Timer 2 can use the input clock with one of 1, 2, 4, 8, 32, 128, 512 and T1 A Match prescaler division rates (T2CK[2:0]). When the values of T2CNTH/T2CNTL and T2ADRH/T2ADRL are identical in timer 2, a match signal is generated and the interrupt of Timer 2 occurs. The T2CNTH/T2CNTL values are automatically cleared by match signal. It can be also cleared by software (T2CC).

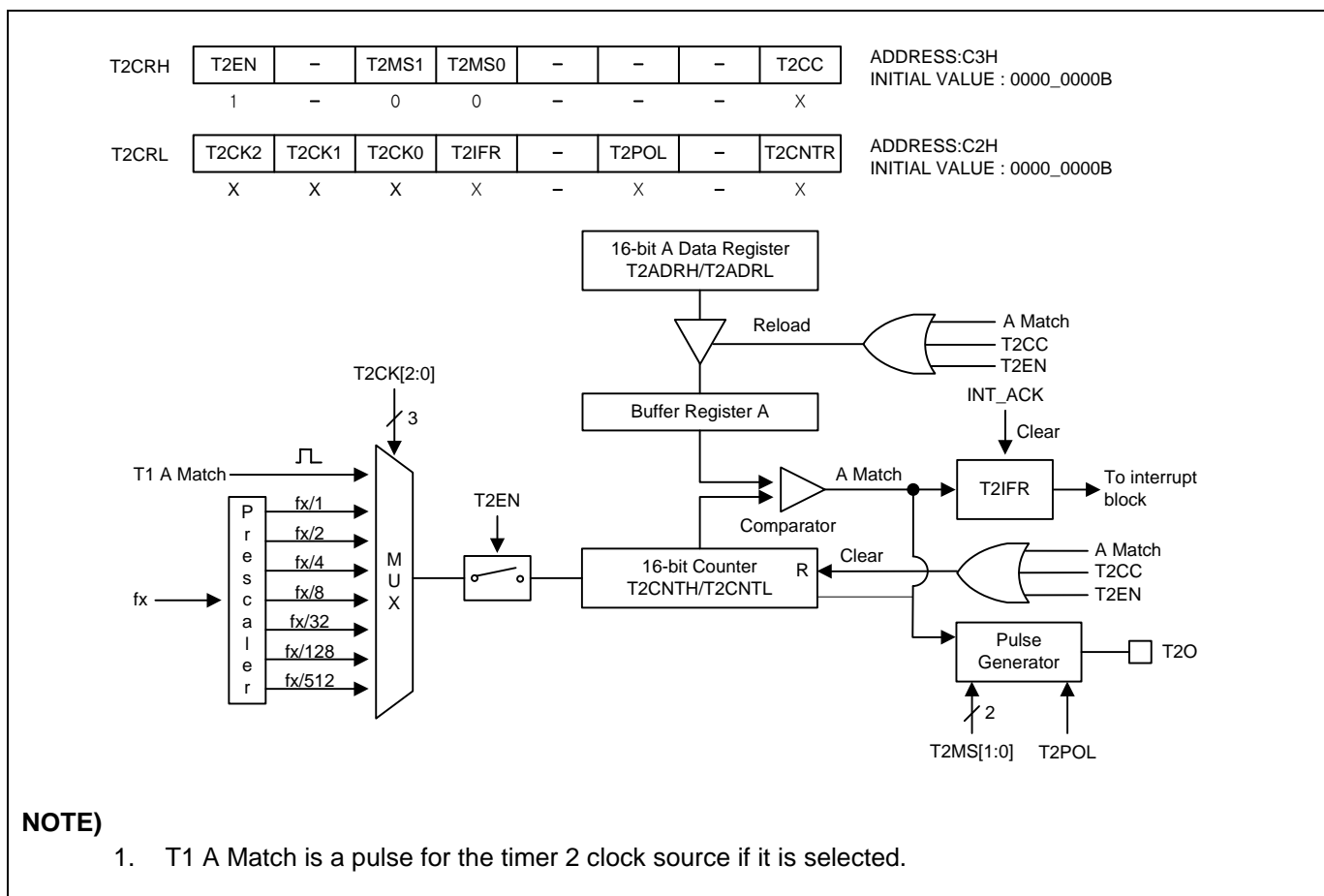


Figure 11.22 16-bit Timer/Counter Mode for Timer 2

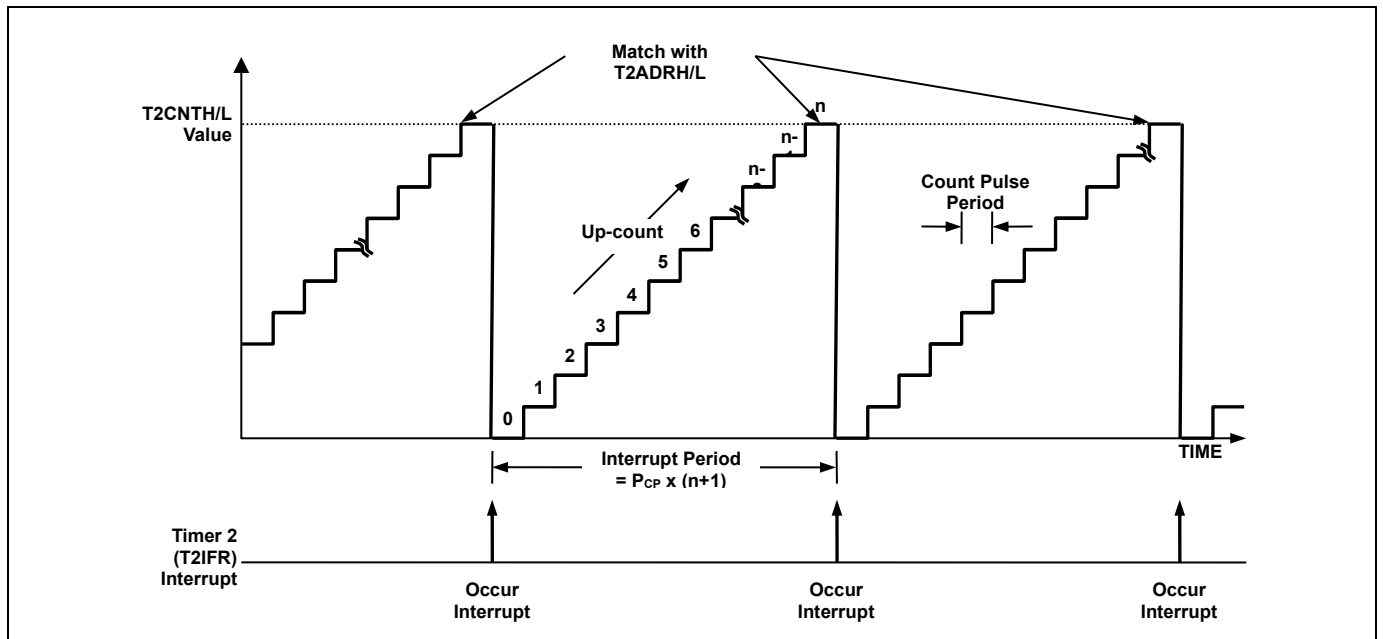


Figure 11.23 16-bit Timer/Counter 2 Example

### 11.7.3 16-bit Capture Mode

The timer 2 capture mode is evoked by setting T2MS[1:0] as '01'. The clock source can use the internal clock. Basically, it has the same function as the 16-bit timer/counter mode and the interrupt occurs when T2CNTH/T2CNTL is equal to T2ADRH/T2ADRL. T2CNTH/T2CNTL values are automatically cleared by match signal and it can be also cleared by software (T2CC).

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

The capture result is loaded into T2BDRH/T2BDRL. In the timer 2 capture mode, timer 2 output(T2O) waveform is not available.

According to EIPOL1 registers setting, the external interrupt EINT12 function is chosen. Of course, the EINT12 pin must be set to an input port.

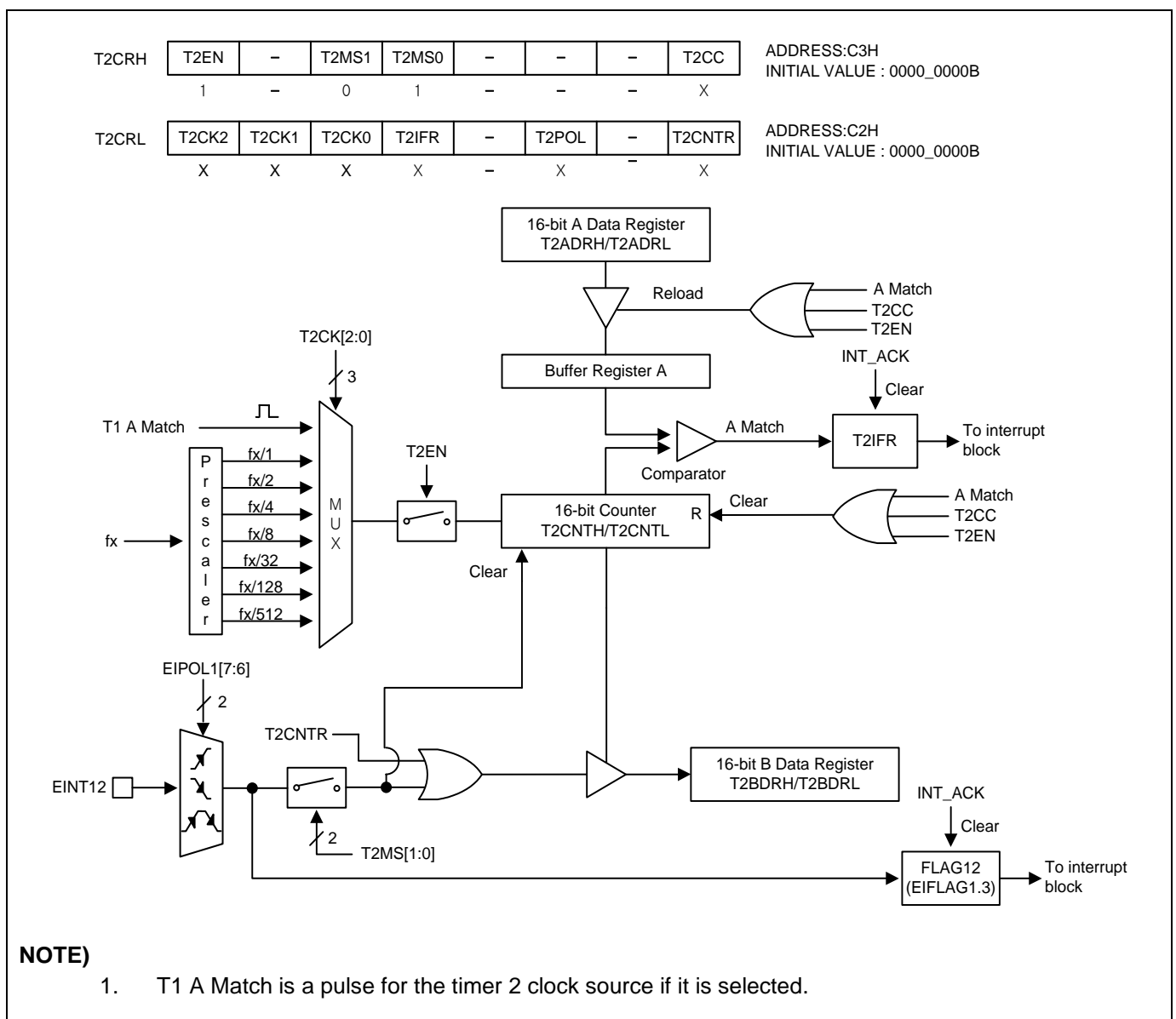


Figure 11.24 16-bit Capture Mode for Timer 2

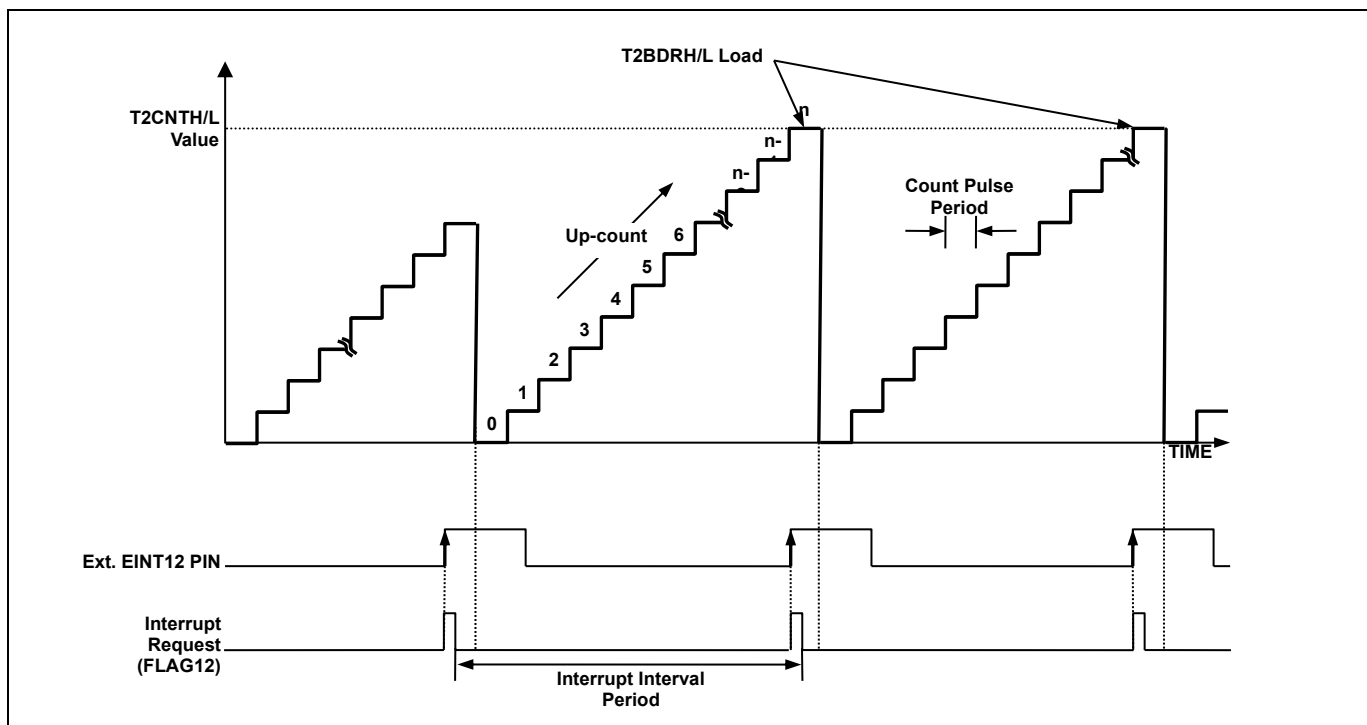


Figure 11.25 Input Capture Mode Operation for Timer 2

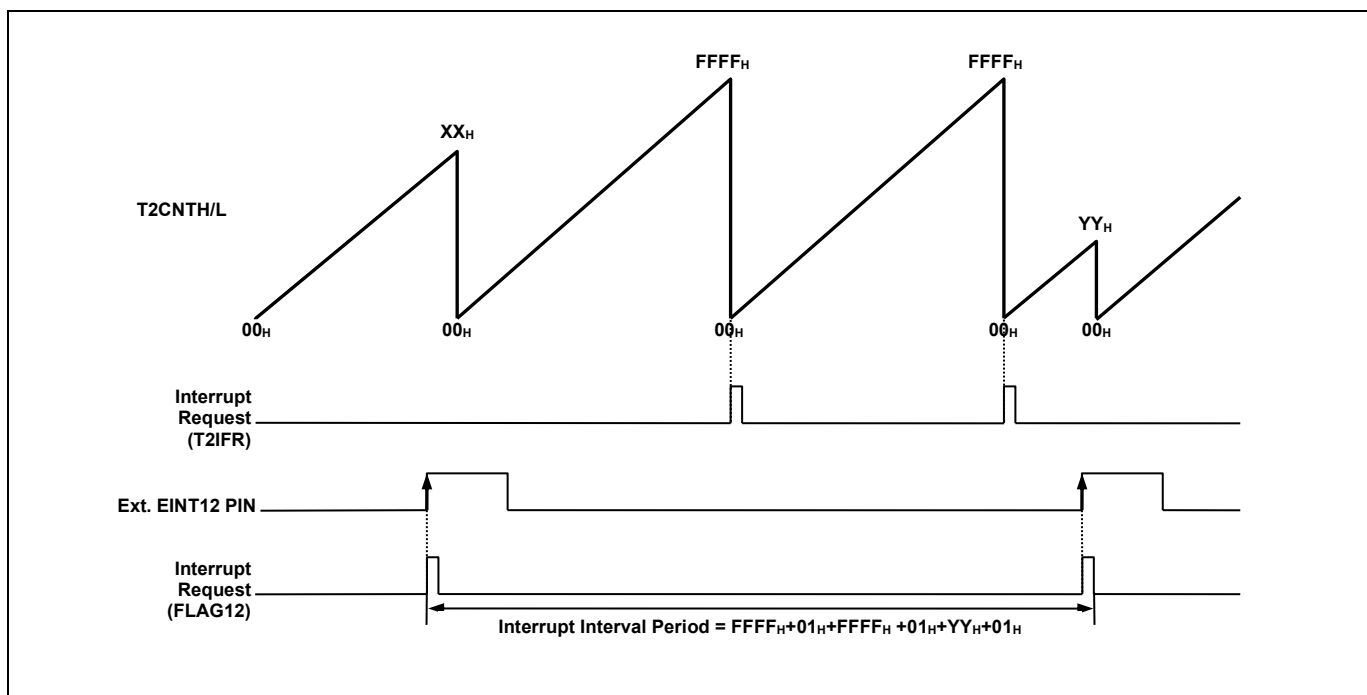


Figure 11.26 Express Timer Overflow in Capture Mode



11.7.4 16-bit PPG Mode

The timer 2 has a PPG (Programmable Pulse Generation) function. In PPG mode, the T2O/PWM2O pin outputs up to 16-bit resolution PWM output. This pin should be configured as a PWM output by set P1FSRL[3:2] to '11'. The period of the PWM output is determined by the T2ADRH/T2ADRL. And the duty of the PWM output is determined by the T2BDRH/T2BDRL.

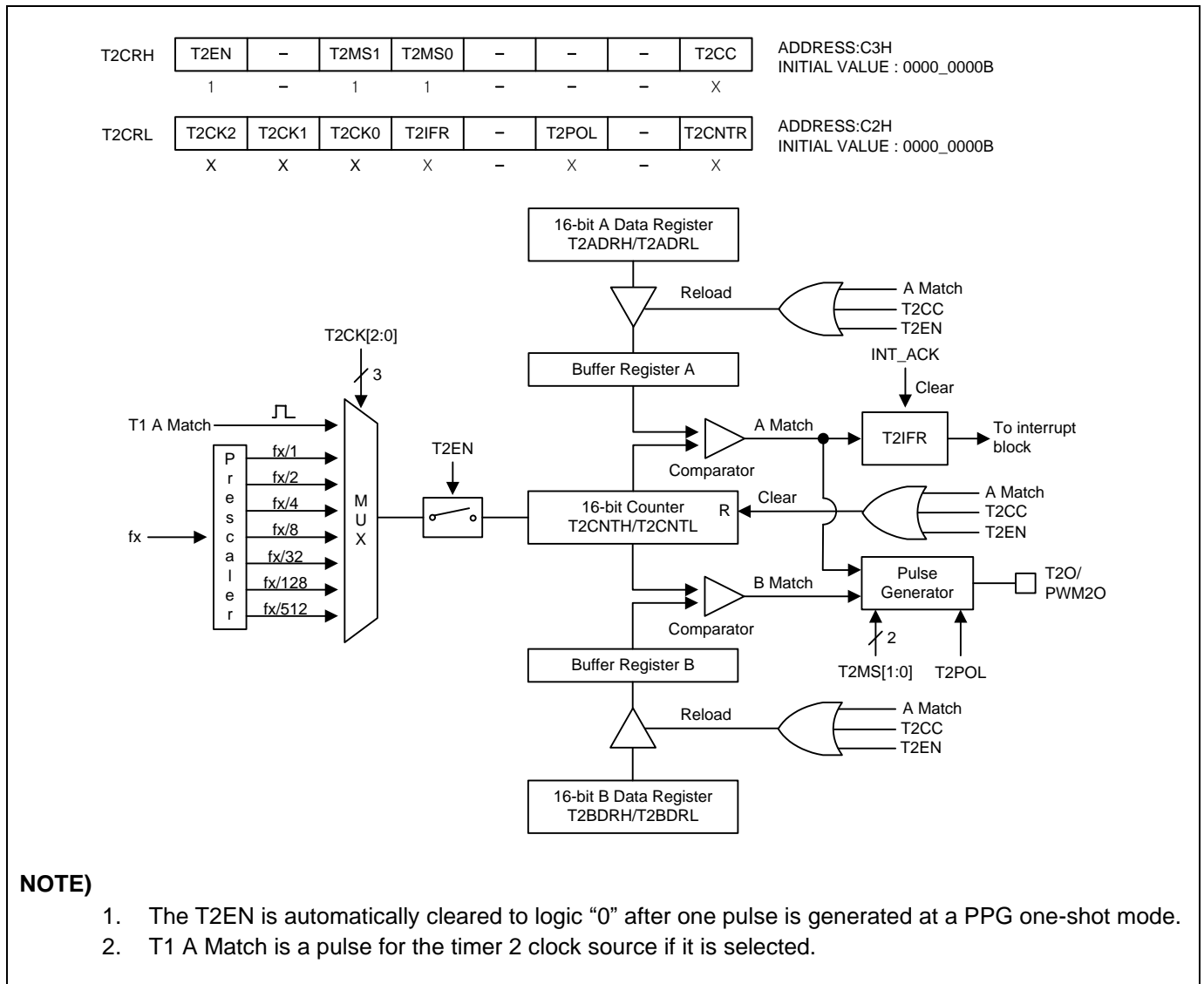


Figure 11.27 16-bit PPG Mode for Timer 2

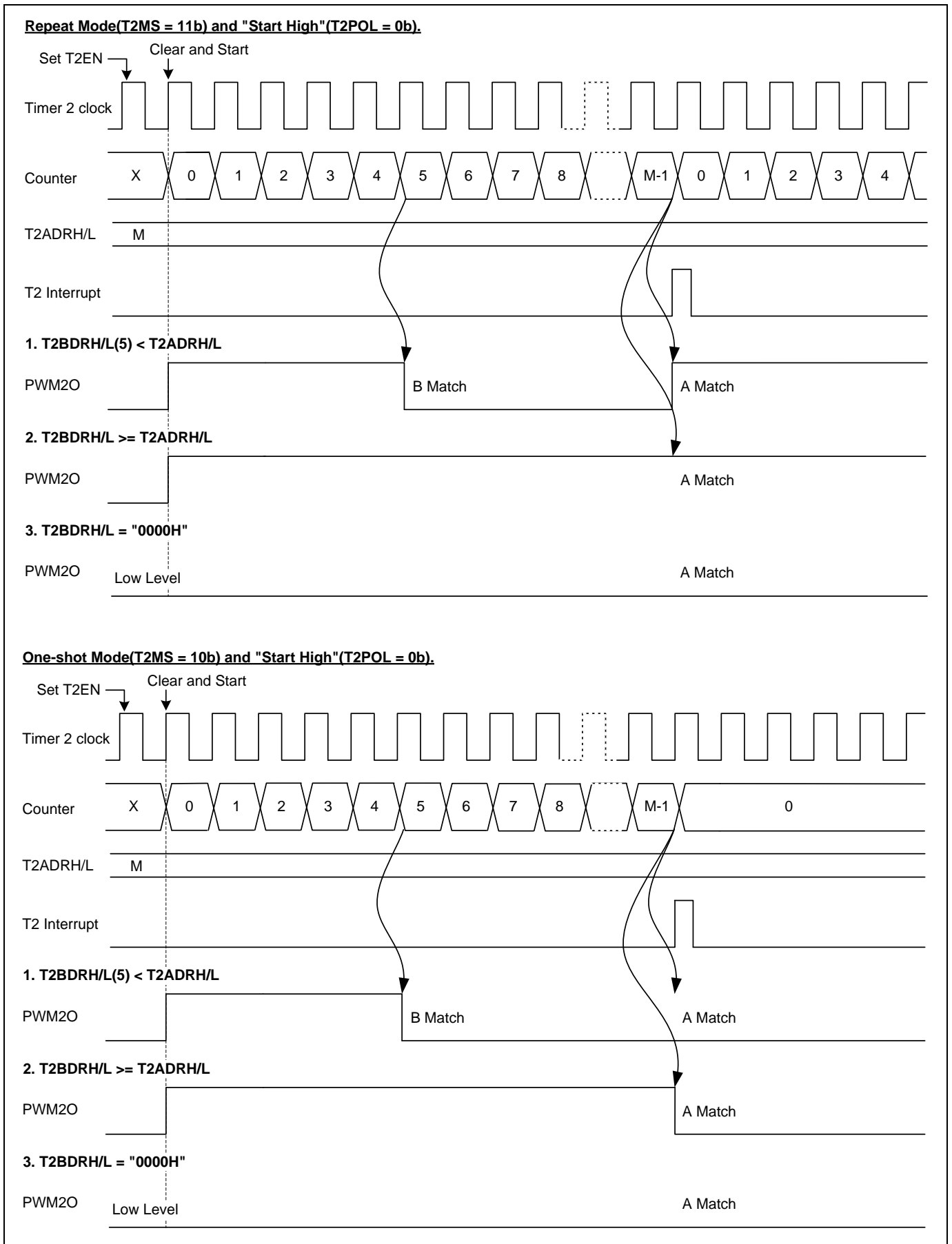


Figure 11.28 16-bit PPG Mode Timing chart for Timer 2

### 11.7.5 Block Diagram

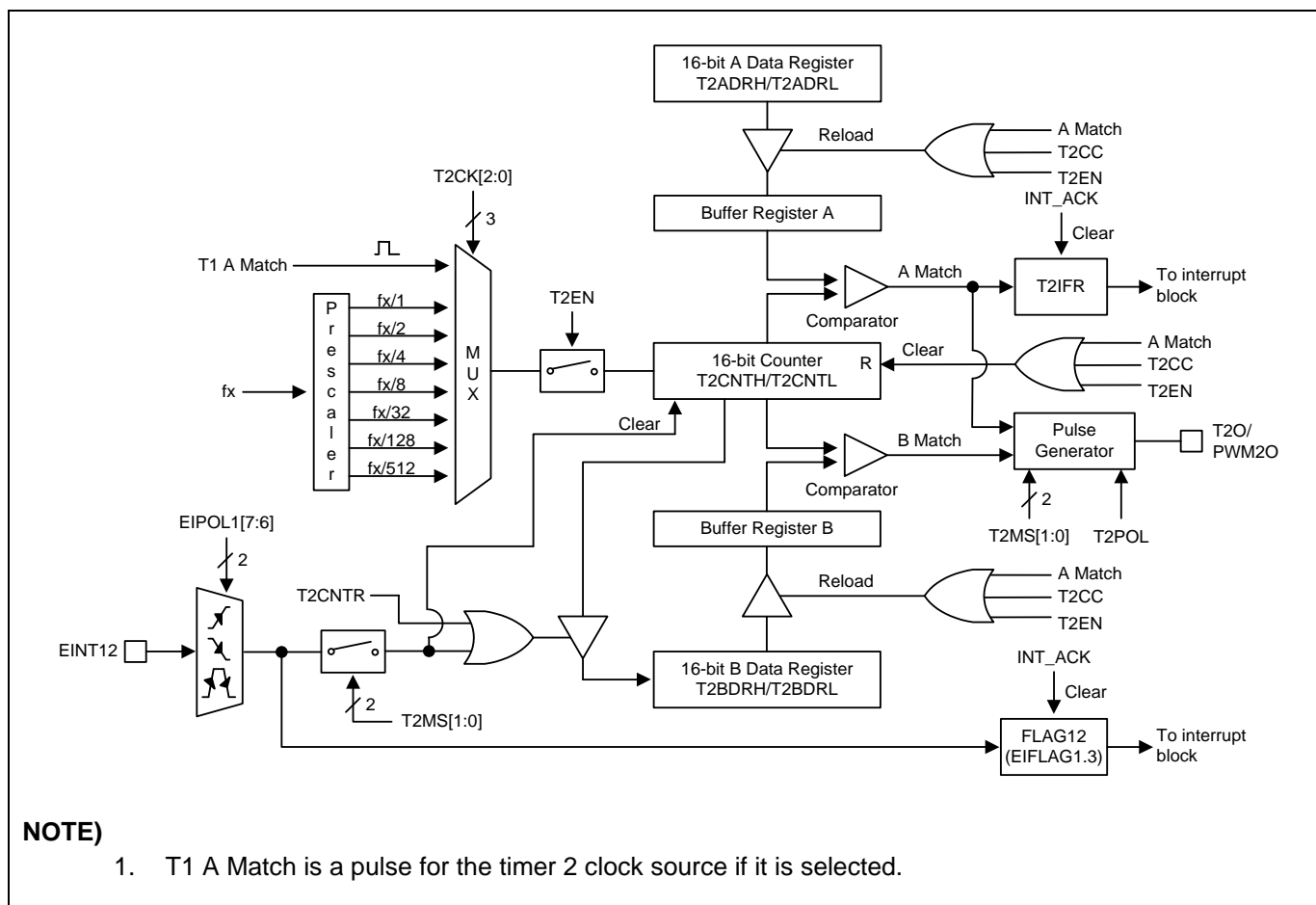


Figure 11.29 16-bit Timer 2 Block Diagram

### 11.7.6 Register Map

Name	Address	Direction	Default	Description
T2ADRH	C5H	R/W	FFH	Timer 2 A Data High Register
T2ADRL	C4H	R/W	FFH	Timer 2 A Data Low Register
T2BDRH	C7H	R/W	FFH	Timer 2 B Data High Register
T2BDRL	C6H	R/W	FFH	Timer 2 B Data Low Register
T2CRH	C3H	R/W	00H	Timer 2 Control High Register
T2CRL	C2H	R/W	00H	Timer 2 Control Low Register

Table 11.10 Timer 2 Register Map

### 11.7.7 Timer/Counter 2 Register Description

The timer/counter 2 register consists of timer 2 A data high register (T2ADRH), timer 2 A data low register (T2ADRL), timer 2 B data high register (T2BDRH), timer 2 B data low register (T2BDRL), timer 2 control high register (T2CRH) and timer 2 control low register (T2CRL).

### 11.7.8 Register Description for Timer/Counter 2

#### T2ADRH (Timer 2 A data High Register): C5H

7	6	5	4	3	2	1	0
T2ADRH7	T2ADRH6	T2ADRH5	T2ADRH4	T2ADRH3	T2ADRH2	T2ADRH1	T2ADRH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

**T2ADRH[7:0]** T2 A Data High Byte

#### T2ADRL (Timer 2 A Data Low Register): C4H

7	6	5	4	3	2	1	0
T2ADRL7	T2ADRL6	T2ADRL5	T2ADRL4	T2ADRL3	T2ADRL2	T2ADRL1	T2ADRL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

**T2ADRL[7:0]** T2 A Data Low Byte

**NOTE)**

1. Do not write "0000H" in the T2ADRH/T2ADRL register when PPG mode.

#### T2BDRH (Timer 2 B Data High Register): C7H

7	6	5	4	3	2	1	0
T2BDRH7	T2BDRH6	T2BDRH5	T2BDRH4	T2BDRH3	T2BDRH2	T2BDRH1	T2BDRH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

**T2BDRH[7:0]** T2 B Data High Byte

#### T2BDRL (Timer 2 B Data Low Register): C6H

7	6	5	4	3	2	1	0
T2BDRL7	T2BDRL6	T2BDRL5	T2BDRL4	T2BDRL3	T2BDRL2	T2BDRL1	T2BDRL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: FFH

**T2BDRL[7:0]** T2 B Data Low Byte

T2CRH (Timer 2 Control High Register): C3H

7	6	5	4	3	2	1	0
T2EN	–	T2MS1	T2MS0	–	–	–	T2CC
RW	–	R/W	R/W	–	–	–	R/W

Initial value: 00H

- T2EN** Control Timer 2
  - 0 Timer 2 disable
  - 1 Timer 2 enable (Counter clear and start)
- T2MS[1:0]** Control Timer 2 Operation Mode
 

T2MS1	T2MS0	Description
0	0	Timer/counter mode (T2O: toggle at A match)
0	1	Capture mode (The A match interrupt can occur)
1	0	PPG one-shot mode (PWM2O)
1	1	PPG repeat mode (PWM2O)
- T2CC** Clear Timer 2 Counter
  - 0 No effect
  - 1 Clear the Timer 2 counter (When write, automatically cleared "0" after being cleared counter)

**T2CRL (Timer 2 Control Low Register): CAH**

7	6	5	4	3	2	1	0
T2CK2	T2CK1	T2CK0	T2IFR	–	T2POL	–	T2CNTR
R/W	R/W	R/W	R/W	–	RW	–	R/W

Initial value: 00H

**T2CK[2:0]** Select Timer 2 clock source. fx is main system clock frequency

T2CK2	T2CK1	T2CK0	Description
0	0	0	fx/512
0	0	1	fx/128
0	1	0	fx/32
0	1	1	fx/8
1	0	0	fx/4
1	0	1	fx/2
1	1	0	fx/1
1	1	1	T1 A Match

**T2IFR** When T2 Match Interrupt occurs, this bit becomes '1'. For clearing bit, write '0' to this bit or auto clear by INT\_ACK signal. Writing "1" has no effect.

0	T2interrupt no generation
1	T2 interrupt generation

**T2POL** T2O/PWM2O Polarity Selection

0	Start High (T2O/PWM2O is low level at disable)
1	Start Low (T2O/PWM2O is high level at disable)

**T2CNTR** Timer 2 Counter Read Control

0	No effect
1	Load the counter value to the B data register (When write, automatically cleared "0" after being loaded)

## 11.8 Timer 3, 4

### 11.8.1 Overview

Timer 3 and timer 4 can be used as either two 8-bit timer/counter or one 16-bit timer/counter with combine them. Each 8-bit timer/event counter module has multiplexer, comparator, 8-bit timer data register, 8-bit counter register, control register and capture data register(T3CNT, T3DR, T3CAPR, T3CR, T4CNT, T4DR, T4CAPR and T4CR). For PWM, it has PWM register (T4PPRL, T4PPRH, T4ADRL, T4ADRH, T4BDRL, T4BDRH, T4CDRL, T4CDRH, T4DLYA, T4DLYB, T4DLYC).

It has five operating modes:

- 8-bit timer/counter mode
- 8-bit capture mode
- 16-bit timer/counter mode
- 16-bit capture mode
- 10-bit PWM mode

The timer/counter 3 and 4 can be clocked by an internal or an external clock source (EC3).The clock source is selected by clock selection logic which is controlled by the clock selection bits (T3CK[2:0], T4CK[3:0]). Also the timer/counter 4 can use more clock sources than timer/counter 3.

- TIMER 3 clock source:  $fx/(2, 4, 8, 32, 128, 512, 2048)$ , EC3
- TIMER 4 clock source:  $fx/(1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, 4096, 8192, 16384)$ , T3 clock

In the capture mode, by EINT0/EINT1, the data is captured into input capture data register (T3CAPR, T4CAPR).

In 8-bit timer/counter 3/4 mode, whenever counter value is equal to T3DR/T4DR, T3O/T4O port toggles. Also In 16-bit timer/counter 3 mode,

The timer 3 outputs the comparison result between counter and data register through T3O port. The PWM wave form to PWMAA, PWMAB, PWMBA, PWMBB, PWMCA, PWMCB Port(6-channel) in the PWM mode.

16BIT	T3MS	T4MS	PWM4E	T3CK[2:0]	T4CK[3:0]	Timer 3	Timer 4
0	0	0	0	XXX	XXXX	8-bit Timer/Counter Mode	8-bit Timer/Counter Mode
0	1	1	0	XXX	XXXX	8-bit Capture Mode	8-bit Capture Mode
1	0	0	0	XXX	XXXX	16-bit Timer/Counter Mode	
1	1	1	0	XXX	XXXX	16-bit Capture Mode	
0	X	X	1	XXX	XXXX	10-bit PWM Mode	

**Table 11.11** Timer 3, 4 Operating Modes

11.8.2 8-bit Timer/Counter 3, 4 Mode

The 8-bit timer/counter mode is selected by control register as shown in Figure 11.30.

The two 8-bit timers have each counter and data register. The counter register is increased by internal or external clock input. Timer 3 can use the input clock with one of 2, 4, 8, 32, 128, 512, 2048 and EC3 prescaler division rates (T3CK[2:0]). Timer 4 can use the input clock with one of 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, 4096, 8192, 16384 and timer 3 clock prescaler division rates (T4CK[3:0]). When the value of T3CNT, T4CNT and T3DR, T4DR are respectively identical in Timer 3, 4, the interrupt Timer 3, 4 occurs.

The external clock (EC3) counts up the timer at the rising edge. If the EC3 is selected as a clock source by T3CK[2:0], EC3 port should be set to the input port by P00IO bit. Timer 4 can't use the external EC3 clock.

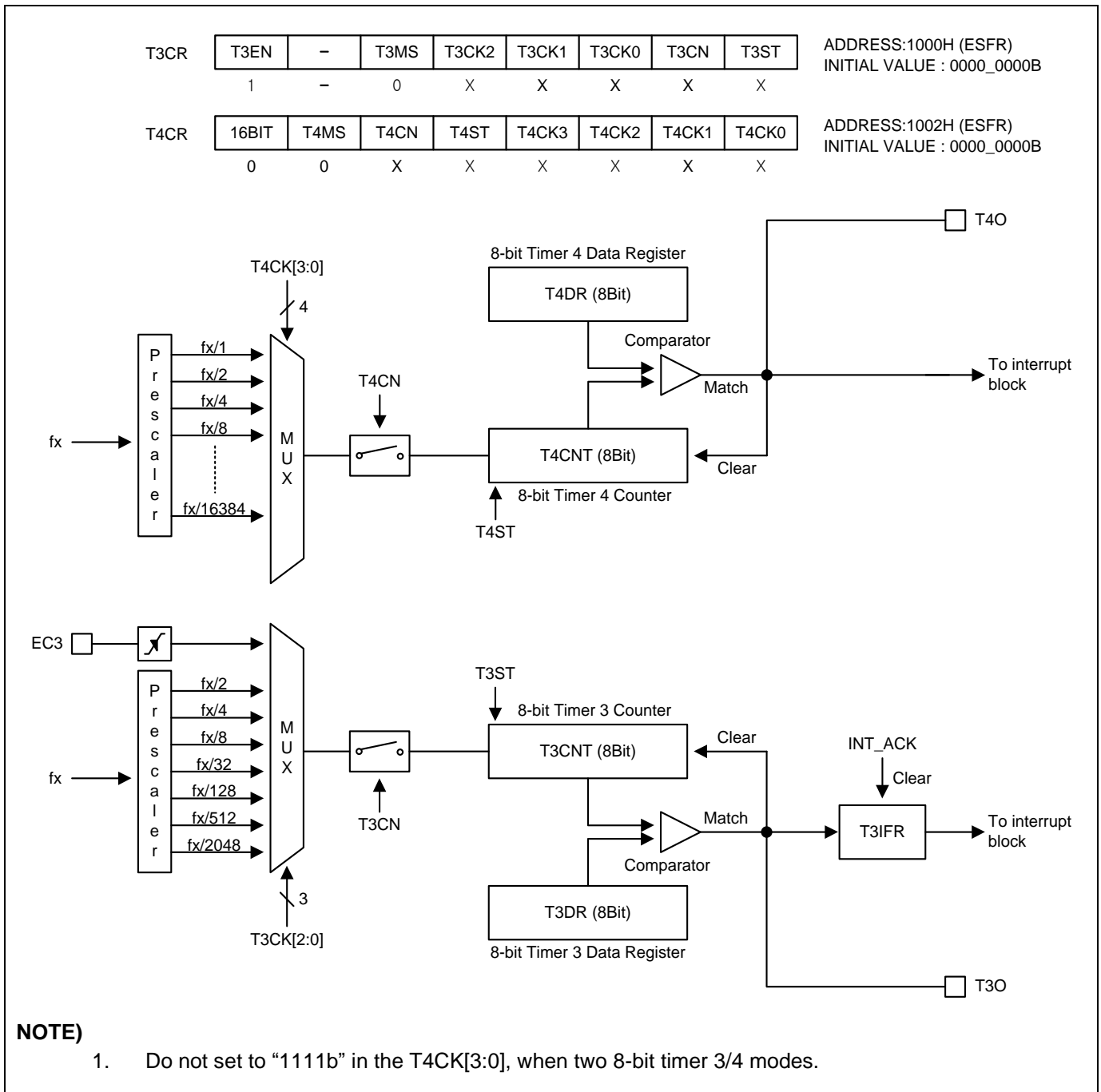


Figure 11.30 8-bit Timer/Counter Mode for Timer 3, 4



### 11.8.3 16-bit Timer/Counter 3 Mode

The 16-bit timer/counter mode is selected by control register as shown in Figure 11.31.

The 16-bit timer has counter and data register. The counter register is increased by internal or external clock input. Timer 3 can use the input clock with one of 2, 4, 8, 32, 128, 512 and 2048 prescaler division rates (T3CK[2:0]).

A 16-bit timer/counter register T3CNT, T4CNT are incremented from 0000H to FFFFH until it matches T3DR, T4DR and then cleared to 0000H. The match signal output generates the Timer 3 Interrupt (No timer 4 interrupt). The clock source is selected from T3CK[2:0] and 16BIT bit must be set to '1'. Timer 3 is LSB 8-bit, the timer 4 is MSB 8-bit.

The external clock (EC3) counts up the timer at the rising edge. If the EC3 is selected as a clock source by T3CK[2:0], EC3 port should be set to the input port by P00IO bit.

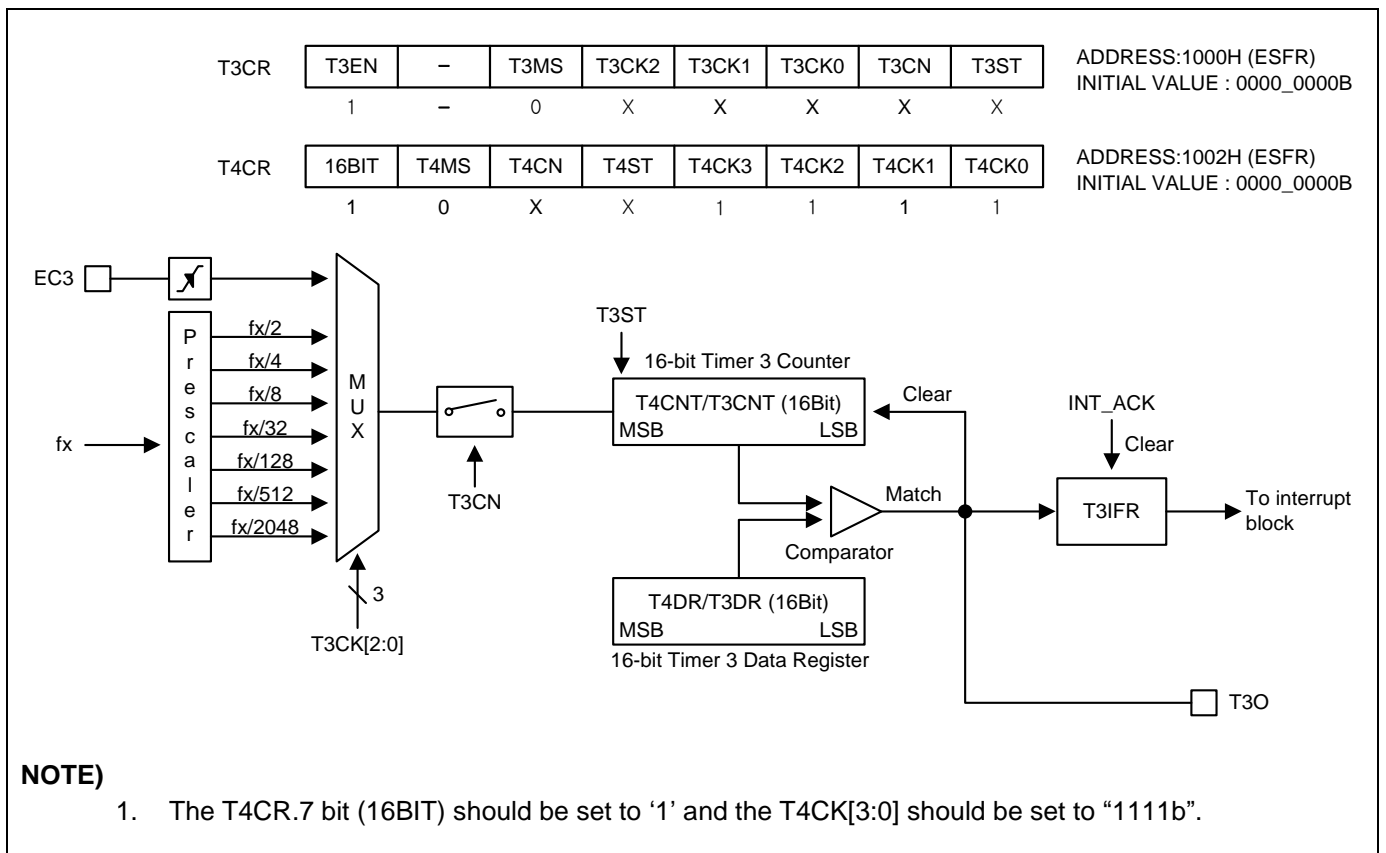


Figure 11.31 16-bit Timer/Counter Mode for Timer 3

#### 11.8.4 8-bit Timer 3, 4 Capture Mode

The 8-bit Capture 3 and 4 mode is selected by control register as shown in Figure 11.32.

The timer 3, 4 capture mode is set by T3MS, T4MS as '1'. The clock source can use the internal/external clock. Basically, it has the same function as the 8-bit timer/counter mode and the interrupt occurs when T3CNT, T4CNT is equal to T3DR, T4DR. The T3CNT, T4CNT value is automatically cleared by match signal.

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

The capture result is loaded into T3CAPR, T4CAPR. In the timer 3, 4 capture mode, timer 3, 4 output (T3O, T4O) waveform is not available.

According to the EIPOL0L register setting, the external interrupt EINT0 and EINT1 function is chose. Of course, the EINT0 and EINT1 pins must be set to an input port.

The T3CAPR and T3DR are in the same address. In the capture mode, reading operation reads T3CAPR, not T3DR and writing operation will update T3DR. The T4CAPR has the same function.

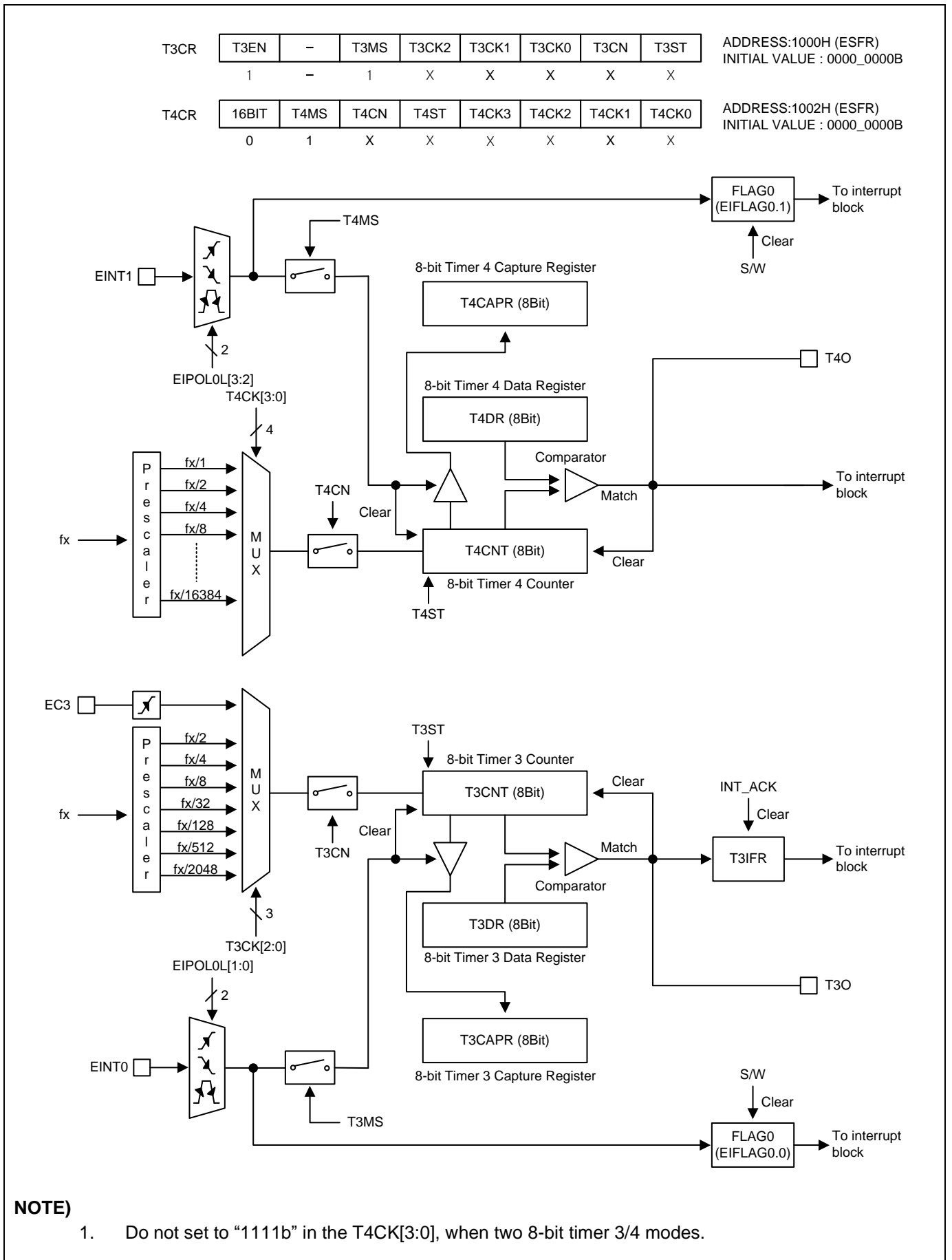


Figure 11.32 8-bit Capture Mode for Timer 3, 4

### 11.8.5 16-bit Timer 3 Capture Mode

The 16-bit Capture mode is selected by control register as shown in Figure 11.33.

The 16-bit capture mode is the same operation as 8-bit capture mode, except that the timer register uses 16 bits. The 16-bit timer 3 capture mode is set by T3MS, T4MS as '1'. The clock source is selected from T3CK[2:0] and 16BIT bit must be set to '1'. Timer 3 is LSB 8-bit, the timer 4 is MSB 8-bit.

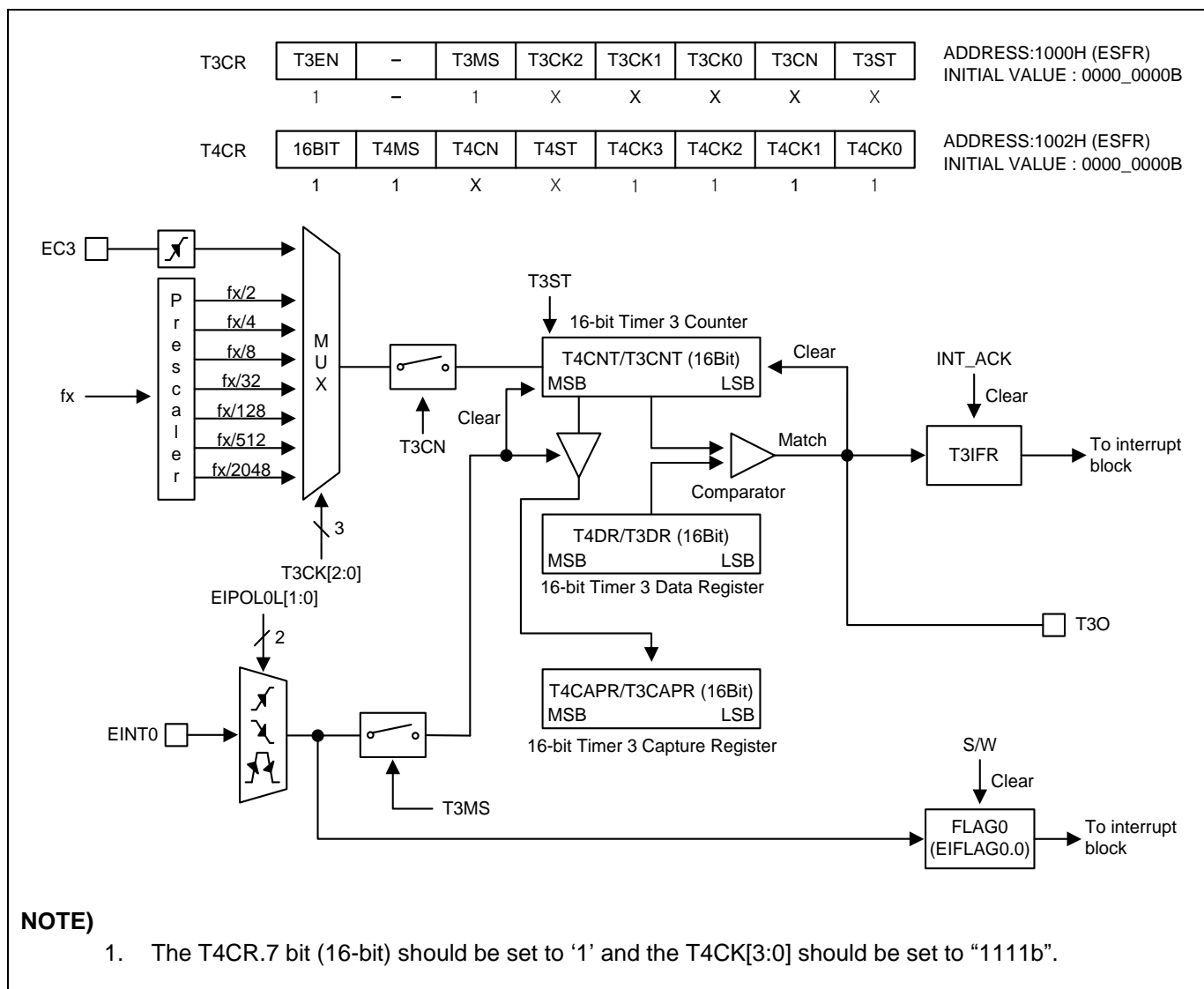


Figure 11.33 16-bit Capture Mode for Timer 3

### 11.8.6 10-bit Timer 4 PWM Mode

The timer 4 has a high speed PWM (Pulse Width Modulation) function. In PWM mode, the 6-channel pins output up to 10-bit resolution PWM output. This pin should be configured as a PWM output by set PWM4E to '1'. When the value of 2-bit +T4CNT and T4PPRH/L are identical in timer 4, a period match signal is generated and the interrupt of timer 4 occurs. In 10-bit PWM mode, A, B, C, bottom(underflow) match signal are generated when the 10-bit counter value are identical to the value of T4xDRH/L. The period of the PWM output is determined by the T4PPRH/L (PWM period register), T4xDRH/L (each channel PWM duty register).

PWM Period= [T4PPRH/T4PPRL ] X Source Clock

PWM Duty(A-ch) = [ T4ADRH/T4ADRL ] X Source Clock

Resolution	Frequency		
	T4CK[3:0]=0001 (250ns)	T4CK[3:0]=0010 (500ns)	T4CK[3:0]=0100 (2us)
10-bit	3.9kHz	1.95kHz	0.49kHz
9-bit	7.8kHz	3.9kHz	0.98kHz
8-bit	15.6kHz	7.8kHz	1.95kHz
7-bit	31.2kHz	15.6kHz	3.91kHz

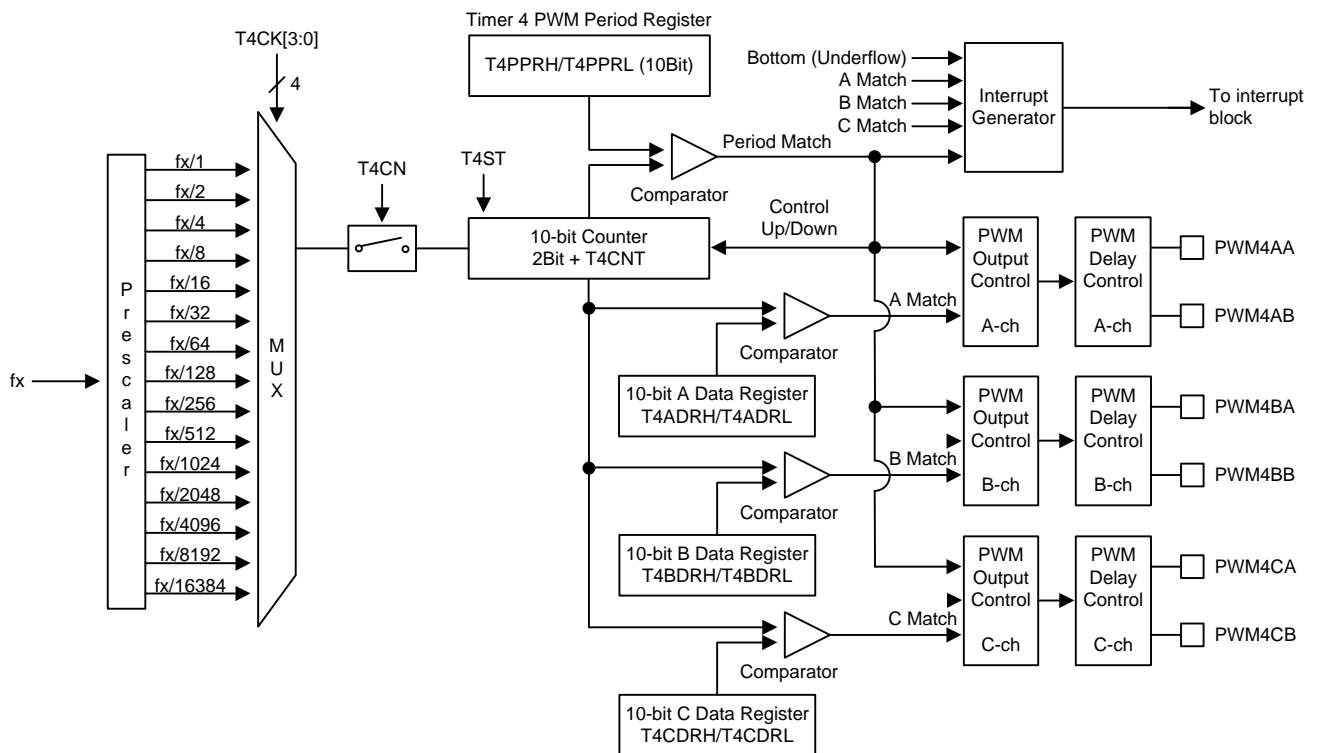
**Table 11.12** PWM Frequency vs. Resolution at 8MHz

The POLxA bit of T4PCR3 register decides the polarity of duty cycle. If the duty value is set same to the period value, the PWM output is determined by the bit POLxA (1: High, 0: Low). And if the duty value is set to "00H", the PWM output is determined by the bit POLxA (1: Low, 0: High).

PHLT:PxxOE	POLxA	POLBO	POLxB	PWM4xA Pin Output	PWM4xB Pin Output	
0x, x0, 00	0	0	0	Low-level	Low-level	
			1	Low-level	High-level	
		1	x	Low-level	Low-level	
	1	0	0	0	High-level	High-level
				1	High-level	Low-level
		1	x	High-level	High-level	
11	0	x	0	Positive-phase	Positive-Phase	
			1	Positive-phase	Negative-Phase	
	1	x	0	Negative-Phase	Negative-Phase	
			1	Negative-Phase	Positive-phase	

**Table 11.13** PWM Channel Polarity

T4CR	16BIT	T4MS	T4CN	T4ST	T4CK3	T4CK2	T4CK1	T4CK0	ADDRESS:1002H (ESFR) INITIAL VALUE : 0000_0000B
	0	X	X	X	X	X	X	X	
T4PCR1	PWM4E	ESYNC	BMOD	PHLT	UPDT	UALL	NOPS1	NOPS0	ADDRESS:1003H (ESFR) INITIAL VALUE : 0000_0000B
	1	X	X	X	X	X	X	X	
T4PCR2	FORCA	-	PAAOE	PABOE	PBAOE	PBBOE	PCAOE	PCBOE	ADDRESS:1004H (ESFR) INITIAL VALUE : 0000_0000B
	0	-	X	X	X	X	X	X	
T4PCR3	HZCLR	POLBO	POLAA	POLAB	POLBA	POLBB	POLCA	POLCB	ADDRESS:1005H (ESFR) INITIAL VALUE : 0000_0000B
	X	X	X	X	X	X	X	X	

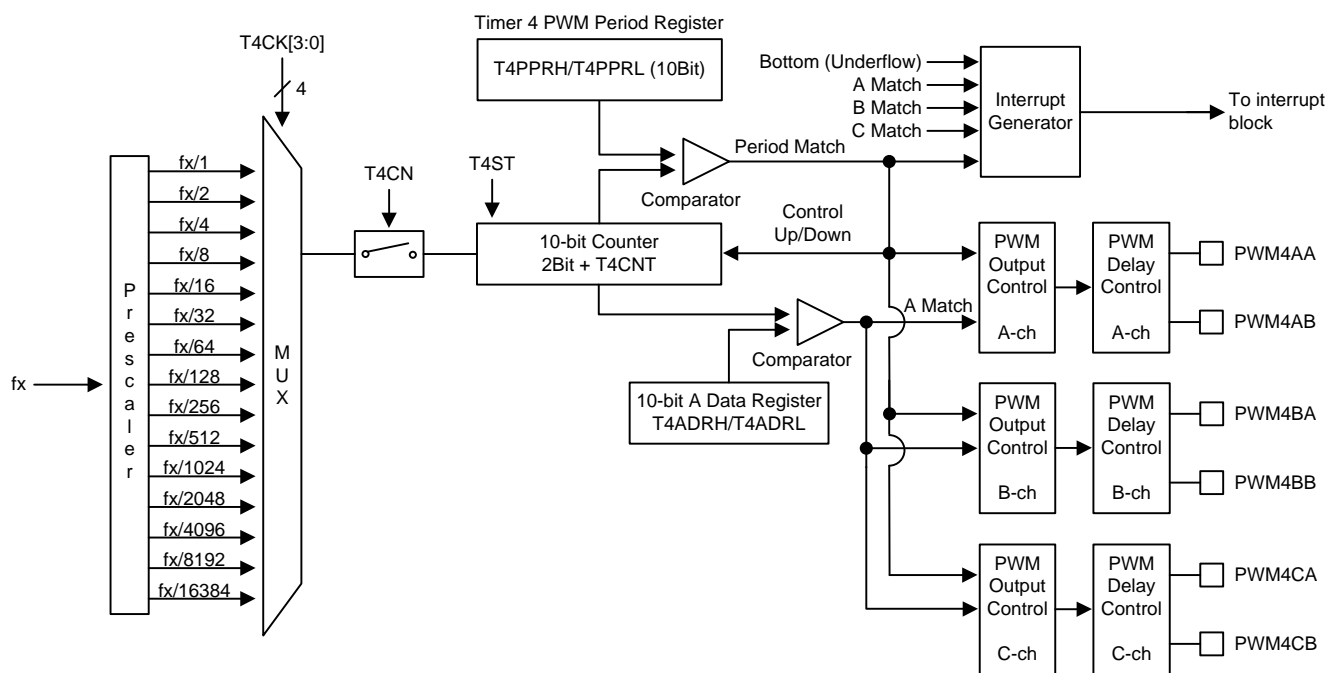


**NOTE)**

1. Do not set to "1111b" in the T4CK[3:0], when two 8-bit timer 3/4 modes.

**Figure 11.34** 10-bit PWMMode (Force 6-ch)

T4CR	16BIT	T4MS	T4CN	T4ST	T4CK3	T4CK2	T4CK1	T4CK0	ADDRESS:1002H (ESFR) INITIAL VALUE : 0000_0000B
	0	X	X	X	X	X	X	X	
T4PCR1	PWM4E	ESYNC	BMOD	PHLT	UPDT	UALL	NOPS1	NOPS0	ADDRESS:1003H (ESFR) INITIAL VALUE : 0000_0000B
	1	X	X	X	X	X	X	X	
T4PCR2	FORCA	-	PAAOE	PABOE	PBAOE	PBBOE	PCAOE	PCBOE	ADDRESS:1004H (ESFR) INITIAL VALUE : 0000_0000B
	1	-	X	X	X	X	X	X	
T4PCR3	HZCLR	POLBO	POLAA	POLAB	POLBA	POLBB	POLCA	POLCB	ADDRESS:1005H (ESFR) INITIAL VALUE : 0000_0000B
	X	X	X	X	X	X	X	X	



**NOTE)**

1. Do not set to "1111b" in the T4CK[3:0], when two 8-bit timer 3/4 modes.

Figure 11.35 10-bit PWM Mode (Force All-ch)

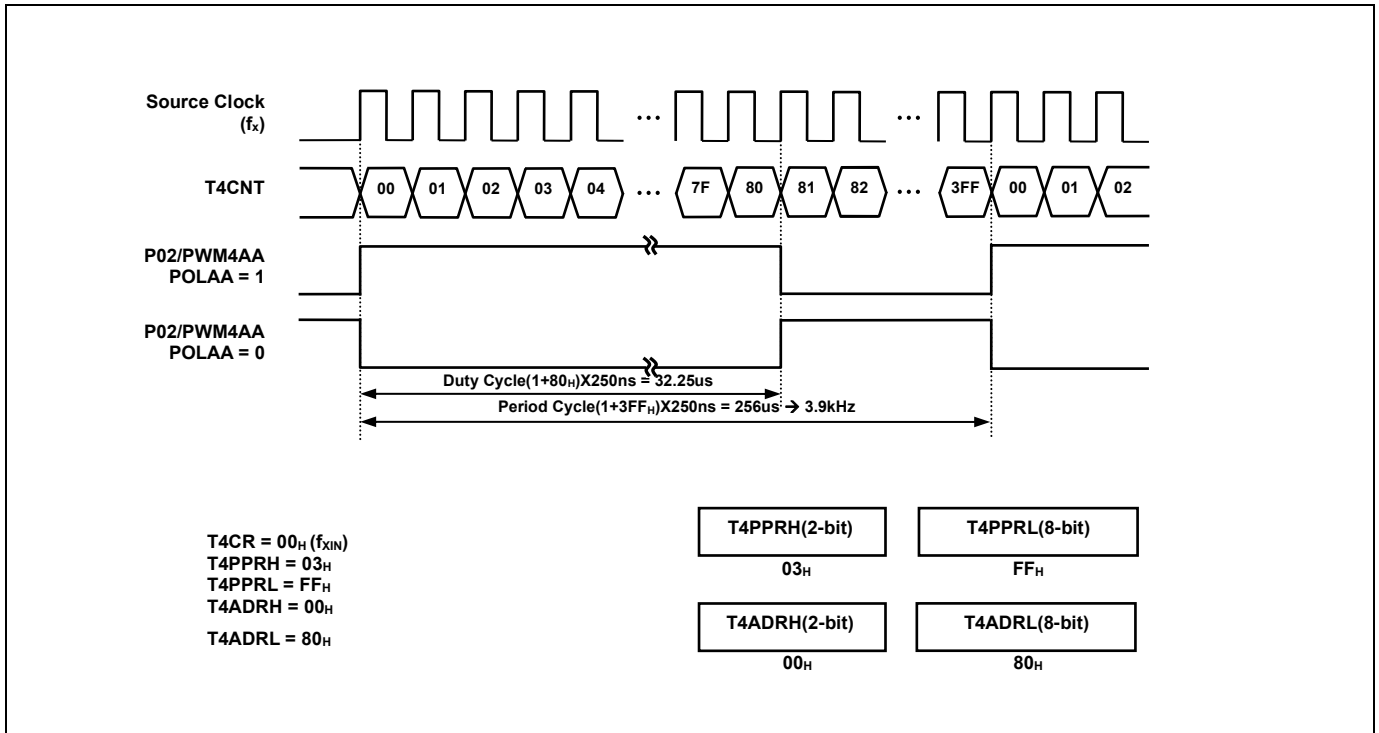


Figure 11.36 Example of PWM at 4 MHz

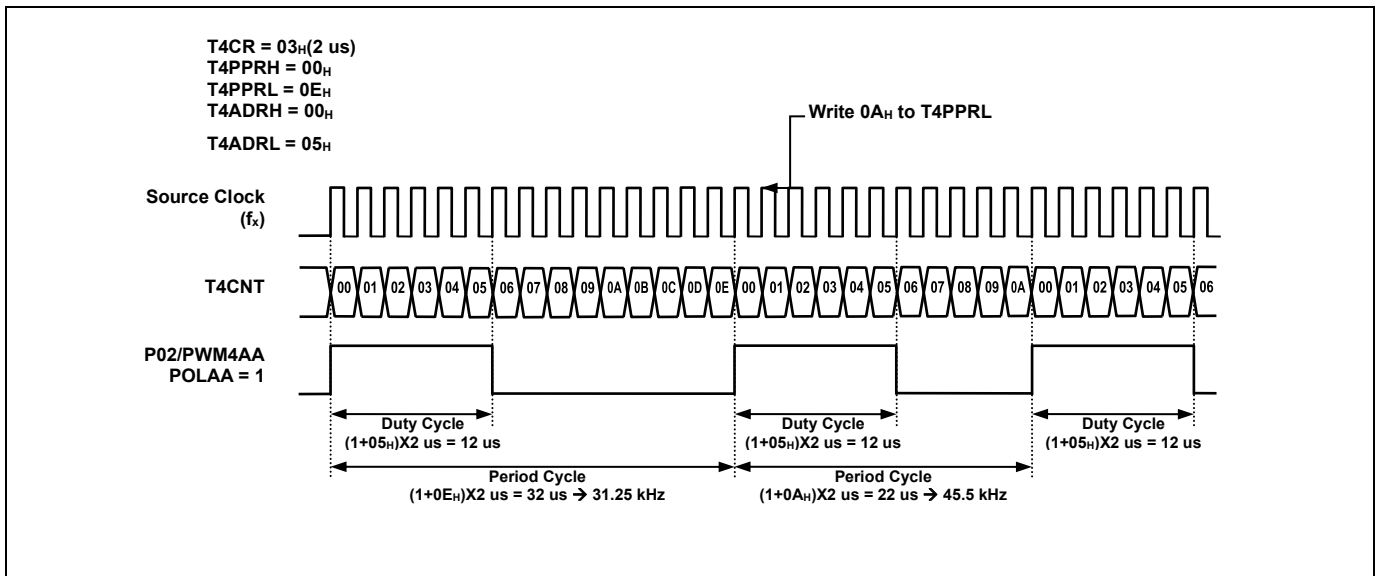


Figure 11.37 Example of Changing the Period in Absolute Duty Cycle at 4 MHz

**Update period & duty register value at once**

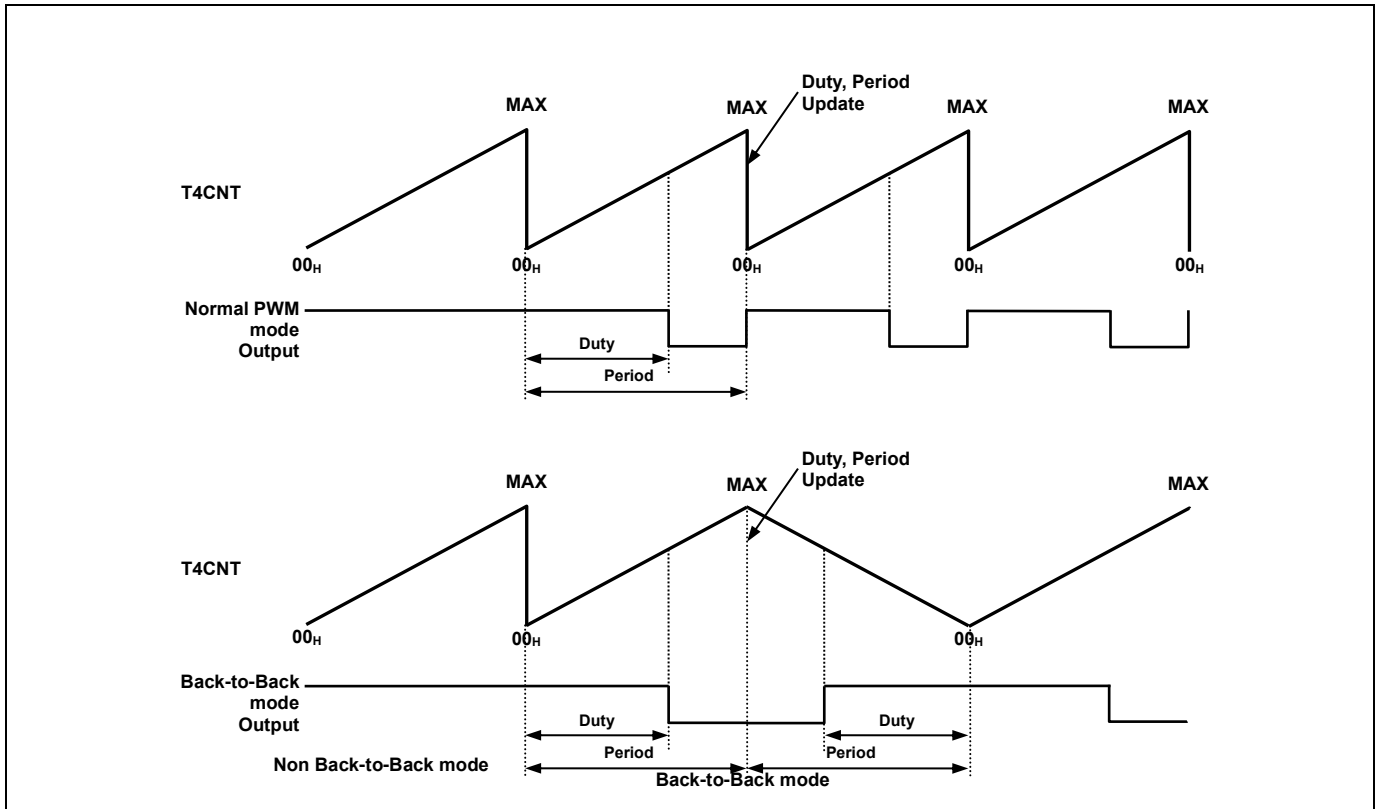
The period and duty of PWM comes to move from temporary registers to T4PPRH/L (PWM Period Register) and T4ADRH/L/T4BDRH/L/T4CDRH/L (PWM Duty Register) when always period match occurs. If you want that the period and duty is immediately changed, the UPDT bit in the T4PCR1 register must set to '1'. It should be noted that it needs the 3 cycle of timer clock for data transfer in the internal clock synchronization circuit. So the update data is written before 3 cycle of timer clock to get the right output waveform.



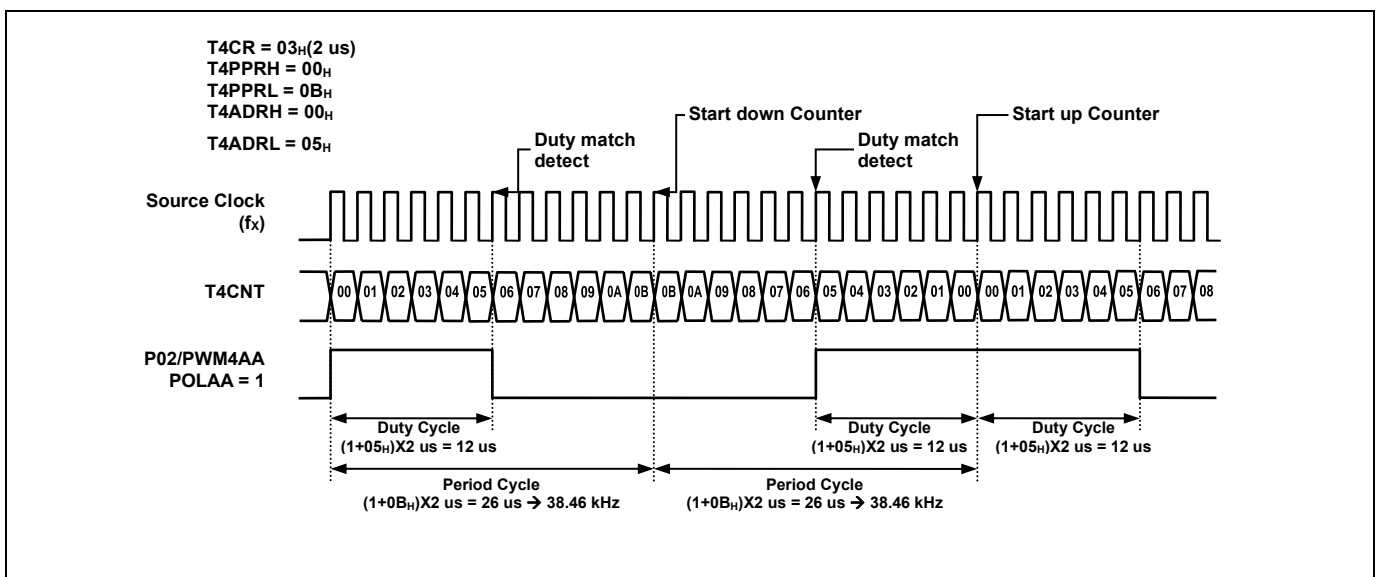
**Phase correction & Frequency correction**

On operating PWM, the phase and the frequency can be changed by using BMOD bit (back-to-back mode) in T4PCR1 register. (Figure 1.38, Figure 11.39, Figure 11.40 referred)

In the back-to-back mode, the counter of PWM repeats up/down count. In fact, the effective duty and period becomes twofold of the register set values. (Figure 1.38, Figure 11.39 referred)



**Figure 11.38** Example of PWM Output Waveform



**Figure 11.39** Example of PWM waveform in Back-to-Back mode at 4 MHz

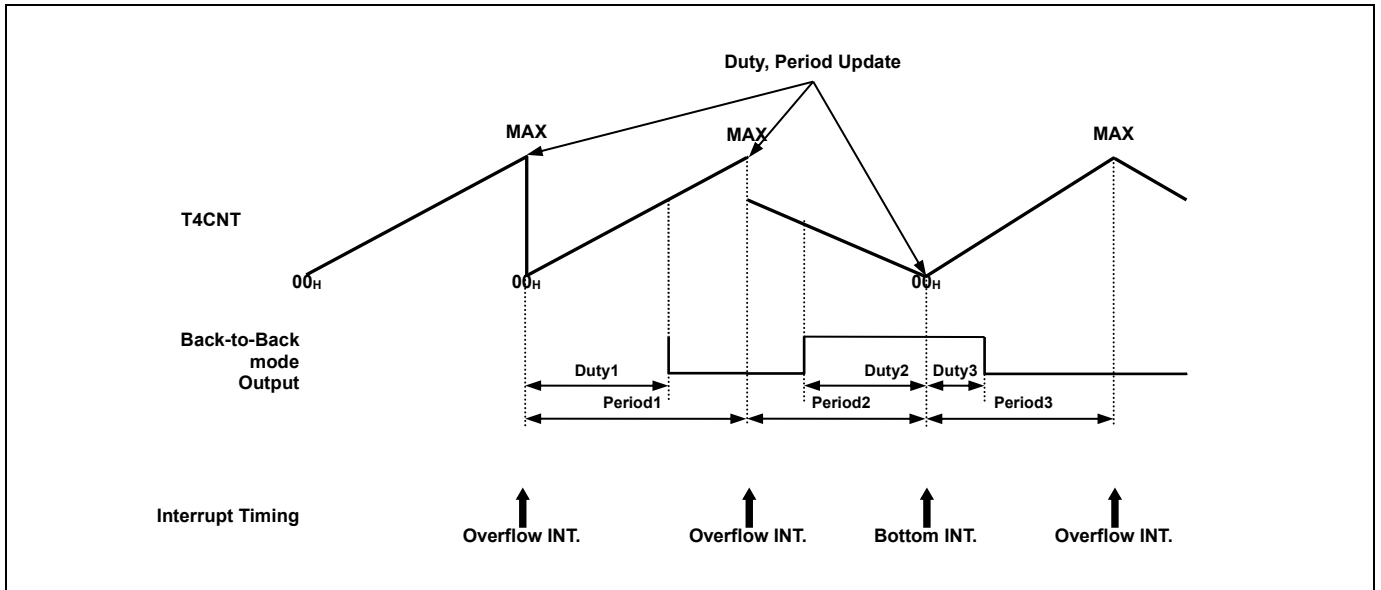


Figure 11.40 Example of Phase Correction and Frequency correction of PWM

**External Sync**

If using ESYNC bit of T4PCR1 register, it is possible to synchronize the output of PWM from external signal. If ESYNC bit sets to '1', the external signal moves to PWM module through the BLNK pin. If BLNK signal is low, immediately PWM output becomes a reset value and internal counter becomes reset. If BLNK signal returns to '1', the counter is started again and PWM output is normally generated. (Figure 11.41 referred)

**PWM Halt**

If using PHLT bit of T4PCR1 register, it is possible to stop PWM operation by the software. During PHLT bit being '1', PWM output becomes a reset value and internal counter becomes reset as 0. Without changing PWM setting, it can temporarily stop PWM. In case of T4CNT, when stopping counter, PWM output pin remains before states. But if PHLT bit sets to '1', PWM output pin has reset value.

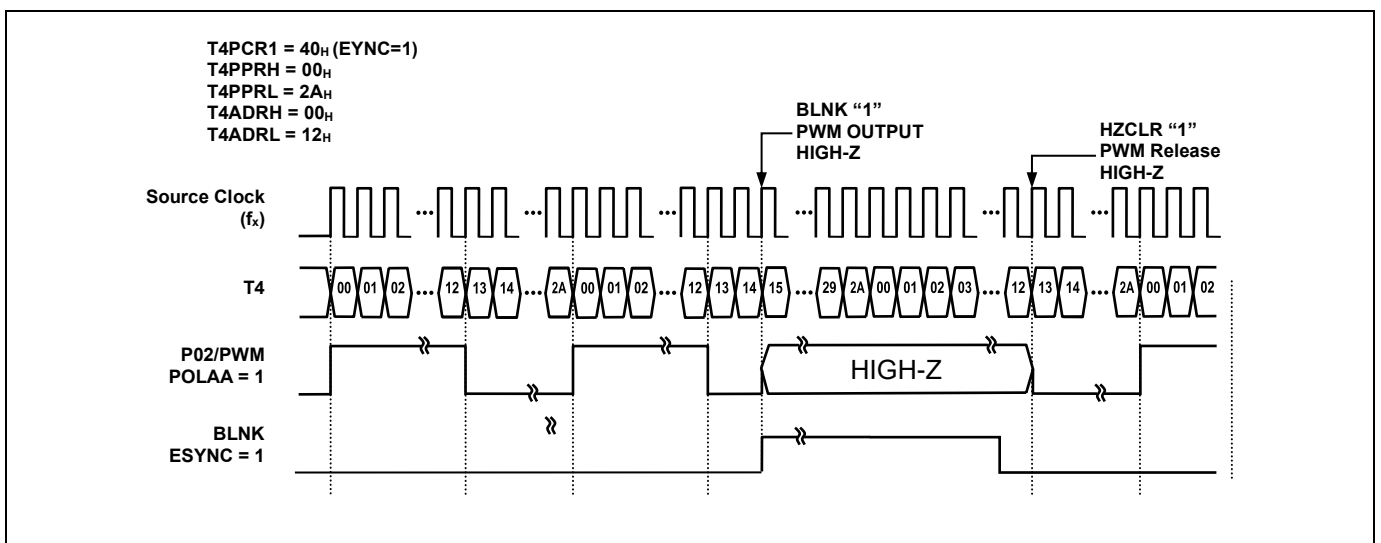
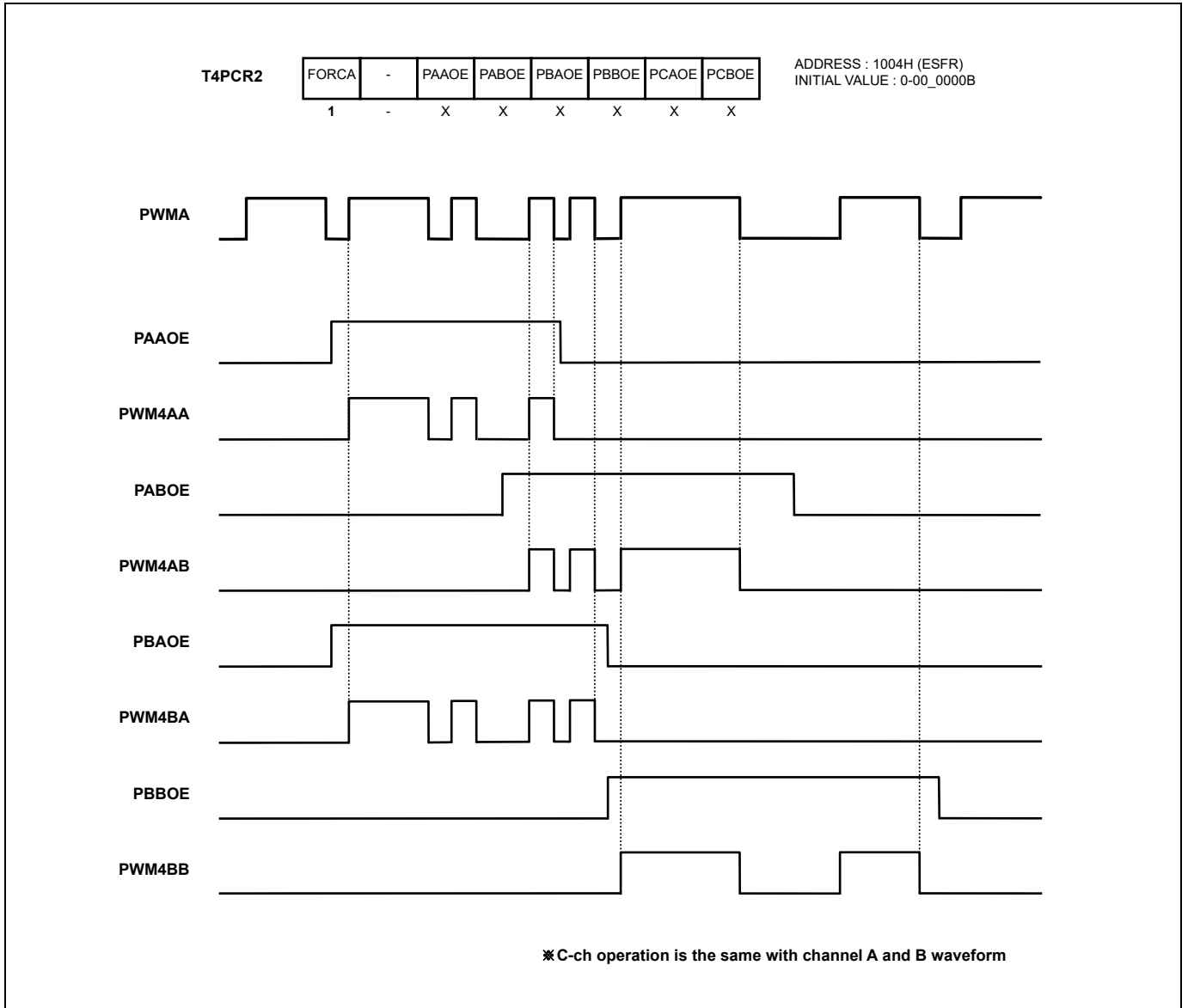


Figure 11.41 Example of PWM External Synchronization with BLNK Input

**FORCE Drive ALL Channel with A-ch mode**

If FORCA bit sets to '1', it is possible to enable or disable all PWM output pins through PWM outputs which occur from A-ch duty counter. It is noted that the inversion outputs of A, B, C channel have the same A-ch output waveform. According to POLAA/BB/CC, it is able to control the inversion of outputs.



**Figure 11.42** Example of Force Drive All Channel with A-ch

**FORCE 6-Ch Drive**

If FORCA bit sets to '0', it is possible to enable or disable PWM output pin and inversion output pin generated through the duty counter of each channel. The inversion output is the reverse phase of the PWM output. A AA/AB output of the A-channel duty register, a BA/BB output of the B-channel duty register, a CA/CB output of the C-channel duty register are controlled respectively. If the UALL bit is set to '1', it is updated B/C channel duty at the same time, when it is written by a A-channel duty register.

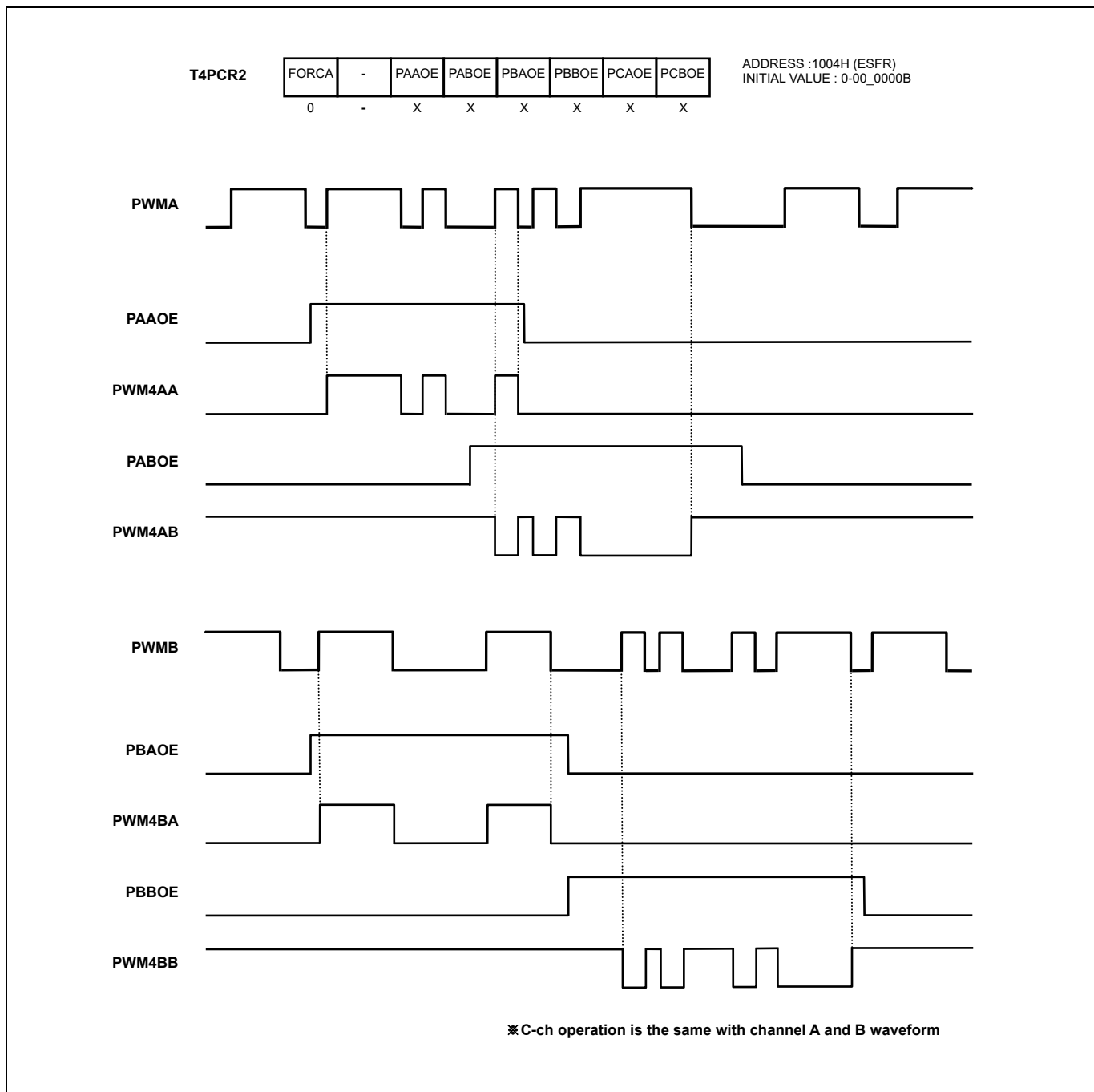


Figure 11.43 Example of Force Drive 6-ch Mode

**PWM output Delay**

If using the T4DLYA, T4DLYB and T4DLYC register, it can delay PWM output based on the rising edge. At that time, it does not change the falling edge, so the duty is reduced as the time delay. In POLAA/BA/CA setting to '0', the delay is applied to the falling edge. In POLAA/BA/CA setting to '1', the delay is applied to the rising edge. It can produce a pair of Non-overlapping clock. The each channel is able to have 4-bit delay. As it can select the clock up to 1/8 divided clock using NOPS[1:0] the delay of its maximum 128 timer clock cycle is produced.

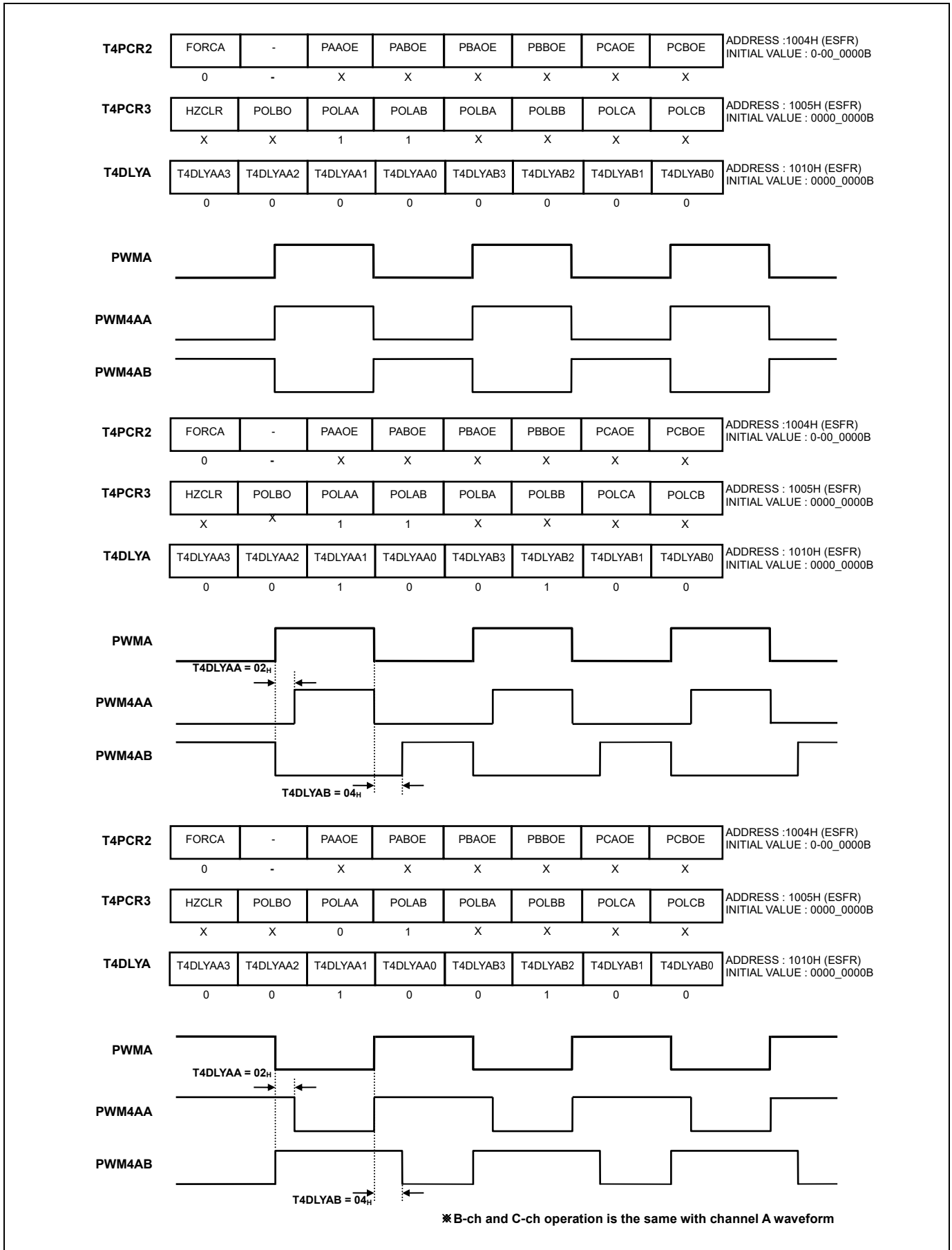


Figure 11.44 Example of PWM Delay

11.8.7 Block Diagram

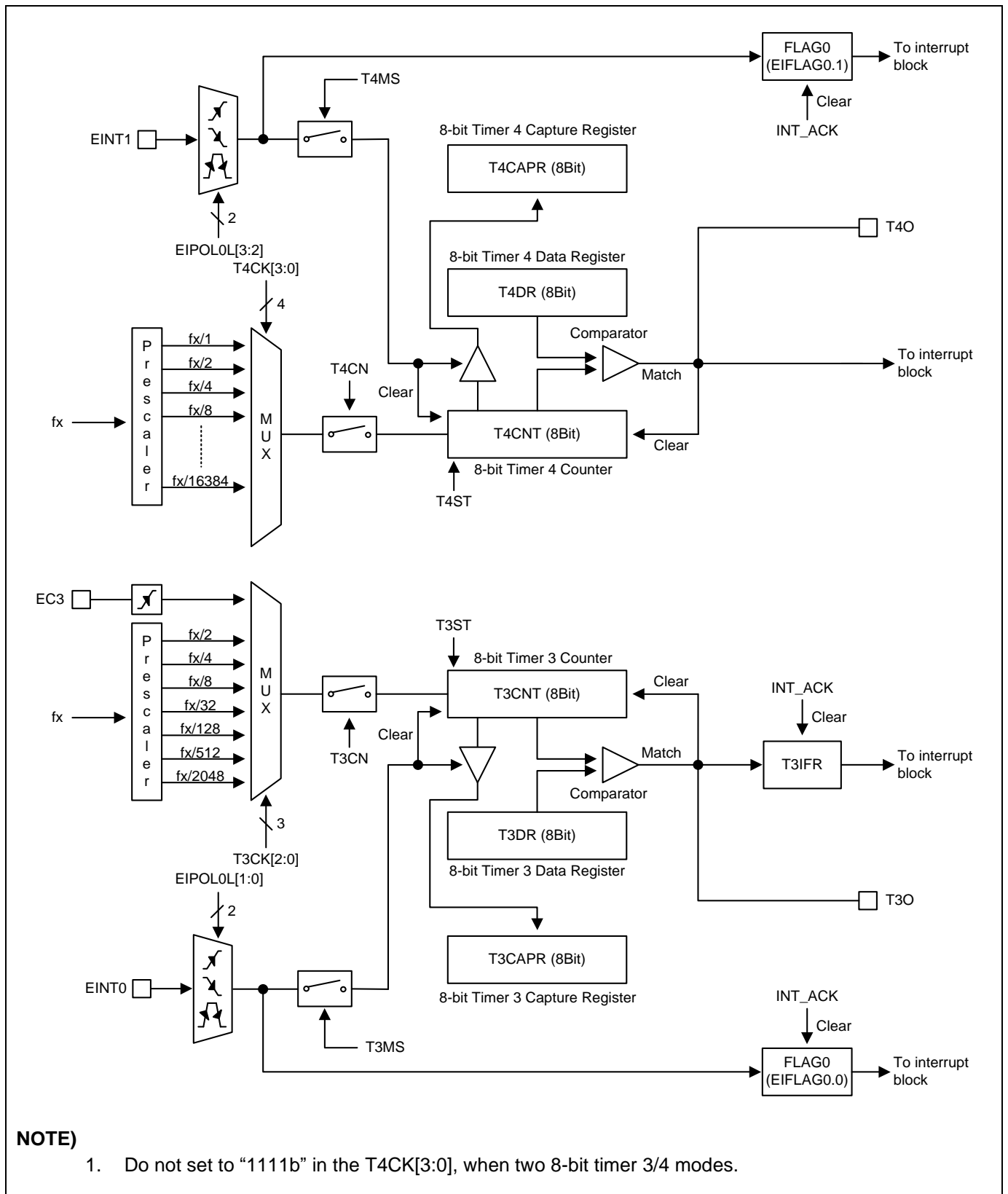


Figure 11.45 Two 8-bit Timer 3, 4 Block Diagram

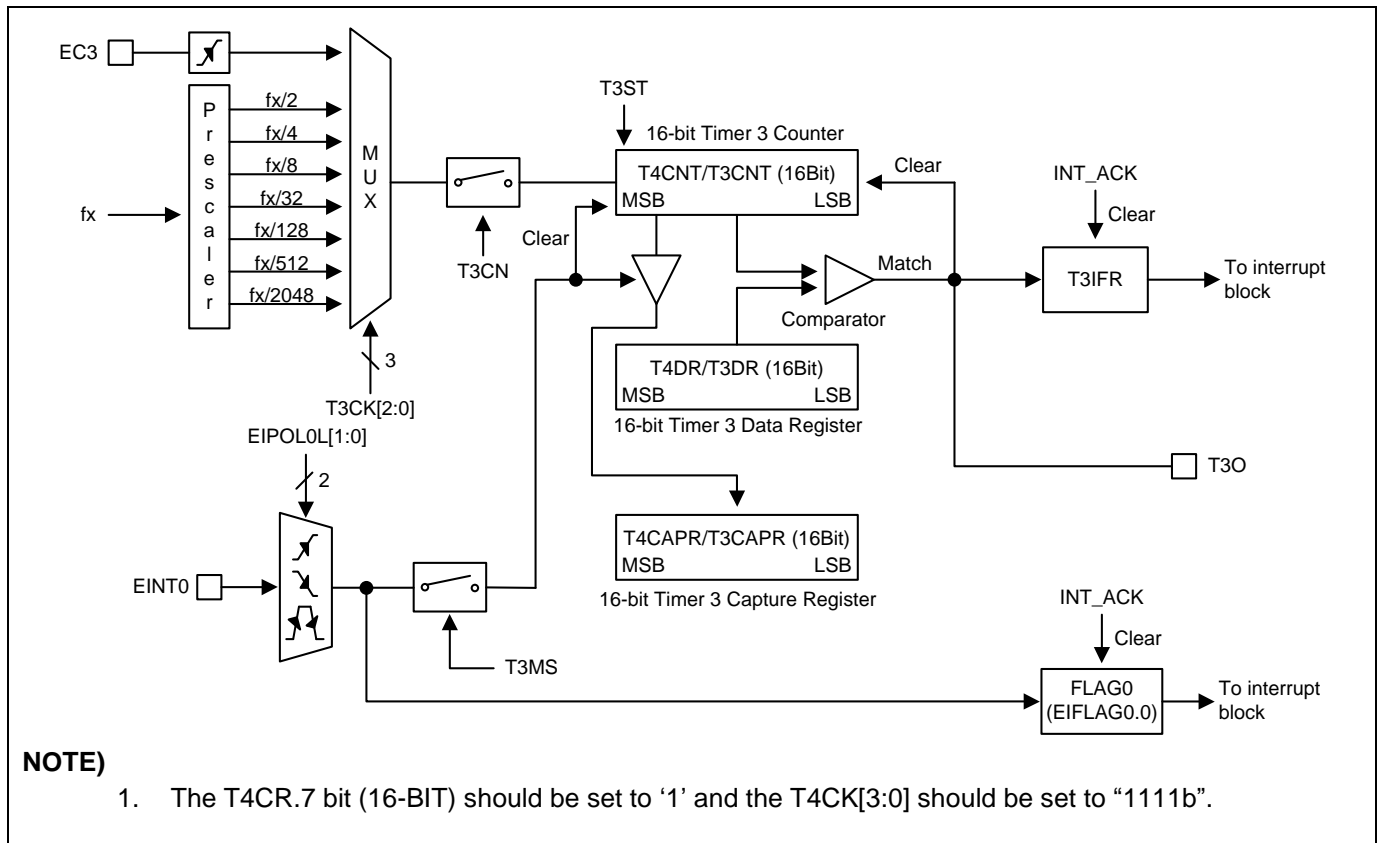


Figure 11.46 16-bit Timer 3 Block Diagram

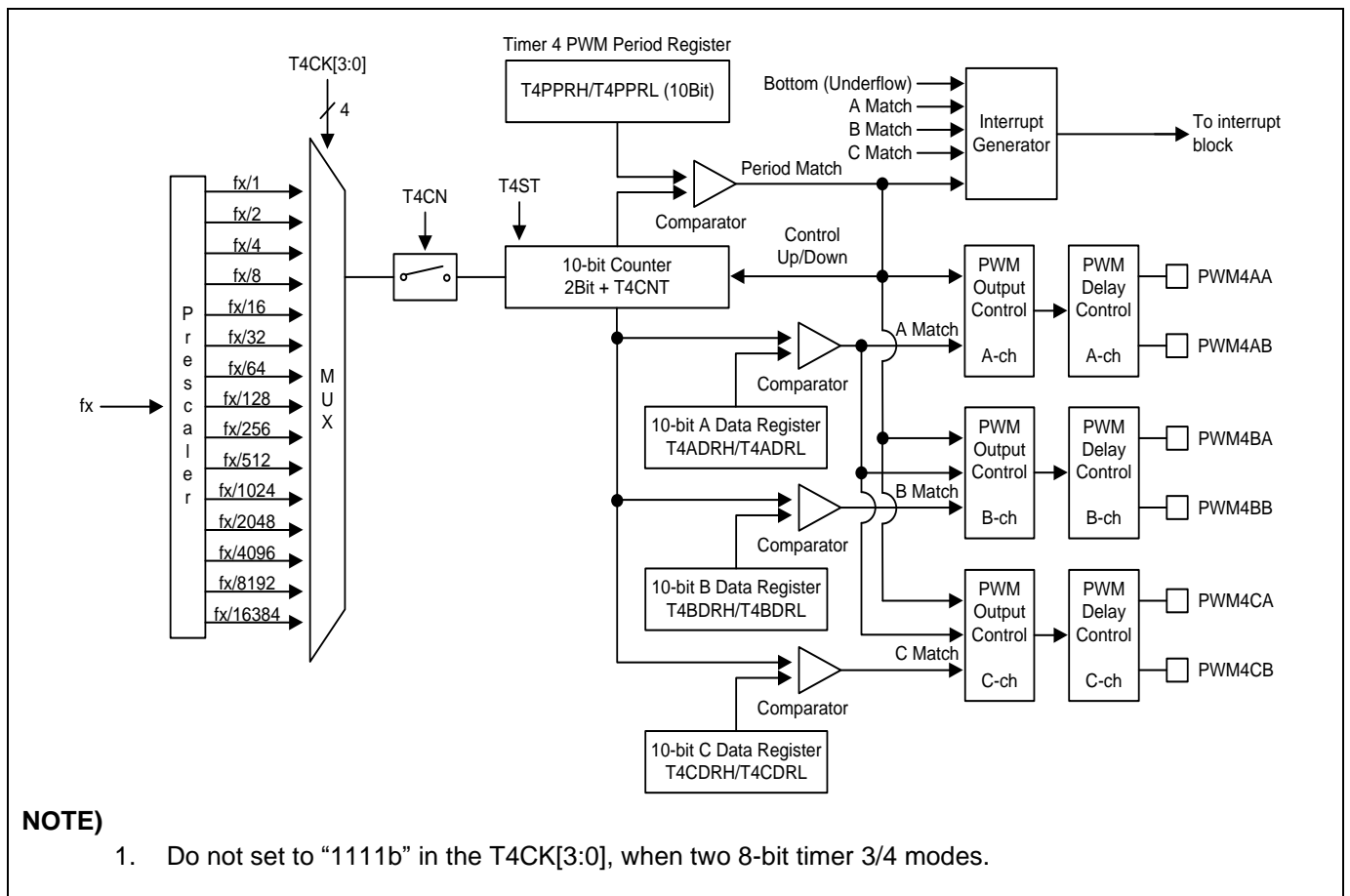


Figure 11.47 10-bit PWM Timer 4 Block Diagram



## 11.8.8 Register Map

Name	Address	Direction	Default	Description
T3CNT	1001H (ESFR)	R	00H	Timer 3 Counter Register
T3DR	1001H (ESFR)	W	FFH	Timer 3 Data Register
T3CAPR	1001H (ESFR)	R	00H	Timer 3 Capture Data Register
T3CR	1000H (ESFR)	R/W	00H	Timer 3 Control Register
T4PPRH	1009H (ESFR)	R/W	00H	Timer 4 PWM Period High Register
T4PPRL	1008H (ESFR)	R/W	FFH	Timer 4 PWM Period Low Register
T4ADRH	100BH (ESFR)	R/W	00H	Timer 4 PWM A Duty High Register
T4ADRL	100AH (ESFR)	R/W	7FH	Timer 4 PWM A Duty Low Register
T4BDRH	100DH (ESFR)	R/W	00H	Timer 4 PWM B Duty High Register
T4BDRL	100CH (ESFR)	R/W	7FH	Timer 4 PWM B Duty Low Register
T4CDRH	100FH (ESFR)	R/W	00H	Timer 4 PWM C Duty High Register
T4CDRL	100EH (ESFR)	R/W	7FH	Timer 4 PWM C Duty Low Register
T4DLYA	1010H (ESFR)	R/W	00H	Timer 4 PWM A Delay Register
T4DLYB	1011H (ESFR)	R/W	00H	Timer 4 PWM B Delay Register
T4DLYC	1012H (ESFR)	R/W	00H	Timer 4 PWM C Delay Register
T4DR	1013H (ESFR)	R/W	FFH	Timer 4 Data Register
T4CAPR	1014H (ESFR)	R	00H	Timer 4 Capture Data Register
T4CNT	1015H (ESFR)	R	00H	Timer 4 Counter Register
T4CR	1002H (ESFR)	R/W	00H	Timer 4 Control Register
T4PCR1	1003H (ESFR)	R/W	00H	Timer 4 PWM Control Register 1
T4PCR2	1004H (ESFR)	R/W	00H	Timer 4 PWM Control Register 2
T4PCR3	1005H (ESFR)	R/W	00H	Timer 4 PWM Control Register 3
T4ISR	1006H (ESFR)	R/W	00H	Timer 4 Interrupt Status Register
T4MSK	1007H (ESFR)	R/W	00H	Timer 4 Interrupt Mask Register

Table 11.14 Timer 3, 4 Register Map

### 11.8.9 Timer/Counter 3 Register Description

The timer/counter 3 register consists of timer 3 counter register (T3CNT), timer 3 data register (T3DR), timer 3 capture data register (T3CAPR) and timer 3 control register (T3CR).

#### 11.8.10 Register Description for Timer/Counter 3

##### T3CNT (Timer 3 Counter Register: Read Case, Timer mode only): 1001H (ESFR)

7	6	5	4	3	2	1	0
T3CNT7	T3CNT6	T3CNT5	T3CNT4	T3CNT3	T3CNT2	T3CNT1	T3CNT0
R	R	R	R	R	R	R	R

Initial value: 00H

T3CNT[7:0] T3 Counter

##### T3DR (Timer 3 Data Register: Write Case): 1001H (ESFR)

7	6	5	4	3	2	1	0
T3DR7	T3DR6	T3DR5	T3DR4	T3DR3	T3DR2	T3DR1	T3DR0
W	W	W	W	W	W	W	W

Initial value: FFH

T3DR[7:0] T3 Data

##### T3CAPR (Timer 3 Capture Data Register: Read Case, Capture mode only): 1001H (ESFR)

7	6	5	4	3	2	1	0
T3CAPR7	T3CAPR6	T3CAPR5	T3CAPR4	T3CAPR3	T3CAPR2	T3CAPR1	T3CAPR0
R	R	R	R	R	R	R	R

Initial value: 00H

T3CAPR[7:0] T3 Capture Data

**T3CR (Timer 3 Control Register): 1000H (ESFR)**

7	6	5	4	3	2	1	0
T3EN	–	T3MS	T3CK2	T3CK1	T3CK0	T3CN	T3ST
RW	–	RW	RW	RW	RW	RW	RW

Initial value: 00H

<b>T3EN</b>	Control Timer 3			
	0	Timer 3 disable		
	1	Timer 3 enable		
<b>T3MS</b>	Control Timer 3 Operation Mode			
	0	Timer/counter mode (T3O: toggle at match)		
	1	Capture mode (the match interrupt can occur)		
<b>T3CK[2:0]</b>	Select Timer 3 clock source. fx is main system clock frequency			
	T3CK2	T3CK1	T3CK0	Description
	0	0	0	fx/2
	0	0	1	fx/4
	0	1	0	fx/8
	0	1	1	fx/32
	1	0	0	fx/128
	1	0	1	fx/512
	1	1	0	fx/2048
	1	1	1	External Clock (EC3)
<b>T3CN</b>	Control Timer 3 Count Pause/Continue			
	0	Temporary count stop		
	1	Continue count		
<b>T3ST</b>	Control Timer 3 Start/Stop			
	0	Counter stop		
	1	Clear counter and start		

**NOTE)**

1. Refer to the external interrupt flag 1 register (EIFLAG1) for the T3 interrupt flag.

### 11.8.11 Timer/Counter 4 Register Description

The timer/counter 4 register consists of timer 4 PWM period high/low register (T4PPRH/L), timer 4 PWM A duty high/low register (T4ADRH/L), timer 4 PWM B duty high/low register (T4BDRH/L), timer 4 PWM C duty high/low register (T4CDRH/L), timer 4 PWM A delay register (T4DLYA), timer 4 PWM B delay register (T4DLYB), timer 4 PWM C delay register (T4DLYC), timer 4 data register (T4DR), timer 4 capture data register (T4CAPR), timer 4 counter register (T4CNT), timer 4 control register (T4CR), timer 4 PWM control register 1 (T4PCR1), timer 4 PWM control register 2 (T4PCR2), timer 4 PWM control register 3 (T4PCR3), timer 4 interrupt status register (T4ISR) and timer 4 interrupt mask register (T4MSK).

### 11.8.12 Register Description for Timer/Counter 4

#### T4PPRH (Timer 4 PWM Period High Register: 6-ch PWM mode only): 1009H (ESFR)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	T4PPRH1	T4PPRH0
–	–	–	–	–	–	RW	RW

Initial value: 00H

**T4PPRH[1:0]** T4 PWM Period Data High Byte

#### T4PPRL (Timer 4 PWM Period Low Register: 6-ch PWM mode only): 1008H (ESFR)

7	6	5	4	3	2	1	0
T4PPRL7	T4PPRL6	T4PPRL5	T4PPRL4	T4PPRL3	T4PPRL2	T4PPRL1	T4PPRL0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: FFH

**T4PPRL[7:0]** T4 PWM Period Data Low Byte

#### T4ADRH (Timer 4 PWM A Duty High Register: 6-ch PWM mode only): 100BH (ESFR)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	T4ADRH1	T4ADRH0
–	–	–	–	–	–	RW	RW

Initial value: 00H

**T4ADRH[1:0]** T4 PWM A Duty Data High Byte

#### T4ADRL (Timer 4 PWM A Duty Low Register: 6-ch PWM mode only): 100AH (ESFR)

7	6	5	4	3	2	1	0
T4ADRL7	T4ADRL6	T4ADRL5	T4ADRL4	T4ADRL3	T4ADRL2	T4ADRL1	T4ADRL0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 7FH

**T4ADRL[7:0]** T4 PWM A Duty Data Low Byte

**T4BDRH (Timer 4 PWM B Duty High Register: 6-ch PWM mode only): 100DH (ESFR)**

7	6	5	4	3	2	1	0
–	–	–	–	–	–	T4BDRH1	T4BDRH0
–	–	–	–	–	–	RW	RW

Initial value: 00H

**T4BDRH[1:0]** T4 PWM B Duty Data High Byte**T4BDRL (Timer 4 PWM B Duty Low Register: 6-ch PWM mode only): 100CH (ESFR)**

7	6	5	4	3	2	1	0
T4BDRL7	T4BDRL6	T4BDRL5	T4BDRL4	T4BDRL3	T4BDRL2	T4BDRL1	T4BDRL0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 7FH

**T4BDRL[7:0]** T4 PWM B Duty Data Low Byte**T4CDRH (Timer 4 PWM C Duty High Register: 6-ch PWM mode only): 100FH (ESFR)**

7	6	5	4	3	2	1	0
–	–	–	–	–	–	T4CDRH1	T4CDRH0
–	–	–	–	–	–	RW	RW

Initial value: 00H

**T4CDRH[1:0]** T4 PWM C Duty Data High Byte**T4CDRL (Timer 4 PWM C Duty Low Register: 6-ch PWM mode only): 100EH (ESFR)**

7	6	5	4	3	2	1	0
T4CDRL7	T4CDRL6	T4CDRL5	T4CDRL4	T4CDRL3	T4CDRL2	T4CDRL1	T4CDRL0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 7FH

**T4CDRL[7:0]** T4 PWM C Duty Data Low Byte**T4DLYA (Timer 4 PWM A Delay Register: 6-ch PWM mode only): 1010H (ESFR)**

7	6	5	4	3	2	1	0
T4DLYAA3	T4DLYAA2	T4DLYAA1	T4DLYAA0	T4DLYAB3	T4DLYAB2	T4DLYAB1	T4DLYAB0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**T4DLYAA[3:0]** PWM4AA Delay Data (Rising edge only)**T4DLYAB[3:0]** PWM4AB Delay Data (Rising edge only)**T4DLYB (Timer 4 PWM B Delay Register: 6-ch PWM mode only): 1011H (ESFR)**

7	6	5	4	3	2	1	0
T4DLYBA3	T4DLYBA2	T4DLYBA1	T4DLYBA0	T4DLYBB3	T4DLYBB2	T4DLYBB1	T4DLYBB0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**T4DLYBA[3:0]** PWM4BA Delay Data (Rising edge only)**T4DLYBB[3:0]** PWM4BB Delay Data (Rising edge only)

**T4DLYC (Timer 4 PWM C Delay Register: 6-ch PWM mode only): 1012H (ESFR)**

7	6	5	4	3	2	1	0
T4DLYCA3	T4DLYCA2	T4DLYCA1	T4DLYCA0	T4DLYCB3	T4DLYCB2	T4DLYCB1	T4DLYCB0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**T4DLYCA[3:0]** PWM4CA Delay Data (Rising edge only)

**T4DLYCB[3:0]** PWM4CB Delay Data (Rising edge only)

**T4DR (Timer 4 Data Register: Timer and Capture mode only): 1013H (ESFR)**

7	6	5	4	3	2	1	0
T4DR7	T4DR6	T4DR5	T4DR4	T4DR3	T4DR2	T4DR1	T4DR0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: FFH

**T4DR[7:0]** T4 Data

**T4CAPR (Timer 4 Capture Data Register: Read Case, Capture mode only): 1014H (ESFR)**

7	6	5	4	3	2	1	0
T4CAPR7	T4CAPR6	T4CAPR5	T4CAPR4	T4CAPR3	T4CAPR2	T4CAPR1	T4CAPR0
R	R	R	R	R	R	R	R

Initial value: 00H

**T4CAPR[7:0]** T4 Capture Data

**T4CNT (Timer 4 Counter Register: Read Case, Timer mode only): 1015H (ESFR)**

7	6	5	4	3	2	1	0
T4CNT7	T4CNT6	T4CNT5	T4CNT4	T4CNT3	T4CNT2	T4CNT1	T4CNT0
R	R	R	R	R	R	R	R

Initial value: 00H

**T4CNT[7:0]** T4 Counter

## T4CR (Timer 4 Control Register): 1002H (ESFR)

7	6	5	4	3	2	1	0
16BIT	T4MS	T4CN	T4ST	T4CK3	T4CK2	T4CK1	T4CK0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

<b>16BIT</b>	Select Two 8-bit or 16-bit Mode for Timer 3/4				
	0	Two 8-bit Timer 3/4			
	1	16-bit Timer 3			
<b>T4MS</b>	Control Timer 4 Operation Mode				
	0	Timer/counter mode (T4O: toggle at match)			
	1	Capture mode (the match interrupt can occur)			
<b>T4CN</b>	Control Timer 4 Count Pause/Continue				
	0	Temporary count stop			
	1	Continue count			
<b>T4ST</b>	Control Timer 4 Start/Stop				
	0	Counter stop			
	1	Clear counter and start			
<b>T4CK[3:0]</b>	Select Timer 4 clock source. fx is main system clock frequency				
	T4CK3	T4CK2	T4CK1	T4CK0	Description
	0	0	0	0	fx/1
	0	0	0	1	fx/2
	0	0	1	0	fx/4
	0	0	1	1	fx/8
	0	1	0	0	fx/16
	0	1	0	1	fx/32
	0	1	1	0	fx/64
	0	1	1	1	fx/128
	1	0	0	0	fx/256
	1	0	0	1	fx/512
	1	0	1	0	fx/1024
	1	0	1	1	fx/2048
	1	1	0	0	fx/4096
	1	1	0	1	fx/8192
	1	1	1	0	fx/16384
	1	1	1	1	Timer 3 clock (only 16-bit Timer 3)

T4PCR1 (Timer 4 PWM Control Register 1): 1003H (ESFR)

7	6	5	4	3	2	1	0
PWM4E	ESYNC	BMOD	PHLT	UPDT	UALL	NOPS1	NOPS0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

- PWM4E** Control Timer 4 Mode
  - 0 Select timer/counter or capture mode of Timer 4
  - 1 Select 10-bit PWM mode of Timer 4
- ESYNC** Select the Operation of External Sync with the BLNK pin
  - 0 Disable external sync operation
  - 1 Enable external sync operation  
(The all PWM4xA/PWM4xB pins are high-impedance outputs on rising edge of the BLNK input pin. Where x= A, B and C)
- BMOD** Control Back-to-Back Mode Operation
  - 0 Disable back-to-back mode (up count only)
  - 1 Enable back-to-back mode (up/down count only)
- PHLT** Control Timer 4 PWM Operation
  - 0 Run 10-bit PWM
  - 1 Stop 10-bit PWM (counter hold and output disable)
- UPDT** Select the Update Timer of T4PPR/T4ADR/T4BDR/T4CDR
  - 0 Update at period match of T4CNT and T4PPR
  - 1 Update at any time when written
- UALL** Control Update All Duty Registers (T4ADR/T4BDR/T4CDR)
  - 0 Write a duty register separately
  - 1 Write all duty registers via Timer 4 PWM A duty register (T4ADR)
- NOPS[1:0]** Select on-Overlap Pre-scale
 

NOPS1	NOPS0	Description
0	0	$f_{PWM}/1$
0	1	$f_{PWM}/2$
1	0	$f_{PWM}/4$
1	1	$f_{PWM}/8$

**NOTE)**

1. Where the  $f_{PWM}$  is the clock frequency of the Timer 4 PWM.



## T4PCR2 (Timer 4 PWM Control Register 2): 1004H (ESFR)

7	6	5	4	3	2	1	0
FORCA	–	PAAOE	PABOE	PBAOE	PBBOE	PCAOE	PCBOE
RW	–	RW	RW	RW	RW	RW	RW

Initial value: 00H

- FORCA** Control The PWM outputs Mode
- 0 6-channel mode  
(The PWM4xA/PWM4xB pins are output according to the T4xDR registers, respectively. Where x = A, B and C)
  - 1 Force A-channel mode  
(The all PWM4xA/PWM4xB pins are output according to the only T4ADR registers. Where x = A, B and C)
- PAAOE** Select Channel PWM4AA Operation
- 0 Disable PWM4AA output
  - 1 Enable PWM4AA output
- PABOE** Select Channel PWM4AB Operation
- 0 Disable PWM4AB output
  - 1 Enable PWM4AB output
- PBAOE** Select Channel PWM4BA Operation
- 0 Disable PWM4BA output
  - 1 Enable PWM4BA output
- PBBOE** Select Channel PWM4BB Operation
- 0 Disable PWM4BB output
  - 1 Enable PWM4BB output
- PCAOE** Select Channel PWM4CA Operation
- 0 Disable PWM4CA output
  - 1 Enable PWM4CA output
- PCBOE** Select Channel PWM4CB Operation
- 0 Disable PWM4CB output
  - 1 Enable PWM4CB output

T4PCR3 (Timer 4 PWM Control Register 3): 1005H (ESFR)

7	6	5	4	3	2	1	0
HZCLR	POLBO	POLAA	POLAB	POLBA	POLBB	POLCA	POLCB
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

- HZCLR** High-Impedance Output Clear Bit
  - 0 No effect
  - 1 Clear high-impedance output  
(The PWM4xA/PWM4xB pins are back to output and this bit is automatically cleared to logic '0'. where x = A, B and C)
  
- POLBO** Configure PWM4AB/PWM4BB/PWM4CB Channel Polarity When these pins are disabled
  - 0 These pins are output according to the polarity setting when disable (POLAB/POLBB/POLCB bits)
  - 1 These pins are same level as the PWM4xA pins regardless of the polarity setting when disable (POLAB/POLBB/POLCB bits, where x = A, B and C)
  
- POLAA** Configure PWM4AA Channel Polarity
  - 0 Start at high level (This pin is low level when disable)
  - 1 Start at low level (This pin is high level when disable)
  
- POLAB** Configure PWM4AB Channel Polarity
  - 0 Non-inversion signal of PWM4AA pin
  - 1 Inversion signal of PWM4AA pin
  
- POLBA** Configure PWM4BA Channel Polarity
  - 0 Start at high level (This pin is low level when disable)
  - 1 Start at low level (This pin is high level when disable)
  
- POLBB** Configure PWM4BB Channel Polarity
  - 0 Non-inversion signal of PWM4BA pin
  - 1 Inversion signal of PWM4BA pin
  
- POLCA** Configure PWM4CA Channel Polarity
  - 0 Start at high level (This pin is low level when disable)
  - 1 Start at low level (This pin is high level when disable)
  
- POLCB** Configure PWM4CB Channel Polarity
  - 0 Non-inversion signal of PWM4CA pin
  - 1 Inversion signal of PWM4CA pin

**T4ISR (Timer 4 Interrupt Status Register): 1006H (ESFR)**

7	6	5	4	3	2	1	0
IOVR	IBTM	ICMA	ICMB	ICMC	–	–	–
RW	RW	RW	RW	RW	–	–	–

Initial value: 00H

<b>IOVR</b>	Timer 4 Compare Match or Timer 4 Overflow Interrupt Status, Write '0' to this bit for clear
0	Compare match or Overflow no occurrence
1	Compare match or Overflow occurrence
<b>IBTM</b>	Timer 4 Bottom Interrupt Status, Write '0' to this bit for clear (In the Back-to-Back mode)
0	Bottom no occurrence
1	Bottom occurrence
<b>ICMA</b>	Timer 4 PWM A-ch Match Interrupt Status, Write '0' to this bit for clear
0	PWM A-ch match no occurrence
1	PWM A-ch match occurrence
<b>ICMB</b>	Timer 4 PWM B-ch Match Interrupt Status, Write '0' to this bit for clear
0	PWM B-ch match no occurrence
1	PWM B-ch match occurrence
<b>ICMC</b>	Timer 4 PWM C-ch Match Interrupt Status, Write '0' to this bit for clear
0	PWM C-ch match no occurrence
1	PWM C-ch match occurrence

**T4MSK (Timer 4 Interrupt Mask Register): 1007H (ESFR)**

7	6	5	4	3	2	1	0
OVRMSK	BTMMSK	CMAMSK	CMBMSK	CMCMSK	–	–	–
RW	RW	RW	RW	RW	–	–	–

Initial value: 00H

<b>OVRMSK</b>	Control Timer 4 compare match or Overflow Interrupt
0	Disable compare match or overflow interrupt
1	Enable compare match or overflow interrupt
<b>BTMMSK</b>	Control Timer 4 Bottom Interrupt
0	Disable bottom interrupt
1	Enable bottom interrupt
<b>CMAMSK</b>	Control Timer 4 PWM A-ch Match Interrupt
0	Disable PWM A-ch match interrupt
1	Enable PWM A-ch match interrupt
<b>CMBMSK</b>	Control Timer 4 PWM B-ch Match Interrupt
0	Disable PWM B-ch match interrupt
1	Enable PWM B-ch match interrupt
<b>CMCMSK</b>	Control Timer 4 PWM C-ch Match Interrupt
0	Disable PWM C-ch match interrupt
1	Enable PWM C-ch match interrupt

## 11.9 Buzzer Driver

### 11.9.1 Overview

The Buzzer consists of 8bit counter, buzzer data register (BUZDR) and buzzer control register (BUZCR). The Square Wave (61.035Hz~125.0kHz @ 8MHz) is outputted through P13/SEG17/AN10/EC1/BUZO pin. The buzzer data register (BUZDR) controls the buzzer frequency (look at the following expression). In buzzer control register (BUZCR), BUCK[1:0] selects source clock divided by prescaler.

$$f_{BUZ}(\text{Hz}) = \frac{\text{Oscillator Frequency}}{2 \times \text{Prescaler Ratio} \times (\text{BUZDR} + 1)}$$

BUZDR[7:0]	Buzzer Frequency (kHz)			
	BUZCR[2:1]=00	BUZCR[2:1]=01	BUZCR[2:1]=10	BUZCR[2:1]=11
0000_0000	125kHz	62.5kHz	31.25kHz	15.625kHz
0000_0001	62.5kHz	31.25kHz	15.625kHz	7.812kHz
...	...	...	...	...
1111_1101	492.126Hz	246.063Hz	123.031Hz	61.515Hz
1111_1110	490.196Hz	245.098Hz	122.549Hz	61.274Hz
1111_1111	488.281Hz	244.141Hz	122.07Hz	61.035Hz

Table 11.15 Buzzer Frequency at 8 MHz

### 11.9.2 Block Diagram

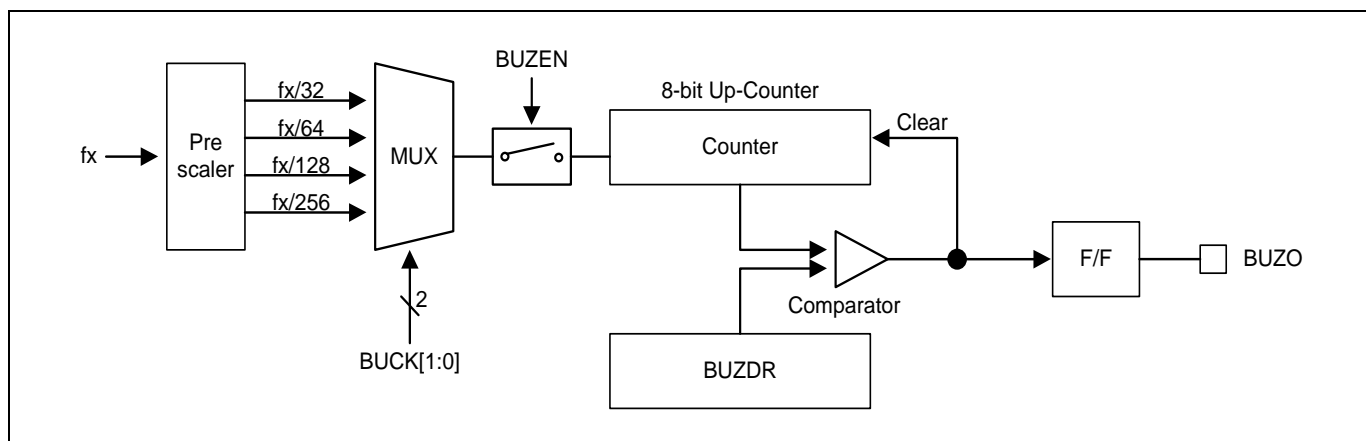


Figure 11.48 Buzzer Driver Block Diagram

### 11.9.3 Register Map

Name	Address	Direction	Default	Description
BUZDR	8FH	R/W	FFH	Buzzer Data Register
BUZCR	97H	R/W	00H	Buzzer Control Register

Table 11.16 Buzzer Driver Register Map

### 11.9.4 Buzzer Driver Register Description

Buzzer driver consists of buzzer data register (BUZDR) and buzzer control register (BUZCR).

### 11.9.5 Register Description for Buzzer Driver

#### BUZDR (Buzzer Data Register): 8FH

7	6	5	4	3	2	1	0
BUZDR7	BUZDR6	BUZDR5	BUZDR4	BUZDR3	BUZDR2	BUZDR1	BUZDR0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: FFH

**BUZDR[7:0]** This bits control the Buzzer frequency  
Its resolution is 00H ~ FFH

#### BUZCR (Buzzer Control Register): 97H

7	6	5	4	3	2	1	0
–	–	–	–	–	BUCK1	BUCK0	BUZEN
–	–	–	–	–	RW	RW	RW

Initial value: 00H

**BUCK[1:0]** Buzzer Driver Source Clock Selection

BUCK1	BUCK0	Description
0	0	fx/32
0	1	fx/64
1	0	fx/128
1	1	fx/256

**BUZEN** Buzzer Driver Operation Control

0	Buzzer Driver disable
1	Buzzer Driver enable

#### NOTE)

1. fx: System clock oscillation frequency.

## 11.10 SPI 2

### 11.10.1 Overview

There is serial peripheral interface (SPI 2) one channel in MC96F6432A. The SPI 2 allows synchronous serial data transfer between the external serial devices. It can do Full-duplex communication by 4-wire (MOSI2, MISO2, SCK2, SS2), support master/slave mode, can select serial clock (SCK2) polarity, phase and whether LSB first data transfer or MSB first data transfer.

### 11.10.2 Block Diagram

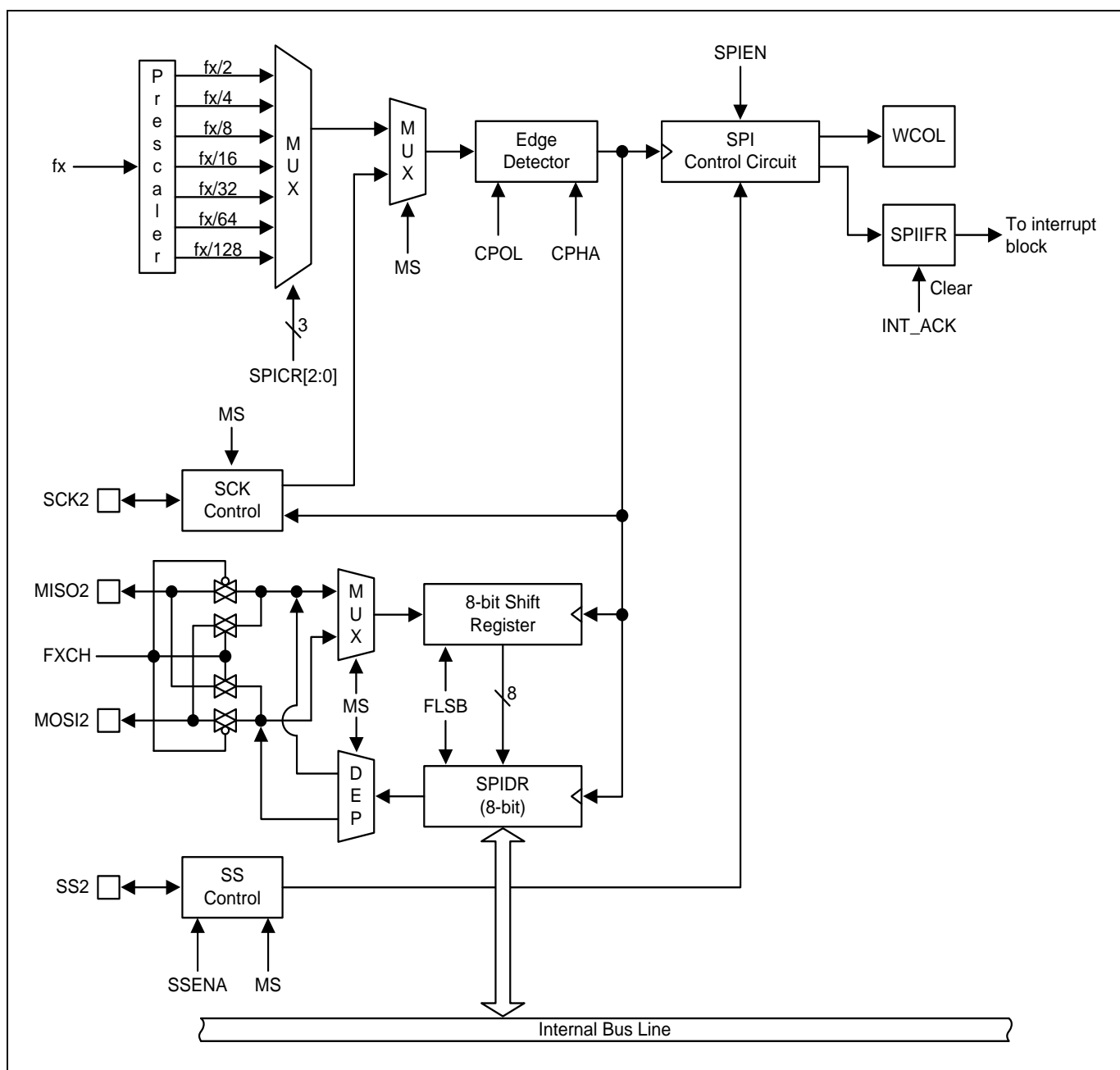


Figure 11.49 SPI 2 Block Diagram

### 11.10.3 Data Transmit / Receive Operation

User can use SPI 2 for serial data communication by following step

1. Select SPI 2 operation mode(master/slave, polarity, phase) by control register SPICR.
2. When the SPI 2 is configured as a Master, it selects a Slave by SS2 signal (active low).  
When the SPI 2 is configured as a Slave, it is selected by SS2 signal incoming from Master
3. When the user writes a byte to the data register SPIDR, SPI 2 will start an operation.
4. In this time, if the SPI 2 is configured as a Master, serial clock will come out of SCK2 pin. And Master shifts the eight bits into the Slave (transmit), Slave shifts the eight bits into the Master at the same time (receive). If the SPI 2 is configured as a Slave, serial clock will come into SCK2 pin. And Slave shifts the eight bits into the Master (transmit), Master shifts the eight bits into the Slave at the same time (receive).
5. When transmit/receive is done, SPIIFR bit will be set. If the SPI 2 interrupt is enabled, an interrupt is requested. And SPIIFR bit is cleared by hardware when executing the corresponding interrupt. If SPI 2 interrupt is disable, SPIIFR bit is cleared when user read the status register SPISR and then access (read/write) the data register SPIDR.

### 11.10.4 SS2 pin function

1. When the SPI 2 is configured as a Slave, the SS2 pin is always input. If LOW signal comes into SS2 pin, the SPI 2 logic is active. And if 'HIGH' signal comes into SS2 pin, the SPI 2 logic is stop. In this time, SPI 2 logic will be reset and invalidated any received data.
2. When the SPI 2 is configured as a Master, the user can select the direction of the SS2 pin by port direction register (P17IO). If the SS2 pin is configured as an output, user can use general P17IO output mode. If the SS2 pin is configured as an input, 'HIGH' signal must come into SS2 pin to guarantee Master operation. If 'LOW' signal comes into SS2 pin, the SPI 2 logic interprets this as another master selecting the SPI 2 as a slave and starting to send data to it. To avoid bus contention, MSB bit of SPICR will be cleared and the SPI 2 becomes a Slave and then, SPIIFR bit of SPISR will be set and if the SPI 2 interrupt is enabled, an interrupt is requested.

#### NOTE)

1. When the SS2 pin is configured as an output at Master mode, SS2 pin's output value is defined by user's software (P17IO). Before SPICR setting, the direction of SS2 pin must be defined
2. If you don't need to use SS2 pin, clear the SSENA bit of SPISR. So, you can use disabled pin by P17IO freely. In this case, SS2 signal is driven by 'HIGH' or 'LOW' internally. In other words, master is 'HIGH', slave is 'LOW'
3. When SS2 pin is configured as input, if 'HIGH' signal come into SS2 pin, SS\_HIGH flag bit will be set. And you can clear it by writing '0'.

11.10.5 SPI 2 Timing Diagram

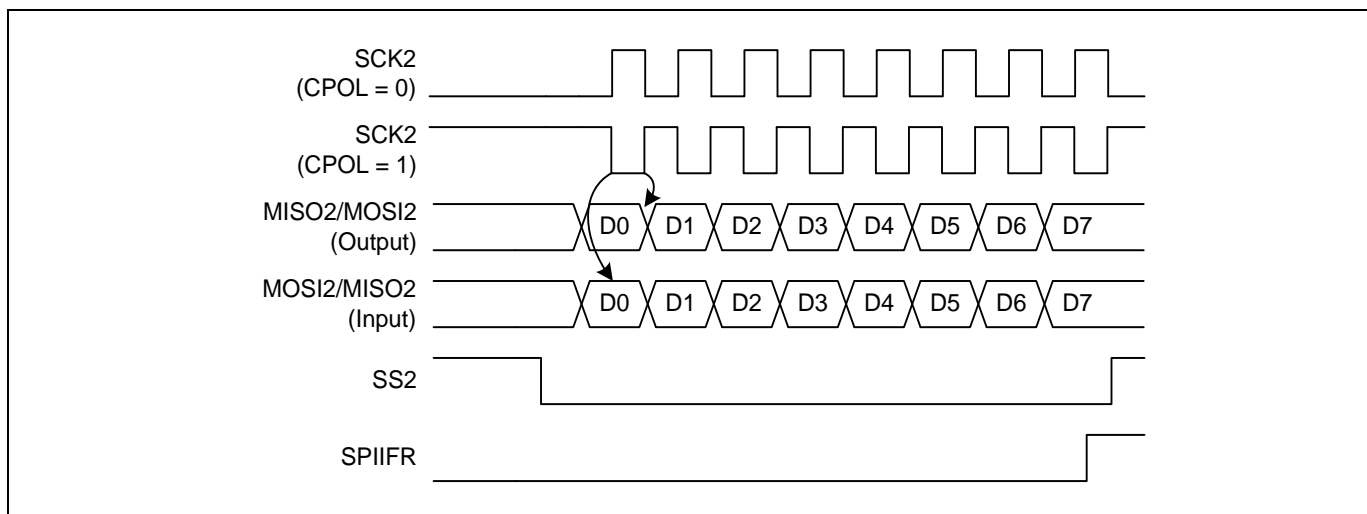


Figure 11.50 SPI 2 Transmit/Receive Timing Diagram at CPHA = 0

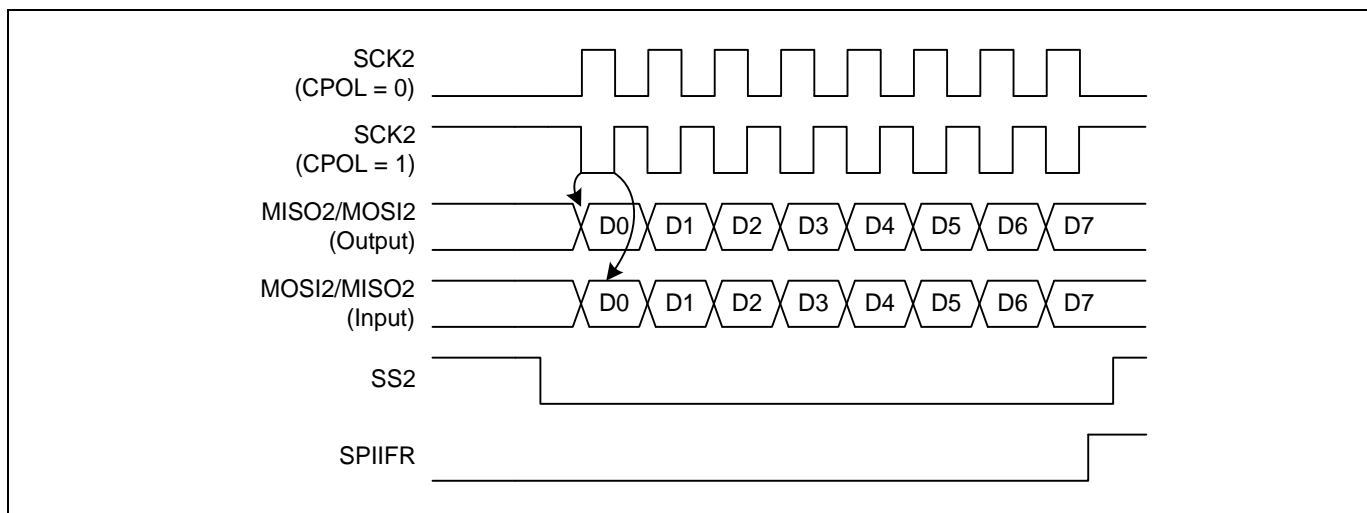


Figure 11.51 SPI 2 Transmit/Receive Timing Diagram at CPHA = 1



### 11.10.6 Register Map

Name	Address	Direction	Default	Description
SPISR	B7H	R/W	00H	SPI 2 Status Register
SPIDR	B6H	R/W	00H	SPI 2 Data Register
SPICR	B5H	R/W	00H	SPI 2 Control Register

Table 11.17 SPI 2 Register Map

### 11.10.7 SPI 2 Register Description

The SPI 2 register consists of SPI 2 control register (SPICR), SPI 2 status register (SPISR) and SPI 2 data register (SPIDR)

### 11.10.8 Register Description for SPI 2

#### SPIDR (SPI 2 Data Register): B6H

7	6	5	4	3	2	1	0
SPIDR7	SPIDR6	SPIDR5	SPIDR4	SPIDR3	SPIDR2	SPIDR1	SPIDR0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

#### SPIDR [7:0]

SPI 2 Data

When it is written a byte to this data register, the SPI 2 will start an operation.

**SPI SR (SPI 2 Status Register): B7H**

7	6	5	4	3	2	1	0
SPIIFR	WCOL	SS_HIGH	–	FXCH	SSENA	–	–
RW	R	RW	–	RW	RW	–	–

Initial value: 00H

- SPIIFR**      When SPI 2 Interrupt occurs, this bit becomes ‘1’. If SPI 2 interrupt is enable, this bit is auto cleared by INT\_ACK signal. And if SPI 2 Interrupt is disable, this bit is cleared when the status register SPI SR is read and then access (read/write) the data register SPIDR. Writing “1” has no effect.

  - 0      SPI 2 Interrupt no generation
  - 1      SPI 2 Interrupt generation
  
- WCOL**      This bit is set if any data are written to the data register SPIDR during transfer. This bit is cleared when the status register SPI SR is read and then access (read/write) the data register SPIDR

  - 0      No collision
  - 1      Collision
  
- SS\_HIGH**    When the SS2 pin is configured as input, if “HIGH” signal comes into the pin, this flag bit will be set.

  - 0      Cleared when ‘0’ is written
  - 1      No effect when ‘1’ is written
  
- FXCH**      SPI 2 port function exchange control bit.

  - 0      No effect
  - 1      Exchange MOSI2 and MISO2 function
  
- SSENA**      This bit controls the SS2 pin operation

  - 0      Disable
  - 1      Enable (The P17 should be a normal input)

**SPICR (SPI 2 Control Register): B5H**

7	6	5	4	3	2	1	0
SPIEN	FLSB	MS	CPOL	CPHA	DSCR	SCR1	SCR0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

- SPIEN** This bit controls the SPI 2 operation
  - 0 Disable SPI 2 operation
  - 1 Enable SPI 2 operation
  
- FLSB** This bit selects the data transmission sequence
  - 0 MSB first
  - 1 LSB first
  
- MS** This bit selects whether Master or Slave mode
  - 0 Slave mode
  - 1 Master mode
  
- CPOL** **CPHA** This two bits control the serial clock (SCK2) mode.  
 Clock polarity(CPOL) bit determine SCK2's value at idle mode.  
 Clock phase (CPHA) bit determine if data are sampled on the leading or trailing edge of SCK2.
 

CPOL	CPHA	Leading edge	Trailing edge
0	0	Sample (Rising)	Setup (Falling)
0	1	Setup (Rising)	Sample (Falling)
1	0	Sample (Falling)	Setup (Rising)
1	1	Setup (Falling)	Sample (Rising)
  
- DSCR** **SCR[2:0]** These three bits select the SCK2 rate of the device configured as a master. When DSCR bit is written one, SCK2 will be doubled in master mode.
 

DSCR	SCR1	SCR0	SCK2 frequency
0	0	0	fx/4
0	0	1	fx/16
0	1	0	fx/64
0	1	1	fx/128
1	0	0	fx/2
1	0	1	fx/8
1	1	0	fx/32
1	1	1	fx/64

## 11.11 12-bit A/D Converter

### 11.11.1 Overview

The analog-to-digital converter (A/D) allows conversion of an analog input signal to corresponding 12-bit digital value. The A/D module has eight analog inputs. The output of the multiplexer is the input into the converter which generates the result through successive approximation. The A/D module has four registers which are the A/D converter control high register (ADCCRH), A/D converter control low register (ADCCRL), A/D converter data high register (ADCDRH) and A/D converter data low register (ADCDRL). The channels to be converted are selected by setting ADSEL[3:0]. To execute A/D conversion, TRIG[2:0] bits should be set to 'xxx'. The register ADCDRH and ADCDRL contains the results of the A/D conversion. When the conversion is completed, the result is loaded into the ADCDRH and ADCDRL, the A/D conversion status bit AFLAG is set to '1' and the A/D interrupt is set. During A/D conversion, AFLAG bit is read as '0'.

### 11.11.2 Conversion Timing

The A/D conversion process requires 4 steps (4 clock edges) to convert each bit and 10 clocks to set up A/D conversion. Therefore, total of 58 clocks are required to complete a 12-bit conversion: When fxx/8 is selected for conversion clock with a 8MHz fxx clock frequency, one clock cycle is 1 $\mu$ s. Each bit conversion requires 4 clocks, the conversion rate is calculated as follows:

4 clocks/bit  $\times$  12 bits + set-up time = 58 clocks,

58 clock  $\times$  1 $\mu$ s = 58 $\mu$ s at 1MHz (8MHz/8)

#### NOTE)

1. The A/D converter needs at least 20 $\mu$ s for conversion time. So you must set the conversion time more than 20 $\mu$ s.

11.11.3 Block Diagram

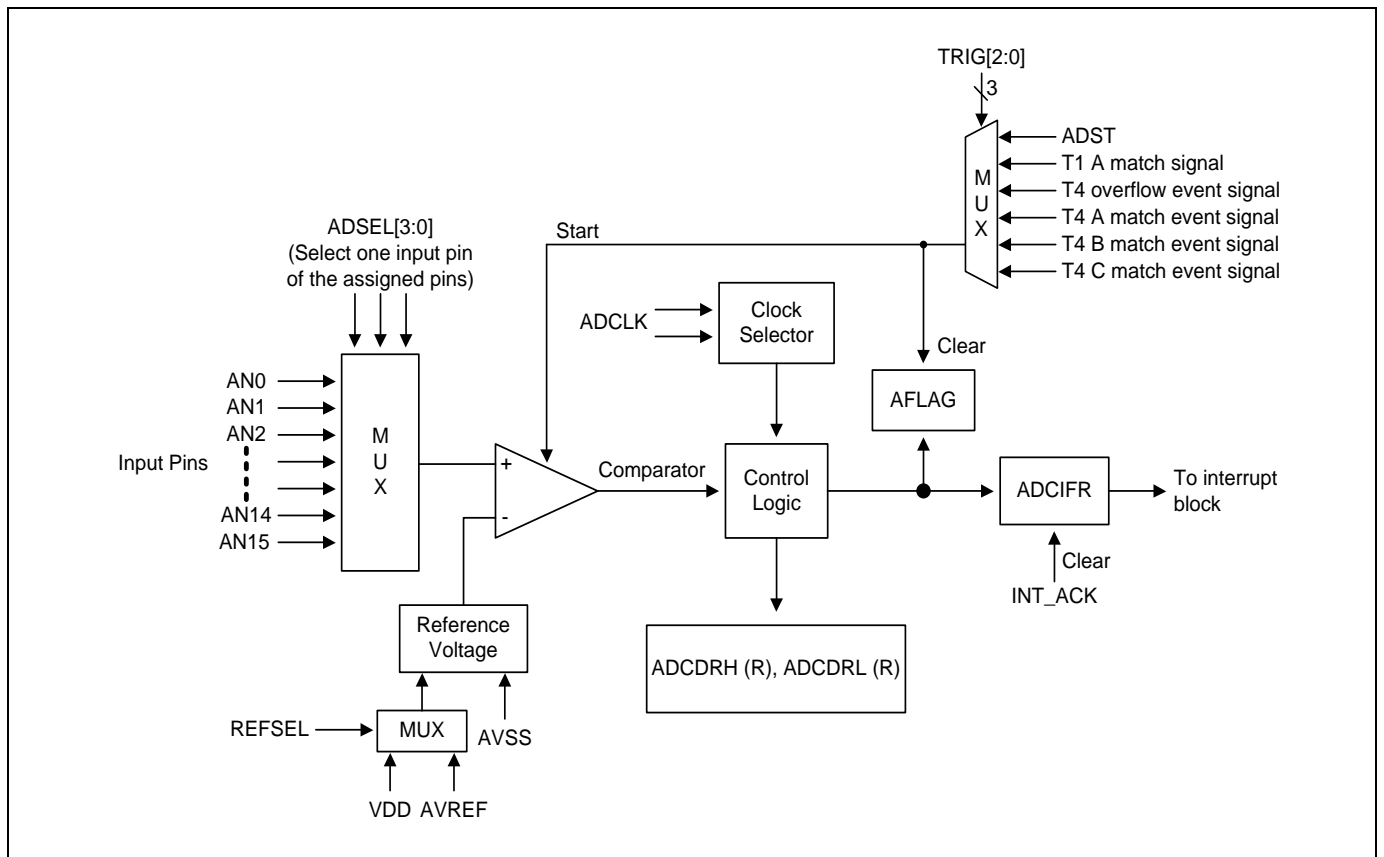


Figure 11.52 12-bit ADC Block Diagram

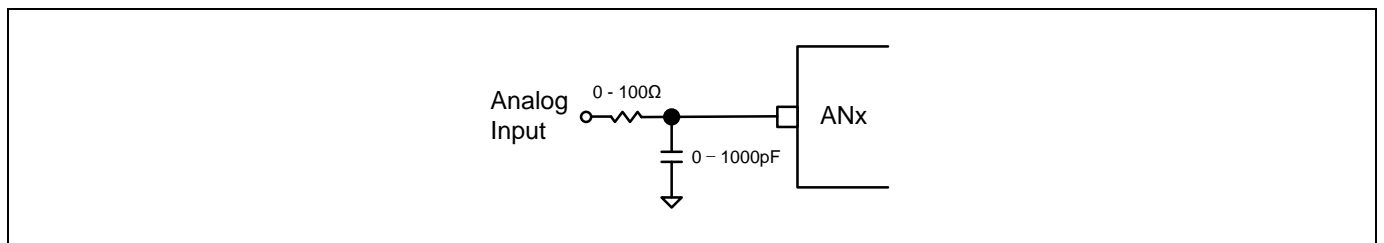


Figure 11.53 A/D Analog Input Pin with Capacitor

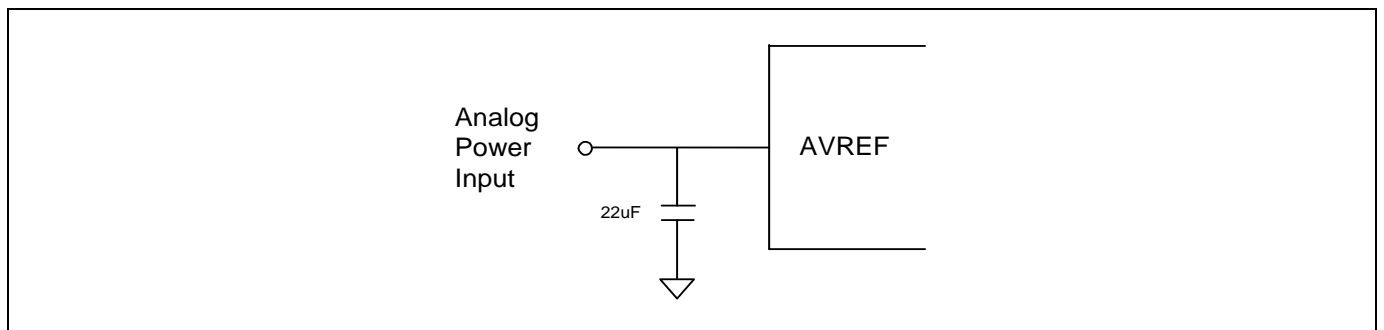


Figure 11.54 A/D Power (AVREF) Pin with Capacitor

11.11.4 ADC Operation

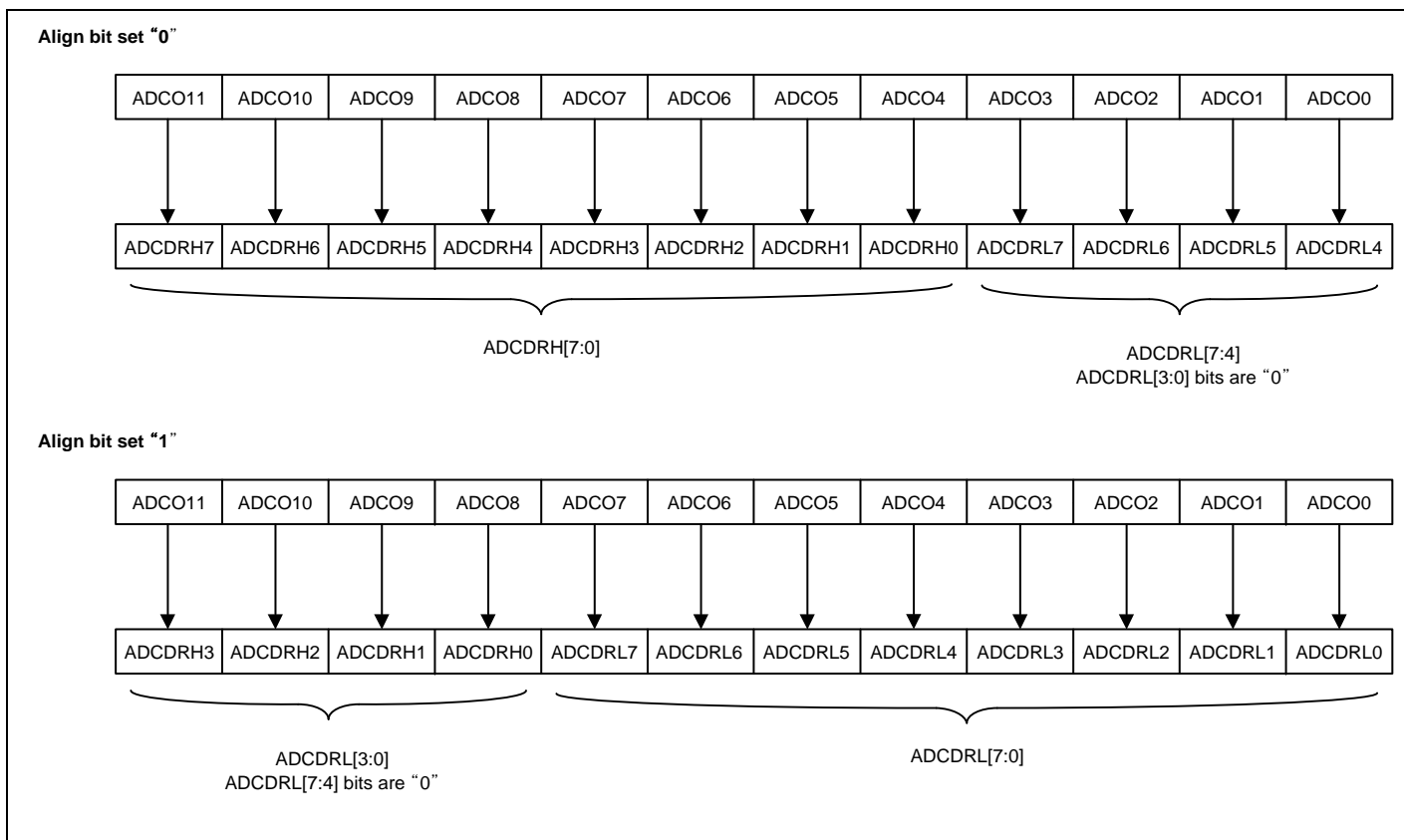


Figure 11.55 ADC Operation for Align Bit

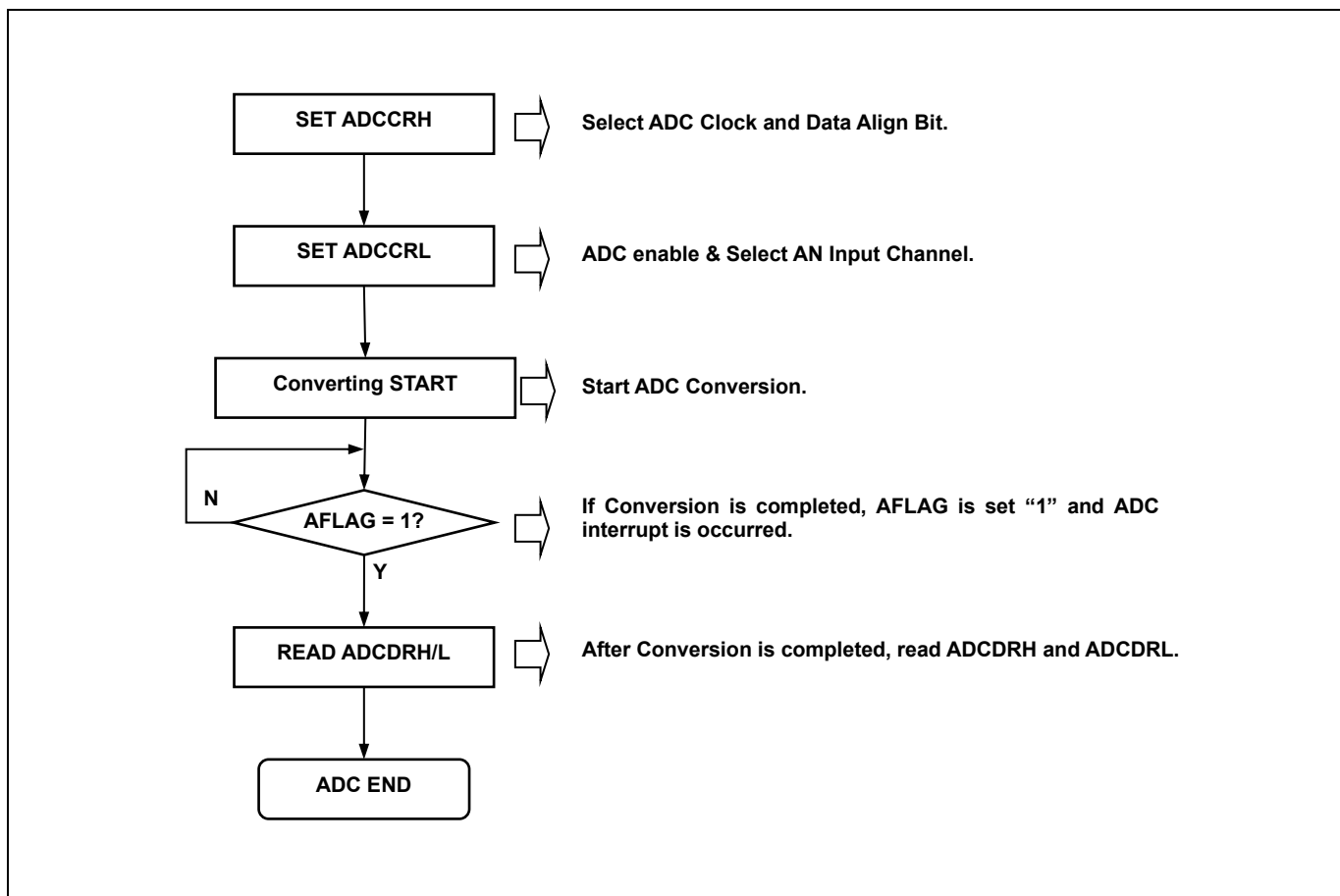


Figure 11.56 A/D Converter Operation Flow

### 11.11.5 Register Map

Name	Address	Direction	Default	Description
ADCDRH	9FH	R	xxH	A/D Converter Data High Register
ADCDRL	9EH	R	xxH	A/D Converter Data Low Register
ADCCRH	9DH	R/W	00H	A/D Converter Control High Register
ADCCRL	9CH	R/W	00H	A/D Converter Control Low Register

Table 11.18 ADC Register Map

### 11.11.6 ADC Register Description

The ADC register consists of A/D converter data high register (ADCDRH), A/D converter data low register (ADCDRL), A/D converter control high register (ADCCRH) and A/D converter control low register (ADCCRL).

### 11.11.7 Register Description for ADC

#### ADCDRH (A/D Converter Data High Register): 9FH

7	6	5	4	3	2	1	0
ADDM11	ADDM10	ADDM9	ADDM8	ADDM7 ADDL11	ADDM6 ADDL10	ADDM5 ADDL9	ADDM4 ADDL8
R	R	R	R	R	R	R	R

Initial value: xxH

**ADDM[11:4]** MSB align, A/D Converter High Data (8-bit)

**ADDL[11:8]** LSB align, A/D Converter High Data (4-bit)

#### ADCDRL (A/D Converter Data Low Register): 9EH

7	6	5	4	3	2	1	0
ADDM3 ADDL7	ADDM2 ADDL6	ADDM1 ADDL5	ADDM0 ADDL4	ADDL3	ADDL2	ADDL1	ADDL0
R	R	R	R	R-	R	R	R

Initial value: xxH

**ADDM[3:0]** MSB align, A/D Converter Low Data (4-bit)

**ADDL[7:0]** LSB align, A/D Converter Low Data (8-bit)

#### ADCCRH (A/D Converter Control High Register): 9DH

7	6	5	4	3	2	1	0
ADCIFR	–	TRIG2	TRIG1	TRIG0	ALIGN	CKSEL1	CKSEL0
RW	–	RW	RW	RW	RW	RW	RW

Initial value: 00H

**ADCIFR** When ADC interrupt occurs, this bit becomes ‘1’. For clearing bit, write ‘0’ to this bit or auto clear by INT\_ACK signal. Writing “1” has no effect.

0 ADC Interrupt no generation

1 ADC Interrupt generation

**TRIG[2:0]** A/D Trigger Signal Selection

TRIG2	TRIG1	TRIG0	Description
0	0	0	ADST
0	0	1	Timer 1 A match signal
0	1	0	Timer 4 overflow event signal
0	1	1	Timer 4 A match event signal
1	0	0	Timer 4 B match event signal
1	0	1	Timer 4 C match event signal

Other Values Not used

**ALIGN** A/D Converter data align selection.

0 MSB align (ADCDRH[7:0], ADCDRL[7:4])

1 LSB align (ADCDRH[3:0], ADCDRL[7:0])

**CKSEL[1:0]** A/D Converter Clock selection

CKSEL1	CKSEL0	Description
0	0	fx/1
0	1	fx/2
1	0	fx/4
1	1	fx/8



## ADCCRL (A/D Converter Control Low Register): 9CH

7	6	5	4	3	2	1	0
STBY	ADST	REFSEL	AFLAG	ADSEL3	ADSEL2	ADSEL1	ADSEL0
RW	RW	RW	R	RW	RW	RW	RW

Initial value: 00H

<b>STBY</b>	Control Operation of A/D (The ADC module is automatically disabled at stop mode)				
	0	ADC module disable			
	1	ADC module enable			
<b>ADST</b>	Control A/D Conversion stop/start.				
	0	No effect			
	1	ADC Conversion Start and auto clear			
<b>REFSEL</b>	A/D Converter Reference Selection				
	0	Internal Reference (VDD)			
	1	External Reference (AVREF)			
<b>AFLAG</b>	A/D Converter Operation State (This bit is cleared to '0' when the STBY bit is set to '0' or when the CPU is at STOP mode)				
	0	During A/D Conversion			
	1	A/D Conversion finished			
<b>ADSEL[3:0]</b>	A/D Converter input selection				
	ADSEL3	ADSEL2	ADSEL1	ADSEL0	Description
	0	0	0	0	AN0
	0	0	0	1	AN1
	0	0	1	0	AN2
	0	0	1	1	AN3
	0	1	0	0	AN4
	0	1	0	1	AN5
	0	1	1	0	AN6
	0	1	1	1	AN7
	1	0	0	0	AN8
	1	0	0	1	AN9
	1	0	1	0	AN10
	1	0	1	1	AN11
	1	1	0	0	AN12
	1	1	0	1	AN13
	1	1	1	0	AN14
	1	1	1	1	AN15

## 11.12 USI (USART + SPI + I2C)

### 11.12.1 Overview

The USI is an acronym of USART, SPI and I2C, MC96F6432A has two USI function blocks, USI0 and USI1 are absolutely same functionally. Each USI consists of USI control register1/2/3/4, USI status register 1/2, USI baud-rate generation register, USI data register, USI SDA hold time register, USI SCL high period register, USI SCL low period register and USI slave address register (USInCR1, USInCR2, USInCR3, USInCR4, USInST1, USInST2, USInBD, USInDR, USInSDHR, USInSCHR, USInSCLR, USInSAR) n is 0 or 1.

The operation mode is selected by the operation mode of USIn selection bits (USInMS[1:0]).

It has four operating modes:

- Asynchronous mode (UART)
- Synchronous mode (USART)
- SPI mode
- I2C mode

### 11.12.2 USIn UART Mode

The universal synchronous and asynchronous serial receiver and transmitter (USART) is a highly flexible serial communication device. The main features are listed below.

- Full Duplex Operation (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation
- Baud Rate Generator
- Supports Serial Frames with 5,6,7,8 or 9 Data bits and 1 or 2 Stop bits
- Odd or Even Parity Generation and Parity Check are Supported by Hardware
- Data OverRun Detection
- Framing Error Detection
- Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion
- Double Speed Asynchronous communication mode

The USIn comprises clock generator, transmitter and receiver. The clock generation logic consists of synchronization logic for external clock input used by synchronizing or SPI slave operation and the baud rate generator for asynchronous or master (synchronous or SPI) operation.

The Transmitter consists of a single write buffer, a serial shift register, parity generator and control logic for handling different serial frame formats. The write buffer allows continuous transfer of data without any delay between frames. The receiver is the most complex part of the UART module due to its clock and data recovery units. The recovery unit is used for asynchronous data reception. In addition to the recovery unit, the receiver includes a parity checker, a shift register, a two-level receive FIFO (USInDR) and control logic. The receiver supports the same frame formats as the transmitter and can detect frame error, data overrun and parity errors.

11.12.3 US<sub>n</sub> UART Block Diagram

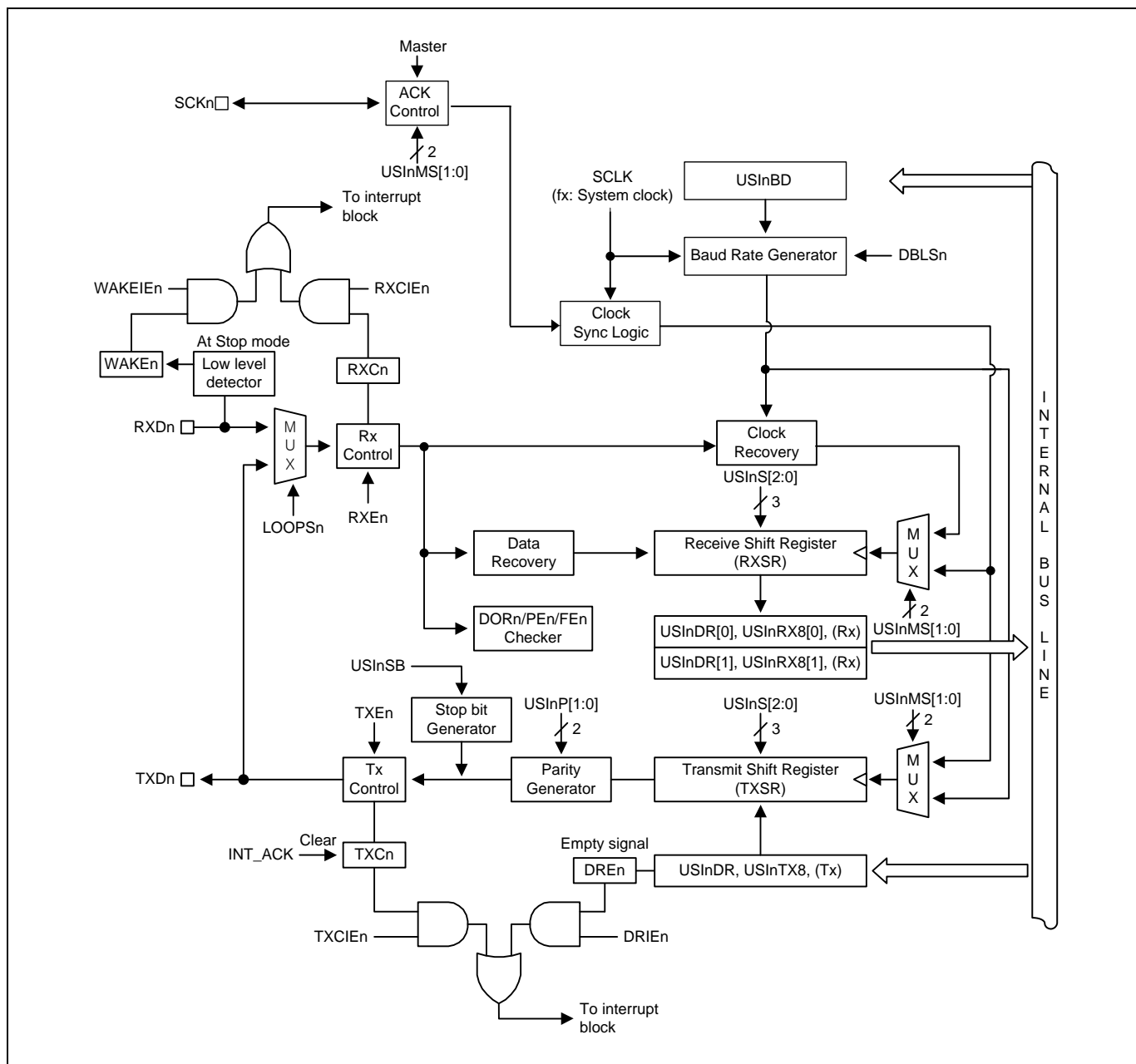


Figure 11.57 US<sub>n</sub> USART Block Diagram(n = 0, 1)

11.12.4 USIn Clock Generation

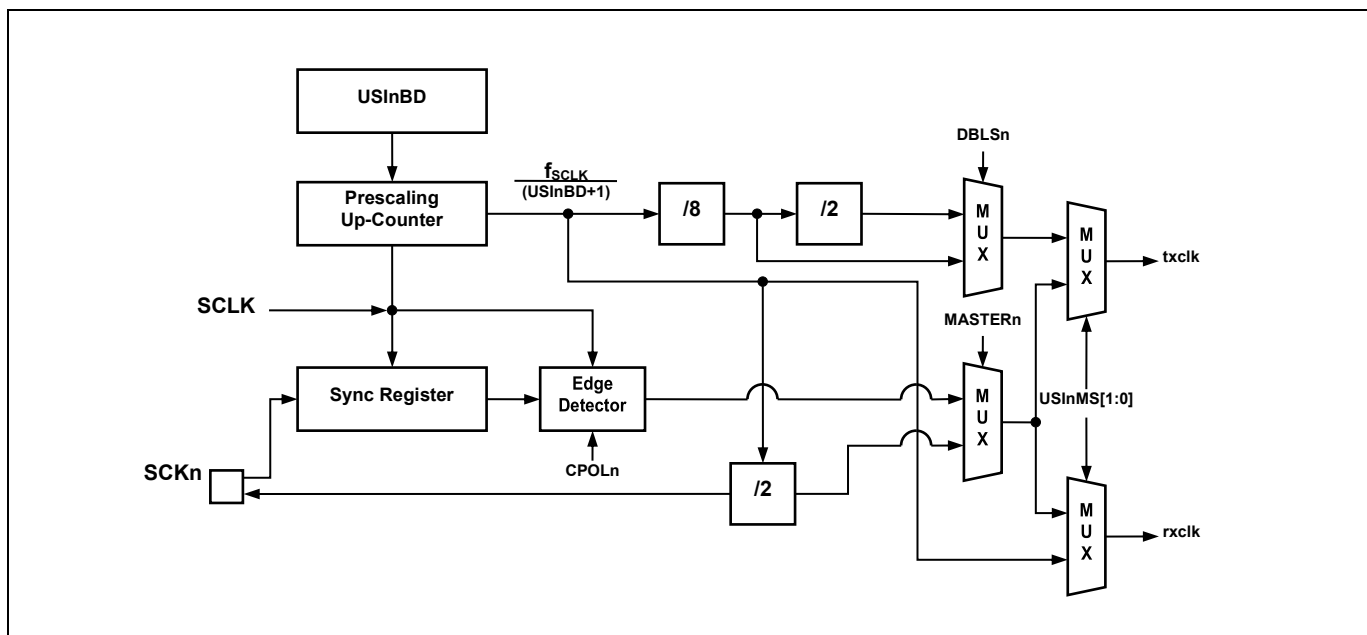


Figure 11.58 Clock Generation Block Diagram (USIn)

The clock generation logic generates the base clock for the transmitter and receiver. The USIn supports four modes of clock operation and those are normal asynchronous, double speed asynchronous, master synchronous and slave synchronous mode. The clock generation scheme for master SPI and slave SPI mode is the same as master synchronous and slave synchronous operation mode. The USInMS[1:0] bits in USInCR1 register selects asynchronous or synchronous operation. Asynchronous double speed mode is controlled by the DBLSn bit in the USInCR2 register. The MASTERn bit in USInCR3 register controls whether the clock source is internal (master mode, output pin) or external (slave mode, input pin). The SCKn pin is active only when the USIn operates in synchronous or SPI mode.

Following table shows the equations for calculating the baud rate (in bps).

Operating Mode	Equation for Calculating Baud Rate
Asynchronous Normal Mode (DBLSn=0)	$\text{Baud Rate} = \frac{f_x}{16(\text{USInBD} + 1)}$
Asynchronous Double Speed Mode (DBLSn=1)	$\text{Baud Rate} = \frac{f_x}{8(\text{USInBD} + 1)}$
Synchronous or SPI Master Mode	$\text{Baud Rate} = \frac{f_x}{2(\text{USInBD} + 1)}$

Table 11.19 Equations for Calculating USIn Baud Rate Register Setting

### 11.12.5 USIn External Clock (SCKn)

External clocking is used in the synchronous mode of operation.

External clock input from the SCKn pin is sampled by a synchronization logic to remove meta-stability. The output from the synchronization logic must be passed through an edge detector before it is used by the transmitter and receiver. This process introduces two CPU clock period delay. The maximum frequency of the external SCKn pin is limited up to 1MHz.

### 11.12.6 USIn Synchronous mode operation

When synchronous or SPI mode is used, the SCKn pin will be used as either clock input (slave) or clock output (master). Data sampling and transmitter is issued on the different edge of SCKn clock each other. For example, if data input on RXDn (MISO in SPI mode) pin is sampled on the rising edge of SCKn clock, data output on TXDn (MOSI in SPI mode) pin is altered on the falling edge.

The CPOLn bit in USInCR1 register selects which SCKn clock edge is used for data sampling and which is used for data change. As shown in the figure below, when CPOLn is zero, the data will be changed at SCKn rising edge and sampled at SCKn falling edge.

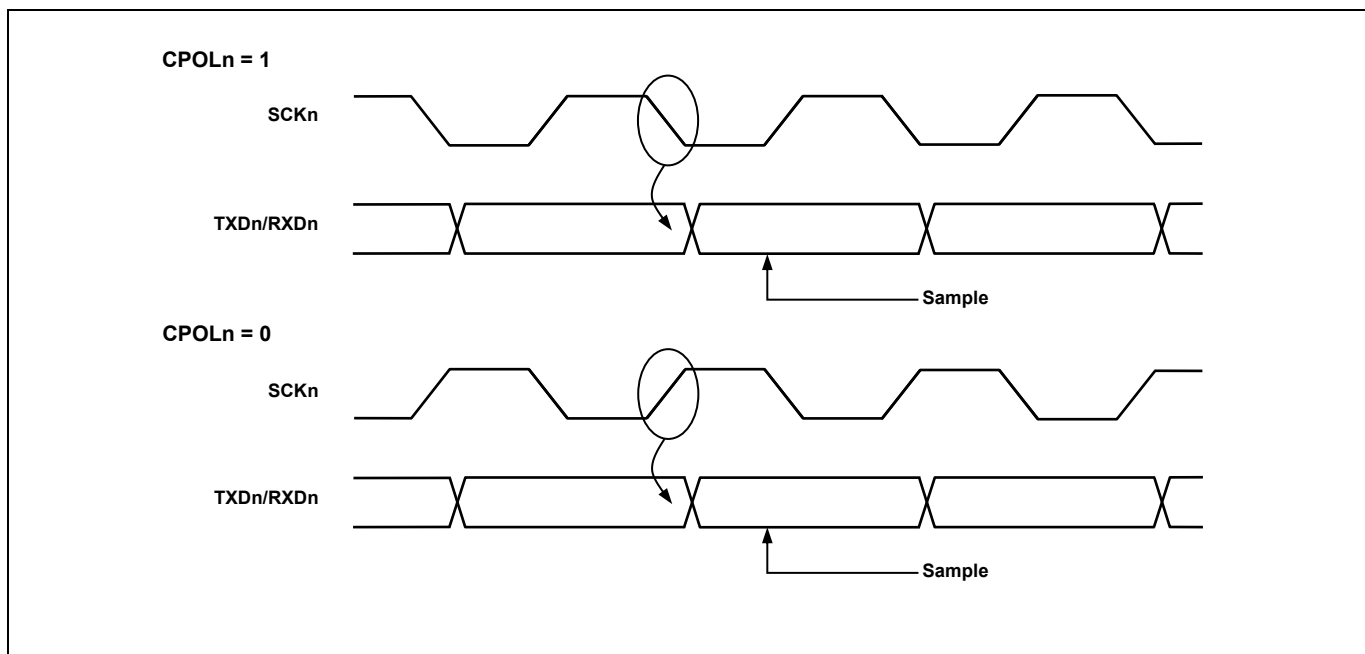


Figure 11.59 Synchronous Mode SCKn Timing (USIn)

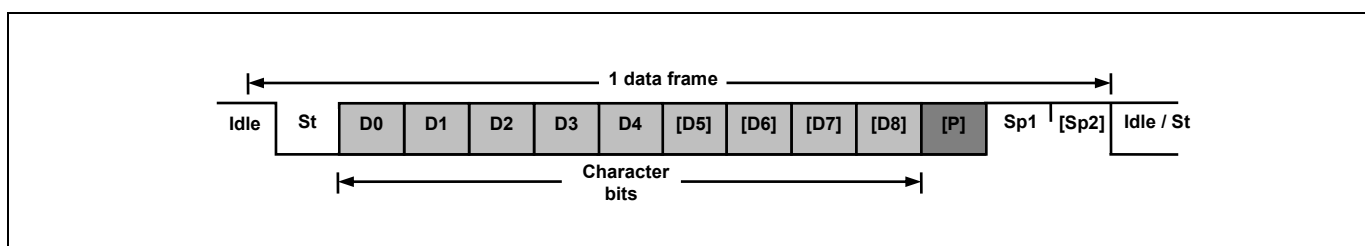
### 11.12.7 USIn UART Data format

A serial frame is defined to be one character of data bits with synchronization bits (start and stop bits) and optionally a parity bit for error detection.

The USART supports all 30 combinations of the following as valid frame formats.

- 1 start bit
- 5, 6, 7, 8 or 9 data bits
- no, even or odd parity bit
- 1 or 2 stop bits

A frame starts with the start bit followed by the least significant data bit (LSB). Then the next data bits, up to nine, are succeeding, ending with the most significant bit (MSB). If parity function is enabled, the parity bit is inserted between the last data bit and the stop bit. A high-to-low transition on data pin is considered as start bit. When a complete frame is transmitted, it can be directly followed by a new frame or the communication line can be set to an idle state. The idle means high state of data pin. The following figure shows the possible combinations of the frame formats. Bits inside brackets are optional.



**Figure 11.60** Frame Format(USIn)

1 data frame consists of the following bits

- Idle No communication on communication line (TXDn/RXDn)
- St Start bit (Low)
- Dn Data bits (0~8)
- Parity bit ----- Even parity, Odd parity, No parity
- Stop bit(s) ----- 1 bit or 2 bits

The frame format used by the UART is set by the USInS[2:0], USInPM[1:0] bits in USInCR1 register and USInSB bit in USInCR3 register. The transmitter and receiver use the same figures.

### 11.12.8 USIn UART Parity bit

The parity bit is calculated by doing an exclusive-OR of all the data bits. If odd parity is used, the result of the exclusive-OR is inverted. The parity bit is located between St + bits and first stop bit of a serial frame.

$$P_{\text{even}} = D_{n-1} \wedge \dots \wedge D_3 \wedge D_2 \wedge D_1 \wedge D_0 \wedge 0$$

$$P_{\text{odd}} = D_{n-1} \wedge \dots \wedge D_3 \wedge D_2 \wedge D_1 \wedge D_0 \wedge 1$$

$P_{\text{even}}$  : Parity bit using even parity

$P_{\text{odd}}$  : Parity bit using odd parity

$D_n$  : Data bit n of the character

### 11.12.9 USIn UART Transmitter

The UART transmitter is enabled by setting the TXEn bit in USInCR2 register. When the Transmitter is enabled, the TXDn pin should be set to TXDn function for the serial output pin of UART by the P4FSR[3:2] and P2FSRL[1:0]. The baud-rate, operation mode and frame format must be set up once before doing any transmission. In synchronous operation mode, the SCKn pin is used as transmission clock, so it should be selected to do SCKn function by P4FSR[5:4] and P2FSRL[3:2].

#### 11.12.9.1 USIn UART Sending TX data

A data transmission is initiated by loading the transmit buffer (USInDR register I/O location) with the data to be transmitted. The data be written in transmit buffer is moved to the shift register when the shift register is ready to send a new frame. The shift register is loaded with the new data if it is in idle state or immediately after the last stop bit of the previous frame is transmitted. When the shift register is loaded with new data, it will transfer one complete frame according to the settings of control registers. If the 9-bit characters are used in asynchronous or synchronous operation mode, the ninth bit must be written to the USInTX8 bit in USInCR3 register before it is loaded to the transmit buffer (USInDR register).

#### 11.12.9.2 USIn UART Transmitter flag and interrupt

The USART transmitter has two flags which indicate its state. One is USART data register empty flag (DREn) and the other is transmit completion flag (TXCn). Both flags can be used as interrupt sources.

DREn flag indicates whether the transmit buffer is ready to receive new data. This bit is set when the transmit buffer is empty and cleared when the transmit buffer contains transmission data which has not yet been moved into the shift register. And also this flag can be cleared by writing '0' to this bit position. Writing '1' to this bit position is not valid.

When the data register empty interrupt enable (DRIEn) bit in USInCR2 register is set and the global interrupt is enabled, USInST1 status register empty interrupt is generated while DREn flag is set.

The transmit complete (TXCn) flag bit is set when the entire frame in the transmit shift register has been shifted out and there is no more data in the transmit buffer. The TXCn flag is automatically cleared when the transmit complete interrupt serve routine is executed or it can be cleared by writing '0' to TXCn bit in USInST1 register.

When the transmit complete interrupt enable (TXCIEn) bit in USInCR2 register is set and the global interrupt is enabled, UART transmit complete interrupt is generated while TXCn flag is set.



### 11.12.9.3 USIn UART Parity Generator

The parity generator calculates the parity bit for the serial frame data to be sent. When parity bit is enabled (USInPM1=1), the transmitter control logic inserts the parity bit between the bits and the first stop bit of the frame to be sent.

### 11.12.9.4 USIn UART Disabling Transmitter

Disabling the transmitter by clearing the TXEn bit will not become effective until ongoing transmission is completed. When the Transmitter is disabled, the TXDn pin can be used as a normal general purpose I/O (GPIO).

### 11.12.10 USIn UART Receiver

The USART receiver is enabled by setting the RXEn bit in the USInCR2 register. When the receiver is enabled, the RXDn pin should be set to RXDn function for the serial input pin of UART by P4FSR[1:0] and P4FSR[1:0]. The baud-rate, mode of operation and frame format must be set before serial reception. In synchronous or SPI operation mode the SCKn pin is used as transfer clock input, so it should be selected to do SCKn function by P4FSR[5:4] and P2FSRL[3:2]. In SPI operation mode the SSn input pin in slave mode or can be configured as SSn output pin in master mode. This can be done by setting USInSSEN bit in USInCR3 register.

#### 11.12.10.1 USIn UART Receiving RX data

When UART is in synchronous or asynchronous operation mode, the receiver starts data reception when it detects a valid start bit (LOW) on RXD0 pin. Each bit after start bit is sampled at pre-defined baud-rate (asynchronous) or sampling edge of SCKn (synchronous) and shifted into the receive shift register until the first stop bit of a frame is received. Even if there's the second stop bit in the frame, the second stop bit is ignored by the receiver. That is, receiving the first stop bit means that a complete serial frame is presented in the receiver shift register and contents of the shift register are to be moved into the receive buffer. The receive buffer is read by reading the USInDR register.

If 9-bit characters are used (USInS[2:0] = "111"), the ninth bit is stored in the USInRX8 bit position in the USInCR3 register. The ninth bit must be read from the USInRX8 bit before reading the low 8 bits from the USInDR register. Likewise, the error flags FEn, DORn, PEn must be read before reading the data from USInDR register. It's because the error flags are stored in the same FIFO position of the receive buffer.

### 11.12.10.2 USIn UART Receiver Flag and Interrupt

The UART receiver has one flag that indicates the receiver state.

The receive complete (RXCn) flag indicates whether there are unread data in the receive buffer. This flag is set when there is unread data in the receive buffer and cleared when the receive buffer is empty. If the receiver is disabled (RXEn=0), the receiver buffer is flushed and the RXCn flag is cleared.

When the receive complete interrupt enable (RXCIEn) bit in the USInCR2 register is set and global interrupt is enabled, the UART receiver complete interrupt is generated while RXCn flag is set.

The UART receiver has three error flags which are frame error (FEn), data overrun (DORn) and parity error (PEn). These error flags can be read from the USInST1 register. As received data is stored in the 2-level receive buffer, these error flags are also stored in the same position of receive buffer. So, before reading received data from USInDR register, read the USInST1 register first which contains error flags.

The frame error (FEn) flag indicates the state of the first stop bit. The FEn flag is '0' when the stop bit was correctly detected as "1" and the FEn flag is "1" when the stop bit was incorrect, i.e. detected as "0". This flag can be used for detecting out-of-sync conditions between data frames.

The data overrun (DORn) flag indicates data loss due to a receive buffer full condition. DORn occurs when the receive buffer is full and another new data is presented in the receive shift register which are to be stored into the receive buffer. After the DORn flag is set, all the incoming data are lost. To avoid data loss or clear this flag, read the receive buffer.

The parity error (PEn) flag indicates that the frame in the receive buffer had a parity error when received. If parity check function is not enabled (USInPM1=0), the PE bit is always read "0".

### 11.12.10.3 USIn UART Parity Checker

If parity bit is enabled (USInPM1=1), the Parity Checker calculates the parity of the data bits in incoming frame and compares the result with the parity bit from the received serial frame.

### 11.12.10.4 USIn UART Disabling Receiver

In contrast to transmitter, disabling the Receiver by clearing RXEn bit makes the Receiver inactive immediately. When the receiver is disabled, the receiver flushes the receive buffer, the remaining data in the buffer is all reset and the RXDn pin can be used as a normal general purpose I/O (GPIO).

11.12.10.5 USIn Asynchronous Data Reception

To receive asynchronous data frame, the UART includes a clock and data recovery unit. The clock recovery logic is used for synchronizing the internally generated baud-rate clock to the incoming asynchronous serial frame on the RXDn pin.

The Data recovery logic samples incoming bits and low pass filters them, and this removing the noise of RXDn pin.

The next figure illustrates the sampling process of the start bit of an incoming frame. The sampling rate is 16 times of the baud-rate in normal mode and 8 times the baud-rate for double speed mode (DBLSn=1). The horizontal arrows show the synchronization variation due to the asynchronous sampling process. Note that larger time variation is shown when using the double speed mode.

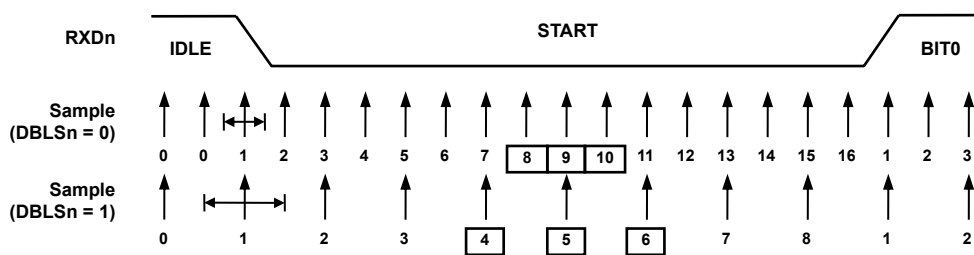


Figure 11.61 Asynchronous Start Bit Sampling (USIn)

When the receiver is enabled (RXEn=1), the clock recovery logic tries to find a high-to-low transition on the RXDn line, the start bit condition. After detecting high to low transition on RXDn line, the clock recovery logic uses samples 8, 9 and 10 for normal mode to decide if a valid start bit is received. If more than 2 samples have logical low level, it is considered that a valid start bit is detected and the internally generated clock is synchronized to the incoming data frame. And the data recovery can begin. The synchronization process is repeated for each start bit.

As described above, when the receiver clock is synchronized to the start bit, the data recovery can begin. Data recovery process is almost same to the clock recovery process. The data recovery logic samples 16 times for each incoming bits for normal mode and 8 times for double speed mode and uses sample 8, 9 and 10 to decide data value. If more than 2 samples have low levels, the received bit is considered to a logic '0' and if more than 2 samples have high levels, the received bit is considered to a logic '1'. The data recovery process is then repeated until a complete frame is received including the first stop bit. The decided bit value is stored in the receive shift register in order. Note that the Receiver only uses the first stop bit of a frame. Internally, after receiving the first stop bit, the Receiver is in idle state and waiting to find start bit.

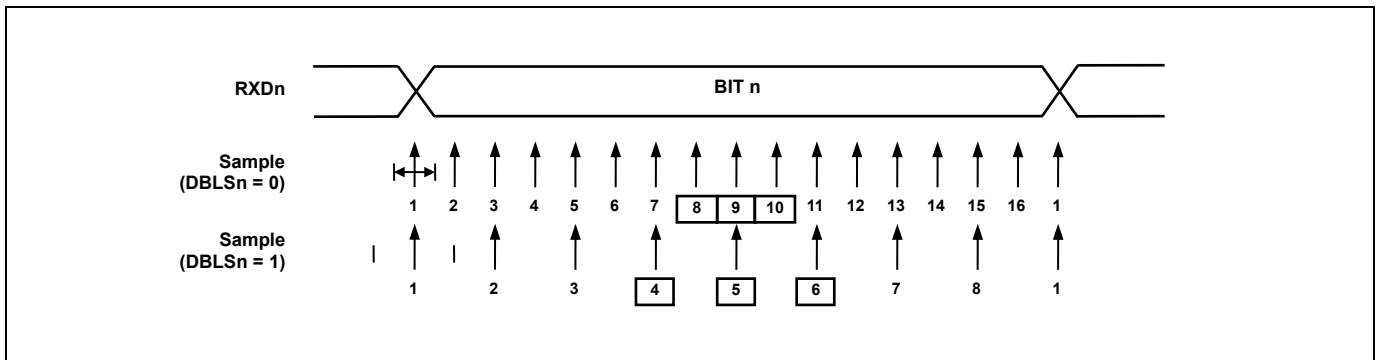


Figure 11.62 Asynchronous Sampling of Data and Parity Bit (USn)

The process for detecting stop bit is same as clock and data recovery process. That is, if 2 or more samples of 3 center values have high level, correct stop bit is detected, else a frame error (FEn) flag is set. After deciding whether the first stop bit is valid or not, the Receiver enters into idle state and monitors the RXDn line to check a valid high to low transition is detected (start bit detection).

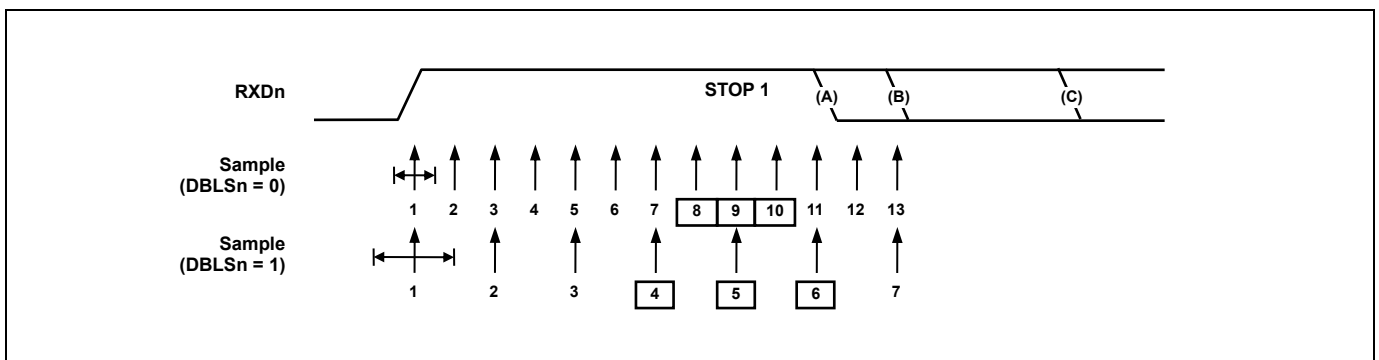


Figure 11.63 Stop Bit Sampling and Next Start Bit Sampling (USn)

### 11.12.11 USIn SPI Mode

The USIn can be set to operate in industrial standard SPI compliant mode. The SPI mode has the following features.

- Full Duplex, Three-wire synchronous data transfer
- Master and Slave Operation
- Supports all four SPI modes of operation (mode 0, 1, 2 and 3)
- Selectable LSB first or MSB first data transfer
- Double buffered transmit and receive
- Programmable transmit bit rate

When SPI mode is enabled (USInMS[1:0]="11"), the slave select (SSn) pin becomes active LOW input in slave mode operation or can be output in master mode operation if USInSSEN bit is set to '0'.

Note that during SPI mode of operation, the pin RXDn is renamed as MISO<sub>n</sub> and TXDn is renamed as MOS<sub>n</sub> for compatibility to other SPI devices.

### 11.12.12 USIn SPI Clock Formats and Timing

To accommodate a wide variety of synchronous serial peripherals from different manufacturers, the USIn has a clock polarity bit (CPOL<sub>n</sub>) and a clock phase control bit (CPHAN) to select one of four clock formats for data transfers. CPOL<sub>n</sub> selectively insert an inverter in series with the clock. CPHAN selects one of two different clock phase relationships between the clock and data. Note that CPHAN and CPOL<sub>n</sub> bits in USInCR1 register have different meanings according to the USInMS[1:0] bits which decides the operating mode of USIn.

Table below shows four combinations of CPOL<sub>n</sub> and CPHAN for SPI mode 0, 1, 2 and 3.

SPI Mode	CPOL <sub>n</sub>	CPHAN	Leading Edge	Trailing Edge
0	0	0	Sample (Rising)	Setup (Falling)
1	0	1	Setup (Rising)	Sample (Falling)
2	1	0	Sample (Falling)	Setup (Rising)
3	1	1	Setup (Falling)	Sample (Rising)

**Table 11.20** CPOL<sub>n</sub> Functionality

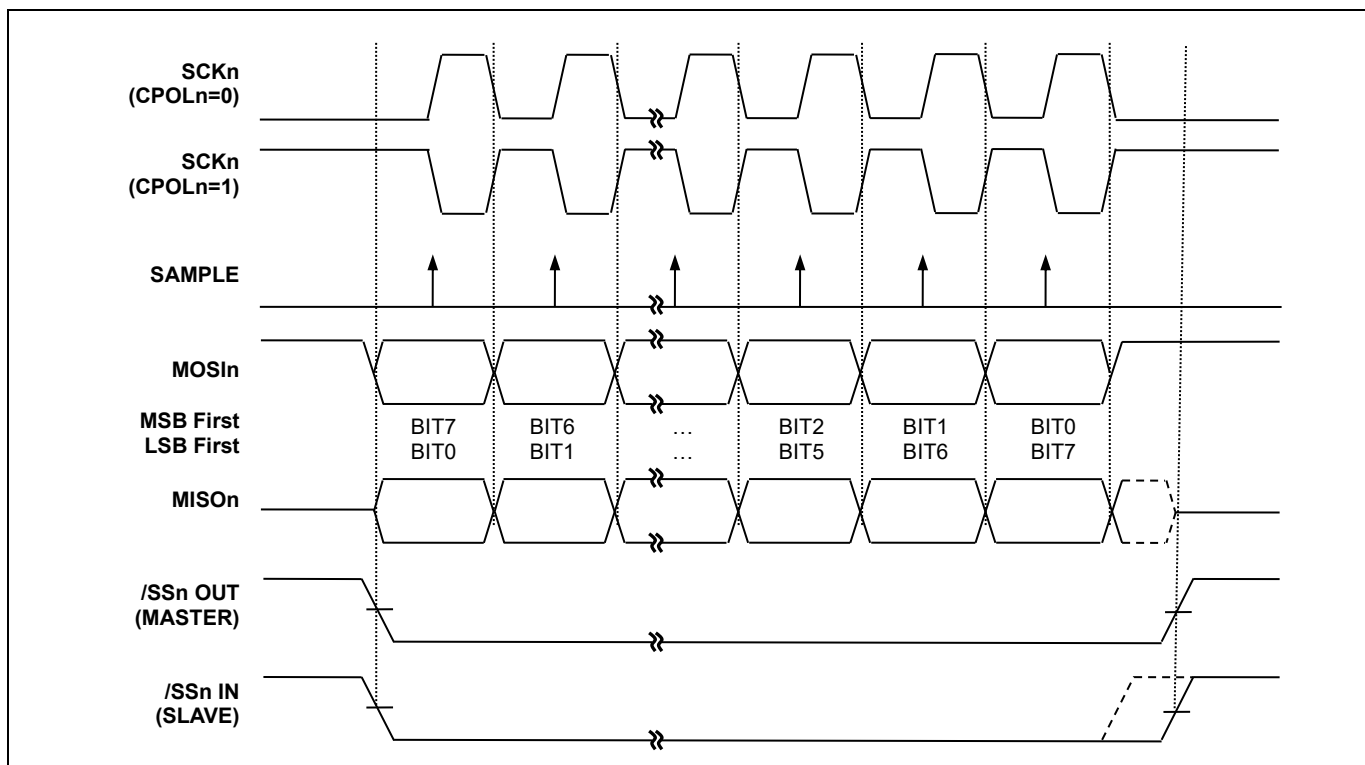


Figure 11.64 USIn SPI Clock Formats when CPHAn=0

When CPHAn=0, the slave begins to drive its MISOIn output with the first data bit value when SSn goes to active low. The first SCKn edge causes both the master and the slave to sample the data bit value on their MISOIn and MOSIn inputs, respectively. At the second SCKn edge, the USIn shifts the second data bit value out to the MOSIn and MISOIn outputs of the master and slave, respectively. Unlike the case of CPHAn=1, when CPHAn=0, the slave's SSn input must go to its inactive high level between transfers. This is because the slave can prepare the first data bit when it detects falling edge of SSn input.

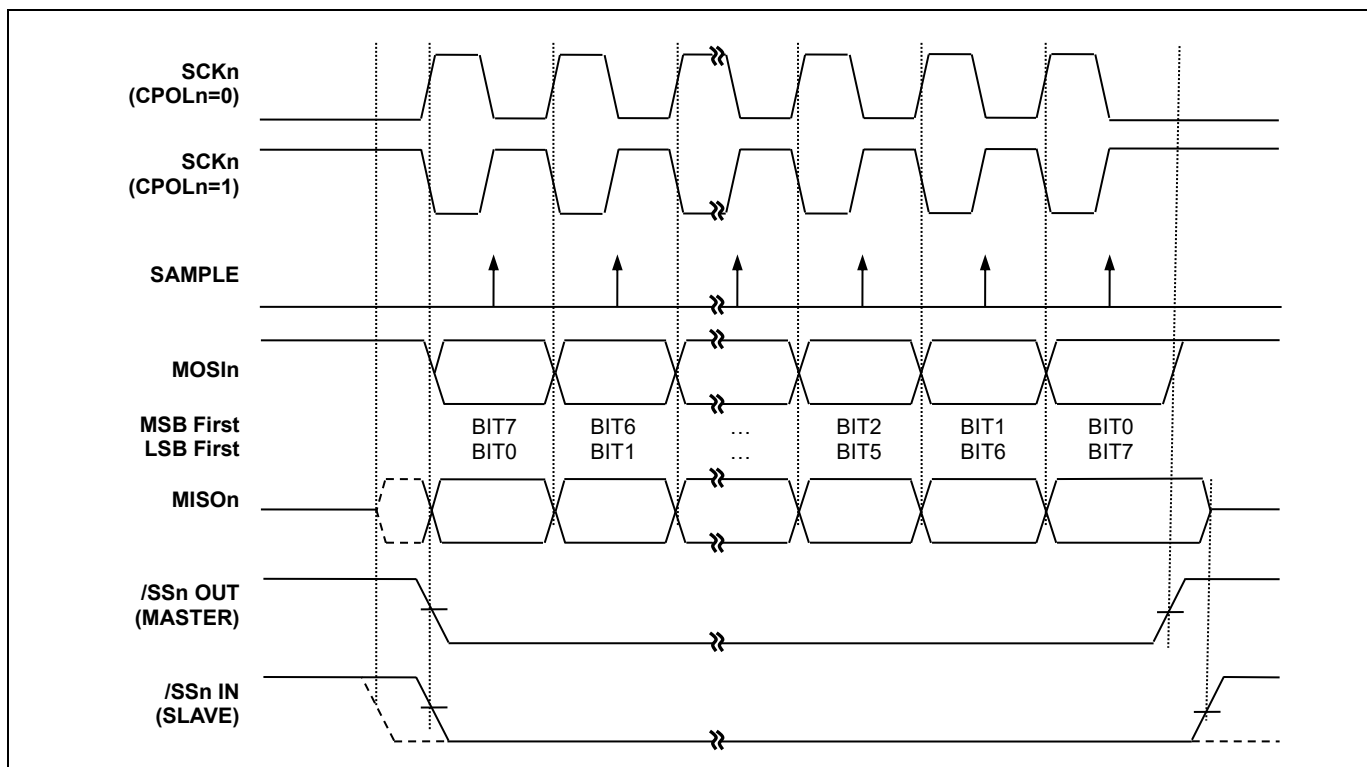


Figure 11.65 USIn SPI Clock Formats when CPHAn=1

When CPHAn=1, the slave begins to drive its MISOIn output when SSn goes active low, but the data is not defined until the first SCKn edge. The first SCKn edge shifts the first bit of data from the shifter onto the MOSIn output of the master and the MISOIn output of the slave. The next SCKn edge causes both the master and slave to sample the data bit value on their MISOIn and MOSIn inputs, respectively. At the third SCKn edge, the USIn shifts the second data bit value out to the MOSIn and MISOIn output of the master and slave respectively. When CPHAn=1, the slave's SSn input is not required to go to its inactive high level between transfers.

Because the SPI logic reuses the USIn resources, SPI mode of operation is similar to that of synchronous or asynchronous operation. An SPI transfer is initiated by checking for the USIn Data Register Empty flag (DREn=1) and then writing a byte of data to the USInDR Register. In master mode of operation, even if transmission is not enabled (TXEn=0), writing data to the USInDR register is necessary because the clock SCKn is generated from transmitter block.

11.12.13 USIn SPI Block Diagram

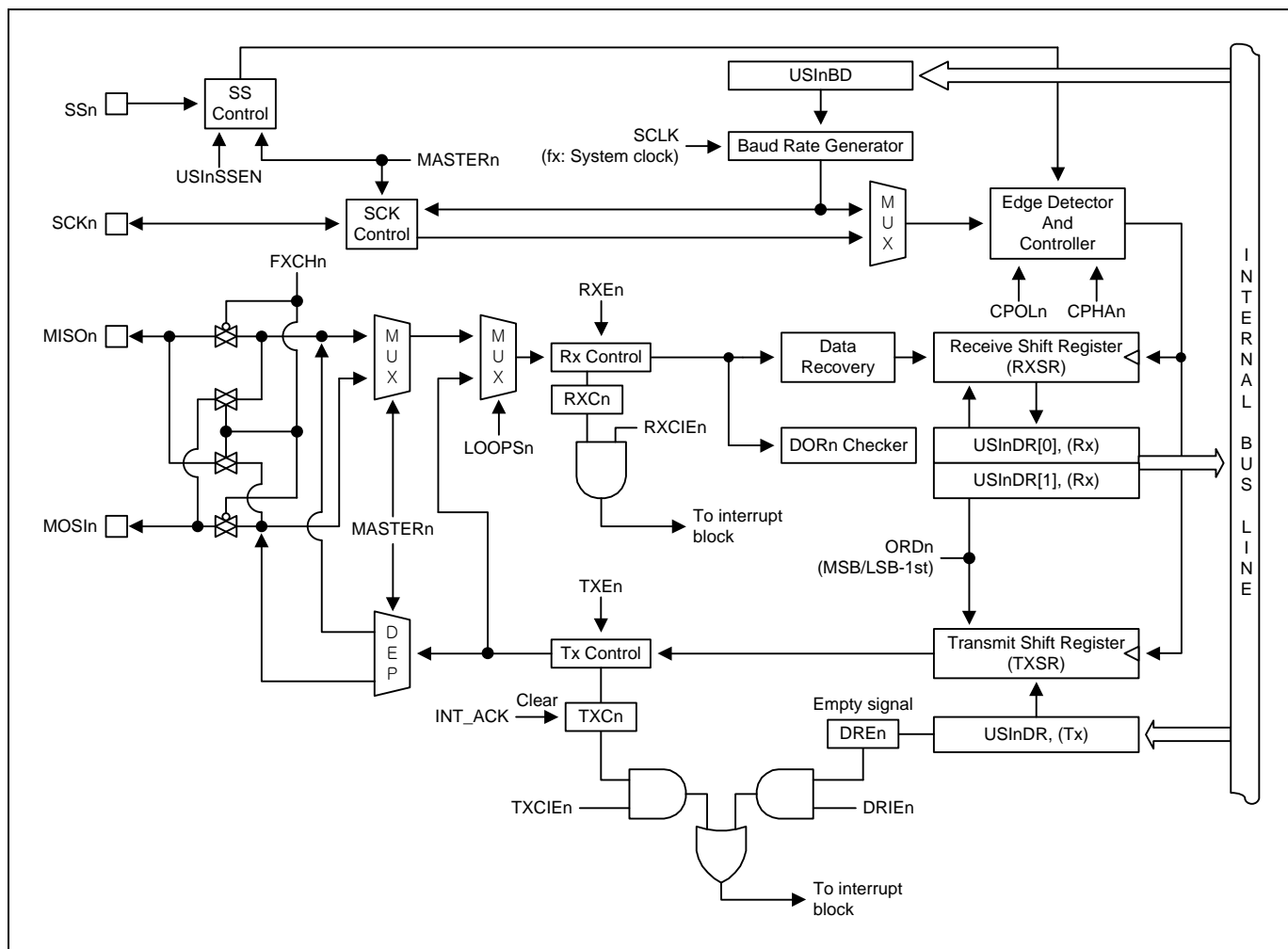


Figure 11.66 USIn SPI Block Diagram(n = 0, 1)



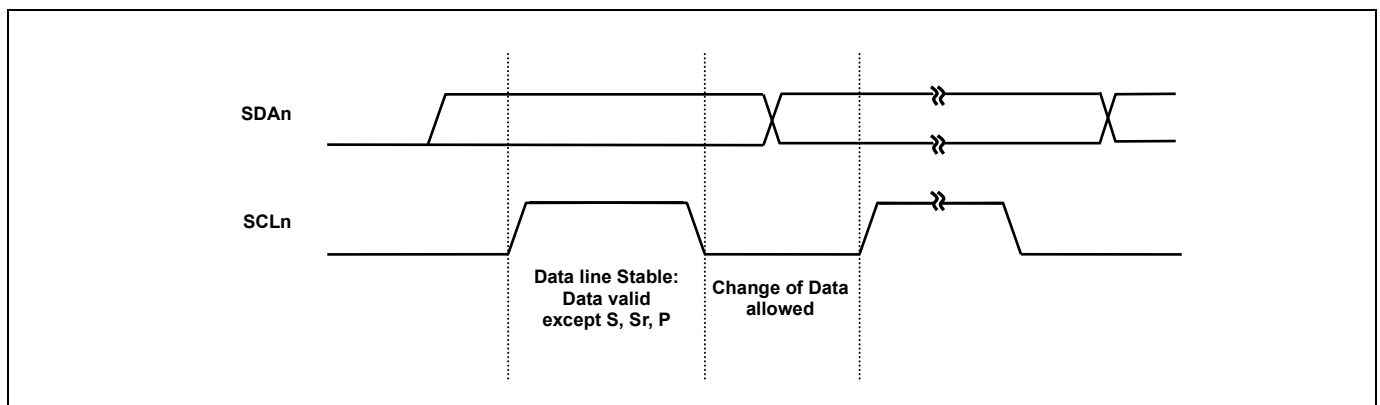
### 11.12.14 USIn I2C Mode

The USIn can be set to operate in industrial standard serial communication protocols mode. The I2C mode uses 2 bus lines serial data line (SDAn) and serial clock line (SCLn) to exchange data. Because both SDAn and SCLn lines are open-drain output, each line needs pull-up resistor. The features are as shown below.

- Compatible with I2C bus standard
- Multi-master operation
- Up to 400kHz data transfer read speed
- 7 bit address
- Both master and slave operation
- Bus busy detection

### 11.12.15 USIn I2C Bit Transfer

The data on the SDAn line must be stable during HIGH period of the clock, SCLn. The HIGH or LOW state of the data line can only change when the clock signal on the SCLn line is LOW. The exceptions are START(S), repeated START(Sr) and STOP(P) condition where data line changes when clock line is high.



**Figure 11.67** Bit Transfer on the I2C-Bus (USIn)

11.12.16 USIn I2C Start / Repeated Start / Stop

One master can issue a START (S) condition to notice other devices connected to the SCLn, SDAn lines that it will use the bus. A STOP (P) condition is generated by the master to release the bus lines so that other devices can use it. A high to low transition on the SDAn line while SCLn is high defines a START (S) condition. A low to high transition on the SDAn line while SCLn is high defines a STOP (P) condition. START and STOP conditions are always generated by the master. The bus is considered to be busy after START condition. The bus is considered to be free again after STOP condition, ie, the bus is busy between START and STOP condition. If a repeated START condition (Sr) is generated instead of STOP condition, the bus stays busy. So, the START and repeated START conditions are functionally identical.

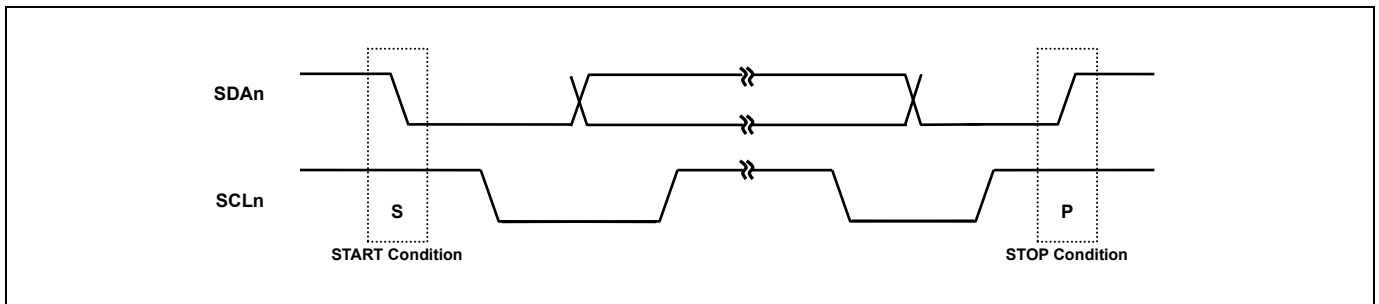


Figure 11.68 START and STOP Condition (USIn)

11.12.17 USIn I2C Data Transfer

Every byte put on the SDAn line must be 8-bits long. The number of bytes that can be transmitted per transfer is unlimited. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a slave can't receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCLn LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCLn.

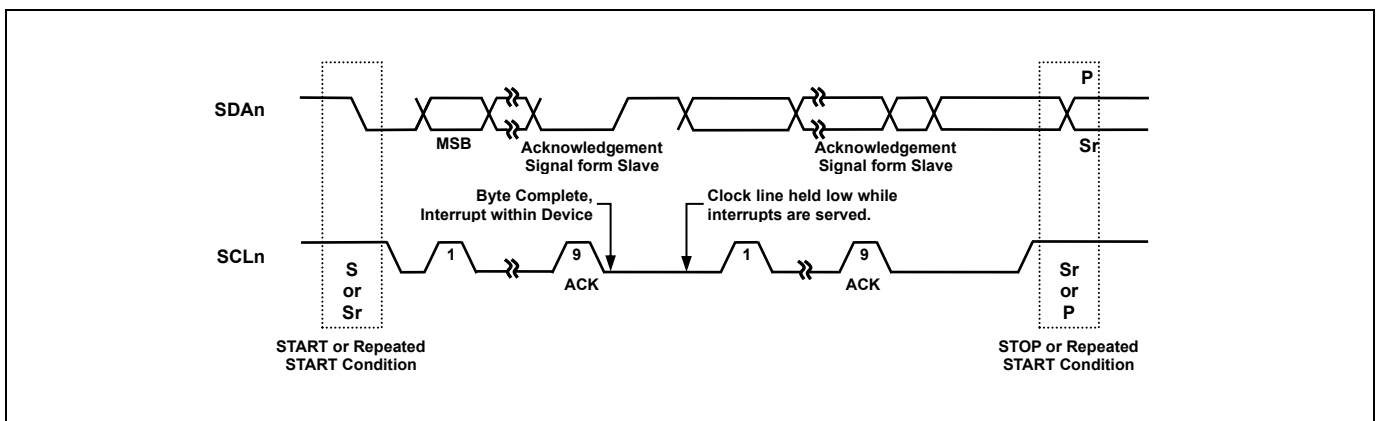


Figure 11.69 Data Transfer on the I2C-Bus (USIn)

11.12.18 USIn I2C Acknowledge

The acknowledge related clock pulse is generated by the master. The transmitter releases the SDAn line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDAn line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse. When a slave is addressed by a master (Address Packet) and if it is unable to receive or transmit because it's performing some real time function, the data line must be left HIGH by the slave. And also, when a slave addressed by a master is unable to receive more data bits, the slave receiver must release the SDAn line (Data Packet). The master can then generate either a STOP condition to abort the transfer or a repeated START condition to start a new transfer.

If a master receiver is involved in a transfer, it must signal the end of data to the slave transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave transmitter must release the data line to allow the master to generate a STOP or repeated START condition.

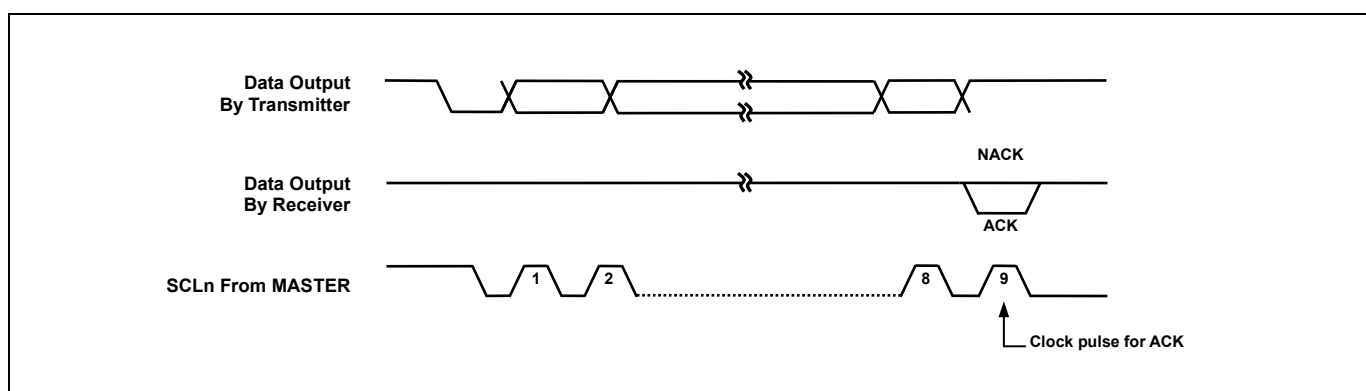


Figure 11.70 Acknowledge on the I2C-Bus (USIn)

11.12.19 USIn I2C Synchronization / Arbitration

Clock synchronization is performed using the wired-AND connection of I2C interfaces to the SCLn line. This means that a HIGH to LOW transition on the SCLn line will cause the devices concerned to start counting off their LOW period and it will hold the SCLn line in that state until the clock HIGH state is reached. However the LOW to HIGH transition of this clock may not change the state of the SCLn line if another clock is still within its LOW period. In this way, a synchronized SCLn clock is generated with its LOW period determined by the device with the longest clock LOW period and its HIGH period determined by the one with the shortest clock HIGH period.

A master may start a transfer only if the bus is free. Two or more masters may generate a START condition. Arbitration takes place on the SDAn line, while the SCLn line is at the HIGH level, in such a way that the master which transmits a HIGH level, while another master is transmitting a LOW level will switch off its DATA output state because the level on the bus doesn't correspond to its own level. Arbitration continues for many bits until a winning master gets the ownership of I2C bus. Its first stage is comparison of the address bits.

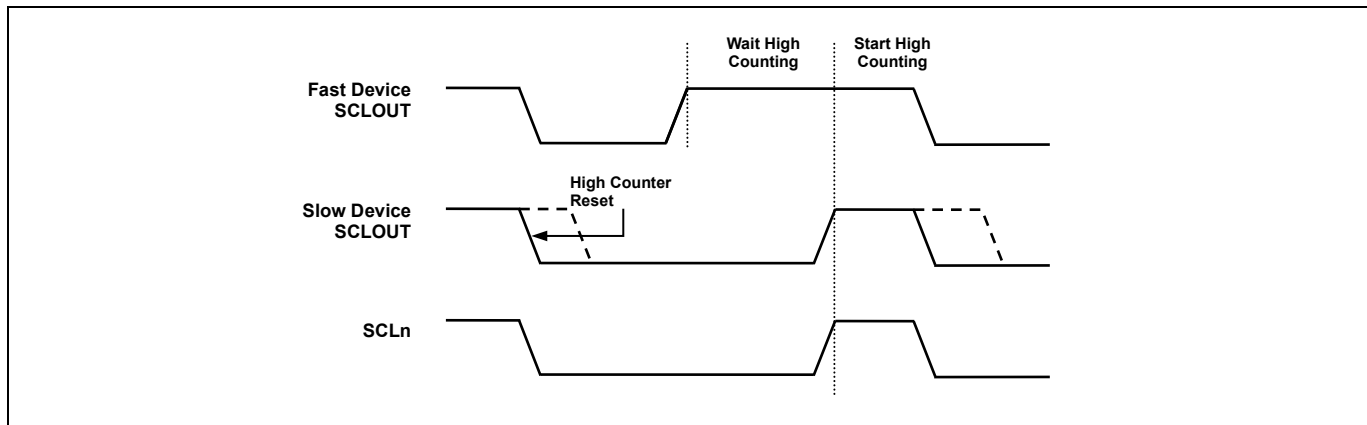


Figure 11.71 Clock Synchronization during Arbitration Procedure (USIn)

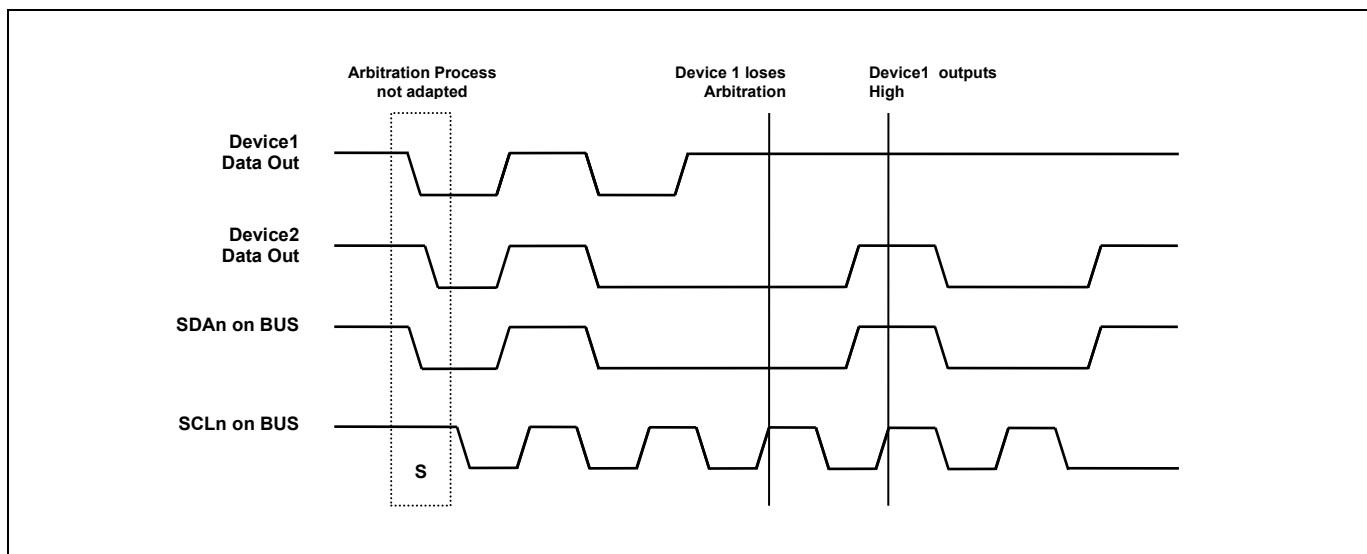


Figure 11.72 Arbitration Procedure of Two Masters (USIn)

### 11.12.20 USIn I2C Operation

The I2C is byte-oriented and interrupt based. Interrupts are issued after all bus events except for a transmission of a START condition. Because the I2C is interrupt based, the application software is free to execute other operations during a I2C byte transfer.

Note that when a I2C interrupt is generated, IICnIFR flag in USInCR4 register is set, it is cleared when all interrupt source bits in the USInST2 register are cleared to "0b". When I2C interrupt occurs, the SCLn line is hold LOW until clearing "0b" all interrupt source bits in USInST2 register. When the IICnIFR flag is set, the USInST2 contains a value indicating the current state of the I2C bus. According to the value in USInST2, software can decide what to do next.

I2C can operate in 4 modes by configuring master/slave, transmitter/receiver. The operating mode is configured by a winning master. A more detailed explanation follows below.

### 11.12.20.1 USIn I2C Master Transmitter

To operate I2C in master transmitter, follow the recommended steps below.

1. Enable I2C by setting USInMS[1:0]bits in USInCR1 and USInEN bit in USInCR2. This provides main clock to the peripheral.
2. Load SLAn+W into the USInDR where SLAn is address of slave device and W is transfer direction from the viewpoint of the master. For master transmitter, W is '0'. Note that USInDR is used for both address and data.
3. Configure baud rate by writing desired value to both USInSCLR and USInSCHR for the Low and High period of SCLn line.
4. Configure the USInSDHR to decide when SDAn changes value from falling edge of SCLn. If SDAn should change in the middle of SCLn LOW period, load half the value of USInSCLR to the USInSDHR.
5. Set the STARTCn bit in USInCR4. This transmits a START condition. And also configure how to handle interrupt and ACK signal. When the STARTCn bit is set, 8-bit data in USInDR is transmitted out according to the baud-rate.
6. This is ACK signal processing stage for address packet transmitted by master. When 7-bit address and 1-bit transfer direction is transmitted to target slave device, the master can know whether the slave acknowledged or not in the 9<sup>th</sup> high period of SCLn. If the master gains bus mastership, I2C generates GCALL interrupt regardless of the reception of ACK from the slave device. When I2C loses bus mastership during arbitration process, the MLOSTn bit in USInST2 is set and I2C waits in idle state or can be operate as an addressed slave. To operate as a slave when the MLOSTn bit in USInST2 is set, the ACKnEN bit in USInCR4 must be set and the received 7-bit address must equal to the USInSLA[6:0] bits in USInSAR. In this case I2C operates as a slave transmitter or a slave receiver (go to appropriate section). In this stage, I2C holds the SCLn LOW. This is because to decide whether I2C continues serial transfer or stops communication. The following steps continue assuming that I2C does not lose mastership during first data transfer.

I2C (Master) can choose one of the following cases regardless of the reception of ACK signal from slave.

- 1) Master receives ACK signal from slave, so continues data transfer because slave can receive more data from master. In this case, load data to transmit to USInDR.
- 2) Master stops data transfer even if it receives ACK signal from slave. In this case, set the STOPCn bit in USInCR4.
- 3) Master transmits repeated START condition with not checking ACK signal. In this case, load SLAn+R/W into the USInDR and set STARTCn bit in USInCR4.

After doing one of the actions above, clear to "0b" all interrupt source bits in USInST2 to release SCLn line. In case of 1), move to step 7. In case of 2), move to step 9 to handle STOP interrupt. In case of 3), move to step 6 after transmitting the data in USInDR and if transfer direction bit is '1' go to master receiver section.

7. 1-Byte of data is being transmitted. During data transfer, bus arbitration continues.

8. This is ACK signal processing stage for data packet transmitted by master. I2C holds the SCLn LOW. When I2C loses bus mastership while transmitting data arbitrating other masters, the MLOSTn bit in USInST2 is set. If then, I2C waits in idle state. When the data in USInDR is transmitted completely, I2C generates TENDn interrupt.

I2C can choose one of the following cases regardless of the reception of ACK signal from slave.

- 1) Master receives ACK signal from slave, so continues data transfer because slave can receive more data from master. In this case, load data to transmit to USInDR.
- 2) Master stops data transfer even if it receives ACK signal from slave. In this case, set the STOPCn bit in USInCR4.
- 3) Master transmits repeated START condition with not checking ACK signal. In this case, load SLAn+R/W into the USInDR and set the STARTCn bit in USInCR4.

After doing one of the actions above, clear to "0b" all interrupt source bits in USInST2 to release SCLn line. In case of 1), move to step 7. In case of 2), move to step 9 to handle STOP interrupt. In case of 3), move to step 6 after transmitting the data in USInDR and if transfer direction bit is '1' go to master receiver section.

9. This is the final step for master transmitter function of I2C, handling STOP interrupt. The STOP bit indicates that data transfer between master and slave is over. To clear USInST2, write "0" to USInST2. After this, I2C enters idle state.

### 11.12.20.2 USIn I2C Master Receiver

To operate I2C in master receiver, follow the recommended steps below.

1. Enable I2C by setting USInMS[1:0]bits in USInCR1 and USInEN bit in USInCR2. This provides main clock to the peripheral.
2. Load SLAn+R into the USInDR where SLA is address of slave device and R is transfer direction from the viewpoint of the master. For master receiver, R is '1'. Note that USInDR is used for both address and data.
3. Configure baud rate by writing desired value to both USInSCLR and USInSCHR for the Low and High period of SCLn line.
4. Configure the USInSDHR to decide when SDAn changes value from falling edge of SCLn. If SDAn should change in the middle of SCLn LOW period, load half the value of USInSCLR to the USInSDHR.
5. Set the STARTCn bit in USInCR4. This transmits a START condition. And also configure how to handle interrupt and ACK signal. When the STARTCn bit is set, 8-bit data in USInDR is transmitted out according to the baud-rate.
6. This is ACK signal processing stage for address packet transmitted by master. When 7-bit address and 1-bit transfer direction is transmitted to target slave device, the master can know whether the slave acknowledged or not in the 9<sup>th</sup> high period of SCLn. If the master gains bus mastership, I2C generates GCALL interrupt regardless of the reception of ACK from the slave device. When I2C loses bus mastership during arbitration process, the MLOSTn bit in USInST2 is set and I2C waits in idle state or can be operate as an addressed slave. To operate as a slave when the MLOSTn bit in USInST2 is set, the ACKnEN bit in USInCR4 must be set and the received 7-bit address must equal to the USInSLA[6:0] bits in USInSAR. In this case I2C operates as a slave transmitter or a slave receiver (go to appropriate section). In this stage, I2C holds the SCLn LOW. This is because to decide whether I2C continues serial transfer or stops communication. The following steps continue assuming that I2C does not lose mastership during first data transfer.

I2C (Master) can choose one of the following cases according to the reception of ACK signal from slave.

- 1) Master receives ACK signal from slave, so continues data transfer because slave can prepare and transmit more data to master. Configure ACKnEN bit in USInCR4 to decide whether I2C ACKnowledges the next data to be received or not.
- 2) Master stops data transfer because it receives no ACK signal from slave. In this case, set the STOPCn bit in USInCR4.
- 3) Master transmits repeated START condition due to no ACK signal from slave. In this case, load SLAn+R/W into the USInDR and set STARTCn bit in USInCR4.

After doing one of the actions above, clear to "0b" all interrupt source bits in USInST2 to release SCLn line. In case of 1), move to step 7. In case of 2), move to step 9 to handle STOP interrupt. In case of 3), move to step 6 after transmitting the data in USInDR and if transfer direction bit is '0' go to master transmitter section.

7. 1-Byte of data is being received.
8. This is ACK signal processing stage for data packet transmitted by slave. I2C holds the SCLn LOW. When 1-Byte of data is received completely, I2C generates TENDn interrupt.

I2C can choose one of the following cases according to the RXACKn flag in USInST2.

- 1) Master continues receiving data from slave. To do this, set ACKnEN bit in USInCR4 to ACKnowledge and the next data to be received.
- 2) Master wants to terminate data transfer when it receives next data by not generating ACK signal. This can be done by clearing ACKnEN bit in USInCR4.
- 3) Because no ACK signal is detected, master terminates data transfer. In this case, set the STOPCn bit in USInCR4.
- 4) No ACK signal is detected and master transmits repeated START condition. In this case, load SLAn+R/W into the USInDR and set the STARTCn bit in USInCR4.

After doing one of the actions above, clear to "0b" all interrupt source bits in USInST2 to release SCLn line. In case of 1) and 2), move to step 7. In case of 3), move to step 9 to handle STOP interrupt. In case of 4), move to step 6 after transmitting the data in USInDR and if transfer direction bit is '0' go to master transmitter section.

9. This is the final step for master receiver function of I2C, handling STOP interrupt. The STOP bit indicates that data transfer between master and slave is over. To clear USInST2, write "0" to USInST2. After this, I2C enters idle state.



### 11.12.20.3 USIn I2C Slave Transmitter

To operate I2C in slave transmitter, follow the recommended steps below.

1. If the main operating clock (SCLK) of the system is slower than that of SCLn, load value 0x00 into USInSDHR to make SDA<sub>n</sub> change within one system clock period from the falling edge of SCL<sub>n</sub>. Note that the hold time of SDA<sub>n</sub> is calculated by SDAH x period of SCLK where SDAH is multiple of number of SCLK coming from USInSDHR. When the hold time of SDA<sub>n</sub> is longer than the period of SCLK, I2C (slave) cannot transmit serial data properly.
2. Enable I2C by setting USInMS[1:0]bits in USInCR1 , IICnIE bit in USInCR4 and USInEN bit in USInCR2. This provides main clock to the peripheral.
3. When a START condition is detected, I2C receives one byte of data and compares it with USInSLA[6:0] bits in USInSAR. If the GCALL<sub>n</sub> bit in USInSAR is enabled, I2C compares the received data with value 0x00, the general call address.
4. If the received address does not equal to USInSLA[6:0] bits in USInSAR, I2C enters idle state ie, waits for another START condition. Else if the address equals to USInSLA[6:0] bits and the ACKnEN bit is enabled, I2C generates SSEL<sub>n</sub> interrupt and the SCL<sub>n</sub> line is held LOW. Note that even if the address equals to USInSLA[6:0] bits, when the ACKnEN bit is disabled, I2C enters idle state. When SSEL<sub>n</sub> interrupt occurs, load transmit data to USInDR and clear to "0b" all interrupt source bits in USInST2 to release SCL<sub>n</sub> line.
5. 1-Byte of data is being transmitted.
6. In this step, I2C generates TEND<sub>n</sub> interrupt and holds the SCL<sub>n</sub> line as LOW regardless of the reception of ACK signal from master. Slave can select one of the following cases.

1) No ACK signal is detected and I2C waits STOP or repeated START condition.

2) ACK signal from master is detected. Load data to transmit into USInDR.

After doing one of the actions above, clear to "0b" all interrupt source bits in USInST2 to release SCL<sub>n</sub> line. In case of 1) move to step 7 to terminate communication. In case of 2) move to step 5. In either case, a repeated START condition can be detected. For that case, move step 4.

7. This is the final step for slave transmitter function of I2C, handling STOP interrupt. The STOPC<sub>n</sub> bit indicates that data transfer between master and slave is over. To clear USInST2, write "0" to USInST2. After this, I2C enters idle state.

#### 11.12.20.4 USIn I2C Slave Receiver

To operate I2C in slave receiver, follow the recommended steps below.

1. If the main operating clock (SCLK) of the system is slower than that of SCLn, load value 0x00 into USInSDHR to make SDA<sub>n</sub> change within one system clock period from the falling edge of SCL<sub>n</sub>. Note that the hold time of SDA<sub>n</sub> is calculated by SDAH x period of SCLK where SDAH is multiple of number of SCLK coming from USInSDHR. When the hold time of SDA<sub>n</sub> is longer than the period of SCLK, I2C (slave) cannot transmit serial data properly.
2. Enable I2C by setting USInMS[1:0] bits in USInCR1, IICnIE bit in USInCR4 and USInEN bit in USInCR2. This provides main clock to the peripheral.
3. When a START condition is detected, I2C receives one byte of data and compares it with USInSLA[6:0] bits in USInSAR. If the GCALL<sub>n</sub> bit in USInSAR is enabled, I2C<sub>n</sub> compares the received data with value 0x00, the general call address.
4. If the received address does not equal to SLA<sub>n</sub> bits in USInSAR, I2C enters idle state ie, waits for another START condition. Else if the address equals to SLA<sub>n</sub> bits and the ACK<sub>n</sub>EN bit is enabled, I2C generates SSEL<sub>n</sub> interrupt and the SCL<sub>n</sub> line is held LOW. Note that even if the address equals to SLA<sub>n</sub> bits, when the ACK<sub>n</sub>EN bit is disabled, I2C enters idle state. When SSEL<sub>n</sub> interrupt occurs and I2C is ready to receive data, clear to "0b" all interrupt source bits in USInST2 to release SCL<sub>n</sub> line.
5. Byte of data is being received.
6. In this step, I2C generates TEND<sub>n</sub> interrupt and holds the SCL<sub>n</sub> line LOW regardless of the reception of ACK signal from master. Slave can select one of the following cases.
  - 1) No ACK signal is detected (ACK<sub>n</sub>EN=0) and I2C waits STOP or repeated START condition.
  - 2) ACK signal is detected (ACK<sub>n</sub>EN=1) and I2C can continue to receive data from master.

After doing one of the actions above, clear to "0b" all interrupt source bits in USInST2 to release SCL<sub>n</sub> line. In case of 1) move to step 7 to terminate communication. In case of 2) move to step 5. In either case, a repeated START condition can be detected. For that case, move step 4.

7. This is the final step for slave receiver function of I2C, handling STOP interrupt. The STOPC<sub>n</sub> bit indicates that data transfer between master and slave is over. To clear USInST2, write "0" to USInST2. After this, I2C enters idle state.

11.12.21 USIn I2C Block Diagram

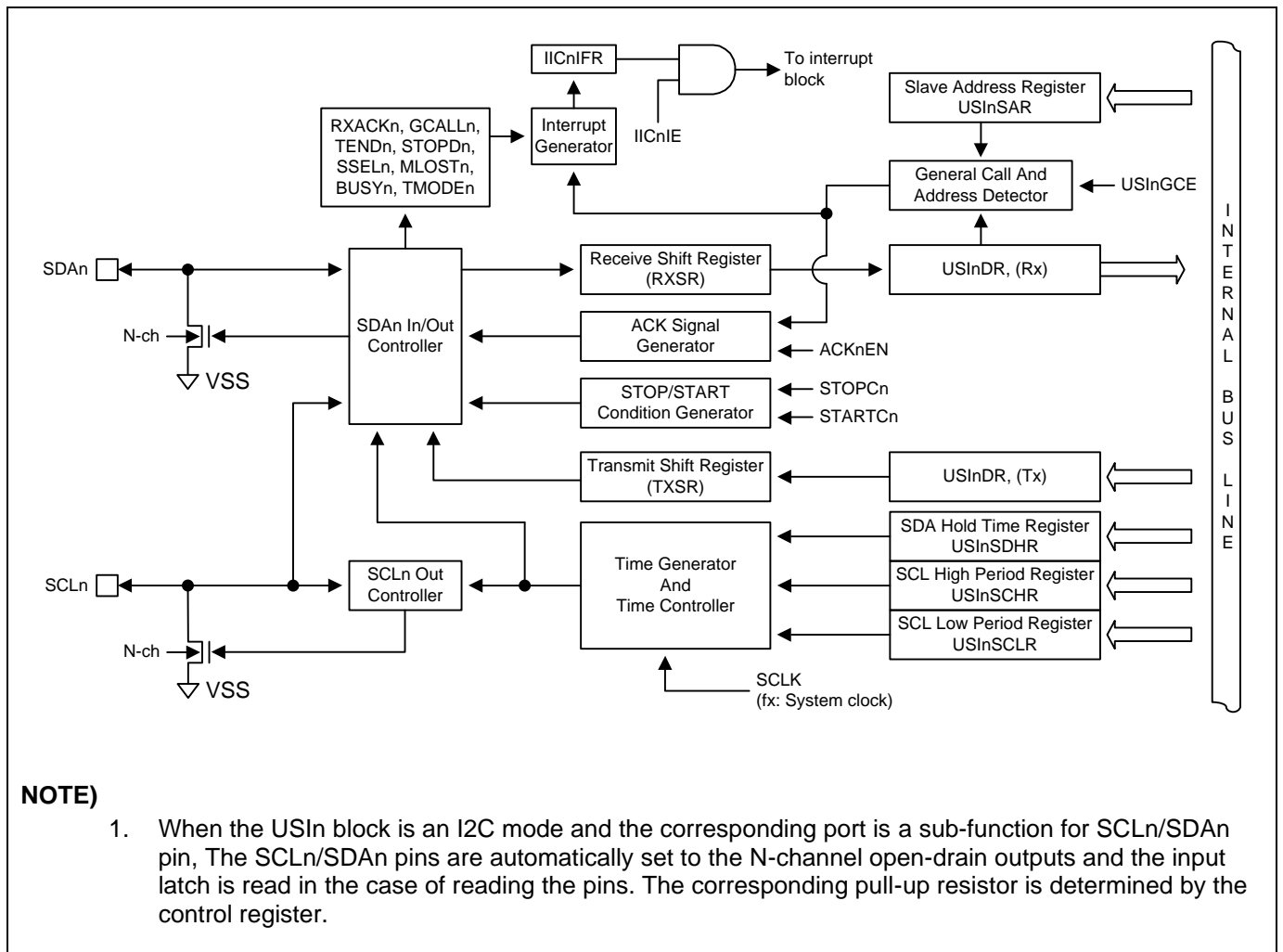


Figure 11.73 USIn I2C Block Diagram

**11.12.22 Register Map**

Name	Address	Direction	Default	Description
USI0BD	E3H	R/W	FFH	USI0 Baud Rate Generation Register
USI0DR	E5H	R/W	00H	USI0 Data Register
USI0SDHR	E4H	R/W	01H	USI0 SDA Hold Time Register
USI0SCHR	E7H	R/W	3FH	USI0 SCL High Period Register
USI0SCLR	E6H	R/W	3FH	USI0 SCL Low Period Register
USI0SAR	DDH	R/W	00H	USI0 Slave Address Register
USI0CR1	D9H	R/W	00H	USI0 Control Register 1
USI0CR2	DAH	R/W	00H	USI0 Control Register 2
USI0CR3	DBH	R/W	00H	USI0 Control Register 3
USI0CR4	DCH	R/W	00H	USI0 Control Register 4
USI0ST1	E1H	R/W	80H	USI0 Status Register 1
USI0ST2	E2H	R	00H	USI0 Status Register 2
USI1BD	F3H	R/W	FFH	USI1 Baud Rate Generation Register
USI1DR	F5H	R/W	00H	USI1 Data Register
USI1SDHR	F4H	R/W	01H	USI1 SDA Hold Time Register
USI1SCHR	F7H	R/W	3FH	USI1 SCL High Period Register
USI1SCLR	F6H	R/W	3FH	USI1 SCL Low Period Register
USI1SAR	EDH	R/W	00H	USI1 Slave Address Register
USI1CR1	E9H	R/W	00H	USI1 Control Register 1
USI1CR2	EAH	R/W	00H	USI1 Control Register 2
USI1CR3	EBH	R/W	00H	USI1 Control Register 3
USI1CR4	ECH	R/W	00H	USI1 Control Register 4
USI1ST1	F1H	R/W	80H	USI1 Status Register 1
USI1ST2	F2H	R	00H	USI1 Status Register 2

**Table 11.21** USI Register Map

**11.12.23 USIn Register Description**

USIn module consists of USIn baud rate generation register (USInBD), USIn data register (USInDR), USIn SDA hold time register (USInSDHR), USIn SCL high period register (USInSCHR), USIn SCL low period Register (USInSCLR), USIn slave address register (USInSAR), USIn control register 1/2/3/4 (USInCR1/2/3/4), USIn status register 1/2 (USInST1/2).

## 11.12.24 Register Description for USIn

**USInBD (USIn Baud- Rate Generation Register: For UART and SPI mode): E3H/F3H, n = 0, 1**

7	6	5	4	3	2	1	0
USInBD7	USInBD6	USInBD5	USInBD4	USInBD3	USInBD2	USInBD1	USInBD0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: FFH

**USInBD[7:0]** The value in this register is used to generate internal baud rate in asynchronous mode or to generate SCKn clock in SPI mode. To prevent malfunction, do not write '0' in asynchronous mode and do not write '0' or '1' in SPI mode.

**NOTE)**

1. In common with USInSAR register, USInBD register is used for slave address register when the USIn I2C mode.

**USInDR (USIn Data Register: For UART, SPI and I2C mode): E5H/F5H, n = 0, 1**

7	6	5	4	3	2	1	0
USInDR7	USInDR6	USInDR5	USInDR4	USInDR3	USInDR2	USInDR1	USInDR0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**USInDR[7:0]** The USIn transmit buffer and receive buffer share the same I/O address with this DATA register. The transmit data buffer is the destination for data written to the USInDR register. Reading the USInDR register returns the contents of the receive buffer.

Write to this register only when the DREn flag is set. In SPI master mode, the SCK clock is generated when data are written to this register.

**USInSDHR (USInSDA Hold Time Register: For I2C mode): E4H/F4H, n = 0, 1**

7	6	5	4	3	2	1	0
USInSDHR7	USInSDHR6	USInSDHR5	USInSDHR4	USInSDHR3	USInSDHR2	USInSDHR1	USInSDHR0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 01H

**USInSDHR[7:0]** The register is used to control SDAn output timing from the falling edge of SCI in I2C mode.

**NOTE)**

1. That SDAn is changed after  $t_{SCLK} \times (USInSDHR+2)$ , in master SDAn change in the middle of SCLn.
2. In slave mode, configure this register regarding the frequency of SCLn from master.
3. The SDAn is changed after  $t_{SCLK} \times (USInSDHR+2)$  in master mode. So, to insure operation in slave mode, the value
4.  $t_{SCLK} \times (USInSDHR+2)$  must be smaller than the period of SCL.

**USInSCHR (USInSCL High Period Register: For I2C mode): E7H/F7H, n = 0, 1**

7	6	5	4	3	2	1	0
USInSCHR7	USInSCHR6	USInSCHR5	USInSCHR4	USInSCHR3	USInSCHR2	USInSCHR1	USInSCHR0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 3FH

**USInSCHR[7:0]** This register defines the high period of SCLn when it operates in I2C master mode. The base clock is SCLK, the system clock and the period is calculated by the formula:  $t_{SCLK} \times (4 \times USInSCHR + 2)$  where  $t_{SCLK}$  is the period of SCLK.

So, the operating frequency of I2C master mode is calculated by the following equation.

$$f_{I2C} = \frac{1}{t_{SCLK} \times (4 \times (USInSCLR + USInSCHR) + 4)}$$

**USInSCLR (USInSCL Low Period Register: For I2C mode): E6H/F6H, n = 0, 1**

7	6	5	4	3	2	1	0
USInSCLR7	USInSCLR6	USInSCLR5	USInSCLR4	USInSCLR3	USInSCLR2	USInSCLR1	USInSCLR0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 3FH

**USInSCLR[7:0]** This register defines the high period of SCLn when it operates in I2C master mode. The base clock is SCLK, the system clock and the period is calculated by the formula:  $t_{SCLK} \times (4 \times USInSCLR + 2)$  where  $t_{SCLK}$  is the period of SCLK.

**USInSAR (USIn Slave Address Register: For I2C mode): DDH/EDH, n = 0, 1**

7	6	5	4	3	2	1	0
USInSLA6	USInSLA5	USInSLA4	USInSLA3	USInSLA2	USInSLA1	USInSLA0	USInGCE
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**USInSLA[6:0]** These bits configure the slave address of I2C when it operates in I2C slave mode.

**USInGCE** This bit decides whether I2C allows general call address or not in I2C slave mode.

0 Ignore general call address

1 Allow general call address

**USInCR1 (USIn Control Register 1: For UART, SPI and I2C mode): D9H/E9H, n = 0, 1**

7	6	5	4	3	2	1	0
USInMS1	USInMS0	USInPM1	USInPM0	USInS2	USInS1 ORDn	USInS0 CPHAn	CPOLn
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

- USInMS[1:0]** Selects operation mode of USIn
- |         |         |                          |
|---------|---------|--------------------------|
| USInMS1 | USInMS0 | Operation mode           |
| 0       | 0       | Asynchronous Mode (UART) |
| 0       | 1       | Synchronous Mode         |
| 1       | 0       | I2C mode                 |
| 1       | 1       | SPI mode                 |
- USInPM[1:0]** Selects parity generation and check methods (only UART mode)
- |         |         |             |
|---------|---------|-------------|
| USInPM1 | USInPM0 | Parity      |
| 0       | 0       | No Parity   |
| 0       | 1       | Reserved    |
| 1       | 0       | Even Parity |
| 1       | 1       | Odd Parity  |
- USInS[2:0]** When in asynchronous or synchronous mode of operation, selects the length of data bits in frame
- |        |        |        |             |
|--------|--------|--------|-------------|
| USInS2 | USInS1 | USInS0 | Data Length |
| 0      | 0      | 0      | 5 bit       |
| 0      | 0      | 1      | 6 bit       |
| 0      | 1      | 0      | 7 bit       |
| 0      | 1      | 1      | 8 bit       |
| 1      | 0      | 0      | Reserved    |
| 1      | 0      | 1      | Reserved    |
| 1      | 1      | 0      | Reserved    |
| 1      | 1      | 1      | 9 bit       |
- ORDn** This bit in the same bit position with USInS1. The MSB of the data byte is transmitted first when set to '1' and the LSB when set to '0' (only SPI mode)
- |   |           |
|---|-----------|
| 0 | LSB-first |
| 1 | MSB-first |
- CPHAn** This bit is in the same bit position with USInS0. This bit determines if data are sampled on the leading or trailing edge of SCKn (only SPI mode).
- |       |       |                  |                  |
|-------|-------|------------------|------------------|
| CPOLn | CPHAn | Leading edge     | Trailing edge    |
| 0     | 0     | Sample (Rising)  | Setup (Falling)  |
| 0     | 1     | Setup (Rising)   | Sample (Falling) |
| 1     | 0     | Sample (Falling) | Setup (Rising)   |
| 1     | 1     | Setup (Falling)  | Sample (Rising)  |
- CPOLn** This bit determines the clock polarity of ACK in synchronous or SPI mode.
- |   |   |
|---|---|
| 0 | TXD change @Rising Edge, RXD change @Falling Edge |
| 1 | TXD change @Falling Edge, RXD change @Rising Edge |



**USInCR2 (USIn Control Register 2: For UART, SPI and I2C mode): DAH/EAH, n = 0, 1**

7	6	5	4	3	2	1	0
DRIEn	TXCIEn	RXCIEn	WAKEIEn	TXEn	RXEn	USInEN	DBLSn
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

<b>DRIEn</b>	Interrupt enable bit for data register empty (only UART and SPI mode). 0 Interrupt from DREn is inhibited (use polling) 1 When DREn is set, request an interrupt
<b>TXCIEn</b>	Interrupt enable bit for transmit complete (only UART and SPI mode). 0 Interrupt from TXCn is inhibited (use polling) 1 When TXCn is set, request an interrupt
<b>RXCIEn</b>	Interrupt enable bit for receive complete (only UART and SPI mode). 0 Interrupt from RXCn is inhibited (use polling) 1 When RXCn is set, request an interrupt
<b>WAKEIEn</b>	Interrupt enable bit for asynchronous wake in STOP mode. When device is in stop mode, if RXDn goes to low level an interrupt can be requested to wake-up system. (only UART mode). At that time the DRIEn bit and USInST1 register value should be set to '0b' and "00H", respectively. 0 Interrupt from Wake is inhibited 1 When WAKEn is set, request an interrupt
<b>TXEn</b>	Enables the transmitter unit (only UART and SPI mode). 0 Transmitter is disabled 1 Transmitter is enabled
<b>RXEn</b>	Enables the receiver unit (only UART and SPI mode). 0 Receiver is disabled 1 Receiver is enabled
<b>USInEN</b>	Activate USIn function block by supplying. 0 USIn is disabled 1 USIn is enabled
<b>DBLSn</b>	This bit selects receiver sampling rate (only UART). 0 Normal asynchronous operation 1 Double Speed asynchronous operation

**USInCR3 (USIn Control Register 3: For UART, SPI and I2C mode): DBH/EBH, n = 0, 1**

7	6	5	4	3	2	1	0
MASTERn	LOOPSn	DISSCKn	USInSSEN	FXCHn	USInSB	USInTX8	USInRX8
RW	RW	RW	RW	RW	RW	RW	R

Initial value: 00H

- MASTERn** Selects master or slave in SPI and synchronous mode operation and controls the direction of SCKn pin
  - 0 Slave mode operation (External clock for SCKn).
  - 1 Master mode operation (Internal clock for SCKn).
- LOOPSn** Controls the loop back mode of USIn for test mode (only UART and SPI mode)
  - 0 Normal operation
  - 1 Loop Back mode
- DISSCKn** In synchronous mode of operation, selects the waveform of SCKn output
  - 0 ACK is free-running while UART is enabled in synchronous master mode
  - 1 ACK is active while any frame is on transferring
- USInSSEN** This bit controls the SSn pin operation (only SPI mode)
  - 0 Disable
  - 1 Enable (The SSn pin should be a normal input)
- FXCHn** SPI port function exchange control bit (only SPI mode)
  - 0 No effect
  - 1 Exchange MOSIn and MISOOn function
- USInSB** Selects the length of stop bit in asynchronous or synchronous mode of operation.
  - 0 1 Stop Bit
  - 1 2 Stop Bit
- USInTX8** The ninth bit of data frame in asynchronous or synchronous mode of operation. Write this bit first before loading the USInDR register
  - 0 MSB (9<sup>th</sup> bit) to be transmitted is '0'
  - 1 MSB (9<sup>th</sup> bit) to be transmitted is '1'
- USInRX8** The ninth bit of data frame in asynchronous or synchronous mode of operation. Read this bit first before reading the receive buffer (only UART mode).
  - 0 MSB (9<sup>th</sup> bit) received is '0'
  - 1 MSB (9<sup>th</sup> bit) received is '1'

USI0CR4 (USIn Control Register 4: For I2C mode): DCH/ECH, n = 0, 1

7	6	5	4	3	2	1	0
IICnIFR	–	TXDLYENBn	IICnIE	ACKnEN	IMASTERn	STOPCn	STARTCn
R	–	R/W	R/W	R/W	R	R/W	R/W

Initial value: 00H

- IICnIFR** This is an interrupt flag bit for I2C mode. When an interrupt occurs, this bit becomes ‘1’. This bit is cleared when all interrupt source bits in the USInST2 register are cleared to “0b”. Writing “1” has no effect.
  - 0 I2C interrupt no generation
  - 1 I2C interrupt generation
- TXDLYENBn** USInSDHR register control bit
  - 0 Enable USInSDHR register
  - 1 Disable USInSDHR register
- IICnIE** Interrupt Enable bit for I2C mode
  - 0 Interrupt from I2C is inhibited (use polling)
  - 1 Enable interrupt for I2C
- ACKnEN** Controls ACK signal Generation at ninth SCLn period.
  - 0 No ACK signal is generated (SDAn =1)
  - 1 ACK signal is generated (SDAn =0)

**NOTE) ACK signal is output (SDA =0) for the following 3 cases.**

  - 1. When received address packet equals to USInSLA bits in USInSAR.
  - 2. When received address packet equals to value 0x00 with GCALLn enabled.
  - 3. When I2C operates as a receiver (master or slave)
- IMASTERn** Represent operating mode of I2C
  - 0 I2C is in slave mode
  - 1 I2C is in master mode
- STOPCn** When I2C is master, STOP condition generation
  - 0 No effect
  - 1 STOP condition is to be generated
- STARTCn** When I2C is master, START condition generation
  - 0 No effect
  - 1 START or repeated START condition is to be generated

**USInST1 (USIn Status Register 1: For UART and SPI mode): E1H/F1H, n = 0, 1**

7	6	5	4	3	2	1	0
DREn	TXCn	RXCn	WAKEn	USInRST	DORn	FEn	PEn
RW	RW	R	RW	RW	R	RW	RW

Initial value: 80H

- DREn**      The DREn flag indicates if the transmit buffer (USInDR) is ready to receive new data. If DREn is '1', the buffer is empty and ready to be written. This flag can generate a DREn interrupt.

  - 0      Transmit buffer is not empty.
  - 1      Transmit buffer is empty.
  
- TXCn**      This flag is set when the entire frame in the transmit shift register has been shifted out and there is no new data currently present in the transmit buffer. This flag is automatically cleared when the interrupt service routine of a TXCn interrupt is executed. This flag can generate a TXCn interrupt. This bit is automatically cleared.

  - 0      Transmission is ongoing.
  - 1      Transmit buffer is empty and the data in transmit shift register are shifted out completely.
  
- RXCn**      This flag is set when there are unread data in the receive buffer and cleared when all the data in the receive buffer are read. The RXCn flag can be used to generate a RXCn interrupt.

  - 0      There is no data unread in the receive buffer
  - 1      There are more than 1 data in the receive buffer
  
- WAKEn**      This flag is set when the RXDn pin is detected low while the CPU is in STOP mode. This flag can be used to generate a WAKEn interrupt. This bit is set only when in asynchronous mode of operation. This bit should be cleared by program software. (only UART mode)

  - 0      No WAKE interrupt is generated.
  - 1      WAKE interrupt is generated
  
- USInRST**    This is an internal reset and only has effect on USIn. Writing '1' to this bit initializes the internal logic of USIn and this bit is automatically cleared to '0'.

  - 0      No operation
  - 1      Reset USIn
  
- DORn**      This bit is set if a Data Overrun occurs. While this bit is set, the incoming data frame is ignored. This flag is valid until the receive buffer is read.

  - 0      No Data Overrun
  - 1      Data Overrun detected
  
- FEn**        This bit is set if the first stop bit of next character in the receive buffer is detected as '0'. This bit is valid until the receive buffer is read. (only UART mode)

  - 0      No Frame Error
  - 1      Frame Error detected
  
- PEn**        This bit is set if the next character in the receive buffer has a Parity Error to be received while Parity Checking is enabled. This bit is valid until the receive buffer is read. (only UART mode)

  - 0      No Parity Error
  - 1      Parity Error detected

## USInST2 (USIn Status Register 2: For I2C mode): E2H/F2H, n = 0, 1

7	6	5	4	3	2	1	0
GCALLn	TENDn	STOPDn	SSELn	MLOSTn	BUSYn	TMODEn	RXACKn
RW	RW	RW	RW	RW	RW	R	RW

Initial value: 00H

- GCALLn** This bit has different meaning depending on whether I2C is master or slave. When I2C is a master, this bit represents whether it received AACK (address ACK) from slave.
- 0 No AACK is received (Master mode)
  - 1 AACK is received (Master mode)
- When I2C is a slave, this bit is used to indicated general call.
- 0 General call address is not detected (Slave mode)
  - 1 General call address is detected (Slave mode)
- TENDn** This bit is set when 1-byte of data is transferred completely
- 0 1 byte of data is not completely transferred
  - 1 1 byte of data is completely transferred
- STOPDn** This bit is set when a STOP condition is detected.
- 0 No STOP condition is detected
  - 1 STOP condition is detected
- SSELn** This bit is set when I2C is addressed by other master.
- 0 I2C is not selected as a slave
  - 1 I2C is addressed by other master and acts as a slave
- MLOSTn** This bit represents the result of bus arbitration in master mode.
- 0 I2C maintains bus mastership
  - 1 I2C maintains bus mastership during arbitration process
- BUSYn** This bit reflects bus status.
- 0 I2C bus is idle, so a master can issue a START condition
  - 1 I2C bus is busy
- TMODEn** This bit is used to indicate whether I2C is transmitter or receiver.
- 0 I2C is a receiver
  - 1 I2C is a transmitter
- RXACKn** This bit shows the state of ACK signal
- 0 No ACK is received
  - 1 ACK is received at ninth SCL period

**NOTE)**

1. The GCALLn, TENDn, STOPDn, SSELn, and MLOSTn bits can be source of interrupt.
2. When an I2C interrupt occurs except for STOP mode, the SCLn line is hold LOW. To release SCLn, Clear to "0b" all interrupt source bits in USInST2 register.
3. The GCALLn, TENDn, STOPDn, SSELn, MLOSTn, and RXACKn bits are cleared when "0b" is written to the corresponding bit.

11.12.25 Baud Rate setting (example)

Baud Rate (bps)	fx=1.00MHz		fx=1.8432MHz		fx=2.00MHz	
	USI0BD/USI1BD	ERROR	USI0BD/USI1BD	ERROR	USI0BD/USI1BD	ERROR
2400	25	0.2%	47	0.0%	51	0.2%
4800	12	0.2%	23	0.0%	25	0.2%
9600	6	-7.0%	11	0.0%	12	0.2%
14.4k	3	8.5%	7	0.0%	8	-3.5%
19.2k	2	8.5%	5	0.0%	6	-7.0%
28.8k	1	8.5%	3	0.0%	3	8.5%
38.4k	1	-18.6%	2	0.0%	2	8.5%
57.6k	-	-	1	-25.0%	1	8.5%
76.8k	-	-	1	0.0%	1	-18.6%
115.2k	-	-	-	-	-	-
230.4k	-	-	-	-	-	-

Baud Rate (bps)	fx=1.00MHz		fx=1.8432MHz		fx=2.00MHz	
	USI0BD/USI1BD	ERROR	USI0BD/USI1BD	ERROR	USI0BD/USI1BD	ERROR
2400	25	0.2%	47	0.0%	51	0.2%
4800	12	0.2%	23	0.0%	25	0.2%
9600	6	-7.0%	11	0.0%	12	0.2%
14.4k	3	8.5%	7	0.0%	8	-3.5%
19.2k	2	8.5%	5	0.0%	6	-7.0%
28.8k	1	8.5%	3	0.0%	3	8.5%
38.4k	1	-18.6%	2	0.0%	2	8.5%
57.6k	-	-	1	-25.0%	1	8.5%
76.8k	-	-	1	0.0%	1	-18.6%
115.2k	-	-	-	-	-	-
230.4k	-	-	-	-	-	-

Baud Rate (bps)	fx=8.00MHz	
	USI0BD/USI1BD	ERROR
2400	207	0.2%
4800	103	0.2%
9600	51	0.2%
14.4k	34	-0.8%
19.2k	25	0.2%
28.8k	16	2.1%
38.4k	12	0.2%
57.6k	8	-3.5%
76.8k	6	-7.0%
115.2k	3	8.5%
230.4k	1	8.5%
250k	1	0.0%
0.5M	-	-
1M	-	-

Table 11.22 Examples of USI0BD and USI1BD Settings for Commonly Used Oscillator Frequencies

## 11.13 LCD Driver

### 11.13.1 Overview

The LCD driver is controlled by the LCD Control Register (LCDCRH/L). The LCLK[1:0] determines the frequency of COM signal scanning of each segment output. A RESET clears the LCD control register LCDCRH and LCDCRL values to logic '0'.

The LCD display can continue operating during IDLE and STOP modes if a sub-frequency clock is used as LCD clock source.

### 11.13.2 LCD Display RAM Organization

Display data are stored to the display data area in the external data memory.

The display data which stored to the display external data area (address 0000H-001AH) are read automatically and sent to the LCD driver by the hardware. The LCD driver generates the segment signals and common signals in accordance with the display data and drive method. Therefore, display patterns can be changed by only overwriting the contents of the display external data area with a program.

Figure 11-99 shows the correspondence between the display external data area and the COM/SEG pins. The LCD is turned on when the display data is “1” and turned off when “0”.

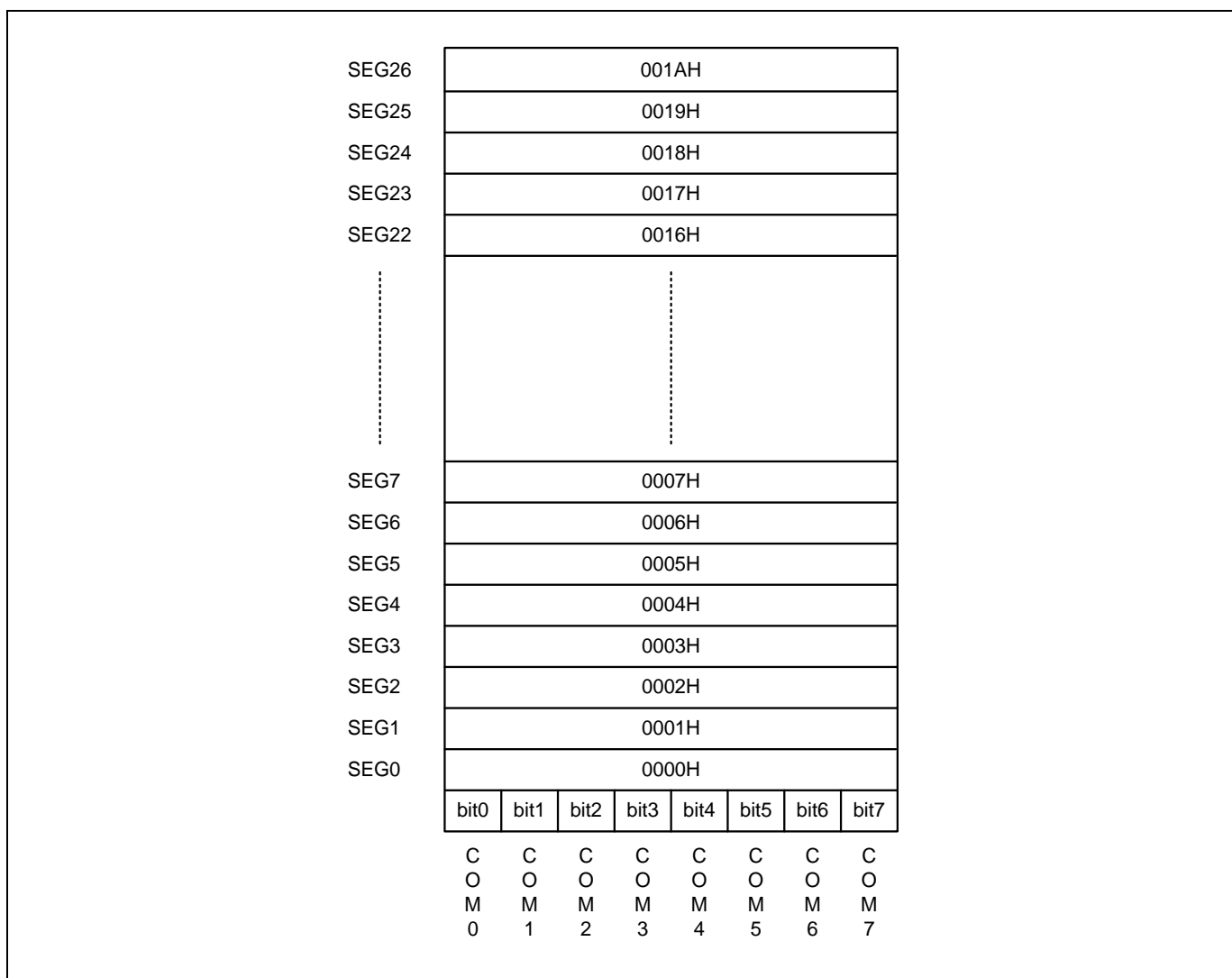


Figure 11.74 LCD Circuit Block Diagram



11.13.3 LCD Signal Waveform

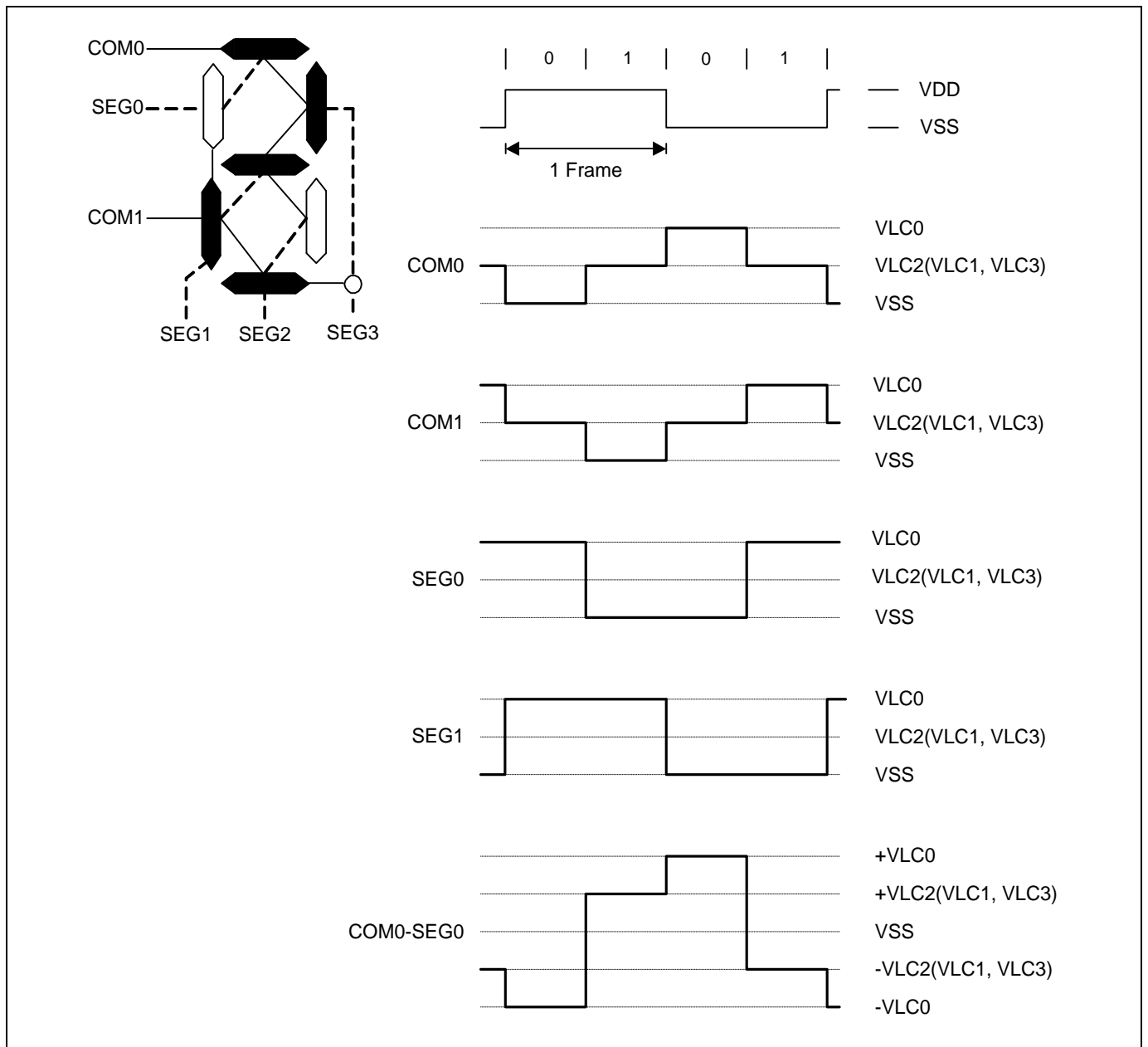


Figure 11.75 LCD Signal Waveforms (1/2Duty, 1/2Bias)

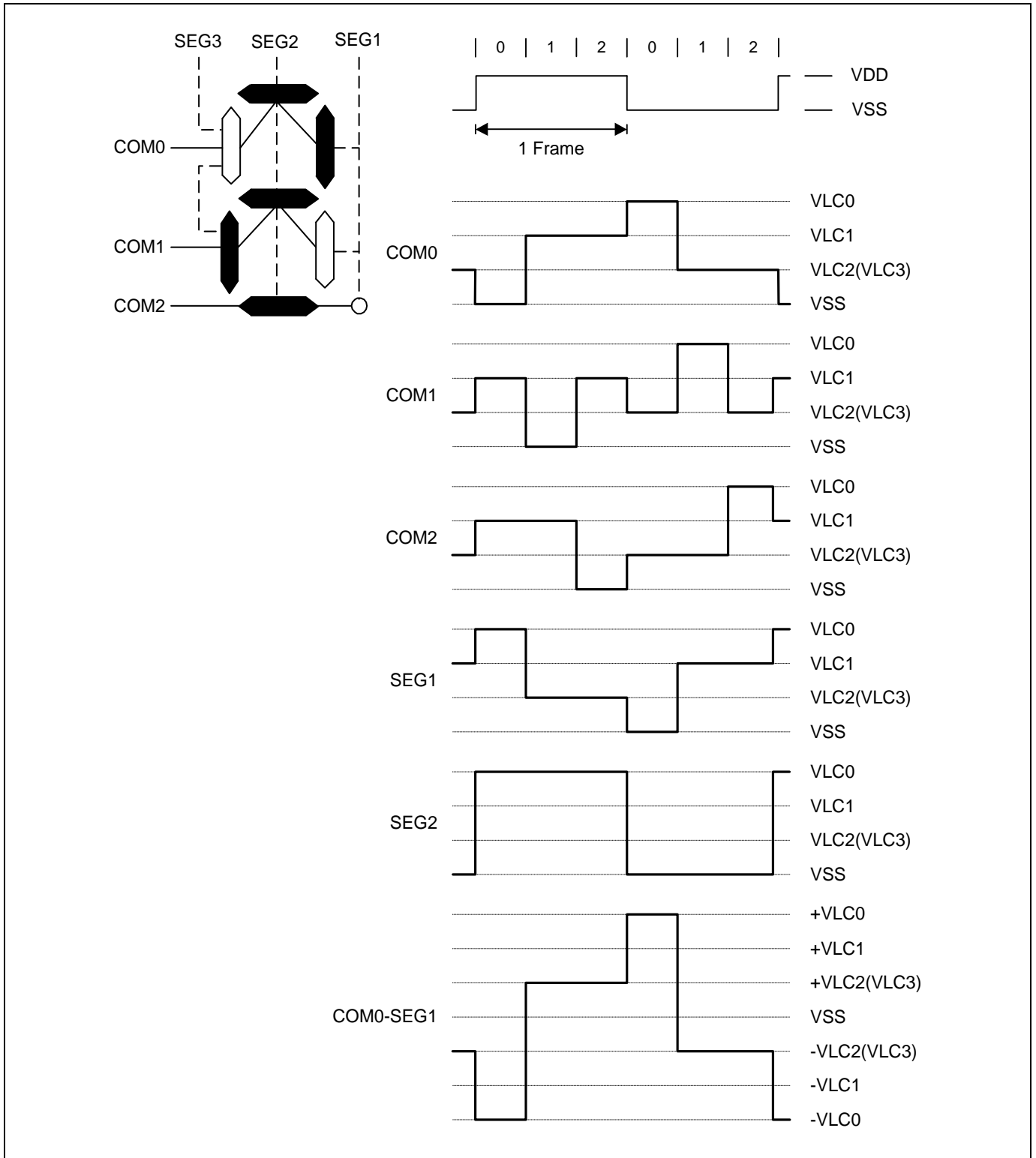


Figure 11.76 LCD Signal Waveforms (1/3Duty, 1/3Bias)

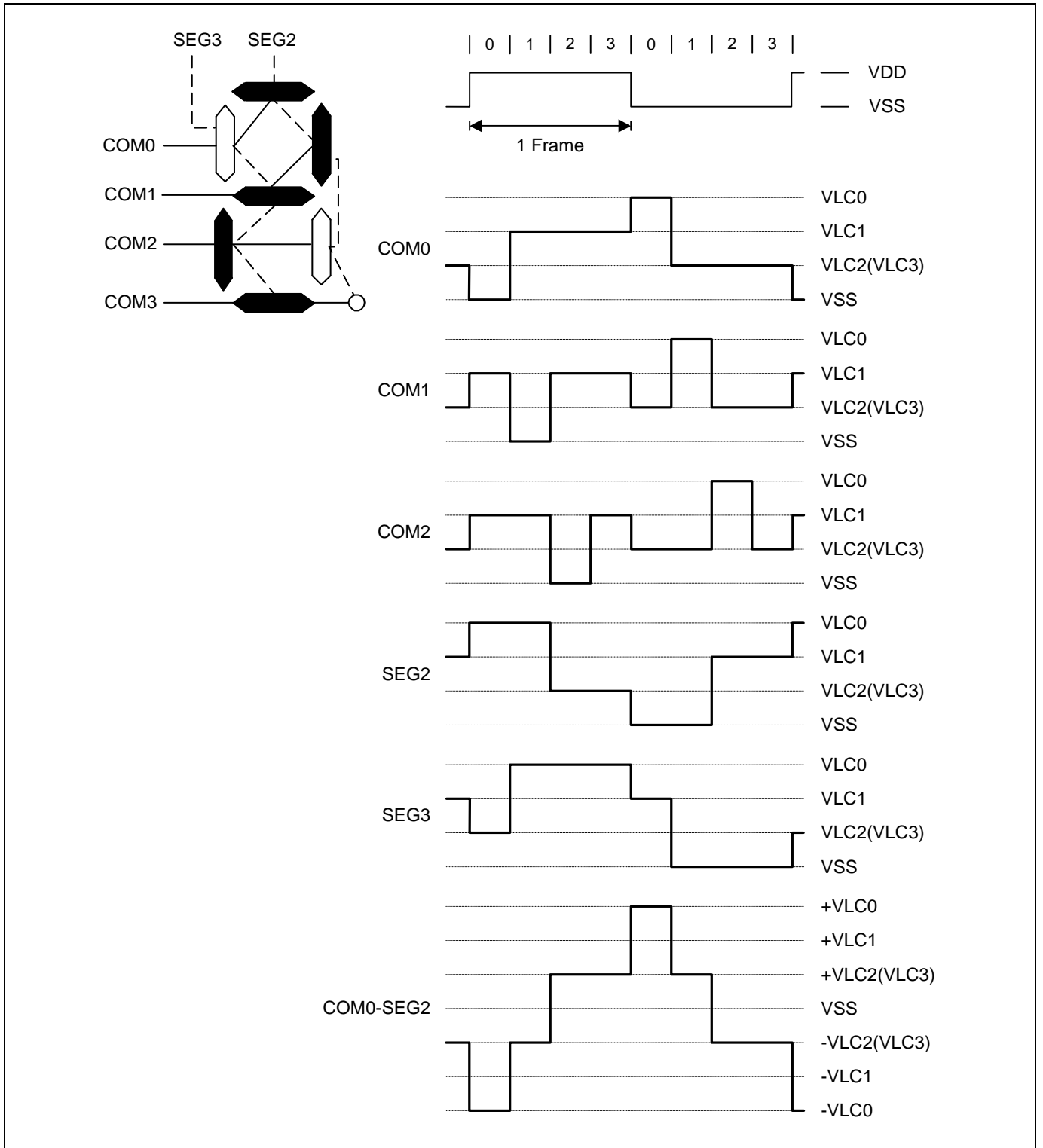


Figure 11.77 LCD Signal Waveforms (1/4Duty, 1/3Bias)

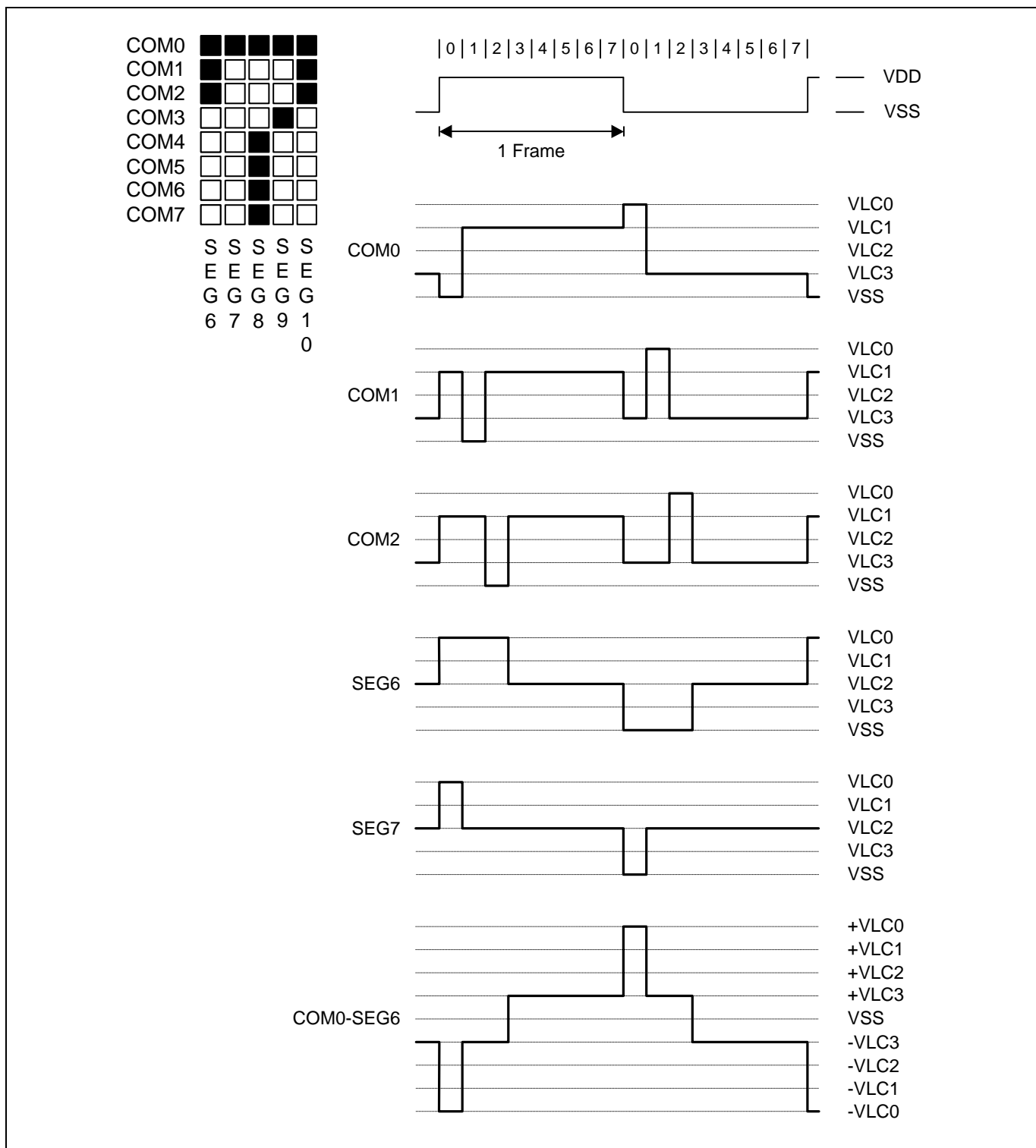


Figure 11.78 LCD Signal Waveforms (1/8Duty, 1/4Bias)

11.13.4 LCD Voltage Dividing Resistor Connection

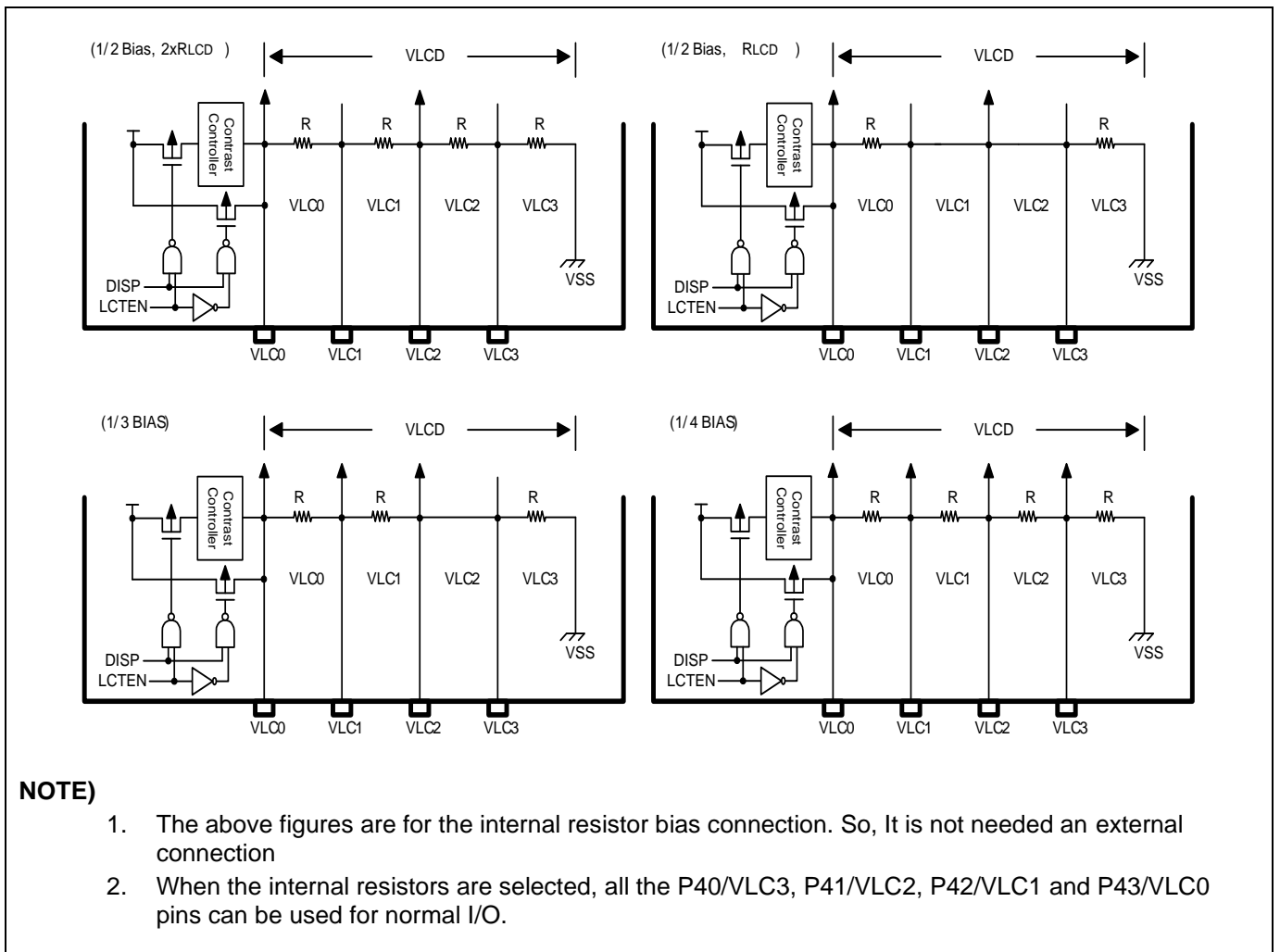
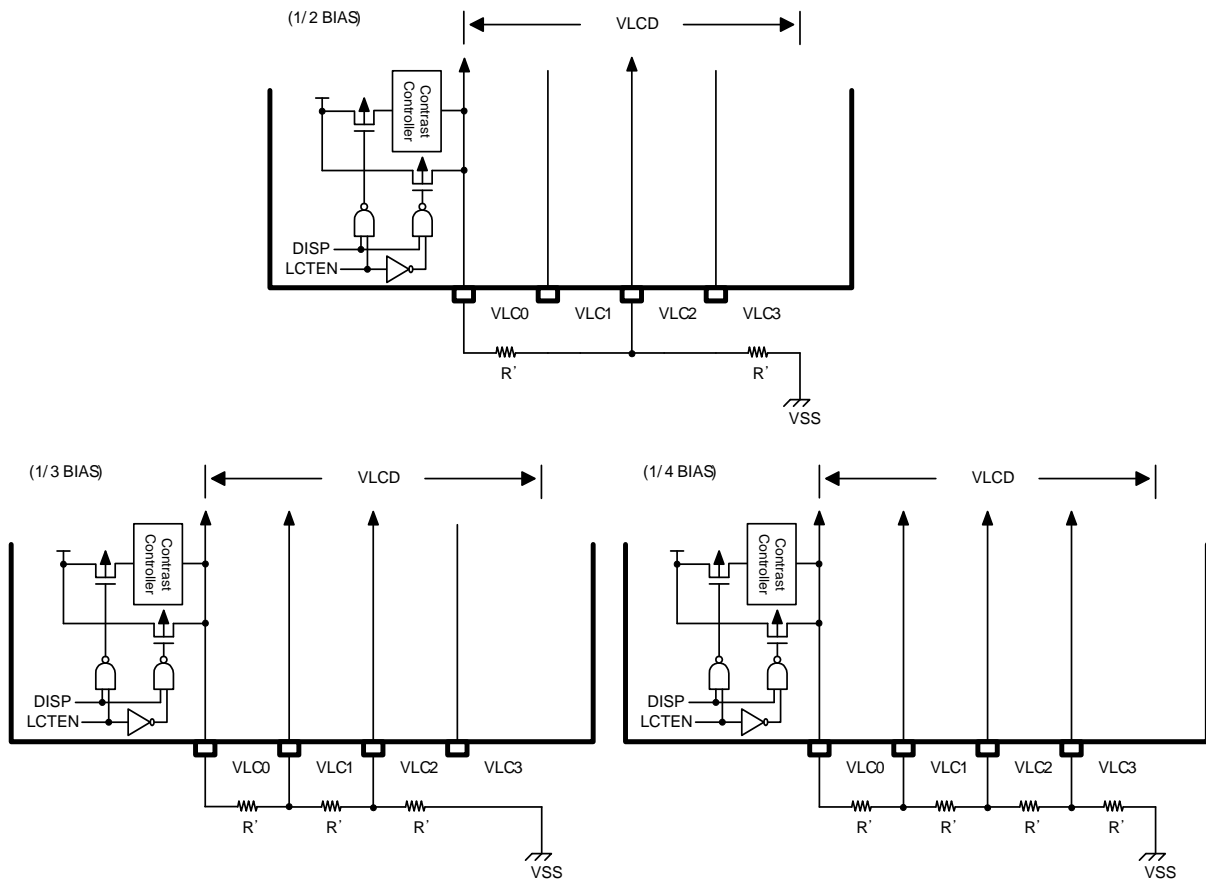


Figure 11.79 Internal Resistor Bias Connection



**NOTE)**

1. When the external resistor bias is selected, the internal resistors for bias are disconnected.
2. When the external resistor bias is selected, the dividing resistors should be connected like the above figure and the needed bias pins should be selected as the LCD bias function pins (VLC0, VLC1, VLC2 and VLC3) by P4FSR register.
3. When it is 1/2 bias, the P43/VLC0 and P41/VLC2 pins should be selected as VLC0 and VLC2 functions. The other pins can be used for normal I/O.
4. When it is 1/3 bias, the P43/VLC0, P42/VLC1 and P41/VLC2 pins should be selected as VLC0, VLC1 and VLC2 functions. Another pin can be used for normal I/O.
5. When it is 1/4 bias, the P43/VLC0, P42/VLC1, P41/VLC2 and P40/VLC3 pins should be selected as VLC0, VLC1, VLC2 and VLC3 functions

**Figure 11.80** External Resistor Bias Connection

11.13.5 Block Diagram

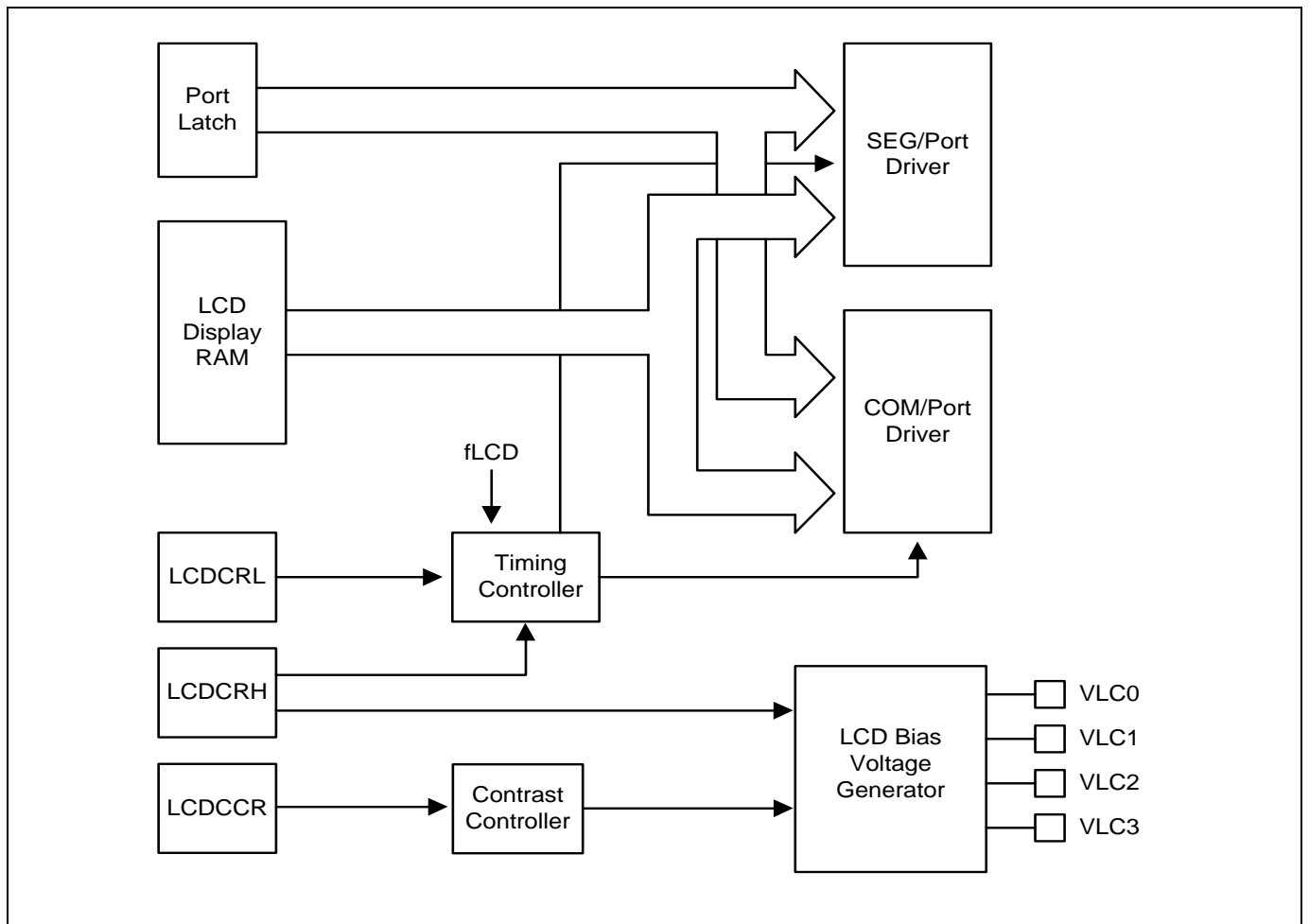


Figure 11.81 LCD Circuit Block Diagram

11.13.6 Register Map

Name	Address	Direction	Default	Description
LCDCRH	9AH	R/W	00H	LCD Driver Control High Register
LDCRHL	99H	R/W	00H	LCD Driver Control Low Register
LCDCCR	9BH	R/W	00H	LCD Driver Contrast Control Register

Table 11.23 LCD Register Map

11.13.7 LCD Driver Register Description

LCD driver register has two control registers, LCD driver control high register (LCDCRH), LCD driver control low register (LDCRHL) and LCD driver contrast control register (LCDCCR).

11.13.8 Register Description for LCD Driver

LCDCRH (LCD Driver Control High Register): 9AH

7	6	5	4	3	2	1	0
–	–	–	COMCHG	–	–	LCDDR	DISP
–	–	–	RW	–	–	RW	RW

Initial value: 00H

**COMCHG** Common Signal Output Port Change Control  
 0 COM0 – COM3 signals are outputted through the P37-P34  
 1 COM0 – COM3 signals are outputted through the P33-P30

**NOTE)**

1. The COM0/COM1/COM2/COM3 signals can be outputted through the P33/P32/P31/P30, respectively.
2. For example, the COM0 signal may be outputted to P33 pin if the P3FSR.3 is “1b” and the COMCHG bit is “1b”.
3. Refer to the port3 function selection register (P3FSR).
4. Available only below the 1/4 duty.

**LCDDR** LCD Driving Resistor for Bias Select  
 0 Internal LCD driving resistors for bias  
 1 External LCD driving resistors for bias

**DISP** LCD Display Control  
 0 Display off  
 1 Normal display on



**LCDCR1 (LCD Driver Control Low Register): 99H**

7	6	5	4	3	2	1	0
IRSEL	–	DBS3	DBS2	DBS1	DBS0	LCLK1	LCK0
RW	–	R/W	R/W	R/W	R/W	R/W	R/W

Initial value: 00H

- IRSEL** Internal LCD Bias Dividing Resistor Select
  - 0  $R_{LCD} = 60k\Omega (R_{LCD1})$
  - 1  $R_{LCD} = 120k\Omega (R_{LCD2})$
- DBS[3:0]** LCD Duty and Bias Select (NOTE)
 

DBS3	DBS2	DBS1	DBS0	Description
0	0	0	0	1/8Duty, 1/4Bias, $R_{LCD}$
0	0	0	1	1/6Duty, 1/4Bias, $R_{LCD}$
0	0	1	0	1/5Duty, 1/3Bias, $R_{LCD}$
0	0	1	1	1/4Duty, 1/3Bias, $R_{LCD}$
0	1	0	0	1/3Duty, 1/3Bias, $R_{LCD}$
0	1	0	1	1/3Duty, 1/2Bias, $R_{LCD}$
0	1	1	0	1/3Duty, 1/2Bias, $2xR_{LCD}$
0	1	1	1	1/2Duty, 1/2Bias, $R_{LCD}$
1	0	0	0	1/2Duty, 1/2Bias, $2xR_{LCD}$

Other values Not available
- LCLK[1:0]** LCD Clock Select (When  $f_{wck}$ (Watch timer clock)= 32.768kHz)
 

LCLK1	LCLK0	Description
0	0	$f_{LCD} = 128Hz$
0	1	$f_{LCD} = 256Hz$
1	0	$f_{LCD} = 512Hz$
1	1	$f_{LCD} = 1024Hz$

**NOTE)**

1. The LCD clock is generated by watch timer clock ( $f_{wck}$ ). So the watch timer should be enabled when the LCD display is turned on.

LCD Clock Frequency ( $f_{LCD}$ )	LCD Frame Frequency ( $f_{FRAME}$ )						Unit
	1/2 Duty	1/3 Duty	1/4 Duty	1/5 Duty	1/6 Duty	1/8 Duty	
128	64	43	32	26	21	16	Hz
256	128	85	64	51	43	32	
512	256	171	128	102	85	64	
1024	512	341	256	205	171	128	

**Table 11.24** LCD Frame Frequency

The LCD frame frequency is calculated by the following formula:

$$LCD \text{ Frame Frequency } (f_{FRAME}) = f_{LCD} \times \text{Duty Hz}$$

Ex) In case of 1/4 duty and  $f_{LCD}=512Hz$ ,  $f_{FRAME} = f_{LCD} \times 1/4 = 512 \times 1/4 = 128Hz$

**LCDCCR (LCD Driver Contrast Control Low Register): 9BH**

7	6	5	4	3	2	1	0
LCTEN	–	–	–	VLCD3	VLCD	VLCD1	VLCD0
RW	–	–	–	RW	RW	RW	RW

Initial value: 00H

**LCTEN** Control LCD Driver Contrast  
 0 LCD Driver Contrast disable  
 1 LCD Driver Contrast enable

**VLCD[3:0]** VLC0 Voltage Control when the contrast is enabled

VLCD3	VLCD 2	VLCD 1	VLCD 0	Description
0	0	0	0	VLC0 = VDD x 16/31 step
0	0	0	1	VLC0 = VDD x 16/30 step
0	0	1	0	VLC0 = VDD x 16/29 step
0	0	1	1	VLC0 = VDD x 16/28 step
0	1	0	0	VLC0 = VDD x 16/27 step
0	1	0	1	VLC0 = VDD x 16/26 step
0	1	1	0	VLC0 = VDD x 16/25 step
0	1	1	1	VLC0 = VDD x 16/24 step
1	0	0	0	VLC0 = VDD x 16/23 step
1	0	0	1	VLC0 = VDD x 16/22 step
1	0	1	0	VLC0 = VDD x 16/21 step
1	0	1	1	VLC0 = VDD x 16/20 step
1	1	0	0	VLC0 = VDD x 16/19 step
1	1	0	1	VLC0 = VDD x 16/18 step
1	1	1	0	VLC0 = VDD x 16/17 step
1	1	1	1	VLC0 = VDD x 16/16 step

**NOTE) The LCD contrast step is based on 1/4 bias and R<sub>LCD</sub>=60kΩ.**

1. 1/4 bias : VDD x 16/(31 – VLC[3:0]) when R<sub>LCD</sub>= 60kΩ  
 VDD x 32/(47 – VLC[3:0]) when R<sub>LCD</sub>= 120kΩ
2. 1/3 bias : VDD x 12/(27 – VLC[3:0]) when R<sub>LCD</sub>= 60kΩ  
 VDD x 24/(39 – VLC[3:0]) when R<sub>LCD</sub>= 120kΩ
3. 1/2 bias : VDD x 8/(23 – VLC[3:0]) when R<sub>LCD</sub>= 60kΩ  
 VDD x 16/(31 – VLC[3:0]) when R<sub>LCD</sub>= 120kΩ

## 12 Power Down Operation

### 12.1 Overview

The MC96F6432A has two power-down modes to minimize the power consumption of the device. In power down mode, power consumption is reduced considerably. The device provides three kinds of power saving functions, Main-IDLE, Sub-IDLE and STOP mode. In three modes, program is stopped.

### 12.2 Peripheral Operation in IDLE/STOP Mode

Peripheral	IDLE Mode	STOP Mode
CPU	ALL CPU Operation are Disable	ALL CPU Operation are Disable
RAM	Retain	Retain
Basic Interval Timer	Operates Continuously	Stop
Watch Dog Timer	Operates Continuously	Stop (Can be operated with WDTRC OSC)
Watch Timer	Operates Continuously	Stop (Can be operated with sub clock)
Timer0~4	Operates Continuously	Halted (Only when the Event Counter Mode is Enabled, Timer operates Normally)
ADC	Operates Continuously	Stop
BUZ	Operates Continuously	Stop
SPI	Operates Continuously	Only operate with external clock
USI0/1	Operates Continuously	Only operate with external clock
LCD Controller	Operates Continuously	Stop (Can be operated with sub clock)
Internal OSC (16MHz)	Oscillation	Stop when the system clock (fx) is fIRC
WDTRC OSC (5kHz)	Can be operated with setting value	Can be operated with setting value
Main OSC (0.4~8.5MHz)	Oscillation	Stop when fx = fXIN
Sub OSC (32.768kHz)	Oscillation	Stop when fx = fSUB
I/O Port	Retain	Retain
Control Register	Retain	Retain
Address Data Bus	Retain	Retain
Release Method	By RESET, all Interrupts	By RESET, Timer Interrupt (EC0, EC1, EC3), SPI (External clock), External Interrupt, UART by RX, WT (sub clock), WDT

**Table 12.1** Peripheral Operation during Power Down Mode

### 12.3 IDLE Mode

The power control register is set to '01h' to enter the IDLE Mode. In this mode, the internal oscillation circuits remain active. Oscillation continues and peripherals are operated normally but CPU stops. It is released by reset or interrupt. To be released by interrupt, interrupt should be enabled before IDLE mode. If using reset, because the device becomes initialized state, the registers have reset value.

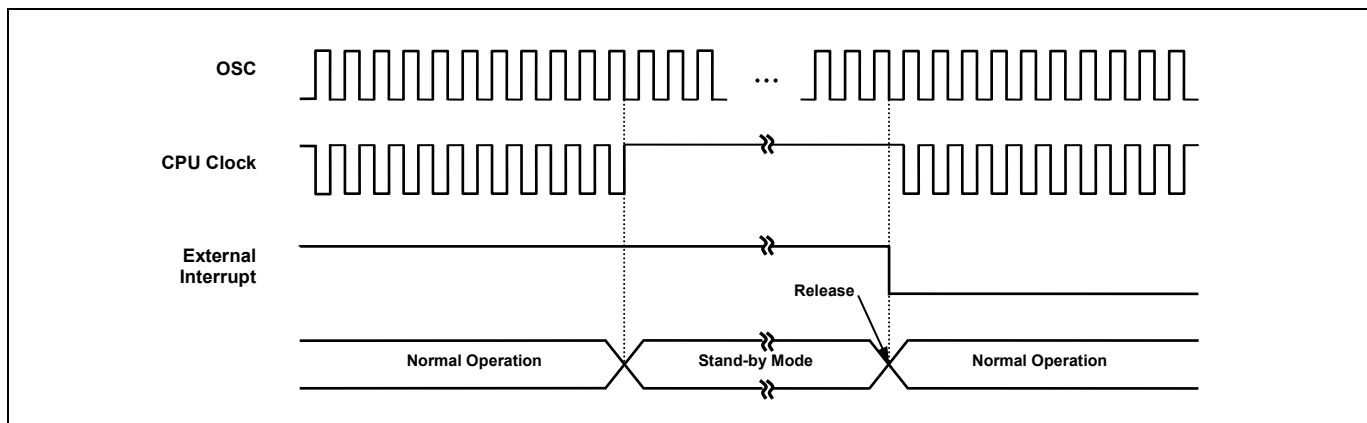


Figure 12.1 IDLE Mode Release Timing by External Interrupt

## 12.4 STOP Mode

The power control register is set to '03H' to enter the STOP Mode. In the stop mode, the selected oscillator, system clock and peripheral clock is stopped, but watch timer can be continued to operate with sub clock. With the clock frozen, all functions are stopped, but the on-chip RAM and control registers are held. For example, If the internal RC oscillator ( $f_{IRC}$ ) is selected for the system clock and the sub clock ( $f_{SUB}$ ) is oscillated, the internal RC oscillator stops oscillation and the sub clock is continuously oscillated in stop mode. At that time, the watch timer and LCD controller can be operated with the sub clock.

The source for exit from STOP mode is hardware reset and interrupts. The reset re-defines all the control registers. When exit from STOP mode, enough oscillation stabilization time is required to normal operation. Figure 12.2 shows the timing diagram. When released from STOP mode, the Basic interval timer is activated on wake-up. Therefore, before STOP instruction, user must be set its relevant prescale divide ratio to have long enough time. This guarantees that oscillator has started and stabilized.

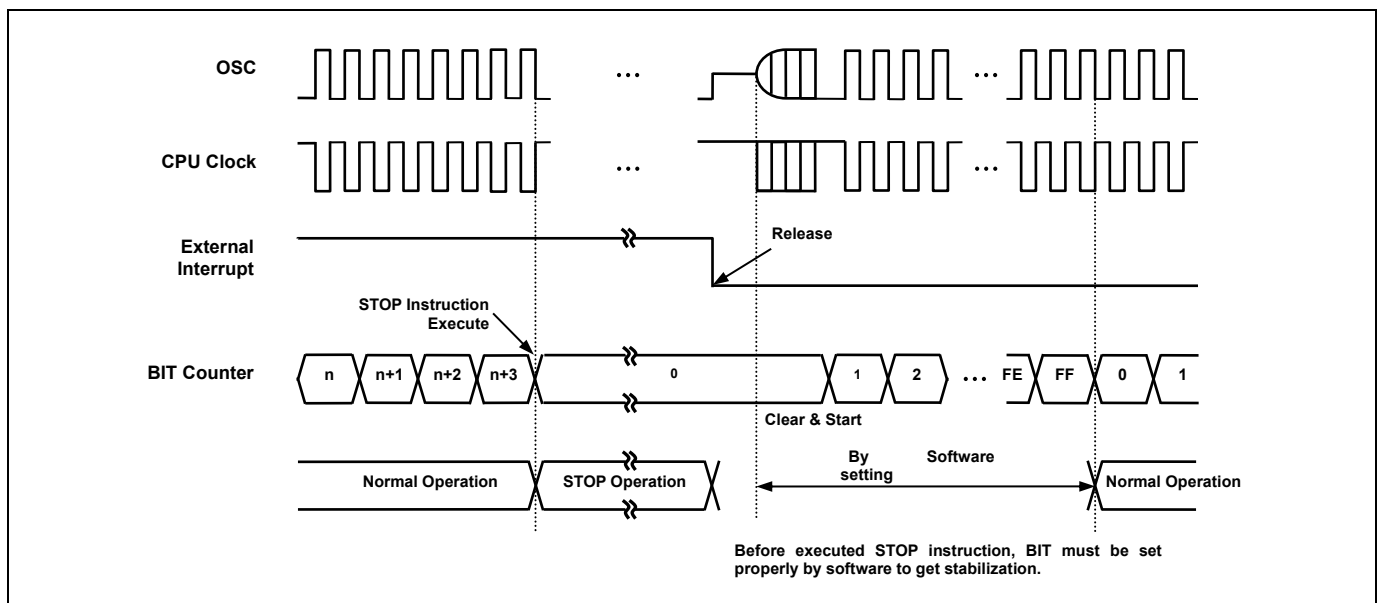


Figure 12.2 STOP Mode Release Timing by External Interrupt

### 12.5 Release Operation of STOP Mode

After STOP mode is released, the operation begins according to content of related interrupt register just before STOP mode start (Figure 12.3). If the global interrupt Enable Flag (IE.EA) is set to '1', the STOP mode is released by the interrupt which each interrupt enable flag = '1' and the CPU jumps to the relevant interrupt service routine. Even if the IE.EA bit is cleared to '0', the STOP mode is released by the interrupt of which the interrupt enable flag is set to '1'.

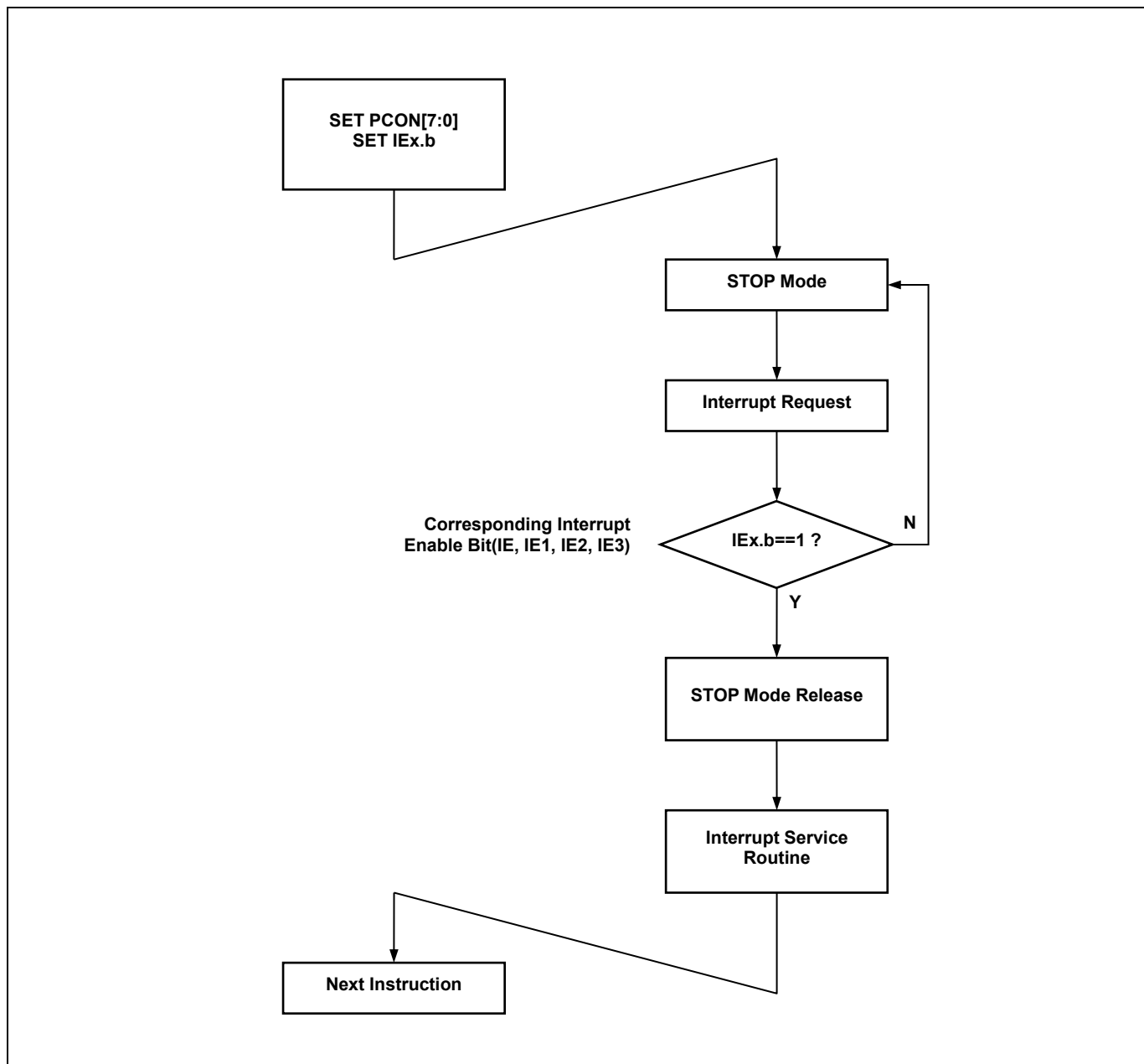


Figure 12.3 STOP Mode Release Flow

## 12.6 Register Map

Name	Address	Direction	Default	Description
PCON	87H	R/W	00H	Power Control Register

Table 12.2 Power Down Operation Register Map

## 12.7 Power Down Operation Register Description

The power down operation register consists of the power control register (PCON).

## 12.8 Register Description for Power Down Operation

PCON (Power Control Register): 87H

7	6	5	4	3	2	1	0
PCON7	–	–	–	PCON3	PCON2	PCON1	PCON0
RW	–	–	–	RW	RW	RW	RW

Initial value: 00H

**PCON[7:0]** Power Control  
 01H IDLE mode enable  
 03H STOP mode enable  
 Other Values Normal operation

### NOTE)

- To enter IDLE mode, PCON must be set to '01H'.
- To enter STOP mode, PCON must be set to '03H'.
- The PCON register is automatically cleared by a release signal in STOP/IDLE mode.
- Three or more NOP instructions must immediately follow the instruction that make the device enter STOP/IDLE mode. Refer to the following examples.

Ex1) MOV PCON, #01H ; IDLE mode  
 NOP  
 NOP  
 NOP  
 •  
 •  
 •

Ex2) MOV PCON, #03H ; STOP mode  
 NOP  
 NOP  
 NOP  
 •  
 •  
 •

# 13 RESET

## 13.1 Overview

The following is the hardware setting value.

On Chip Hardware	Initial Value
Program Counter (PC)	0000h
Accumulator	00h
Stack Pointer (SP)	07h
Peripheral Clock	On
Control Register	Refer to the Peripheral Registers

Table 13.1 Reset State

## 13.2 Reset Source

The MC96F6432A has five types of reset sources. The following is the reset sources.

- External RESETB
- Power ON RESET (POR)
- WDT Overflow Reset (In the case of WDTEN = `1`)
- Low Voltage Reset (In the case of LVREN = `0`)

## 13.3 RESET Block Diagram

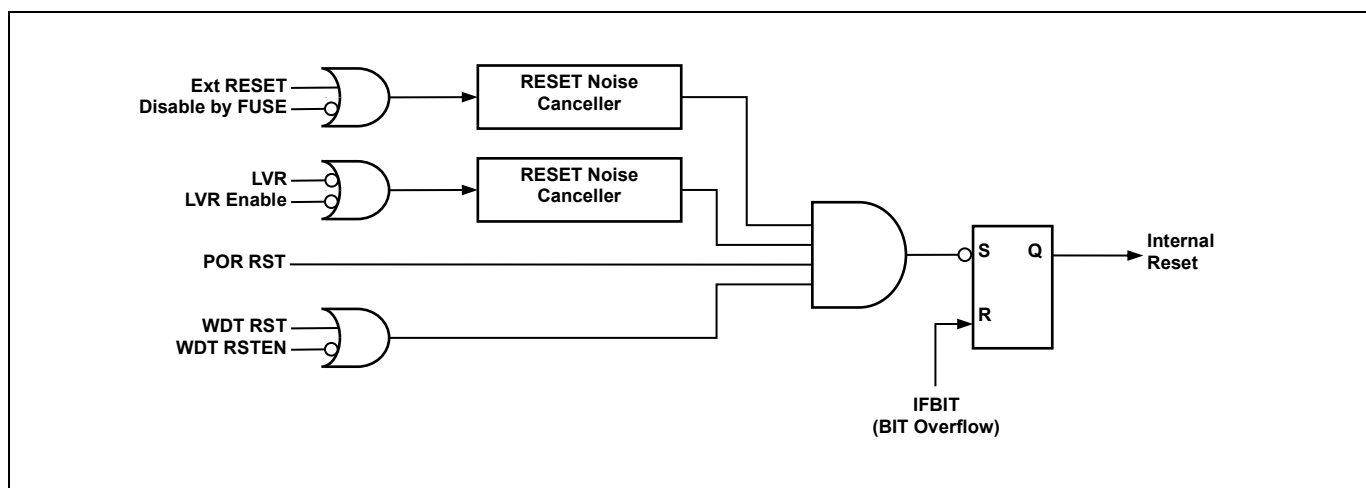


Figure 13.1 RESET Block Diagram



### 13.4 RESET Noise Canceller

The Figure 13.2 is the Noise canceller time diagram for Noise cancel of Port RESET. It has the Noise cancel value is about 2us(@V<sub>DD</sub>=5V) to Port Reset input.

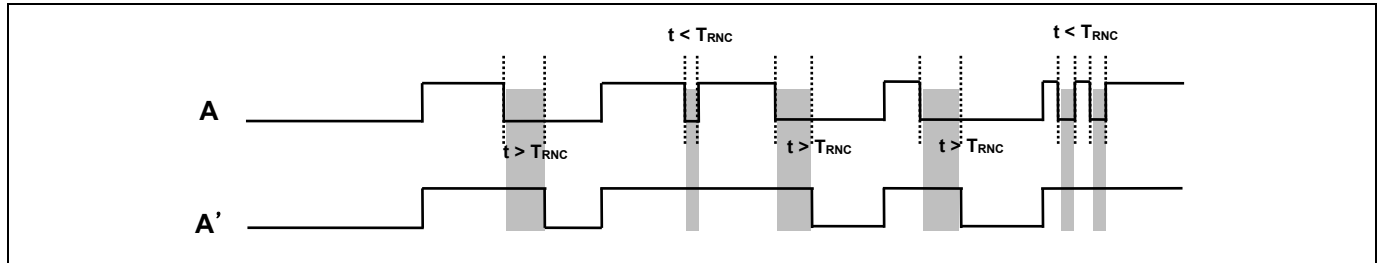


Figure 13.2 Reset noise canceller timer diagram

### 13.5 Power on RESET

When rising device power, the POR (Power On Reset) has a function to reset the device. If POR is used, it executes the device RESET function instead of the RESET IC or the RESET circuits.

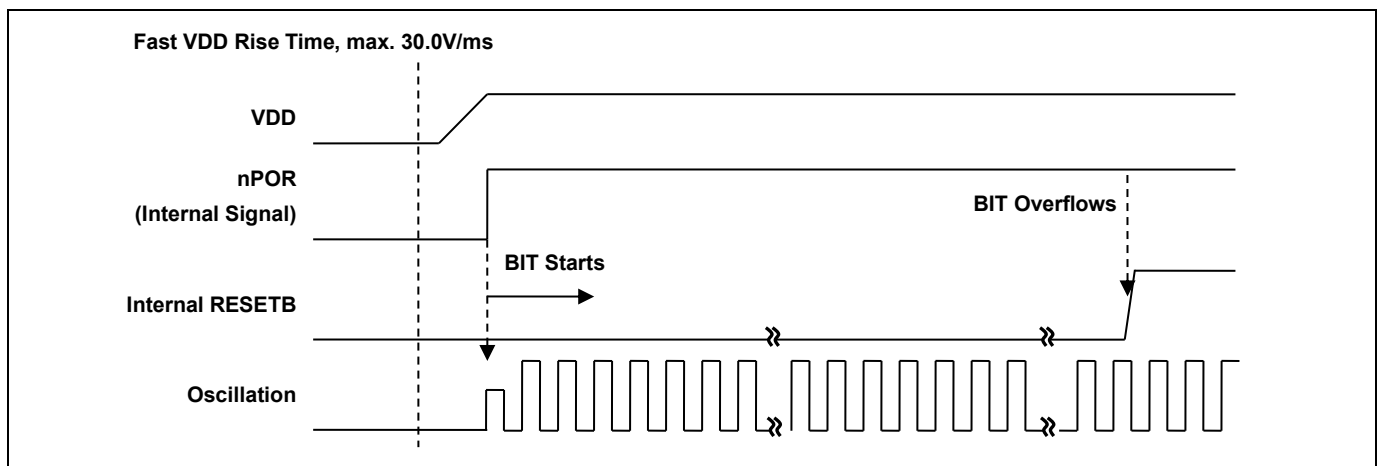


Figure 13.3 Fast VDD Rising Time

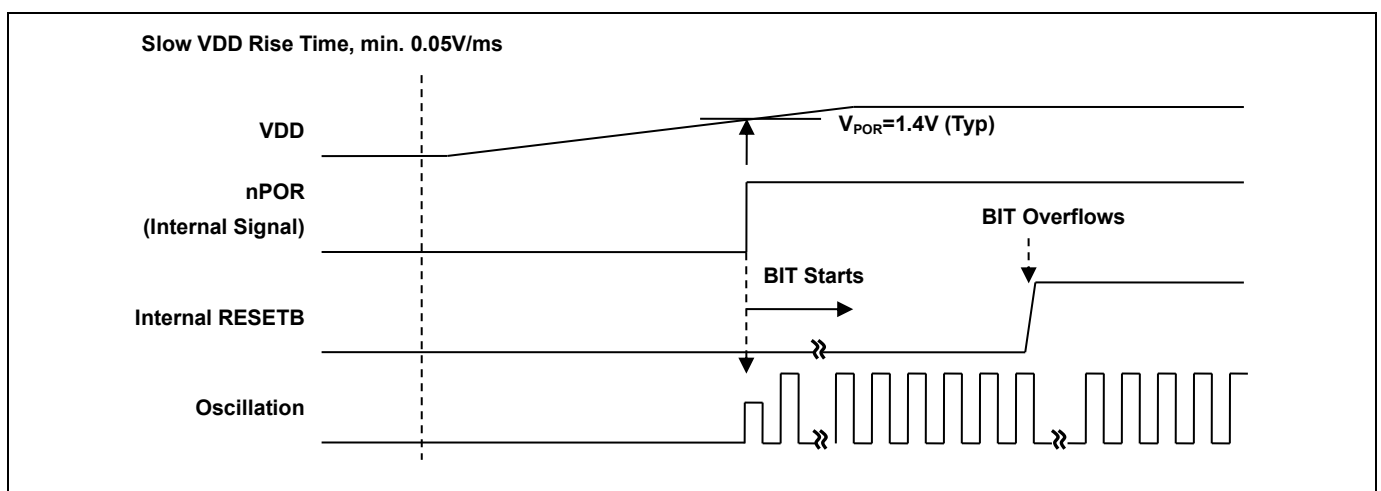


Figure 13.4 Internal RESET Release Timing On Power-Up

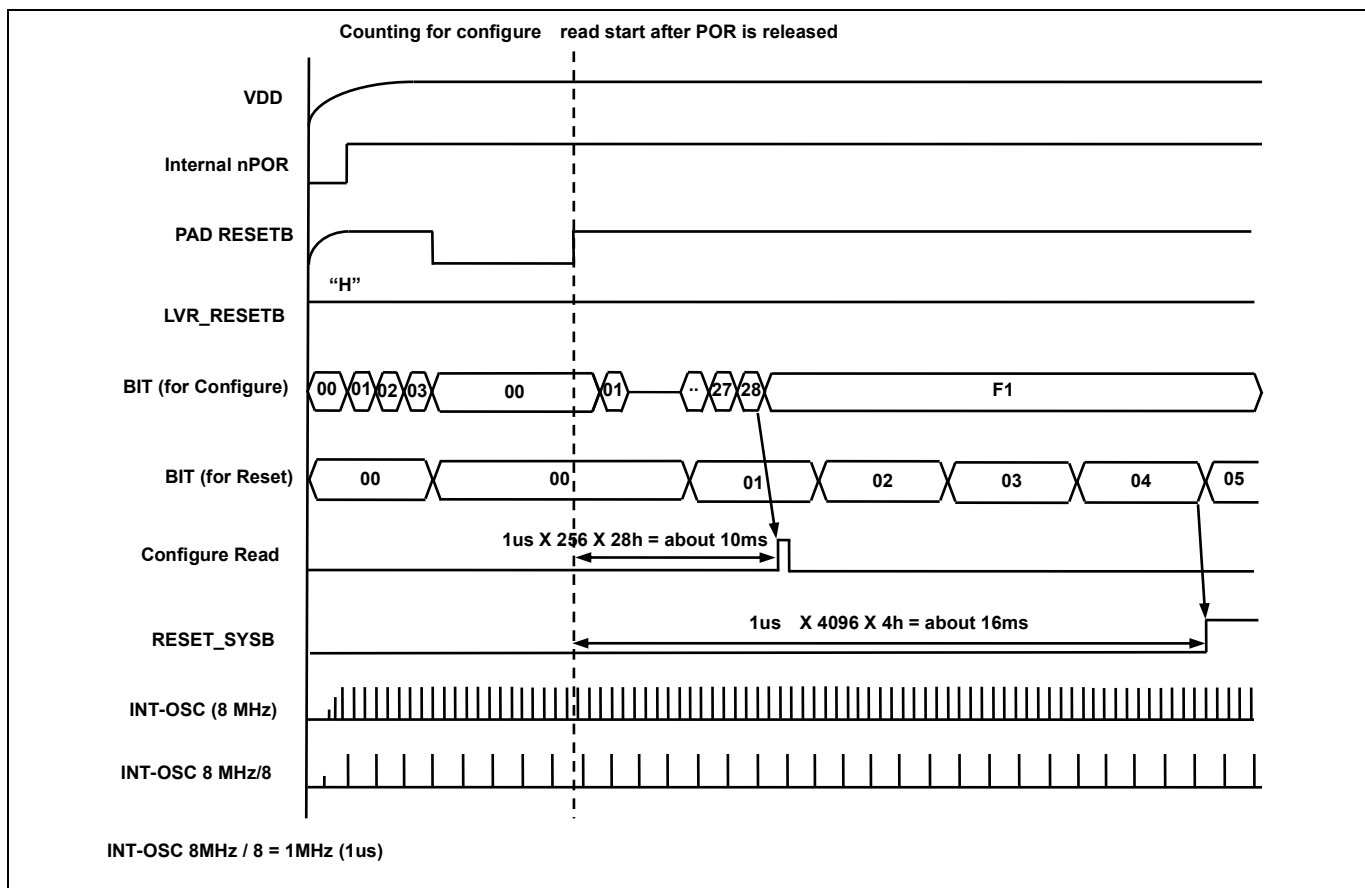


Figure 13.5 Configuration Timing when Power-on

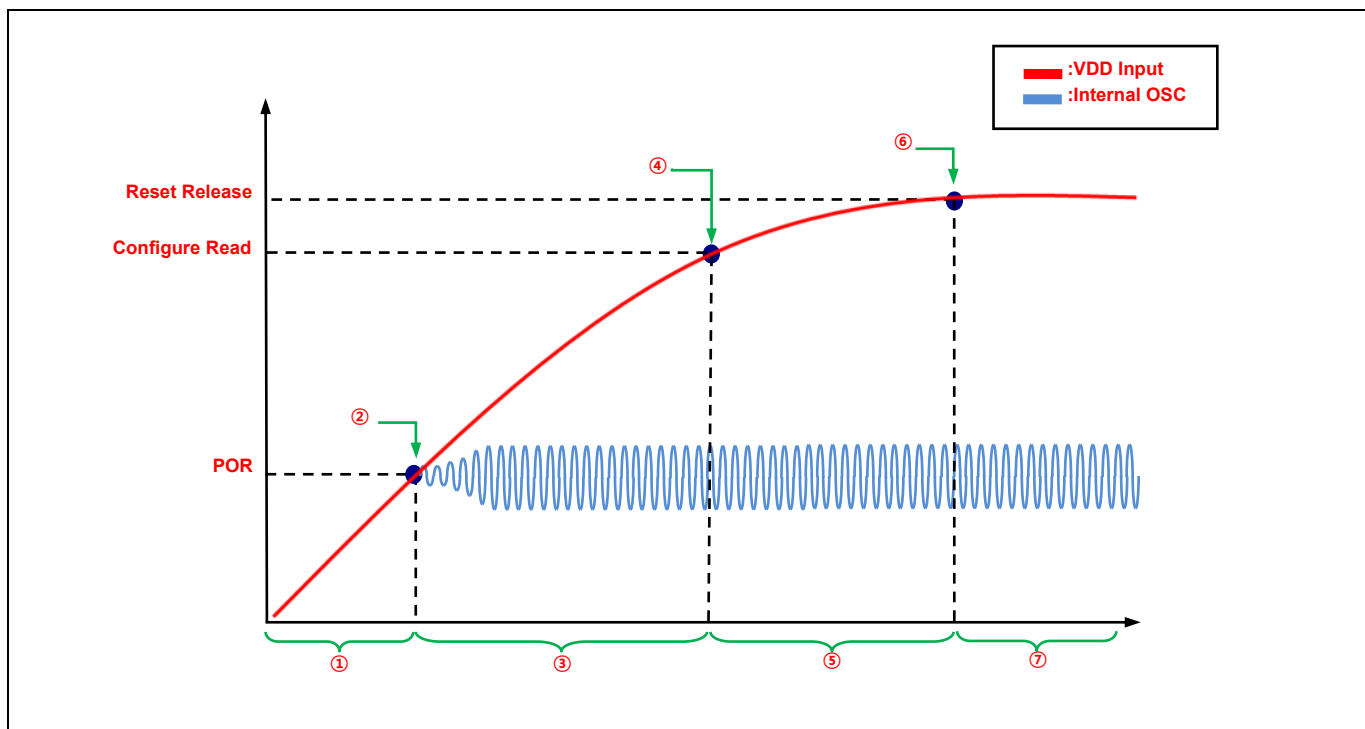


Figure 13.6 Boot Process WaveForm

Process	Description	Remarks
①	- No Operation	
②	-1st POR level Detection	-about 1.4V
③	- (INT-OSC 8MHz/8)x256x28h Delay section (=10ms) -VDD input voltage must rise over than flash operating voltage for Configure option read	-Slew Rate $\geq$ 0.05V/ms
④	- Configure option read point	-about 1.5V ~ 1.6V -Configure Value is determined by Writing Option
⑤	- Rising section to Reset Release Level	-16ms point after POR or Ext_reset release
⑥	- Reset Release section (BIT overflow) i) after 16ms, after External Reset Release (External reset) ii) 16ms point after POR (POR only)	- BIT is used for Peripheral stability
⑦	-Normal operation	

**Table 13.2** Boot Process Description

### 13.6 External RESETB Input

The External RESETB is the input to a Schmitt trigger. If RESETB pin is held with low for at least 10us over within the operating voltage range and stable oscillation, it is applied and the internal state is initialized. After reset state becomes '1', it needs the stabilization time with 16ms and after the stable state, the internal RESET becomes '1'. The Reset process step needs 5 oscillator clocks. And the program execution starts at the vector address stored at address 0000H.

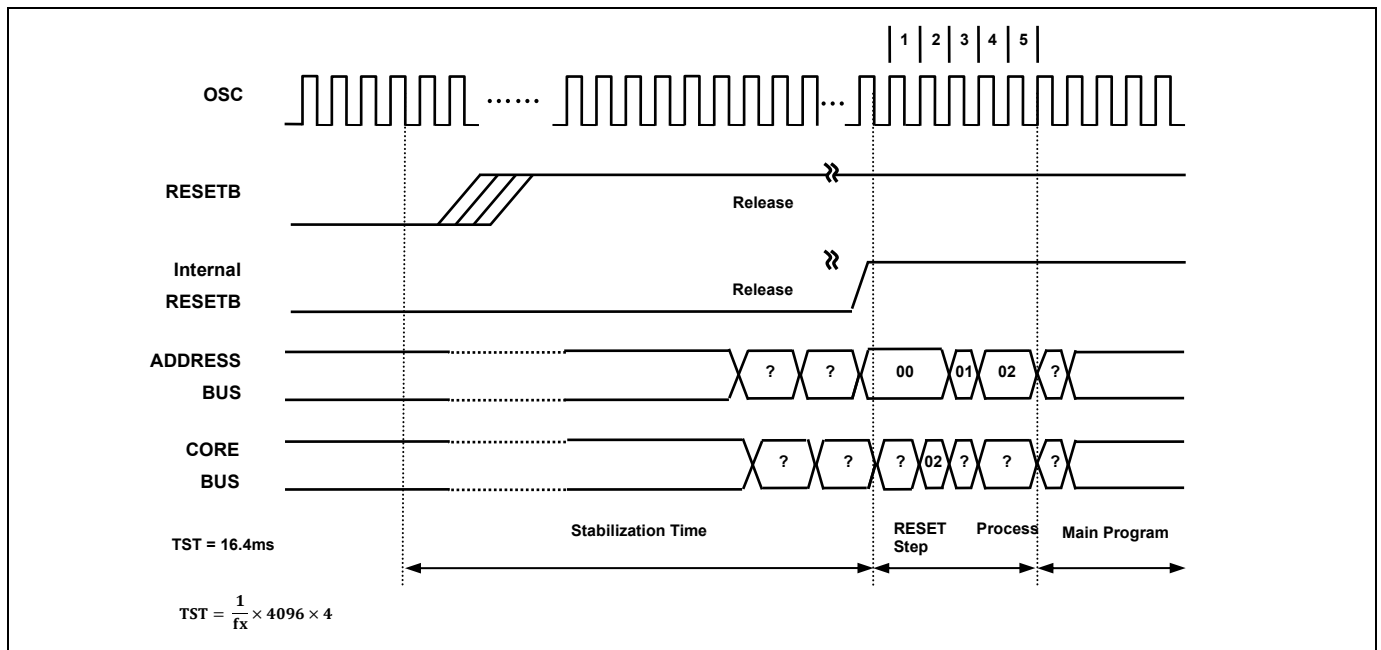


Figure 13.7 Timing Diagram after RESET

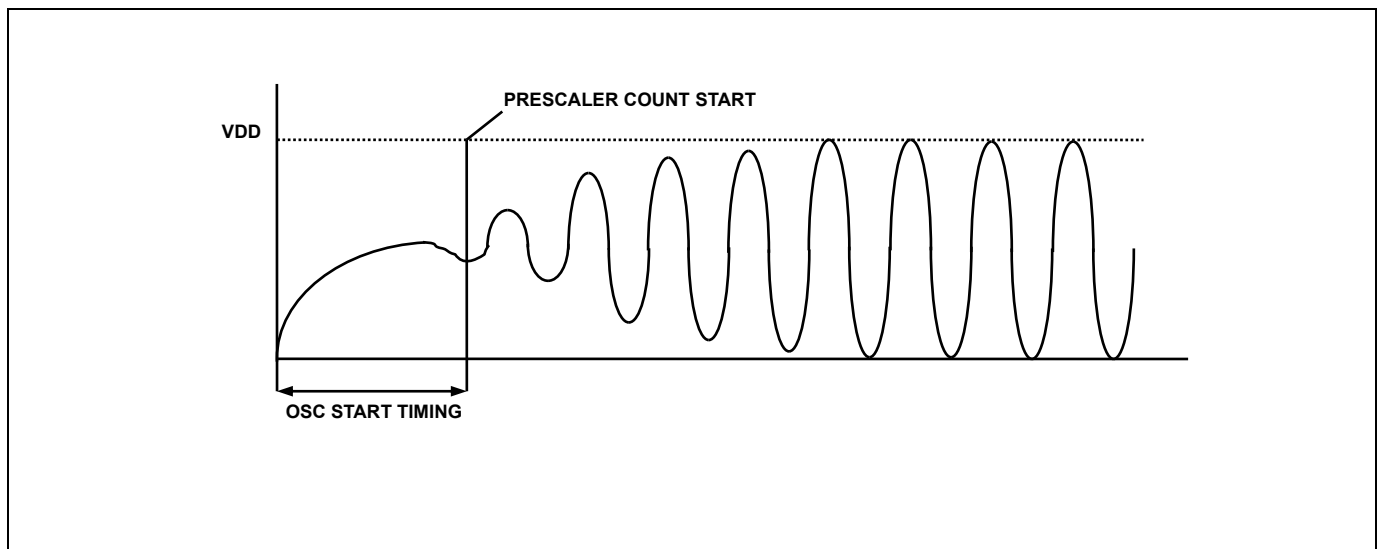


Figure 13.8 Oscillator generating waveform example

**NOTE)**

1. As shown Figure 13.8, the stable generating time is not included in the start-up time.
2. The RESETB pin has a Pull-up register by hardware

### 13.7 Brown Out Detector Processor

The MC96F6432A has an On-chip brown-out detection circuit (BOD) for monitoring the VDD level during operation by comparing it to a fixed trigger level. The trigger level for the BOD can be selected by LVRVS[3:0] bit to be 1.85V, 2.20V, 2.32V, 2.44V, 2.59V, 2.75V, 2.93V, 3.14V, 3.38V, 3.67V, 4.00V, 4.40V. In the STOP mode, this will contribute significantly to the total current consumption. So to minimize the current consumption, the LVREN bit is set to off by software.

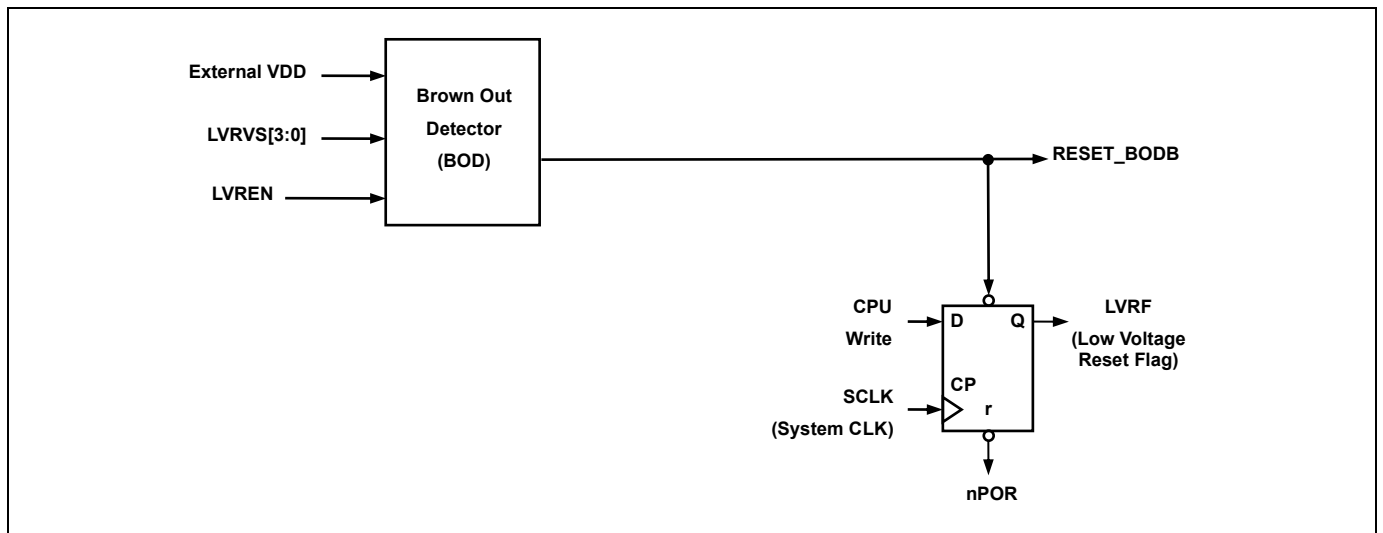


Figure 13.9 Block Diagram of BOD

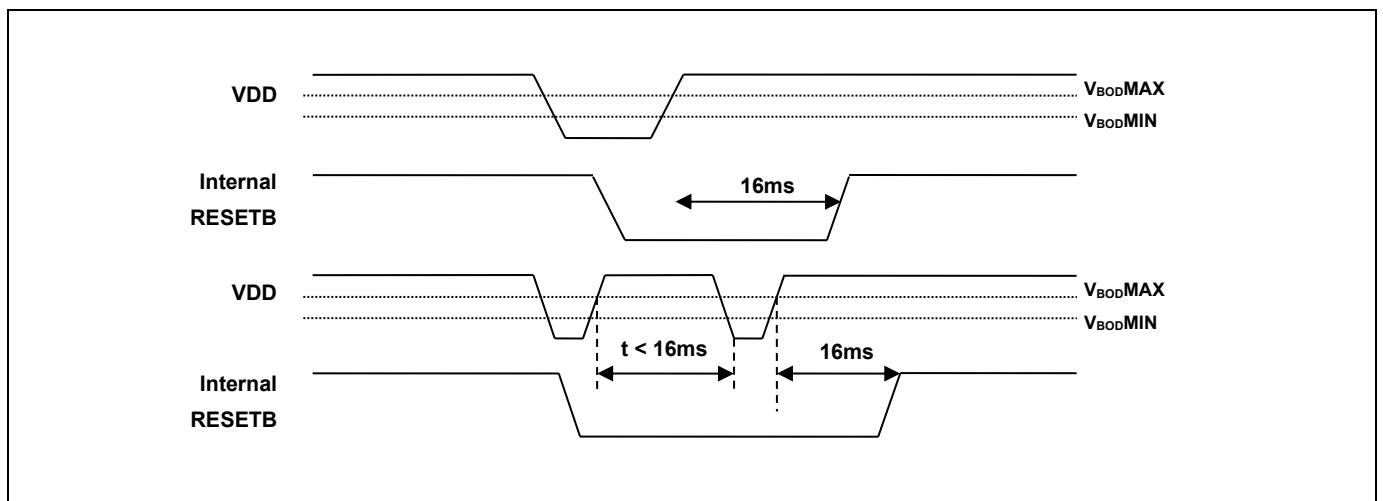


Figure 13.10 Internal Reset at the power fail situation

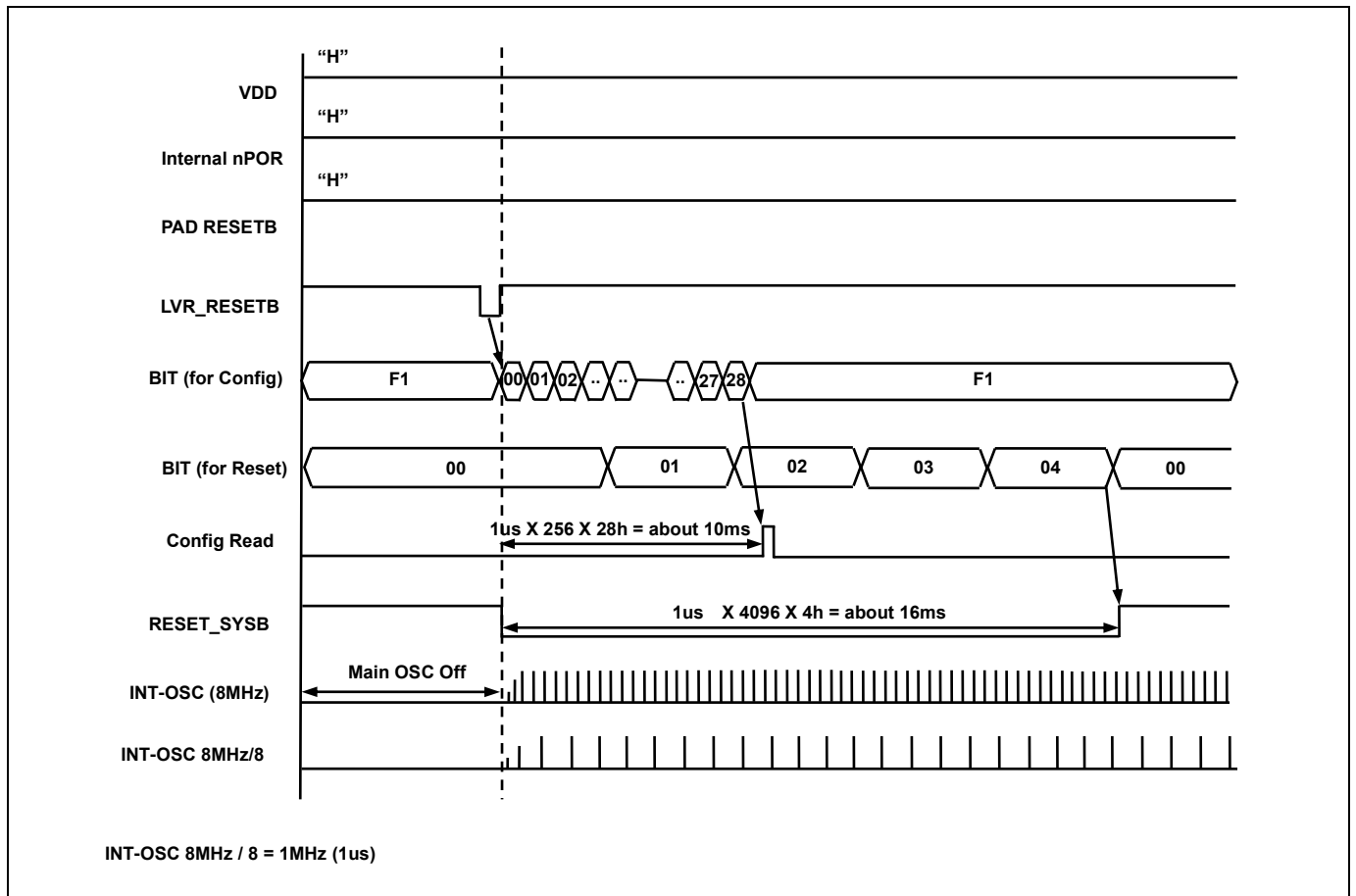


Figure 13.11 Configuration timing when BOD RESET

## 13.8 LVI Block Diagram

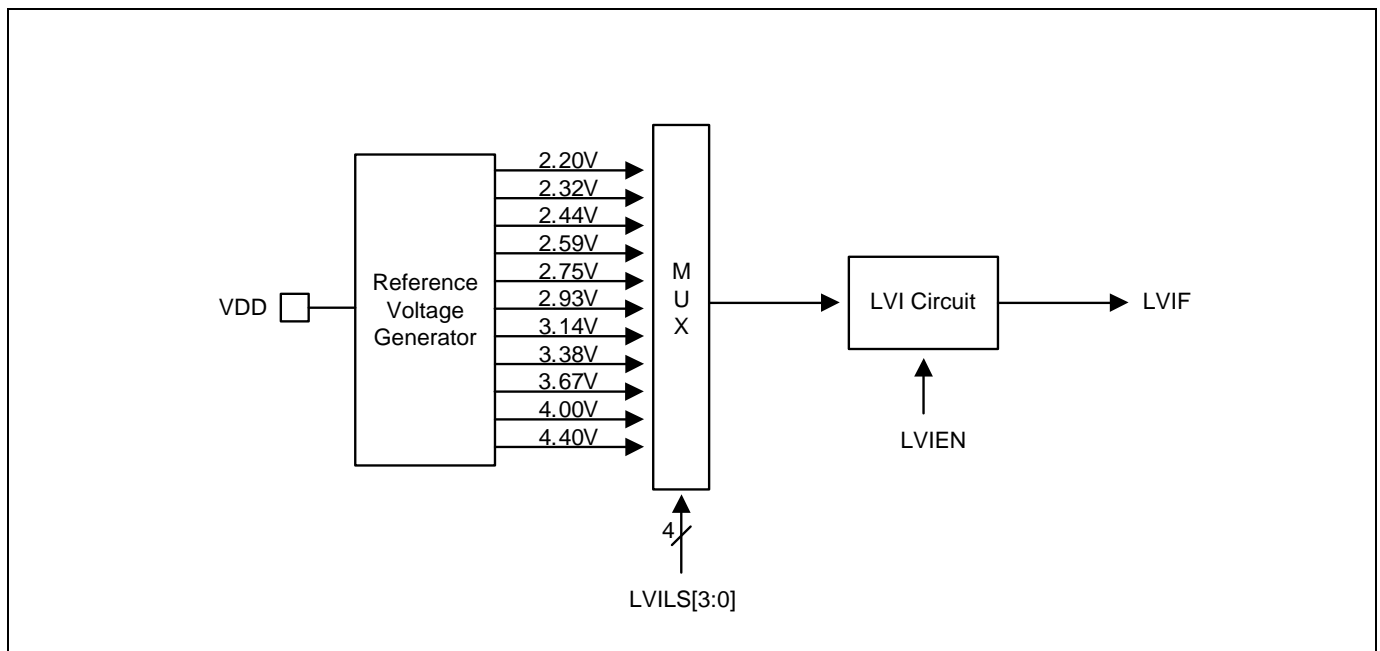


Figure 13.12 LVI Diagram

## 13.9 Register Map

Name	Address	Direction	Default	Description
RSTFR	E8H	R/W	80H	Reset Flag Register
LVRCCR	D8H	R/W	00H	Low Voltage Reset Control Register
LVICR	86H	R/W	00H	Low Voltage Indicator Control Register

Table 13.3 Reset Operation Register Map

## 13.10 Reset Operation Register Description

The reset control register consists of the reset flag register (RSTFR), low voltage reset control register (LVRCCR) and low voltage indicator control register (LVICR).

### 13.11 Register Description for Reset Operation

**RSTFR (Reset Flag Register): E8H**

7	6	5	4	3	2	1	0
PORF	EXTRF	WDTRF	–	LVRF	–	–	–
RW	RW	RW	–	RW	–	–	–

Initial value: 80H

- PORF** Power-On Reset flag bit. The bit is reset by writing '0' to this bit.
  - 0 No detection
  - 1 Detection
- EXTRF** External Reset (RESETB) flag bit. The bit is reset by writing '0' to this bit or by Power-On Reset.
  - 0 No detection
  - 1 Detection
- WDTRF** Watch Dog Reset flag bit. The bit is reset by writing '0' to this bit or by Power-On Reset.
  - 0 No detection
  - 1 Detection
- LVRF** Low Voltage Reset flag bit. The bit is reset by writing '0' to this bit or by Power-On Reset.
  - 0 No detection
  - 1 Detection

**NOTE)**

1. When the Power-On Reset occurs, the PORF bit is only set to "1", the other flag (WDTRF) bits are all cleared to "0".
2. When the Power-On Reset occurs, the EXTRF bit is unknown. At that time, the EXTRF bit can be set to "1" when External Reset (RESETB) occurs.
3. When the Power-On Reset occurs, the LVRF bit is unknown. At that time, the LVRF bit can be set to "1" when LVR Reset occurs.
4. When a reset except the POR occurs, the corresponding flag bit is only set to "1", the other flag bits are kept in the previous values.



## LVRCR (Low Voltage Reset Control Register): D8H

7	6	5	4	3	2	1	0
LVRST	–	–	LVRVS3	LVRVS2	LVRVS1	LVRVS0	LVREN
RW	–	–	RW	RW	RW	RW	RW

Initial value: 00H

**LVRST** LVR Enable when Stop Release  
 0 Not effect at stop release  
 1 LVR enable at stop release

**NOTE)**

- When this bit is '1', the LVREN bit is cleared to '0' by stop mode to release. (LVR enable)
- When this bit is '0', the LVREN bit is not effect by stop mode to release.

**LVRVS[3:0]** LVR Voltage Select

LVRVS3	LVRVS2	LVRVS1	LVRVS0	Description
0	0	0	0	1.85V
0	0	0	1	2.20V
0	0	1	0	2.20V
0	0	1	1	2.20V
0	1	0	0	2.32V
0	1	0	1	2.44V
0	1	1	0	2.59V
0	1	1	1	2.75V
1	0	0	0	2.93V
1	0	0	1	3.14V
1	0	1	0	3.38V
1	0	1	1	3.67V
1	1	0	0	4.00V
1	1	0	1	4.40V
1	1	1	0	Not available
1	1	1	1	Not available

**LVREN** LVR Operation  
 0 LVR Enable  
 1 LVR Disable

**NOTE)**

- The LVRST, LVRVS[3:0] bits are cleared by a power-on reset but are retained by other reset signals.
- The LVRVS[3:0] bits should be set to '0000b' while LVREN bit is "1".
- The LVRVS[3:0] bits should be set to one of "0x1" – "0xd" during LVR is enabled by LVREN = "0b".

LVICR (Low Voltage Indicator Control Register): 86H

7	6	5	4	3	2	1	0
–	–	LVIF	LVLEN	LVILS3	LVILS2	LVILS1	LVILS0
–	–	RW	RW	RW	RW	RW	RW

Initial value: 00H

**LVIF** Low Voltage Indicator Flag Bit

0 No detection

1 Detection

**LVLEN** LVI Enable/Disable

0 Disable

1 Enable

**LVILS[3:0]** LVI Level Select

LVILS3	LVILS2	LVILS1	LVILS0	Description
--------	--------	--------	--------	-------------

0	0	0	0	2.20V
---	---	---	---	-------

0	0	0	1	2.20V
---	---	---	---	-------

0	0	1	0	2.20V
---	---	---	---	-------

0	0	1	1	2.32V
---	---	---	---	-------

0	1	0	0	2.44V
---	---	---	---	-------

0	1	0	1	2.59V
---	---	---	---	-------

0	1	1	0	2.75V
---	---	---	---	-------

0	1	1	1	2.93V
---	---	---	---	-------

1	0	0	0	3.14V
---	---	---	---	-------

1	0	0	1	3.38V
---	---	---	---	-------

1	0	1	0	3.67V
---	---	---	---	-------

1	0	1	1	4.00V
---	---	---	---	-------

1	1	0	0	4.40V
---	---	---	---	-------

Other Values				Not available
--------------	--	--	--	---------------

## 14 On-chip Debug System(MC96F6432 ONLY)

### 14.1 Overview

#### 14.1.1 Description

MC96F6432A can not support On-chip debug(OCD). MC96F6432A isn't equipped with on-chip debugger. We recommend to develop and debug program with MC96F6432. On-chip debug system of MC96F6432 can be used for programming the non-volatile memories and on-chip debugging. Detail descriptions for programming via the OCD interface can be found in the following chapter.

Figure 14.1 shows a block diagram of the OCD interface and the On-chip Debug system.

14.1.2 Feature

- Two-wire external interface: 1-wire serial clock input, 1-wire bi-directional serial data bus
- Debugger Access to:
  - All Internal Peripheral Units
  - Internal data RAM
  - Program Counter
  - Flash and Data EEPROM Memories
- Extensive On-chip Debug Support for Break Conditions, Including
  - Break Instruction
  - Single Step Break
  - Program Memory Break Points on Single Address
  - Programming of Flash, EEPROM, Fuses and Lock Bits through the two-wire Interface
  - On-chip Debugging Supported by Dr.Choice®
- Operating frequency
  - Supports the maximum frequency of the target MCU

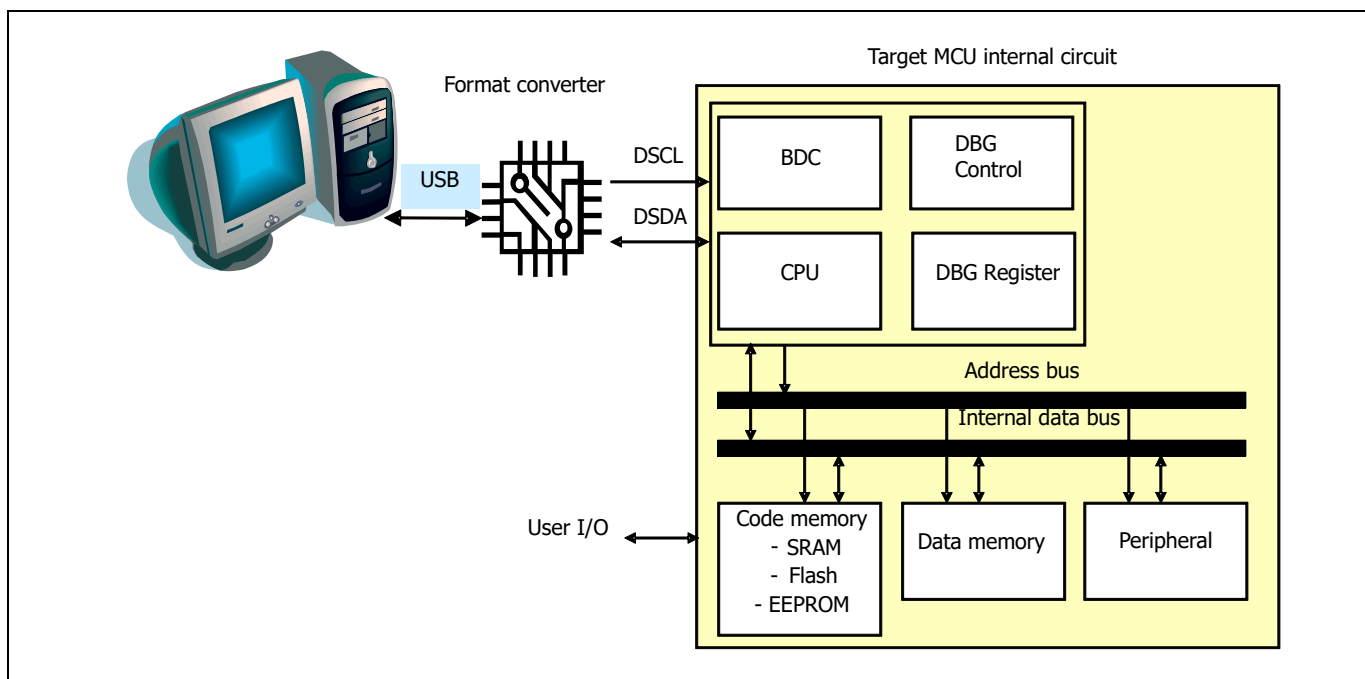


Figure 14.1 Block Diagram of On-Chip Debug System

## 14.2 Two-Pin External Interface

### 14.2.1 Basic Transmission Packet

- 10-bit packet transmission using two-pin interface.
- 1-packet consists of 8-bit data, 1-bit parity and 1-bit acknowledge.
- Parity is even of '1' for 8-bit data in transmitter.
- Receiver generates acknowledge bit as '0' when transmission for 8-bit data and its parity has no error.
- When transmitter has no acknowledge(Acknowledge bit is '1' at tenth clock), error process is executed in transmitter.
- When acknowledge error is generated, host PC makes stop condition and transmits command which has error again.
- Background debugger command is composed of a bundle of packet.
- Start condition and stop condition notify the start and the stop of background debugger command respectively.

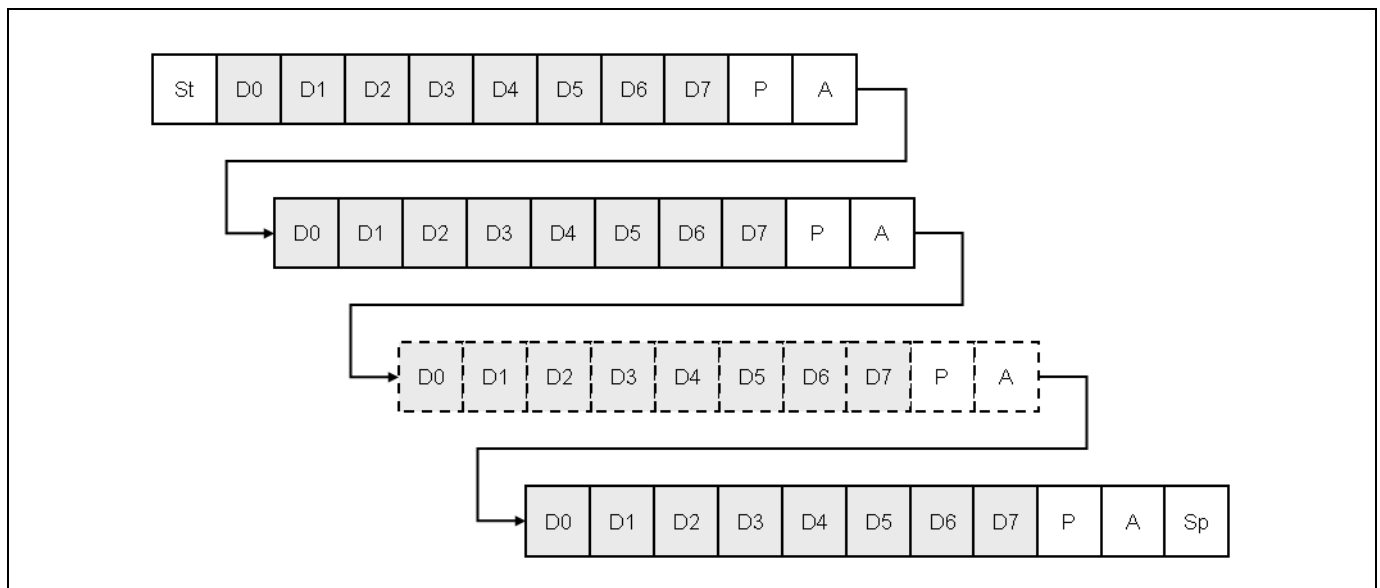


Figure 14.2 10-bit Transmission Packet

### 14.2.2 Packet Transmission Timing

#### 14.2.2.1 Data Transfer

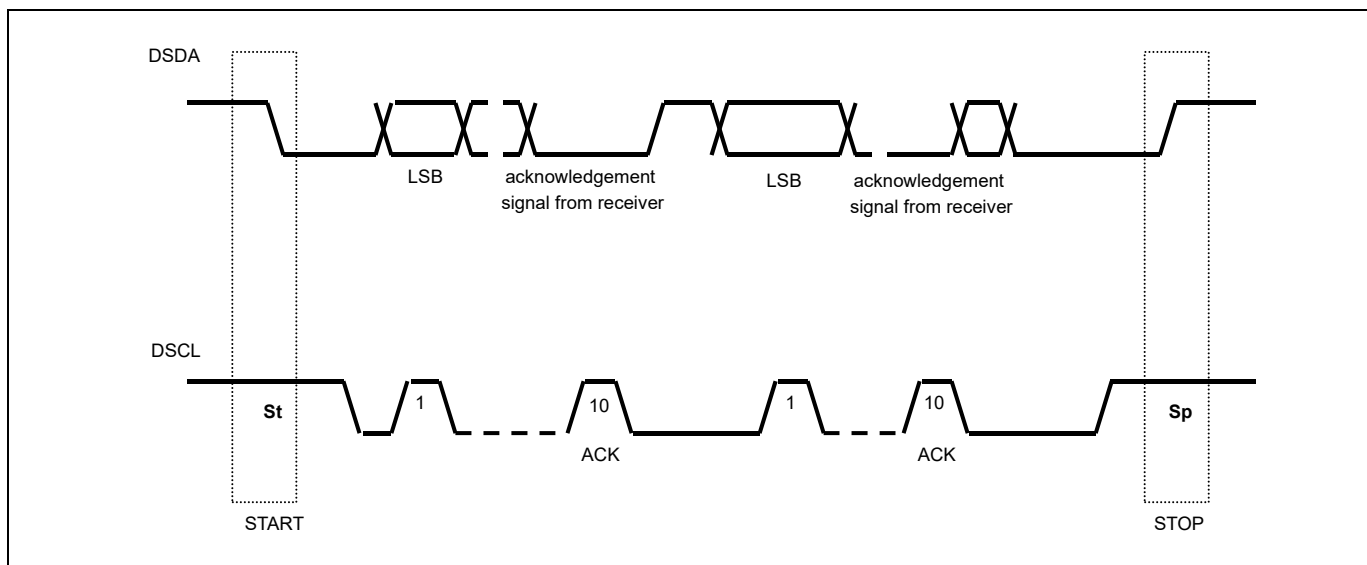


Figure 14.3 Data Transfer on the Twin Bus

#### 14.2.2.2 Bit Transfer

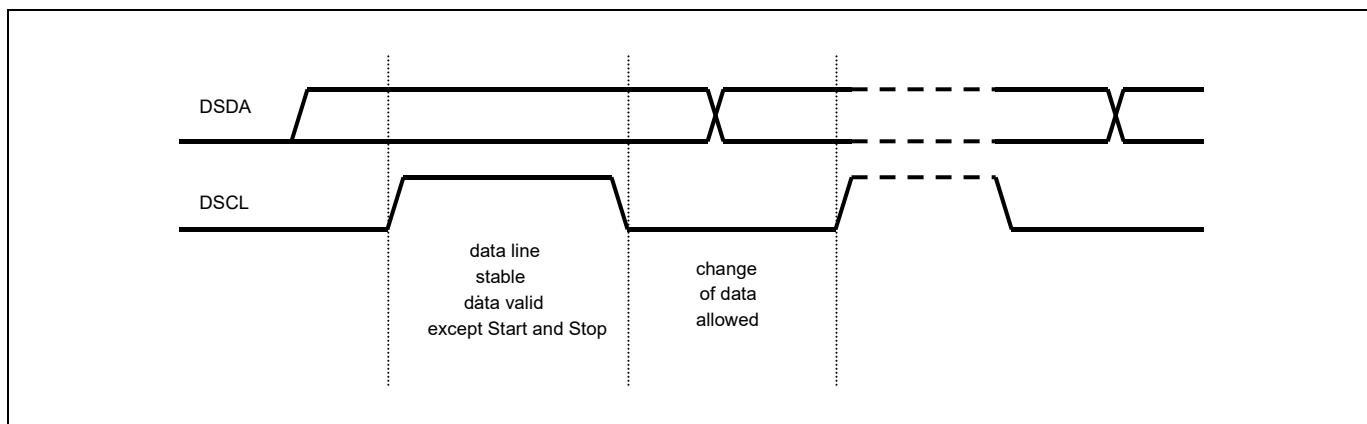


Figure 14.4 Bit Transfer on the Serial Bus

14.2.2.3 Start and Stop Condition

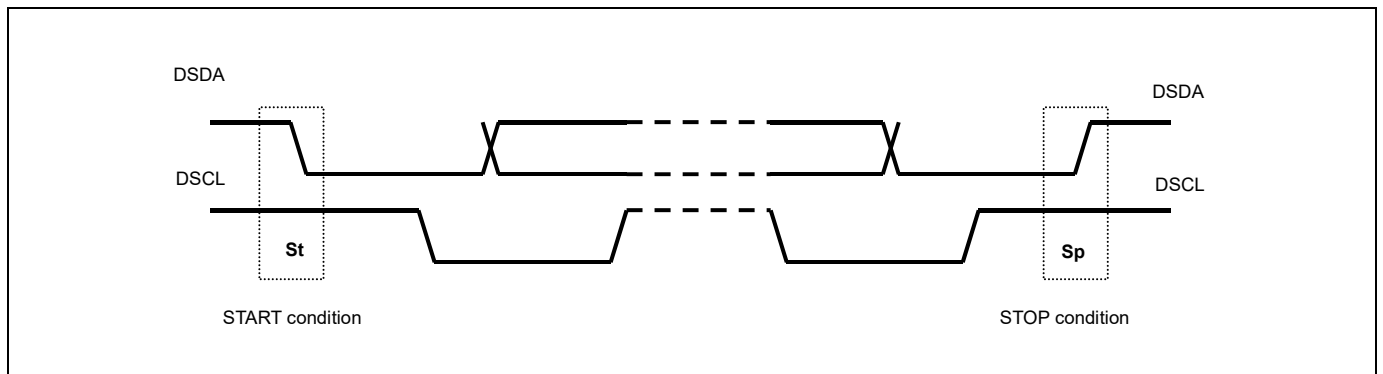


Figure 14.5 Start and Stop Condition

14.2.2.4 Acknowledge Bit

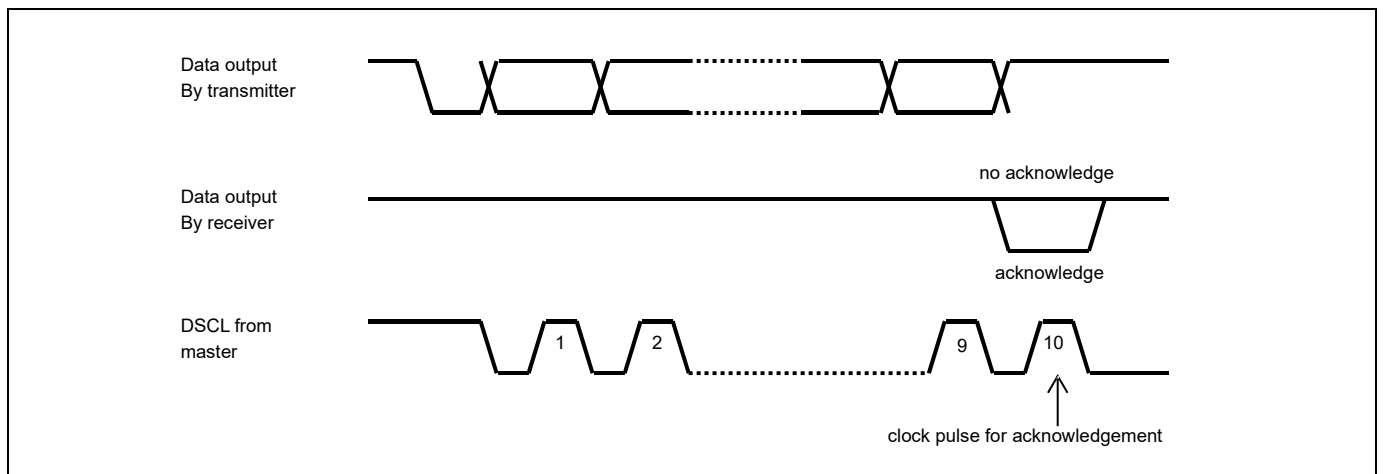


Figure 14.6 Acknowledge on the Serial Bus

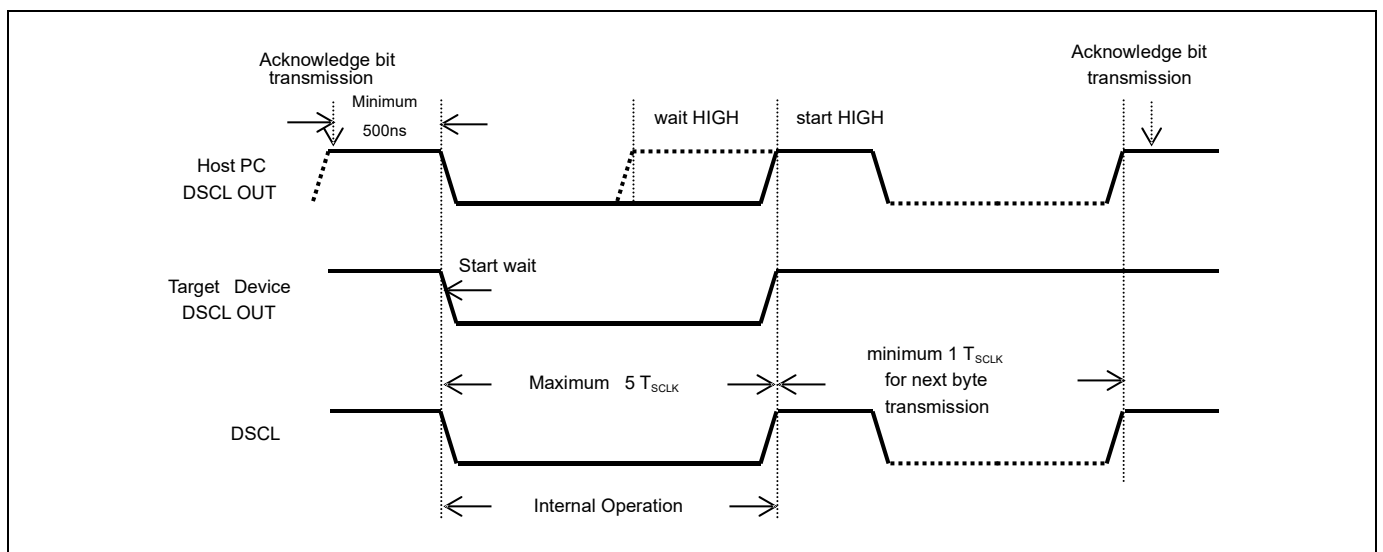
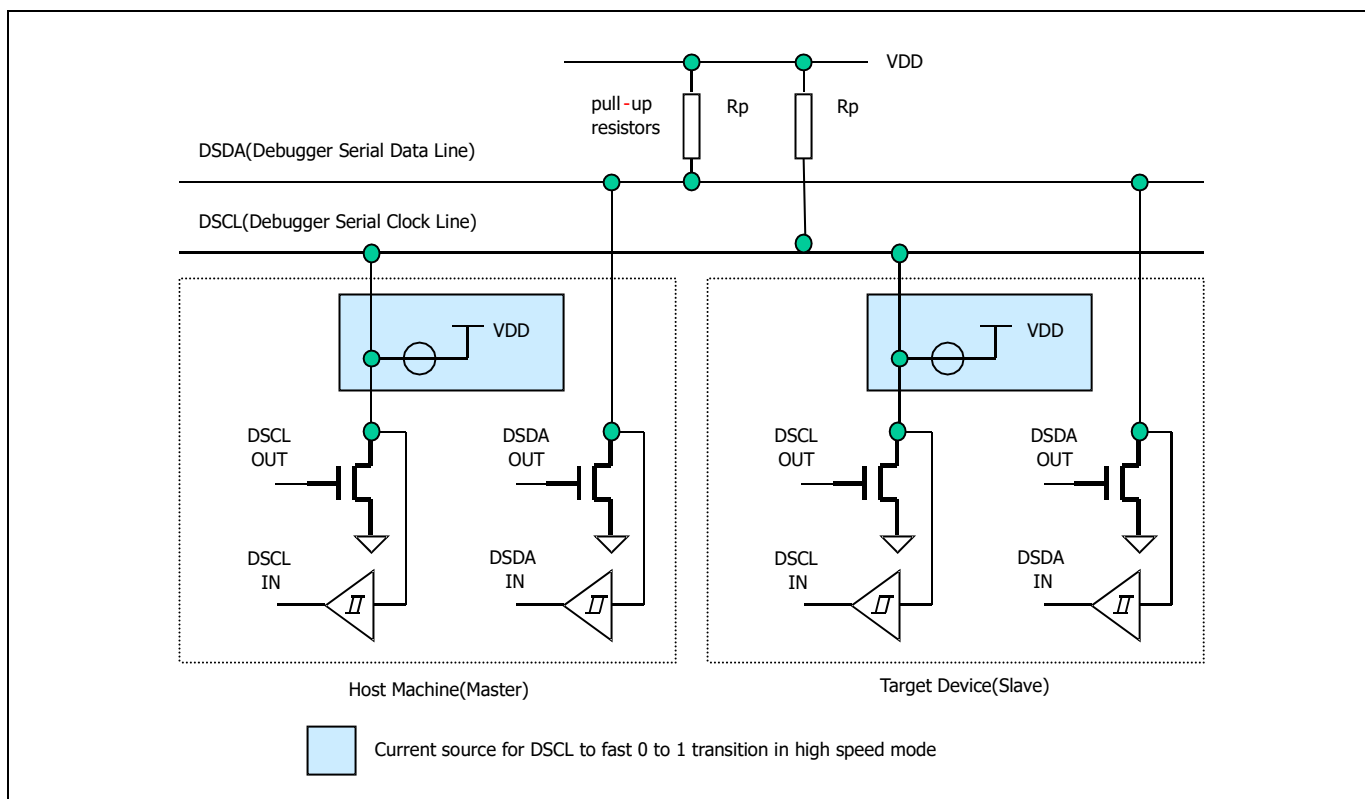


Figure 14.7 Clock Synchronization during Wait Procedure

### 14.2.3 Connection of Transmission

Two-pin interface connection uses open-drain(wire-AND bidirectional I/O).



**Figure 14.8** Connection of Transmission



## 15 Flash Memory

### 15.1 Overview

#### 15.1.1 Description

MC96F6432A incorporates flash memory to which a program can be written, erased and overwritten while mounted on the board. The flash memory can be read by 'MOVC' instruction and it can be programmed in serial ISP mode or user program mode.

- Flash Size : 32Kbytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 10,000(Sector 0~507) /100,000(Sector 508~511) program/erase cycles at typical voltage and temperature for flash memory

#### NOTE)

1. The RXE bit of USInCR2 register should be disabled before flash memory erase and write start.

15.1.2 Flash Program ROM Structure

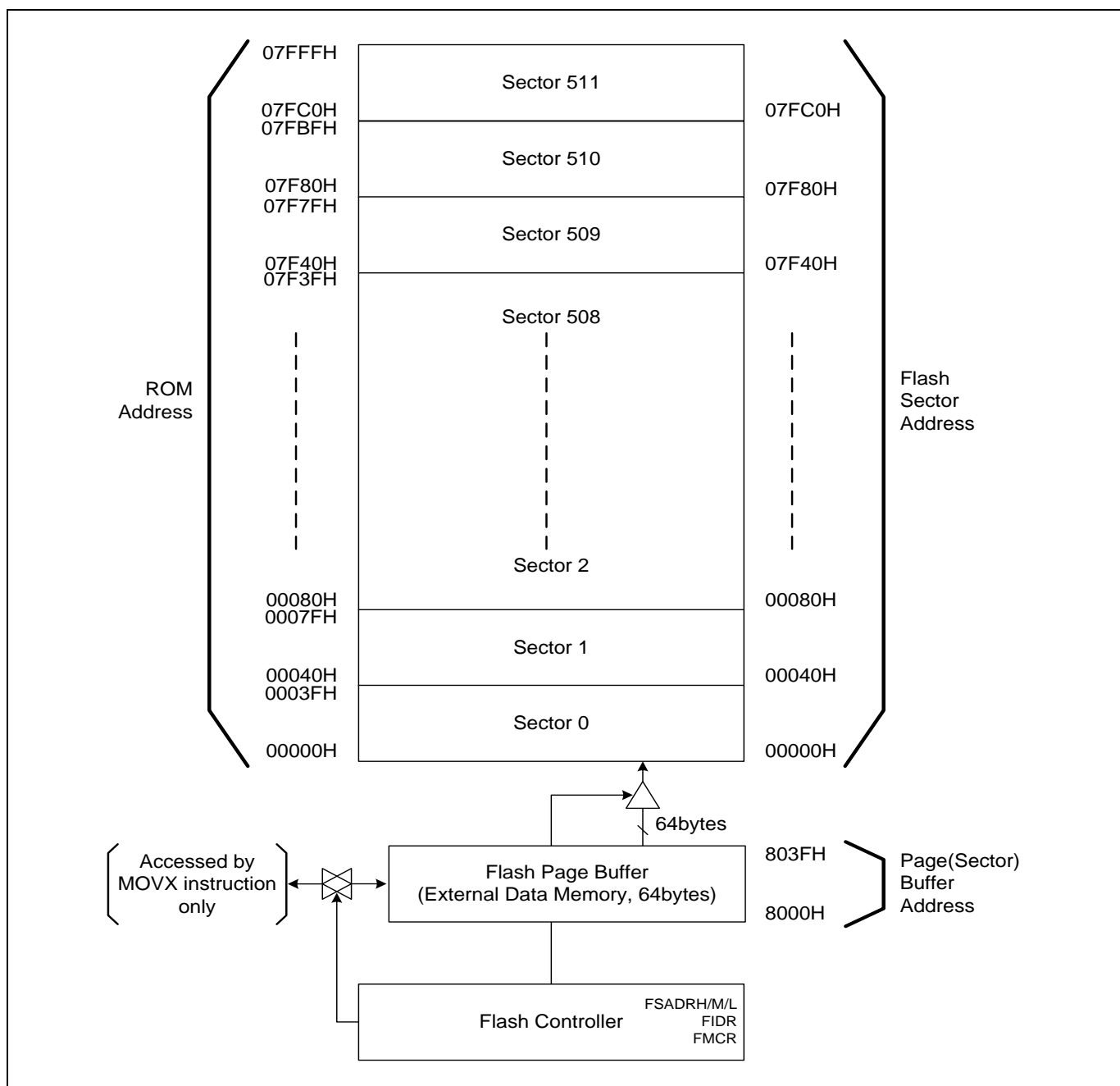


Figure 15.1 Flash Program ROM Structure

### 15.1.3 Register Map

Name	Address	Direction	Default	Description
FSADRH	FAH	R/W	00H	Flash Sector Address High Register
FSADRM	FBH	R/W	00H	Flash Sector Address Middle Register
FSADRL	FCH	R/W	00H	Flash Sector Address Low Register
FIDR	FDH	R/W	00H	Flash Identification Register
FMCR	FEH	R/W	00H	Flash Mode Control Register

**Table 15.1** Flash Memory Register Map

### 15.1.4 Register Description for Flash Memory Control and Status

Flash control register consists of the flash sector address high register (FSADRH), flash sector address middle register (FSADRM), flash sector address low register (FSADRL), flash identification register (FIDR) and flash mode control register (FMCR). They are mapped to SFR area and can be accessed only in programming mode.

15.1.5 Register Description for Flash

**FSADRH (Flash Sector Address High Register): FAH**

7	6	5	4	3	2	1	0
–	–	–	–	FSADRH3	FSADRH2	FSADRH1	FSADRH0
–	–	–	–	RW	RW	RW	RW

Initial value: 00H

**FSADRH[3:0]** Flash Sector Address High

**FSADRM (Flash Sector Address Middle Register): FBH**

7	6	5	4	3	2	1	0
FSADRM7	FSADRM6	FSADRM5	FSADRM4	FSADRM3	FSADRM2	FSADRM1	FSADRM0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**FSADRM[7:0]** Flash Sector Address Middle

**FSADRL (Flash Sector Address Low Register): FCH**

7	6	5	4	3	2	1	0
FSADRL7	FSADRL6	FSADRL5	FSADRL4	FSADRL3	FSADRL2	FSADRL1	FSADRL0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**FSADRL[7:0]** Flash Sector Address Low

**FIDR (Flash Identification Register): FDH**

7	6	5	4	3	2	1	0
FIDR7	FIDR6	FIDR5	FIDR4	FIDR3	FIDR2	FIDR1	FIDR0
RW	RW	RW	RW	RW	RW	RW	RW

Initial value: 00H

**FIDR[7:0]** Flash Identification

Others No identification value

10100101 Identification value for a flash mode

(These bits are automatically cleared to logic '00H' immediately after one time operation)

**FMCR (Flash Mode Control Register): FEH**

7	6	5	4	3	2	1	0
FMBUSY	–	–	–	–	FMCR2	FMCR1	FMCR0
R	–	–	–	–	RW	RW	RW

Initial value: 00H

**FMBUSY** Flash Mode Busy Bit. This bit will be used for only debugger.

0 No effect when “1” is written

1 Busy

**FMCR[2:0]** Flash Mode Control Bits. During a flash mode operation, the CPU is hold and the global interrupt is on disable state regardless of the IE.7 (EA) bit.

FMCR2	FMCR1	FMCR0	Description
0	0	1	Select flash page buffer reset mode and start regardless of the FIDR value (Clear all 64bytes to '0')
0	1	0	Select flash sector erase mode and start operation when the FIDR="10100101b'
0	1	1	Select flash sector write mode and start operation when the FIDR="10100101b'
1	0	0	Select flash sector Code Write Protection and Start operation when the FIDR="10100101b'

Others Values: No operation

(These bits are automatically cleared to logic '00H' immediately after one time operation)

### 15.1.6 Serial In-System Program (ISP) Mode

Serial in-system program uses the interface of debugger which uses two wires. Refer to chapter 14 in details about debugger

### 15.1.7 Protection Area (User program mode)

MC96F6432A can program its own flash memory (protection area). The protection area can not be erased or programmed. The protection areas are available only when the PAEN bit is cleared to '0', that is, enable protection area at the configure option 2 if it is needed. If the protection area isn't enabled (PAEN = '1'), this area can be used as a normal program memory.

The size of protection area can be varied by setting of configure option 2.

Protection Area Size Select			Size of Protection Area	Address of Protection Area
PASS2	PASS1	PASS0		
0	0	0	0.7Kbytes	0100H – 0FFFH
0	0	1	1.7Kbytes	0100H – 07FFH
0	1	0	2.7Kbytes	0100H – 03FFH
0	1	1	3.7Kbytes	0100H – 01FFH
1	0	0	29.7Kbytes	0100H – 77FFH
1	0	1	30.7Kbytes	0100H – 7BFFH
1	1	0	31.2Kbytes	0100H – 7DFFH
1	1	1	31.5Kbytes	0100H – 7EFFH

**Table 15.2** Protection Area size

**NOTE)**

1. Refer to chapter 16 in configure option control.

### 15.1.8 Erase Mode

#### The sector erase program procedure in user program mode

1. Page buffer clear (FMCR=0x01)
2. Write '0' to page buffer
3. Set flash sector address register (FSADRH/FSADRM/FSADRL).
4. Set flash identification register (FIDR).
5. Check the UserID for to prevent the invalid work<sup>(Note)</sup>.
6. Set flash mode control register (FMCR).
7. Erase verify

#### NOTE)

1. Please refer to the chapter "Protection for Invalid Erase/Write"
2. On flash memory erase and write, it should be disabled the RXE bit of USInCR2 register.

#### Program Tip – sector erase

```

        ANL     EO, #0xF8                ;Set DPTR0
        MOV     FMCR, #0x01            ;page buffer clear
        NOP                                     ;Dummy instruction, This instruction must be needed.
        NOP                                     ;Dummy instruction, This instruction must be needed.
        NOP                                     ;Dummy instruction, This instruction must be needed.

        MOV     A, #0
        MOV     R0, #SectorSize        ;Sector size of Device
        MOV     DPH, #0x80             ;Page Buffer Address is 8000H
        MOV     DPL, #0

Pgbuf_clr:
        MOVX    @DPTR, A
        INC     DPTR
        DJNZ    R0, Pgbuf_clr          ;Write '0' to all page buffer

        MOV     FSADRH, #SAH           ;Sector Address High Byte.
        MOV     FSADRM, #SAM           ;Sector Address Middle Byte
        MOV     FSADRL, #SAL           ;Sector Address Low Byte
        MOV     FIDR, #0xA5           ;Identification value

        MOV     A, #ID_DATA_1          ;Check the UserID(written by user)
        CJNE    A, UserID1, No_WriteErase;This routine for UserID must be needed.
        MOV     A, #ID_DATA_2
        CJNE    A, UserID2, No_WriteErase

        MOV     FMCR, #0x02            ;Start flash erase mode
        NOP                                     ;Dummy instruction, This instruction must be needed.
        NOP                                     ;Dummy instruction, This instruction must be needed.
        NOP                                     ;Dummy instruction, This instruction must be needed.

        LJMP    Erase_verify

No_WriteErase:
        MOV     FIDR, #00H
        MOV     UserID1, #00H
        MOV     UserID2, #00H
        ---

Erase_verify:
        ---

Verify_error:
        ---

```

### 15.1.9 Write Mode

#### The sector Write program procedure in user program mode

1. Page buffer clear (FMCR=0x01)
2. Write data to page buffer
3. Set flash sector address register (FSADRH/FSADRM/FSADRL).
4. Set flash identification register (FIDR).
5. Check the UserID for to prevent the invalid work<sup>(Note1)</sup>.
6. Set flash mode control register (FMCR).
7. Erase verify

#### NOTE)

1. Please refer to the chapter “Protection for Invalid Erase/Write”
2. All data of the sector should be “00H” before writing data to a sector
3. On flash memory erase and write, it should be disabled the RXE bit of USInCR2 register.

#### Program Tip – sector write

```

        ANL     EO, #0xF8                ;Set DPTR0
        MOV     FMCR, #0x01             ;page buffer clear
        NOP                    ;Dummy instruction, This instruction must be needed.
        NOP                    ;Dummy instruction, This instruction must be needed.
        NOP                    ;Dummy instruction, This instruction must be needed.

        MOV     A, #0
        MOV     R0, #SectorSize         ;Sector size of Device
        MOV     DPH, #0x80              ;Page Buffer Address is 8000H
        MOV     DPL, #0

Pgbuf_WR:  MOVX   @DPTR, A
          INC    A
          INC    DPTR
          DJNZ   R0, Pgbuf_WR           ;Write data to all page buffer

          MOV    FSADRH, #SAH           ;Sector Address High Byte.
          MOV    FSADRM, #SAM           ;Sector Address Middle Byte
          MOV    FSADRL, #SAL           ;Sector Address Low Byte
          MOV    FIDR, #0xA5           ;Identification value

          MOV    A, #ID_DATA_1          ;Check the UserID(written by user)
          CJNE   A, UserID1, No_WriteErase;This routine for UserID must be needed.
          MOV    A, #ID_DATA_2
          CJNE   A, UserID2, No_WriteErase

          MOV    FMCR, #0x03            ;Start flash write mode
          NOP                    ;Dummy instruction, This instruction must be needed.
          NOP                    ;Dummy instruction, This instruction must be needed.
          NOP                    ;Dummy instruction, This instruction must be needed.

          LJMP   Write_verify
          ---

No_WriteErase:
          MOV    FIDR, #00H
          MOV    UserID1, #00H
          MOV    UserID2, #00H
          ---

Write_verify:
          ---

Verify_error:
          ---

```



**The Byte Write program procedure in user program mode**

1. Page buffer clear (FMCR=0x01)
2. Write data to page buffer
3. Set flash sector address register (FSADRH/FSADRM/FSADRL).
4. Set flash identification register (FIDR).
5. Check the UserID for to prevent the invalid work<sup>(Note1)</sup>.
6. Set flash mode control register (FMCR).
7. Erase verify

**NOTE)**

1. Please refer to the chapter "Protection for Invalid Erase/Write".
2. Data of the address should be "00H" before writing data to an address.
3. On flash memory erase and write, it should be disabled the RXE bit of USInCR2 register.

**Program Tip – byte write**

```

ANL    EO, #0xF8                ;Set DPTR0
MOV    FMCR, #0x01              ;page buffer clear
NOP    ;Dummy instruction, This instruction must be needed.
NOP    ;Dummy instruction, This instruction must be needed.
NOP    ;Dummy instruction, This instruction must be needed.

MOV    A, #5
MOV    DPH, #0x80
MOV    DPL, #0
MOVX   @DPTR, A                ;Write data to page buffer

MOV    A, #6
MOV    DPH, #0x80
MOV    DPL, #0x05
MOVX   @DPTR, A                ;Write data to page buffer

MOV    FSADRH, #SAH             ;Sector Address High Byte.
MOV    FSADRM, #SAM             ;Sector Address Middle Byte
MOV    FSADRL, #SAL             ;Sector Address Low Byte
MOV    FIDR, #0xA5              ;Identification value

MOV    A, #ID_DATA_1            ;Check the UserID(written by user)
CJNE   A, UserID1, No_WriteErase;This routine for UserID must be needed.
MOV    A, #ID_DATA_2
CJNE   A, UserID2, No_WriteErase

MOV    FMCR, #0x03              ;Start flash write mode
NOP    ;Dummy instruction, This instruction must be needed.
NOP    ;Dummy instruction, This instruction must be needed.
NOP    ;Dummy instruction, This instruction must be needed.

LJMP   Write_verify
---
```

```

No_WriteErase:
MOV    FIDR, #00H
MOV    UserID1, #00H
MOV    UserID2, #00H
---
```

```

Write_verify:
---
```

```

Verify_error:
---
```

### 15.1.10 Protection for Invalid Erase/Write

It should be taken care to the flash erase/write programming in code.

You must make preparations for invalid jump to the flash erase/write code by malfunction, noise and power off.

**NOTE)** For more information, please refer to the appendix “Flash Protection for Invalid Erase/Write”.

1. User ID check routine for the flash erase/write code.

```
ErWt_rtn:
---
MOV    FIDR,#10100101B      ;ID Code
MOV    A,#ID_DATA_1        ;Ex) ID_DATA_1: 93H, ID_DATA_2: 85H, ID_DATA_3: 5AH
CJNE   A,UserID1,No_WriteErase
MOV    A,#ID_DATA_2
CJNE   A,UserID2,No_WriteErase
MOV    A,#ID_DATA_3
CJNE   A,UserID3,No_WriteErase
MOV    FMCR,#0x??          ;0x03 if write, 0x02 if erase
---
---
RET

No_WriteErase:
MOV    FIDR,#00H
MOV    UserID1,#00H
MOV    UserID2,#00H
MOV    UserID3,#00H
MOV    Flash_flag,#00H
RET
```

If code is like the above lines, an invalid flash erase/write can be avoided.

**NOTE)** On flash memory erase and write, it should be disabled the RXE bit of USInCR2 register.

2. It is important where the UserID1/2/3 is written. It will be remain the invalid flash erase/write problem if the UserID1/2/3 is written at the above line of the instruction “MOV FIDR,#10100101B”. So. It had better writing the UserID1/2/3 in another routine after return.

```
Decide_ErWt:
---
MOV    Flash_flag1,#38H    ;Random value for example, in case of erase/write needs
MOV    FSADRL,#20H        ;Here 20H is example,
MOV    Flash_flag2,#75H
RET
```

3. The flash sector address (FSADRH/FSADRM/FSADRL) should always keep the address of the flash which is used for data area. For example, The FSADRH/FSADRM is always 0x00/0x7f if 0x7f00 to 0x7fff is used for data.
4. Overview of main

```

---
CALL    Work1
CALL    Decide_ErWt
CALL    Work2
CALL    ID_write
CALL    Work3
CALL    Flash_erase
CALL    Flash_write
---
---
---
ID_wire:
MOV     A,#38H
CJNE   A,Flash_flag1,No_write_ID
MOV     A,#75H
CJNE   A,Flash_flag2,No_write_ID
MOV    UserID1,#ID_DATA_1      ;Write User ID1
MOV     A,#38H
CJNE   A,Flash_flag1,No_write_ID
MOV     A,#75H
CJNE   A,Flash_flag2,No_write_ID
MOV    UserID2,#ID_DATA_2      ;Write User ID2
MOV     A,#38H
CJNE   A,Flash_flag1,No_write_ID
MOV     A,#75H
CJNE   A,Flash_flag2,No_write_ID
MOV    UserID3,#ID_DATA_3      ;Write User ID3
RET

No_write_ID:
MOV     UserID1,#00H
MOV     UserID2,#00H
MOV     UserID3,#00H
RET

```

15.1.10.1 Flow of Protection for Invalid Erase/Write

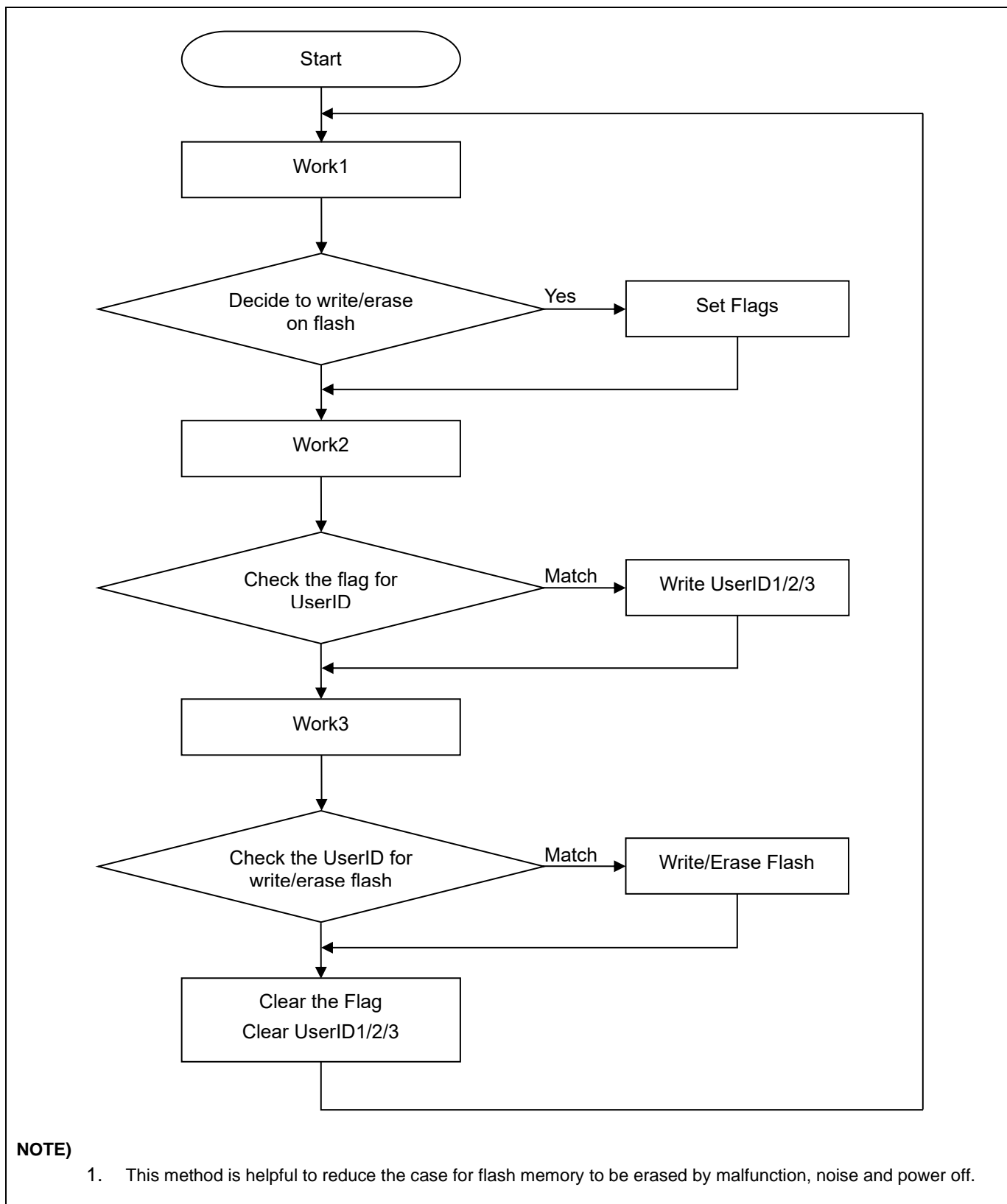


Figure 15.2 Flow of Protection for Invalid Erase/Write

### 15.1.11 Read Mode

#### The Reading program procedure in user program mode

1. Load receive data from flash memory on MOVC instruction by indirectly addressing mode.

#### Program Tip – reading

```

MOV     A, #0
MOV     DPH, #0x7F
MOV     DPL, #0x40           ;flash memory address

MOVC    A, @A+DPTR          ;read data from flash memory

```

### 15.1.12 Code Write Protection Mode

#### The Code Write Protection program procedure in user program mode

1. Set flash identification register (FIDR).
2. Check the UserID for to prevent the invalid work<sup>(Note)</sup>.
3. Set flash mode control register (FMCR).

**NOTE)** Please refer to the chapter “Protection for Invalid Erase/Write”

#### Program Tip – Code Write Protection

```

MOV     FIDR, #0xA5           ;Identification value

MOV     A, #ID_DATA_1         ;Check the UserID(written by user)
CJNE   A, UserID1, No_WriteErase;This routine for UserID must be needed.
MOV     A, #ID_DATA_2
CJNE   A, UserID2, No_WriteErase

MOV     FMCR, #0x04           ;Start flash Code Write Protection mode
NOP                                           ;Dummy instruction, This instruction must be needed.
NOP                                           ;Dummy instruction, This instruction must be needed.
NOP                                           ;Dummy instruction, This instruction must be needed.

No_WriteErase:
MOV     FIDR, #00H
MOV     UserID1, #00H
MOV     UserID2, #00H
---
```

## 16 Configure Option

### 16.1 Configure Option Control

The data for configure option should be written in the configure option area (003EH – 003FH) by programmer (Writer tools).

#### CONFIGURE OPTION 2 : ROM Address 003FH

7	6	5	4	3	2	1	0
R_P	HL	–	VAPEN	–	–	–	RSTS

Initial value : 00H

<b>R_P</b>	Code Read Protection
0	Disable
1	Enable
<b>HL</b>	Code Write Protection
0	Disable
1	Enable
<b>VAPEN</b>	Vector Area (00H – FFH) Protection Enable/Disable
0	Disable Protection (Erasable by instruction)
1	Enable Protection (Not erasable by instruction)
<b>RSTS</b>	Select RESETB pin
0	Disable RESETB pin(P55)
1	Enable RESETB pin

#### CONFIGURE OPTION 1: ROM Address 003EH

7	6	5	4	3	2	1	0
–	–	–	–	PAEN	PASS2	PASS1	PASS0

Initial value : 00H

<b>PAEN</b>	Enable Specific Area Write Protection		
0	Disable Protection (Erasable by instruction)		
1	Enable Protection (Not erasable by instruction)		
<b>PASS [2:0]</b>	Select Specific Area for Write Protection		
<b>NOTE)</b>			
1. When PAEN = '1', it is applied.			
PASS2	PASS1	PASS0	Description
0	0	0	0.7Kbytes (Address 0100H – 03FFH)
0	0	1	1.7Kbytes (Address 0100H – 07FFH)
0	1	0	2.7Kbytes (Address 0100H – 0BFFH)
0	1	1	3.7Kbytes (Address 0100H – 0FFFH)
1	0	0	29.7Kbytes (Address 0100H – 77FFH)
1	0	1	30.7Kbytes (Address 0100H – 7BFFH)
1	1	0	31.2Kbytes (Address 0100H – 7DFFH)
1	1	1	31.5Kbytes (Address 0100H – 7EFFH)

## 17 APPENDIX

### 17.1 Instruction Table

Instructions are either 1, 2 or 3 bytes long as listed in the 'Bytes' column below.

Each instruction takes either 1, 2 or 4 machine cycles to execute as listed in the following table. 1 machine cycle comprises 2 system clock cycles.

ARITHMETIC				
Mnemonic	Description	Bytes	Cycles	Hex code
ADD A, Rn	Add register to A	1	1	28-2F
ADD A, dir	Add direct byte to A	2	1	25
ADD A, @Ri	Add indirect memory to A	1	1	26-27
ADD A, #data	Add immediate to A	2	1	24
ADDC A, Rn	Add register to A with carry	1	1	38-3F
ADDC A, dir	Add direct byte to A with carry	2	1	35
ADDC A, @Ri	Add indirect memory to A with carry	1	1	36-37
ADDC A, #data	Add immediate to A with carry	2	1	34
SUBB A, Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A, dir	Subtract direct byte from A with borrow	2	1	95
SUBB A, @Ri	Subtract indirect memory from A with borrow	1	1	96-97
SUBB A, #data	Subtract immediate from A with borrow	2	1	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC dir	Increment direct byte	2	1	05
INC @Ri	Increment indirect memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC dir	Decrement direct byte	2	1	15
DEC @Ri	Decrement indirect memory	1	1	16-17
INC DPTR	Increment data pointer	1	2	A3
MUL AB	Multiply A by B	1	4	A4
DIV AB	Divide A by B	1	4	84
DAA	Decimal Adjust A	1	1	D4

LOGICAL				
Mnemonic	Description	Bytes	Cycles	Hex code
ANL A, Rn	AND register to A	1	1	58-5F
ANL A, dir	AND direct byte to A	2	1	55
ANL A, @Ri	AND indirect memory to A	1	1	56-57
ANL A, #data	AND immediate to A	2	1	54
ANL dir, A	AND A to direct byte	2	1	52
ANL dir, #data	AND immediate to direct byte	3	2	53
ORL A, Rn	OR register to A	1	1	48-4F
ORL A, dir	OR direct byte to A	2	1	45
ORL A, @Ri	OR indirect memory to A	1	1	46-47
ORL A, #data	OR immediate to A	2	1	44
ORL dir, A	OR A to direct byte	2	1	42
ORL dir, #data	OR immediate to direct byte	3	2	43
XRL A, Rn	Exclusive-OR register to A	1	1	68-6F
XRL A, dir	Exclusive-OR direct byte to A	2	1	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	1	66-67
XRL A, #data	Exclusive-OR immediate to A	2	1	64
XRL dir, A	Exclusive-OR A to direct byte	2	1	62
XRL dir, #data	Exclusive-OR immediate to direct byte	3	2	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13



DATA TRANSFER				
Mnemonic	Description	Bytes	Cycles	Hex code
MOV A, Rn	Move register to A	1	1	E8-EF
MOV A, dir	Move direct byte to A	2	1	E5
MOV A, @Ri	Move indirect memory to A	1	1	E6-E7
MOV A, #data	Move immediate to A	2	1	74
MOV Rn, A	Move A to register	1	1	F8-FF
MOV Rn, dir	Move direct byte to register	2	2	A8-AF
MOV Rn, #data	Move immediate to register	2	1	78-7F
MOV dir, A	Move A to direct byte	2	1	F5
MOV dir, Rn	Move register to direct byte	2	2	88-8F
MOV dir, dir	Move direct byte to direct byte	3	2	85
MOV dir, @Ri	Move indirect memory to direct byte	2	2	86-87
MOV dir, #data	Move immediate to direct byte	3	2	75
MOV @Ri, A	Move A to indirect memory	1	1	F6-F7
MOV @Ri, dir	Move direct byte to indirect memory	2	2	A6-A7
MOV @Ri, #data	Move immediate to indirect memory	2	1	76-77
MOV DPTR, #data	Move immediate to data pointer	3	2	90
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	2	93
MOVC A, @A+PC	Move code byte relative PC to A	1	2	83
MOVX A, @Ri	Move external data(A8) to A	1	2	E2-E3
MOVX A, @DPTR	Move external data(A16) to A	1	2	E0
MOVX @Ri, A	Move A to external data(A8)	1	2	F2-F3
MOVX @DPTR, A	Move A to external data(A16)	1	2	F0
PUSH dir	Push direct byte onto stack	2	2	C0
POP dir	Pop direct byte from stack	2	2	D0
XCH A, Rn	Exchange A and register	1	1	C8-CF
XCH A, dir	Exchange A and direct byte	2	1	C5
XCH A, @Ri	Exchange A and indirect memory	1	1	C6-C7
XCHD A, @Ri	Exchange A and indirect memory nibble	1	1	D6-D7

BOOLEAN				
Mnemonic	Description	Bytes	Cycles	Hex code
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	1	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	1	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	1	B2
ANL C, bit	AND direct bit to carry	2	2	82
ANL C, /bit	AND direct bit inverse to carry	2	2	B0
ORL C, bit	OR direct bit to carry	2	2	72
ORL C, /bit	OR direct bit inverse to carry	2	2	A0
MOV C, bit	Move direct bit to carry	2	1	A2
MOV bit, C	Move carry to direct bit	2	2	92

BRANCHING				
Mnemonic	Description	Bytes	Cycles	Hex code
ACALL addr 11	Absolute jump to subroutine	2	2	11→F1
LCALL addr 16	Long jump to subroutine	3	2	12
RET	Return from subroutine	1	2	22
RETI	Return from interrupt	1	2	32
AJMP addr 11	Absolute jump unconditional	2	2	01→E1
LJMP addr 16	Long jump unconditional	3	2	02
SJMP rel	Short jump (relative address)	2	2	80
JC rel	Jump on carry = 1	2	2	40
JNC rel	Jump on carry = 0	2	2	50
JB bit, rel	Jump on direct bit = 1	3	2	20
JNB bit, rel	Jump on direct bit = 0	3	2	30
JBC bit, rel	Jump on direct bit = 1 and clear	3	2	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	2	60
JNZ rel	Jump on accumulator ≠0	2	2	70
CJNE A, dir, rel	Compare A, direct jne relative	3	2	B5
CJNE A, #d, rel	Compare A, immediate jne relative	3	2	B4
CJNE Rn, #d, rel	Compare register, immediate jne relative	3	2	B8-BF
CJNE @Ri, #d, rel	Compare indirect, immediate jne relative	3	2	B6-B7
DJNZ Rn, rel	Decrement register, jnz relative	2	2	D8-DF
DJNZ dir, rel	Decrement direct byte, jnz relative	3	2	D5

MISCELLANEOUS				
Mnemonic	Description	Bytes	Cycles	Hex code
NOP	No operation	1	1	00

ADDITIONAL INSTRUCTIONS (selected through EO[7:4])				
Mnemonic	Description	Bytes	Cycles	Hex code
MOVC @(DPTR++), A	M8051W/M8051EW-specific instruction supporting software download into program memory	1	2	A5
TRAP	Software break command	1	1	A5

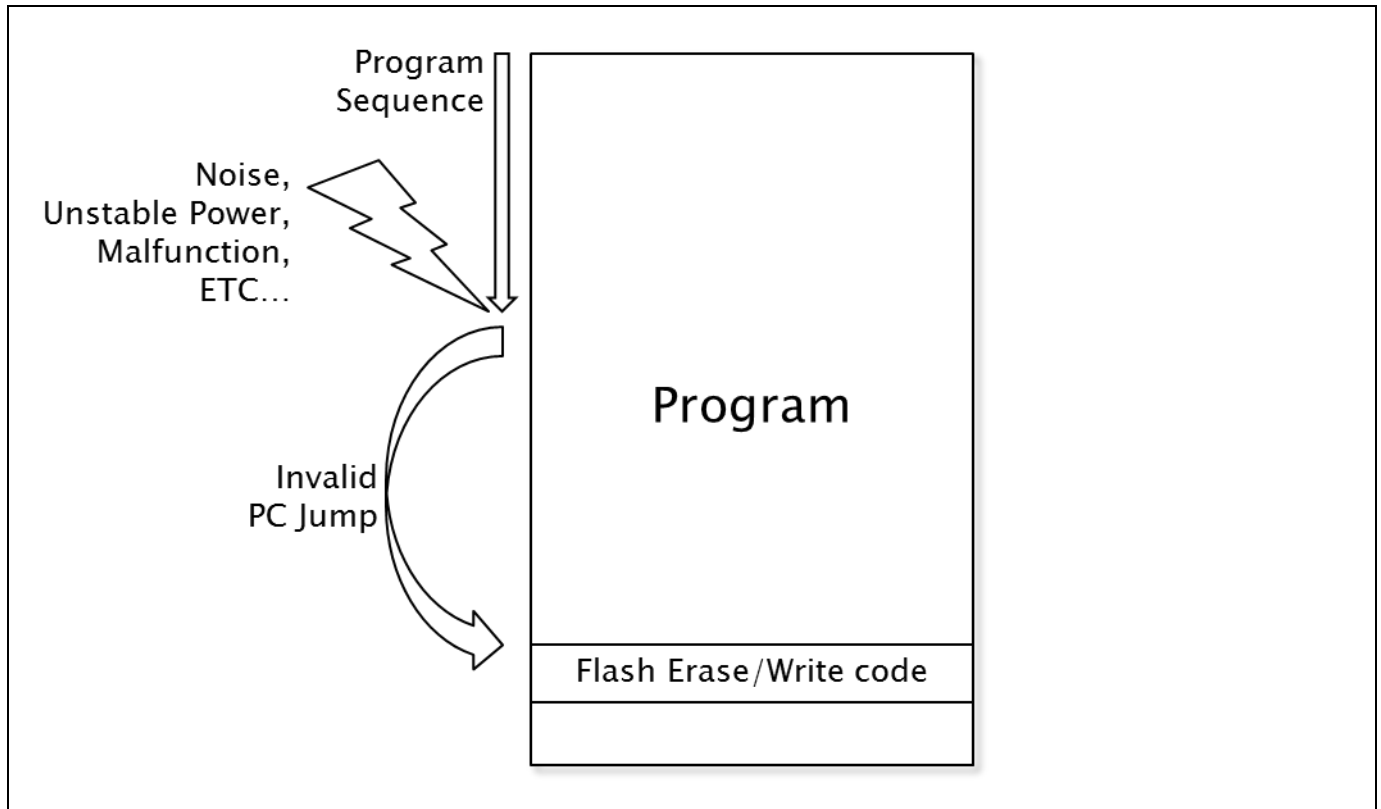
In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11→F1 (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the destination address.

The CJNE instructions use the abbreviation #d for immediate data; other instructions use #data.

## 17.2 Flash Protection for Invalid Erase/Write

### ➤ Overview

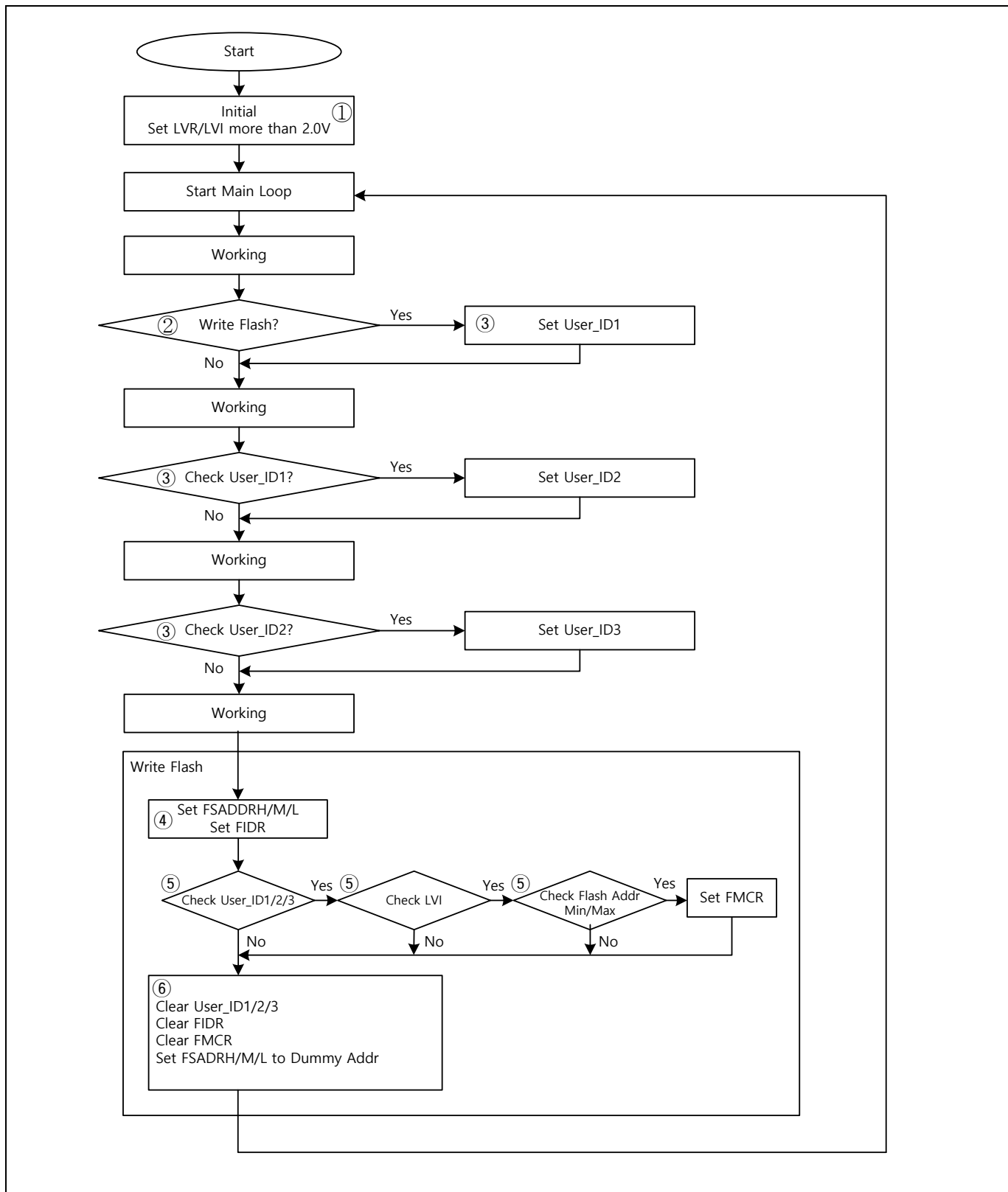
This is example to prevent changing code or data in flash by abnormal operation(noise, unstable power, malfunction, etc...).



### ➤ How to protect the flash

- Divide into decision and execution to Erase/Write in flash.
  - Check the program sequence from decision to execution in order of precedence about Erase/Write.
  - Setting the flags in program and check the flags in main loop at the end
  - When the Flash Erase/Write is executed, check the flags. If not matched, do not execute.
- Check the range of Flash Sector Address
  - If the flash sector address is outside of specific area, do not execute.
- Use the Dummy Address
  - Set the flash sector address to dummy address in usually run time.
  - Change the flash sector address to real area range shortly before Erase/Write.
  - Even if invalid Erase/Write occurred, it will be Erase/Write in dummy address in flash.
- Use the LVR/LVI
  - Unstable or low powers give an adverse effect on MCU. So use the LVR/LVI

➤ Flowchart



## ➤ Descript of Flowchart

- ① Initialization
  - Set the LVR/LVI  
Check the power by LVR/LVI and do not execute under unstable or low power.
  - Initialize User\_ID1/2/3
  - Set Flash Sector Address High/Middle/Low to Dummy address  
Dummy address is set to unused area range in flash.
- ② Decide to Write
  - When the Erase/Write are determined, set flag. Do not directly Erase/Write in flash.
  - Make the user data.
- ③ Check and Set User\_ID1/2/3
  - In the middle of source, insert code which can check and set the flags.
  - By setting the User\_ID 1/2/3 sequentially and identify the flow of the program.
- ④ Set Flash Sector Address
  - Set address to real area range shortly before Erase/Write in flash.  
Set to Dummy address after Erase/Write  
Even if invalid work occurred, it will be Erase/Write in Dummy address in flash.
- ⑤ Check Flags
  - If every flag(User\_ID1/2/3, LVI, Flash Address Min/Max) was set, than do Erase/Write.
  - If the Flash Sector Address is outside of Min/Max, do not execute
  - Address Min/Max is set to unused area.
- ⑥ Initialize Flags
  - Initialize User\_ID1/2/3
  - Set Flash Sector Address to Dummy Address
- Sample Source
  - Refer to the ABOV homepage.
  - It is created based on the MC97F2664.
  - Each product should be modified according to the Page Buffer Size and Flash Size

## ➤ Etc

- Protection by Configure option
  - Set flash protection by MCU Write Tool(OCD, PGM+, etc...)  
Vector Area :  
00H~FFH  
Specific Area :  
3.7k Bytes (Address 0100H – 0FFFH)  
1.7k Bytes (Address 0100H – 07FFFH)  
768 Bytes (Address 0100H – 03FFFH)  
256 Bytes (Address 0100H – 01FFFH)
  - The range of protection may be different each product.

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