32-bit Cortex-M3 based
Programmable Motor Controller

Flash 128KB / SRAM 12KB

AC33M8128
AC33M8128L
AC33M6128L

USER MANUAL

Version 1.23

2023.05.08.

Revision History:

Date	By	Version	Description
2012/10/17	MG Kim	0.0	File created
2014/1/20	BC Lee	0.1	Temperature spec was changed with the range of -40~+85℃.
2014/2/3	BC Lee	0.2	LQFP-80, LQFP-64 PKG were added
2014/2/7	BC Lee	0.3	Typo errors were corrected
2014/3/5	LJ Deng	0.4	Detail description of following contects were corrected: RSSR,PRER1,PER,PCER,CSCR,WDTCON,UnIER,MPWM and pin description of PA11
2014/3/17	BC Lee	0.5	Added current consumption in DC characteristic
2014/12/3	BC Lee	0.6	Correct LQFP-80 size as 12x12
2015/2/6	SJ Park, BC Lee	0.7	Review, Maximum I/O Current
2015/8/31	SJ Park	0.8	Typo errors were corrected Explanation of FM.MR was modified.
2015/12/15	SJ Park	0.9	Power down mode was removed. Explanation of Reset was added.
2015/01/07	SJ Park, MJ Kim	1.0	Clock configuration procedure was modified.
2016/03/25	MJ Kim	1.1	Modified I_{OL}/I_{OH}, V_{OL}/V_{OH} spec in DC characteristic
2016/06/07	SJ Park	1.2.0	Added debounce logic description in PCU
2017/04/06	SJ Park	1.2.1	Description of SMR contects was corrected PCC.MR's PC11(BOOT) reset value changed.
2017/10/09	DH Shin	1.2.2	Modified Operation Frequency of PLL. (80MHz → 72MHz)
2018/08/28	Donghyo.Shin	1.2.3	Descriptions of bit field are modified in ADn.TRG2 Description of TRGSCR bits is modified in ADn.MR
2023/05/08	TW Lim	1.23	Changed the format of the revision number to "X.YZ" according to internal policy.

SECTION 1.INTRODUCTION

CHAPTER 1. OVERVIEW

1.1 INTRODUCTION

AC33MX128 is special purpose microcontroller for motor application. This microcontroller brings high-performance 32-bit computing to low cost system solution.

AC33MX128 provides 3-phase PWM generator units which are suitable to inverter motor drive system. Built-in two channels of 3-phase PWM generators control two inverter motors simultaneously.

Three 12-bit high speed ADC units with 16-channel analog multiplexed inputs support to get feedback information from motor. It can control up to two inverter motors or one inverter motor and PFC (Power Factor Correction) function simultaneously.

On-chip four operational AMPs and four analog comparators help to measure analog input signals. The Op-Amp can amplify input signal to proper signal range and transfer it to ADC input channel. The comparator monitors external signals and helps to makes internal emergency signal

Powerful and various external serial interface engines help to communicate with on-board sensors and devices.

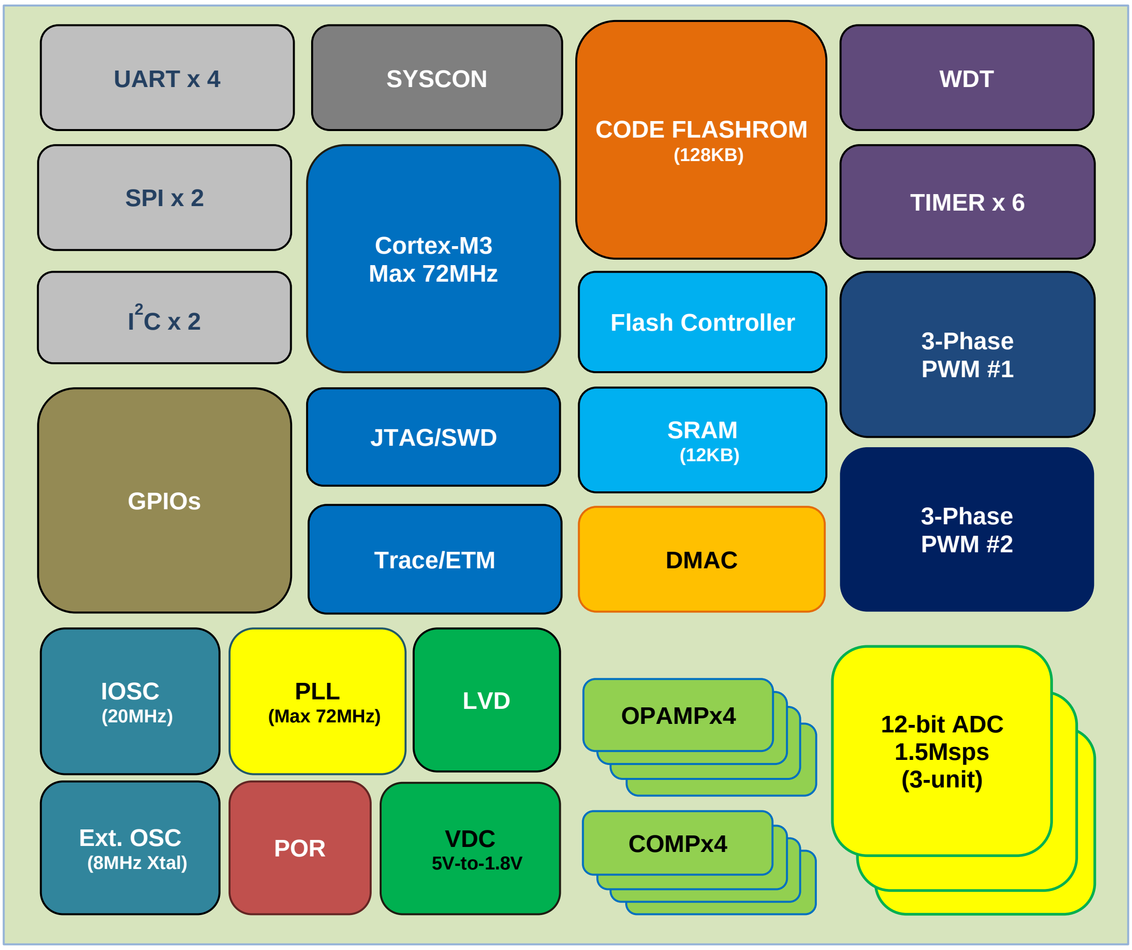
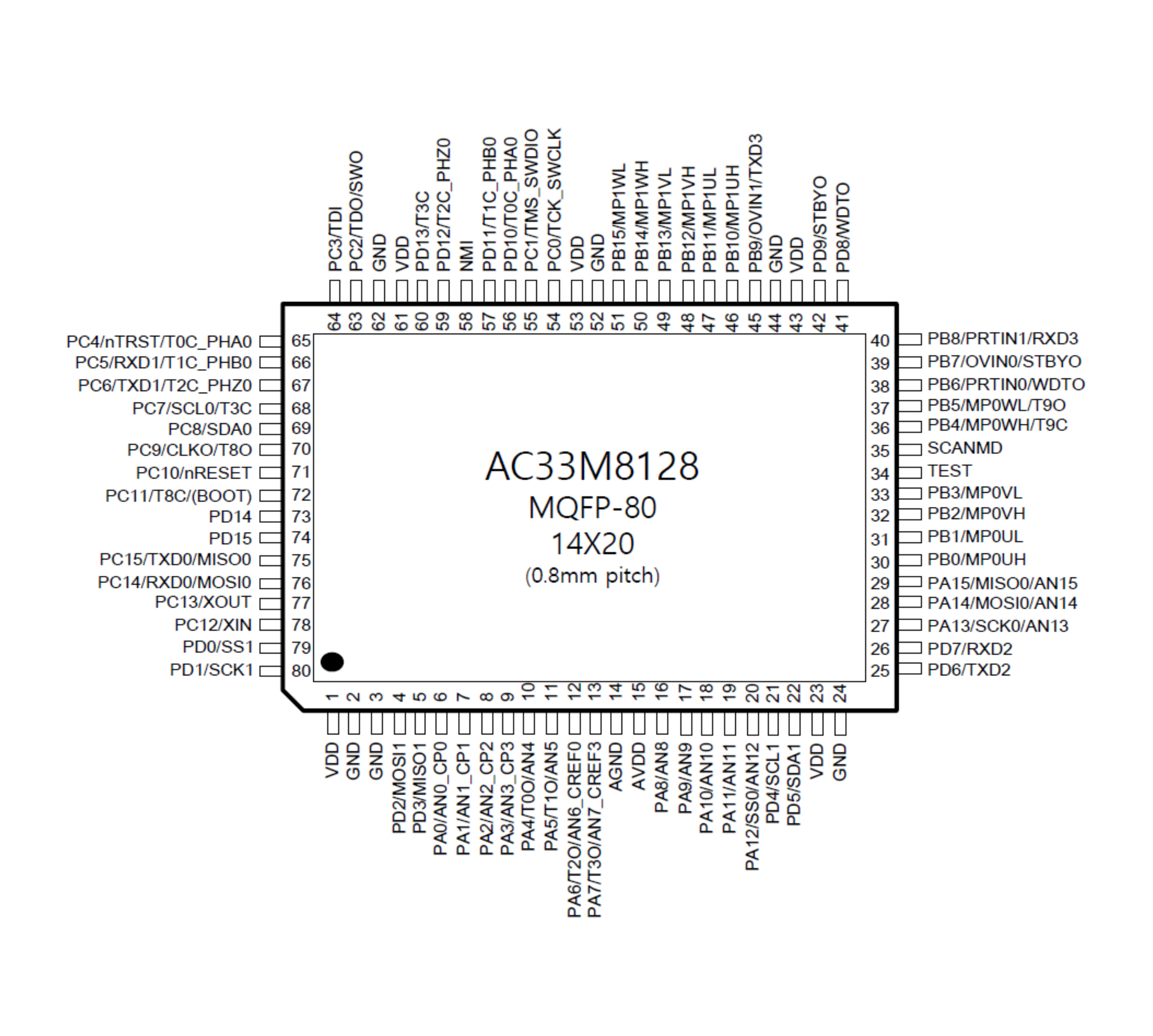


Figure 1.1. Block Diagram

Figure 1.2. Pin layout (MQFP-80)



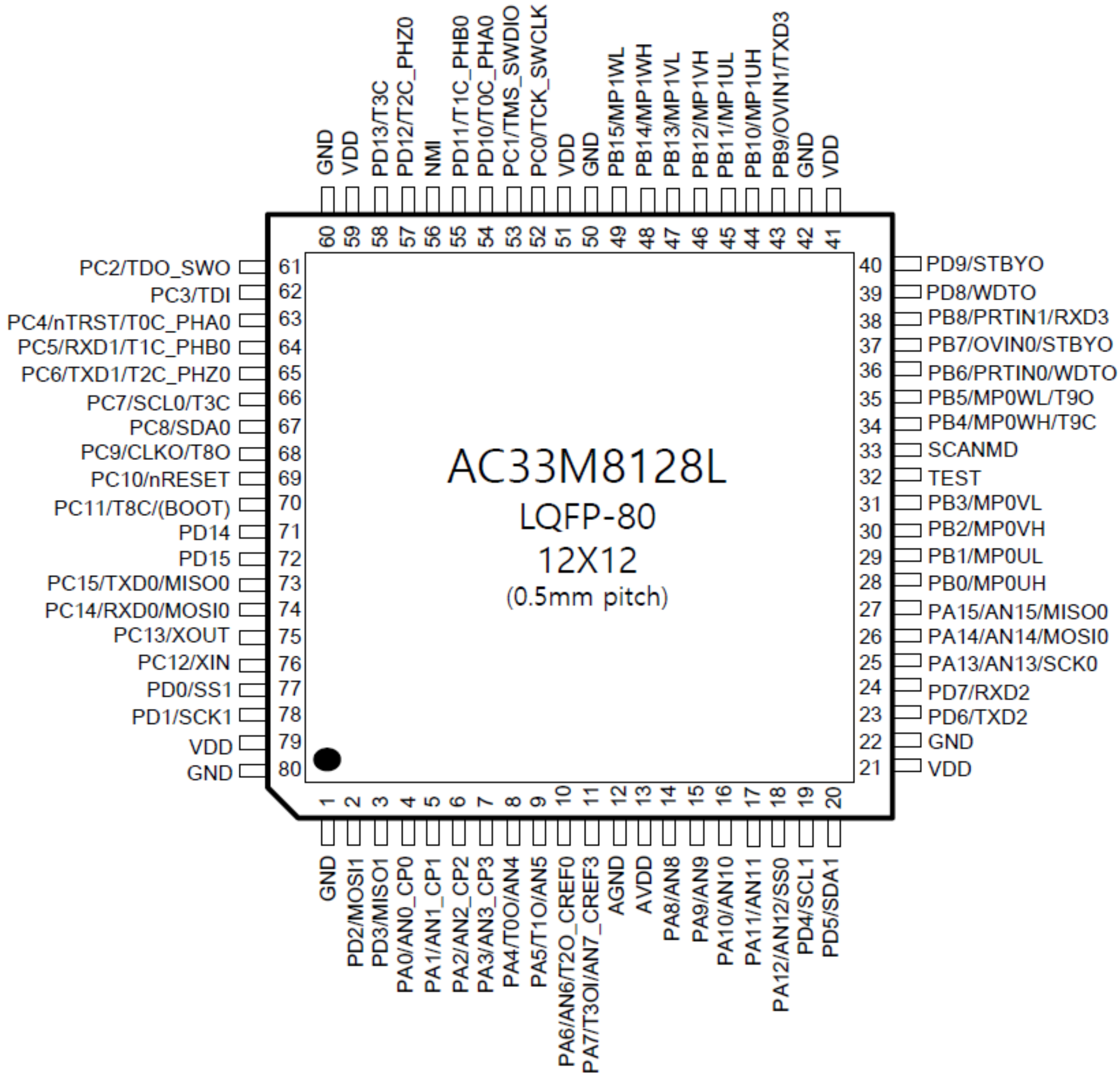
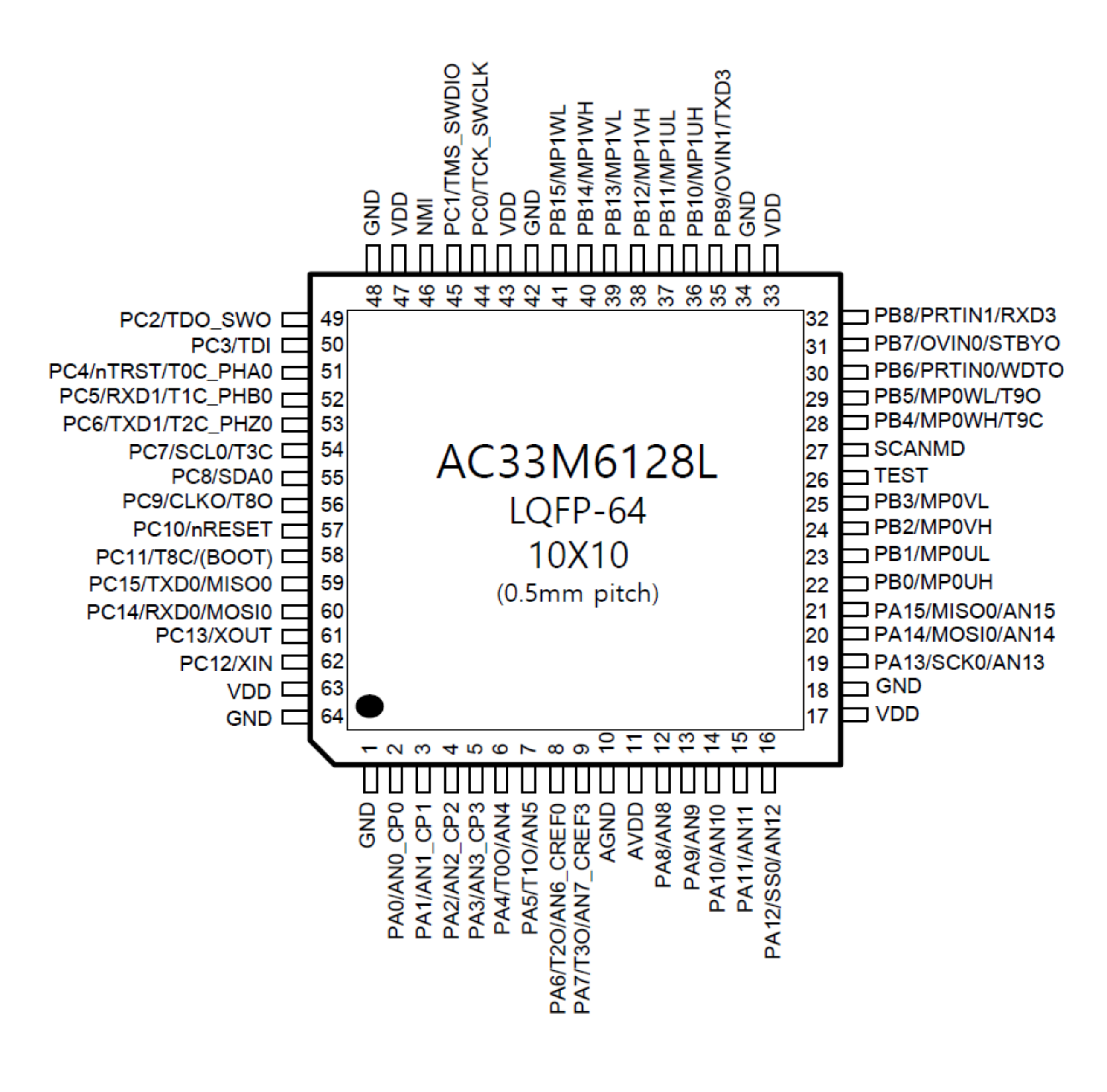


Figure 1.3. Pin layout (LQFP-80)

Figure 1.4. Pin layout (LQFP-64)



1.2 Product Features

Product features of AC33MX128 are as below:

- High Performance Low-power Cortex-M3 Core
- 128KB Code Flash Memory with Cache function
- 12KB SRAM
- 3-Phase Motor PWM with ADC triggering function
  - 2 Channels
- 1.5Msps high-speed ADC with burst conversion function
  - 2 or 3 units with 16 channel input
- Built-in PGA(Programmable Gain Amplifier) for ADC inputs
  - 4 Channels
    - 3 Channels for 3 shunt resistor configuration
    - 1 Channel for 1 shunt resistor configuration
- Built-in Analog Comparator
  - 4 channels
    - 3 channels for 3 shunt resistor configuration
    - 1 channel for 1 shunt resistor configuration
- System Fail-Safe function by Clock Monitoring
- XTAL OSC Fail monitoring
- Precision Internal Oscillator Clock (20MHz ±3%)
- Watchdog Timer
- Six General Purpose Timers
- Quadrature Encoder Counter
- External communication ports: 4 UARTs, 2 I^2Cs, 2 SPIs
- High current driving port for UART photo couplers
- Debug and Emergency stop function
- Real-time Monitoring function support for more effective development
- JTAG and SWD in-circuit debugger
- Various Memory size and Package options
  - MQFP-80, LQFP-80, LQFP-64
- Industrial grade operating temperature (-40 ~ +85℃)

Table1.1. Device type

Part Number	Flash	SRAM	UART	SPI	I2C	MPWM	ADC	I/O PORT	PKG
AC33M8128	128KB	12KB	4	2	2	2	3-unit 16 ch	64	MQFP-80
AC33M8128L			4	2	2	2		64	LQFP-80
AC33M6128L			2	2	1	2		48	LQFP-64

1.3 ARCHITECTURE

1.3.1 Block Diagram

AC33MX128 Block diagram.

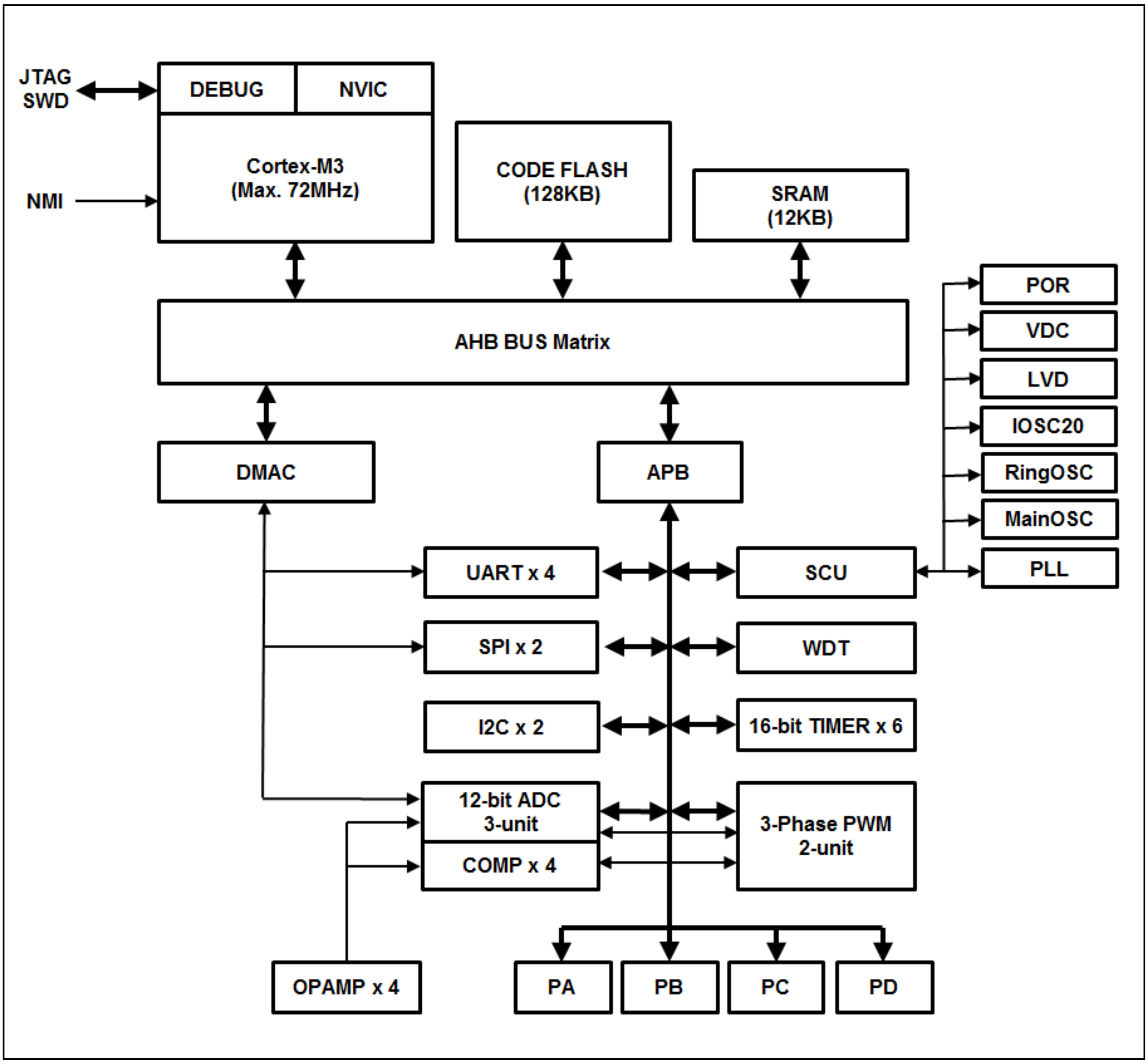


Figure1.5. Internal Block Diagram

1.3.2 Functional Description

The following section provides an overview of the features of AC33MX128 microcontroller.

ARM Cortex-M3

ARM powered Cortex-M3 Core based on v7M architecture which is optimized for small size and low power system.
On core system timer (SYSTICK) provides a simple 24 bit timer easy to manage the system operation
Thumb-compatible Thumb-2 only instruction set processor core makes code high-density.
Hardware division and single-cycle multiplication is present
Integrated Nested Vectored Interrupt Controller (NVIC) providing deterministic interrupt handling.
Full feature of debug solution is provided – JTAG and SWD, FPB, DWT, ITM and TPIU.
Max 72MHz operating frequency with zero wait execution

Nested Vector-Interrupt Controller (NVIC)

The ARM Nested Vectored Interrupt Controller (NVIC) on the ARM Cortex-M3 core is included which handles all the internal and external exceptions. When interrupt condition is detected, the processor state is automatically stored to the stack and automatically restored from the stack at the end of interrupt service routine.

The vector is fetched in parallel to the state saving, which enables efficient interrupt entry.

The processor supports tail-chaining, which enables back-to-back interrupts to be performed without the overhead of state saving and restoring.

128KB Internal Code Flash Memory

The AC33MX128 provides internal 128KB code flash memory and its controller. This is enough to program motor algorithm and general control the system. Self-programming is available and ISP and JTAG programming is also supported in boot or debugging mode.

Instruction and data cache buffer are present and overcome the low bandwidth flash memory.

12KB 0-wait Internal SRAM

On chip 12KB 0-wait SRAM can be used for working memory space and program code can be loaded on this SRAM.

Boot Logic

The smart boot logic supports the flash programming. The AC33MX128 can be entered by external boot pin and UART and SPI programming are available in boot mode. UART0 or SPI0 is used in boot mode communication.

System Control Unit (SCU)

The SCU block manages internal power, clock, reset and operation mode. It also controls analog blocks (INTOSC, VDC and LVD)

32-bit Watchdog Timer (WDT)

The watchdog timer performs system monitoring function. It will generate internal reset or interrupt to notice abnormal status of the system.

Multi-purpose 16bit Timer

Six-channel 16-bit general purpose timers supports below functions.

- Periodic timer mode
- Counter mode
- PWM mode
- Capture mode

PWM Generator

3-phase PWM generator 2 channels are implemented. 16 bit up/down counter with prescaler supports both of triangular and saw tooth waveform.

The PWM generate internal ADC trigger signal to measure the signal on time.

Dead time insertion and emergency stop functionality help that the chip and system are under safety conditions.

Serial Peripheral Interface (SPI)

Synchronous serial communication is provided with SPI block. The AC33MX128 has 2 channel SPI modules. It has DMA function supported by DMA controller. Transfer data moved to/from memory area without CPU operation.

Boot mode will use this SPI block to download flash program.

Inter-Integrated Circuit Interface (I^2C)

The AC33MX128 has 2 channel I^2C block and it support up to 400KHz I^2C communication. The master and the slave mode supported.

Universal Asynchronous Receiver/Transmitter (UART)

The AC33MX128 has 4 channels UART block. For accurate baud rate control, the fractional baud rate generator is provided.

It has DMA function supported by DMA controller. Transfer data moved to/from memory area without CPU operation.

General PORT I/Os

16 bits PA, PB, PC, PD ports are available and provide multiple functionality

- General I/O port
- Independent bit set/clear function
- External interrupt input port
- Pull-up/Open-drain
- On chip Debounce Filter

12-bit Analog-to-Digital Converter (ADC)

3 built-in ADCs can convert analog signal up to 1usec conversion rate. 16-channel analog mux and OP-AMP provides various combinations from external analog signals.

Operational Amplifier (OPAMP)

4 built-in OPAMPs amplify analog signals up to x8.74 gain.

Analog Comparator (COMP)

4 built-in analog comparators.

1.4 Pin Description

Below pin configuration is temporary one and 16 pins are reserved for power/ground pair and dedicated pins. The configuration including pin ordering will be changed in the future.

Table1.2. Pin Description

Pin No			Pin Name	Type	Description	Remark
MQFP80	LQFP80	LQFP64				
1	79	63	VDD	P	VDD	
2	80	64	GND	P	Ground	
3	1	1	GND	P	Ground	
4	2	-	PD2	IOUS	PORT D Bit 2 Input/Output	
			MOSI1	I/O	SPI Channel 1 Master Out / Slave In	
5	3	-	PD3*	IOUS	PORT D Bit 3 Input/Output	
			MISOI1	I/O	SPI Channel 1 Master In / Slave Out	
6	4	2	PA0*	IOUS	PORT A Bit 0 Input/Output	
			AN0	IA	Analog Input 0	
			COMP0	IA	Comparator 0 Input	
7	5	3	PA1*	IOUS	PORT A Bit 1 Input/Output	
			AN1	IA	Analog Input1	
			COMP1	IA	Comparator 1 Input	
8	6	4	PA2*	IOUS	PORT A Bit 2 Input/Output	
			AN2	IA	Analog Input 2	
			COMP2	IA	Comparator 2 Input	
9	7	5	PA3*	IOUS	PORT A Bit 3 Input/Output	
			AN3	IA	Analog Input 3	
			COMP3	IA	Comparator 3 Input	
10	8	6	PA4*	IOUS	PORT A Bit 4 Input/Output	
			T0O	Output	Timer 0 Output	
			AN4	IA	Analog Input 4	
11	9	7	PA5*	IOUS	PORT A Bit 5 Input/Output	
			T1O	Output	Timer 1 Output	
			AN5	IA	Analog Input 5	
12	10	8	PA6*	IOUS	PORT A Bit 6 Input/Output	
			T2O	Output	Timer 2 Output	
			AN6	IA	Analog Input 6	
			CREF0	IA	Comparator 0 Reference Input	
13	11	9	PA7*	IOUS	PORT A Bit 7 Input/Output	
			TRACED3	Output	ETM Trace Data 3	
			T3O	Output	Timer 3 Output	
			AN7	IA	Analog Input 7	
			CREF3	IA	Comparator 3 Reference Input	
14	12	10	AGND	P	Analog Ground	
15	13	11	AVDD	P	Analog VDD	
16	14	12	PA8*	IOUS	PORT A Bit 8 Input/Output	
			TRACECLK	Output	ETM Trace Clock	
			AD0O	Output	ADC0 Start Signal	
			AN8	IA	Analog Input 8	
17	15	13	PA9*	IOUS	PORT A Bit 9 Input/Output	
			TRACED0	Output	ETM Trace Data 0	
			AD1O	Output	ADC1 Start Signal	
			AN9	IA	Analog Input 9	

18	16	14	PA10*	IOUS	PORT A Bit 10 Input/Output	
			TRACED1	Output	ETM Trace Data 1	
			AD2O	Output	ADC2 Start Signal	
			AN10	IA	Analog Input 10	
19	17	15	PA11*	IOUS	PORT A Bit 11 Input/Output	
			TRACED2	Output	ETM Trace Data 2	
			AN11	IA	Analog Input 11	
20	18	16	PA12*	IOUS	PORT A Bit 12 Input/Output	
			SS0	I/O	SPI0 Slave Select signal	
			AD2I	Input	ADC2 Start Input signal	
			AN12	IA	Analog Input 12	
21	19	-	PD4	IOUS	PORT D Bit 4 Input/Output	
			SCL1	Output	I2C Channel 1 SCL In/Out	
22	20	-	PD5	IOUS	PORT D Bit 5 Input/Ouput	
			SDA1	Output	I2C Channel 1 SDA In/Out	
23	21	17	VDD	P	VDD	
24	22	18	GND	P	Ground	
25	23	-	PD6*	IOUS	PORT D Bit 6 Input/Ouput	
			TXD2	Output	UART Channel 2 TxD Input	
			AD0I	Input	ADC0 Start Input signal	
26	24	-	PD7*	IOUS	PORT D Bit 7 Input/Ouput	
			RXD2	Input	UART Channel 2 RxD Input	
			AD1I	Input	ADC1 Start Input signal	
27	25	19	PA13*	IOUS	PORT A Bit 13 Input/Output	
			SCK0	I/O	SPI0 Data Clock Input/Output	
			AN13	IA	Analog Input 13	
28	26	20	PA14*	IOUS	PORT A Bit 14 Input/Output	
			MOSI0	I/O	SPI0 Master-Output/Slave-Input Data signal	
			AN14	IA	Analog Input 14	
29	27	21	PA15*	IOUS	PORT A Bit 15 Input/Output	
			MISO0	I/O	SPI0 Master-Input/Slave-Output Data signal	
			AN15	IA	Analog Input 15	
30	28	22	PB0	IOUS	PORT B Bit 0 Input/Output	
			PWM0H0	Output	PWM0 H0 Output	
31	29	23	PB1	IOUS	PORT B Bit 1 Input/Output	
			PWM0L0	Output	PWM0 L0 Output	
32	30	24	PB2	IOUS	PORT B Bit 0 Input/Output	
			PWM0H1	Output	PWM0 H1 Output	
33	31	25	PB3	IOUS	PORT B Bit 1 Input/Output	
			PWM0L1	Output	PWM0 L1 Output	
34	32	26	TEST	Input	Test-mode Input (Always tied ‘L’)	Pull-down
35	33	27	SCANMD	Input	Scan-mode Input (Always tied ‘L’)	Pull-down
36	34	28	PB4	IOUS	PORT B Bit 4 Input/Output	
			PWM0H2	Output	PWM0 H2 Output	
			T9C	I/O	Timer 9 Clock/Capture Input	
37	35	29	PB5	IOUS	PORT B Bit 5 Input/Output	
			PWM0L2	Output	PWM0 L2 Output	
			T9O	I/O	Timer 9 Output	
38	36	30	PB6	IOUS	PORT B Bit 6 Input/Output	
			PRTIN0	Input	PWM0 Protection Input signal 0	
			WDTO	Output	WDT Output	
39	37	31	PB7	IOUS	PORT B Bit 7 Input/Output	
			OVIN0	Input	PWM0 Over-voltage put signal 1	

			STBYO	Output	Power-down mode indication signal	
40	38	32	PB8	IOUS	PORT B Bit 8 Input/Output	
			PRTIN1	Input	PWM1 Protection Input signal 0	
			RXD3	Input	UART3 RXD Input	
41	39	-	PD8	IOUS	PORT D Bit 8 Input/Output	
			WDTO	Output	WDT Output	
42	30	-	PD9	IOUS	PORT D Bit 9 Input/Output	
			STBYO	Output	Power-down mode indication signal	
43	41	33	VDD	P	VDD	
44	42	34	GND	P	Ground	
45	43	35	PB9	IOUS	PORT B Bit 9 Input/Output	
			OVIN1	Input	PWM1 Over-voltage Input signal 1	
			TXD3	Output	UART3 TXD Output	
46	44	36	PB10	IOUS	PORT B Bit 10 Input/Output	
			PWM1H0	Output	PWM Channel 1 Phase 0 H-side Output	
47	45	37	PB11	IOUS	PORT B Bit 11 Input/Output	
			PWM1L0	Output	PWM Channel 1 Phase 0 L-side Output	
48	46	38	PB12	IOUS	PORT B Bit 12 Input/Output	
			PWM1H1	Output	PWM Channel 1 Phase 1 H-side Output	
49	47	39	PB13	IOUS	PORT B Bit 13 Input/Output	
			PWM1L1	Output	PWM Channel 1 Phase 1 L-side Output	
50	48	40	PB14	IOUS	PORT B Bit 14 Input/Output	
			PWM1H2	Output	PWM Channel 1 Phase 2 H-side Output	
51	49	41	PB15	IOUS	PORT B Bit 15 Input/Output	
			PWM1L2	Output	PWM Channel 1 Phase 2 L-side Output	
52	50	42	GND	P	Ground	
53	51	43	VDD	P	VDD	
54	52	44	PC0	IOUS	PORT C Bit 0 Input/Output	
			TCK/SWCK	Input	JTAG TCK, SWD Clock Input	
55	53	45	PC1	IOUS	PORT C Bit 1 Input/Output	
			TMS/SWDIO	I/O	JTAG TMS, SWD Data Input/Output	
56	54	-	PD10	IOUS	PORT D Bit 10 Input/Output	
			AD0SOC	Output	ADC0 Start-of-Conversion	
			T0C/PHA	Input	Timer 0 Clock/Capture/Phase-A Input	
57	55	-	PD11	IOUS	PORT D Bit 10 Input/Output	
			AD0EOC	Output	ADC0 End-of-Conversion	
			T1C/PHB	Input	Timer 1 Clock/Capture/Phase-B Input	
58	56	46	NMI	Input	Non-maskable Interrupt Input	
59	57	-	PD12	IOUS	PORT D Bit 12 Input/Output	
			AD1SOC	Output	ADC1 Start-of-Conversion	
			T2C/PHZ0	Input	Timer 2 Clock/Capture/Phase-Z Input	
60	58	-	PD13	IOUS	PORT D Bit 13 Input/Output	
			AD1EOC	Output	ADC1 End-of-Conversion	
			T3C	Input	Timer 3 Clock/Capture Input	
61	59	47	VDD	P	VDD	
62	60	48	GND	P	Ground	
63	61	49	PC2	IOUS	PORT C Bit 2 Input/Output	
			TDO/SWO	Output	JTAG TDO, SWO Output	
64	62	50	PC3	IOUS	PORT C Bit 3 Input/Output	
			TDI	Input	JTAG TDI Input	
65	63	51	PC4	IOUS	PORT C Bit 4Input/Output	
			nTRST	Input	JTAG nTRST Input	

			T0C/PHA	Input	Timer 0 Clock/Capture/Phase-A Input	
66	64	52	PC5	IOUS	PORT C Bit 5Input/Output	
			RXD1	Input	UART1 RXD Input	
			T1C/PHB	Input	Timer 1 Clock/Capture/Phase-B Input	
67	65	53	PC6	IOUS	PORT C Bit 6Input/Output	
			TXD1	Output	UART1 TXD Output	
			T2C/PHZ	Input	Timer 2 Clock/Capture/Phase-Z Input	
68	66	54	PC7	IOUS	PORT C Bit 7Input/Output	
			SCL0	Output	I^2C Channel 0 SCL In/Out	
			T3C	Input	Timer 3 Clock/Capture input	
69	67	55	PC8	IOUS	PORT C Bit 8 Input/Output	
			SDA0	Output	I^2C Channel 0 SDA In/Out	
70	68	56	PC9	IOUS	PORT C Bit 9 Input/Output	
			CLKO	Output	System Clock Output	
			T8O	Output	Timer 8 Output	
71	69	57	PC10	IOUS	PORT C Bit 10 Input/Output	
			nRESET	Input	External Reset Input	Pull-up
72	70	58	PC11	IOUS	PORT C Bit 11 Input/Output	
			BOOT	Input	Boot mode Selection Input	
			T8C	Input	Timer 8 Clock/Capture Input	
73	71	-	PD14	IOUS	PORT D Bit 14 Input/Output	
			AD2SOC	Output	ADC2 Start-of-Conversion Output signal	
74	72	-	TD15	IOUS	PORT D Bit 15 Input/Output	
			AD2EOC	Output	ADC2 Start-of-Conversion Output signal	
75	73	59	PC15	IOUS	PORT C Bit 14 Input/Output	
			TXD0	Output	UART0 TXD Output	
			MISO0	I/O	SPI0 Master-Input/Slave-Output	
76	74	60	PC14	IOUS	PORT C Bit 14 Input/Output	
			RXD0	Input	UART0 RXD Input	
			MOSI0	I/O	SPI0 Master-Output/Slave-Input	
			VMARGIN	OA	Not used. (test purpose)	
77	75	61	PC13	IOUS	PORT C Bit 13 Input/Output	
			XOUT	OA	External Crystal Oscillator Output	
78	76	62	PC12	IOUS	PORT C Bit 12 Input/Output	
			XIN	IA	External Crystal Oscillator Input	
79	77	-	PD0	IOUS	PORT D Bit 0 Input/Output	
			SS1	I/O	SPI1 Slave Select	
80	78	-	PD1	IOUS	PORT D Bit 1 Input/Output	
			SCK1	I/O	SPI1 Clock Input/Output	

*Notation: I=Input, O=Output, U=Pull-up, D=Pull-down,
S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
(*) Selected pin function after reset condition
Pin order may be changed with revision notice

1.5 Memory Map

Memory map

Address		Region
0x0000_0000	0x0001_FFFF	Code Flash ROM (128KB)
0x0002_0000	0x1FFE_FFFF	Reserved
0x1FFF_0000	0x1FFF_07FF	Boot ROM
0x1FFF_0800	0x1FFF_FFFF	Reserved
0x2000_0000	0x2000_2FFF	SRAM (12K)
0x2000_3000	0x2FFF_FFFF	Reserved
0x2200_0000	0x23FF_FFFF	SRAM Bit-banding region
0x2400_0000	0x2FFF_FFFF	Reserved
0x3000_0000	0x3001_FFFF	Code Flash ROM(Mirrored) (128KB)
0x3002_0000	0x3002_07FF	Boot ROM (Mirrored)
0x3003_0000	0x3003_07FF	OTP ROM (Mirrored)
0x3004_0000	0x3FFF_FFFF	Reserved
0x4000_0000	0x4000_FFFF	Peripherals
0x4001_0000	0x41FF_FFFF	Reserved
0x4200_0000	0x43FF_FFFF	Peripherals bit-banding region
0x4400_0000	0x5FFF_FFFF	Reserved
0x6000_0000	0x9FFF_FFFF	External Memory (Not supported)
0xA000_0000	0xDFFF_FFFF	External Device (Not supported)
0xE000_0000	0xE003_FFFF	Private peripheral bus: Internal
0xE004_0000	0xE00F_FFFF	Private peripheral bus: Debug/External
0xE010_0000	0xFFFF_FFFF	Vendor Specific

Figure1.6. Main Memory MAP

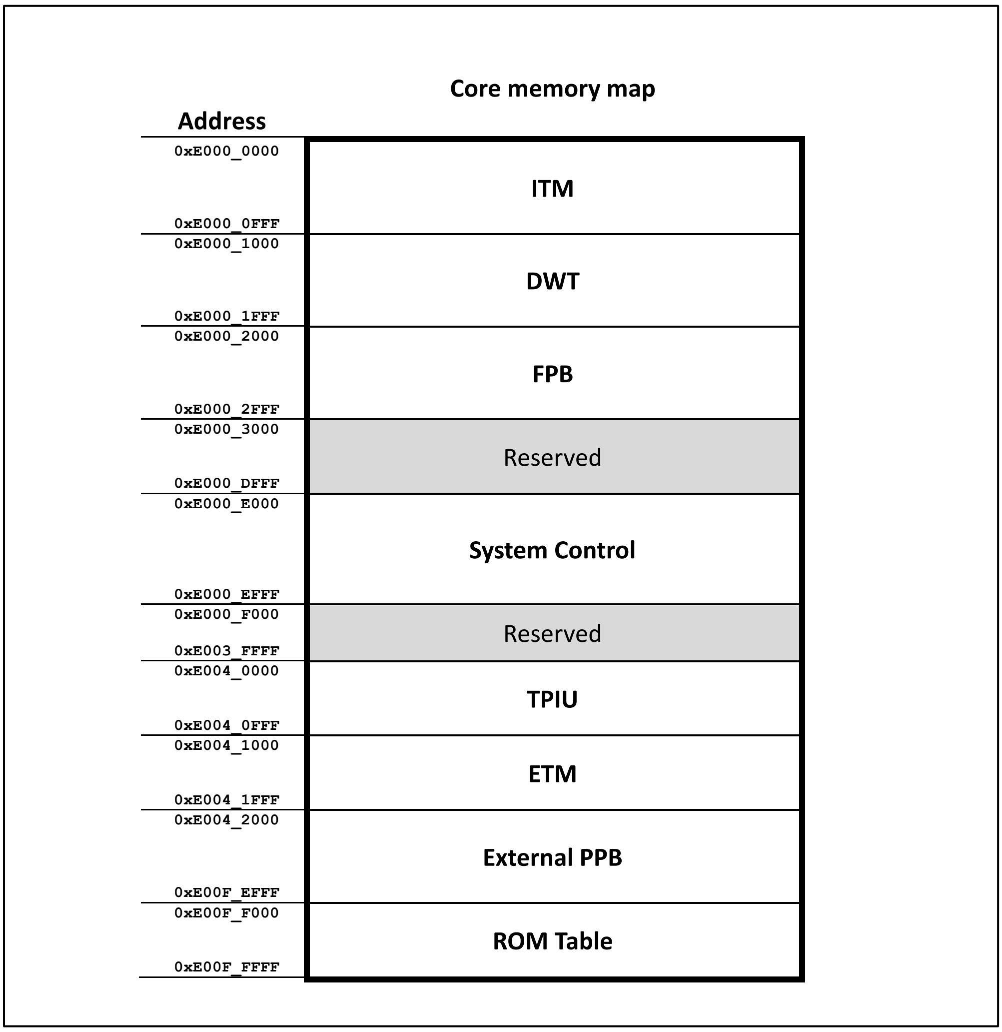


Figure1.7. Cortex-M3 Private Memory Map

Address	Peripheral map
0x4000_0000	SCU
0x4000_0100	FMC
0x4000_0200	WDT
0x4000_0300	Reserved
0x4000_0400	DMAC(15)
0x4000_0500	Reserved
0x4000_1000	PCU
0x4000_2000	GPIO(A,B,C,D)
0x4000_3000	TIMER(6)
0x4000_4000	MPWM0
0x4000_5000	MPWM1
0x4000_6000	Reserved
0x4000_8000	UART0
0x4000_8100	UART1
0x4000_8200	UART2
0x4000_8300	UART3
0x4000_8600	Reserved
0x4000_9000	SPI0
0x4000_9100	SPI1
0x4000_9200	Reserved
0x4000_A000	I^2C0
0x4000_A100	I^2C1
0x4000_A200	Reserved
0z4000_B000	ADC0
0x4000_B100	ADC1
0x4000_B200	ADC2
0x4000_B300	AFE
0x4000_B400 – 0x4000_FFFF	Reserved

Figure1.8. Peripheral Memory Map

CHAPTER 2. CPU

2.1 Cortex-M3 Core

CPU core is supported from the ARM Cortex-M3 processor which provides a high-performance, low-cost platform. Document DDI337 from ARM provides detail information of Cortex-M3.

2.2 Interrupt Controller

Table2.1. Interrupt Vector Map

Priority	Vector Address	Interrupt Source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Address
-14	0x0000_0008	NMI Handler
-13	0x0000_000C	Hard Fault Handler
-12	0x0000_0010	MPU Fault Handler
-11	0x0000_0014	BUS Fault Handler
-10	0x0000_0018	Usage Fault Handler
-9	0x0000_001C	Reserved
-8	0x0000_0020	
-7	0x0000_0024	
-6	0x0000_0028	
-5	0x0000_002C	SVCall Handler
-4	0x0000_0030	Debug Monitor Handler
-3	0x0000_0034	Reserved
-2	0x0000_0038	PenSV Handler
-1	0x0000_003C	SysTick Handler
0	0x0000_0040	LVDDETECT
1	0x0000_0044	SCLKFAIL
2	0x0000_0048	XOSCFAIL
3	0x0000_004C	WDT
4	0x0000_0050	Reserved
5	0x0000_0054	TIMER0
6	0x0000_0058	TIMER1
7	0x0000_005C	TIMER2
8	0x0000_0060	TIMER3
9	0x0000_0064	Reserved
10	0x0000_0068	
11	0x0000_006C	
12	0x0000_0070	
13	0x0000_0074	TIMER8
14	0x0000_0078	TIMER9
15	0x0000_007C	Reserved
16	0x0000_0080	GPIOAE
17	0x0000_0084	GPIOAO
18	0x0000_0088	GPIOBE
19	0x0000_008C	GPIOBO
20	0x0000_0090	GPIOCE
21	0x0000_0094	GPIOCO
22	0x0000_0098	Reserved

23	0x0000_009C	GPIODO
24	0x0000_00A0	MPWM0
25	0x0000_00A4	MPWM0PROT
26	0x0000_00A8	MPWM0OVV
27	0x0000_00AC	MPWM1
28	0x0000_00B0	MPWM1PROT
29	0x0000_00B4	MPWM1OVV
30	0x0000_00B8	Reserved
31	0x0000_00BC	
32	0x0000_00C0	SPI0
33	0x0000_00C4	SPI1
34	0x0000_00C8	Reserved
35	0x0000_00CC	
36	0x0000_00D0	I2C0
37	0x0000_00D4	I2C1
38	0x0000_00D8	UART0
39	0x0000_00DC	UART1
40	0x0000_00E0	UART2
41	0x0000_00E4	UART3
42	0x0000_00E8	Reserved
43	0x0000_00EC	ADC0
44	0x0000_00F0	ADC1
45	0x0000_00F4	ADC2
46	0x0000_00F8	COMP0
47	0x0000_00FC	COMP1
48	0x0000_0100	COMP2
49	0x0000_0104	COMP3
50	0x0000_0108	Reserved
51	0x0000_010C	
52	0x0000_0110	
53	0x0000_0114	
54	0x0000_0118	
55	0x0000_011C	
56	0x0000_0120	
57	0x0000_0124	
58	0x0000_0128	
59	0x0000_012C	
60	0x0000_0130	
61	0x0000_0134	
62	0x0000_0138	
63	0x0000_013C	

(Note)

Each external interrupt has an associated priority-level register. Each of them is 3 bits wide, occupying the three MSBs of the Interrupt Priority Level Registers. Each Interrupt Priority Level Register occupies 1 byte (8 bits). NVIC registers in the Cortex-M3 processor can only be accessed using word-size transfers, so for each access, four Interrupt Priority Level Registers are accessed at the same time.

** __NVIC_PRIO_BITS = 3

CHAPTER 3. Boot Mode

3.1 Boot Mode Pins

AC33MX128 has boot mode option to program internal flash memory.
Boot mode can be entered by setting BOOT pin to 'L' at reset timing. (Normal state is 'H')
The boot mode supports UART boot and SPI boot.
UART boot uses UART0 port, and SPI boot uses SPI0.
The pins for boot mode are listed as following:

Table3.1. Boot mode pin list

Block	Pin Name	Dir	Description
SYSTEM	nRESET/PC10	I	Reset Input signal
	BOOT/PC11	I	'0' to enter Boot mode
UART0	RXD0/PC14	I	UART Boot Receive Data
	TXD0/PC15	O	UART Boot Transmit Data
SPI0	SS0/PA12	I	SPI Boot Slave Select
	SCK0/PA13	I	SPI Boot Clock Input
	MOSI0/PA14	I	SPI Boot Data Input
	MISO0/PA15	O	SPI Boot Data Output

3.2 Boot Mode Connections

User can design target board using any of boot mode ports – UART or SPI.
Followings are sample connection diagrams of boot mode.

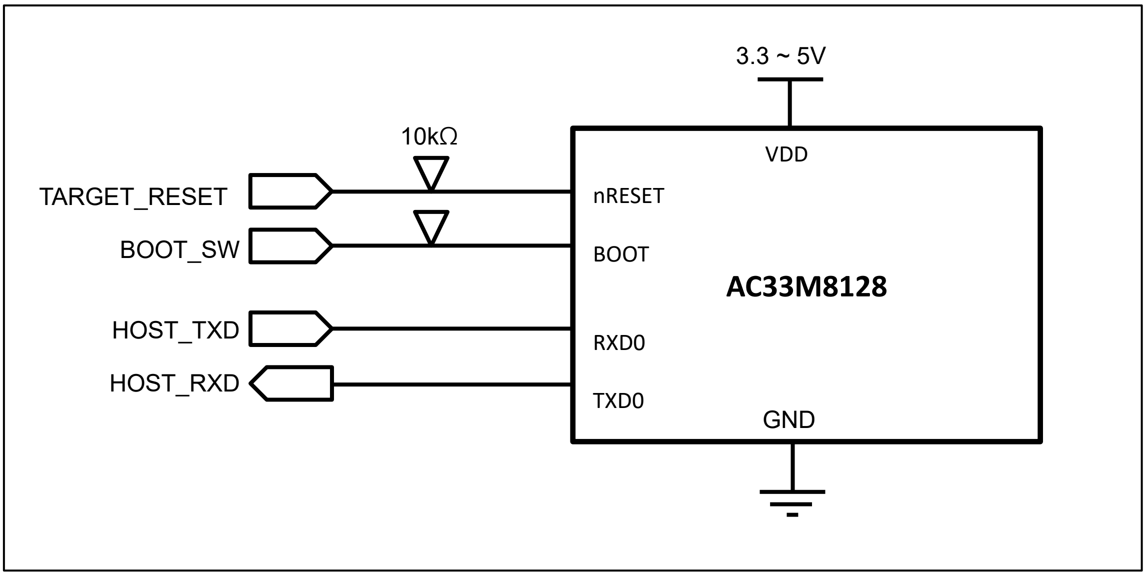


Figure3.1. Connection diagram of UART Boot

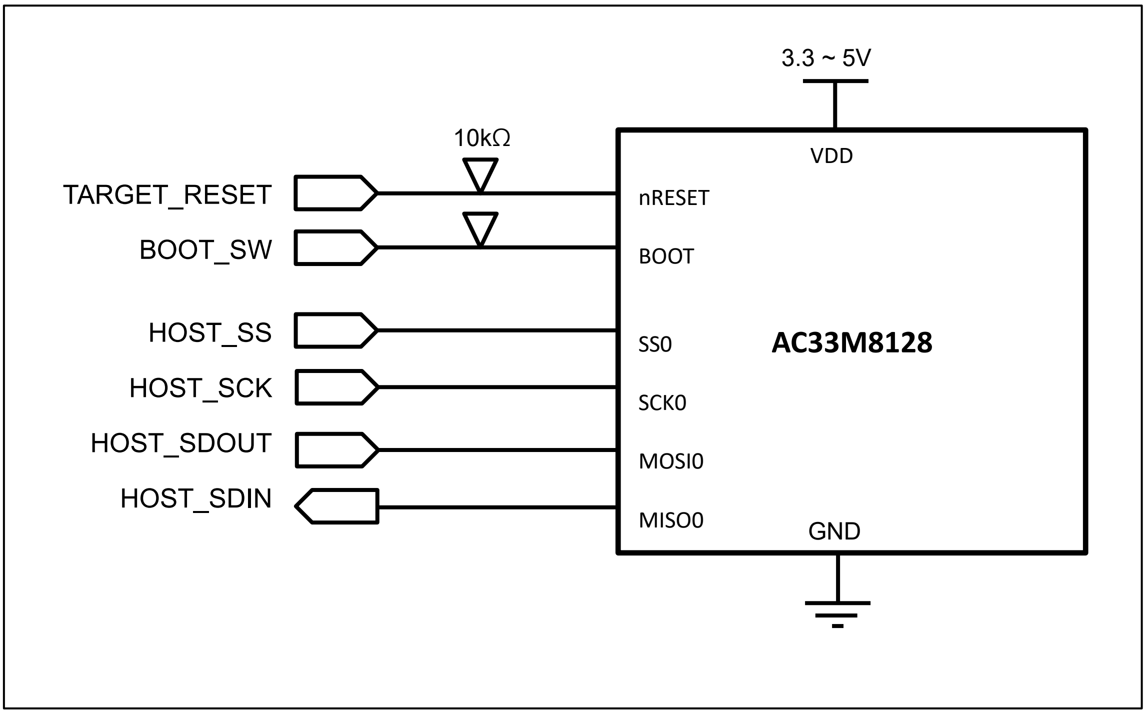


Figure3.2. Connection diagram of SPI Boot

SECTION 2.PERIPHERALS

CHAPTER 1. SYSTEM CONTROL UNIT (SCU)

1.1 OVERVIEW

The AC33MX128 has built-in intelligent power control block which manages system analog blocks and operating modes Internal reset and clock signals are controlled by SCU block to maintain optimize system performance and power dissipation.

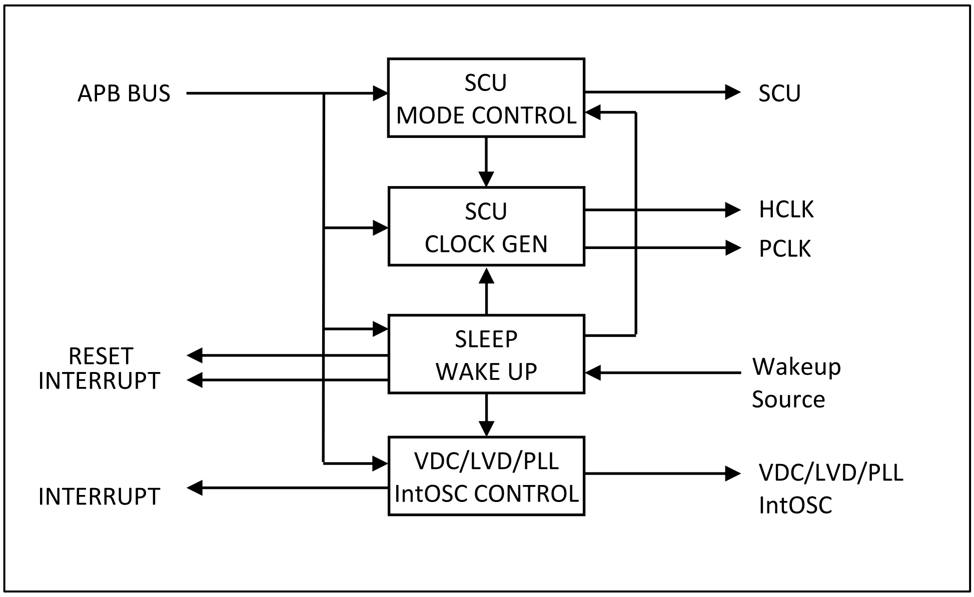


Figure1.1. SCU Block Diagram

1.2 CLOCK SYSTEM

AC33MX128 has two main operating clocks. One is HCLK which supplies the clock to CPU and AHB bus system. The other one is PCLK which supplies the clock to Peripheral systems.

User can control the clock system variation by software. Figure 1.2 shows the clock system of the chip. And Table 1.1 shows clock source descriptions.

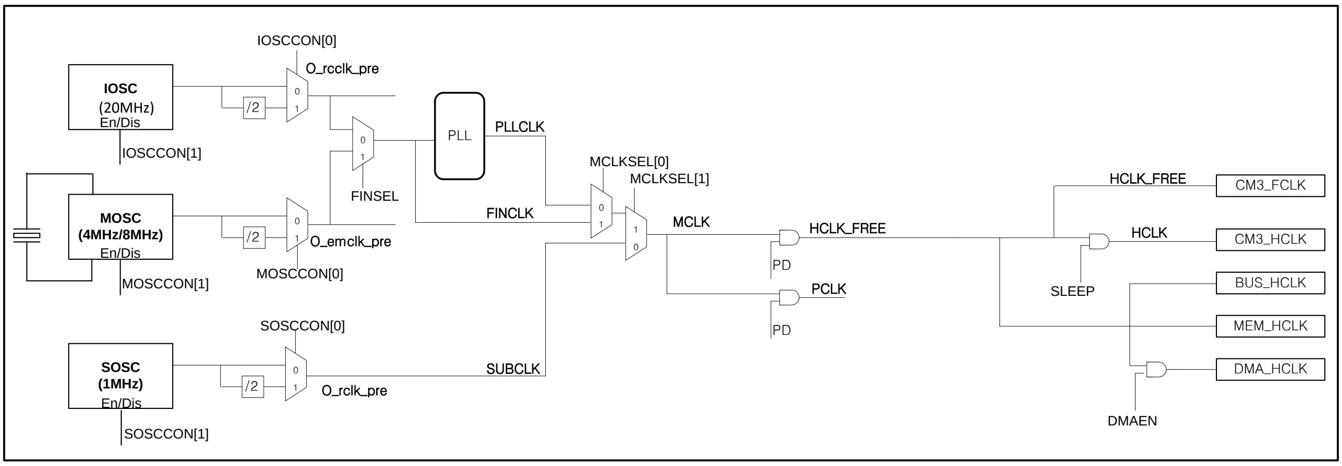


Figure 1.2. System clock configuration

All the mux to switch clock source have a glitch-free circuit in each. So clock can be switched without glitch risks.

Table1.1. Clock sources

Clock name	Frequency	Description
IOSC20	20MHz	Internal OSC
MainOSC	X-TAL(4MHz~8MHz)	External Crystal IOSC
PLL Clock	8MHz ~ 72MHz	On Chip PLL
ROSC	1MHz	Internal RING OSC

The PLL can synthesize PLLCLK clock up to 72MHz with FIN reference clock. It also has internal pre-divider and post-divider.

1.2.1 HCLK clock domain

HCLK clock feeds the clock to the CPU and AHB bus. Cortex-M3 CPU requires 2 clocks related with HCLK clock. FCLK and HCLK. FCLK is free running clock and it is always running except power down mode. HCLK can be stopped in the idle mode.

1.2.2 Miscellaneous clock domain for Cortex-M3

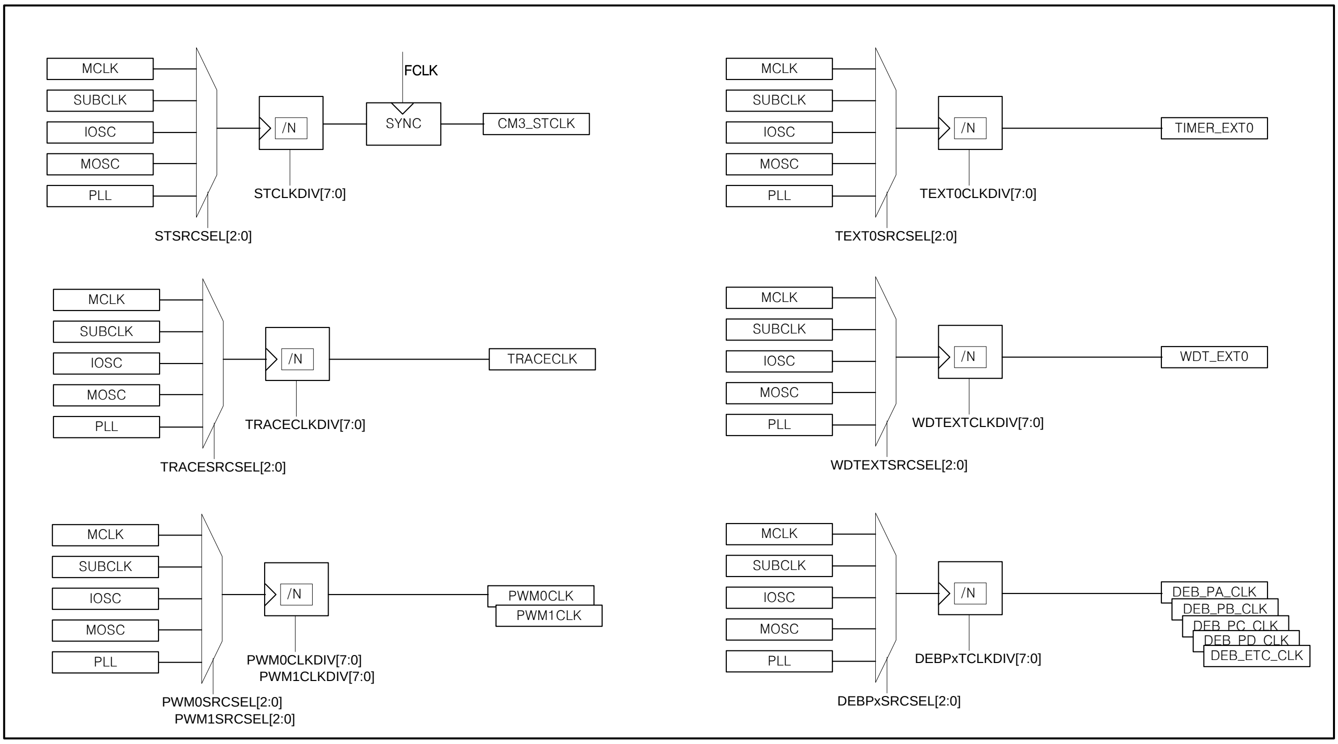


Figure 1.3. Miscellaneous clock configuration

1.2.3 PCLK clock domain

PCLK is master clock of all the peripherals. It can be stopped in powerdown mode. Each peripheral clocks generated by PCER register set.

1.2.4 Clock configuration procedure

After power up, the defulat system clock is feed by RINGOSC (1MHz) clock. RINGOSC is default enabled at power up sequence. The other clock sources will be enabled by user controls with the RINGOSC system clock.

MOSC clock can be enabled by CSCR register. Before enable MOSC block, the pin mux configuration should be set for XIN, XOUT function. PC12 and PC13 pins are shared with MOSC's XIN and XOUT function - PCCMR and PCCCR registers should be configured properly. After enabling the MOSC block, you must wait for more than 1msec time to ensure stable operation of crystal oscillation.

PLL clock can be enabled by PLLCON register. After enabling the PLL block, you must wait for pll lock flag. PLL output clock is stable, you can select MCLK for your system requirement. Before changing the system clock, flash access wait should be set to the maximum value. After the system clock is changed, you will need to set flash access wait that you want if necessary.

You can find an example flow chart to configure the system clock in Figure 1.4

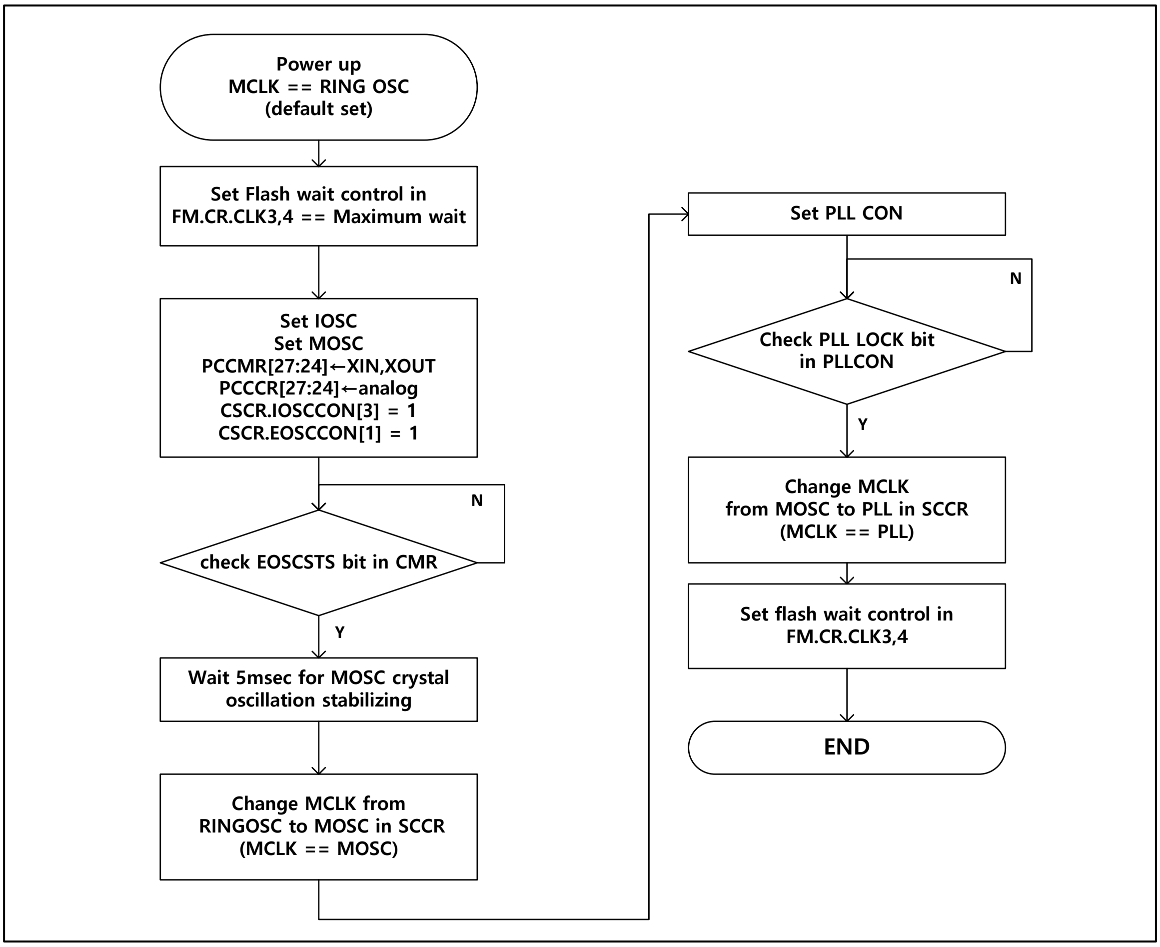


Figure 1.4. Clock configuration procedure

When you speed up the system clock until max operating frequency, you should check flash wait control configuration. CLK3 and CLK4 bit field in FMCR register can control the wat time. Flash read access time is one of limitation factor for the performance. The wait control recommendation is provided in Table 1.2.

Table 1.2 Flash wait control recommendation

FMCR	FLASH Access Wait	Available Max System clock frequency
CLK3	3 clock wait	~48MHz
CLK4	4 clock wait	~72MHz

1.3 RESET

AC33MX128 has two system reset. One is the cold reset by POR which is effective during power up or down sequence. The other reset is the warm reset which is generated by several reset sources. The reset event make the chip to turn initial state.

The cold reset has only one reset source which is POR.

The warm reset has several reset sources as below

- nRESET pin
- WDT reset
- LVD reset
- MCLK Fail reset
- MOSC Fail reset
- S/W reset
- CPU request reset

1.3.1 The Cold Reset

The cold reset is important feature of the chip when power is up. This characteristic will globaly affect the system boot. Internal VDC is enabled when VDD power is turn on. Internal VDD level slope will follow by External VDD power slope. Internal PoR trigger level is 1.4V of internal VDC voltage out level. At this time, boot operation is started. The ringosc clock is enabled and counts 4msec time for internal VDC level stabilizing. In this time, external VDD voltage level should be over than initial LVD level (2.3V). After 4msec counting , the CPU reset is released and start the operation.

The figure 1.5 shows power up sequence and internal reset waveform.

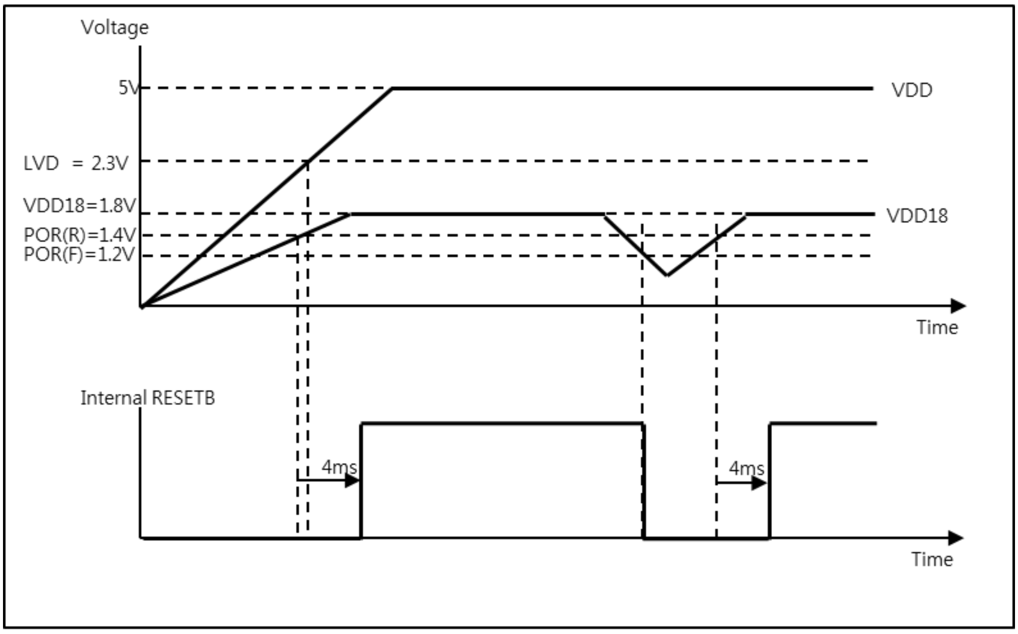


Figure 1.5. Power-up POR sequence

RSSR register shows the POR reset status. The last reset is come from POR, RSSR.PORST is set to “1”. After power up, this bit is always “1”. If abonormal internal voltage drop is occurred during normal operation, the system will be reset and this bit also set to “1”.

When the cold reset applied, all the chip returns to initial state.

1.3.2 The Warm Reset

The warm reset event has several reset sources and some parts of chip returns to itinial state when warm reset codition is occurred.

The wram reset source is controlled by RSER register and the status is appeared in RSSR register. The reset for each peripheral blocks is controlled by PRER register. The reset can be masked independently.

The CM3_SYSRESETn signal resets the processor excluding debug logics in the processor.

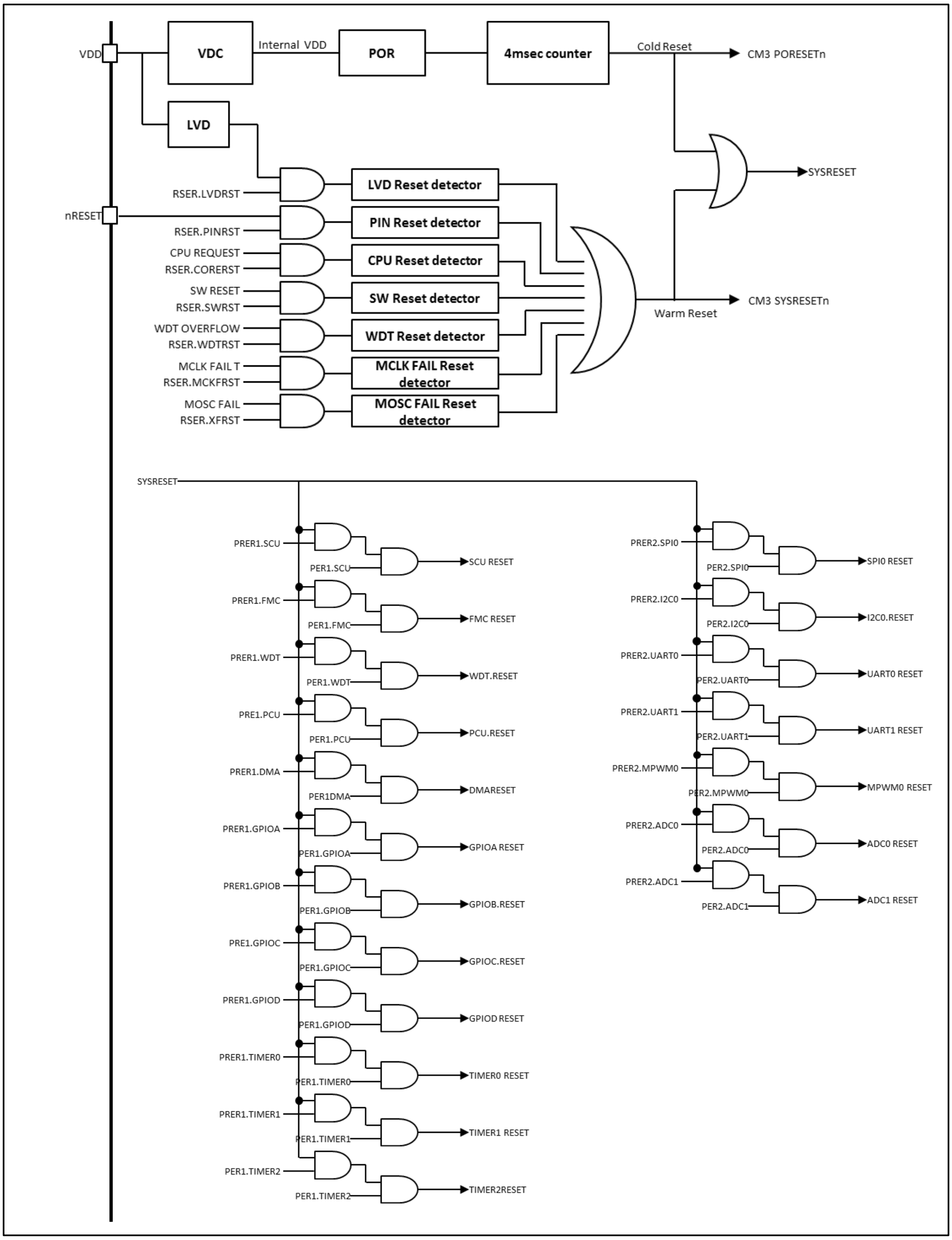


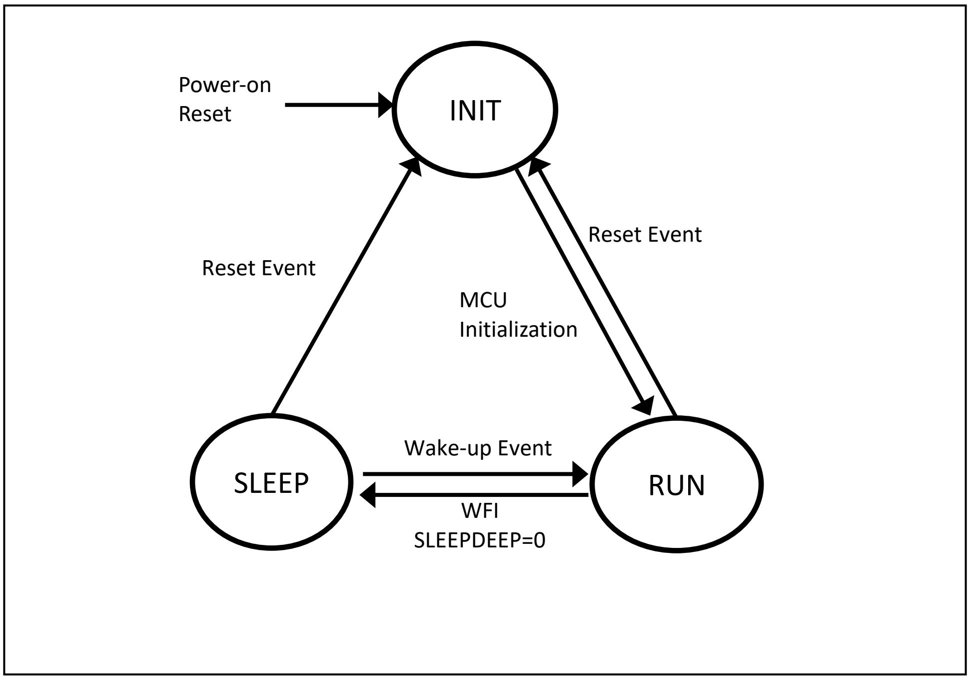
Figure 1.6. Reset configuration

1.4 OPERATION MODE

The INIT mode is initial state of the chip when reset is asserted. The RUN mode is max performance of the CPU with high-speed clock system. And the SLEEP mode can be used as the low power consumption mode. The low power consumption is achieved by halting processor core and unused peripherals.

Figure 1.5 shows the operation mode transition diagram.

Figure1.7. Operating Mode



1.4.1 RUN Mode

This mode is to operate the CPU core and the peripheral hardware by using the high-speed clock. After reset followed by INIT state, it is entered into RUN mode.

1.4.2 SLEEP Mode

Only the CPU is stopped in this mode. Each peripheral function can be enabled by the function enable and clock enable bit in the PER and PCER register.

1.5 PIN DESCRIPTION

Table1.2. SCU and PLL pins

PIN NAME	TYPE	DESCRIPTION
nRESET	I	External Reset Input
XIN/XOUT	OSC	External Crystal Oscillator
STBYO	O	Stand-by Output Signal
CLKO	O	Clock Output Monitoring Signal

1.6 REGISTERS

The base Address of SCU is 0x4000_0000 and register map is described in Table.1.4

Table1.3. Base address of SCU

NAME	BASE ADDRESS
SCU	0x4000_0000

Table1.4. SCU Register Map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
CIDR	0x0000	R	CHIP ID Register	AC33_8128
SMR	0x0004	RW	System Mode Register	0000_0000
SRCR	0x0008	RW	System Reset Control Register	0000_0000
WUER	0x0010	RW	Wake up source enable register	0000_0000
WUSR	0x0014	RW	Wake up source status register	0000_0000
RSER	0x0018	RW	Reset source enable register	0000_0049
RSSR	0x001C	RW	Reset source status register	0000_0080*
PRER1	0x0020	RW	Peripheral reset enable register 1	03FF_1F1F*
PRER2	0x0024	RW	Peripheral reset enable register 2	00F3_0F33*
PER1	0x0028	RW	Peripheral enable register 1	0000_000F*
PER2	0x002C	RW	Peripheral enable register 2	0000_0101*
PCER1	0x0030	RW	Peripheral clock enable register 1	0000_000F*
PCER2	0x0034	RW	Peripheral clock enable register 2	0000_0101*
CSCR	0x0040	RW	Clock Source Control register	0000_0020
SCCR	0x0044	RW	System Clock Control register	0000_0000
CMR	0x0048	RW	Clock Monitoring register	0000_0003
NMIR	0x004C	RW	NMI control register	0000_0000
COR	0x0050	RW	Clock Output Control register	0000_000F
TRIMENT	0x005C	RW	Trim Area Access Enable	0000_0000
PLLCON	0x0060	RW	PLL Control register	0000_1000
VDCCON	0x0064	RW	VDC Control register	0000_000F
LVDCON	0x0068	RW	LVD Control register	0000_0001
IOSCTRIM	0x006C	RW	Internal RC OSC Control register	0000_0000
OPA0TRIM	0x0070	RW	OPAM 0 trim register	0000_0000
OPA1TRIM	0x0074	RW	OPAM 1 trim register	0000_0000
OPA2TRIM	0x0078	RW	OPAM 2 trim register	0000_0000
OPA3TRIM	0x007C	RW	OPAM 3 trim register	0000_0000
EOSCR	0x0080	RW	External Oscillator control register	0000_0000
EMODR	0x0084	RW	External mode pin read register	0000_000X
MCCR1	0x0090	RW	Misc Clock Control register 1	0404_0001
MCCR2	0x0094	RW	Misc Clock Control register 2	0000_0000
MCCR3	0x0098	RW	Misc Clock Control register 3	0000_0001
MCCR4	0x009C	RW	Misc Clock Control register 4	0000_0000

MCCR5	0x00A0	RW	Misc Clock Control register 5	0000_0000
MCCR6	0x00A4	RW	Misc Clock Control register 6	0000_0001

1.6.1 CIDR Chip ID Register

CHIP ID Register shows chip identification information.
This register is 32-bit read-only register.

CIDR=0x4000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHIPID																															
0xAC33_8128																															
RO																															

31 0	CHIP ID	Device ID 0xAC33_8128

1.6.2 SMR System Mode Register

Current operating mode is shown in this SCU mode register. The previous operating mode will be saved in this register after reset event

System Mode Register is 16-bit register.

SMR=0x4000_0004

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										PREVMODE					
0	0	0	0	0	0	0	0	0	0	00		0	0	0	0
								R							

5 4	PREVMODE	Previous operating mode before current reset event.	
		00	Previous operating mode was RUN mode
		01	Previous operating mode was SLEEP mode
		10	Previous operating mode was PowerDown mode
		11	Previous operating mode was INIT mode

1.6.3 SRCR System Reset Control Register

System reset control register is 8-bit register.

SRCR=0x4000_0008

7	6	5	4	3	2	1	0
							SWRST
0	0	0	0	0	0	0	0
							W

1	SWRST	Internal soft reset activation bit	
		0	Normal operation
		1	Internal soft reset is applied and auto cleared

1.6.4 WUER Wakeup Source Enable Register

Enable wakeup source when the chip is in the PowerDown mode. Wakeup sources which will be used the source of chip wakeup should be enabled in each bit field. If the source will be used the wakeup source, write '1' into its enable bit. If the source will not be used the wakeup source, write 0 into its enable bit.

This register is 16-bit register.

WUER=0x4000_0010

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				GPIODWUE	GPIOCWUE	GPIOBWUE	GPIOAWUE							WDTWUE	LVDWUE
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
				RW	RW	RW	RW							RW	RW

12	GPIOEWUE	Enable wakeup source of GPIOE port pin change event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation
11	GPIODWUE	Enable wakeup source of GPIOD port pin change event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation
10	GPIOCWUE	Enable wakeup source of GPIOC port pin change event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation
9	GPIOBWUE	Enable wakeup source of GPIOB port pin change event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation
8	GPIOAWUE	Enable wakeup source of GPIOA port pin change event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation
1	WDTWUE	Enable wakeup source of watchdog timer event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation
0	LVDWUE	Enable wakeup source of LVD event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation

1.6.5 WUSR Wakeup Source Status Register

When the system is waked up by any wakeup source, the wakeup source is identified by reading this register. When the bit is set 1, the related wakeup source issues the wakeup to the SCU. The bit will be cleared when the event is cleared by the software.

WUSR=0x4000_0014

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				GPIODWU	GPIOCWU	GPIOBWU	GPIOAWU							WDTWU	LVDWU
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
				R	R	R	R							R	R

11	GPIODWU	Status of wakeup source of GPIOD port pin change event	
		0	No wakeup event
		1	Wakeup event was generated
10	GPIOCWU	Status of wakeup source of GPIOC port pin change event	
		0	No wakeup event
		1	Wakeup event was generated
9	GPIOBWU	Status of wakeup source of GPIOB port pin change event	
		0	No wakeup event
		1	Wakeup event was generated
8	GPIOAWU	Status of wakeup source of GPIOA port pin change event	
		0	No wakeup event
		1	Wakeup event was generated
1	WDTWU	Status of wakeup source of watchdog timer event	
		0	No wakeup event
		1	Wakeup event was generated
0	LVDWU	Status of wakeup source of LVD event	
		0	No wakeup event
		1	Wakeup event was generated

1.6.6 RSER Reset Source Enable Register

The reset source which will generate the reset event, can be selected by RSER register. When writing 1 in the bit field of each reset source, the reset source event will be transferred to reset generator. When writing 0 in the bit field of each reset source, the reset source event will be masked and not generate the reset event.

RSER=0x4000_0018

7	6	5	4	3	2	1	0
	PINRST	CPURST	SWRST	WDTRST	MCKFRST	XFRST	LVDRST
0	1	0	0	1	0	0	1
	RW	RW	RW	RW	RW	RW	RW

6	PINRST	External pin reset enable bit	
		0	Reset from this event is masked
		1	Reset from this event is enabled
5	CPURST	CPU request reset enable bit	
		0	Reset from this event is masked
		1	Reset from this event is enabled
4	SWRST	Software reset enable bit	
		0	Reset from this event is masked
		1	Reset from this event is enabled
3	WDTRST	Watchdog Timer reset enable bit	
		0	Reset from this event is masked
		1	Reset from this event is enabled
2	MCKFRST	MCLK Clock fail reset enable bit	
		0	Reset from this event is masked
		1	Reset from this event is enabled
1	XFRST	External OSC Clock fail reset enable bit	
		0	Reset from this event is masked
		1	Reset from this event is enabled
0	LVDRST	LVD reset enable bit	
		0	Reset from this event is masked
		1	Reset from this event is enabled

1.6.7 RSSR Reset Source Status Register

The RSSR shows the reset source information when reset event is occurred. “1” shows reset event was exist and “0” shows reset event is not exist for corresponding reset source.

When reset source is founded, write “1” into the corresponding bit will clear the reset status.

This register is 8-bit register

RSSR=0x4000_001C

7	6	5	4	3	2	1	0
PORST	PINRST	CPURST	SWRST	WDTRST	MCKFRST	XFRST	LVDRST
1	0	0	0	0	0	0	0
RC1	RC1	RC1	RC1	RC1	RC1	RC1	RC1

Bit	Name	Value	Description
7	PORST		Power on reset status bit
		0	Read : Reset from this event was not exist Write : no effect
		1	Read :Reset from this event was occurred Write : Clear the status
6	PINRST		External pin reset status bit
		0	Read : Reset from this event was not exist Write : no effect
		1	Read :Reset from this event was occurred Write : Clear the status
5	CPURST		CPU request reset status bit
		0	Read : Reset from this event was not exist Write : no effect
		1	Read :Reset from this event was occurred Write : Clear the status
4	SWRST		Software reset status bit
		0	Read : Reset from this event was not exist Write : no effect
		1	Read :Reset from this event was occurred Write : Clear the status
3	WDTRST		Watchdog Timer reset status bit
		0	Read : Reset from this event was not exist Write : no effect
		1	Read :Reset from this event was occurred Write : Clear the status
2	MCLKFRST		MCLK Fail reset status bit
		0	Read : Reset from this event was not exist Write : no effect
		1	Read :Reset from this event was occurred Write : Clear the status
1	XFRST		Clock fail reset status bit
		0	Read : Reset from this event was not exist Write : no effect
		1	Read :Reset from this event was occurred Write : Clear the status
0	LVDRST		LVD reset status bit
		0	Read : Reset from this event was not exist Write : no effect
		1	Read :Reset from this event was occurred Write : Clear the status

1.6.8 PRER1 Peripheral Reset Enable Register 1

The reset of each peripheral by event reset, can be masked by user setting. PRER1/2 register will control the enable of the event reset. If the corresponding bit is '1', the peripheral corresponded with this bit, accepts the reset event. Otherwise, the peripheral is protected from reset event and maintain current operation.

PRER1=0x4000_0020

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						TIMER9	TIMER8					TIMER3	TIMER2	TIMER1	TIMER0					GPIOD	GPIOC	GPIOB	GPIOA				DMA	PCU	WDT	FMC	SCU
0	0	0	0	0	0	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	1
						RW	RW					RW	RW	RW	RW					RW	RW	RW	RW				RW	RW	RW	RW	RW

25	TIMER9	TIMER9 reset mask
24	TIMER8	TIMER8 reset mask
19	TIMER3	TIMER3 reset mask
18	TIMER2	TIMER2 reset mask
17	TIMER1	TIMER1 reset mask
16	TIMER0	TIMER0 reset mask
11	GPIOD	GPIOD reset mask
10	GPIOC	GPIOC reset mask
9	GPIOB	GPIOB reset mask
8	GPIOA	GPIOA reset mask
4	DMA	DMA reset mask
3	PCU	Port Control Unit reset mask
2	WDT	Watchdog Timer reset mask
1	FMC	Flash memory controller reset mask
0	SCU	System Control Unit reset mask

1.6.9 PRER2 Peripheral Reset Enable Register 2

Peripheral Reset Enable Register 2 is 32-bit register.

PRER2=0x4000_0024

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								AFE	ADC2	ADC1	ADC0			MPWM1	MWPM0					UART3	UART2	UART1	UART0			I2C1	I2C0			SPI1	SPI0
0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	1	0	0	0	0	1	1	1	1	0	0	1	1	0	0	1	1
								RW	RW	RW	RW			RW	RW					RW	RW	RW	RW			RW	RW			RW	RW

23	AFE	AFE reset enable
22	ADC2	ADC2 reset enable
21	ADC1	ADC1 reset enable
20	ADC0	ADC0 reset enable
17	MPWM1	MPWM1 reset enable
16	MPWM0	MPWM0 reset enable
11	UART3	UART3 reset enable
10	UART2	UART2 reset enable
9	UART1	UART1 reset enable
8	UART0	UART0 reset enable
5	I2C1	I^2C1 reset enable
4	I2C0	I^2C0 reset enable
1	SPI1	SPI1 reset enable
0	SPI0	SPI0 reset enable

1.6.10 PER1 Peripheral Enable Register 1

To use peripheral unit, it should be activated by writing "1"to the correspond bit in the PER1/2 register. Before the activation, the peripheral will stay in reset state.

All the peripherals enabled by default. To disable the peripheral unit, write "0" to the correspond bit in the PER0/1 register, and then the peripheral enter the reset state.

PER1=0x4000_0028

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
						TIMER9	TIMER8					TIMER3	TIMER2	TIMER1	TIMER0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
						RW	RW					RW	RW	RW	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				GPIOD	GPIOC	GPIOB	GPIOA				DMA				
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
				RW	RW	RW	RW				RW	R	R	R	R

25	TIMER9	TIMER9 function enable
24	TIMER8	TIMER8 function enable
19	TIMER3	TIMER3 function enable
18	TIMER2	TIMER2 function enable
17	TIMER1	TIMER1 function enable
16	TIMER0	TIMER0 function enable
11	GPIOD	GPIOD function enable
10	GPIOC	GPIOC function enable
9	GPIOB	GPIOB function enable
8	GPIOA	GPIOA function enable
4	DMA	DMA function enable
3		Reserved
2		
1		
0		

1.6.11 PER2 Peripheral Enable Register 2

Peripheral Enable Register 2 is 32-bit register.

PER2=0x4000_002C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								AFE	ADC2	ADC1	ADC0			MPWM1	MWPM0					UART3	UART2	UART1	UART0			I2C1	I2C0			SPI1	SPI0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
								RW	RW	RW	RW			RW	RW					RW	RW	RW	RW			RW	RW			RW	RW

23	AFE	AFE function enable
22	ADC2	ADC2 function enable
21	ADC1	ADC1 function enable
20	ADC0	ADC0 function enable
17	MPWM1	MPWM1 function enable
16	MPWM0	MPWM0 function enable
11	UART3	UART3 function enable
10	UART2	UART2 function enable
9	UART1	UART1 function enable
8	UART0	UART0 function enable
5	I2C1	I^2C1 function enable
4	I2C0	I^2C0 function enable
1	SPI1	SPI1 function enable
0	SPI0	SPI0 function enable

1.6.12 PCER1 Peripheral Clock Enable Register 1

To use peripheral unit, its clock should be activated by writing ‘1’to the correspond bit in the PCER1/2 register. Before enabling its clock, the peripheral won’t operate properly.

To stop the clock of the peripheral unit, write ‘0’to the correspond bit in the PCER1/2 register, and then the clock of the peripheral is stopped.

PCER1=0x4000_0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						TIMER9	TIMER8					TIMER3	TIMER2	TIMER1	TIMER0					GPIOD	GPIOC	GPIOB	GPIOA				DMA				
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
						RW	RW					RW	RW	RW	RW					RW	RW	RW	RW				RW	R	R	R	R

25	TIMER9	TIMER9 clock enable
24	TIMER8	TIMER8 clock enable
19	TIMER3	TIMER3 clock enable
18	TIMER2	TIMER2 clock enable
17	TIMER1	TIMER1 clock enable
16	TIMER0	TIMER0 clock enable
11	GPIOD	GPIOD clock enable
10	GPIOC	GPIOC clock enable
9	GPIOB	GPIOB clock enable
8	GPIOA	GPIOA clock enable
4	DMA	DMA clock enable
3		Reserved
2		
1		
0		

1.6.13 PCER2 Peripheral Clock Enable Register 2

To use peripheral unit, its clock should be activated by writing '1' to the correspond

PCER2=0x4000_0034

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								AFE	ADC2	ADC1	ADC0			MPWM1	MWPM0					UART3	UART2	UART1	UART0			I2C1	I2C0			SPI1	SPI0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
								RW	RW	RW	RW			RW	RW					RW	RW	RW	RW			RW	RW			RW	RW

23	AFE	AFE clock enable
22	ADC2	ADC2 clock enable
21	ADC1	ADC1 clock enable
20	ADC0	ADC0 clock enable
17	MPWM1	MPWM1 clock enable
16	MPWM0	MPWM0 clock enable
11	UART3	UART3 clock enable
10	UART2	UART2 clock enable
9	UART1	UART1 clock enable
8	UART0	UART0 clock enable
5	I2C1	I^2C1 clock enable
4	I2C0	I^2C0 clock enable
1	SPI1	SPI1 clock enable
0	SPI0	SPI0 clock enable

1.6.14 CSCR Clock Source Control Register

The AC33MX128 has multiple clock sources to generate internal operating clocks. Each clock sources can be controlled by CSCR register.

This register is 8-bit register.

CSCR=0x4000_0040

7	6	5	4	3	2	1	0
-		RINGOSCCON		IOSCCON		EOSCCON	
00		10		00		00	
R		RW		RW		RW	

5 4	RINGOSCCON	Internal ring oscillator control	
		0X	Stop internal sub oscillator
		10	Enable internal sub oscillator
		11	Enable internal sub oscillator divide by 2
3 2	IOSCCON	Internal oscillator control	
		0X	Stop internal oscillator
		10	Enable internal oscillator
		11	Enable internal oscillator divide by 2
1 0	EOSCCON	External crystal oscillator control	
		0X	Stop External Ctystal oscillator
		10	Enable External Ctystal oscillator
		11	Enable External Ctystal divide by 2

1.6.15 SCCR System Clock Control Register

The AC33MX128 has multiple clock sources to generate internal operating clocks. Each clock sources can be controlled by SCCR register.

SCCR=0x4000_0044

7	6	5	4	3	2	1	0
-					FINSEL	MCLKSEL	
0000					0	00	
R					RW	RW	

2	FINSEL	PLL input source FIN select register	
		0	IOSC clock is used as FIN clock
		1	MOSC clock is used as FIN clock
1 0	MCLKSEL	System clock select register	
		0X	Internal sub oscillator
		10	PLL bypassed clock
		11	PLL output clock

When change FINSEL, both of internal OSC and external OSC should be alive, otherwise the chip will do mal function.

1.6.16 CMR Clock Monitoring Register

Internal clock can be monitored by internal sub oscillator for security purpose.
Clock Monitoring Register is 16-bit register.

CMR=0x4000_0048

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MCLKREC								MCLKMNT	MCLKIE	MCLKFAIL	MCLKSTS	EOSCMNT	EOSCIE	EOSCFAIL	EOSCSTS
0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0
RW								RW	RW	RC1	RC1	RW	RW	RC1	RC1

15	MCLKREC	MCLK fail auto recovery	
		0	MCLK is changed to RINGOSC by default when MCLKFAIL issued
		1	MCLK auto recovery is disabled
7	MCLKMNT	MCLK monitoring enable	
		0	MCLK monitoring disabled
		1	MCLK monitoring enabled
6	MCLKIE	MCLK fail interrupt enable	
		0	MCLK fail interrupt disabled
		1	MCLK fail interrupt enabled
5	MCLKFAIL	MCLK fail interrupt	
		0	MCLK fail interrupt not occurred
		1	Read : MCLK fail interrupt is pending Write : Clear pending interrupt
4	MCLKSTS	MCLK clock status	
		0	No clock is present on MCLK
		1	Clock is present on MCLK
3	EOSCMNT	External oscillator monitoring enable	
		0	External oscillator monitoring disabled
		1	External oscillator monitoring enabled
2	EOSCIE	External oscillator fail interrupt enable	
		0	External oscillator fail interrupt disabled
		1	External oscillator fail interrupt enabled
1	EOSCFAIL	External oscillator fail interrupt	
		0	External oscillator fail interrupt not occurred
		1	Read : External oscillator fail interrupt is pending Write : Clear pending interrupt
0	EOSCSTS	External oscillator status	
		0	Not oscillate
		1	External oscillator is working normally

Clock Monitoring function can not cover all mal function cases. It is just used for the reference. Fig1.8 shows the operational diagram for clock monitoring function.

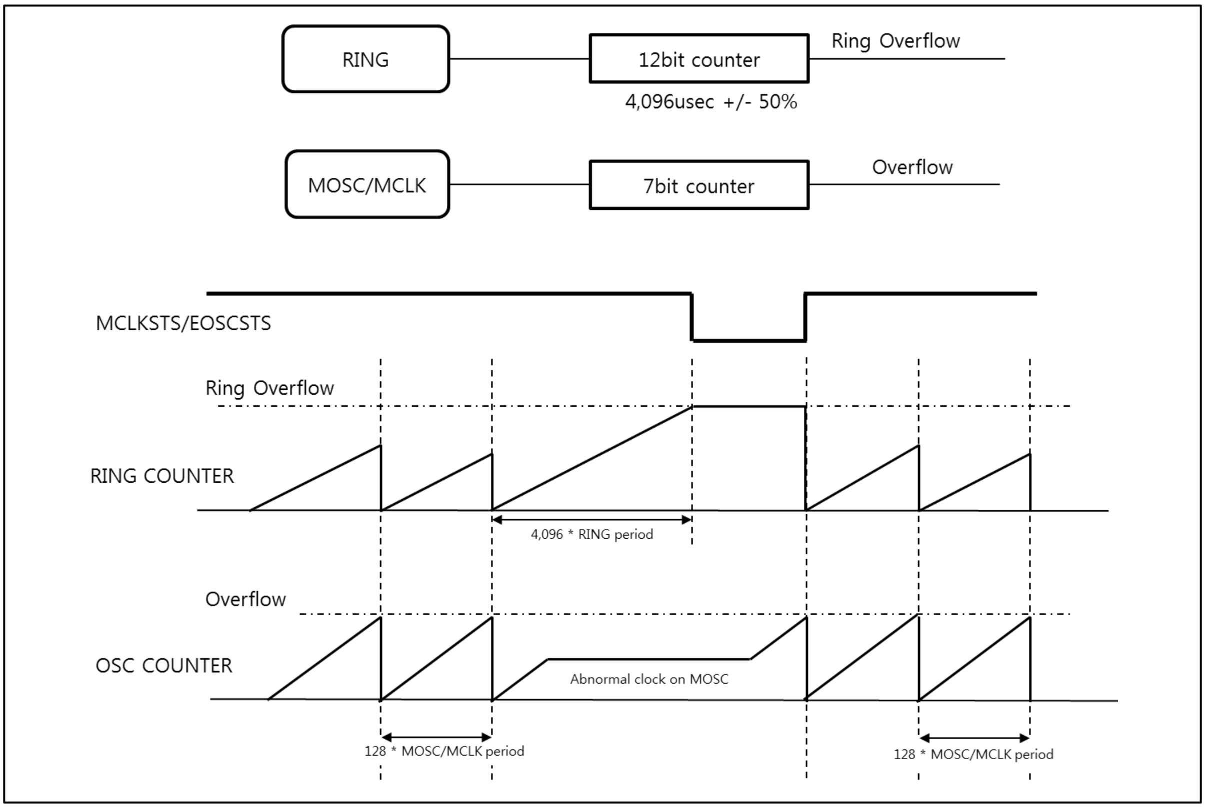


Figure1.8. Clock monitoring function diagram

1.6.17 NMIR NMI Control Register

NMI control register, enable and disable NMI, and the status of NMI PIN.

NMIR=0x4000_004C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												NMISTAT	NMIFLAG	NMIDBEN	NMIEN
00								0	0	0	0	0	0	0	0
												RW	RW	RW	RW

3	MMISTAT	NMI Pin status	
		0	NMI pin is low status
		1	NMI pin is high status
2	NMIFLAG	NMI interrupt flag	
		0	NMI interrupt is not pending
		1	NMI interrupt is pending
1	NMIDBENL	NMI pin debounce enable	
		0	NMI pin debounce disable
		1	NMI pin debounce enable
0	NMIEN	NMI Enable Write permission is required by PCU write enable sequence	
		0	NMI pin disable
		1	NMI pin enable

1.6.18 COR Clock Output Register

The AC33MX128 can drive the clock from internal MCLK clock with dedicated post divider. Clock Output Register is 8-bit.

COR=0x4000_0050

7	6	5	4	3	2	1	0
-			CLKOEN	CLKODIV			
000			0	1111			
R			RW	RW			

4	CLKOEN	Clock output enable	
		0	CLKO is disabled and stay "L" output
		1	CLKO Is enabled
3 0	CLKODIV	Clock output divider value CLKO = MCLK (CLKODIV = 0) $\text{CLKO} = \frac{MCLK}{2 * (\text{CLKODIV} + 1)} \quad (CLKODIV > 0)$	

1.6.19 PLLCON PLL Control Register

Integrated PLL will synthesize high speed clock for extremely high performance of the CPU. The PLL controlled by register setting.

PLL Control Register is 16-bit register.

PLLCON=0x4000_0060

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLLRSTB	PLLEN	BYPASS	LOCKSTS				PREDIV	FBCTRL				POSTDIV			
0	0	0	0	0	0	0	0	0000				0000			
RW	RW	RW	R				RW	RW				RW			

15	PLLRSTB	PLL reset			
		0	PLL reset is asserted		
		1	PLL reset is negated		
14	PLLEN	PLL enable			
		0	PLL is disabled		
		1	PLL is enabled		
13	BYPASS	FIN bypass			
		0	FOUT is bypassed as FIN		
		1	FOUT is PLL output		
12	LOCK	LOCK status			
		0	PLL is not locked		
		1	PLL is locked		
8	PREDIV	FIN predivider			
		0	FIN divided by 1		
		1	FIN divided by 2		
7 4	FBCTRL	Feedback control			
		0000	M = 6	1000	M = 32
		0001	M = 8	1001	M = 36
		0010	M = 10	1010	M = 40
		0011	M = 12	1011	M = 64
		0100	M = 16	1100	Not available
		0101	M = 18	1101	
		0110	M = 20	1110	
		0111	M = 26	1111	
3 0	POSTDIV	Post divider control			
		000	N = 1		
		001	N = 2		
		010	N = 3		
		011	N = 4		
		100	N = 6		
		101	N = 8		
		110	Not available		
		111	N =16		

(note)

M : Feed back control value,N: Post divider control value

You can change PLL clock with these are eqations.

$\mathrm{PLL(MHz)} = \mathrm{FINCLK(MHz)} \times \frac{1}{1} \times M \times \frac{1}{N}$, (PREDIV[8] = 0).

$\mathrm{PLL(MHz)} = \mathrm{FINCLK(MHz)} \times \frac{1}{2} \times M \times \frac{1}{N}$, (PREDIV[8] = 1).

If you want to make 72MHz PLL clock with 8MHz FINCLK, You can choose PREDIV[8] = 1, M = 18, N = 1.

$(72\mathrm{(MHz)} = 8\mathrm{(MHz)} \times \frac{1}{2} \times 18 \times \frac{1}{1})$

1.6.20 VDCCON VDC Control Register

On chip VDC control register. VDCTRIM is used for the trim value of VDC output. To modify VDCTRIM bit, VDCTE should be write “1”simultaneously. VDCWDLY value can be written with writing “1” to VDCDE bit simultaneously.

VDCCON=0x4000_0064

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVE						RESERVED							VDCTRIM										VDCDE				VDCWDLY				
0	0	0	0	0		100		0	0	0	0		0000			0	0	0	0	0	0	0	0				0x7F				
W						RW							RW										W				RW				

31	RESERVE	Reference reserved write enable.
		0 RESERVED field is not updated by writing
		1 RESERVED filed can be updated by writing
26 24	RESERVED	Reserved data for the future
23	VDCTE	VDCTRIM value write enable. Write only with VDCTRIM value.
		0 VDCTRIM field is not updated by writing
		1 VDCTRIM filed can be updated by writing
19 16	VDCTRIM	VDC output voltage trim value Not recommended strongly to write into this field
8	VDCDE	VDCWDLY value write enable. Write only with VDCWDLY value
		0 FOUT is PLL output
		1 FOUT is bypassed as FIN
7 0	VDCWDLY	VDC warm-up delay count value. When SCU is waked up from powerdown mode, the warm-up delay is inserted for VDC output being stabilized. The amount of delay can be defined with this register value 7F : 2msec

1.6.21 LVDCON LVD Control Register

On chip Brown-out detector control register.

This register is 32-bit register.

LVDCON=0x4000_0068

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								LVDTE						LVDTRIM		SELEN						LVDSEL								LVDLVL	LVDEN
0	0	0	0	0	0	0	0	0	0	0	0	0	0	00		0	0	0	0	0	0	00		0	0	0	0	0	0	0	1
								W						RW		W						RW								R	RW

23	LVDTE	LVDTRIM value write enable. Write only with LVDTRIM value.	
		0	LVDTRIM field is not updated by writing
		1	LVDTRIM filed can be updated by writing
17 16	LVDTRIM	LVD voltage level trim value Not recommended strongly to write into this field	
15	SELEN	LVDSEL value write enable. Write only with LVDSEL value.	
		0	LVDSEL field is not updated by writing
		1	LVDSEL filed can be updated by writing
9 8	LVDSEL	LVD detect level select	
		00	LVD detect level is 1.8V
		01	LVD detect level is 2.2V
		10	LVD detect level is 2.7V
		11	LVD detect level is 4.3V
1	LVDLVL	LVD Level	
		0	LVD level is not detected
		1	LVD level is detected
0	LVDEN	LVD Function enable	
		0	LVD is not enabled
		1	LVD is enabled

1.6.22 IOSCTRIM Internal OSC Trim Register

Internal oscillator frequency trim register

This register is 32-bit register.

IOSCTRIM=0x4000_006C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								TSLEN					TSL			LTEN		LT				LTM		UDCEN			UDCH		UDCL		
0	0	0	0	0	0	0	0	0	0	0	0	0	000			0	0	0000				00		0	0	0	00		000		
								W					RW			W		RW				RW		W			RW		RW		

23	TSLEN	TSL trim value write enable. Write only with TSL trim value.	
		0	TSL field is not updated by writing
		1	TSL filed can be updated by writing
18 16	TSL[2:0]	TSL trim value	
15	LTEN	LTM/LT value write enable. Write only with LTM/LT value	
		0	LT field is not updated by writing
		1	LT filed can be updated by writing
13 8	LTM/LT	Internal oscillator LT trim value Not recommended strongly to write into this field	
7	UDCEN	UDCH/UDCL value write enable. Write only with UDC value	
		0	UDC field is not updated by writing
		1	UDC filed can be updated by writing
4 0	UDCH/UDCL	Internal oscillator UDC trim value Not recommended strongly to write into this field	

All trim bit can be writable when trim mode is enabled

1.6.23 EOSCR External Oscillator Control Register

External main crystal oscillator has two characteristics. For the noise immunity, NMOS amp type is recommended and for the low power characteristic, INV amp type is recommended. This register is 16-bit register.

EOSCR=0x4000_0080

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISELEN						ISEL		AMPEN							AMPSEL
0	0	0	0	0	0	11		0	0	0	0	0	0	0	0
W						RW		W							RW

15	ISELEN	Write enable of bit field ISEL.	
		0	Write access of ISEL field is masked
		1	Write access of ISEL field is accepted
9 8	ISEL	Select current.	
		00	Minimum current driving option
		01	Low current driving option
		10	High current driving option
		11	Maximum current driving option
7	AMPEN	Write enable of bit field AMPSEL	
		0	Write access of AMPSEL field is masked
		1	Write access of AMPSEL field is accepted
0	AMPSEL	Select amplifier type	
		0	NMOS type
		1	Inverter type

1.6.24 OPAnTRIM Internal OPAMP n Trim Register

OPA0TRIM Internal OPAMP 0 Trim Register
OPA1TRIM Internal OPAMP 1 Trim Register
OPA2TRIM Internal OPAMP 2 Trim Register
OPA3TRIM Internal OPAMP 3 Trim Register

Internal OPAMP trim register.

OPATRIM0=0x4000_0070, OPATRIM1=0x4000_0074
OPATRIM2=0x4000_0078 , OPATRIM3=0x4000_007C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								ABMEN						ABM		GTRIMEN				GTRIMH		GTRIML		ATRIMEN				ATRIM			
0	0	0	0	0	0	0	0	0	0	0	0	0	0	00		0	0	0	0	00		10		0	0	0	0	0000			
								W						RW		W				RW		RW		W				RW			

23	ABMEN	ABM trim value write enable. Write only with ABM trim value.	
		0	ABM field is not updated by writing
		1	ABM filed can be updated by writing
18 16	ABM[1:0]	OPAMP BIAS trim value	
15	GTRIMEN	LTM/LT value write enable. Write only with LTM/LT value	
		0	LT field is not updated by writing
		1	LT filed can be updated by writing
11 8	GTRIMHL[1:0]/GTRIML[1:0]	OPAMP Gain trim value GAINH[1:0],GAINL[1:0] Not recommended strongly to write into this field	
7	ATRIMEN	ATRIM value write enable. Write only with ATRIM value	
		0	ATRIM field is not updated by writing
		1	ATRIM filed can be updated by writing
3 0	ATRIM[3:0]	OPAMP VIO (Offset) Trimming value Not recommended strongly to write into this field	

1.6.25 EMODR External Mode Status Register

External Mode Status Register shows external mode pin status while booting.
This register is 8-bit register.

EMODR=0x4000_0084

7	6	5	4	3	2	1	0
					SCANMD	TEST	BOOT
		0x0			0	0	-
		R			R	R	R

Bit	Name	Description	
2	SCANMD	SCANMD pin level	
		0	SCANMD pin is low
		1	SCANMD pin is high
1	TEST	TEST pin level	
		0	TEST pin is low
		1	TEST pin is high
0	BOOT	BOOT pin level	
		0	BOOT pin is low
		1	BOOT pin is high

1.6.26 MCCR1 Miscellaneous Clock Control Register 1

The AC33MX128 can drive the clock from internal MCLK clock with dedicated post divider. This register is 32-bit register.

MCCR1=0x4000_0090

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRCPOL					TRCSEL			TRACEDIV													STCSEL			SYSTICKDIV							
0	0	0	0	0	100			0x04								0	0	0	0	0	000			0x01							
W					RW			RW													RW			RW							

26 24	TRCSEL	TRACE Clock source select bit	
		0xx	RING OSC 1Mhz
		100	MCLK (bus clock)
		101	INT OSC 20MHz
		110	External Main OSC
		111	PLL Clock
23 16	TRACEDIV	TRACE Clock N divider TRACE Clock = CLK_IN/DIV (If TRACEDIV is 0, input clock will be stopped)	
10 8	STCSEL	SYSTIC Clock source select bit	
		0xx	RING OSC 1Mhz
		100	MCLK (bus clock)
		101	INT OSC 20MHz
		110	External Main OSC
		111	PLL Clock
7 0	STDIV	SYSTIC Clock N divider Systick input clock = Clock source / STDIV (If STDIV is 0 or 1, input clock will be stopped)	

1.6.27 MCCR2 Miscellaneous Clock Control Register 2

The AC33MX128 can drive the clock from internal MCLK clock with dedicated post divider. This register is 32-bit register.

MCCR2=0x4000_0094

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					PWM1CSEL			PWM1DIV													PWM0CSEL			PWM0DIV							
0	0	0	0	0	000			0x00								0	0	0	0	0	000			0x00							
					RW			RW													RW			RW							

26 24	PWM1CSEL	PWM1 Clock source select bit	
		0xx	RING OSC 1Mhz
		100	MCLK (bus clock)
		101	INT OSC 20MHz
		110	External Main OSC
		111	PLL Clock
23 16	PWM1DIV	PWM1 Clock N divider PWM1 input clock = Clock source / PWM1DIV (If PWM1DIV is 0, input clock will be stopped)	
10 8	PWM0CSEL	PWM0 Clock source select bit	
		0xx	RING OSC 1Mhz
		100	MCLK (bus clock)
		101	INT OSC 20MHz
		110	External Main OSC
		111	PLL Clock
7 0	PWM0DIV	PWM0 Clock N divider PWM0 input clock = Clock source / PWM0DIV (If PWM0DIV is 0, input clock will be stopped)	

1.6.28 MCCR3 Miscellaneous Clock Control Register 3

The AC33MX128 can drive the clock from internal MCLK clock with dedicated post divider. This register is 32-bit register.

MCCR3=0x4000_0098

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					TEXT0CSEL			TEXT0DIV													WDTCSEL			WDTDIV							
0	0	0	0	0	000			0x01								0	0	0	0	0	000			0x01							
					RW			RW													RW			RW							

26 24	TEXT0CSEL	TIMER EXT0 Clock source select bit	
		0xx	RING OSC 1Mhz
		100	MCLK (bus clock)
		101	INT OSC 20MHz
		110	External Main OSC
		111	PLL Clock
23 16	TEXT0DIV	TEXT0 Clock N divider TEXT0 input clock = Clock source / TEXT0DIV (If TEXT0DIV is 0, input clock will be stopped)	
10 8	WDTCSEL	WDT Clock source select bit	
		0xx	RING OSC 1Mhz
		100	MCLK (bus clock)
		101	INT OSC 20MHz
		110	External Main OSC
		111	PLL Clock
7 0	WDTDIV	WDT Clock N divider WDT input clock = Clock source / WDTDIV (If WDTDIV is 0, input clock will be stopped)	

1.6.29 MCCR4 Miscellaneous Clock Control Register 4

The AC33MX128 can drive the clock from internal MCLK clock with dedicated post divider. This register is 32-bit register.

MCCR4=0x4000_009C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					PBDCSEL			PBDDIV													PADCSEL			PADDIV							
0	0	0	0	0	000			0x01								0	0	0	0	0	000			0x01							
					RW			RW													RW			RW							

26 24	PBDCSEL	Debounce Clock for Port B source select bit	
		0xx	RING OSC 1Mhz
		100	MCLK (bus clock)
		101	INT OSC 20MHz
		110	External Main OSC
		111	PLL Clock
23 16	PBDDIV	PORT B Debounce Clock N divider PORT B Debounce clock = Clock source / PBDDIV (If PBDDIV is 0, input clock will be stopped)	
10 8	PADCSEL	Debounce Clock for Port A source select bit	
		0xx	RING OSC 1Mhz
		100	MCLK (bus clock)
		101	INT OSC 20MHz
		110	External Main OSC
		111	PLL Clock
7 0	PADDIV	PORT A Debounce Clock N divider PORT A Debounce clock = Clock source / PADDIV (If PADDIV is 0, input clock will be stopped)	

1.6.30 MCCR5 Miscellaneous Clock Control Register 5

The AC33MX128 can drive the clock from internal MCLK clock with dedicated post divider. This register is 32-bit register.

MCCR5=0x4000_00A0

31	30	29	28	27	26 25 24	23 22 21 20 19 18 17 16	15	14	13	12	11	10 9 8	7 6 5 4 3 2 1 0
					PDDCSEL	PDDDIV						PCDCSEL	PCDDIV
0	0	0	0	0	000	0x01	0	0	0	0	0	000	0x01
					RW	RW						RW	RW

26 24	PDDCSEL	Debounce Clock for PORT D source select bit	
		0xx	RING OSC 1Mhz
		100	MCLK (bus clock)
		101	INT OSC 20MHz
		110	External Main OSC
		111	PLL Clock
23 16	PDDDIV	PORT D Debounce Clock N divider PORT D Debounce clock = Clock source / PDDDIV (If PDDDIV is 0, input clock will be stopped)	
10 8	PCDCSEL	Debounce Clock for PORT C source select bit	
		0xx	RING OSC 1Mhz
		100	MCLK (bus clock)
		101	INT OSC 20MHz
		110	External Main OSC
		111	PLL Clock
7 0	PCDDIV	PORT C Debounce Clock N divider PORT C Debounce clock = Clock source / PCDDIV (If PCDDIV is 0, input clock will be stopped)	

1.6.31 MCCR6 Miscellaneous Clock Control Register 6

The AC33MX128 can drive the clock from internal MCLK clock with dedicated post divider. .

MCCR6=0x4000_00A4

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					ADCCSEL			ADCCDIV													ETCDSEL			ETCDDIV							
0	0	0	0	0	000			0x00								0	0	0	0	0	000			0x01							
					RW			RW													RW			RW							

26 24	ADCCSEL	ADC clock source select bit	
		0xx	RING OSC 1Mhz
		100	MCLK (bus clock)
		101	INT OSC 20MHz
		110	External Main OSC
		111	PLL Clock
23 16	ADCCDIV	ADC Clock N divider ADC clock = Clock source / ADCCDIV (If ADCCDIV is 0, input clock will be stopped)	
10 8	ETCDCSEL	Debounce Clock for ETC(NMI) source select bit	
		0xx	RING OSC 1Mhz
		100	MCLK (bus clock)
		101	INT OSC 20MHz
		110	External Main OSC
		111	PLL Clock
7 0	ETCDDIV	ETC Debounce Clock N divider ETC clock = Clock source / ETCDDIV (If ETCDDIV is 0, input clock will be stopped)	

CHAPTER 2. PORT CONTROL UNIT (PCU)

2.1 OVERVIEW

PCU(Port Control Unit) controls the external I/Os as below

- Set external signal directions of each pins
- Set interrupt trigger mode for each pins
- Set internal pull-up register control and open drain control

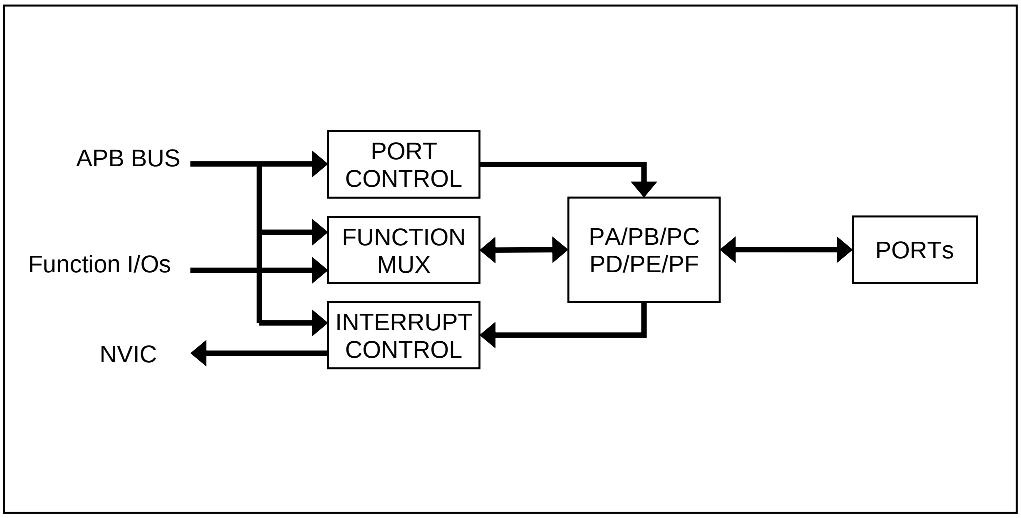


Figure2.1. Block Diagram

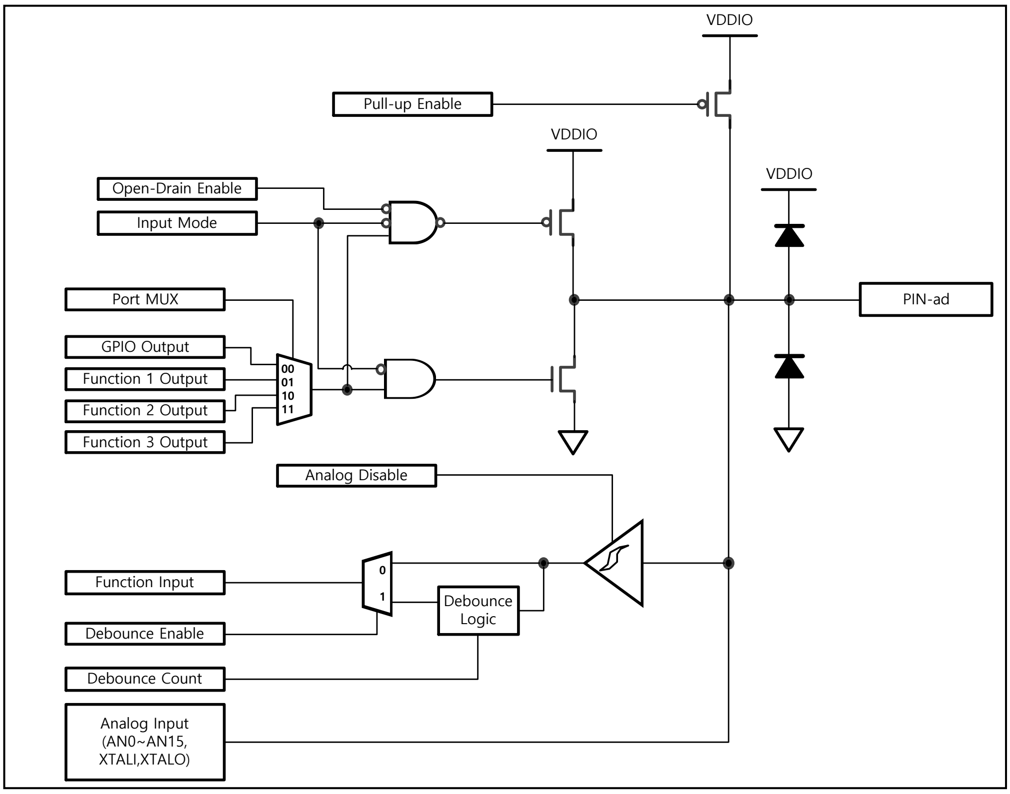


Figure2.2. I/O Port Block Diagram (ADC and External Oscillator pins)

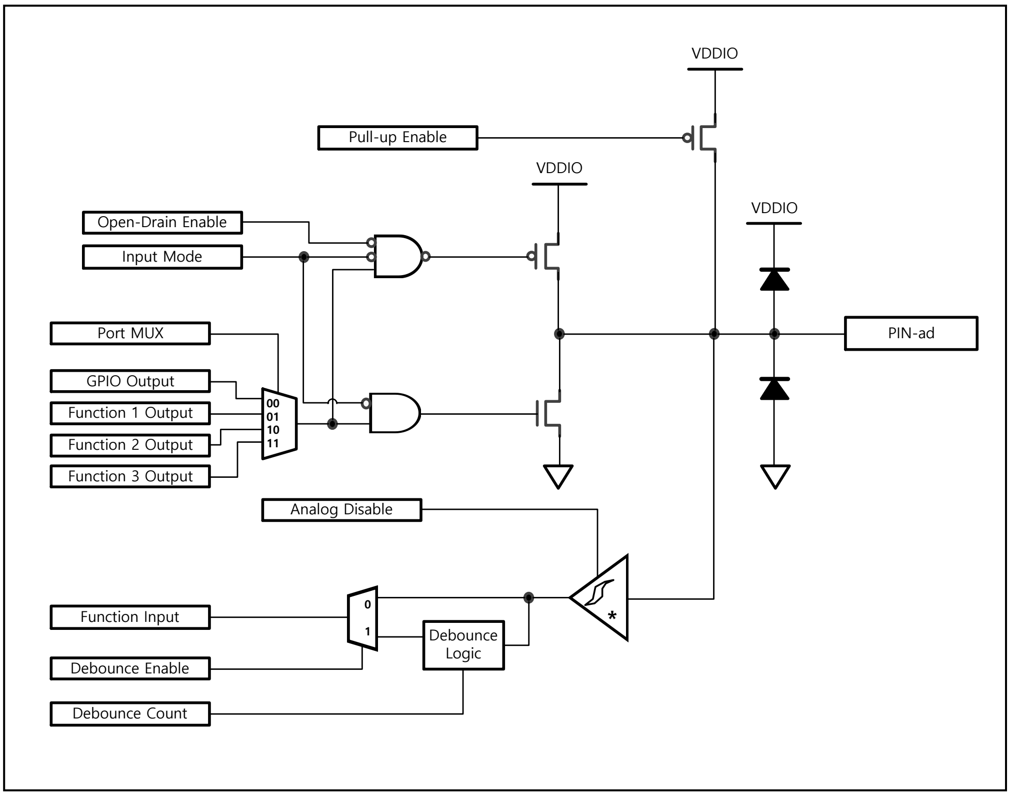


Figure2.3. I/O Port Block Diagram (General I/O pins)

2.2 Pin Multiplexing

GPIO pins have alternative function pins. Below table shows pin multiplexing information.

Table 2.1. GPIO Alternative function

PORT		FUNCTION			
		00	01	10	11
PA	0	**PA0***			AIN0/COMP0
	1	**PA1***			AIN1/COMP1
	2	**PA2***			AIN2/COMP2
	3	**PA3***			AIN3/COMP3
	4	**PA4***		T0O	AIN4
	5	**PA5***		T1O	AIN5
	6	**PA6***		T2O	AIN6/CREF0
	7	**PA7***	TRACED3	T3O	AIN7/CREF3
	8	**PA8***	TRACECLK	AD0O	AIN8
	9	**PA9***	TRACED0	AD1O	AIN9
	10	**PA10***	TRACED1	AD2O	AIN10
	11	**PA11***	TRACED2		AIN11
	12	**PA12***	SS0	AD2I	AIN12
	13	**PA13***	SCK0		AIN13
	14	**PA14***	MOSI0		AIN14
	15	**PA15***	MISO0		AIN15
PB	0	**PB0***	PWM0H0		
	1	**PB1***	PWM0L0		
	2	**PB2***	PWM0H1		
	3	**PB3***	PWM0L1		
	4	**PB4***	PWM0H2	T9C	
	5	**PB5***	PWM0L2	T9O	
	6	**PB6***	PRTIN0	WDTO(2)	
	7	**PB7***	OVIN0	STBYO(2)	
	8	**PB8***	PRTIN1	RXD3	
	9	**PB9***	OVIN1	TXD3	
	10	**PB10***	PWM1H0		
	11	**PB11***	PWM1L0		
	12	**PB12***	PWM1H1		
	13	**PB13***	PWM1L1		
	14	**PB14***	PWM1H2		
	15	**PB15***	PWM1L2		

(*) mark indicates default pin setting.
(2) mark indicates secondary port

Table2.2. GPIO Alternative function

PORT		FUNCTION			
		00	01	10	11
PC	0	PC0	**TCK/SWCLK***		
	1	PC1	**TMS/SWDIO***		
	2	PC2	**TDO/SWO***		
	3	PC3	**TDI***		
	4	PC4	**nTRST***	T0C/PHA(2)	
	5	**PC5***	RXD1	T1C/PHB(2)	
	6	**PC6***	TXD1	T2C/PHZ(2)	
	7	**PC7***	SCL0	T3C	
	8	**PC8***	SDA0		
	9	**PC9***	CLKO	T8O	
	10	PC10	**nRESET***		
	11	**PC11/BOOT***		T8C	
	12	**PC12***	XIN		
	13	**PC13***	XOUT		
	14	**PC14***	RXD0	MISO0(2)	
	15	**PC15***	TXD0	MOSI0(2)	
PD	0	**PD0***	SS1		
	1	**PD1***	SCK1		
	2	**PD2***	MOSI1		
	3	**PD3***	MISO1		
	4	**PD4***	SCL1		
	5	**PD5***	SDA1		
	6	**PD6***	TXD2	AD0I	
	7	**PD7***	RXD2	AD1I	
	8	**PD8***		WDTO	
	9	**PD9***		STBO	
	10	**PD10***	AD0SOC	T0C/PHA	
	11	**PD11***	AD0EOC	T1C/PHB	
	12	**PD12***	AD1SOC	T2C/PHZ	
	13	**PD13***	AD1EOC	T3C	
	14	**PD14***	AD2SOC		
	15	**PD15***	AD2EOC		

(*) mark indicates default pin setting.
(2) mark indicates secondary port

2.3 REGISTERS

Base address of PCU block is 0x4000_1000.

All the register access is globaly masked by PORTEN register. In other to change register value exept PORTEN register, the port access should be enabled in advance.

Table2.3. Base address of port

NAME	BASE ADDRESS
PCA	0x4000_1000
PCB	0x4000_1100
PCC	0x4000_1200
PCD	0x4000_1300

Table2.4. PCU Register map

NAME	OFFSET	TYPE	DESCRIPTION
PC*n*.MR	0x--00	RW	Port *n* pin mux select register
PC*n*.CR	0x--04	RW	Port *n* pin control register
PC*n*.PCR	0x--08	RW	Port *n* internal pull-up control register
PC*n*.DER	0x--0C	RW	Port *n* debounce control register
PC*n*.IER	0x--10	RW	Port *n* interrupt enable register
PC*n*.ISR	0x--14	RW	Port *n* interrupt status register
PC*n*.ICR	0x--18	RW	Port *n* interrupt control register
PORTEN	0x1FF0	RW	Port Access enable

2.3.1 PCA.MR PORT A Pin MUX Register

PA port mode select register. This register must be set properly before use the port. Otherwise the port can't guarantee its functionality.

PCA.MR=0x4000_1000

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

PORT	SELECTION BIT			
	00	01	10	11
PA0	PA0			AN0_CP0
PA1	PA1			AN1_CP1
PA2	PA2			AN2_CP2
PA3	PA3			AN3_CP3
PA4	PA4		T0O	AN4
PA5	PA5		T1O	AN5
PA6	PA6		T2O	AN6_CREF0
PA7	PA7	TRACED3	T3O	AN7_CREF3
PA8	PA8	TRACECLK	AD0O	AN8
PA9	PA9	TRACED0	AD1O	AN9
PA10	PA10	TRACED1	AD2O	AN10
PA11	PA11	TRACED2		AN11
PA12	PA12	SS0	AD2I	AN12
PA13	PA13	SCK0		AN13
PA14	PA14	MOSI0		AN14
PA15	PA15	MISO0		AN15

2.3.2 PCB.MR PORT B Pin MUX Register

PB port mode select register. This register must be set properly before use the port. Otherwise the port can't guarantee its functionality.

PCB.MR=0x4000_1100

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

PORT	SELECTION BIT			
	00	01	10	11
PB0	PB0	MP0UH		
PB1	PB1	MP0UL		
PB2	PB2	MP0VH		
PB3	PB3	MP0VL		
PB4	PB4	MP0WH	T9C	
PB5	PB5	MP0WL	T9O	
PB6	PB6	PRTIN0	WDTO	
PB7	PB7	OVIN0	STBYO	
PB8	PB8	PRTIN1	RXD3	
PB9	PB9	OVIN1	TXD3	
PB10	PB10	MP1UH		
PB11	PB11	MP1UL		
PB12	PB12	MP1VH		
PB13	PB13	MP1VL		
PB14	PB14	MP1WH		
PB15	PB15	MP1WL		

2.3.3 PCC.MR PORT C Pin MUX Register

PC port mode select register. This register must be set properly before use the port. Otherwise the port can't guarantee its functionality.

PCC.MR=0x4000_1200

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
00	00	00	00	01	01	00	00	00	00	00	01	01	01	01	01
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

PORT	SELECTION BIT			
	00	01	10	11
PC0	PC0	TCK_SWCLK		
PC1	PC1	TMS_SWDIO		
PC2	PC2	TDO_SWO		
PC3	PC3	TDI		
PC4	PC4	nTRST	T0C_PHA	
PC5	PC5	RXD1	T1C_PHB	
PC6	PC6	TXD1	T2C_PHZ	
PC7	PC7	SCL0	T3C	
PC8	PC8	SDA0		
PC9	PC9	CLKO	T8O	
PC10	PC10	nRESET		
PC11	PC11	BOOT	T8C	
PC12	PC12	XIN		
PC13	PC13	XOUT		
PC14	PC14	RXD0	MISO0	
PC15	PC15	TXD0	MOSI0	

2.3.4 PCD.MR PORT D Pin MUX Register

PD port mode select register. This register must be set properly before use the port. Otherwise the port can't guarantee its functionality.

PCD.MR=0x4000_1300

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

PORT	SELECTION BIT			
	00	01	10	11
PD0	PD0	SS1		
PD1	PD1	SCK1		
PD2	PD2	MOSI1		
PD3	PD3	MISO1		
PD4	PD4	SCL1		
PD5	PD5	SDA1		
PD6	PD6	TXD2	AD0I	
PD7	PD7	RXD2	AD1I	
PD8	PD8		WDTO	
PD9	PD9		STBYO	
PD10	PD10	AD0SOC	T0C_PHA	
PD11	PD11	AD0EOC	T1C_PHB	
PD12	PD12	AD1SOC	T2C_PHZ	
PD13	PD13	AD1EOC	T3C	
PD14	PD14	AD2SOC		
PD15	PD15	AD2EOC		

2.3.5 PCn.CR PORT n Pin Control Register (Except for PCC.CR)

Input or output control of each port pin. Each pin can be configured as input pin, output pin or open-drain pin.

PCA.CR=0x4000_1004, PCB.CR=0x4000_1104, PCD.CR=0x4000_1304

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
11	11	11	11	11	11	11	11	11	11	11	11	11	11	11	11
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

n	Pn	Port control
		00 Push-pull output
		01 Open-drain output
		10 Input
		11 Analog

2.3.6 PCC.CR PORT C Pin Control Register

Input or output control of each port pin. Each pin can be configured as input pin, output pin or open-drain pin.

PCC.CR=0x4000_1204

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
11	11	11	11	10	10	11	11	11	11	11	10	10	00	10	10
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

n	Pn	Port control
		00 Push-pull output
		01 Open-drain output
		10 Input
		11 Analog

2.3.7 PCn.PCR PORT n Pull-up Resistor Control Register

Every pin in the port has on-chip pull-up resistors which can be configured by PCn.PCR registers.

PCA.PCR=0x4000_1008, PCB.PCR=0x4000_1108
PCC.PCR=0x4000_1208, PCD.PCR=0x4000_1308

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PUE15	PUE14	PUE13	PUE12	PUE11	PUE10	PUE9	PUE8	PUE7	PUE6	PUE5	PUE4	PUE3	PUE2	PUE1	PUE0
0000															
RW															

n	PUEn	Port pull-up control
		0 Disable pull-up resistor
		1 Enable pull-up resister

2.3.8 PCn.DER PORT n Debounce Enable Register

Every pin in the port has a digital debounce filter which can be configured by PCn.DER registers.

PCA.DER=0x4000_100C, PCB.DER=0x4000_110C
PCC.DER=0x4000_120C, PCD.DER=0x4000_130C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDE15	PDE14	PDE13	PDE12	PDE11	PDE10	PDE9	PDE8	PDE7	PDE6	PDE5	PDE4	PDE3	PDE2	PDE1	PDE0
0000															
RW															

n	PDEn	Pin debounce enable	
		0	Disable debounce filter
		1	Enable debounce filter

2.3.9 PCn.IER PORT n Interrupt Enable Register

The entire pin can be an external interrupt source. Both of edge trigger interrupt and level trigger interrupt are supported. The interrupt mode can be configured by setting PCn.IER registers

PCA.IER=0x4000_1010, PCB.IER=0x4000_1110
PCC.IER=0x4000_1210, PCD.IER=0x4000_1310

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
PIE15	PIE14	PIE13	PIE12	PIE11	PIE10	PIE9	PIE8	PIE7	PIE6	PIE5	PIE4	PIE3	PIE2	PIE1	PIE0
00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

n	PIEn	Pin interrupt enable	
		00	Interrupt disabled
		01	Enable interrupt as level trigger mode
		10	Reserved
		11	Enable interrupt as edge trigger mode

2.3.10 PCn.ISR PORT n Interrupt Status Register

When an interrupt is delivered to the CPU, the interrupt status can be detected by reading PnISR register. PCn.ISR register will report a source pin of interrupt and a type of interrupt.

PCA.ISR=0x4000_1014, PCB.ISR=0x4000_1114
PCC.ISR=0x4000_1214, PCD.ISR=0x4000_1314

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
PIS15	PIS14	PIS13	PIS12	PIS11	PIS10	PIS9	PIS8	PIS7	PIS6	PIS5	PIS4	PIS3	PIS2	PIS1	PIS0
00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

n	PISn	Pin interrupt status	
		00	No interrupt event
		01	Low level interrupt or Falling edge interrupt event is present
		10	High level interrupt or rising edge interrupt event is present
		11	Both of rising and falling edge interrupt event is present in edge trigger interrupt mode. Not available in level trigger interrupt mode

2.3.11 PCn.ICR PORT n Interrupt Control Register

Interrupt mode control register.

PCA.ICR=0x4000_1018, PCB.ICR=0x4000_1118
PCC.ICR=0x4000_1218, PCD.ICR=0x4000_1318

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
PIC15	PIC14	PIC13	PIC12	PIC11	PIC10	PIC9	PIC8	PIC7	PIC6	PIC5	PIC4	PIC3	PIC2	PIC1	PIC0
00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

n	PICn	Pin interrupt mode	
		00	Prohibit external interrupt
		01	Low level interrupt or Falling edge interrupt mode
		10	High level interrupt or rising edge interrupt mode
		11	Both of rising and falling edge interrupt mode. Not support for level trigger mode

2.3.12 PORTEN Port Access Eable

PORTEN enables register writing permition of all PCU registers.

PORTEN=0x4000_1FF0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								PORTEN							
0	0	0	0	0	0	0	0	--							
								RW							

7 0	PORTEN	Writing the sequence of 0x15 and 0x51 in this register enables writing to PCU registers, and writing other values protects all PCU registers from writing.

2.4 Functional Description

When the input functions of I/O port is used by Pin Control Register, the output function of I/O port is disabled.

The Port Function different according to the Pin Mux Register.

The Input Data Register capture the data present on the I/O pin or Debounced input data at every GPIO Clock cycle.

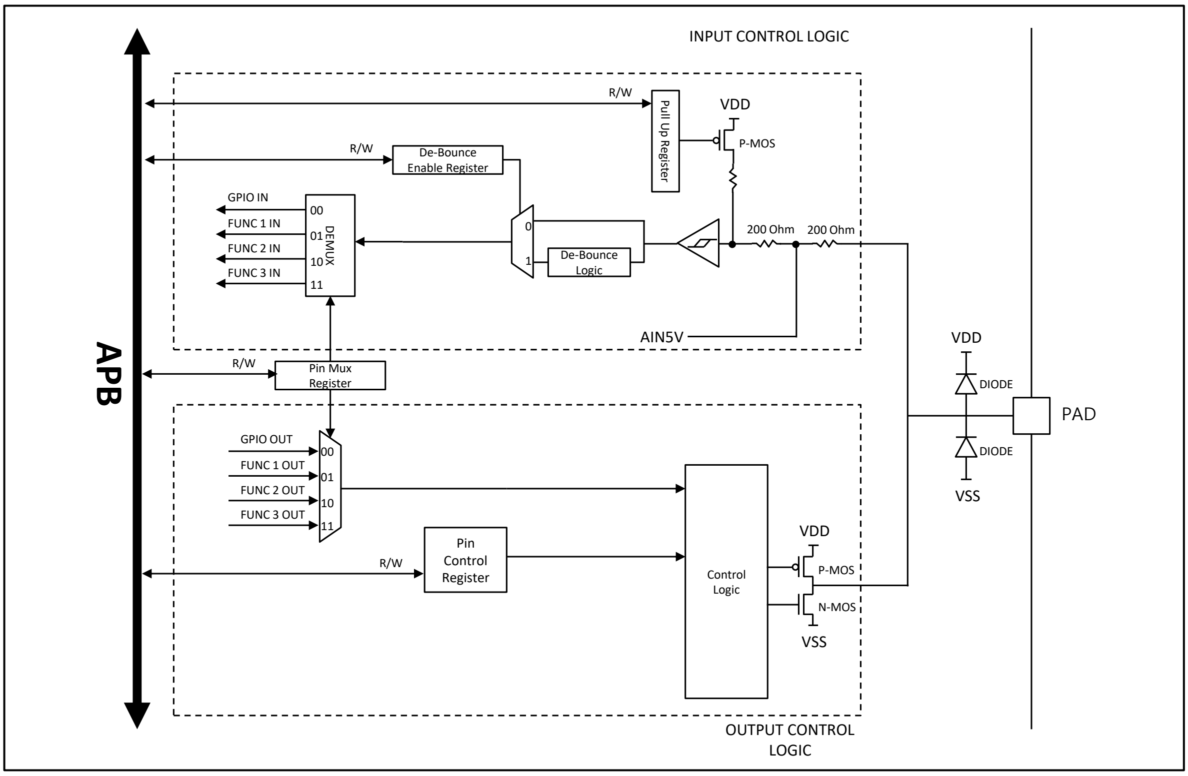


Figure2.4. Port Diagram

When the De-Bounce functions of Input Data is used by Debounce Enable Register. External input data captured by Debounce CLK.

- If CNT Value is “01”, Debounced Input Data is “1”.
- If CNT Value is “10”, Debounced Input Data is “0”

Can change the Debounce CLK of each port group used by MCCR4~5 Register.

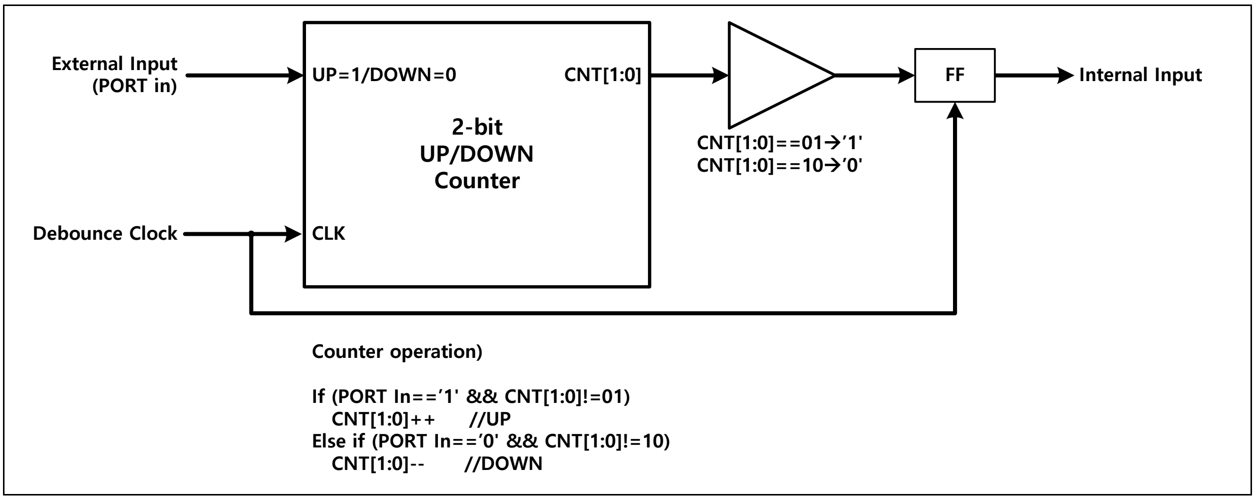


Figure2.5. Debounce Logic

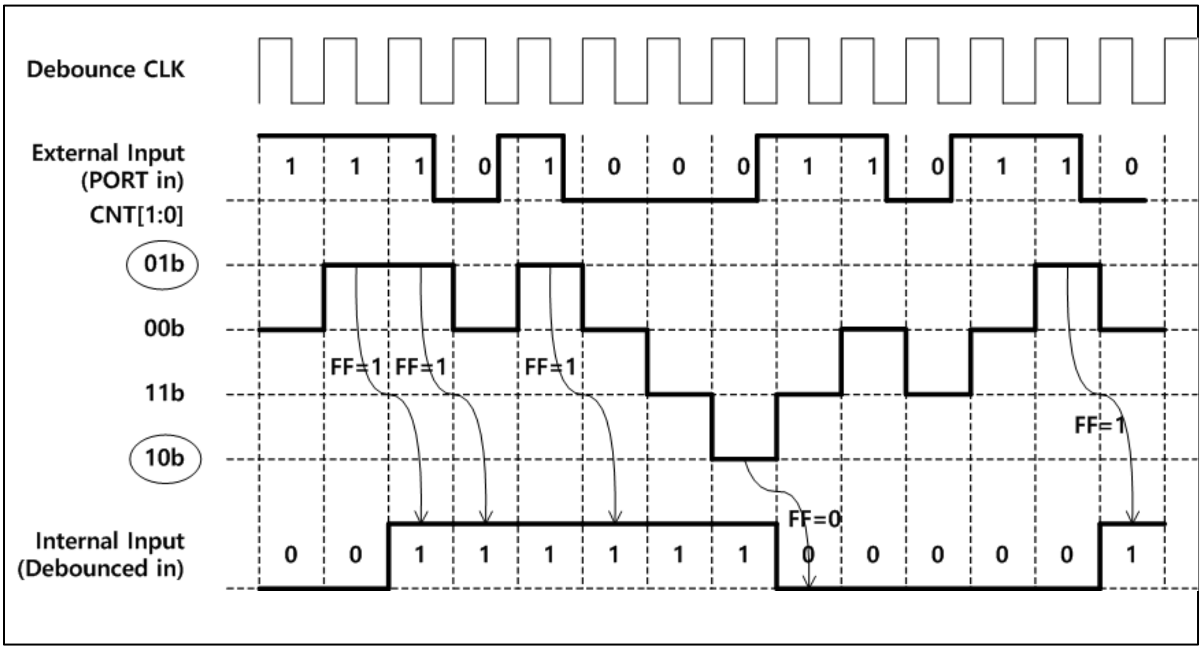


Figure2.6. Port Debounce Example

CHAPTER 3. GENERAL PURPOSE I/O (GPIO)

3.1 OVERVIEW

Most of pins except dedicated function pins can be used general I/O ports. General input/output ports are controlled by GPIO block.

- Output signal level (H/L) select
- Input signal level
- Output Set/Clear pin as writing '1'

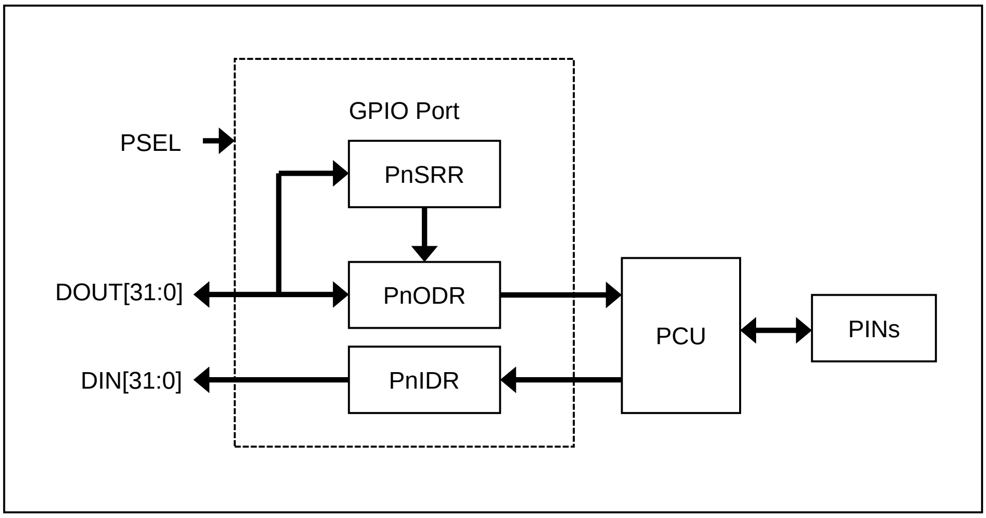


Figure3.1. Block diagram

3.2 Pin description

Table 3.1. External signal

PIN NAME	TYPE	DESCRIPTION
PA	IO	PA0 - PA15
PB	IO	PB0 - PB15
PC	IO	PC0 - PC15
PD	IO	PD0 - PD15

3.3 REGISTERS

The base Address of GPIO is 0x4000_2000 and register map is described in Table3.2 and 3.3.

Table 3.2. Base address of each port

NAME	BASE ADDRESS
PA PORT	0x4000_2000
PB PORT	0x4000_2100
PC PORT	0x4000_2200
PD PORT	0x4000_2300

Table3.3. GPIO Register map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
Pn.ODR	0x--00	RW	Port *n* Output data register	0x00000000
Pn.IDR	0x--04	RO	Port *n* Input data register	0x00000000
Pn.BSR	0x--08	WO	Port *n* Pin set register	0x00000000
Pn.BCR	0x—0C	WO	Port *n* Pin clear register	0x00000000

3.3.1 Pn.ODR PORT n Output Data Register

When the pin is set as output and GPIO mode, the pin output level is defined by Pn.ODR registers.

PA.ODR=0x4000_2000, PB.ODR=0x4000_2100
PC.ODR=0x4000_2200, PD.ODR=0x4000_2300

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ODR															
0000															
RW															

ODR	Pin output level	
	0	Output low level
	1	Output high level

3.3.2 Pn.IDR PORT n Input Data Register

Each pin level status can be read in the Pn.IDR register. Even if the pin is alternative mode except analog mode, the pin level can be detected in the Pn.IDR register.

PA.IDR=0x4000_2004, PB.IDR=0x4000_2104
PC.IDR=0x4000_2204, PD.IDR=0x4000_2304

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDR															
0000															
RO															

IDR	Pin current level	
	0	The pin is low level
	1	The pin is high level

3.3.3 Pn.BSR PORT n Bit Set Register

Pn.BSR is a register for control each bit of Pn.ODR register. When write "1" specific bit then the correspondent bit in the Pn.ODR register will be set.

PA.BSR=0x4000_2008, PB.BSR=0x4000_2108
PC.BSR=0x4000_2208, PD.BSR=0x4000_2308

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BSR															
0000															
WO															

BSR	Pin current level	
	0	Not effect
	1	Set correspondent bit in Pn.ODR register

3.3.4 Pn.BCR PORT n Bit Clear Register

Pn.BCR is a register for control each bit of Pn.ODR register. When write "1" specific bit then the correspondent bit in the Pn.ODR register will be clear.

PA.BCR=0x4000_200C, PB.BCR=0x4000_210C
PC.BCR=0x4000_220C, PD.BCR=0x4000_230C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCR															
0000															
WO															

BCR	Pin current level	
	0	Not effect
	1	Clear correspondent bit in Pn.ODR register

3.4 Functional Description

When configured as output, the value written to the GPIO Ouput Data Register is output on the I/O Pin.
When set the Bit Set Register, GPIO Output Data Register set the high.
When set the Bit Clr Register, GPIO Output Data Register set the Low.
The Input Data Register capture the data present on the I/O pin or Debounced input data at every GPIO Clock cycle.

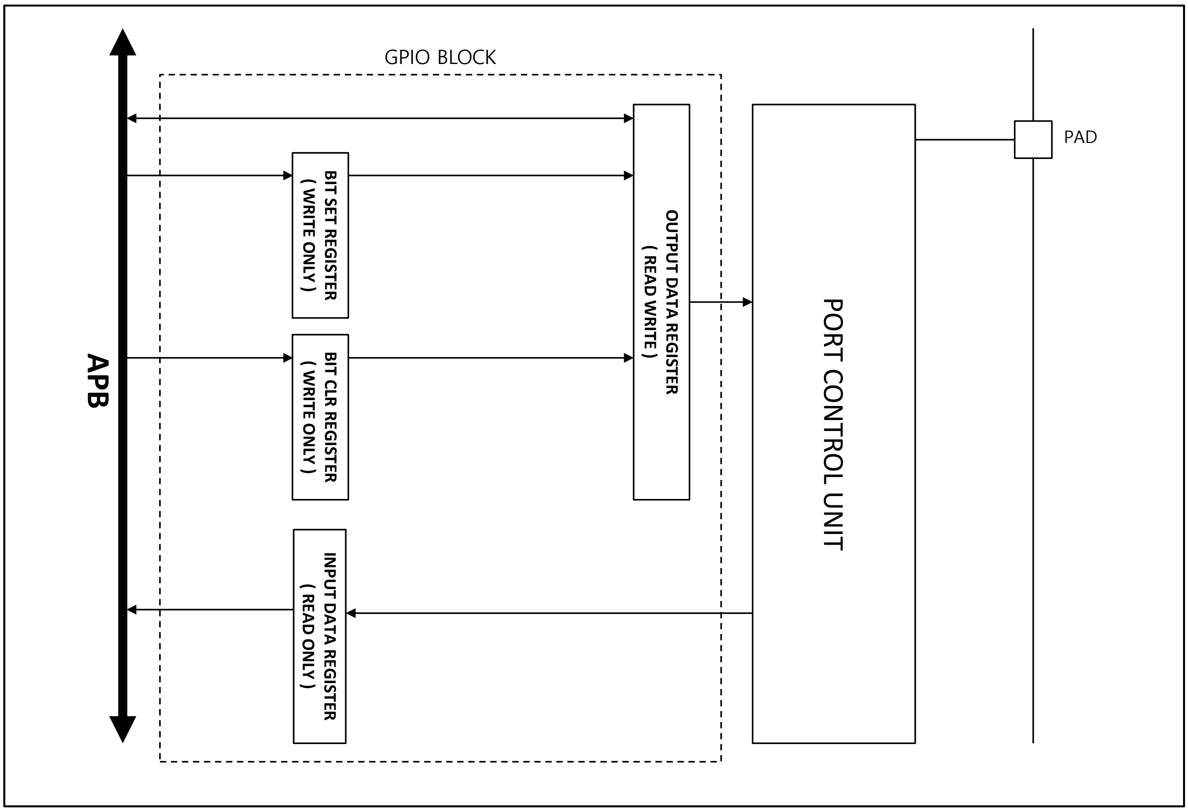


Figure3.2. GPIO Diagram

CHAPTER 4. FLASH MEMORY CONTROLLER

4.1 OVERVIEW

Flash Memory Controller is an internal flash memory interface controller.

- 128KB Flash code memory
- 32-bit read data bus width
- Code cache block for fast access mode
- 128-byte page size
- Support page erase and sector erase
- 128-byte unit program

Table4.1. Internal flash specification

Item	Decription
Size	128KB
Start Address	0x0000_0000
End Address	0x0001_FFFF
Page Size	128-byte
Total Page Count	1,024 pages
PGM Unit	128-byte
Erase Unit	128-byte

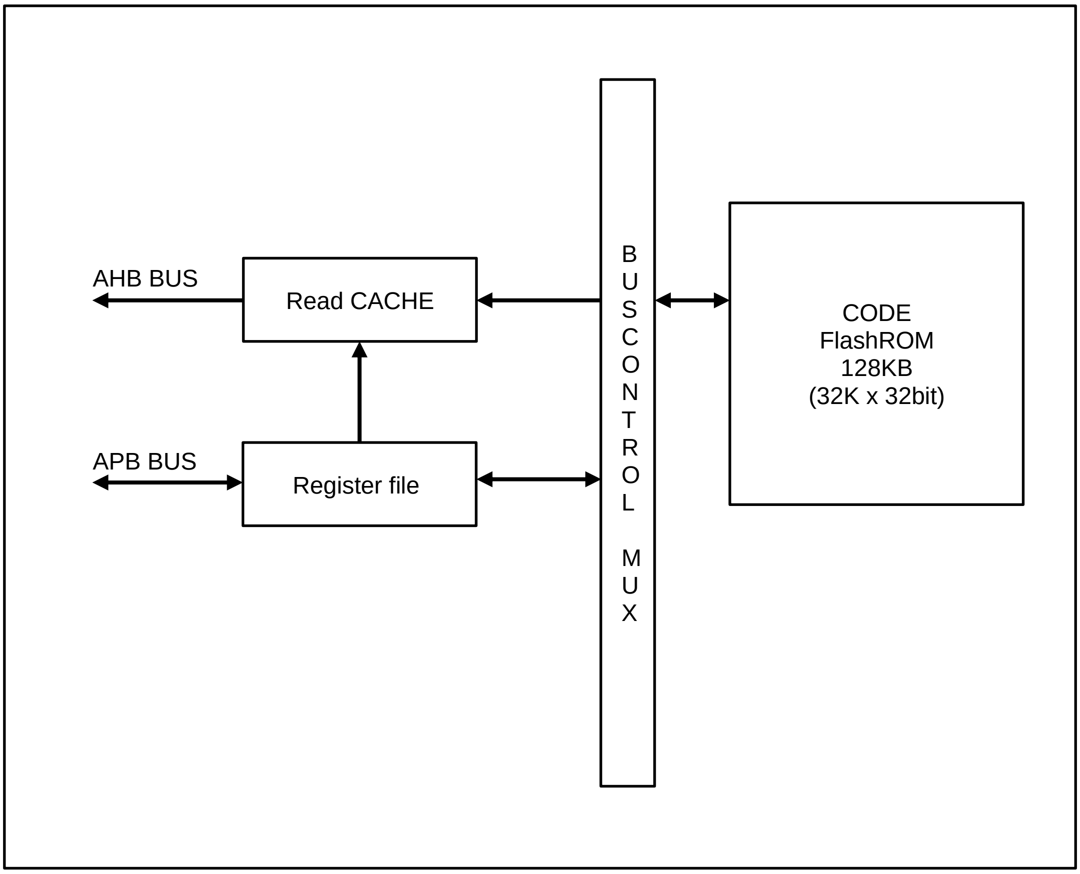


Figure4.1. Block Diagram

4.2 REGISTERS

Base address of Flash Memory Controller is below.

Table4.2. Flash Memory Controller base address

NAME	BASE ADDRESS
Flash Controller	0x4000_0100

Table 4.3 shows Register memory map.

Table4.3. Flash Memory Controller Register map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
FM.MR	0x0004	RW	Flash Memory Mode Select register	0x01000000
FM.CR	0x0008	RW	Flash Memory Control register	0x82000000
FM.AR	0x000C	RW	Flash Memory Address register	0x00000000
FM.DR	0x0010	RW	Flash Memory Data register	0x00000000
FM.TMR	0x0014	RW	Flash Memory Timer register	0x000000bb
FM.DRTY	0x0018	RW	Flash Memory Dirty bit	
FM.TICK	0x001C	RO	Flash Memory Tick Timer	0x00000000
FM.CRC	0x0020	RO	Flash Memory Read CRC Value	
FM.BOOTCR	0x0074	RW	Boot ROM Remap Clear register	0x00000000

4.2.1 FM.MR Flash Memory Mode Register

Internal flash memory mode register. This register is 32-bit register.

FM.MR=0x4000_0104

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOT							IDLE	VERIFY	AMBAEN					TRMEN	TRM							FEMOD	FMOD	ACODE							
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x00							
							R	R	R					R	R							R	R	RW							

31	BOOT	0	
		1	Boot mode enable status(read only)
24	IDLE	0	
		1	Boot mode enable status(read only)
23	VERIFY	0	
		1	Flash Verify mode enable status(read only)
22	AMBAEN	0	AMBA mode disable
		1	AMBA mode enable status(read only)
17	TRMEN	0	
		1	Trim mode entry status(read only)
16	TRM	0	
		1	Trim mode status(read only)
9	FEMOD	0	
		1	Flash mode entry status(read only)
8	FMOD	0	
		1	Flash mode status(read only)
7 0	ACODE	5A → A5	Flash mode
		A5 → 5A	Trim mode
		81 → 28	AMBA mode (FMCR[31:24])

4.2.2 FM.CR Flash Memory Control Register

Internal flash memory control register

FM.CR=0x4000_0108

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved	Reserved	Reserved	Reserved	Reserved		CLK4	CLK3	CRCINIT	CRCEN		TIMER			Reserved	Reserved
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RW	RW	RW	RW		RW	RW	RW	RW		RW			RW	RW

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	EVER	PVER		OTP2E	OTPE		AE			PMOD	WEN	PBLD	PGM	ERS	PBR
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R	RW	RW		RW	RW		RW			RW	RW	RW	RW	RW	RW

25	CLK4	0	If CLK4, CLK3 are 00, flash access in 5 cycles
		1	Flash access in 4 cycles
24	CLK3	0	If CLK4, CLK3 are 00, flash access in 5 cycles
		1	Flash access in 3 cycles
23	CRCINIT	0 1	CRC register winll be initialized. It should be reset again before read flash to generate CRC16 calculation (Initial value of FMCRC is 0xFFFF)
22	CRCEN	0	CRC16 enable
		1	CRC value will be calculated at every flash read timing
20	TIMER	0	Program/Erase timer enable
		1	(timer can be enable by PGM or ERS bit)
14	EVER		Set erase verify mode
13	PVER		Set program verify mode
11	OTPBE		OTP area B enable
10	OTPAE		OTP area A enable
8	AE		All erase enable
5	PMODE		PMODE enable(Address path changing)
4	WE		Write enable
3	PBLD		Page buffer load(WE should be set)
2	PGM		Program enable
1	ERS	0	Program mode enable
		1	Erase mode enable
0	PBR		Page buffer reset

(note)

Before changing the system clock, flash access wait should be set to the maximum value. After the system clock is changed, you will need to set flash access wait that you want if necessary.

4.2.3 FM.AR Flash Memory Address Register

Internal flash memory program, erase address register

FM.AR=0x4000_010C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FADDR														
0	0x0000														
	RW														

14 0	FADDR	32K words address (one word = 4 bytes)

4.2.4 FM.DR Flash Memory Data Register

Internal flash memory program data register

FM.DR=0x4000_0110

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FDATA																															
0x0000_0000																															
RW																															

31 0	FDATA	Flash PGM data (32-bit)

4.2.5 FM.TMR Flash Memory Timer Register

Internal flash memory Timer value register (9-bit), Erase/Program timer runs up to {TMR[8:0],0xFF}

FM.TMR=0x4000_0114

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							TMR								
0	0	0	0	0	0	0	0x0BB								
							RW								

7 0	TMR	Erase/PGM timer (default, 0xBB) Timer counts up to {TMR[8:0], 0xFF} by 20MHz int. OSC clock

4.2.6 FM.DRTY Flash Memory Dirty bit Register

Internal flash memory dirty bit clear register

FM.DRTY=0x4000_0118

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="32">FDRTY</td></tr>
<tr><td colspan="32">-</td></tr>
<tr><td colspan="32">WO</td></tr>
</table>

31 0	FDRTY	Write any value here, cache line fill flag will be cleared.

4.2.7 FM.TICK Flash Memory Tick Timer register

Flash Erase and PGM Timer.

FM.TICK=0x4000_011C

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td colspan="18">FTICK</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="18">0x00000</td></tr>
<tr><td colspan="8"></td><td colspan="24">RW</td></tr>
</table>

17 0	FTICK	TICK goes to 0x3FFFF from written TICK value while TRM runs by PCLK clock

4.2.8 FM.CRC Flash Memory CRC value register

The CRC value resulted from read accesses on internal flash memory.

FM.CRC=0x4000_0120

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td colspan="16">CRC</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="16">--</td></tr>
<tr><td colspan="8"></td><td colspan="24">RO</td></tr>
</table>

15 0	CRC	CRC16 value

4.2.9 FM.BOOTCR Boot ROM Remap Clear Register

Boot ROM remap clear register. This register is 8-bit register.

FM.BOOTCR=0x4000_0174

7	6	5	4	3	2	1	0
							BOOTROM
0	0	0	0	0	0	0	1
							R

0	BOOTROM	Boot Mode (only can be written in boot loader mode) This bit is used to clear boot loader mode at end of boot code (when BOOTROM low, external BOOT pin signal is masked)

4.3 Functional Description

Flash Memory Controller is an internal flash memory interface controller. It mainly controls the program flash memory operation and preparing read data for requesting from the bus.

4.3.1 Flash Orgnization

The 64Kbytes code flash memory consists of 1,024 pages which has uniform 128 bytes page size. The flash controller allows to read or write a data of the flash memory. The read acess can be done by 8, 16 and 32 bits wide

This momory is located at 0x0000_0000 address on system memory map.The system boot address is 0x0000_0000, so this flash memory is boot memory. The code data which is programmed in the flash memory will boot up the device after boot rom sequence is finished.

Flash Memory Controller is an internal flash memory interface controller. It mainly controls the program flash memory operation and preparing read data for requesting from the bus.

4.3.2 Flash Read Operation

The flash data read operation is requested from the bus. The flash controller will response to the request by itself. The wait time should be defined properly. Because normaly the bus speed is faster than flash data access time.

The normal read operation is not available in FLASH MODE in ACODE.FM.MR field.

4.3.3 Flash Program Operation

The erase and program access of flash memory is available only in FLASH MODE in ACODE.FM.MR field. So, self-program is not supported. The flash program/erase operation should be performed by the execution program on the SRAM memory.

The flash program operation will write one page to the target address selected by FM.AR register. At fisrt, user should write the program data into the page buffer. Page buffer write is pefromed by word write access to FM.DR register on FM.AR address. .

After fill the page buffer, user can start to flash write operation and should wait for the IDLE bit set.

Below figure shows page buffer loading operation.

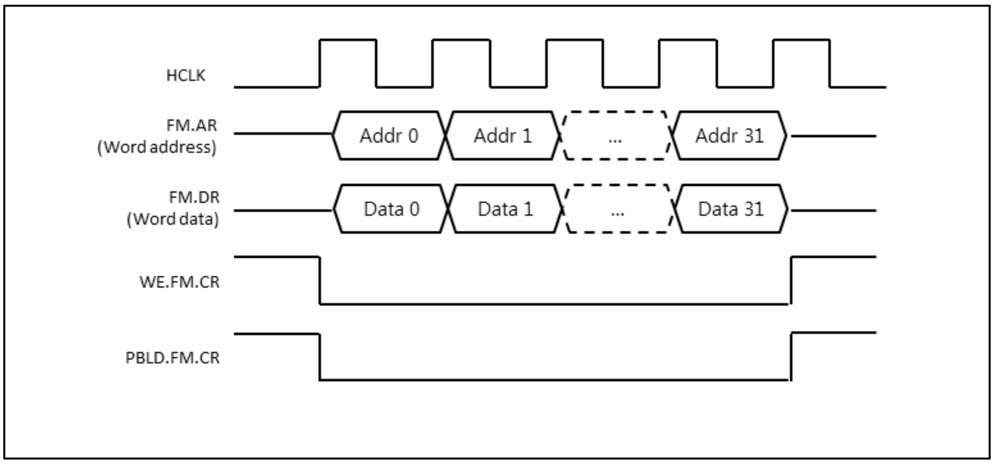


Figure4.2. Page buffer load timing diagram

The flash write of page buffer data is done by PRGM.FM.CR command. The safe writing operation requires propoer program time. The program time tPGM is defined by FM.TMR register. This timer will count the number of HCLK clock to the FM.TMR value. The timer count is start, the IDLE.FM.MR register is cleared. The timer count is done then the IDLE.FM.MR register is set.

In this page write operation, the target page address should be written in FM.AR register.

Below figure shows page write operation.

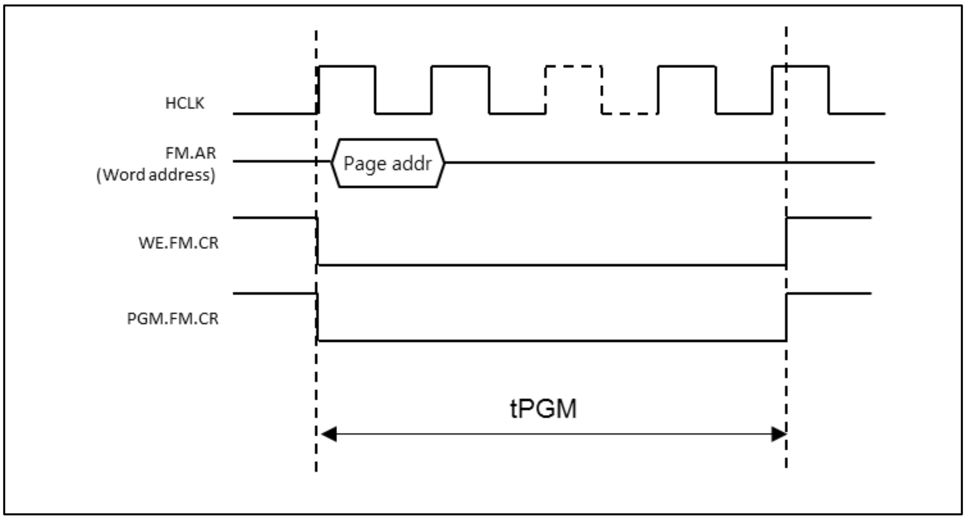


Figure 4.3 Page wirte timing diagram

4.3.4 Flash Erase Operation

The erase and program access of flash memory is available only in FLASH MODE in ACODE.FM.MR field. So, self-program is not supported. The flash program/erase operation should be performed by the execution program on the SRAM memory.

2 kind of flash erase operations are supported. One is page erase and the other one is bulk erase. The page erase operation will erase one page to the target address selected by FM.AR register. .

User starts to flash write operation and should wait for the IDLE bit set.

The bulk erase operation will erase whole flash memory data and the FM.AR address will be ignored. The control is same as the page erase operation except AE.FM.CR bit keep set.

Below figure shows page erase operation.

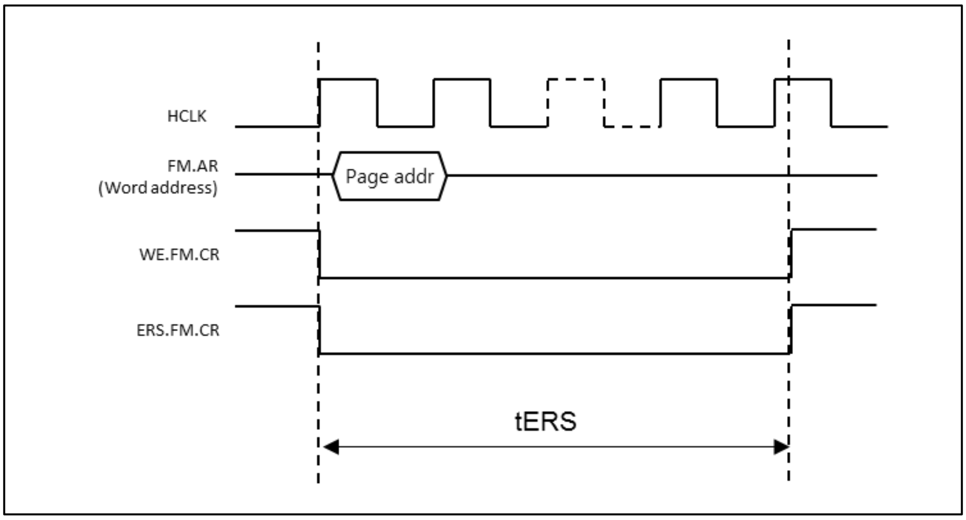


Figure 4.4 Page erase timing diagram

The flash erase of page data is done by ERS.FM.CR command. The safe writing operation requires propoer program time. The erase time tERS is defined by FM.TMR register. This timer will count the number of HCLK clock to the FM.TMR value. The timer count is start , the IDLE.FM.MR register is cleared. The timer count is done then the IDLE.FM.MR register is set.

Below figure shows bulk erase operation.

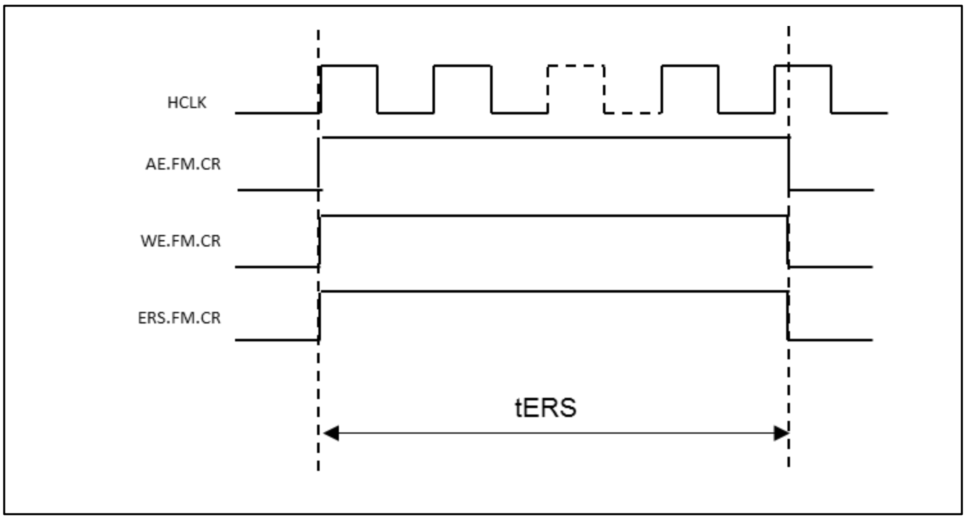


Figure 4.5 Bulk erase timing diagram

CHAPTER 5. INTERNAL SRAM

5.1 OVERVIEW

The AC33MX128 has a block of 0-wait on-chip SRAM. The size of SRAM is 12KB.

The SRAM base address is 0x2000_0000

The SRAM memory area usually used for data memory and stack memory. Sometimes the code is dumped into the SRAM memory for fast operation or flash erase/pgm operation.

This device does not support memory remap starategy. So jump and return is required to perform the code in SRAM memory area

CHAPTER 6. DIRECT MEMORY ACCESS CONTROLLER (DMAC)

6.1 OVERVIEW

DMA is direct memory access controller

- 15 Channels
- Single transfer only
- Support 8/16/32-bit data size
- Support multiple buffer with same size
- Interrupt condition is transferred through peripheral interrupt

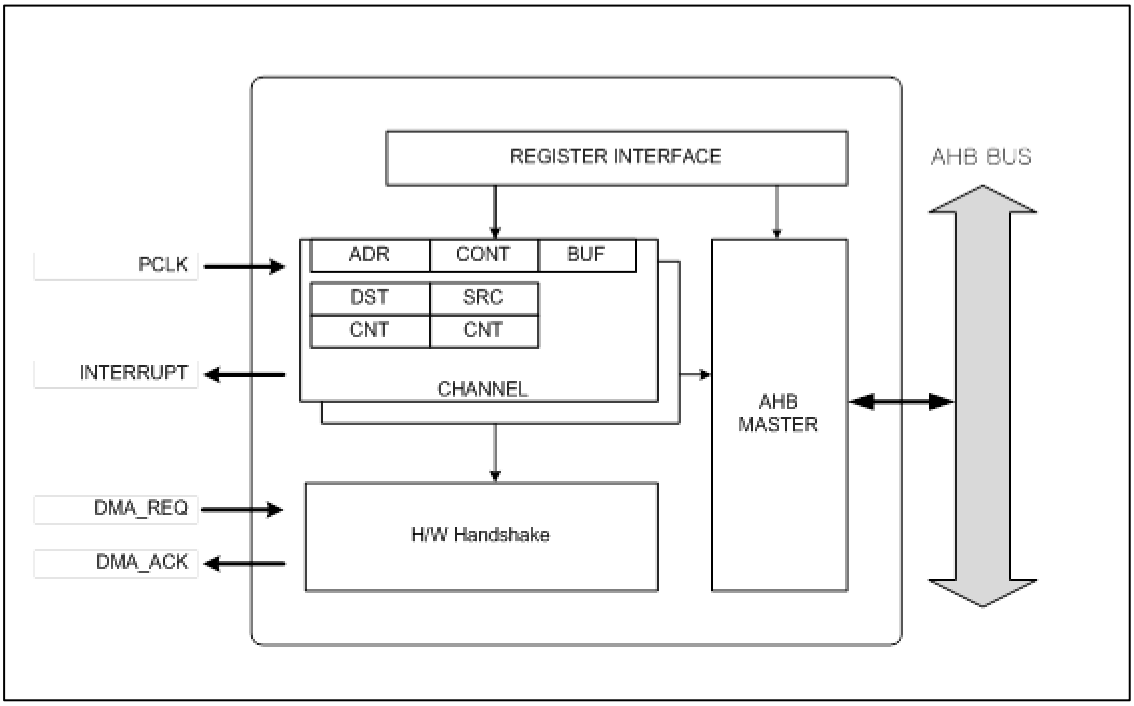


Figure6.1. Block Diagram

6.2 REGISTERS

The base address of DMA controller is below.

Table6.1. DMA Controller base address

NAME	BASE ADDRESS	Assigned Peripheral
DMACH0	0x4000_0400	UART0 RX
DMACH1	0x4000_0410	UART0 TX
DMACH2	0x4000_0420	UART1 RX
DMACH3	0x4000_0430	UART1 TX
DMACH4	0x4000_0440	UART2 RX
DMACH5	0x4000_0450	UART2 TX
DMACH6	0x4000_0460	UART3 RX
DMACH7	0x4000_0470	UART3 TX
DMACH8	0x4000_0480	SPI0 RX
DMACH9	0x4000_0490	SPI0 TX
DMACH10	0x4000_04A0	SPI1 RX
DMACH11	0x4000_04B0	SPI1 TX
DMACH12	0x4000_04C0	ADC0
DMACH13	0x4000_04D0	ADC1
DMACH14	0x4000_04E0	ADC2

Table 6.2 shows register map of DMA controller.

Table6.2. DMAC Register map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
DC0.CR	0x0000	RW	DMA Channel 0 Control Register	0x0000_0000
DC0.SR	0x0004	RW	DMA Channel 0 Status Register	0x0000_0000
DC0.PAR	0x0008	R	DMA Channel 0 Peripheral Address	UART0_RBR
DC0.MAR	0x000C	RW	DMA Channel 0 Memory Address	0x2000_0000
DC1.CR	0x0010	RW	DMA Channel 1 Control Register	0x0000_0000
DC1.SR	0x0014	RW	DMA Channel 1 Status Register	0x0000_0000
DC1.PAR	0x0018	R	DMA Channel 1 Peripheral Address	UART0_THR
DC1.MAR	0x001C	RW	DMA Channel 1 Memory Address	0x2000_0000
DC2.CR	0x0020	RW	DMA Channel 2 Control Register	0x0000_0000
DC2.SR	0x0024	RW	DMA Channel 2 Status Register	0x0000_0000
DC2.PAR	0x0028	R	DMA Channel 2 Peripheral Address	UART1_RBR
DC2.MAR	0x002C	RW	DMA Channel 2 Memory Address	0x2000_0000
DC3.CR	0x0030	RW	DMA Channel 3 Control Register	0x0000_0000
DC3.SR	0x0034	RW	DMA Channel 3 Status Register	0x0000_0000
DC3.PAR	0x0038	R	DMA Channel 3 Peripheral Address	UART1_THR
DC3.MAR	0x003C	RW	DMA Channel 3 Memory Address	0x2000_0000
DC4.CR	0x0040	RW	DMA Channel 4 Control Register	0x0000_0000
DC4.SR	0x0044	RW	DMA Channel 4 Status Register	0x0000_0000
DC4.PAR	0x0048	R	DMA Channel 4 Peripheral Address	UART2_RBR

DC4.MAR	0x004C	RW	DMA Channel 4 Memory Address	0x2000_0000
DC5.CR	0x0050	RW	DMA Channel 5 Control Register	0x0000_0000
DC5.SR	0x0054	RW	DMA Channel 5 Status Register	0x0000_0000
DC5.PAR	0x0058	R	DMA Channel 5 Peripheral Address	UART2_THR
DC5.MAR	0x005C	RW	DMA Channel 5 Memory Address	0x2000_0000
DC6.CR	0x0060	RW	DMA Channel 6 Control Register	0x0000_0000
DC6.SR	0x0064	RW	DMA Channel 6 Status Register	0x0000_0000
DC6.PAR	0x0068	R	DMA Channel 6 Peripheral Address	UART3_RBR
DC6.MAR	0x006C	RW	DMA Channel 6 Memory Address	0x2000_0000
DC7.CR	0x0070	RW	DMA Channel 7 Control Register	0x0000_0000
DC7.SR	0x0074	RW	DMA Channel 7 Status Register	0x0000_0000
DC7.PAR	0x0078	R	DMA Channel 7 Peripheral Address	UART3_THR
DC7.MAR	0x007C	RW	DMA Channel 7 Memory Address	0x2000_0000
DC8.CR	0x0080	RW	DMA Channel 8 Control Register	0x0000_0000
DC8.SR	0x0084	RW	DMA Channel 8 Status Register	0x0000_0000
DC8.PAR	0x0088	R	DMA Channel 8 Peripheral Address	SPI0_RDR
DC8.MAR	0x008C	RW	DMA Channel 8 Memory Address	0x2000_0000
DC9.CR	0x0090	RW	DMA Channel 9 Control Register	0x0000_0000
DC9.SR	0x0094	RW	DMA Channel 9 Status Register	0x0000_0000
DC9.PAR	0x0098	R	DMA Channel 9 Peripheral Address	SPI0_TDR
DC9.MAR	0x009C	RW	DMA Channel 9 Memory Address	0x2000_0000
DC10.CR	0x00A0	RW	DMA Channel 10 Control Register	0x0000_0000
DC10.SR	0x00A4	RW	DMA Channel 10 Status Register	0x0000_0000
DC10.PAR	0x00A8	R	DMA Channel 10 Peripheral Address	SPI1_RDR
DC10.MAR	0x00AC	RW	DMA Channel 10 Memory Address	0x2000_0000
DC11.CR	0x00B0	RW	DMA Channel 11 Control Register	0x0000_0000
DC11.SR	0x00B4	RW	DMA Channel 11 Status Register	0x0000_0000
DC11.PAR	0x00B8	R	DMA Channel 11 Peripheral Address	SPI1_TDR
DC11.MAR	0x00BC	RW	DMA Channel 11 Memory Address	0x2000_0000
DC12.CR	0x00C0	RW	DMA Channel 12 Control Register	0x0000_0000
DC12.SR	0x00C4	RW	DMA Channel 12 Status Register	0x0000_0000
DC12.PAR	0x00C8	R	DMA Channel 12 Peripheral Address	AD0DDR
DC12.MAR	0x00CC	RW	DMA Channel 12 Memory Address	0x2000_0000
DC13.CR	0x00D0	RW	DMA Channel 13 Control Register	0x0000_0000
DC13.SR	0x00D4	RW	DMA Channel 13 Status Register	0x0000_0000
DC13.PAR	0x00D8	R	DMA Channel 13 Peripheral Address	AD1DDR
DC13.MAR	0x00DC	RW	DMA Channel 13 Memory Address	0x2000_0000
DC14.CR	0x00E0	RW	DMA Channel 14 Control Register	0x0000_0000
DC14.SR	0x00E4	RW	DMA Channel 14 Status Register	0x0000_0000
DC14.PAR	0x00E8	R	DMA Channel 14 Peripheral Address	AD2DDR
DC14.MAR	0x00EC	RW	DMA Channel 14 Memory Address	0x2000_0000

6.2.1 DC*n*.CR DMA Controller Configuration Register

DMA operation control register is 32-bit register.

DC0.CR=0x4000_0400 , DC1.CR=0x4000_0410
DC2.CR=0x4000_0420 , DC3.CR=0x4000_0430
DC4.CR=0x4000_0440 , DC5.CR=0x4000_0450
DC6.CR=0x4000_0460 , DC7.CR=0x4000_0470
DC8.CR=0x4000_0480 , DC9.CR=0x4000_0490
DC10.CR=0x4000_04A0 , DC11.CR=0x4000_04B0
DC12.CR=0x4000_04C0 , Dc13.CR=0x4000_04D0
DC14.CR=0x4000_04E0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				TRANSCNT																								SIZE			
0	0	0	0	0x000												0	0	0	0	0	0	0	0	0	0	0	0	00		0	0
RW																								RW							

31 16	TRANSCNT	Number of DMA transfer remained Required transfer number should be written before enable DMA transfer.	
		0	DMA transfer is done.
		N	N transfers are remained
3 2	SIZE	Bus transfer size.	
		00	DMA transfer is byte size transfer
		01	DMA transfer is half word size transfer
		10	DMA transfer is word size transfer
		11	Reserved

6.2.2 DC*n*.SR DMA Controller Status register

DMA Controller Status Register is 8-bit register.

This register represents the current status of DMA Controller and enables DMA function.

DC0.SR=0x4000_0404 , DC1.SR=0x4000_0414
DC2.SR=0x4000_0424 , DC3.SR=0x4000_0434
DC4.SR=0x4000_0444 , DC5.SR=0x4000_0454
DC6.SR=0x4000_0464 , DC7.SR=0x4000_0474
DC8.SR=0x4000_0484 , DC9.SR=0x4000_0494
DC10.SR=0x4000_04A4 , DC11.SR=0x4000_04B4
DC12.SR=0x4000_04C4 , Dc13.SR=0x4000_04D4
DC14.SR=0x4000_04E4

7	6	5	4	3	2	1	0
EOT							DMAEN
1	0	0	0	0	0	0	0
RO							RW

7	EOT	End of transfer.	
		0	Data to be transferred is existing. TRANSCNT shows non zero value
		1	All data is transferred. TRANSCNT shows now 0
0	DMAEN	DMA Enable	
		0	DMA is in stop or hold state
		1	DMA is running or enabled

6.2.3 DC*n*.PAR DMA Controller Peripheral Address register

These registers represent the peripheral address.

DC0.PAR=0x4000_0408 , DC1.PAR=0x4000_0418
DC2.PAR=0x4000_0428 , DC3.PAR=0x4000_0438
DC4.PAR=0x4000_0448 , DC5.PAR=0x4000_0458
DC6.PAR=0x4000_0468 , DC7.PAR=0x4000_0478
DC8.PAR=0x4000_0488 , DC9.PAR=0x4000_0498
DC10.PAR=0x4000_04A8,, DC11.PAR=0x4000_04B8
DC12.PAR=0x4000_04C8,, Dc13.PAR=0x4000_04D8
DC14.PAR=0x4000_04E8

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PAR																															
DC0.PAR=U0.RBR, DC1.PAR=U0THR DC2.PAR=U10RBR, DC3.PAR=U10THR DC4.PAR=U20RBR, DC5.PAR=U20THR DC6.PAR=U30RBR, DC7.PAR=U30THR DC8.PAR=SPI0_RDR, DC9.PAR=SPI0_TDR DC10.PAR=SPI1_RDR, DC11.PAR=SPI1_TDR DC1.2PAR=AD0.DDR, DC13.PAR=AD1.DDR, DC14.PAR=AD2.DDR																															
RO																															

31 0	PAR	Target Peripheral address of transmit buffer or receive buffer. Address is fixed address when each transfer is done.

6.2.4 DC*n*.MAR DMA Controller Memory Address register

These registers represent the memory address.

DC0.MAR=0x4000_040C , DC1.MAR=0x4000_041C
DC2.MAR=0x4000_042C , DC3.MAR=0x4000_043C
DC4.MAR=0x4000_044C , DC5.MAR=0x4000_045C
DC6.MAR=0x4000_046C , DC7.MAR=0x4000_047C
DC8.MAR=0x4000_048C , DC9.MAR=0x4000_049C
DC10.MAR=0x4000_04AC,, DC11.MAR=0x4000_04B8C
DC12.MAR=0x4000_04CC, DC13.MAR=0x4000_04DC
DC14.MAR=0x4000_04EC

31–16	15–0
	MAR
0x2000	0x0000
RO	RW

31 0	MAR	Target memory address of data transfer. Address is automatically incremented according to SIZE bits when each transfer is done.

6.3 Functional description

The DMA controller performs direct memory transfer by sharing the system bus with CPU core. The system bus is shared by 2 AHB masters following the round-robin priority strategy. So the DMA controller can share the half of system bandwidth.

The DMA controller can be triggered only peripheral request. When a peripheral request the transfer to the DMA controller, related channel is activate and access the bus to transfer requested data from memory to peripheral data buffer or from peripheral data buffer to memory space.

- User set both of peripheral address and memory address
- User configure DMA operation mode and transfer count.
- User enable DMA channel
- DMA request is occurred from peripheral.
- DMA activate channel which was requested
- DMA read data from source address and save it internal buffer.
- DMA write the buffered data to destination address.
- Transfer count number is decreased by 1.
- When Transfer count is 0, EOT flag is set and notice to peripheral to issue the interrupt
- DMA does not have interrupt source, the interrupt related DMA status can be shown from assigned peripheral interrupt.

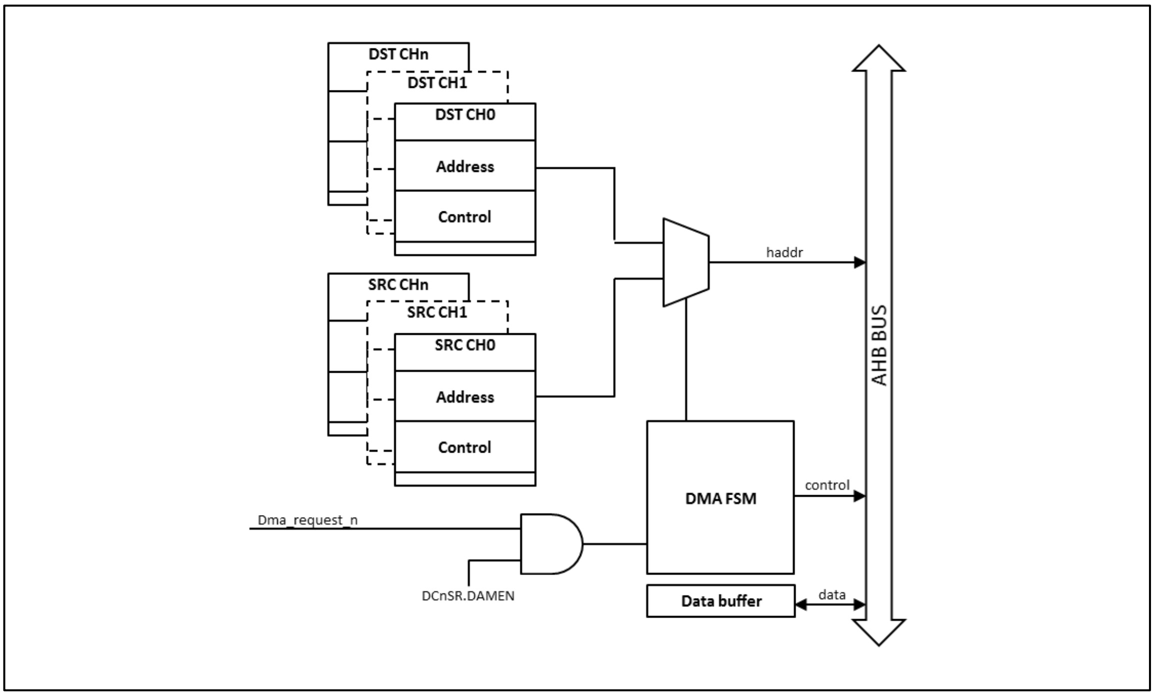


Figure6.2. Block Diagram

Below figure shows the functional timing diagram of dma controller. The transfer request from peripheral is pended internally and it will invoke source data read transfer on the AHB bus. The read data from the source address is stored in the internal buffer. Then this data will be transferred to the destination address when the AHB bus is available.

The timing diagram for a dma transfer from peripheral to memory is shown in below figure. 4-clock cycle latency exists during accessing the peripheral. If the bus is occupied by different bus master, there are amount of bus waiting cycles.

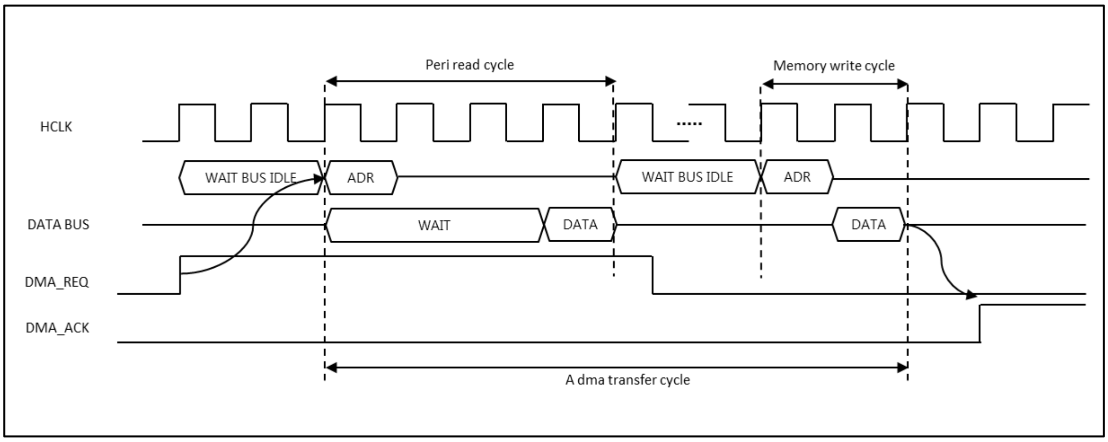


Figure 6.3. DMA transfer from peripheral to memory

The timing diagram for a dma transfer from memory to peripheral is shown in below figure. 4-clock cycle latency exists during accessing the peripheral. If the bus is occupied by different bus master, there are amount of bus waiting cycles.

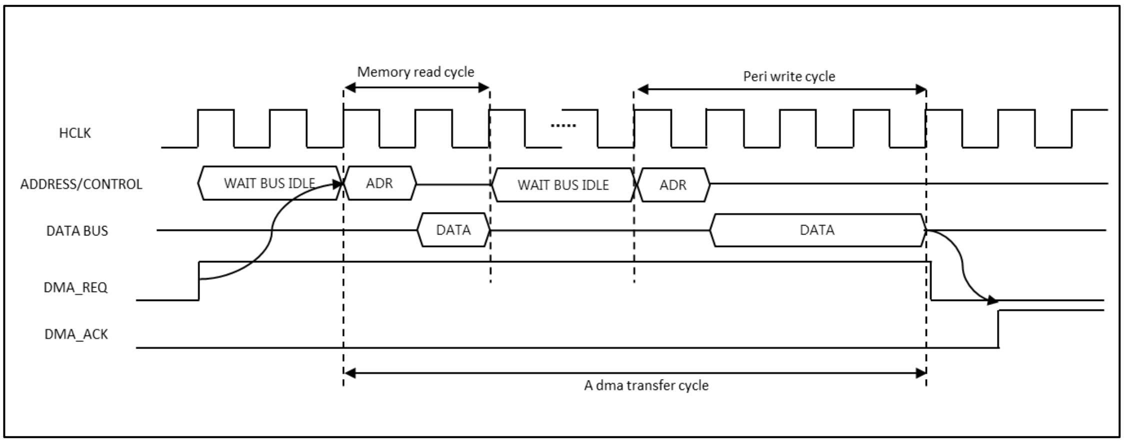


Figure 6.4. DMA transfer from memory to peripheral

The figure is an example N data transfers with the DMA. The DMA transfer is started when DCnSR.DMAEN is set and will be cleared when all the number of transfer is completed.

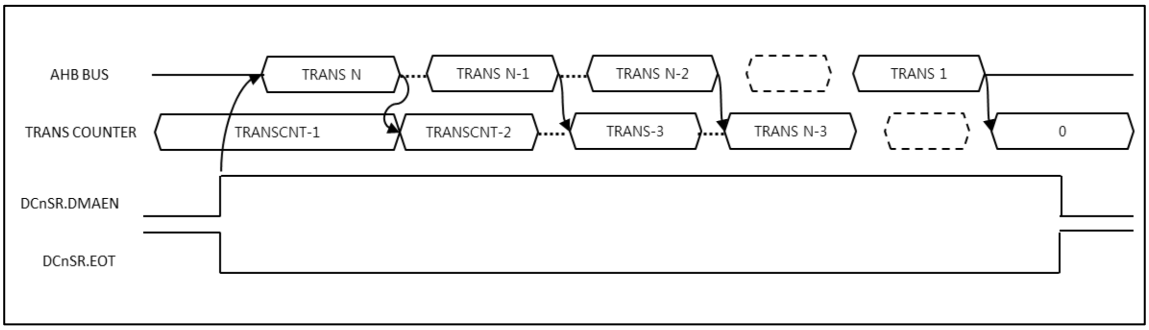


Figure 6.5. N DMA transfer example

CHAPTER 7. WATCH-DOG TIMER (WDT)

7.1 OVERVIEW

The Watchdog timer can monitor the system and generate an interrupt or a reset. It has 32-bit down-counter.

- 32-bit down counter (WDTCNT)
- Select reset or periodic interrupt
- Count clock selection
- Dedicated pre-scaler
- Watchdog overflow output signal

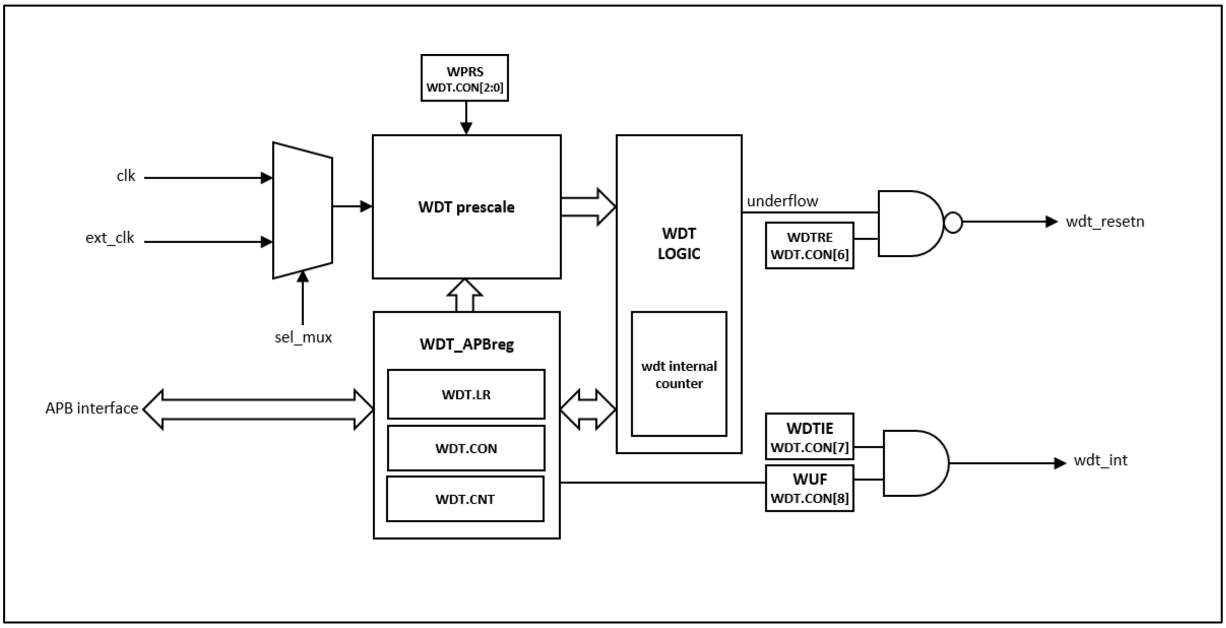


Figure7.1. Block diagram

7.2 REGISTERS

The base Address of watchdog timer is 0x4000_0200 and register map is described in Table 7.2
Initial watchdog time-out period is set to 2000-milisecond.

Table7.1. Base address of SCU

NAME	BASE ADDRESS
WDT	0x4000_0200

Table7.2. Watchdog timer register map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
WDT.LR	0x0000	W	WDT Load register	0x00000000
WDT.CNT	0x0004	R	WDT Current counter register	0x0000FFFF
WDT.CON	0x0008	RW	WDT Control register	0x0000805C

7.2.1 WDT.LR Watchdog Timer Load Register.

The WDTLR register is used to update WDTCNT register. To update WDTCNT register, the WDTEN bit of WDTCON should be set to '1' and write into WDTLR register with target value of WDTCNT. It needs at least 5 WDT counter clocks to update WDTLR to WDTCNT.

WDT.LR=0x4000_0200

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDTLR																															
0x0000_0000																															
W																															

31 0	WDTLR	Watchdog timer load value register Keeping WDTEN bit as '1', write WDTLR register will update WDTCNT value with written value

7.2.2 WDT.CNT Watchdog Timer Current Counter Register.

The WDTCNT register represent the current count value of 32-bit down counter. When the counter value reach to 0, the interrupt or reset will be asserted.

WDT.CNT=0x4000_0204

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDTCNT																															
0x0000_FFFF																															
R																															

31 0	WDTCNT	Watchdog timer current counter register 32-bit down counter will run from the written value.

7.2.3 WDT.CON Watchdog Timer Control Register

WDT module should be configured properly before running. WDT module can make reset event or assert interrupt signal to system. If user don't use both reset and interrupt functions, WDT can be used like a loadable down-counter. WUF flag will be set when WDT counts down to 0.

WDT.CON=0x4000_0208

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDBG							WUF	WDTIE	WDTRE		WDTEN	CKSEL	WPRS		
1	0	0	0	0	0	0	0	0	1	0	1	1	100		
RW							R	RW	RW		RW	RW	RW		

15	WDBG	Watchdog operation control in debug mode	
		0	Watchdog counter running when debug mode
		1	Watchdog counter stopped when debug mode
8	WUF	Watchdog timer underflow flag (This bit is cleared when WDTLR is written)	
		0	No underflow
		1	Underflow is pending
7	WDTIE	Watchdog timer counter underflow interrupt enable	
		0	Disable interrupt
		1	Enable interrupt
6	WDTRE	Watchdog timer counter underflow reset enable	
		0	Disable reset
		1	Enable reset
4	WDTEN	Watchdog Counter enable	
		0	Watch dog counter disabled
		1	Watch dog counter enabled
3	CKSEL	WDTCLKIN clock source select	
		0	PCLK
		1	External clock
2 0	WPRS[2:0]	Counter clock prescaler WDTCLK = WDTCLKIN/WPRS	
		000	WDTCLKIN
		001	WDTCLKIN / 4
		010	WDTCLKIN / 8
		011	WDTCLKIN / 16
		100	WDTCLKIN / 32
		101	WDTCLKIN / 64
		110	WDTCLKIN / 128
		111	WDTCLKIN / 256

7.3 Functional Description

The watchdog timer Count can be enabled by WDTEN (WDT.CON[4]) to 1. As watchdog timer is enabled, the down counter will start counting from the Load Value. If WDTRE (WDT.CON[6]) is set as 1, WDT reset would be asserted when the WDT counter value reached to 0(underflow event) from WDTLR value. Before WDT counter down to 0, software can write a certain value to register WDTLR to reload WDT counter.

7.3.1 Timing diagram

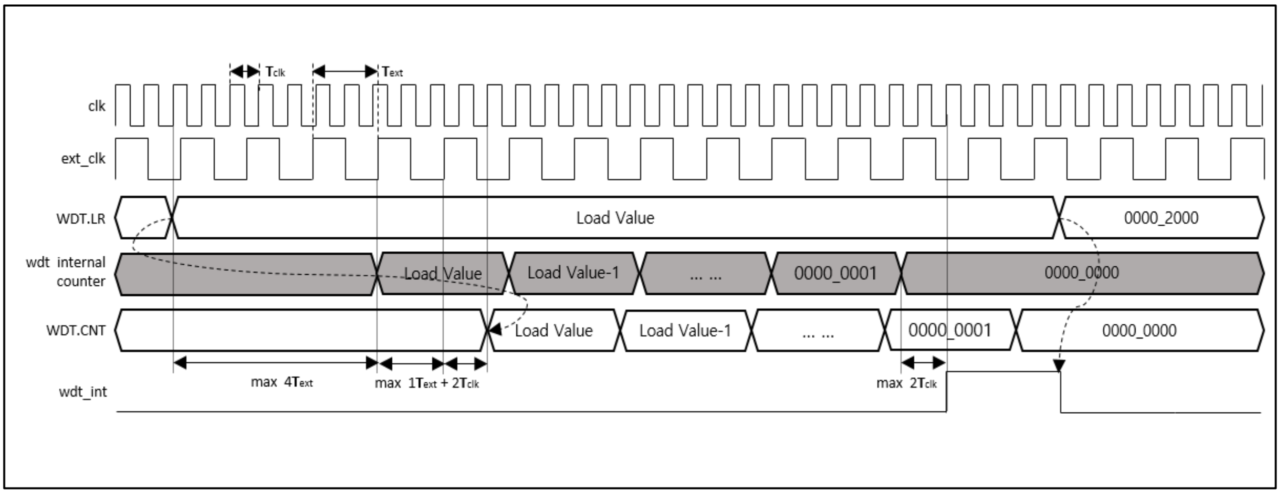


Figure 7.2 Timing diagram in interrupt mode operation when WDT clock is external clock

In WDT interrupt mode, once WDT underflow occurred then a certain count value would be reloaded to prevent next WDT interrupt in short time period and this reloading action only be activated when the watchdog timer counter set to be Interrupt mode(set WDTIE of WDT.CON). It takes up to 5 cycles from Load value to the CNT value. The WDT interrupt signal and CNT value data might be delayed maximum by 2 system bus clocks in synchronous logic.

7.3.2 Prescale table

The WDT includes a 32-bit down counter with programmable pre-scaler to define different time-out intervals.

The clock sources of watchdog timer can be peripheral clock (PCLK) or one of 5 external clock sources. External clock source can be enabled by CKSEL (WDT.CON[3]) set to '1' and External clock source was chosen in MCCR3 register of SCU(system control unit) block.

To make WDT counter base clock, user can control 3-bit pre-scaler WPRS [2:0] in WDT.CON register and the maximum pre-scaled value is "clock source frequency/256". The pre-scaled WDT counter clock frequency values are listed in following table.

Selectable clock source (40 kHz ~ 16 MHz) and the time out interval when 1 count

Time out period = {(Load Value) * (1/pre-scaled WDT counter clock frequency) + max 5T_{ext}} + max 4T_{clk}

*Time out period (time out period from load Value to interrupt set '1')

Table7.3. Pre-scaled WDT counter clock frequency

Clock source	WDTCLKIN	WDTCLKIN /4	WDTCLKIN /8	WDTCLKIN /16	WDTCLKIN /32	WDTCLKIN /64	WDTCLKIN /128	WDTCLKIN /256
Ring OSC	1Mhz	250khz	125khz	62.5khz	31.25khz	15.625khz	7.8125khz	3.90625khz
MCLK	MCLK (BUS CLK)	MCLK/4	MCLK/8	MCLK/16	MCLK/32	MCLK/64	MCLK/128	MCLK/256
IOSC	20Mhz	5Mhz	2.5Mhz	1.25Mhz	625khz	312.5khz	156.25khz	78.125khz
EOSC	XTAL	XTAL/4	XTAL/8	XTAL/16	XTAL/32	XTAL/64	XTAL/128	XTAL/256
PLL	PLL	PLL/4	PLL/8	PLL/16	PLL/32	PLL/64	PLL/128	PLL/256

CHAPTER 8. 16-BIT TIMER

8.1 OVERVIEW

The timer block is consisted with 6 channels of 16 bit General purpose timers. They can support periodic timer, PWM pulse, one-shot timer and capture mode.

- 16-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 10-bit prescaler

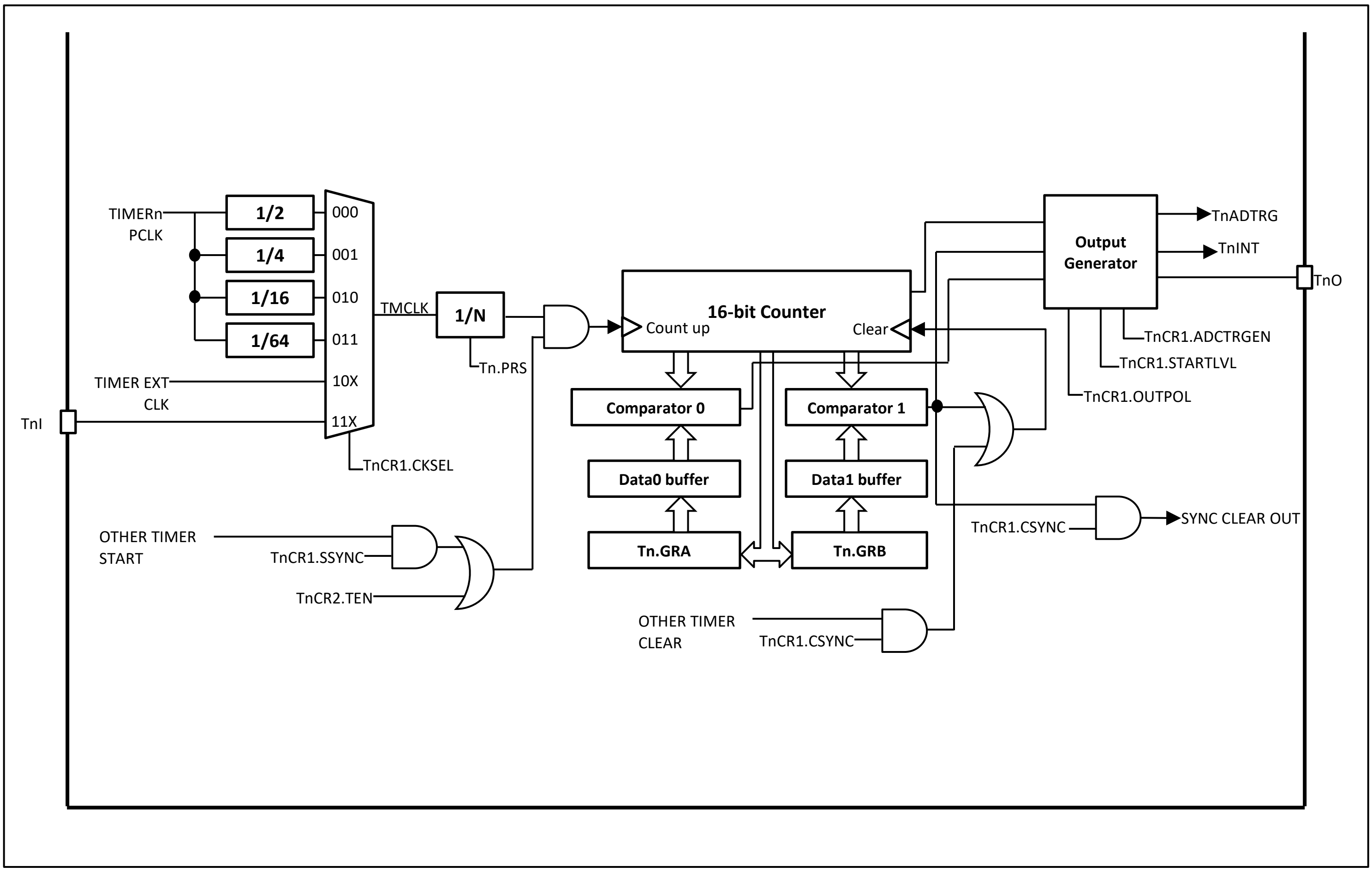


Figure8.1. Block diagram

8.2 Pin description

Table8.1. External pin

PIN NAME	TYPE	DESCRIPTION
TnC	I	External clock / capture input
TnO	O	Timer output

8.3 REGISTERS

The base Address of TIMER is 0x4000_3000 and register map is described in Table.8.2 and 8.3.

Table8.2. Base address of each channel

NAME	BASE ADDRESS
T0	0x4000_3000
T1	0x4000_3020
T2	0x4000_3040
T3	0x4000_3060
T8	0x4000_3100
T9	0x4000_3120

Table8.3. Timer register map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
T*n*.CR1	0x--00	RW	Timer control register 1	0x00000000
T*n*.CR2	0x--04	RW	Timer control register 2	0x00000000
T*n*.PRS	0x--08	RW	Timer prescaler register	0x00000000
T*n*.GRA	0x--0C	RW	Timer general data register A	0x00000000
T*n*.GRB	0x--10	RW	Timer general data register B	0x00000000
T*n*.CNT	0x--14	RW	Timer counter register	0x00000000
T*n*.SR	0x--18	RW	Timer status register	0x00000000
T*n*.IER	0x--1C	RW	Timer interrupt enable register	0x00000000
TGECR	0x0140	RW	Timer Group Encoder Control Register	0x00000000

8.3.1 Tn.CR1 Timer n Control Register 1

Timer Control Register 1 is 16-bit register.

Timer module should be configured properly before running. When target purpose is defined, the timer can be configured in the Tn.CR1 register

T0.CR1=0x4000_3000, T1.CR1=0x4000_3020
T2.CR1=0x4000_3040, T3.CR1=0x4000_3060
T8.CR1=0x4000_3100, T9.CR1=0x4000_3120

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							ADCTRGEN	STARTLV	CKSEL			CLRMOD		MODE	
0	0	0	0	0	0	0	0	0	000			00		00	
							RW	RW	RW			RW		RW	

8	ADCTRGEN	ADC Triger source enable	
		0	Timer does not trigger ADC
		1	Timer triggers ADC
7	STARTLVL	Interval/PWM/One-shot mode initial output value	
		0	Output starts with 'L'
		1	Output starts with 'H'
6 4	CKSEL[2:0]	Counter clock source select	
		000	PCLK/2
		001	PCLK/4
		010	PCLK/16
		011	PCLK/64
		10X	TEXT0 (in MCCR3)
		11X	TnC pin input
3 2	CLRMD	Clear select when capture mode	
		00	Rising edge clear mode
		01	Falling edge clear mode
		10	Both edge clear mode
		11	None clear mode
1 0	MODE[1:0]	Timer operation mode control	
		00	Normal periodic operation mode
		01	PWM mode
		10	One shot mode
		11	Capture mode

8.3.2 Tn.CR2 Timer n Control Register 2

Timer Control Register 2 is 8-bit register.

T0.CR2=0x4000_3004, T1.CR2=0x4000_3024
T2.CR2=0x4000_3044, T3.CR2=0x4000_3064
T8.CR2=0x4000_3104, T9.CR2=0x4000_3124

7	6	5	4	3	2	1	0
						TCLR	TEN
0	0	0	0	0	0	0	0
R	R	R	R	R	R	WO	RW

1	TCLR	Timer Count register clear	
		0	No
		1	Initialize timer. If set to '1', count register will be cleared. This is write-only.
0	TEN	Timer enable bit	
		0	Disable timer
		1	Enable timer

8.3.3 Tn.PRS Timer n Prescaler Register

Timer Prescaler Register is 16-bit register in order to prescale the counter input clock.

T0.PRS=0x4000_3008, T1.PRS=0x4000_3028
T2.PRS =0x4000_3048, T3.PRS=0x4000_3068
T8.PRS=0x4000_3108, T9.PRS=0x4000_3128

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						PRS									
0	0	0	0	0	0	000									
						RW									

9 0	PRS	Pre-scale value of count clock TCLK = CLOCK_IN/(PRS+1) (*CLOCK_IN* is a selected timer input clock in TnCR1[CKSEL])

8.3.4 Tn.GRA Timer n General Register A

Timer General Register A is 16-bit register.

T0.GRA=0x4000_300C, T1.GRA=0x4000_302C
T2.GRA =0x4000_304C, T3.GRA=0x4000_306C
T8.GRA=0x4000_310C, T9.GRA=0x4000_312C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GRA															
0x0000															
RW															

15 0	GRA	Timer n General Register A
		Periodic mode - Period value of time internal. - When the counter value is matched with this value, GRA Match interrupt is requested
		PWM mode - Duty value of PWM Output - When the counter value is matched with this value, GRA Match interrupt is requested
		One-shot mode - One-shot delay timing before output pulse. - When the counter value is matched with this value, GRA Match interrupt is requested
		Capture mode - Falling edge of TnC port will capture the count value when rising edge clear mode - Rising edge of TnC port will capture the count value when falling edge clear mode

8.3.5 Tn.GRB Timer n General Register B

Timer General Register B is 16-bit register.

T0.GRB=0x4000_3010, T1.GRB=0x4000_3030
T2.GRB=0x4000_3050, T3.GRB=0x4000_3070
T8.GRB=0x4000_3110, T9.GRB=0x4000_3130

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GRB															
0x0000															
RW															

Bits	Name	Description
15 0	GRB	Timer n General Register A
		Periodic mode - Not used. No interrupt generated.
		PWM mode - Time interval value of PWM carrier frequency. - When the counter value is matched with this value, GRB Match interrupt is requested only in PWM and one-shot modes.
		One-shot mode - One-shot pulse output stop timing value. - When the counter value is matched with this value, GRB Match interrupt is requested only in PWM and one-shot modes.
		Capture mode - Rising edge of TnC port will capture the count value when rising edge clear mode - Falling edge of TnC port will capture the count value when falling edge clear mode

8.3.6 Tn.CNT Timer n Count Register.

Timer Count Register is 16-bit register.

T0.CNT=0x4000_3014, T1.CNT=0x4000_3034
T2.CNT=0x4000_3054, T3.CNT=0x4000_3074
T8.CNT=0x4000_3114, T9.CNT=0x4000_3134

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT															
0x0000															
RW															

Bits	Name	Description
15 0	CNT	Timer count value register
		R Read current timer count value
		W Set count value

8.3.7 Tn.SR Timer n Status Register

Timer Status Register is 8-bit register.

This register indicates the current status of timer module

T0.SR=0x4000_3018, T1.SR=0x4000_3038
T2.SR=0x4000_3058, T3.SR=0x4000_3078
T8.SR=0x4000_3118, T9.SR=0x4000_3138

7	6	5	4	3	2	1	0
		QDIRCH	QRF		MFA	MFB	OVF
0	0	0	0	0	0	0	0
		RW	RW		RW	RW	RW

5	QDIRCH	Quadrature direction change	
		0	No direction change
		1	Direction is changed. Write '1' to this bit for clear
4	QRF	Quadrature revolution flag	
		0	No revolution flag
		1	Revolution flag is detected. Write '1' to this bit for clear
2	MFA	GRA Match flag	
		0	Not match with GRA
		1	Match flag with GRA. Write '1' to this bit for clear
1	MFB	GRB Match flag	
		0	Not match with GRB
		1	Match flag with GRB. Write '1' to this bit for clear
0	OVF	Counter overflow flag	
		0	No overflow event
		1	Counter overflowed. Write '1' to this bit for clear

8.3.8 Tn.IER Timer n Interrupt Enable Register

Timer Interrupt Enable Register is 8-bit register.

Each status flag of the timer block can issue the interrupt. To enable the interrupt, write “1” in correspondent bit in the Tn.IER register.

T0.IER=0x4000_301C, T1.IER=0x4000_303C
T2.IER=0x4000_305C, T3.IER=0x4000_307C
T8.IER=0x4000_311C, T9.IER=0x4000_313C

7	6	5	4	3	2	1	0
	QERRIE	QDIRCHIE	QRIE		MAIE	MBIE	OVIE
0	0	0	0	0	0	0	0
	RW	RW	RW		RW	RW	RW

6	QERRIE	Quadrature decoder error interrupt enable	
		0	Disable Quadrature decoding error interrupt
		1	Enable Quadrature decoding error interrupt
5	QDIRCHIE	Quadrature direction change interrupt enable	
		0	Disable direction change interrupt
		1	Enable direction change interrupt
4	QRIE	Quadrature revolution interrupt enable	
		0	Disable revolution flag interrupt
		1	Enable revolution flag interrupt
2	MAIE	GRA Match interrupt enable	
		0	Disable match register A interrupt
		1	Enable match register A interrupt
1	MBIE	GRB Match interrupt enable	
		0	Disable match register B interrupt
		1	Enable match register B interrupt
0	OVIE	Counter overflow interrupt enable	
		0	Disable counter overflow interrupt
		1	Enable counter overflow interrupt

8.3.9 TGECR Timer Group Encoder Control Register

Timer Group Encoder Control Register is 16-bit register.

Timer0, Timer1, Timer2 and Timer3 can be used quadrature encoder interface function.

TGECR=0x4000_3140

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				RDIRCON	PDIRCON	BDIRCON	ADIRCON	QDPHBEG		QDPHAEG		QDPHZEG	QDPHSWAP		QDMOD
0	0	0	0	0	0	0	0	00		00		0	0	0	0
				RW	RW	RW	RW	RW		RW		RW	RW		RW

11	RDIRCON	Revolution counter direction control	
		0	DIR status not affect to the counter
		1	DIR status will change count direction
10	PDIRCON	Position counter direction control	
		0	DIR status not affect to the counter
		1	DIR status will change count direction
9	BDIRCON	Phase B counter direction control	
		0	DIR status not affect to the counter
		1	DIR status will change count direction
8	ADIRCON	Phase A counter direction control	
		0	DIR status not affect to the counter
		1	DIR status will change count direction
7 6	QDPHBEG[1:0]	Quadrature mode phase B count for position count	
		00	Rising edge count
		01	Falling edge count
		1X	Both edge count
5 4	QDPHAEG[1:0]	Quadrature mode phase A count for position count	
		00	Rising edge count
		01	Falling edge count
		1X	Both edge count
3	QDPHZEG	Quadrature mode phase Z count for revolution	
		0	PHZ rising edge count
		1	PHZ falling edge count
2	QDPHSWAP	Quadrature input swap	
		0	No swap
		1	Swap PHA and PHB
0	QDMOD	Quadrature decoder mode	
		0	Normal timer mode
		1	Quadrature decoder count mode Timer0 is phase A counter Timer1 is phase B counter Timer2 is position counter Timer3 is revolution counter

8.4 Functional Description

8.4.1 Timer basic operation

TMCLK in Figure 8.2 is reference clock for operation of the timer. This clock will be divided by prescaler setting and the counting clock will work. Below figures show the strating point of the counter and the ending of the period point of the counter in normal periodic mode.

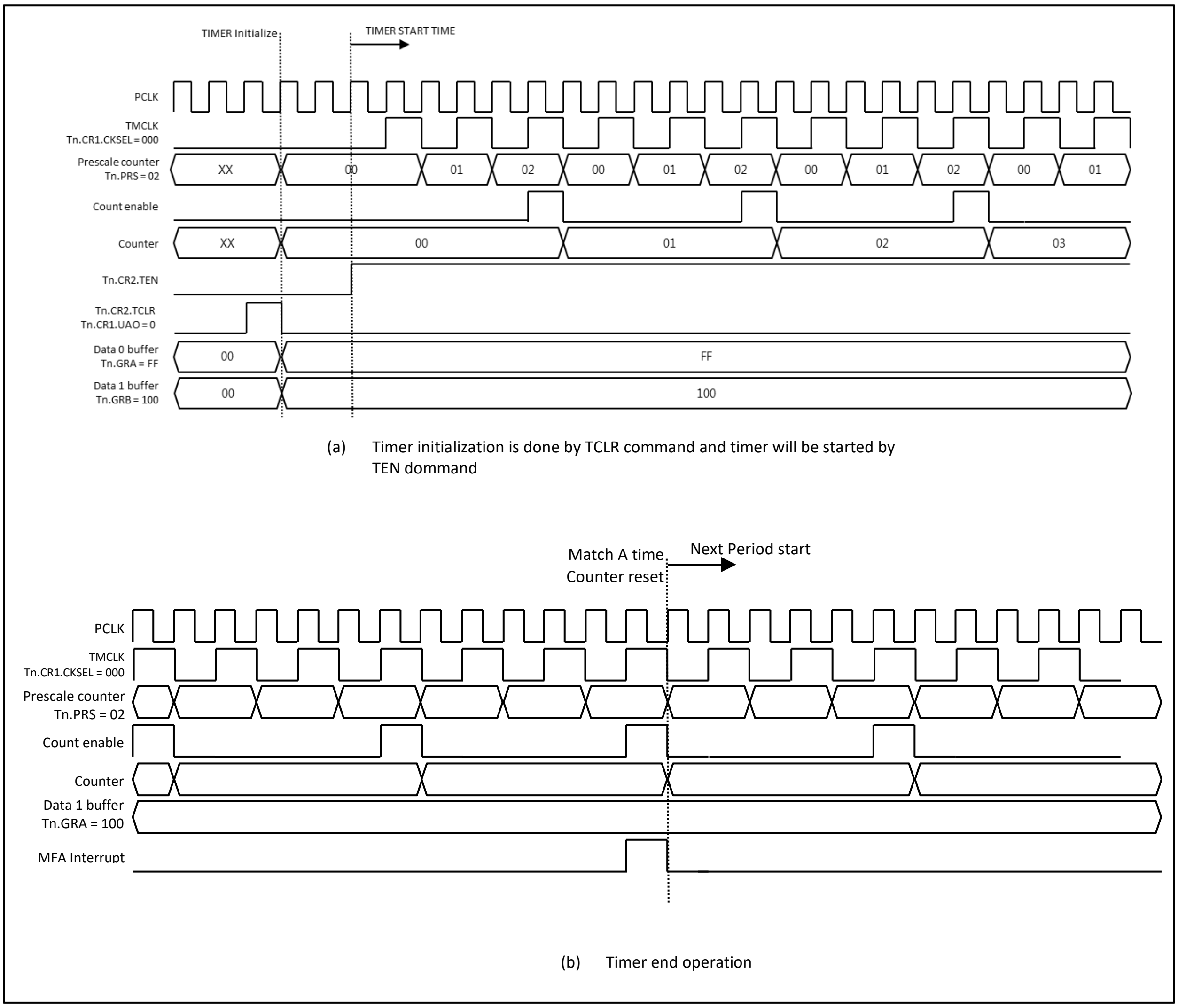


Figure 8.2 Basic start and match operation

The period of timer count can be calculated as below equation.

The period = TMCLK Period * Tn.GRA value.
Match A interrupt time = TMCLK Period * Tn.GRA value.

When you change the timer setting and restart the timer with new setting, it's recommended that you should write CR2.TCLR command before CR2.TEN command.

8.4.2 Normal Periodic Mode

Figure 8.3 shows the timing diagram in normal periodic mode. Tn.GRA value decides the timer period. Tn.GRM register value is don't care.

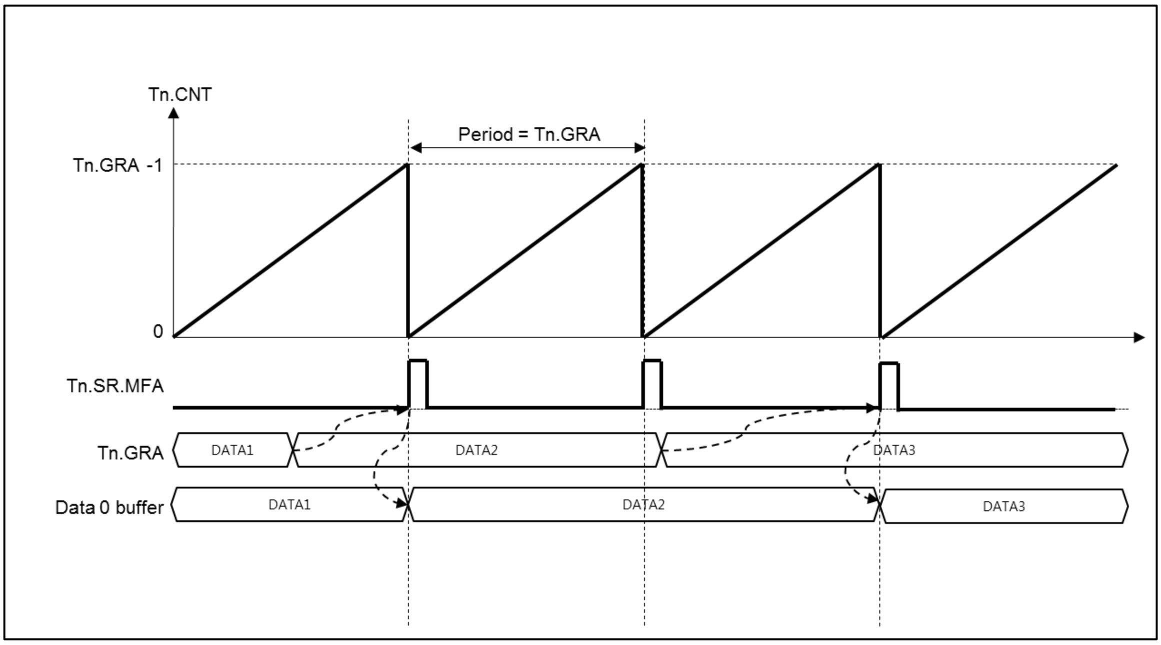


Figure 8.3 Normal periodic mode operation

The priod of timer count can be calculated as below equation.

The period = TMCLK Period * Tn.GRA value.
Match A interrupt time = TMCLK Period * Tn.GRA value.

If Tn.GRA = 0, the timer can not be started even TnCR2.TEN is "1". Because the period is "0".

The value in Tn.GRA and Tn.GRB is loaded into internal compare data buffer 0 when the loading condition is occured. In the periodic mode, Tn.CR2.TCLR write operation will load the data buffer and the next GRA match event will load the data buffer.

8.4.3 One shot Mode

Figure 8.4 shows the timing diagram in one shot mode. Tn.GRB value decides the one shot period. One more compare point is provided with Tn.GRA register value.

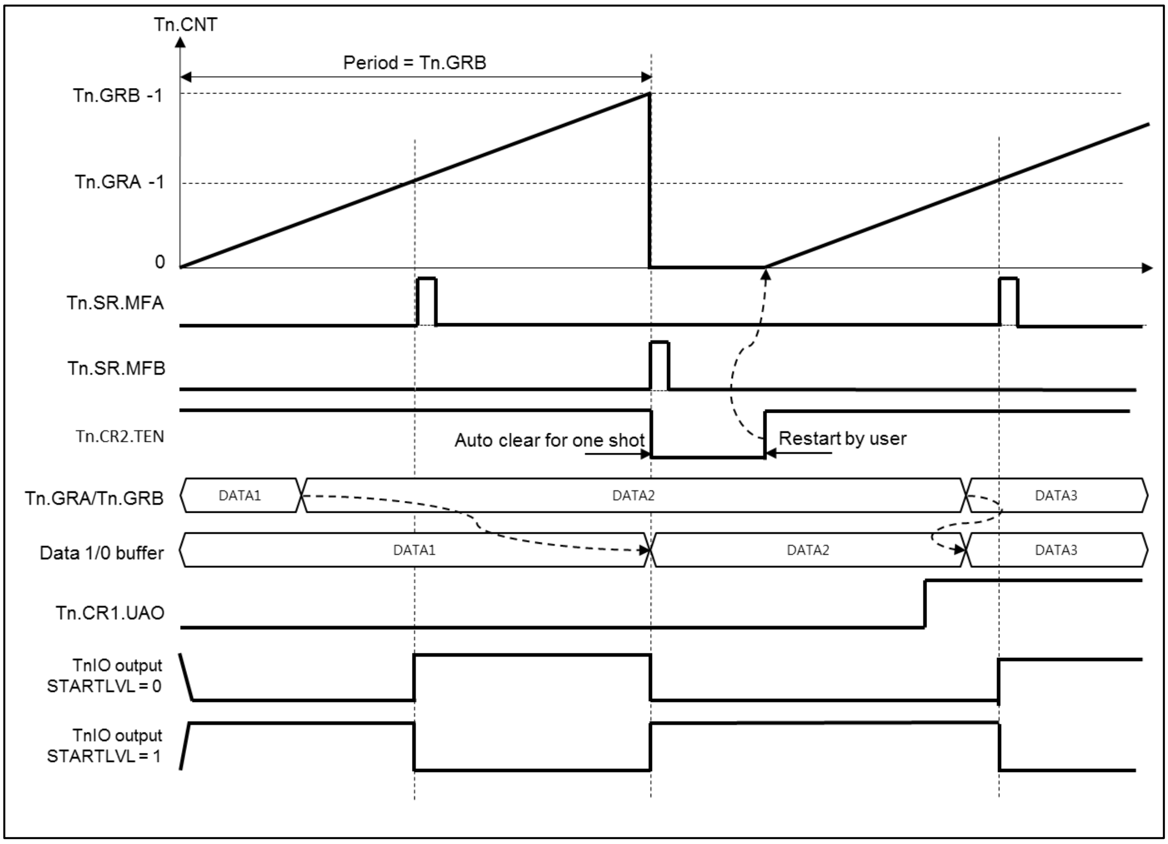


Figure 8.4 One shot mode operation

The priod of one shot count can be calculated as below equation.

The period = TMCLK Period * Tn.GRB value.
Match A interrupt time = TMCLK Period * Tn.GRA value.

If Tn.GRB = 0, the timer can not be started even TnCR2.TEN is “1”. Because the period is “0”.

The value in Tn.GRA and Tn.GRB is loaded into internal compare data buffer 0 and 1 when the loading condition is occurred. In this mode with Tn.CR2.TCLR write operation will load the data buffer and the next GRB match event will load the data buffer.

TnIO output signal format is same as pwm mode. Tn.GRB value defines the output pulse period and Tn.GRA value defines the pulse width of one shot pulse.

8.4.4 PWM Timer output examples

Figure 8.5 shows the timing diagram pwm output mode. Tn.GRB value decides the pwm pulse period. One more compare point is provided with Tn.GRA register value which defines pulse width of pwm output.

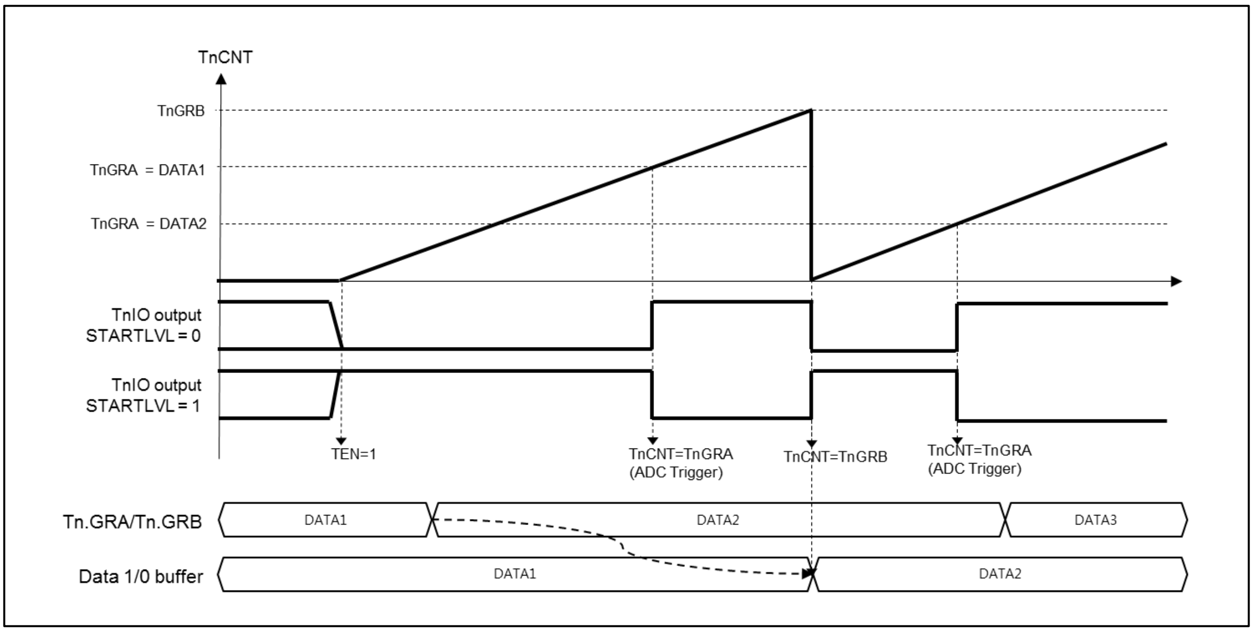


Figure 8.5 PWM Output operation

The priod of PWM pulse can be calculated as below equation.

The period = TMCLK Period * Tn.GRB value.
Match A interrupt time = TMCLK Period * Tn.GRA value.

If Tn.GRB = 0, the timer can not be started even TnCR2.TEN is “1”. Because the period is “0”.

The value in Tn.GRA and Tn.GRB is loaded into internal compare data buffer 0 and 1 when the loading condition is occurred. In this mode, Tn.CR2.TCLR write operation will load the data buffer and the next GRB match event will load the data buffer.

TnIO output signal generates PWM pulse. Tn.GRB value defines the output pulse period and Tn.GRA value defines the pulse width of one shot pulse.The active level of PWM pulse can be control by Tn.CR1.STARTLVL bit value.

ADC Tringger generation is available at Match A interrupt time.

8.4.5 Capture mode

Figure 8.6 shows the timing diagram in capture mode operation. TnIO input signal is used for capture pulse. Both of rising and falling edge can capture the counter valued in each capture coditions.

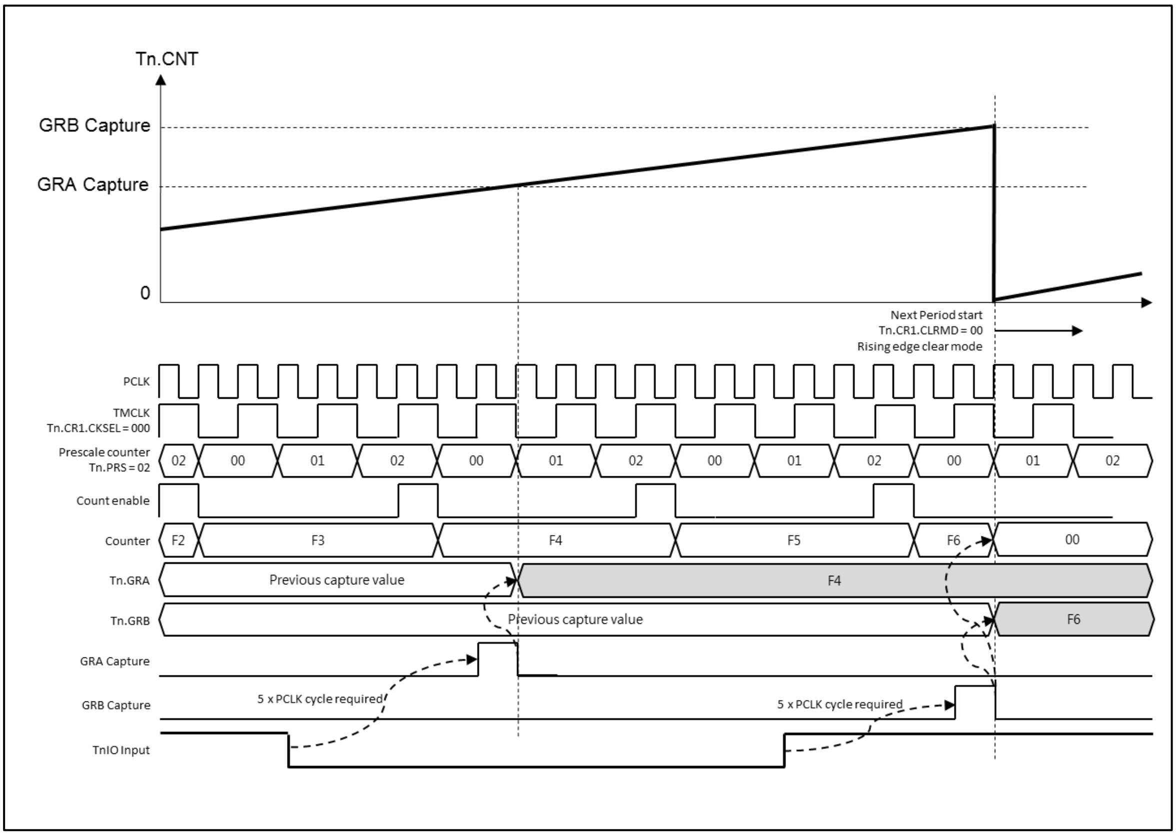


Figure 8.6 Capture mode operation

5 PCLK clock cycle is required internally. So acture capture point is after 5 PCLK clock cycles from rising or falling edge of TnIO input signal.

Internal counter can be cleared in various mode. TnCR1.CLRMD field controls the counter clear mode. Rising edge clear mode, Falling edge clear mode, Both edge clear mode and none clear mode are supported.

Figure 8.8 case is rising edge clear mode.

8.4.6 ADC trigger fucntion

Timer module can generate ADC start trigger signals. One timer can be one trigger source of ADC block. Trigger source control is done by ADC control register.

Figure 8.9 shows ADC trigger function.

The conversion rate must be shorter than timer period. If it is not a case, overrun situation can be happened. ADC acknowledge is not required, because trigger signal will be cleared automatically after 3 PCLK clock pulses.

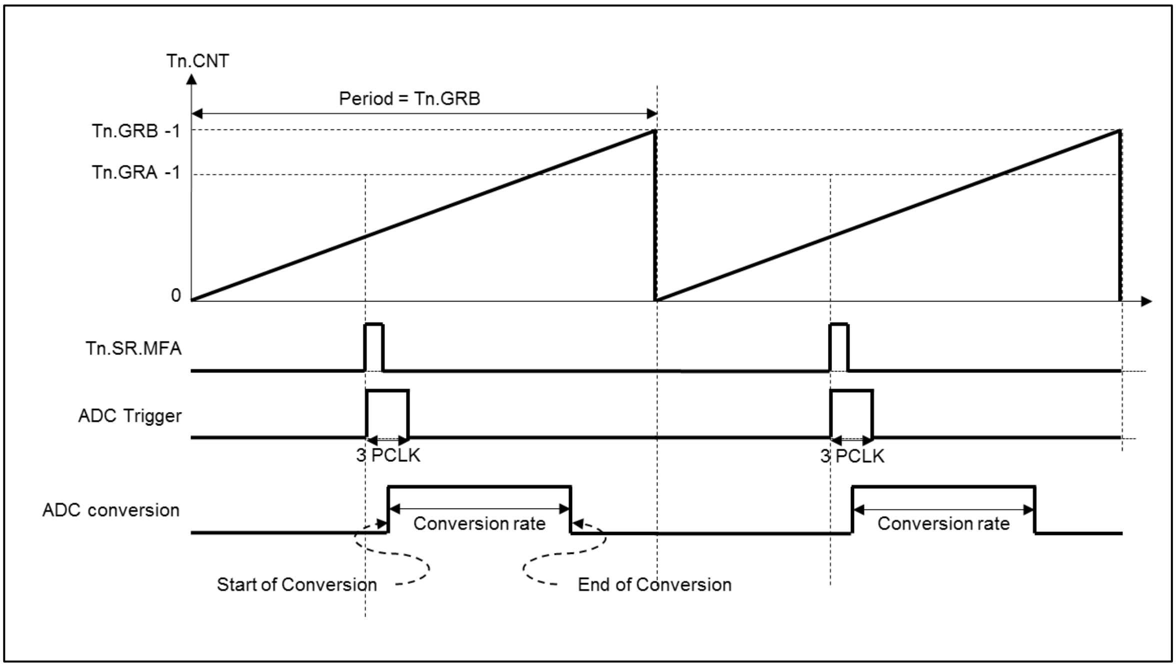


Figure 8.7 ADC trigger function timing diagram

CHAPTER 9. UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)

9.1 OVERVIEW

4-Channel UART (Universal Asynchronous Receiver/Transmitter) modules are provided. Dedicated DMA support to data transfer between memory buffer and transmit or receive buffer of UART block.

UART operation status including error status can be read from status register. The prescaler which generates proper baud rate, is exist for each UART channel. The prescaler can divide the UART clock source which is PCLK/2, from 1 to 65535. And baud rate generation is by clock which internally divided by 16 of the prescaled clock and 8-bit precision clock tuning function.

Programmable interrupt generation function will help to control the communication via UART channel

- Compatible with 16450
- Support DMA transfer
- Standard asynchronous control bit (start, stop, and parity) configurable
- Programmable 16-bit fractional baud generator
- Programmable serial communication
  - 5-, 6-, 7- or 8- bit data transfer
  - Even, odd, or no-parity bit insertion and detection
  - 1-, 1.5- or 2-stop bit-insertion and detection
- 16-bit baud rate generation with 8-bit fraction control
- Hardware inter-frame delay function
- Stop bit error detection
- Detail status register
- Loop-back control

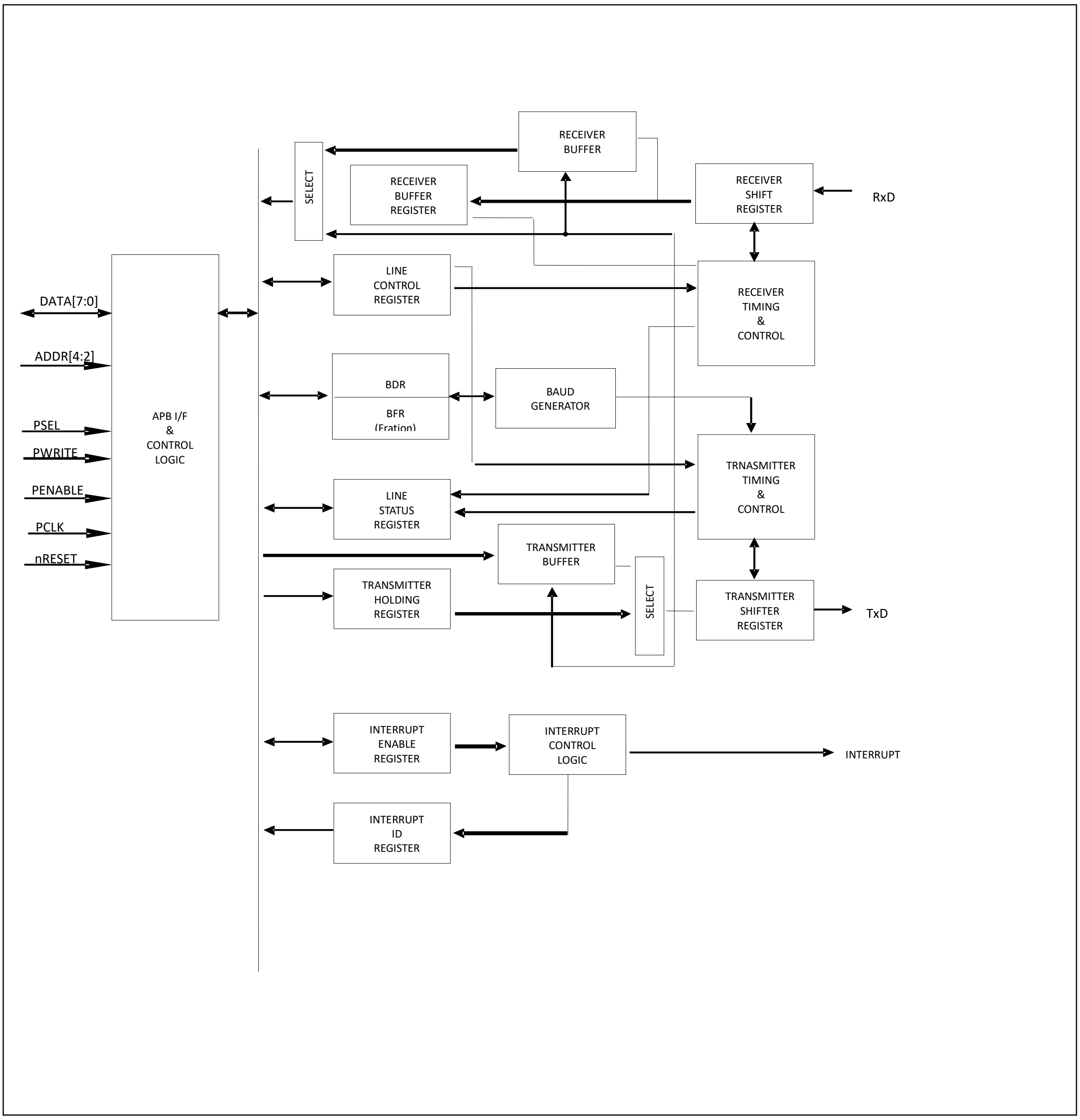


Figure 9.1. Block diagram

9.2 Pin description

Table 9.1. External signal

PIN NAME	TYPE	DESCRIPTION
TXD0	O	UART Channel 0 transmit output
RXD0	I	UART Channel 0 receive input
TXD1	O	UART Channel 1 transmit output
RXD1	I	UART Channel 1 receive input
TXD2	O	UART Channel 2 transmit output
RXD2	I	UART Channel 2 receive input
TXD3	O	UART Channel 3 transmit output
RXD3	I	UART Channel 3 receive input

9.3 REGISTERS

The base Address of UART is 0x4000_8000 and register map is described in Table9.2 and 9.3.

Table 9.2. Base address of each port

NAME	BASE ADDRESS
UART 0	0x4000_8000
UART 1	0x4000_8100
UART 2	0x4000_8200
UART 3	0x4000_8300

Table9.3. UART Register Map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
Un.RBR	0x00	R	Receive data buffer register	0x00
Un.THR	0x00	W	Transmit data hold register	0x00
Un.IER	0x04	RW	Interrupt enable register	0x00
Un.IIR	0x08	R	Interrupt ID register	0x01
Un.LCR	0x0C	RW	Line control register	0x00
Un.DCR	0x10	RW	Data Control Register	0x00
Un.LSR	0x14	R	Line status register	0x60
Un.BDR	0x20	RW	Baud rate Divisor Latch Register	0x0000
Un.BFR	0x24	RW	Baud rate Fractional Counter Value	0x00
Un.IDTR	0x30	RW	Inter-frame Delay Time Register	0x00

9.3.1 UnRBR Receive Buffer Register

UART Receive Buffer Register is 8-bit Read-Only register

U0.RBR=0x4000_8000, U1.RBR=0x4000_8100
U2.RBR=0x4000_8200, U3.RBR=0x4000_8300

7	6	5	4	3	2	1	0
RBR							
-							
RO							

7 0	RBR	Receive Buffer Register

9.3.2 Un.THR Transmit Data Hold Register

UART Transmit Data Hold Register is 8-bit Write-Only register

U0.THR=0x4000_8000, U1.THR=0x4000_8100
U2.THR=0x4000_8200, U3.THR=0x4000_8300

7	6	5	4	3	2	1	0
THR							
-							
WO							

7 0	THR	Transmit Data Hold Register

9.3.3 Un.IER UART Interrupt Enable Register

UART Interrupt Enable Register is 8-bit register.

U0.IER=0x4000_8004, U1.IER=0x4000_8104
U2.IER=0x4000_8204, U3.IER=0x4000_8304

7	6	5	4	3	2	1	0
-	-	DTXIEN	DRXIEN	-	RLSIE	THREIE	DRIE
0	0	0	0	0	0	0	0
		RW	RW		RW	RW	RW

5	DTXIEN	DMA transmit done interrupt enable	
		0	DMA transmit done interrupt is disabled
		1	DMA transmit done interrupt is enabled
4	DRXIEN	DMA receive done interrupt enable	
		0	DMA receive done interrupt is disabled
		1	DMA receive done interrupt is enabled
2	RLSIE	Receiver line status interrupt enable	
		0	Receive line status interrupt is disabled
		1	Receive line status interrupt is enabled
1	THREIE	Transmit holding register empty interrupt enable	
		0	Transmit holding register empty interrupt is disabled
		1	Transmit holding register empty interrupt is enabled
0	DRIE	Data receive interrupt enable	
		0	Data receive interrupt is disabled
		1	Data receive interrupt is enabled

9.3.4 Un.IIR UART Interrupt ID Register

UART Interrupt ID Register is 8-bit register.

U0.IIR=0x4000_8008, U1.IIR=0x4000_8108
U2.IIR=0x4000_8208, U3.IIR=0x4000_8308

7	6	5	4	3	2	1	0
				IID			IPEN
0	0	0	0	000			0
				R			R

3 1	IID	Interrupt source ID See interrupt source ID table	
0	IPEN	Interrupt pending bit	
		0	Interrupt is pending
		1	No interrupt is pending.

The UART supports 3-priority interrupt generation and interrupt source ID register shows one interrupt source which has highest priority among pending interrupts. The priority is defined as below.

- Receive line status interrupt
- Receive data ready interrupt
- Transmit hold register empty interrupt
- Tx/Rx DMA complete interrupts

Table9.4. Interrupt ID and control

Priority	DMA	IID		IPEN	Interrupt sources		
	Bit 3	Bit 2	Bit 1	Bit 0	Interrupt	Interrupt condition	Interrupt clear
-	0	0	0	1	None	-	-
Highest 1	0	1	1	0	Receiver Line Status	Overrun, Parity, Framing or Break Error	Read LSR register
2	0	1	0	0	Receiver Data Available	Receive data is available.	Read receive register or read IIR register
3	0	0	1	0	Transmitter Holding Register Empty	Transmit buffer empty	Write transmit hold register or read IIR register
4	1	1	0	0	Rx DMA done	Rx DMA completed.	Read IIR register
5	1	0	1	0	Tx DMA done	Tx DMA completed.	Read IIR register

9.3.5 Un.LCR UART Line Control Register

UART Line Control Register is 8-bit register.

U0.LCR=0x4000_800C, U1.LCR=0x4000_810C
U2.LCR=0x4000_820C, U3.LCR=0x4000_830C

7	6	5	4	3	2	1	0
	BREAK	STICKP	PARITY	PEN	STOPBIT	DLEN	
0	0	0	0	0	0	0	0
	RW	RW	RW	RW	RW	RW	RW

6	BREAK	When this bit is set, TxD pin will be driven at low state in order to notice the alert to the receiver.	
		0	Normal transfer mode
		1	Break transmit mode
5	STICKP	Force parity and it will be effective when PEN bit is set. See Table9.5	
		0	Parity stuck is disabled
		1	Parity stuck is enabled
4	PARITY	Parity mode selection bit and stuck parity select bit	
		0	Odd parity mode
		1	Even parity mode
3	PEN	Parity bit transfer enable	
		0	The parity bit disabled
		1	The parity bit enabled
2	STOPBIT	The number of stop bit followed by data bits.	
		0	1 stop bit
		1	1.5 / 2 stop bit In case of 5 bit data case, 1.5 stop bit is added. In case of 6,7 or 8 bit data, 2 stop bit is added
1 0	DLEN	The data length in one transfer word.	
		00	5 bit data
		01	6 bit data
		10	7 bit data
		11	8 bit data

Parity bit will be generated according to bit 3,4,5 of UnLCR register. The table shows the variation of parity bit generation.

Table9.5. Variation of parity bit generation

STICKP	PARITY	PEN	Parity
X	X	0	No Parity
0	0	1	Odd Parity
0	1	1	Even Parity
1	0	1	Force parity as “1”
1	1	1	Force parity as “0”

9.3.6 Un.DCR UART Data Control Register

UART Data Control Register is 8-bit register.

U0.DCR=0x4000_8010, U1.DCR=0x4000_8110
U2.DCR=0x4000_8210, U3.DCR=0x4000_8310

7	6	5	4	3	2	1	0
			LBON	RXINV	TXINV		
0	0	0	0	0	0	0	0
			RW	RW	RW		

4	LBON	Local loopback test mode enable	
		0	Normal mode
		1	Local loopback mode (TxD connected to RxD internally)
3	RXINV	Rx Data Inversion Selection	
		0	Normal RxData Input
		1	Inverted RxData Input
2	TXINV	Tx Data Inversion Selection	
		0	Normal TxData Output
		1	Inverted TxData Output

9.3.7 Un.LSR UART Line Status Register

UART Line Status Register is 8-bit register.

U0.LSR=0x4000_8014, U1.LSR=0x4000_8114
U2.LSR=0x4000_8214, U3.LSR=0x4000_8314

7	6	5	4	3	2	1	0
-	TEMT	THRE	BI	FE	PE	OE	DR
0	1	1	0	0	0	0	0
	R	R	R	R	R	R	R

6	TEMT	Transmit empty.	
		0	Transmit register has the data is now transferring
		1	Transmit register is empty.
5	THRE	Transmit holding empty.	
		0	Transmit holding register is not empty.
		1	Transmit holding register empty
4	BI	Break condition indication bit	
		0	Normal status
		1	Break condition is detected
3	FE	Frame Error.	
		0	No framing error.
		1	Framing error. The receive character did not have a valid stop bit
2	PE	Parity Error	
		0	No parity error
		1	Parity error. The receive character does not have correct parity information.
1	OE	Overrun error	
		0	No overrun error
		1	Overrun error. Additional data arrives while the RHR is full
0	DR	Data received	
		0	No data in receive holding register.
		1	Data has been received and is saved in the receive holding register

This register provides the status of data transfers between transmitter and receiver. User can get the line status information from this register and can handle the next process. Bit 1,2,3,4 will arise the line status interrupt when RLSIE bit in Un.IEN register is set. Other bits can generate its interrupt when it's interrupt enable bit in UnIEN register is set.

9.3.8 Un.BDR Baud rate Divisor Latch Register

UART Baud rate Divisor Latch Register is 16-bit register.

U0.BDR=0x4000_8020, U1.BDR=0x4000_8120
U2.BDR=0x4000_8220, U3.BDR=0x4000_8320

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BDR															
0x0000															
RW															

15 0	BDR	Baud rate Divider latch value

To establish the communication with UART channel, the baud rate should be set properly. The programmable baud rate generate is provided to give from 1 to 65535 divider number. The 16 bit divider register (UnBDR) should be written for expected baud rate.

Baud rate calculation formula is below.

$$\mathrm{BDR} = \frac{PCLK\ /\ 2}{16 \times\ BaudRate}$$

In case of 72 MHz PCLK speed, the divider value and error rate is described in table

Table9.6. Example of baud rate calculation

PCLK=72 MHz		
Baud rate	**Divider (BDR)**	**Error (%)**
1200	1875	0.00%
2400	937	0.05%
4800	468	0.16%
9600	234	0.16%
19200	117	0.16%
38400	58	1.02%
57600	39	0.16%
115200	19	2.79%

9.3.9 Un.BFR Baud rate Fraction Counter Register

Baud rate Fraction Counter Register is 8-bit register.

U0.BFR=0x4000_8024, U1.BFR=0x4000_8124
U2.BFR=0x4000_8224, U3.BFR=0x4000_8324

7	6	5	4	3	2	1	0
BFR							
0x00							
RW							

7 0	BFR	Fractions counter value.	
		0	Fraction counter is disabled
		N	Fraction counter enabled. Fraction compensation mode is operating. Fraction counter is incremented by FCNT.

Table9.7. Example of baud rate calculation with BFR

PCLK=72 MHz			
Baud rate	**Divider (BDR)**	**FCNT (BFR)**	**Error (%)**
1200	1875	0	0.0%
2400	937	128	0.0%
4800	468	192	0.0%
9600	234	96	0.0%
19200	117	48	0.0%
38400	58	152	0.0%
57600	39	16	0.0%
115200	19	136	0.0%

$$\mathrm{FCNT} = \mathrm{Float} * 256$$

8-bit fractional counter will count up by FCNT value every (baud rate)/16 period and whenever fractional counter overflow is happen, the divisor value will increment by 1. So this period will be compensated. Then next period, the divisor value will return to original set value.

Ex) if 9600 bps,

$$\frac{PCLK\ /\ 2}{16 \times\ BaudRate} = \frac{72000000\ /\ 2}{16 \times\ 9600} = 234.375 \quad Divider = 234, Float = 0.375$$

$$\mathrm{FCNT} = \mathrm{Float} * 256 \ = 0.375 * 256 = 96$$

BDR = 234, BFR = 96

9.3.10 Un.IDTR Inter-frame Delay Time Register

UART Inter-frame Time Register is 8-bit register.

Dummy delay can be inserted between 2 continuous transmits.

U0.IDTR=0x4000_8030, U1.IDTR=0x4000_8130
U2.IDTR=0x4000_8230, U3.IDTR=0x4000_8330

7	6	5	4	3	2	1	0
-					WAITVAL		
0	0	0	0	0	000		
					RW		

2 0	WAITVAL	Wait time is decided by this value [unit: 1 bit time] $$\text{Wait Time} = \frac{WAITVAL}{BAUDRATE}$$

9.4 Functional Description

The UART module is compatible with 16450 UART. Additionally the dedicated DMA channels and fractional baud rate compensation logic are provided.

It doesn't have internal FIFO block. So data transfers will establish interactively or using DMA support. The DMA operation is described here.

2 DMA channels provided for each UART module, one channel is for TX transfer and the other one is for RX transfer. Each channel has a 32-bit memory address register and a 16bit transfer counter register.

Before DMA operation, DMA memory address register and transfer count register should be configured. For the RX operation, the memory address will be destination memory address and for the TX operation, the memory address will be source memory address.

The transfer counter register will store the number of transfer data. Whenever a single transfer done, the counter will decremented by 1. When the counter reaches zero, the DMA done flag will delivered to UART control block. If the interrupt is enabled, this flag will generate the interrupt.

9.4.1 Receiver Sampling Timing

The UARTs operates as following timing.

If the falling edge on the receive line, UART judges as the start bit. From the start timing, UART oversamples 16 times of 1-bit and detect the bit value at the 7th sample of 16 samples.

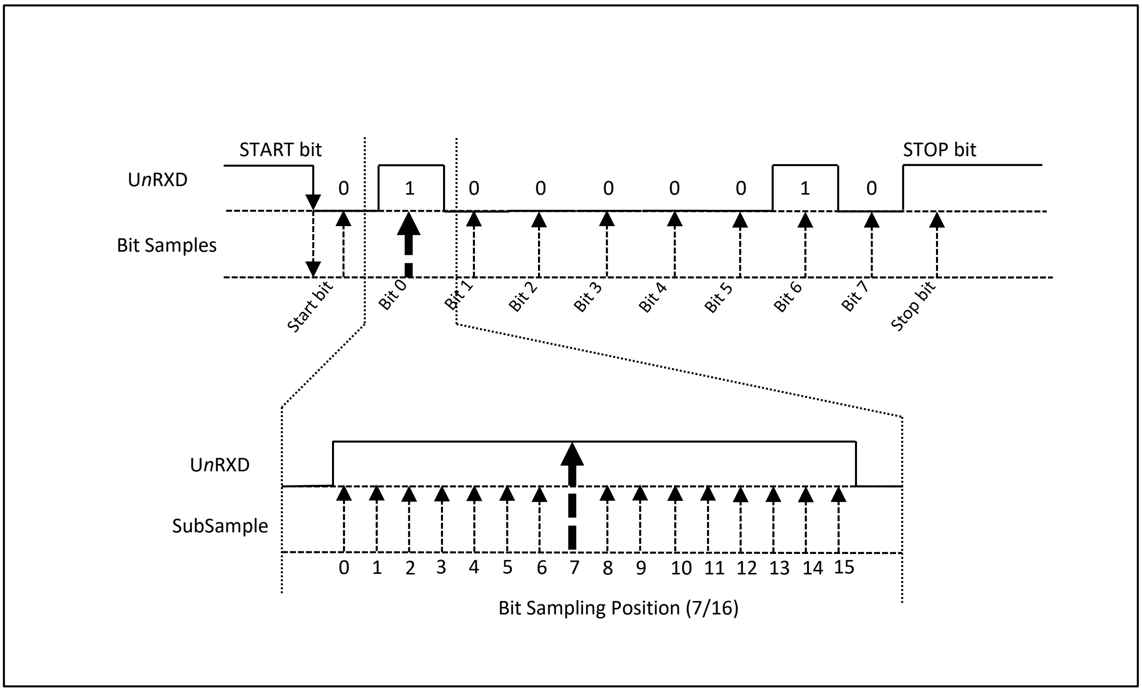


Figure 9.2 The Sampling Timing of UART Receiver

- It is recommended to enable debounce settings in the PCU block to reinforce the immunity of external glitch noise.

9.4.2 Transmitter

The transmitter has data transmit function. The start bit, data bits, optional parity bit and stop bit are serially shifted, least significant bit first.

The number of data bit is selected in the DLAN[1:0] filed in Un.LCR register.

The parity bit is set according to the PARITY and PEN bit filed in Un.LCR register. If the parity type is even then the parity bit depends on the one bit sum of all data bits. For odd parity, the parity bit is the inverted sum of all data bits.

The number of stop bits is selected in the STOPBIT filed in Un.LCR register.

The example of transmit data format is below.

1-bit and detect the bit value at the 7th sample of 16 samples.

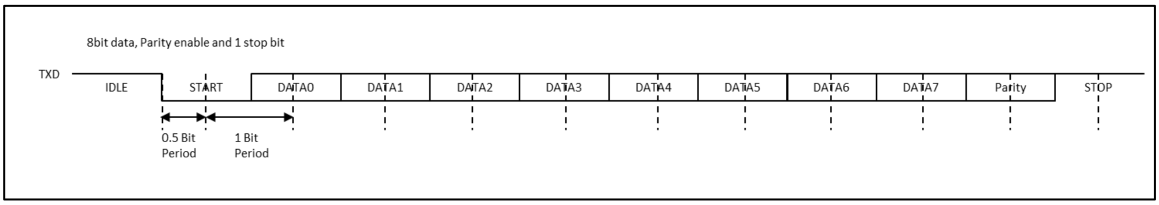


Figure 9.3 Transmit data format example

9.4.3 Inter-frame delay transmittion

The inter-frame delay function allows the transmitter to insert an idel state on the TXD line between 2 characters. The width of the idel state is defined in WAITVAL field in Un.IDTR register. When this field is set 0, no time-delay is generated. Otherwise, the transmitter holds a high level on TXD after each transmitted character during the number of bit periods defined in WATIVAL field.

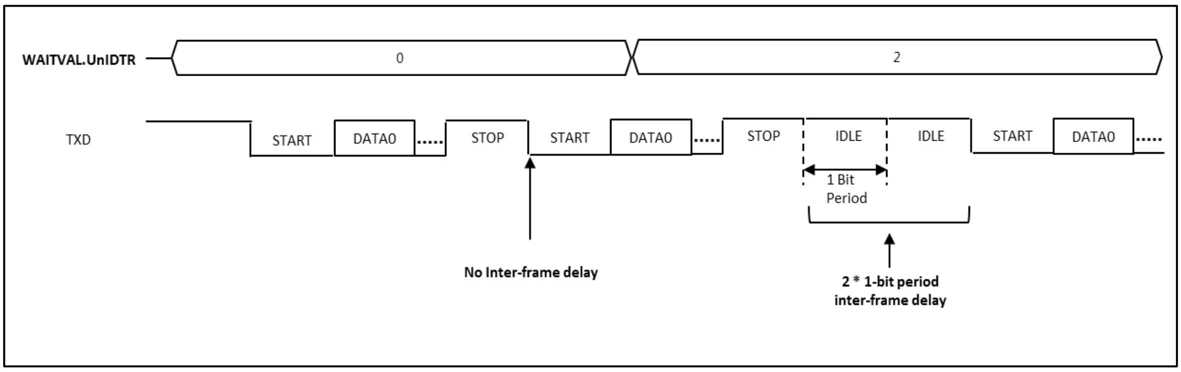


Figure 9.4 Transmit data format example

9.4.4 Transmit Interrupt

The transmit operation makes some kind of interrupt flags. When transmitter holding register is empty, the THRE interrupt flag will be set. Whe transmitter shifter register is empty, the TXE interrupt flag will be set. User can select which interrupt timing is best for the application.

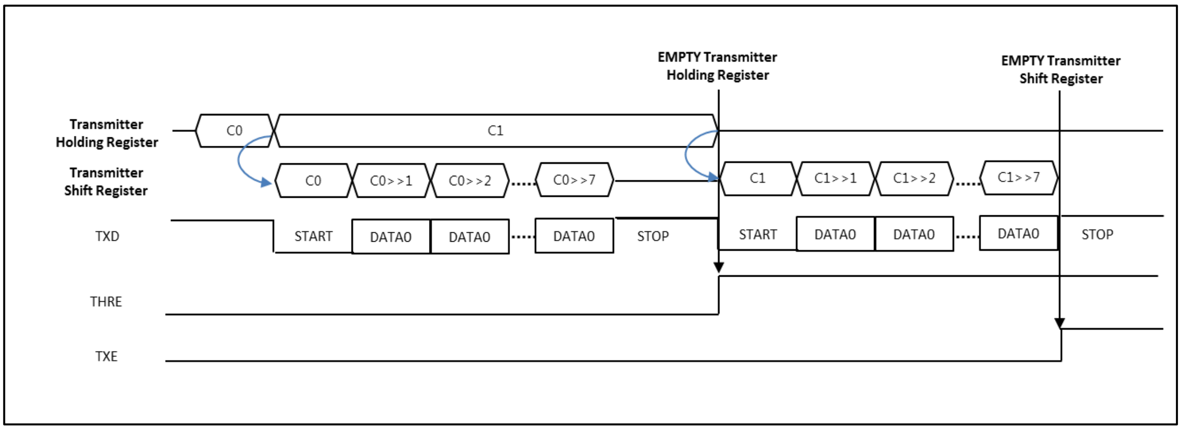


Figure 9.5 Transmit data format example

9.4.5 DMA Transfers

The UART support DMA interface function. It is optionally provided depends on the device. The start memory address for transfer data and the length of transfer data are programmd in the registers in DMA block.

The end of transfer is notified related transfer done flag.

The transmit with DMA operation will invoke the DMA TX done flag DTX.UnIIR and will set DMA TX done interrupt ID when all the transmit data are written to transmit holding register. 2 transmit data are remained in registers in UART block after DMA transfer done interrupt.

The receive with DMA operation will invoke the DMA RX done flag RXT.UnIIR and will set DMA RX done interrupt ID when all the receive data are written to the destination memory. So, UART RXD signal is already IDLE state when the DMA RX done interrupt is issued.

CHAPTER 10. SERIAL PERIPHERAL INTERFACE (SPI)

10.1 OVERVIEW

2-Channel serial Interface are provided for synchronous serial communications with external peripherals. SPI block support both of master and slave mode. 4 signals will be used for SPI communication – SS, SCK, MOSI, and MISO.

- Master or Slave operation.
- Programmable clock polarity and phase.
- 8,9,16,17-bit wide transmit/receive register.
- 8,9,16,17-bit wide data frame.
- Loop-back mode.
- Programmable start, burst, and stop delay time.
- DMA transfer operation.

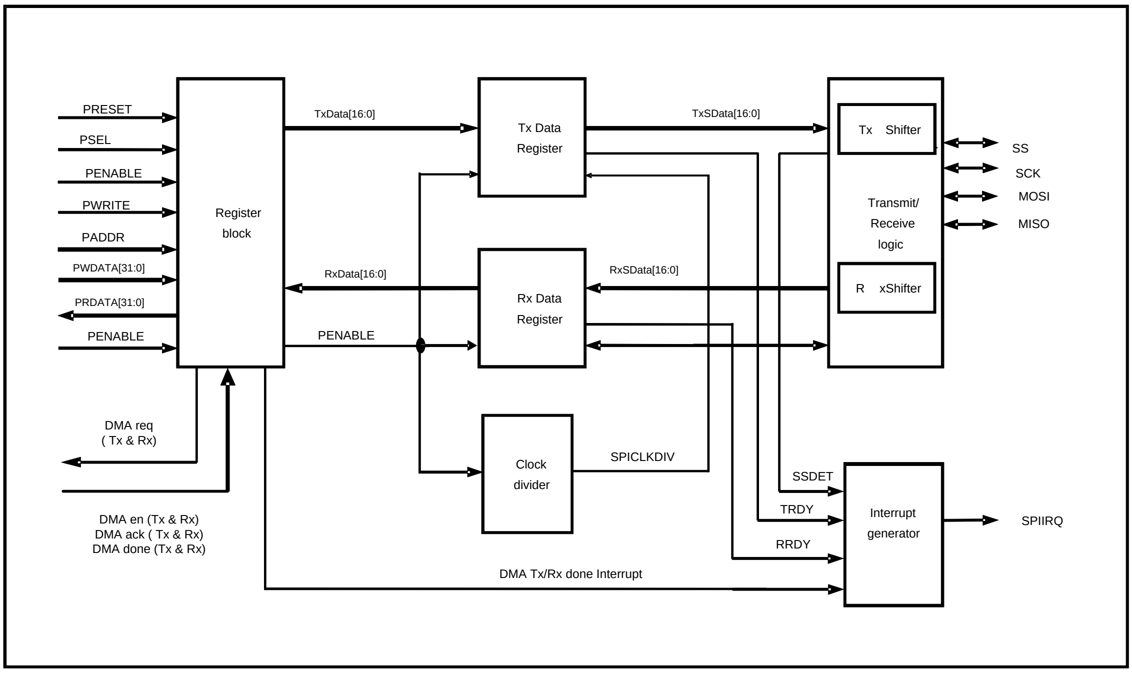


Figure 10.1. SPI block diagram

10.2 PIN DESCRIPTION

Table10.1. External Pins

PIN NAME	TYPE	DESCRIPTION
SS0	I/O	SPI0 Slave select (Master output, Slave input)
SCK0	I/O	SPI0 Serial clock (Master output, Slave input)
MOSI0	I/O	SPI0 Serial data (Master output, Slave input)
MISO0	I/O	SPI0 Serial data (Master input, Slave output)
SS1	I/O	SPI1 Slave select (Master output, Slave input)
SCK1	I/O	SPI1 Serial clock (Master output, Slave input)
MOSI1	I/O	SPI1 Serial data (Master output, Slave input)
MISO1	I/O	SPI1 Serial data (Master input, Slave output)

10.3 REGISTERS

The base address of SPI is 0x4000_9000 and register map is described in Table10.2 and 10.3.

Table10.2. SPI Base Address

NAME	BASE ADDRESS
SPI0	0x4000_9000
SPI1	0x4000_9100

Table10.3. SPI Register Map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
SP*n*.TDR	0x--00	W	SPI n Transmit Data Register	-
SP*n*.RDR	0x--00	R	SPI n Receive Data Register	0x000000
SP*n*.CR	0x--04	RW	SPI n Control Register	0x001020
SP*n*.SR	0x--08	RW	SPI n Status Register	0x000006
SP*n*.BR	0x--0C	RW	SPI n Baud rate Register	0x0000FF
SP*n*.EN	0x--10	RW	SPI n Enable register	0x000000
SPn.LR	0x--14	RW	SPI n delay Length Register	0x010101

10.3.1 SP*n*.CR SPI n Control Register

SPn.CR is a 20-bits read/write register and can be set to configure SPI operation mode.

SP0.CR=0x4000_9004, SP1.CR=0x4000_9104

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
											TXBC	RXBC	TXDIE	RXDIE	SSCIE	TXIE	RXIE	SSMOD	SSOUT	LBE	SSMASK	SSMO	SSPOL			MS	MSBF	CPHA	CPOL	BITSZ	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	00	
											W	W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			RW	RW	RW	RW	RW	

Bit	Name	Description
20	**TXBC**	Tx buffer clear bit.
		0 No action
		1 Clear Tx buffer
19	**RXBC**	Rx buffer clear bit
		0 No action
		1 Clear Rx buffer
18	**TXDIE**	DMA Tx Done Interrupt Enable bit.
		0 DMA Tx Done Interrupt is disabled.
		1 DMA Tx Done Interrupt is enabled.
17	**RXDIE**	DMA Rx Done Interrupt Enable bit.
		0 DMA Rx Done Interrupt is disabled.
		1 DMA Rx Done Interrupt is enabled.
16	**SSCIE**	SS Edge Change Interrupt Enable bit.
		0 nSS interrupt is disabled.
		1 nSS interrupt is enabled for both edges (L→H, H→L)
15	**TXIE**	Transmit Interrupt Enable bit.
		0 Transmit Interrupt is disabled.
		1 Transmit Interrupt is enabled.
14	**RXIE**	Receive Interrupt Enable bit..
		0 Receive Interrupt is disabled.
		1 Receive Interrupt is enabled.
13	**SSMOD**	SS Auto/Manual output select bit in master mode.
		0 SS output is not set by SSOUT (SPnCR[12]). - SS signal is in normal operation mode.
		1 SS output signal is set by SSOUT.
12	**SSOUT**	SS output signal select bit in master mode.
		0 SS output is 'L.'
		1 SS output is 'H'.
11	**LBE**	Loop-back mode select bit in master mode.
		0 Loop-back mode is disabled.
		1 Loop-back mode is enabled.
10	**SSMASK**	SS signal masking bit in slave mode.
		0 SS signal masking is disabled. - Receive data when SS signal is active.
		1 SS signal masking is enabled. - Receive data at SCLK edges. SS signal is ignored.
9	**SSMO**	SS output signal select bit.
		0 SS output signal is disabled.
		1 SS output signal is enabled.
8	**SSPOL**	SS signal Polarity select bit.
		0 SS signal is Active-Low.
		1 SS signal is Active-High.

7 6		Reserved	
5	**MS**	Master/Slave select bit.	
		0	SPI is in Slave mode.
		1	SPI is in Master mode.
4	**MSBF**	MSB/LSB Transmit select bit.	
		0	LSB is transferred first.
		1	MSB is transferred first.
3	**CPHA**	SPI Clock Phase bit.	
		0	Sampling of data occurs at odd edges (1,3,5,…,15).
		1	Sampling of data occurs at even edges (2,4,6,…,16).
2	**CPOL**	SPI Clock Polarity bit.	
		0	Active-high clocks selected.
		1	Active-low clocks selected.
1	**BITSZ**	Transmit/Receive Data Bits select bit.	
		00	8 bits
		01	9 bits
		10	16 bits
0		11	17 bits

CPOL=0, CPHA=0 : data sampling at rising edge, data changing at falling edge

CPOL=0, CPHA=1 : data sampling at falling edge, data changing at rising edge

CPOL=1, CPHA=0 : data sampling at falling edge, data changing at rising edge

CPOL=1, CPHA=1 : data sampling at rising edge, data changing at falling edge

10.3.2 SP*n*.SR SPI n Status Register

SPn.SR is a 10-bits read/write register. It contains the status of SPI interface.

SP0.SR=0x4000_9008, SP1.SR=0x4000_9108

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						TXDMAF	RXDMAF		SSDET	SSON	OVRF	UDRF	TXIDLE	TRDY	RRDY
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
						RC1	RC1		RC1	RC1	RC1	RC1	R	R	R

9	TXDMAF	DMA Transmit Operation Complete flag. (DMA to SPI)
		0 DMA Transmit Op is working or is disabled.
		1 DMA Transmit Op is done.
8	RXDMAF	DMA Receive Operation Complete flag. (SPI to DMA)
		0 DMA Receive Operation is working or is disabled.
		1 DMA Transmit Op is done.
7		Reserved
6	SSDET	The rising or falling edge of SS signal Detect flag.
		0 SS edge is not detected.
		1 SS edge is detected. - The bit is cleared when it is written as “0”.
5	SSON	SS signal Status flag.
		0 SS signal is inactive.
		1 SS signal is active.
4	OVRF	Receive Overrun Error flag.
		0 Receive Overrun error is not detected.
		1 Receive Overrun error is detected. - This bit is cleared by writing or reading SPnRDR.
3	UDRF	Transmit Underrun Error flag.
		0 Transmit Underrun is not occurred.
		1 Transmit Underrun is occurred. - This bit is cleared by writing or reading SPnTDR.
2	TXIDLE	Transmit/Receive Operation flag.
		0 SPI is transmitting data
		1 SPI is in IDLE state.
1	TRDY	Transmit buffer Empty flag.
		0 Transmit buffer is busy.
		1 Transmit buffer is ready. - This bit is cleared by writing data to SPnTDR.
0	RRDY	Receive buffer Ready flag.
		0 Receive buffer has no data.
		1 Receive buffer has data. - This bit is cleared by reading data to SPnRDR.

10.3.3 SP*n*.TDR SPI n Transmit Data Register

SPn.TDR is a 17-bits read/write register. It contains serial transmit data.

SP0.TDR=0x4000_9000, SP1.TDR=0x4000_9100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															TDR																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x00000																
															RW																

16 0	**TDR**	Transmit Data Register

10.3.4 SP*n*.RDR SPI n Receive Data Register

SPn.RDR is a 17-bits read/write register. It contains serial receive data.

SP0.RDR=0x4000_9000, SP1.RDR=0x4000_9100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															RDR																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x00000																
															RW																

16 0	**RDR**	Receive Data Register

10.3.5 SP*n*.BR SPI n Baud Rate Register

SPn.BR is an16-bits read/write register. Baud rate can be set by writing the register.

SP0.BR=0x4000_900C, SP1.BR=0x4000_910C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BR															
0x00FF															
RW															

15 0	**BR**	Baud rate setting bits - Baud Rate = PCLK / (BR + 1). (BR must be bigger than “0”, BR >= 2)

10.3.6 SP*n*.EN SPI n Enable register

SPn.EN is a bit read/write register. It contains SPI enable bit.

SP0.EN=0x4000_9010, SP1.EN=0x4000_9110

7	6	5	4	3	2	1	0
							ENABLE
0	0	0	0	0	0	0	0
							RW

0	**ENABLE**	SPI Enable bit		
			0	SPI is disabled. - SPnSR is initialized by writing “0” to this bit but other registers aren’t initialized.
			1	SPI is enabled. - When this bit is written as “1”, the dummy data of transmit buffer will be shifted. To prevent this, write data to SPTDR before this bit is active.

10.3.7 SP*n*.LR SPI n delay Length Register

SPnLR is a 24-bits read/write register. It contains start, burst, and stop length value.

SP0LR=0x4000_9014, SP1LR=0x4000_9114

31	30	29	28	27	26	25	24	23–16	15–8	7–0
								SPL	BTL	STL
0	0	0	0	0	0	0	0	0x01	0x01	0x01
								RW	RW	RW

Bits	Name	Description
23 16	SPL	StoPLength value 0x01 ~ 0xFF : 1 ~ 255 SCLKs. (SPL >= 1)
15 8	BTL	BursTLength value 0x01 ~ 0xFF : 1 ~ 255 SCLKs. (BTL >= 1)
7 0	STL	STart Length value 0x01 ~ 0xFF : 1 ~ 255 SCLKs. (STL >= 1)

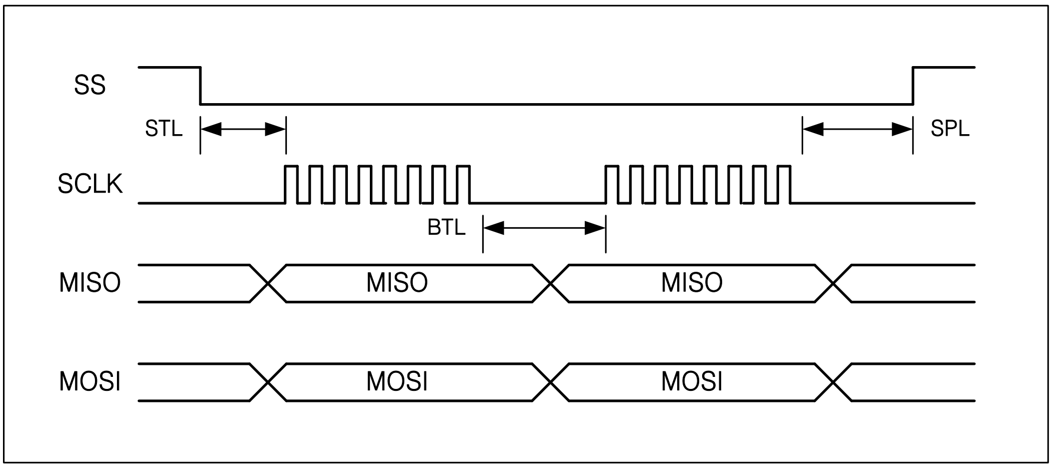


Figure14.2. SPI waveform (STL, BTL, and SPL)

10.4 FUNCTIONAL DESCRIPTION

SPI Transmit block and Receive block share Clock Gen Block but they are independent each other. Transmit block and Receive block have double buffers and SPI is available for back to back transfer operation.

10.4.1 SPI timing

The SPI has four modes of operation. These modes essentially control the way data is clocked in or out of an SPI device. The configuration is done by two bits in the SPI control register (SPnCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock. The clock phase (CPHA) control bit selects one of the two fundamentally different transfer formats. To ensure a proper communication between master and slave both devices have to run in the same mode. This can require a reconfiguration of the master to match the requirements of different peripheral slaves.

The clock polarity has no significant effect on the transfer format. Switching this bit causes the clock signal to be inverted (active high becomes active low and idle low becomes idle high). The settings of the clock phase, however, selects one of the two different transfer timings, which are described closer in the next two chapters. Since the MOSI and MISO lines of the master and the slave are directly connected to each other, the diagrams show the timing of both devices, master and slave. The nSS line is the slave select input of the slave. The nSS pin of the master is not shown in the diagrams. It has to be inactive by a high level on this pin (if configured as input pin) or by configuring it as an output pin.

The timing of a SPI transfer where CPHA is zero is shown in Figure 10.3 and 10.4. Two wave forms are shown for the SCK signal -one for CPOL equals zero and another for CPOL equals one.

When the SPI is configured as a slave, the transmission starts with the falling edge of the /SS line. This activates the SPI of the slave and the MSB of the byte stored in its data register (SPnTDR) is output on the MISO line. The actual transfer is started by a software write to the SPnTDR of the master. This causes the clock signal to be generated. In cases where the CPHA equals zero, the SCLK signal remains zero for the first half of the first SCLK cycle. This ensures that the data is stable on the input lines of both the master and the slave. The data on the input lines is read with the edge of the SCLK line from its inactive to its active. The edge of the SCLK line from its active to its inactive state (falling edge if CPOL equals zero and rising edge if CPOL equals one) causes the data to be shifted one bit further so that the next bit is output on the MOSI and MISO lines.

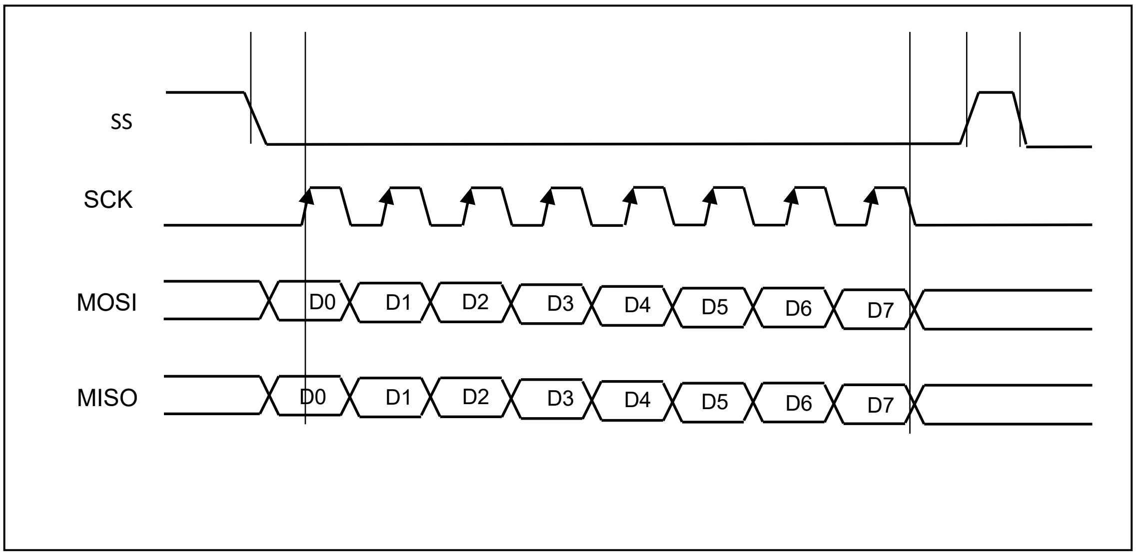


Figure10.3.SPI Transfer Timing 1/4 (CPHA=0, CPOL=0, MSBF=0)

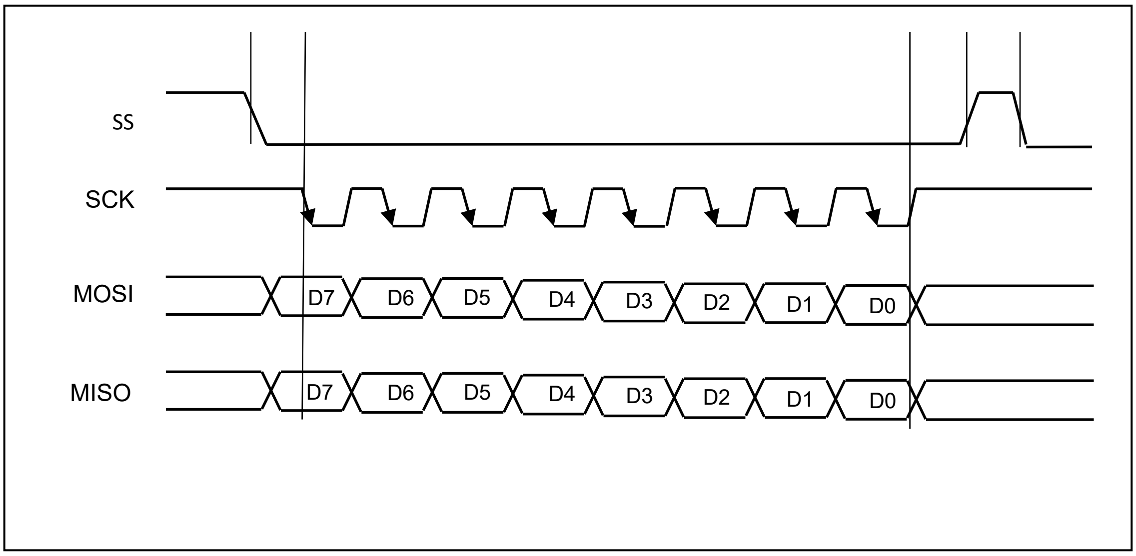


Figure10.4.SPI Transfer Timing 2/4 (CPHA=0, CPOL=1, MSBF=1)

The timing of a SPI transfer where CPHA is one is shown in Figure 10.5 and 10.6.Two wave forms are shown for the SCLK signal -one for CPOL equals zero and another for CPOL equals one.

Like in the previous cases the falling edge of the nSS lines selects and activates the slave. Compared to the previous cases, where CPHA equals zero, the transmission is not started and the MSB is not output by the slave at this stage. The actual transfer is started by a software write to the SPnTDR of the master what causes the clock signal to be generated. The first edge of the SCLK signal from its inactive to its active state (rising edge if CPOL equals zero and falling edge if CPOL equals one) causes both the master and the slave to output the MSB of the byte in the SPnTDR.

As shown in Figure 10.3 and 10.4, there is no delay of half a SCLK-cycle. The SCLK line changes its level immediately at the beginning of the first SCLK-cycle. The data on the input lines is read with the edge of the SCLK line from its active to its inactive state (falling edge if CPOL equals zero and rising edge if CPOL equals one). After eight clock pulses the transmission is completed.

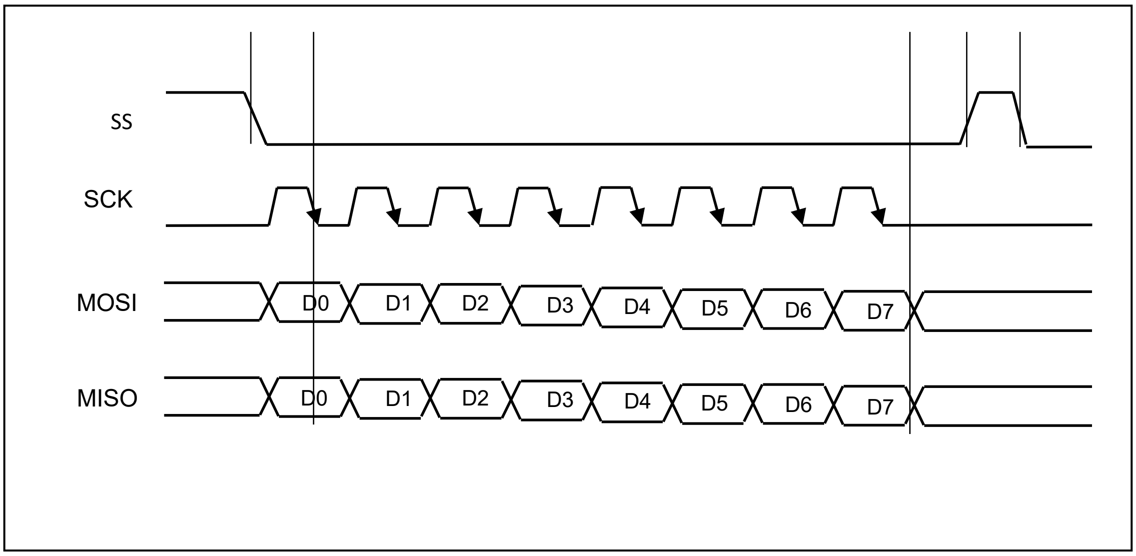


Figure10.5.SPI Transfer Timing 3/4 (CPHA=1, CPOL=0, MSBF=0)

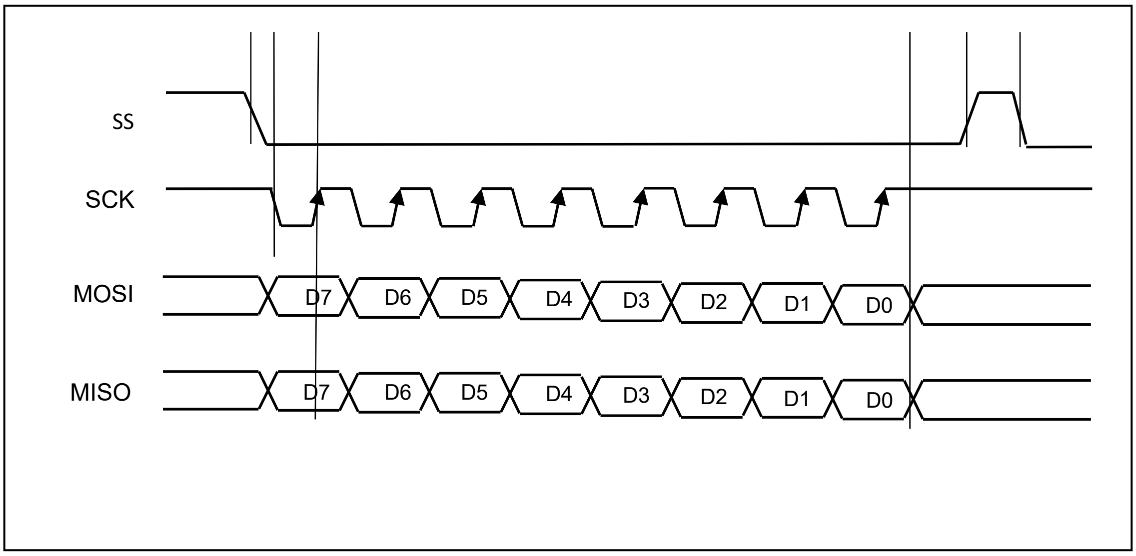


Figure10.6.SPI transfer timing 4/4 (CPHA=1, CPOL=1, MSBF=1)

10.4.2 DMA Handshake

SPI supports DMA handshaking operation. In order to operate DMA handshake, DMA registers should be set first. (See Chapter 6. DMA Controller). SPI0 has 2 channels of DMA, channel 8 for receiver and channel 9 for transmitter. SPI1 has channel 10 for receiver and channel 11 for transmitter. As Transmitter and Receiver are independent each other, SPI can operate the two channels at the same time.

After DMA channel for receiver is enabled and receive buffer is filled, SPI sends Rx request to DMA to empty the buffer and waits ACK signal from DMA. If Receive buffer is filled again after ACK signal, SPI sends Rx request. If DMA Rx DONE becomes high, RXDMAF (SPnSR[8]) goes “1” and an interrupt is serviced when RXDIE (SPnCR[17]) is set.

Likewise, if transmit buffer is empty after DMA channel for transmitter is enabled, SPI sends Tx request to DMA to fill the buffer and waits ACK signal from DMA. If transmit buffer is empty again after ACK signal, SPI sends Tx request. If DMA Tx DONE becomes high, TXDMAF(SPnSR[9]) goes “1” and an interrupt is serviced when TXDIE(SPnCR[18]) is set.

Slave transmitter sends dummy data at the first transfer (8~17 SCLKs) in DMA handshake mode.

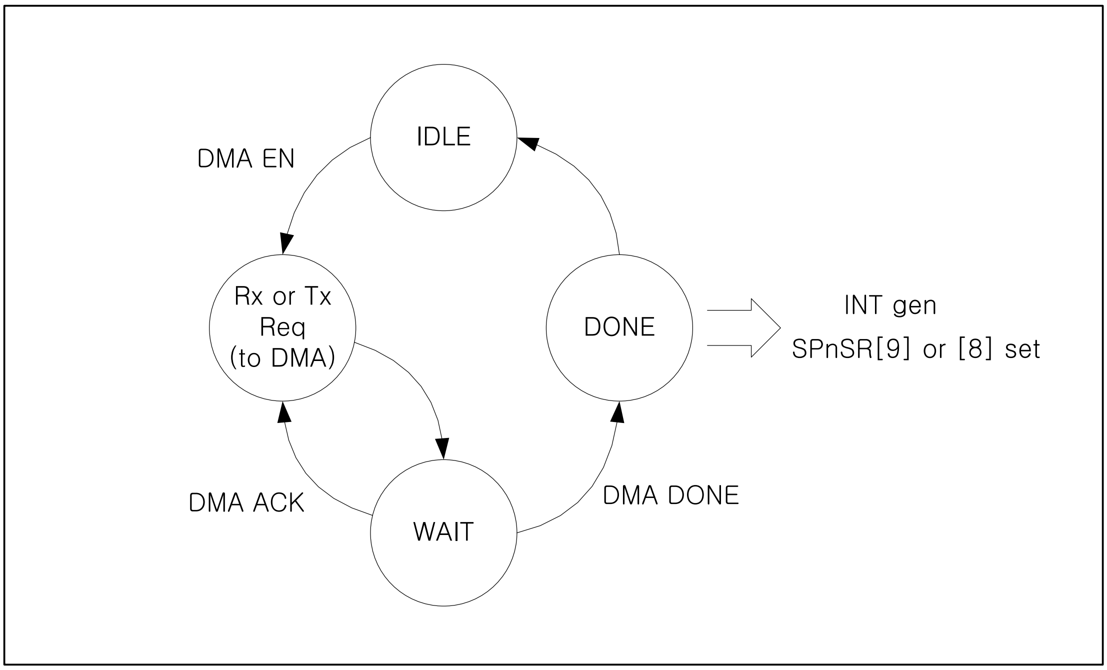


Figure10.7.DMA Handshake Flowchart

CHAPTER 11. I^2C Interface

11.1 OVERVIEW

I^2C(Inter-Integrated Circuit) bus serves as an interface between the microcontroller and the serial I^2C bus. It provides two wires, serial bus interface to a large number of popular devices and allows parallel-bus systems to communicate bidirectionally with the I^2C-bus.

- Master and slave operation
- Programmable communication speed
- Multi-master bus configuration
- 7-bit addressing mode
- Standard data rate of 100/400 kbps
- STOP signal generation and detection
- START signal generation
- ACK bit generation and detection

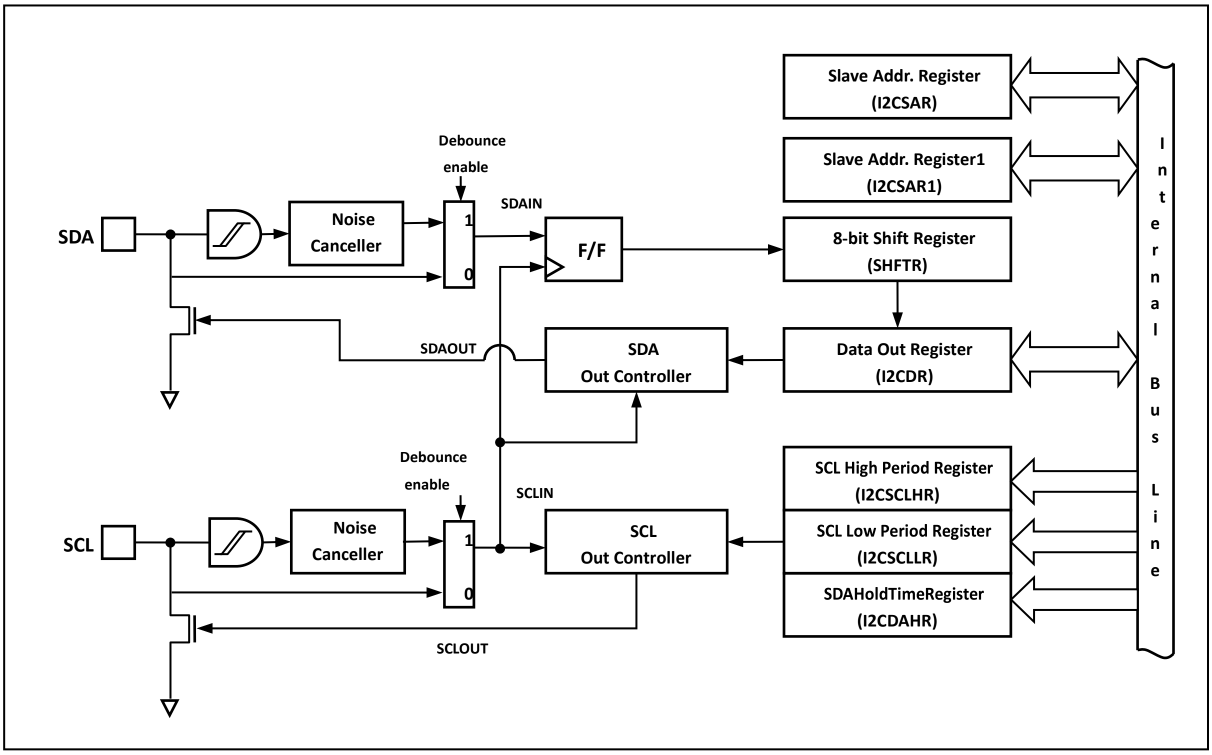


Figure11.1 I^2C Block diagram

11.2 PIN DESCRIPTION

Table11.1 I²C interface external pins

PIN NAME	TYPE	DESCRIPTION
SCL0	I/O	I²C channel 0 Serial clock bus line (open-drain)
SDA0	I/O	I²C channel 0 Serial data bus line (open-drain)
SCL1	I/O	I²C channel 1 Serial clock bus line (open-drain)
SDA1	I/O	I²C channel 1 Serial data bus line (open-drain)

11.3 REGISTERS

The base address of I²C0 is 0x4000_A000 and the base address of I²C1 is 0x4000_A100. The register map is described in Table11.2 and 11.3.

Table11.2.I²C interface base address

NAME	BASE ADDRESS
I²C0	0x4000_A000
I²C1	0x4000_A100

Table11.3.I²C register map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
IC0.DR	0xA000	RW	I²C0 Data Register	0xFF
IC0.SR	0xA008	R, RW	I²C0 Status Register	0x00
IC0.SAR	0xA00C	RW	I²C0 Slave Address Register	0x00
IC0.CR	0xA014	RW	I²C0 Control Register	0x00
IC0.SCLL	0xA018	RW	I²C0 SCL LOW duration Register	0xFFFF
IC0.SCLH	0xA01C	RW	I²C0 SCL HIGH duration Register	0xFFFF
IC0.SDH	0xA020	RW	I²C0 SDA Hold Register	0x7FFF
IC1.DR	0xA100	RW	I²C1 Data Register	0xFF
IC1.SR	0xA108	R, RW	I²C1 Status Register	0x00
IC1.SAR	0xA10C	RW	I²C1 Slave Address Register	0x00
IC1.CR	0xA114	RW	I²C1 Control Register	0x00
IC1.SCLL	0xA118	RW	I²C1 SCL LOW duration Register	0xFFFF
IC1.SCLH	0xA11C	RW	I²C1 SCL HIGH duration Register	0xFFFF
IC1.SDH	0xA120	RW	I²C1 SDA Hold Register	0x7FFF

11.3.1 ICn.DR I²C Data Register

ICn.DR is an 8-bits read/write register. It contains a byte of serial data to be transmitted or a byte which has just been received.

IC0.DR=0x4000_A000, IC1.DR=0x4000_A100,

7	6	5	4	3	2	1	0
DR							
0xFF							
RW							

7 0	ICDR	The most recently received data or data to be transmitted.

11.3.2 ICn.SR I²C Status Register

ICn.SR is an 8-bit read/write register. It contains the status of I²C bus interface. Writing to the register clears the status bits.

IC0.SR=0x4000_A008, IC1.SR=0x4000_A008

7	6	5	4	3	2	1	0
GCALL	TEND	STOP	SSEL	MLOST	BUSY	TMOD	RXACK
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

7	GCALL	This bit has different meaning depending on whether I²C is master or slave When I²C is a master, this bit represents whether it received AACK(Address ACK) from slave. When I²C is slave, this bit is used to indicate general call.	
		0	No AACK is received (master mode)
		1	AACK is received (master mode).
		0	General call is not detected (slave mode)
		1	General call is detected (slave mode)
6	TEND	1 Byte transmission complete flag	
		0	The transmission is working or not completed.
		1	The transmission is completed.
5	STOP	STOP flag	
		0	STOP is not detected.
		1	STOP is detected.
4	SSEL	Slave flag	
		0	Slave is not selected.
		1	Slave is selected.
3	MLOST	Mastership lost flag	
		0	Mastership is not lost.
		1	Mastership is lost.
2	BUSY	BUSY flag	
		0	I²C bus is in IDLE state.
		1	I²C bus is busy.
1	TMOD	Transmitter/Receiver mode flag	
		0	Receiver mode.
		1	Transmitter mode.
0	RXACK	Rx ACK flag	
		0	Rx ACK is not received.
		1	Rx ACK is received.

When an I2C interrupt occurs except for STOP interrupt, the SCL line is hold 'LOW'. To release SCL, write arbitray value to ICnSR. When ICnSR is written, the TEND, STOP, SSEL, MLOST, RXACK bits are cleared.

11.3.3 ICn.SAR I²C Slave Address Register

ICnSAR is an 8-bits read/write register. It shows the address in slave mode.

IC0.SAR=0x4000_A00C, IC1.SAR=0x4000_A10C

7	6	5	4	3	2	1	0
SVAD							GCEN
0x00							0
RW							RW

7 1	SVAD	7-bit Slave Address	
0	GCEN	General call enable bit	
		0	General call is disabled.
		1	General call is enabled.

11.3.4 ICn.CR I²C Control Register

ICnCR is an 8-bits read/write register. The register can be set to configure I²C operation mode and simultaneously allowed for I²C transactions to be kicked off.

IC0.CR=0x4000_A014, IC1.CR=0x4000_A114

7	6	5	4	3	2	1	0
IIF		SOFTRST	INTEN	ACKEN		STOP	START
0	0	0	0	0	0	0	0
RW		RW	RW	RW		RW	RW

7	IIF	Interrupt flag bit	
		0	No interrupt is generated or interrupt is cleared
		1	Interrupt is generated
5	SOFTRST	Soft Reset enable bit.	
		0	Soft Reset is disabled.
		1	Soft Reset is enabled..
4	INTEN	Interrupt enabled bit.	
		0	Interrupt is disabled.
		1	Interrupt is enabled.
3	ACKEN	ACK enable bit in Receiver mode.	
		0	ACK is not sent after receiving data.
		1	ACK is sent after receiving data.
1	STOP	Stop enable bit. When this bit is set as “1” in transmitter mode, next transmission will be stopped even though ACK signal has been received.	
		0	Stop is disabled.
		1	Stop is enabled. When this bit is set, transmission will be stopped.
0	START	Transmission start bit in master mode.	
		0	Waits in slave mode.
		1	Starts transmission in master mode.

11.3.5 ICn.SCLL I²C SCL LOW duration Register

ICnSCLL is a 16-bit read/write register. SCL LOW time can be set by writing this register in master mode.

IC0.SDLL=0x4000_A018, IC1.SDLL=0x4000_A118

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCLL															
0xFFFF															
RW															

15	SCLL	SCL LOW duration value.
		SCLL = (PCLK * SCLL[15:0]) + 2*PCLKs
0		Default value is 0xFFFF.

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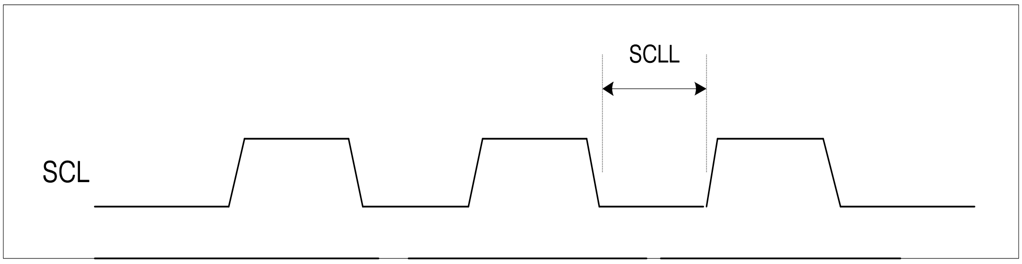


Figure11.2.SCL LOW Timing.

11.3.6 ICn.SCLH I^2C SCL HIGH duration Register

ICnSCLH is a 16-bit read/write register. SCL HIGH time will be set by writing this register in master mode.

IC0.SDLH=0x4000_A01C, IC1.SDLH=0x4000_A11C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCLH															
0xFFFF															
RW															

15 0	SCLH	SCL HIGH duration value. SCLH = (PCLK * SCLH[15:0]) + 3 PCLKs Default value is 0xFFFF.

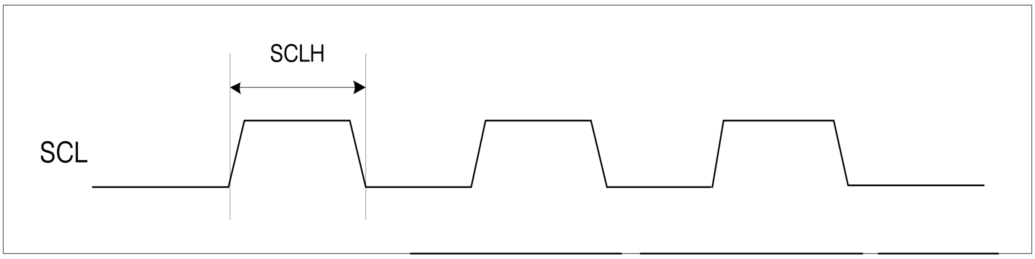


Figure11.3 SCL HIGH Timing

11.3.7 ICn.SDH SDA Hold Register

ICnSDH is a 15-bit read/write register. SDA HOLD time will be set by writing this register in master mode.

IC0.SDH=0x4000_A020, IC1.SDH=0x4000_A120

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SDH														
0x7FFF															
RW															

14	**SDH**	SDA HOLD time setting value. SDH = (PCLK * SDH[14:0]) + 4 PCLKs
0		Default value is 0x7FFF.

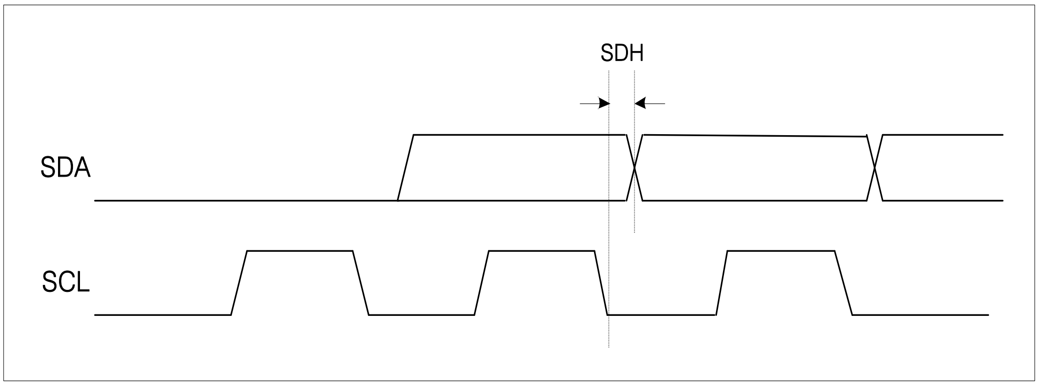


Figure11.4 SDA HOLD Timing

11.4 FUNTIONAL DESCRIPTION

11.4.1 I²C bit transfer

The data on the SDA line must be stable during the “H” period of the clock. The “H” or “L” state of the data line can only change when the clock signal on the SCL line is “L” (see Fig 11.5.).

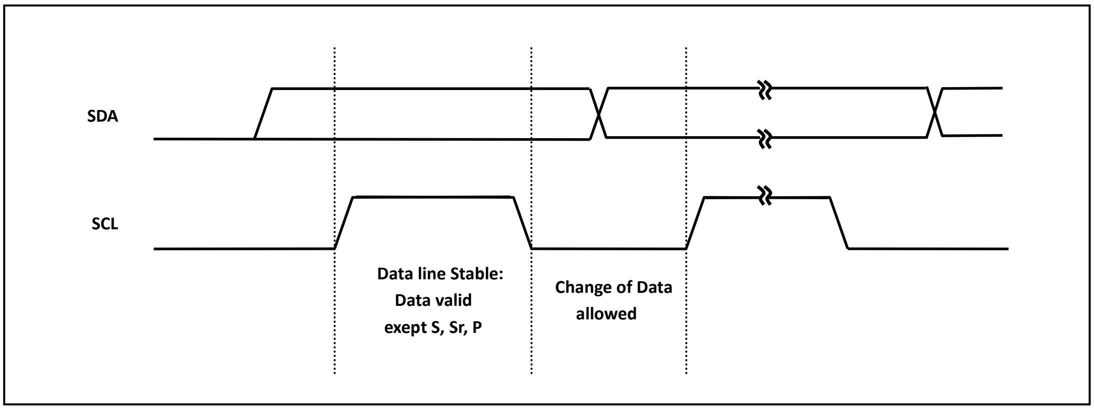


Figure11.5 I²C Bus bit transfer

11.4.2 START/Repeated START/STOP

Within the procedure of the I²C-bus, unique situations arise which are defined as START(S) and STOP(P) conditions (see Figure 11.6.).

i) An "H" to "L" transition on the SDA line while SCL is "H" is one such unique case. This situation indicates a START condition.

ii) A "L" to "H" transition on the SDA line while SCL is "H" defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.

The bus is busy if a repeated START(Sr) is generated instead of a STOP condition. In this respect, the START(S) and repeated START(Sr) conditions are functionally identical. For the remainder of this document therefore, the S symbol will be used as a generic term to represent both the START and repeated START conditions, unless Sr is particularly relevant.

Detection of START and STOP conditions by devices connected to the bus is easy if they incorporate the necessary interfacing hardware. However, microcontrollers with no such interface have to sample the SDA line at least twice per clock period to sense the transition.

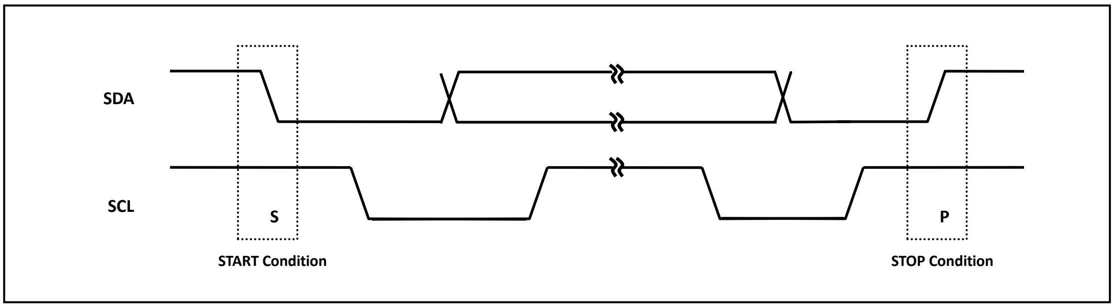


Figure11.6 START and STOP condition

11.4.3 Data Transfer

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (see Figure 11.7). If a slave can't receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL "L" to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

A message which starts with such an address can be terminated by generation of a STOP conditions, even during the transmission of a byte. In this case, no acknowledge is generated.

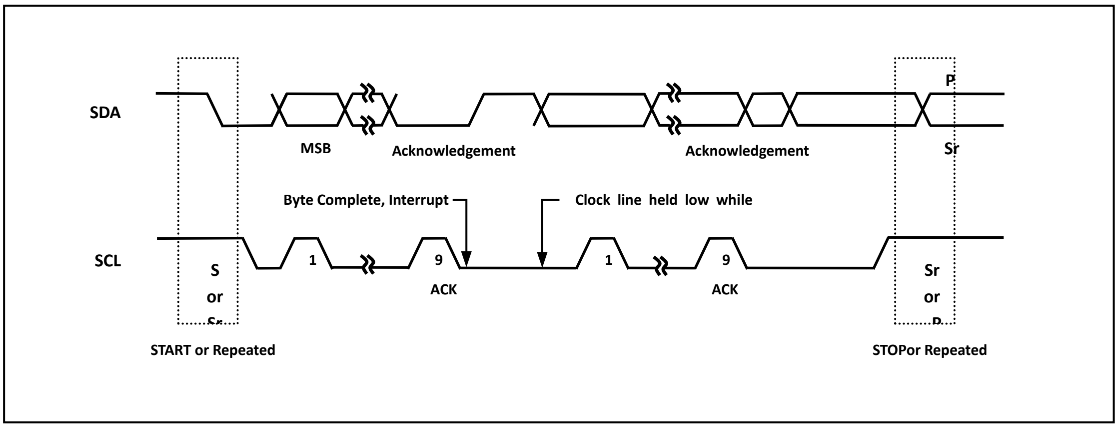


Figure11.7 I^2C Bus data transfer

11.4.4 Acknowledge

Data transfer with acknowledge is obligatory. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse.

The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable "L" during the "H" period of this clock pulse (see Figure 11.8). Of course, set-up and hold times must also be taken into account.

When a slave doesn't acknowledge the slave address (for example, it's unable to receive or transmit because it's performing some real-time function), the data line must be left "H" by the slave. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

If a slave-receiver does acknowledge the slave address but, sometime later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the slave generating the not-acknowledge on the first byte to follow. The slave leaves the data line "H" and the master generates a STOP or a repeated START condition.

If a master-receiver is involved in a transfer, it must signal the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter must release the data line to allow the master to generate a STOP or repeated START condition.

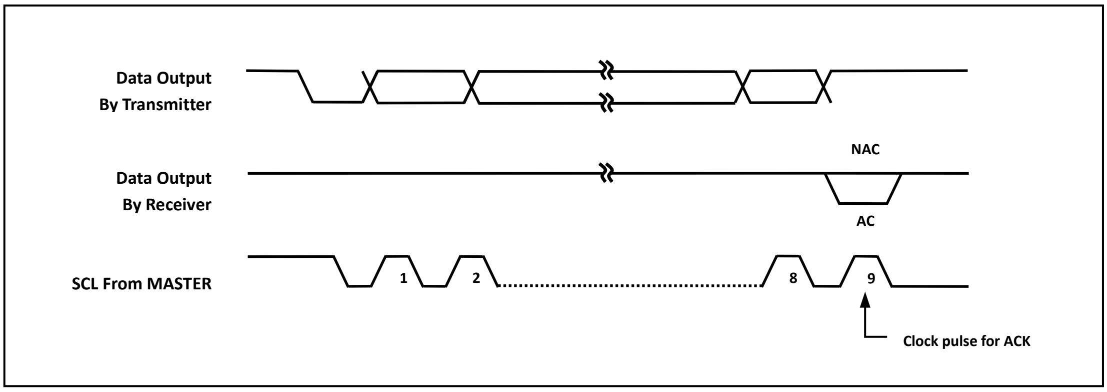


Figure11.8 I²C Bus bus acknowledge

11.4.5 Synchronization

All masters generate their own clock on the SCL line to transfer messages on the I²C-bus. Data is only valid during the "H" period of the clock. A defined clock is therefore needed for the bit-by-bit arbitration procedure to take place.

Clock synchronization is performed using the wired-AND connection of I²C interfaces to the SCL line. This means that an "H" to "L" transition on the SCL line will cause the devices concerned to start counting off their "L" period and, once a device clock has gone "L", it will hold the SCL line in that state until the clock "H" state is reached (see Figure 11.9). However, the "L" to "H" transition of this clock may not change the state of the SCL line if another clock is still within its "L" by the device with the longest "L" period. Devices with shorter "L" periods enter an "H" wait-state during this time.

When all devices concerned have counted off their "L" period, the clock line will be released and go "H". There will then be no difference between the device clocks and the state of the SCL line, and the devices will start counting their "H" periods. The first device to complete its "H" period will again pull the SCL line "L".

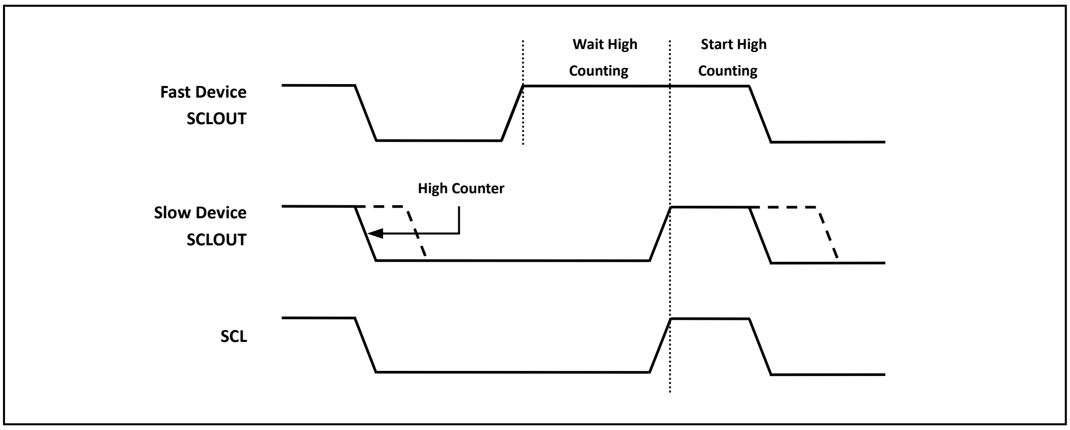


Figure11.9 Clock synchronization during the arbitration procedure

11.4.6 Arbitration

A master may start a transfer only if the bus is free. Two or more masters may generate a START condition within the minimum hold time of the START condition which results in a defined START condition to the bus.

Arbitration takes place on the SDA line, while the SCL line is at the “H” level, in such a way that the master which transmits “H” level, while another master is transmitting a “L” level will switch off its DATA output stage because the level on the bus doesn’t correspond to its own level.

Arbitration can continue for many bits. Its first stage is comparison of the address bits. If the masters are each trying to address the same device, arbitration continues with comparison of the data-bits if they are master-transmitter, or acknowledge-bits if they are master-receiver. Because address and data information on the I²C-bus is determined by the winning master, no information is lost during the arbitration process.

A master that loses the arbitration can generate clock pulses until the end of the byte in which it loses the arbitration.

If a master also incorporates a slave function and it loses arbitration during the addressing stage, it’s possible that the winning master is trying to address it. The losing master must therefore switch over immediately to its slave mode.

Figure 11.10 shows the arbitration procedure for two masters. Of course, more may be involved (depending on how many masters are connected to the bus). The moment there is a difference between the internal data level of the master generating Device1 Dataout and the actual level on the SDA line, its data output is switched off, which means that a “H” output level is then connected to the bus. This will not affect the data transfer initiated by the winning master.

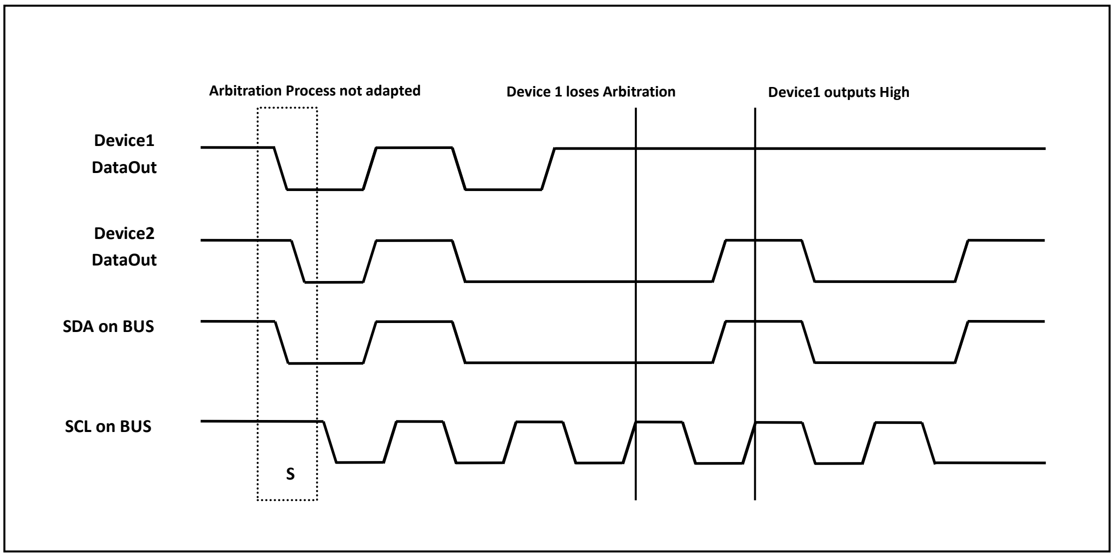


Figure11.10 Arbitration procedure of two masters

11.5 I²C OPERATION

I²C supports interrupt operation. Once interrupt is serviced, IIF(ICnCR[7]) flag is set. ICnSR shows I²C-bus status information and SCL line stays "L" before the register is written as a certain value. The status register can be cleared by writing.

11.5.1 Master Transmitter

It shows the flow of transmitter in master mode (see Figure 11.11.).

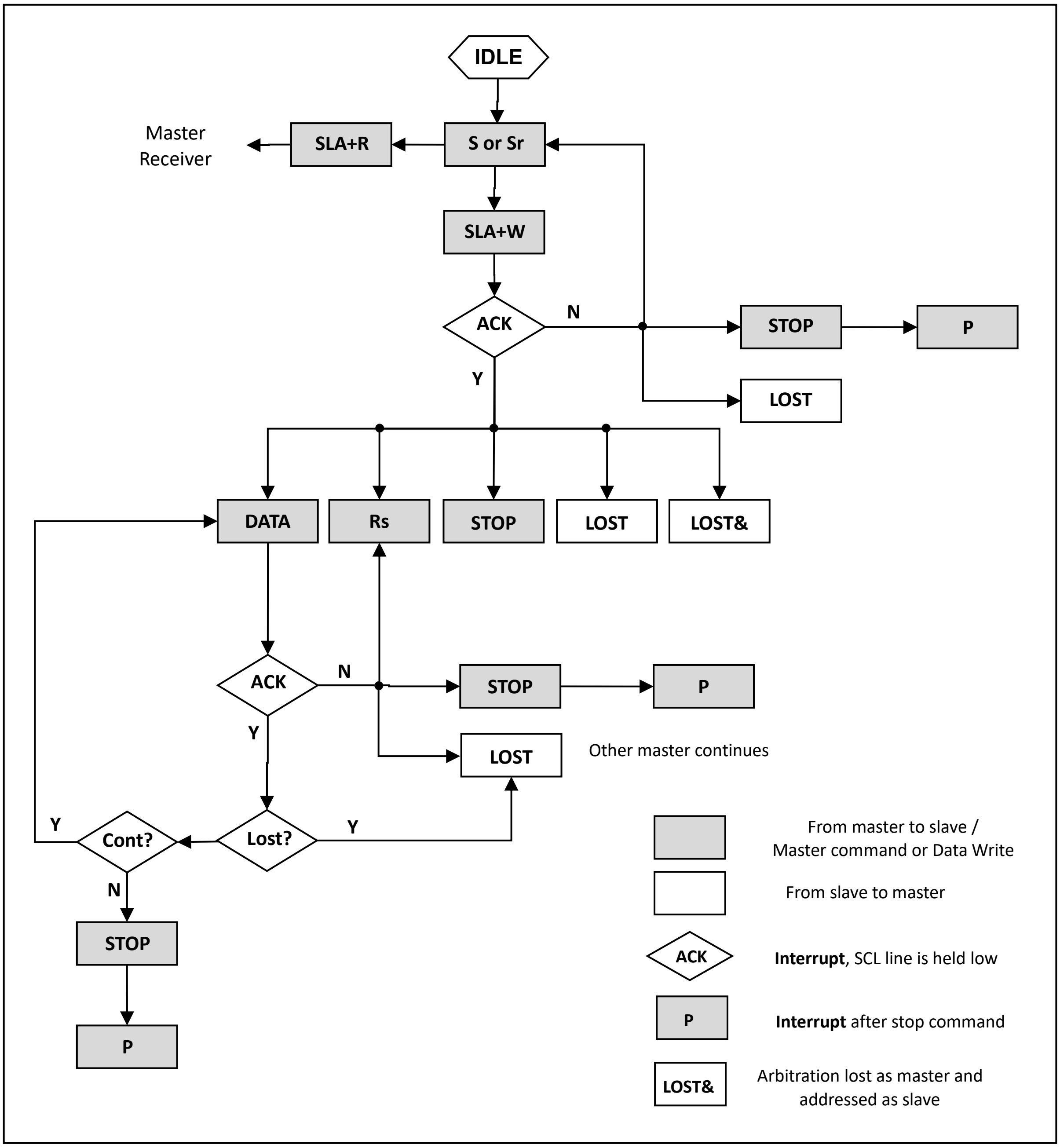


Figure11.11 Transmitter Flowchart in Master mode

11.5.2 Master Receiver

It shows the flow of receiver in master mode (see Figure 11.12).

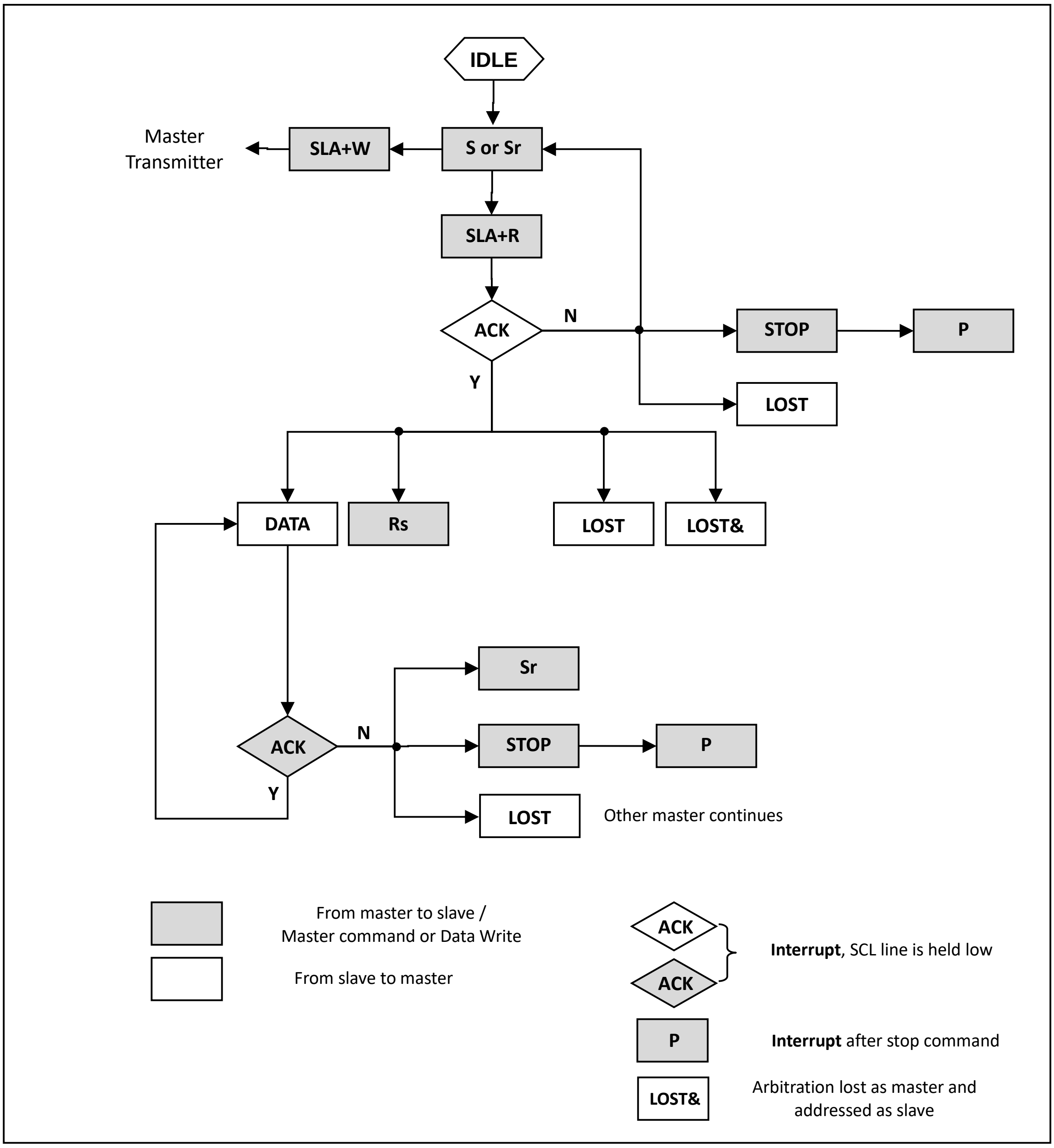


Figure11.12 Receiver Flowchart in Master mode

11.5.3 Slave Transmitter

It shows the flow of transmitter in slave mode (see Figure 11.13).

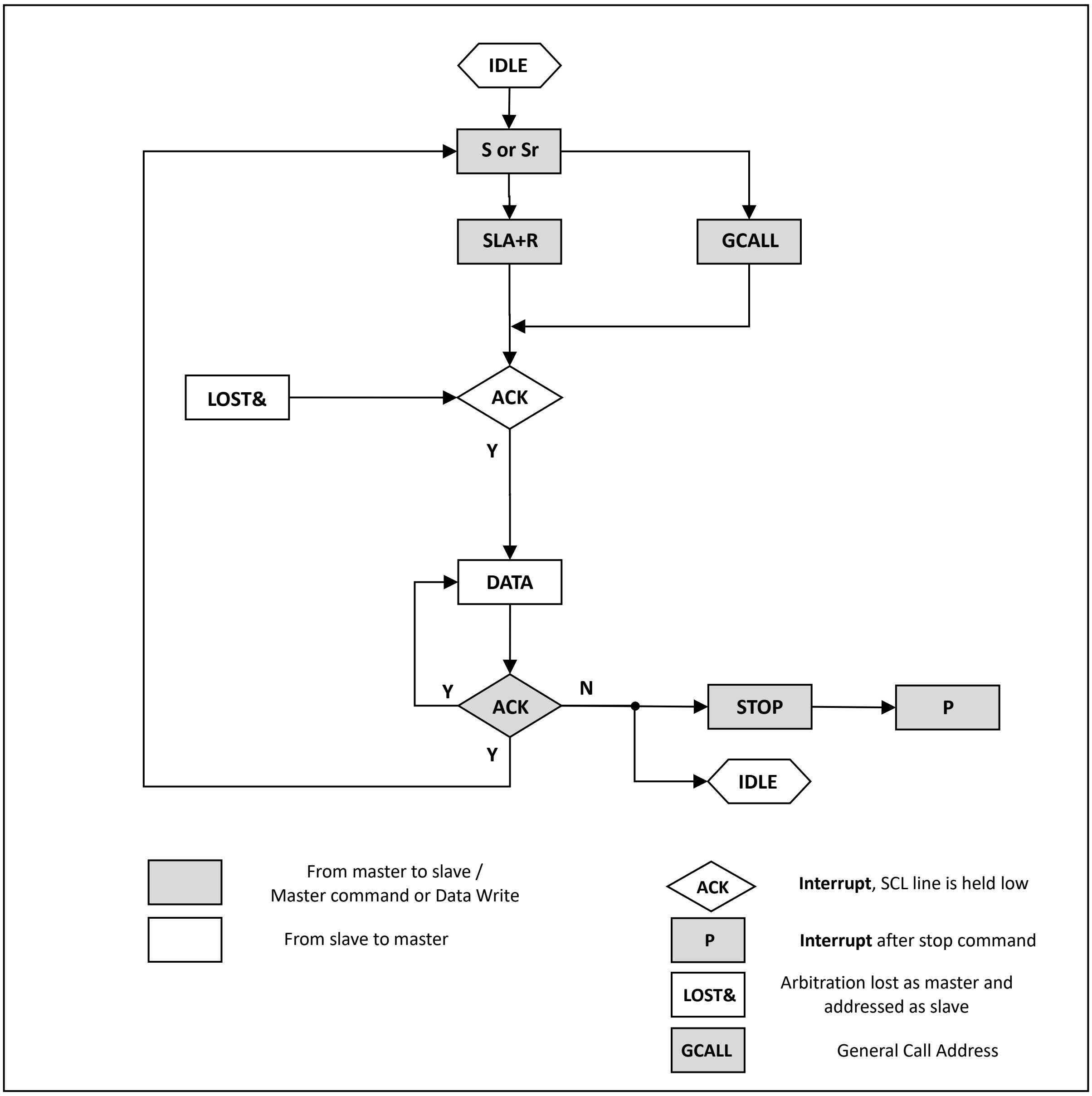


Figure11.13 Transmitter Flowchart in Slave mode

11.5.4 Slave Receiver

It shows the flow of receiver in slave mode (see Figure 11.14).

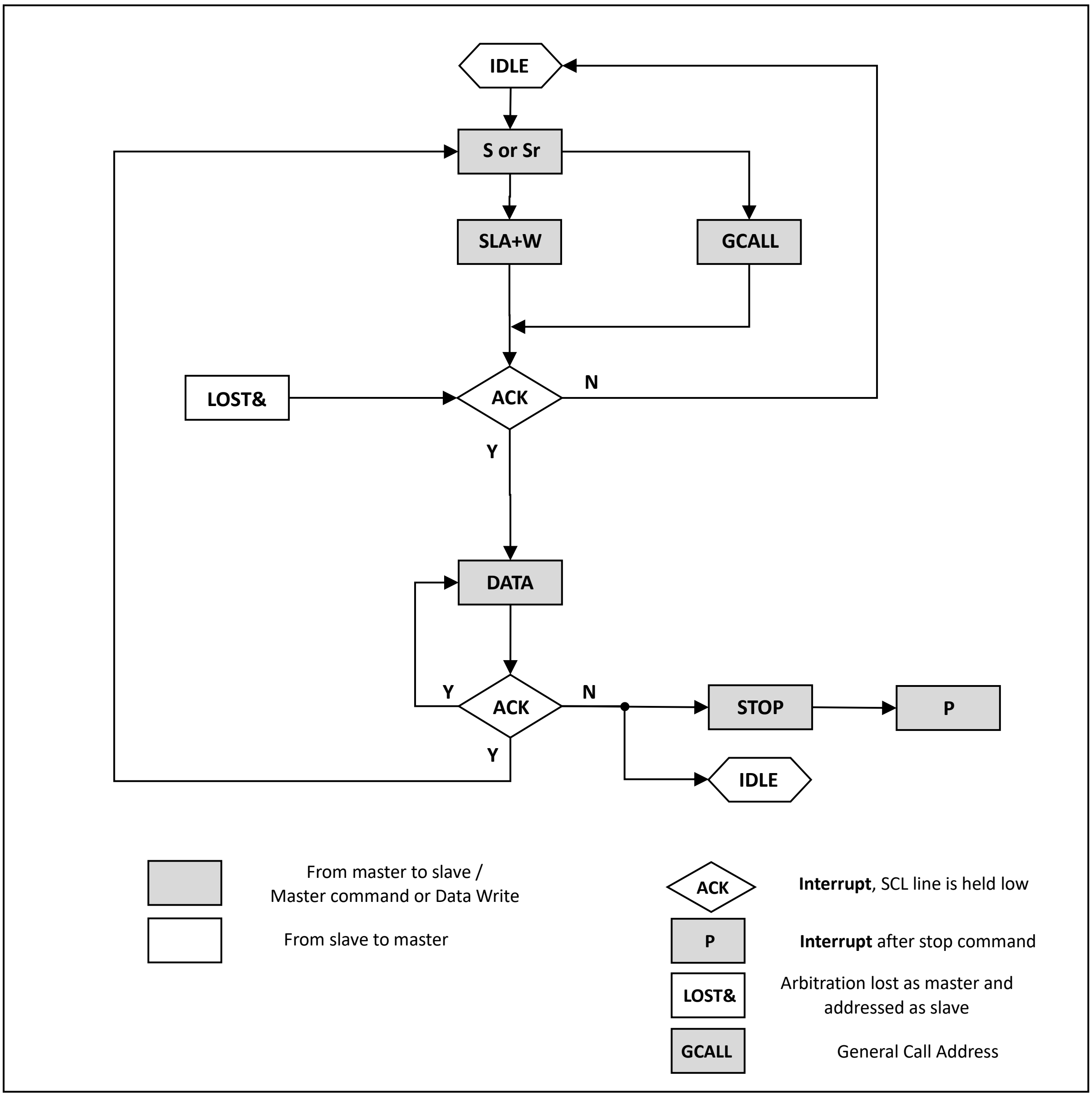


Figure11.14 Receiver Flowchart in Slave mode

CHAPTER 12. MOTOR PULSE-WIDTH-MODULATOR (MPWM)

12.1 OVERVIEW

MPWM is Programmable Motor controller

- 6-Channel outputs for motor control
- Dead- time zone support
- Protection event and over voltage event handling
- Six ADC trigger outputs
- Interval interrupt mode (period interrupt only)
- Up-down count mode

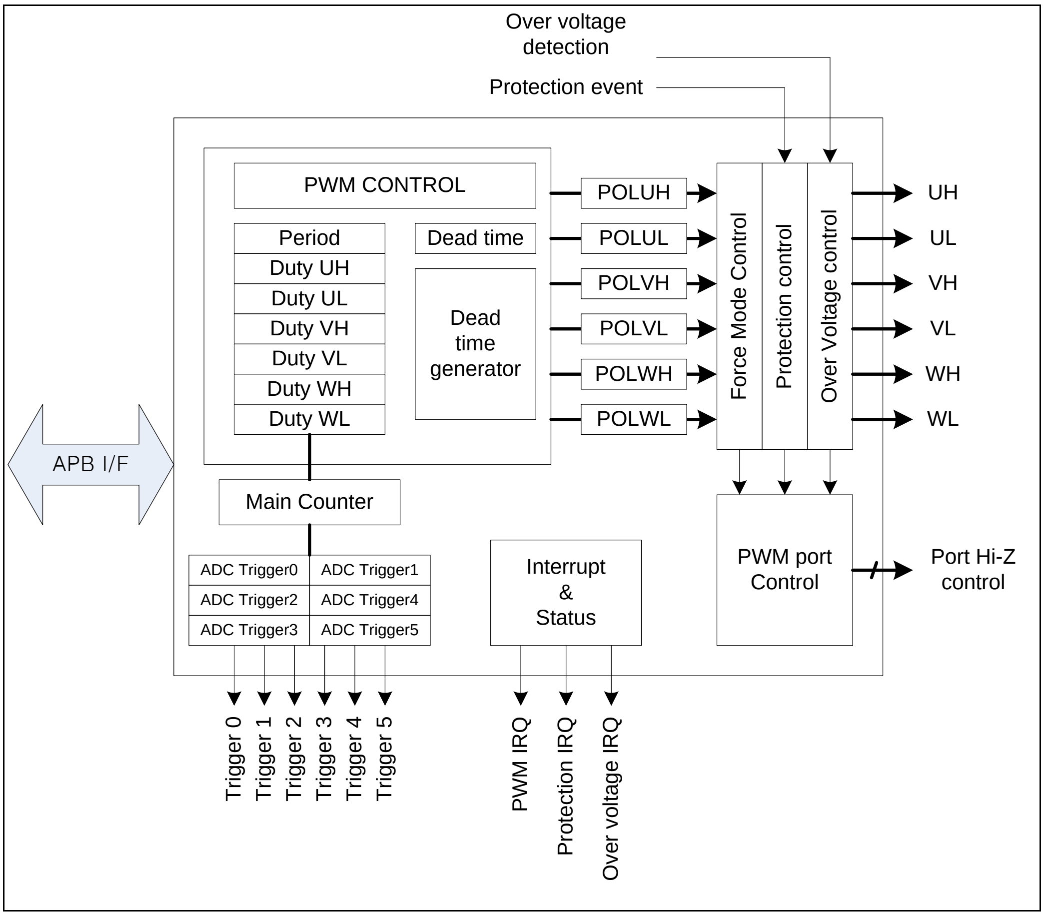


Figure12.1. Block Diagram

12.2 Pin description

Table12.1. External Signals

PIN NAME	TYPE	DESCRIPTION
MP0UH	O	MPWM 0 Phase-U H-side output
MP0UL	O	MPWM 0 Phase-U L-side output
MP0VH	O	MPWM 0 Phase-V H-side output
MP0VL	O	MPWM 0 Phase-V L-side output
MP0WH	O	MPWM 0 Phase-W H-side output
MP0WL	O	MPWM 0 Phase-W L-side output
MP1UH	O	MPWM 1 Phase-U H-side output
MP1UL	O	MPWM 1 Phase-U L-side output
MP1VH	O	MPWM 1 Phase-V H-side output
MP1VL	O	MPWM 1 Phase-V L-side output
MP1WH	O	MPWM 1 Phase-W H-side output
MP1WL	O	MPWM 1 Phase-W L-side output
PRTIN0	I	MPWM 0 Protection Input 0
OVIN0	I	MPWM 0 Over-voltage Input 1
PRTIN1	I	MPWM 1 Protection Input 0
OVIN1	I	MPWM 1 Over-voltage Input 1

12.3 REGISTERS

Base address of MPWM is below..

Table12.2. MPWM base address

NAME	BASE ADDRESS
MPWM0	0x4000_4000
MPWM1	0x4000_5000

Table 12.3 shows Register memory map .

Table12.3. MPWM Register map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
MPn.MR	0x0000	RW	PWM Mode register	0x0000_0000
MPn.PMR	0x0004	RW	PWM Port Mode register	0x0000_0000
MPn.OCR	0x0008	RW	PWM Output control	0x0000_0000
MPn.PRD	0x000C	RW	PWM Period register	0x0000_0002
MPn.DUH	0x0010	RW	PWM Duty UH register	0x0000_0001
MPn.DVH	0x0014	RW	PWM Duty VH register	0x0000_0001
MPn.DWH	0x0018	RW	PWM Duty WH register	0x0000_0001
MPn.DUL	0x001C	RW	PWM Duty UL register	0x0000_0001
MPn.DVL	0x0020	RW	PWM Duty VL register	0x0000_0001
MPn.DWL	0x0024	RW	PWM Duty WL register	0x0000_0001
MPn.CR1	0x0028	RW	PWM Control	0x0000_0000
MPn.CR2	0x002C	RW	PWM Start	0x0000_0000
MPn.SR	0x0030	R	PWM Status	0x0000_0000
MPn.IER	0x0034	RW	PWM Interrupt Enable	0x0000_0000
MPn.CNT	0x0038	R	PWM counter register	0x0000_0001
MPn.DTR	0x003C	RW	PWM dead time control	0x0000_0000
MPn.PCR	0x0040	RW	PWM protection control register	0x0000_0000
MPn.PSR	0x0044	RW	PWM protection status	0x0000_0080
MPn.OVCR	0x0048	RW	PWM over voltage control	0x0000_0000
MPn.OVSR	0x004C	RW	PWM over voltage status	0x0000_0000
MPn.ATCR	0x0054	RW	PWM ADC Trigger control	0x0000_0000
MPn.ATR1	0x0058	RW	PWM ADC Trigger reg1	0x0000_0000
MPn.ATR2	0x005C	RW	PWM ADC Trigger reg2	0x0000_0000
MPn.ATR3	0x0060	RW	PWM ADC Trigger reg3	0x0000_0000
MPn.ATR4	0x0064	RW	PWM ADC Trigger reg4	0x0000_0000
MPn.ATR5	0x0068	RW	PWM ADC Trigger reg5	0x0000_0000
MPn.ATR6	0x006C	RW	PWM ADC Trigger reg6	0x0000_0000

12.3.1 MPn.MR MPWM Mode Register

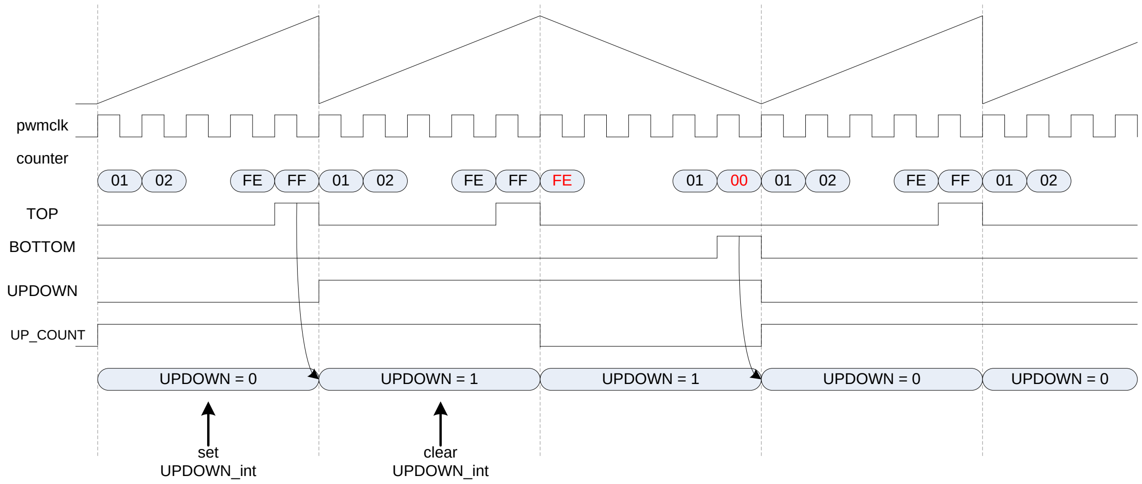
MPWM operation Mode register is 16-bit register.

MP0.MR=0x4000_4000, MP1.MR=0x4000_5000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOTOR		MCHMOD				UPDATE	UALL	FORCEN		FORCM				PDUP	UPDOWN
0	0	00		0	0	0	0	0	0	00		0	0	0	0
RW		RW				RW	RW	RW		RW				RW	RW

15	**MOTOR**	0	Normal PWM mode
		1	Motor PWM mode In Motor mode initial outputs of H-ch become LOW and outputs of L-ch become High (before PWM START)
13 12	**MCHMOD**	00	Motor control channel mode 2 channels symmetric mode Duty H decides the duty value of H-ch Duty L decides the duty value of L-ch
		01	1 channel asymmetric mode Duty H decides the up-counting duty value of H-ch Duty L decides the down-counting duty value of H-ch L channel become the inversion of H channel
		10	1 channel symmetric mode Duty H decides the dut value of H-ch L channel become the inversion of H channel
		11	Not valid (same with 00)
9	**UPDATE**	0	Update all duty, period register after
		1	Update all duty, period register enable. When UPDATE set, Duty and Period V registers are updated after two PWM clocks It should be cleared before PWM start(set PSTART)
8	**UALL**	0	No effect.
		1	Duty V and Duty W register will be stored with the same value of Duty U value when Duty U is written.
7	**FORCEN**	0	Force mode disable(normal mode)
		1	user can enable and disable each channels by Output control register
5 4	**FORCM**	00	Each channel is “AND”ed with MPnOCR (when port enable is low, output becomes low)
		01	Each channel is “OR”ed with MPnOCR (when port enable is high, output becomes high)
		10	Each channel is “XOR”ed with MPnOCR (when port enable is low, output becomes low)
		11	Each channel is “AND”ed with MPnOCR but when port disable, output becomes high-Z
1	**PDUP**	0	Period, duty value updated at every period match (both up count mode and BTB mode)
		1	Period, duty value updated at every period match and bottom(valid in updown count mode)
0	**UPDOWN**	0	PWM Up count mode
		1	PWM Up/Down count mode It must be set for MOTOR mode

Internal set and clear timing of UPDOWN mode from register write operation (UPDOWN_int means UPDOWN bit of MPWM mode register)



12.3.2 MPn.PMR MPWM Port Mode Register

MPWM Port Mode register is 16-bit register.

MP0.PMR=0x4000_4004, MP1.PMR=0x4000_5004

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						PMOD				POLUH	POLUL	POLVH	POLVL	POLWH	POLWL
0	0	0	0	0	0	00		0	0	0	0	0	0	0	0
						RW				RW	RW	RW	RW	RW	RW

9 8	**PMOD**	00	H-ch PWM pulse out, L-ch PWM pulse out
		01	H-ch PWM pulse out , L-ch out High-Z
		10	H-ch out High-Z, L-ch PWM pulse out
		11	H-ch out High-Z, L-ch out High-Z
5 3 1	**POLxH**	0	Normal polarity for UH/VH/WH pins ('H' during duty period in normal mode, 'L' in motor mode. Initial output is 'H')
		1	Inversion polarity for UH/VH/WH pins ('L' during duty period in normal mode, 'H' in motor mode. Initial output is 'L')
4 2 0	**POLxL**	0	Normal polarity for UL/VL/WL pins ('H' during duty period in normal mode, 'L' in motor mode. Initial output is 'L')
		1	Inversion polarity for UL/VL/WL pins ('L' during duty period in normal mode, 'H' in motor mode. Initial output is 'H')

	POL=0		**POL=1**	
PMODE	**UH**	**UL**	**UH**	**UL**
00	PWMUH	PWMUL	~PWMUH	~PWMUL
01	PWMUH	Hi-Z	~PWMUH	Hi-Z
10	Hi-Z	PWMUL	Hi-Z	~PWMUL
11	Hi-Z	Hi-Z	Hi-Z	Hi-Z

12.3.3 MPn.OCR MPWM Output Control Register

MPWM output control register is 8-bit register.

MP0.OCR=0x4000_4008, MP1.OCR=0x4000_5008,

7	6	5	4	3	2	1	0
		UHVAL	ULVAL	VHVAL	VLVAL	WHVAL	WLVAL
0	0	0	0	0	0	0	0
		RW	RW	RW	RW	RW	RW

xHVAL xLVAL	Operator value for each output port in Force Mode (ports output become High/Low or High-Z by FORCM[1:0]) in MPnMR register. Depending on FORCM selection, the output values are calculated with MPnOCR and current MPWM outputs.

12.3.4 MPn.PRD MPWM Period Register

MPWM Period Register is 16-bit register.

MP0.PRD=0x4000_400C, MP1.PRD=0x4000_500C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PERIOD															
0x0002															
RW															

15:0	PERIOD	16-bit PWM period. It should be larger than 0x0010 (if Duty is 0x0000, PWM will not work)

12.3.5 MPn.DUH MPWM Duty UH Register

MPWM U channel duty register is 16-bit register.

MP0.DUH=0x4000_4010, MP1.DUH=0x4000_5010

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUH															
0x0001															
RW															

15:0	DUTY UH [15:0]	16-bit PWM Duty for UH output.

12.3.6 MPn.DVH MPWM Duty VH Register

MPWM V channel duty register is 16-bit register.

MP0.DVH=0x4000_4014, MP1.DVH=0x4000_5014

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DVH															
0x0001															
RW															

15:0	DUTY VH	16-bit PWM Duty for VH output.

12.3.7 MPn.DWH MPWM Duty WH Register

MPWM W channel duty register is 16-bit register.

MP0.DWH=0x4000_4018, MP1.DWH=0x4000_5018

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DWH															
0x0001															
RW															

15:0	DUTY WH	16-bit PWM Duty for WH output.

12.3.8 MPn.DUL MPWM Duty UL Register

MPWM U channel duty register is 16-bit register.

MP0.DUL=0x4000_401C, MP1.DUL=0x4000_501C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUL															
0x0001															
RW															

15:0	DUTY UL	16-bit PWM Duty for UL output.

12.3.9 MPn.DVL MPWM Duty VL Register

MPWM V channel duty register is 16-bit register.

MP0.DVL=0x4000_4020, MP1.DVL=0x4000_5020

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DVL															
0x0001															
RW															

15:0	DUTY VL	16-bit PWM Duty for VL output.

12.3.10 MPn.DWL MPWM Duty WL Register

PWM W channel duty register is 16-bit register.

MP0.DWL=0x4000_4024, MP1.DWL=0x4000_5024

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DWL															
0x0001															
RW															

15:0	DUTY WL	16-bit PWM Duty for WL output.

12.3.11 MPn.CR1 MPWM Control Register 1

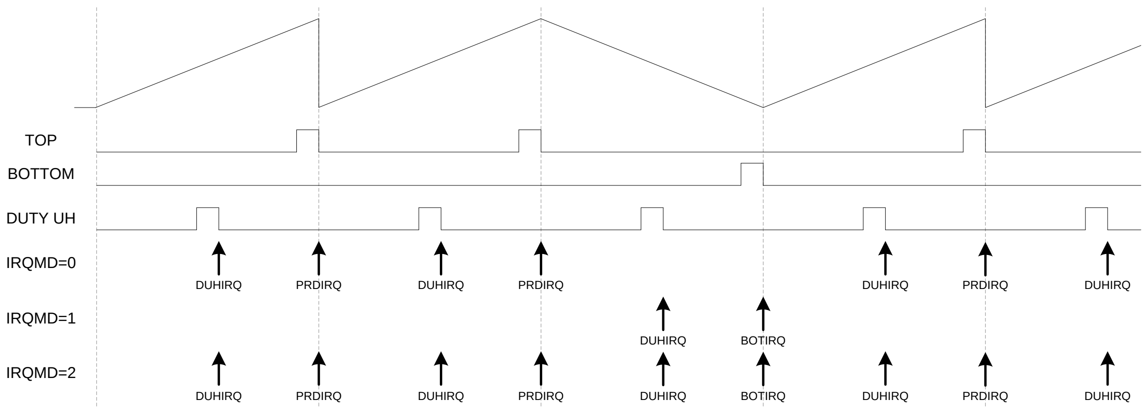
MPWM Control Register 1 is 16-bit register.

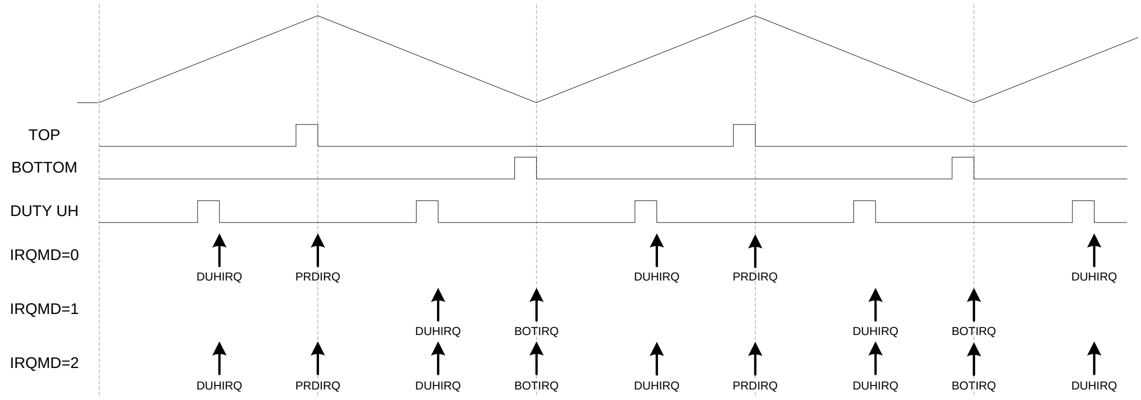
MP0.CR1=0x4000_4028, MP1.CR1=0x4000_5028

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTVEN		IRQMD			IRQN			PWMEN							HALT
0	0	0		0	0			0	0	0	0	0	0	0	0
RW		RW			RW			RW							RW

15	INTVEN		IRQ interval mode (IRQ asserts to CPU at every N-th period IRQ)
13 12	IRQMD	0	IRQ at period, duty match (UP)
		1	IRQ at bottom, duty match (DOWN) (only valid in UPDOWN mode)
		2	IRQ at every period, bottom, duty match (UP & DOWN)
10 8	IRQN[2:0]	IRQ interval number (1~8th PRDIRQ)	
7	PWMEN	PWM enable	
0	HALT	PWM HALT (PWM counter stop but not reset) PWM outputs keep previous state	

Each interrupt source can be enabled or disable by MPWM interrupt enable register





12.3.12 MPn.CR2 MPWM Control Register 2

MPWM Control Register 2 is 8-bit register.

MP0.CR2=0x4000_402C, MP1.CR2=0x4000_502C,

7	6	5	4	3	2	1	0
							PSTART
0	0	0	0	0	0	0	0
							RW

0	PSTART	0	PWM counter stop and clear
		1	PWM counter start (will be resynced @PWM clock twice) PWMEN should be “1” to start PWM counter

12.3.13 MPn.SR MPWM Status Register

PWM Status Register is 16-bit register.

MP0.SR=0x4000_4030, MP1.SR=0x4000_5030

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DOWN		IRQCNT						PRDIRQ	BOTIRQ	DUHIRQ	DULIRQ	DVHIRQ	DVLIRQ	DWHIRQ	DWLIRQ
0		000		0	0	0	0	0	0	0	0	0	0	0	0
RW		RW						RW	RW	RW	RW	RW	RW	RW	RW

15	DOWN	0	PWM Count Up
		1	PWM Count Down (in BTB mode)
14 12	IRQCNT[2:0]		Interrupt count number of period match (Interval PRDIRQ mode)
7	PRDIRQ		PWM period interrupt flag (0: no int / 1: int occurred) Write “1” to clear flag
6	BOTIRQ		PWM bottom interrupt flag (0: no int / 1: int occurred) Write “1” to clear flag
5	DUHIRQ		PWM duty UH interrupt flag (0: no int / 1: int occurred) Write “1” to clear flag
4	DULIRQ		PWM duty UL interrupt flag (0: no int / 1: int occurred) Write “1” to clear flag
3	DVHIRQ		PWM duty VH interrupt flag (0: no int / 1: int occurred) Write “1” to clear flag
2	DVLIRQ		PWM duty VL interrupt flag (0: no int / 1: int occurred) Write “1” to clear flag
1	DWHIRQ		PWM duty UH interrupt flag (0: no int / 1: int occurred) Write “1” to clear flag *This flag will be enabled by DUHIEN bit.
0	DWLIRQ		PWM duty WL interrupt flag (0: no int / 1: int occurred) Write “1” to clear flag

12.3.14 MPn.IER MPWM Interrupt Enable Register

MPWM Interrupt Enable Register is 8-bit register.

MP0.IER=0x4000_4034, MP1.IER=0x4000_5034,

7	6	5	4	3	2	1	0
PRDIEN	BOTIEN	DUHIEN	DULIEN	DVHIEN	DVLIEN	DWHIEN	DWLIEN
0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

7	PRDIEN	PWM period interrupt enable 0: interrupt disable 1: interrupt enable
6	BOTIEN	PWM bottom interrupt enable 0: interrupt disable 1: interrupt enable
5	DUHIEN	PWM U Duty H match interrupt enable 0: interrupt disable 1: interrupt enable
4	DULIEN	PWM U Duty L match interrupt enable 0: interrupt disable 1: interrupt enable
3	DVHIEN	PWM V Duty H match interrupt enable 0: interrupt disable 1: interrupt enable
2	DVLIEN	PWM V Duty L match interrupt enable 0: interrupt disable 1: interrupt enable
1	DWHIEN	PWM W Duty H match interrupt enable 0: interrupt disable 1: interrupt enable
0	DWLIEN	PWM W Duty L match interrupt enable 0: interrupt disable 1: interrupt enable

12.3.15 MPn.CNT MPWM Counter Register

PWM Counter Register is 16-bit Read-Only register.

MP0.CNT=0x4000_4038, MP1.CNT=0x4000_5038

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT															
0x0000															
RW															

MPnCNT	PWM counter value read (16-bit)

12.3.16 MPn.DTR MPWM Dead Time Register

PWM Dead Time Register is 16-bit register.

MP0.DTR=0x4000_403C, MP1.DTR=0x4000_503C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTEN							DTCLK	DT							
0	0	0	0	0	0	0	0	0x00							
RW							RW	RW							

15	DTEN	0	Dead Time disable
		1	Dead Time enable
8	DTCLK	0	Dead time counter uses PWM CLK/4
		1	Dead time counter uses PWM CLK/8
7 0	DT[7:0]	Dead Time value (Dead time setting makes output delay of 'low to high transition' in normal polarity) 0x01 ~0xFF : Dead time	

12.3.17 MPn.PCR MPWM Protection control Register

PWM Protection Control Register is 32-bit register.

MP0.PCR=0x4000_4040, MP1.PCR=0x4000_5040

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								PRTIN	C3IN	C2IN	C1IN	C0IN	AD2IN	AD1IN	AD0IN	PROTDIS		UHPROT	ULPROT	VHPROT	VLPROT	WHPROT	WLPROT	PROTCLR	PTDBC					PTSEL	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	000			0	0	00	
								RW	RW	RW	RW	RW	RW	RW	RW	RW		RW	RW	RW	RW	RW	RW	RW	RW					RW	

23	PRTIN	External PRTIN pin input (Active High)
22	C3IN	Comparator #3 output
21	C2IN	Comparator #2 output
20	C1IN	Comparator #1 output
19	C0IN	Comparator #0 output
18	AD2IN	ADC2 comparator output
17	AD1IN	ADC1 comparator output
16	AD0IN	ADC0 comparator output
15	PROTDIS	Protection mode disable (default 0, protection enable) To set PROTDIS as ‘1’, 0xA5A5 should be written to PROTPAT[31:16]
13	UHPROT	U-phase H-side protection output (‘0’=L/’1’=H)
12	ULPROT	U-phase L-side protection output (‘0’=L/’1’=H)
11	VHPROT	V-phase H-side protection output (‘0’=L/’1’=H)
10	VLPROT	V-phase L-side protection output (‘0’=L/’1’=H)
9	WHPROT	W-phase H-side protection output (‘0’=L/’1’=H)
8	WLPROT	W-phase L-side protection output (‘0’=L/’1’=H)
7	PROTCLR	Protection clear (after protection mode active) To clear PROTCLR bit, 0x39AA should be written to PROTPAT[31:16]
6 4	PTDBC[2:0]	Protection signal debounce 00 – no debounce 1~7 – debounce by (fsystem * PTDBC[2:0])
3 2		reserved
1 0	PTSEL[1:0]	Protection mode select 00 – no output control 01 – no control for UH/VH/WH UL/VL/WL controlled by UL~WLPROT 10 – no control for UL/VL/WL UH/VH/WH controlled by UH~WHPROT 11 – all outputs controlled by UH~WLPROT

12.3.18 MPn.PSR MPWM Protection Status Register

PWM Protection Status Register is 32-bit register.

MP0.PSR=0x4000_4044, MP1.PSR=0x4000_5044

31–16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROTPAT									PROTEN							PROTIN
0x0000	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1
RW									RW							RW

31 16	PROTPAT	Lock PROTPAT to set or reset Protection or Over voltage control bit
7	PROTEN	Protection mode enable status
0	PROTIN	Protection input status

12.3.19 MPn.OVCR MPWM Over Voltage control Register

PWM Over Voltage Control Register is 32-bit register.

MP0.PCR=0x4000_4048, MP1.PCR=0x4000_5048

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								OVIN	C3IN	C2IN	C1IN	C0IN	AD2IN	AD1IN	AD0IN	OVEN								OVCLR	OVDBC					OVSEL	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	000			0	0	00	
								RW	RW	RW	RW	RW	RW	RW	RW	RW								RW	RW					RW	

23	OVIN	External OVIN pin input
22	C3IN	Comparator #3 output
21	C2IN	Comparator #2 output
20	C1IN	Comparator #1 output
19	C0IN	Comparator #0 output
18	AD2IN	ADC2 comparator output (AD2CCR[23])
17	AD1IN	ADC1 comparator output (AD1CCR[23])
16	AD0IN	ADC0 comparator output (AD0CCR[23])
15	OVEN	Over voltage protection mode enable (default 0, over voltage protection disable) To set OVEN as ‘1’, 0x7788 should be written to PROTPAT[31:16]
7	OVCLR	OV Protection clear (after OV protection mode active) To clrea OVCLR flag, 0x5596 should be written to PROTPAT[31:16]
6 5 4	OVDBC	Over voltage protection signal debounce 00 – no debounce 1~7 – debounce by (fsystem * PTDBC[2:0])
1 0	OVSEL	Over Voltage Protection mode select 00 – no output control 01 – High output for UH/VH/WH + POL Low output for UL/VL/WL + POL 10 – Low output for UH/VH/WH + POL High output for UL/VL/WL + POL 11 – all outputs controlled by UH~WLPROT

12.3.20 MPn.OVSR MPWM Over Voltage Status Register

PWM Over Voltage Status Register is 8-bit Read-Only register.

MP0.OVSR=0x4000_404C, MP1.OVCR=0x4000_504C,

7	6	5	4	3	2	1	0
OVSTAT							OVPIN
0	0	0	0	0	0	0	0
R							R

7	OVSTAT	Over voltage protection mode status
0	OVPIN	Over voltage protection input status

12.3.21 MPn.ATCR MPWM ADC Trigger Control Register

PWM ADC Trigger Control Register is 16-bit register.

MP0.ATCR=0x4000_4054, MP1.ATCR=0x4000_5054

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							ATRGALL	ATRGEN						ATRGM	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	00	
							RW	RW						RW	

8	ATRGALL	ADC Trigger register 0 match event makes all trigger signals	
7	ATRGEN	ADC Trigger mode enable	
1 0	ATRGM	00	Always ADC Trigger enable when TRGEN is high
		01	ADC Trigger disable in protection state
		10	ADC Trigger disable in over voltage state
		11	ADC Trigger disable in protection, over voltage state

12.3.22 MPn.ATRm MPWMn ADC Trigger Counter m Register

MPn.ATR1 MPWM ADC Trigger Counter 1 Register
MPn.ATR2 MPWM ADC Trigger Counter 2 Register
MPn.ATR3 MPWM ADC Trigger Counter 3 Register
MPn.ATR4 MPWM ADC Trigger Counter 4 Register
MPn.ATR5 MPWM ADC Trigger Counter 5 Register
MPn.ATR6 MPWM ADC Trigger Counter 6 Register

PWM ADC Trigger Counter Register is 32-bit register.

MP0.ATR1=0x4000_4058, MP1.ATR1=0x4000_5058
MP0.ATR2=0x4000_405C, MP1.ATR2=0x4000_505C
MP0.ATR3=0x4000_4060, MP1.ATR3=0x4000_5060
MP0.ATR4=0x4000_4064, MP1.ATR4=0x4000_5064
MP0.ATR5=0x4000_4068, MP1.ATR5=0x4000_5068
MP0.ATR6=0x4000_406C, MP1.ATR6=0x4000_506C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												ATUDT		ATMOD		ATCNT															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0x0000															
												RW		RW		RW															

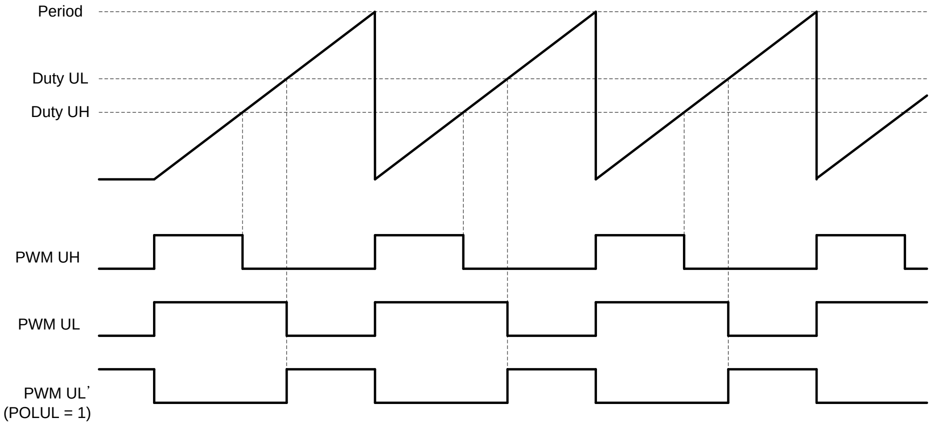
19	ATUDT	0	Trigger register update mode ADC trigger value applied at period match event (at the same time with period and duty registers update)
		1	Trigger register update mode When this bit set, written Trigger register values are sent to trigger compare block after two PWM clocks (through synchronization logic)
17 16	ATMOD	00	ADC trigger Mode register ADC trigger Disable
		01	Trigger out when up count match
		10	Trigger out when down count match
		11	Trigger out when up-down count match
15 0	ATCNT	ADC Trigger counter 0 (it should be less than PWM period)	

12.4 Functional Description

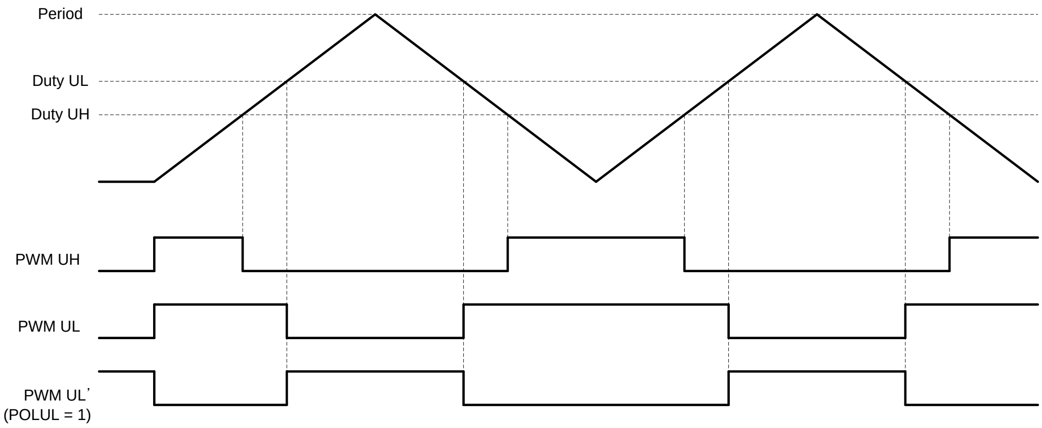
12.4.1 Normal PWM mode timing diagram Register

Normal PWM Mode

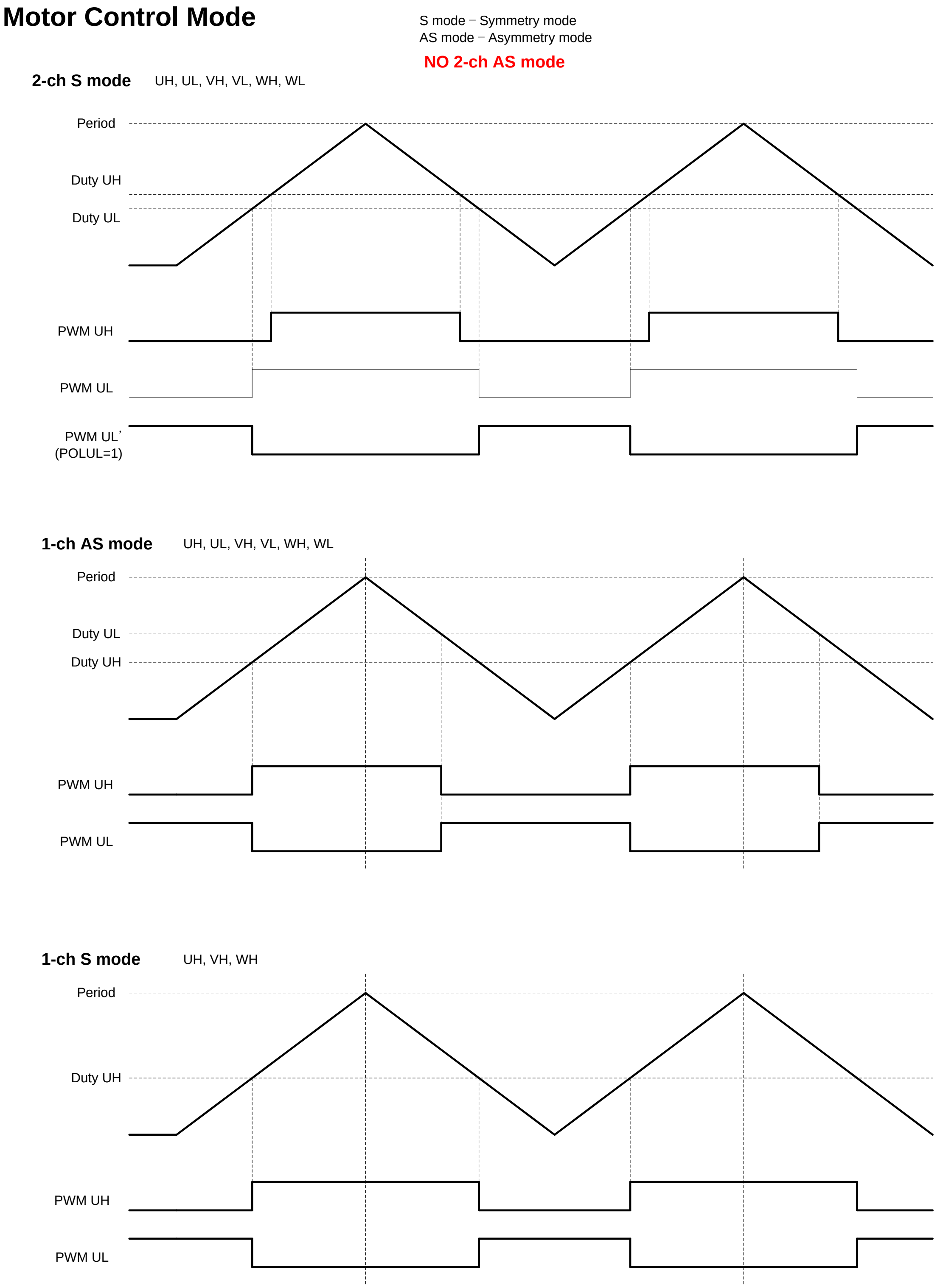
UP Count mode



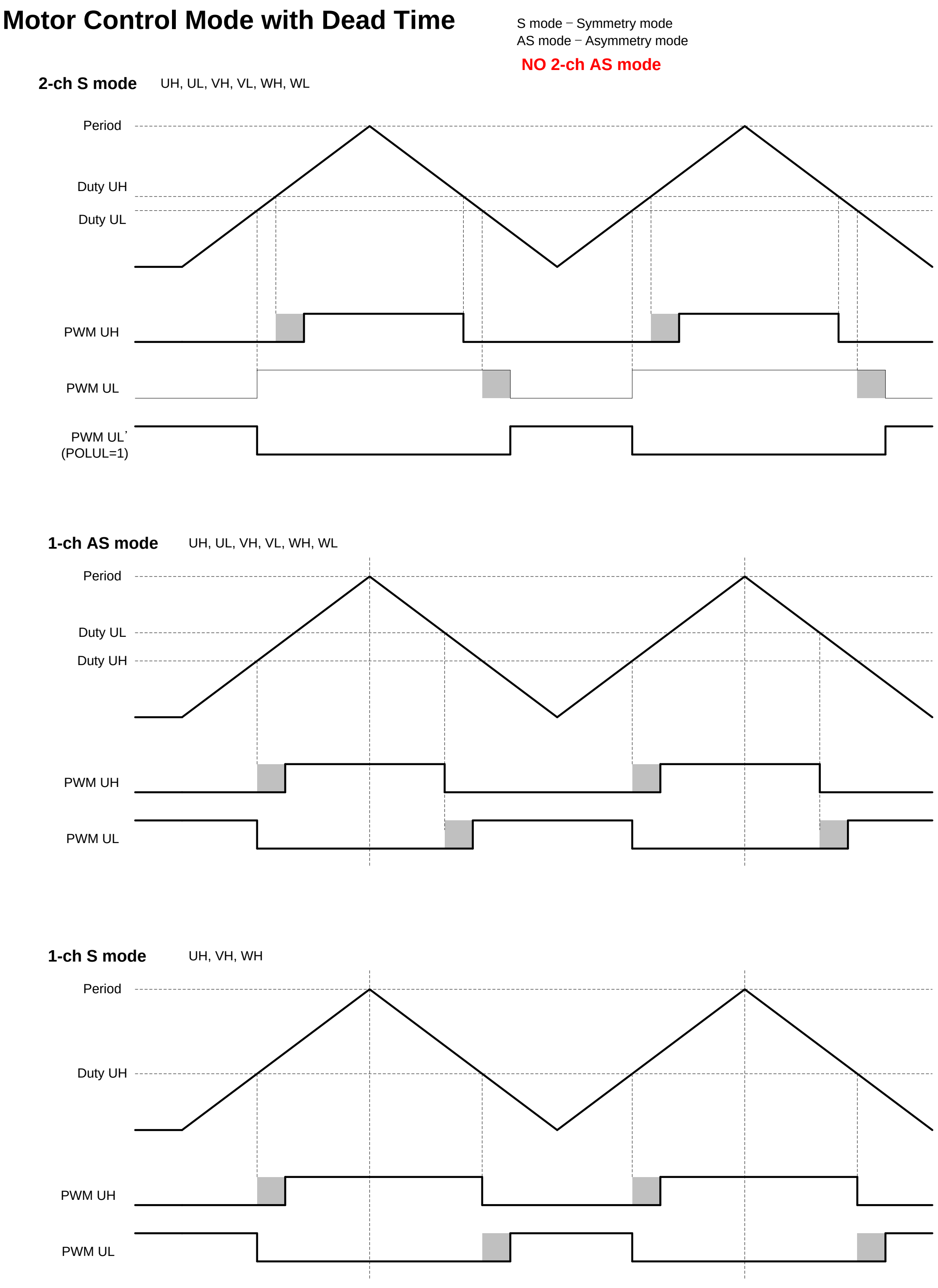
UP/DOWN Count mode



12.4.2 Motor PWM Mode timing diagram



12.4.3 Motor PWM mode with dead time zone



12.4.4 PWM output combination table

PWM mode : PWM out becomes high for duty duration

Motor mode : PWM out becomes low for duty duration

PWM mode		UHOUT	ULOUT	VHOUT	VLOUT	WHOUT	WLOUT
	initial	L	L	L	L	L	L
UPDOWN=0	up count	up@period	up@period	up@period	up@period	up@period	up@period
	up count	down@dutyUH	down@dutyUL	down@dutyVH	down@dutyVL	down@dutyWH	down@dutyWL
UPDOWN=1	up count	down@dutyUH	down@dutyUL	down@dutyVH	down@dutyVL	down@dutyWH	down@dutyWL
	down count	up@dutyUH	up@dutyUL	up@dutyVH	up@dutyVL	up@dutyWH	up@dutyWL
MOTOR mode		UHOUT	ULOUT	VHOUT	VLOUT	WHOUT	WLOUT
2CHS	initial	L	L	L	L	L	L
	up count	up@dutyUH	up@dutyUL	up@dutyVH	up@dutyVL	up@dutyWH	up@dutyWL
	down count	down@dutyUH	down@dutyUL	down@dutyVH	down@dutyVL	down@dutyWH	down@dutyWL
1CHAS	initial	L	~UHOUT	L	~VHOUT	L	~WHOUT
	up count	up@dutyUH	~UHOUT	up@dutyVH	~VHOUT	up@dutyWH	~WHOUT
	down count	down@dutyUL	~UHOUT	down@dutyVL	~VHOUT	down@dutyWL	~WHOUT
1CHS	initial	L	~UHOUT	L	~VHOUT	L	~WHOUT
	up count	up@dutyUH	~UHOUT	up@dutyVH	~VHOUT	up@dutyWH	~WHOUT
	down count	down@dutyUH	~UHOUT	down@dutyVH	~VHOUT	down@dutyWH	~WHOUT
POLARITY control		Polarity UH	Polarity UL	Polarity VH	Polarity VL	Polarity WH	Polarity WL

PMOD	00	UHOUT	ULOUT	VHOUT	VLOUT	WHOUT	WLOUT
	01	UHOUT	hi-Z	VHOUT	hi-Z	WHOUT	hi-Z
	10	hi-Z	ULOUT	hi-Z	VLOUT	hi-Z	WLOUT
priority = 4	11	hi-Z	hi-Z	hi-Z	hi-Z	hi-Z	hi-Z
FORCM	00	UHOUT & UHEN	ULOUT & ULEN	VHOUT & VHEN	VLOUT & VLEN	WHOUT & WHEN	WLOUT & WLEN
	01	UHOUT | UHEN	ULOUT | ULEN	VHOUT | VHEN	VLOUT | VLEN	WHOUT | WHEN	WLOUT | WLEN
	10	UHOUT ^ UHEN	ULOUT ^ ULEN	VHOUT ^ VHEN	VLOUT ^ VLEN	WHOUT ^ WHEN	WLOUT ^ WLEN
	11	UHOUT & UHEN	ULOUT & ULEN	VHOUT & VHEN	VLOUT & VLEN	WHOUT & WHEN	WLOUT & WLEN
priority = 3		if ~UHEN, hi-Z	if ~ULEN, hi-Z	if ~VHEN, hi-Z	if ~VLEN, hi-Z	if ~WHEN, hi-Z	if ~WLEN, hi-Z

PTSEL	00	UHOUT	ULOUT	VHOUT	VLOUT	WHOUT	WLOUT
PROTIN=1	01	UHOUT	ULPROT	VHOUT	VLPROT	WHOUT	WLPROT
	10	UHPROT	ULOUT	VHPROT	VLOUT	WHPROT	WLOUT
priority = 2	11	UHPROT	ULPROT	VHPROT	VLPROT	WHPROT	WLPROT
OVSEL	00	UHOUT	ULOUT	VHOUT	VLOUT	WHOUT	WLOUT
OVPIN=1	01	high	low	high	low	high	low
	10	low	high	low	high	low	high
priority = 1	11	UHPROT	ULPROT	VHPROT	VLPROT	WHPROT	WLPROT

CHAPTER 13. 12-BIT A/D CONVERTER

13.1 OVERVIEW

ADC block consists of 3 independent ADC units.

- 16 Channels of analog inputs
- Single and Continuous conversion mode
- Up to 8 times burst conversion support
- External pin trigger support
- 4 internal trigger sources support (PWMs, timers)
- Adjustable sample & hold time

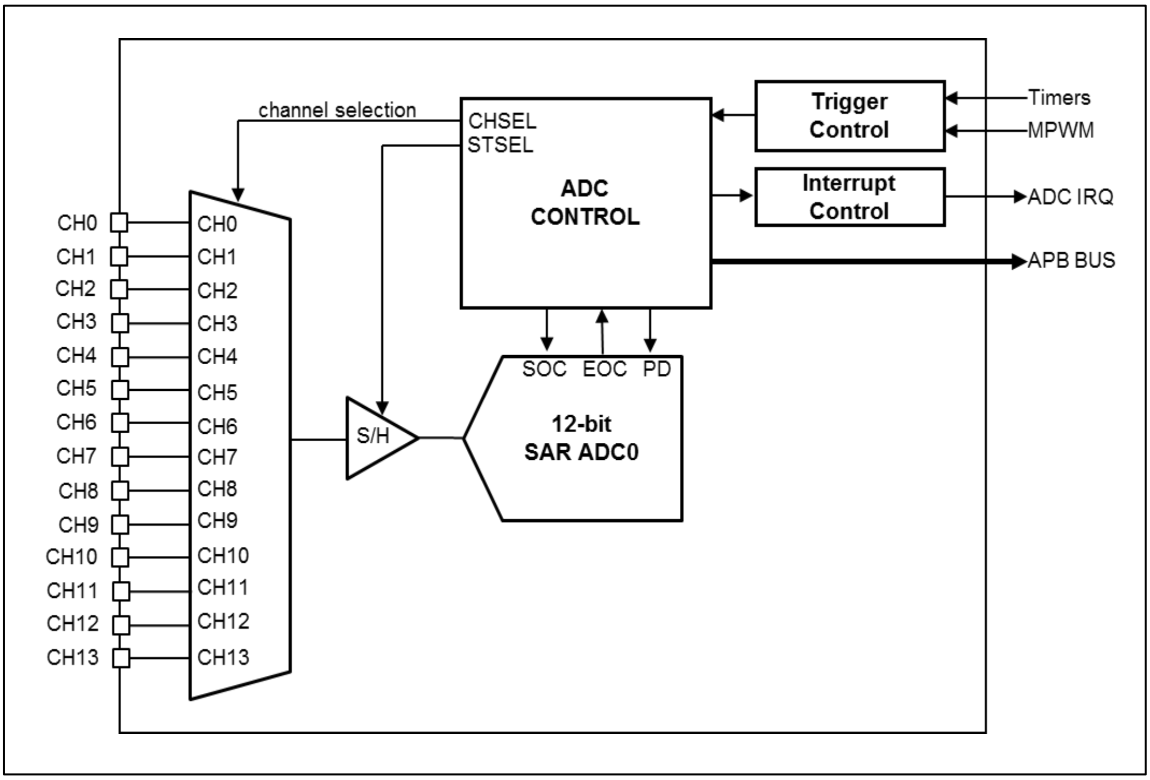


Figure13.1. Block Diagram

13.2 Pin description

Table13.1. External Signal

PIN NAME	TYPE	DESCRIPTION
AVDD	P	Analog Power(3.0V~VDD)
AVSS	P	Analog GND
AN0	A	ADC Input 0
AN1	A	ADC Input 1
AN2	A	ADC Input 2
AN3	A	ADC Input 3
AN4	A	ADC Input 4
AN5	A	ADC Input 5
AN6	A	ADC Input 6
AN7	A	ADC Input 7
AN8	A	ADC Input 8
AN9	A	ADC Input 9
AN10	A	ADC Input 10
AN11	A	ADC Input 11
AN12	A	ADC Input 12
AN13	A	ADC Input 13
AN14	A	ADC Input 14
AN15	A	ADC Input 15

13.3 REGISTERS

Base addresses of ADC units are as below..

Table13.2. ADC base address

NAME	BASE ADDRESS
ADC0	0x4000_B000
ADC1	0x4000_B100
ADC2	0x4000_B200

Table 13.3 shows Register memory map .

Table13.3. ADC Register map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
ADn.MR	0x0000	RW	ADC Mode register	0x00
ADn.CSR	0x0004	RW	ADC Channel Select register	0x00
ADn.CR1	0x0008	RW	ADC Control register	0x80
ADn.TRG0	0x000C	RW	ADC Trigger 0 channel register	0x00
ADn.TRG1	0x0010	RW	ADC Trigger 1 channel register	0x00
ADn.TRG2	0x0014	RW	ADC Trigger 2 channel register	0x00
ADn.BCSR	0x0018	RW	ADC Burst mode channel select	0x00
ADn.CR2	0x0020	RW	ADC Start	0x00
ADn.SR	0x0024	RW	ADC Status	0x00
ADn.IER	0x0028	RW	ADC Interrupt Enable register	0x00
AD0/1/2 DDR	0x002C	R	ADC0/1/2 DMA Data Register	0x00
ADn.CCR	0x0070	RW	ADC Channel compare register	0x00

13.3.1 AD*n*.MR ADC*n* Mode Register

ADC Mode Registers are 32-bit registers.

This register configures ADC operation Mode.

AD0.MR=0x4000_B000, AD1.MR=0x4000_B100, AD2.MR=0x4000_B200

31–24	23	22	21	20	19	18	17	16	15	14	13	12	11	10–8	7	6	5–4	3	2–0
BWAIT							DMAEN	DMACH				BWAITEN		BSTCNT	ADCEN		ADCMOD	TRGEN	TRGSRC
0x00	0	0	0	0	0	0	0	0	0	0	0	0	0	000	0	0	00	0	000
RW							RW	RW				RW		RW	RW		RW	RW	RW

31 24	**BWAIT**		Burst wait count value (8-bit) ADC conversion delayed for "BWAIT value" * MCLK for next conversion in burst mode		
17	**DMAEN**		DMA enable bit – **should be set to '1'** when ADCEN='1'. When DMA function is enable, DMA request at every end of conversion(also in burst mode) and interrupt request only be generated when ADC receives DMA done from DMAC.		
16	**DMACH**		DMA channel option When DMACH is set, Channel information of DMA data will be located at ADDMAR[3:0] for half word size transfer. Channel information is at ADDMAR[19:16] in default.(DMACH is low)		
12	**BWAITEN**		Burst wait Enable In burst mode, wait cycles can be inserted between next channel selection and conversion start		
		0	BWAIT in burst mode disable		
		1	BWAIT in burst mode enable		
10 8	**BSTCNT**	000	No Burst mode(Single)	100	5 burst AD conversion
		001	2 burst AD conversion	101	6 burst AD conversion
		010	3 burst AD conversion	110	7 burst AD conversion
		011	4 burst AD conversion	111	8 burst AD conversion
7	**ADCEN**	0	ADC disable		
		1	ADC enable		
5 4	**ADCMOD**	00	Single conversion mode		
		01	Continuous conversion mode		
		10	Reserved		
		11	Burst Mode		
3	**TRGEN**	0	Trigger sources disable		
		1	Trigger sources enable Trigger sources only support single & burst mode (not support continuous mode)		
2 0	**TRGSRC**	000	External pin Trigger		
		001	Timer Group 1 Trigger		
		010	Timer Group 2 Trigger		
		011	Timer Group 3 Trigger		
		100	MPWM 0 trigger		
		101	MPWM 1 trigger		
		110	Reserved		
		111	Reserved		

ADC	TIMER TRIGGER SOURCE		
	Timer Group 1	**Timer Group 2**	**Timer Group 3**
ADC0	TIMER1	TIMER2	-
ADC1	TIMER1	TIMER2	TIMER8
ADC2	TIMER1	TIMER2	TIMER9

If ADCMOD was set for Burst Mode, ADC channels controlled by BST0CH ~ BST7CH. Burst mode always start from BST0CH.(In 3 bust mode, Analog inputs of channels which assigned at BST0CH/BST1CH /BST2CH are converted sequentially)

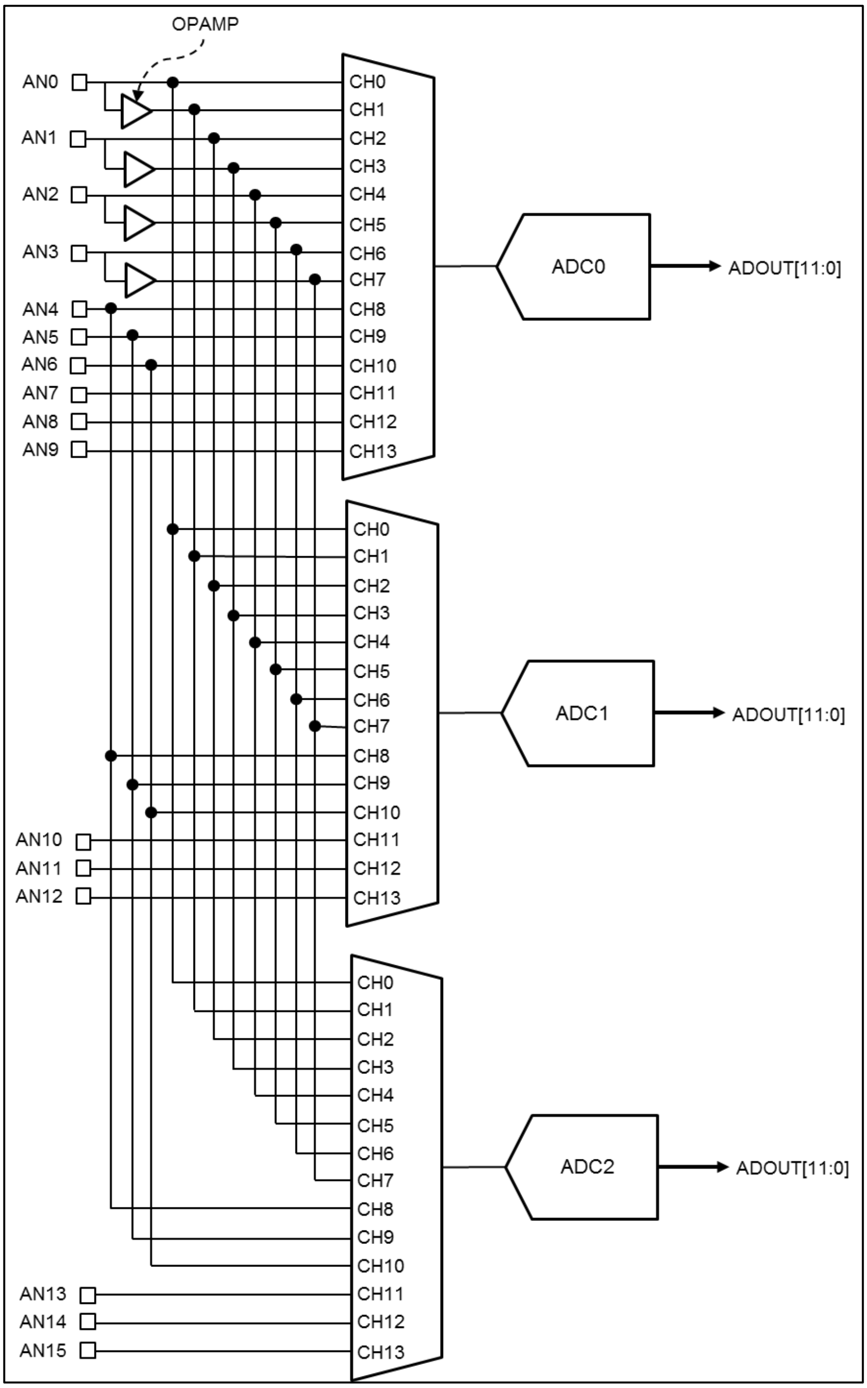


Figure 13.2 Analog Channel Block Diagram

13.3.2 ADn.CSR ADCn Channel Select Register

ADC Channel Select Registers are 8-bit registers.
ADC input channel select register

AD0.SR=0x4000_B004, AD1.SR=0x4000_B104, AD2.SR=0x4000_B204,

7	6	5	4	3	2	1	0
				CHSEL			
0	0	0	0	0x0			
				RW			

3 0	CHSEL	0000	ADC channel 0 selection
		0001	ADC channel 1 selection
		0010	ADC channel 2 selection
		0011	ADC channel 3 selection
		0100	ADC channel 4 selection
		0101	ADC channel 5 selection
		0110	ADC channel 6 selection
		0111	ADC channel 7 selection
		1000	ADC channel 8 selection
		1001	ADC channel 9 selection
		1010	ADC channel 10 selection
		1011	ADC channel 11 selection
		1100	ADC channel 12 selection
		1101	ADC channel 13 selection
		1110	ADC channel 14 selection
		1111	ADC channel 15 selection

Table13.4. ADC channel select

CHSEL	ADC0	ADC1	ADC2	
0000	AIN0	AIN0	AIN0	CH0
0001	AIN0_OPAMP	AIN0_OPAMP	AIN0_OPAMP	CH1
0010	AIN1	AIN1	AIN1	CH2
0011	AIN1_OPAMP	AIN1_OPAMP	AIN1_OPAMP	CH3
0100	AIN2	AIN2	AIN2	CH4
0101	AIN2_OPAMP	AIN2_OPAMP	AIN2_OPAMP	CH5
0110	AIN3	AIN3	AIN3	CH6
0111	AIN3_OPAMP	AIN3_OPAMP	AIN3_OPAMP	CH7
1000	AIN4	AIN4	AIN4	CH8
1001	AIN5	AIN5	AIN5	CH9
1010	AIN6	AIN6	AIN6	CH10
1011	AIN7	AIN10	AIN13	CH11
1100	AIN8	AIN11	AIN14	CH12
1101	AIN9	AIN12	AIN15	CH13
1110	-	-	-	CH14
1111	-	-	-	CH15

13.3.3 AD*n*.CR1 ADC*n* Control Register 1

ADC Control Registers are 16-bit registers.

ADC period register

AD0.CR1=0x4000_B008, AD1.CR1=0x4000_B108, AD2.CR1=0x4000_B208

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCPDA	CKDIV							ADCPD	EXTCLK	CLKINVT	STSEL				
0	0x00							1	0	0	0x00				
RW	RW							RW	RW	RW	RW				

15	ADCPDA	ADC R-DAC disable to save power Don't set "1" here(it's optional bit)
14 8	CLKDIV[6:0]	ADC clock divider when EXTCLK is '0'. ADC clock = system clock/CLKDIV CKDIV=0 : ADC clock=system clock CKDIV=1 : ADC clock=stop
7	ADCPD	ADC Power Down 0 – ADC normal mode 1 – ADC Power Down mode
6	EXTCLK	Select if ADC uses external clock. 0 – internal clock(CKDIV enabled, PCLK) 1 – external clock(MCCR6)
5	CLKINVT	Divided clock inversion(optional bit) 0 – duty ratio of divided clock is larger than 50% 1 – duty ratio of divided clock is less than 50%
4 0	STSEL[4:0]	Sampling Time Selection ADC Sample & Hold circuit sampling time become (2 + STSEL[4:0]) MCLK cycles Minimum sampling time is 2 MCLK cycle When STSEL[4:0]=11111, sampling channel is always on.

13.3.4 AD*n*.CR2 ADCn Control Register 2

ADC start register. This register 2 is 8-bit register.

AD0.CR2=0x4000_B020, AD1.CR=0x4000_B120, AD2.CR=0x4000_B220,

7	6	5	4	3	2	1	0
			ASTOP				START
0	0	0	0	0	0	0	0
			W				RW

4	ASTOP	0	No
		1	ADC conversion stop (will be clear next @ADC clock) If ASTOP set after conversion cycle start, present conversion would be completed.
0	ASTART	0	No ADC conversion
		1	ADC conversion start (will be clear next @ADC clock) ADCEN should be "1" to start ADC

13.3.5 AD*n*.TRG0 ADC Trigger 0 Channel Register

ADC Trigger 0 registers are 32-bit registers.

ADC Trigger 0 (from MPWM0) channel register

AD0.TRG0=0x4000_B00C, AD1.TRG0=0x4000_B10C, AD2.TRG0=0x4000_B20C

31	30	29–24	23–20	19–16	15–12	11–8	7–4	3–0
		TRG0EN	MP0TRG6	MP0TRG5	MP0TRG4	MP0TRG3	MP0TRG2	MP0TRG1
0	0	0x00	0x0	0x0	0x0	0x0	0x0	0x0
		RW	RW	RW	RW	RW	RW	RW

29 24	**TRG0EN**	Bit-5	0 – MP0TRG6 disable 1 – MP0TRG6 enable
		Bit-4	0 – MP0TRG5 disable 1 – MP0TRG5 enable
		Bit-3	0 – MP0TRG4 disable 1 – MP0TRG4 enable
		Bit-2	0 – MP0TRG3 disable 1 – MP0TRG3 enable
		Bit-1	0 – MP0TRG2 disable 1 – MP0TRG2 enable
		Bit-0	0 – MP0TRG1 disable 1 – MP0TRG1 enable
23 20	**MP0TRG6**		ADC trigger channel number for MP0ATR6 trigger (Channel number 14 and 15 are prohibited)
19 16	**MP0TRG5**		ADC trigger channel number for MP0ATR5 trigger (Channel number 14 and 15 are prohibited)
15 12	**MP0TRG4**		ADC trigger channel number for MP0ATR4 trigger (Channel number 14 and 15 are prohibited)
11 8	**MP0TRG3**		ADC trigger channel number for MP0ATR3 trigger (Channel number 14 and 15 are prohibited)
7 4	**MP0TRG2**		ADC trigger channel number for MP0ATR2 trigger (Channel number 14 and 15 are prohibited)
3 0	**MP0TRG1**		ADC trigger channel number for MP0ATR1 trigger (Channel number 14 and 15 are prohibited)

13.3.6 AD*n*.TRG1 ADC Trigger 1 Channel Register

ADC Trigger 1 registers are 32-bit registers.

ADC Trigger 1 (from MPWM1) channel register

AD0.TRG1=0x4000_B010, AD1.TRG1=0x4000_B110, AD2.TRG1=0x4000_B210

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		TRG1EN						MP1TRG6				MP1TRG5				MP1TRG4				MP1TRG3				MP1TRG2				MP1TRG1			
0	0	0x00						0x0				0x0				0x0				0x0				0x0				0x0			
RW								RW				RW				RW				RW				RW				RW			

29 24	**TRG1EN**	Bit-5	0 – MP1TRG6 disable 1 – MP1TRG6 enable
		Bit-4	0 – MP1TRG5 disable 1 – MP1TRG5 enable
		Bit-3	0 – MP1TRG4 disable 1 – MP1TRG4 enable
		Bit-2	0 – MP1TRG3 disable 1 – MP1TRG3 enable
		Bit-1	0 – MP1TRG2 disable 1 – MP1TRG2 enable
		Bit-0	0 – MP1TRG1 disable 1 – MP1TRG1 enable
23 20	**MP1TRG6**		ADC trigger channel number by MP1ATR6 trigger (Channel number 14 and 15 are prohibited)
19 16	**MP1TRG5**		ADC trigger channel number by MP1ATR5 trigger (Channel number 14 and 15 are prohibited)
15 12	**MP1TRG4**		ADC trigger channel number by MP1ATR4 trigger (Channel number 14 and 15 are prohibited)
11 8	**MP1TRG3**		ADC trigger channel number by MP1ATR3 trigger (Channel number 14 and 15 are prohibited)
7 4	**MP1TRG2**		ADC trigger channel number by MP1ATR2 trigger (Channel number 14 and 15 are prohibited)
3 0	**MP1TRG1**		ADC trigger channel number by MP1ATR1 trigger (Channel number 14 and 15 are prohibited)

13.3.7 AD*n*.TRG2 ADC Trigger 2 Channel Register

ADC Trigger 2 registers are 32-bit registers.

ADC Trigger 2 channel register

AD0.TRG2=0x4000_B014, AD1.TRG2=0x4000_B114, AD2.TRG2=0x4000_B214

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15-12	11-8	7-4	3-0
																EXTCH	TG3CH	TG2CH	TG1CH
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0	0x0	0x0	0x0
																RW	RW	RW	RW

15 12	**EXTCH**	ADC trigger channel number by External Trigger (Channel number 14 and 15 are prohibited)
11 8	**TG3CH**	ADC trigger channel number by Timer Group 3 trigger (Channel number 14 and 15 are prohibited)
7 4	**TG2CH**	ADC trigger channel number by Timer Group 2 trigger (Channel number 14 and 15 are prohibited)
3 0	**TG1CH**	ADC trigger channel number by Timer Group 1 trigger (Channel number 14 and 15 are prohibited)

ADC	**TIMER TRIGGER SOURCE**		
	Timer Group 1	**Timer Group 2**	**Timer Group 3**
ADC0	TIMER1	TIMER2	-
ADC1	TIMER1	TIMER2	TIMER8
ADC2	TIMER1	TIMER2	TIMER9

13.3.8 ADn.BCSR ADC Burst Mode Channel select

ADC Burst Mode Channel Select Register is 32-bit register.

AD0.BCSR=0x4000_B018, AD1.BCSR=0x4000_B118, AD2.BCSR=0x4000_B218

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BST8CH				BST7CH				BST6CH				BST5CH				BST4CH				BST3CH				BST2CH				BST1CH			
0x0				0x0				0x0				0x0				0x0				0x0				0x0				0x0			
RW				RW				RW				RW				RW				RW				RW				RW			

31 28	BST8CH	8th conversion channel selection in burst mode
27 24	BST7CH	7th conversion channel selection in burst mode
23 20	BST6CH	6th conversion channel selection in burst mode
19 16	BST5CH	5th conversion channel selection in burst mode
15 12	BST4CH	4th conversion channel selection in burst mode
11 8	BST3CH	3rd conversion channel selection in burst mode
7 4	BST2CH	2nd conversion channel selection in burst mode
3 0	BST1CH	1st conversion channel selection in burst mode

13.3.9 ADn.SR ADCn Status Register

ADC Status Register is 32-bit register.

AD0.SR=0x4000_B024, AD1.SR=0x4000_B124, AD2.SR=0x4000_B224

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		MPWM1TRG								MPWM0TRG						ADCH				TRG	BSTAT			ADEND	ABUSY	DOVRUN	DMAIRQ	TIRQ	BIRQ	CIRQ	SIRQ
0	0	0x00						0	0	0x00						0x0				0	000			0	0	0	0	0	0	0	0
R								R								R				R	R			R	R	R	R	R	R	R	R

29 24	MPWM1TRG	This is only Test
21 16	MPWM0TRG	This is only Test
15 12	ADCH	ADC channel bits of present operation
11	TRG	Trigger event status TRG bit set @trigger_event and clear @EOC(end of conversion)
10 8	BSTAT	Burst mode operation count status
7	ADEND	ADC conversion end flag(will be reset @next ADC START)
6	ABUSY	ADC conversion busy flag
5	DOVRUN	DMA overrun flag (not interrupt) (DMA ACK didn’t come until end of next conversion)
4	DMAIRQ	DMA done received (1: DMA transfer is completed) Write “1” to clear flag
3	TIRQ	ADC Trigger interrupt flag (0: no int / 1: int occurred) Write “1” to clear flag
2	BIRQ	ADC Burst interrupt flag (0: no int / 1: int occurred) Write “1” to clear flag
1	CIRQ	ADC Continuous interrupt flag (0: no int / 1: int occurred) Write “1” to clear flag
0	SIRQ	ADC Single interrupt flag (0: no int / 1: int occurred) Write “1” to clear flag

13.3.10 AD*n*.IER Interrupt Enable Register

AD0.IER=0x4000_B028, AD1.IER=0x4000_B128, AD2.IER=0x4000_B228,

7	6	5	4	3	2	1	0
			DIEN	TIEN	BIEN	CIEN	SIEN
0	0	0	0	0	0	0	0
			RW	RW	RW	RW	RW

4	DIEN	DMA done interrupt enable 0: interrupt disable 1: interrupt enable
3	TIEN	ADC trigger conversion interrupt enable
2	BIEN	ADC burst conversion interrupt enable
1	CIEN	ADC continuous conversion interrupt enable
0	SIEN	ADC single conversion interrupt enable

13.3.11 AD*n*.DDR ADC 0/1/2 DMA Data Register

ADC DMA Data Registers are 16-bit registers.

ADC conversion result register for DMA and single conversion (AD data of just completed conversion)

AD0.DDR=0x4000_B02C, AD1.DDR=0x4000_B12C, AD2.DDR=0x4000_B22C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC DMA Data												ADMACH			
0x000												0x0			
R												R			

15 4	ADDMAR	ADC conversion result data (12-bit)
3 0	ADMACH	ADC data channel indicator

13.3.12 ADn.CCR ADC Channel Compare Control Register

ADC Channel Compare Control Registers are 32-bit registers.

ADC channel compare register

AD0.CCR=0x4000_B070, AD1.CCR=0x4000_B170, AD2.CCR=0x4000_B270

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								COMPOUT			LTE	CCH				CVAL															
0	0	0	0	0	0	0	0	0	0	0	0	000				0x000												0	0	0	0
								R			RW	RW				RW															

23	COMPOUT	0	If LTE condition is FALSE
		1	If LTE condition is TRUE (MPWM trigger source)
20	LTE	0	Set compare output when AD conversion value is greater than compare value (CVAL)
		1	Set compare output when AD conversion value is less than or equal to compare value(CVAL)
19 16	CCH	Compare channel	
15 4	CVAL	Compare value	

13.4 Functional Description

There are three ADC in this chip and each ADC has their own three trigger source to start ADC conversion which is TIMER, MPWM and soft trigger(ASTART)

13.4.1 ADC Single mode timing diagram

ADC conversion will be started by ADCn.CR.ASTART written as '1' in single conversion mode. Once ADCnCR.ASTART is set, SOC (start of Conversion) will be activated in 2 ADC clocks and ADCn.SR.SIRQ will be set in 1 ADC clock and 2 PCLKs after the End of Conversion.

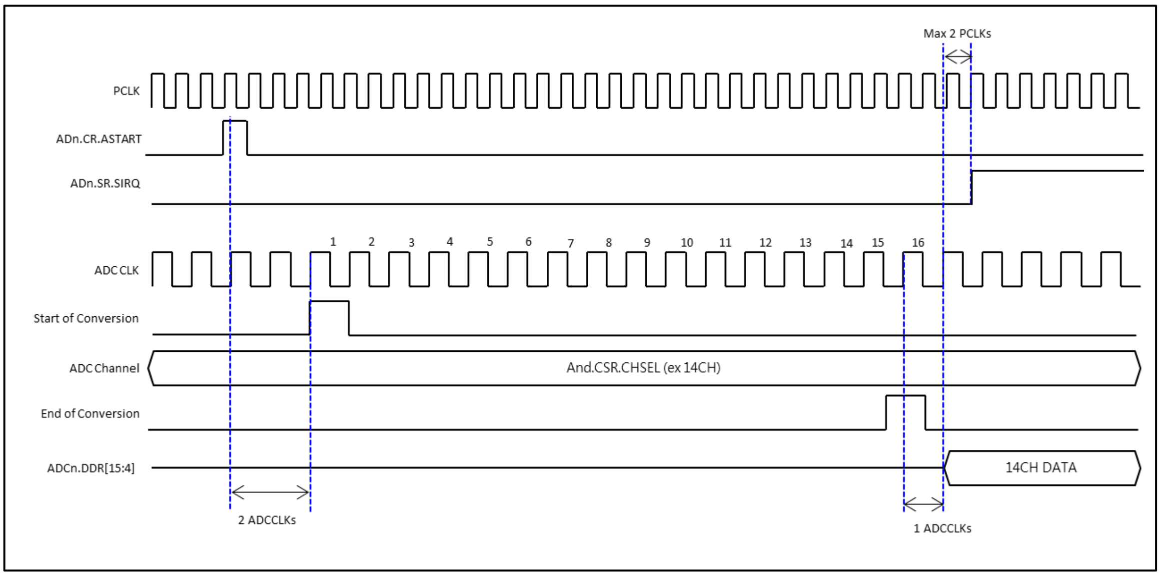


Figure 13.3 ADC Single mode timing

13.4.2 ADC Continuous Mode timing diagram

ADn.SR.CIRQ is set as 1 when every End of Conversion in continuous mode and ADn.SR.CIRQ is cleared by writing the bit. Once ADC conversion start in continuous mode then the ADC keeps running until the mode is off. ADC channel is updated at next conversion if ADnCSR.CHSEL is written.

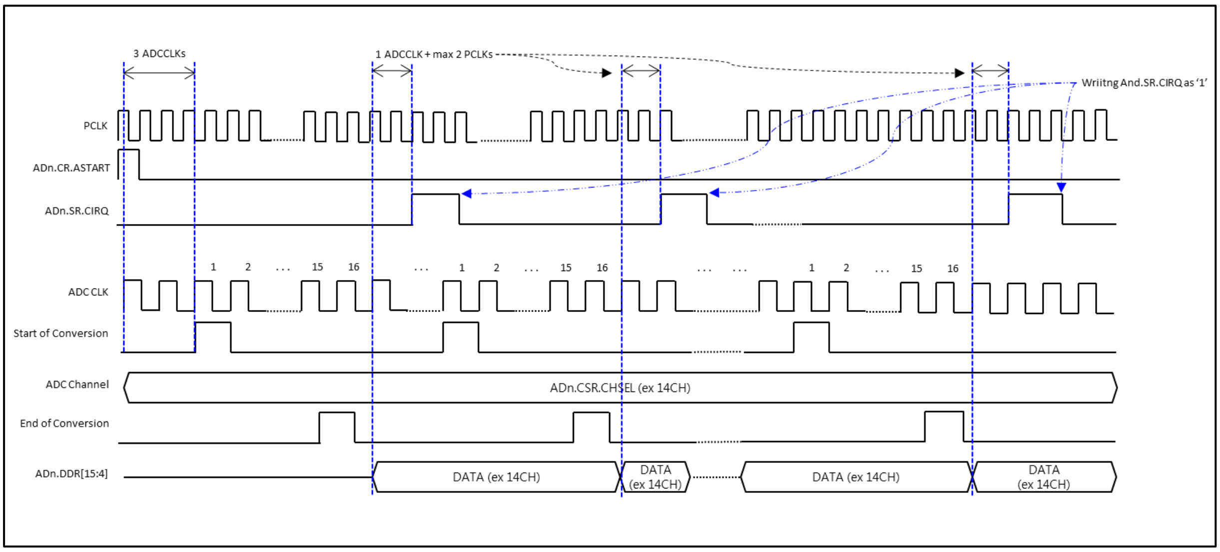


Figure 13.4 ADC Continous mode timing

13.4.3 ADC Burst mode timing diagram

The ADC conversion in burst mode is almost same as continuous mode. Burst mode has ADnCR.BWAIT. BWAIT is 8-bit register and can delay the time of SOC. Burst wait counter(BWAIT) is in ADC clock domain. ADnSR.BIRQ is set as 1 after the last burst operation. See figure 13.5

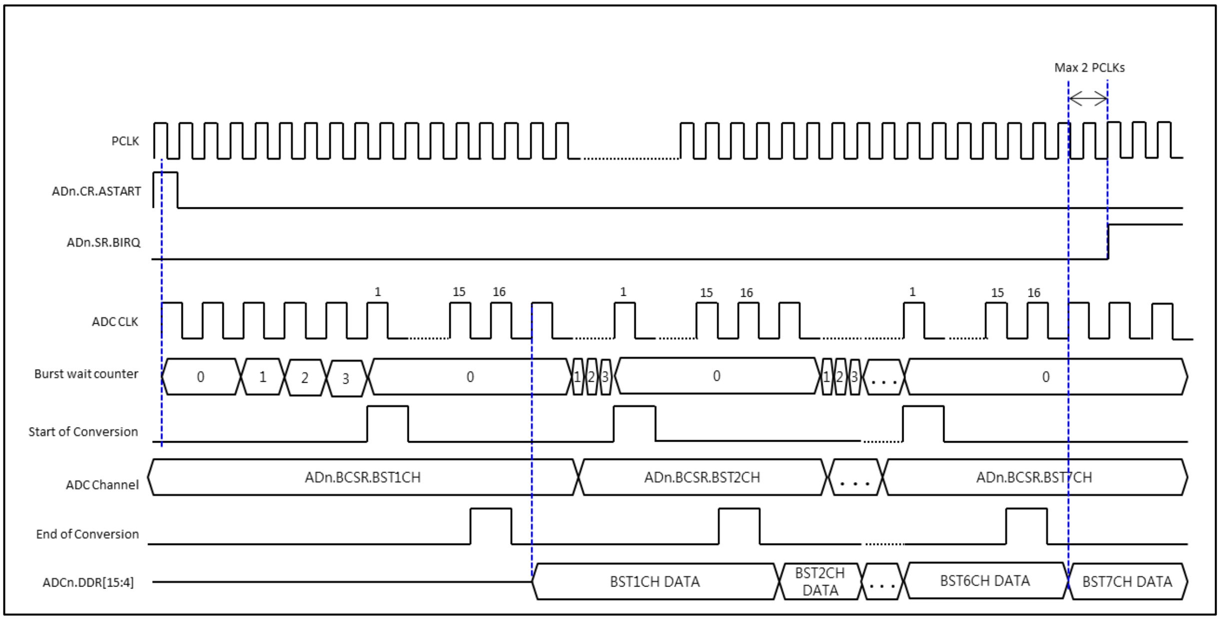


Figure 13.5 ADC Burst mode timing (when ADCn.MR.BWAIT = '8'h3' and BSTCNT = '3'b111')

CHAPTER 14. ANALOG FRONT END (AFE)

14.1 OVERVIEW

AFE(Analog Front End) is OPAMPs and comparators interface controller

- 4 OPAMPs
- 4 Comparators
- OPAMP output can be connected with ADC or comparator
- Internal BGR reference for comparator
- Comparator output de-bounce function
- Level and edge interrupt mode support for comparator

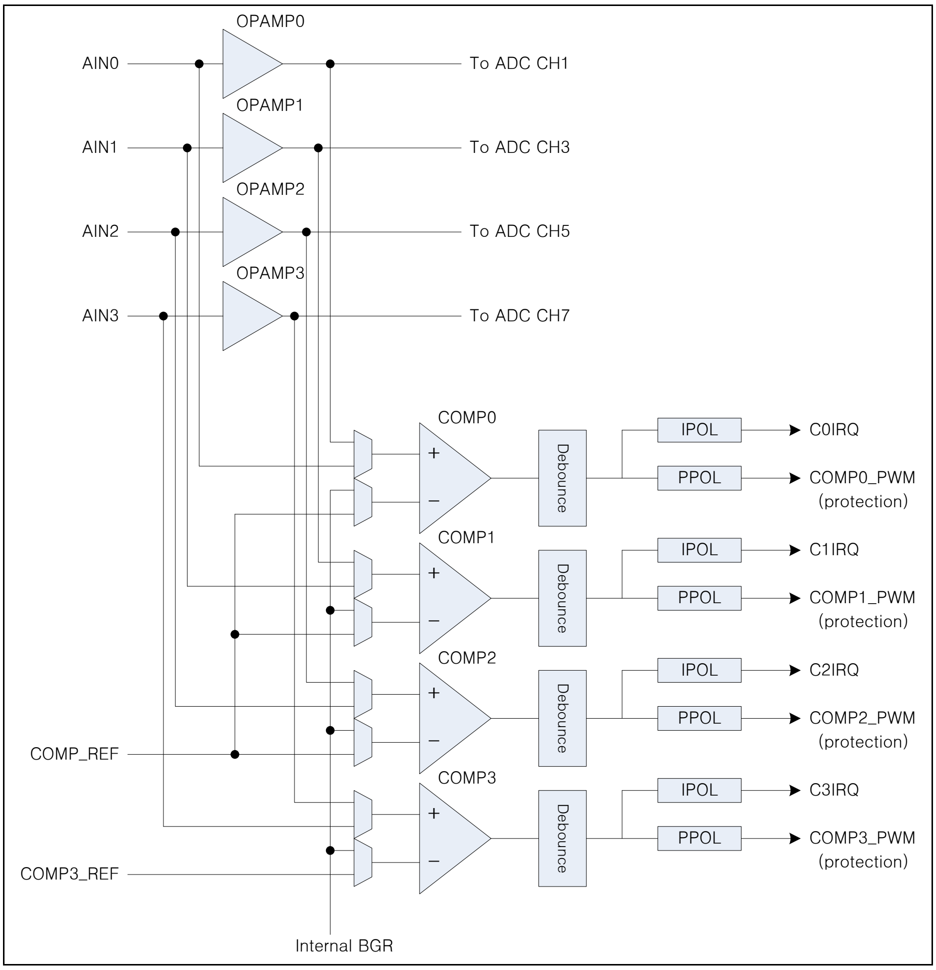


Figure14.1. Block Diagram

14.2 Pin description

Table14.1. External Signal

PIN NAME	TYPE	DESCRIPTION
AVDD	P	Analog Power (3.0V~VDD)
AVSS	P	Analog GND
CP0	A	Comparator Input 0
CP1	A	Comparator Input 1
CP2	A	Comparator Input 2
CP3	A	Comparator Input 3
CREF0	A	Comparator Reference Input 0
CREF3	A	Comparator Reference Input 3

14.3 REGISTERS

Base address of AFE is below.

Table 14.2. AFE base address

NAME	BASE ADDRESS
AFE	0x4000_B300

Table 14.3 shows Register memory map .

Table 14.3. AFE Register map

NAME	OFFSET	TYPE	DESCRIPTION	RESET VALUE
OPA0.CR	0x0000	RW	AFE OPAMP 0 control register	0x00
OPA1.CR	0x0004	RW	AFE OPAMP 1 control register	0x00
OPA2.CR	0x0008	RW	AFE OPAMP 2 control register	0x00
OPA3.CR	0x000C	RW	AFE OPAMP 3 control register	0x00
CMP0.CR	0x0020	RW	AFE Comparator 0 control register	0x10
CMP1.CR	0x0024	RW	AFE Comparator 1 control register	0x10
CMP2.CR	0x0028	RW	AFE Comparator 2 control register	0x10
CMP3.CR	0x002C	RW	AFE Comparator 3 control register	0x10
CMP.DBR	0x0030	RW	AFE Comparator de-bounce register	0x00
CMP.ICR	0x0034	RW	AFE Comparator interrupt control	0x00
CMP.IER	0x0038	RW	AFE Comparator interrupt enable	0x00
CMP.SR	0x003C	R	AFE Comparator status register	0x00

14.3.1 OPAn.CR OPAMP 0/1/2/3 Control Registers

Analog-front-end OPAMP 0/1/2/3 Control Registers are 8-bit registers.
AFE OPAMP control registers. All four registers(AFEOPA0~AFEOPA3) have the same functions.

OPA0.CR=0x4000_B300, OPA1.CR =0x4000_B304
OPA2.CR =0x4000_B308, OPA3.CR =0x4000_B30C

7	6	5	4	3	2	1	0
			OPAEN	GAIN			
0	0	0	0	0x0			
			RW	RW			

4	OPAEN	0	OPAMP n Disable		
		1	OPAMP n Enable		
3 0	GAIN	0000	Gain = 2.19	1000	Gain = 4.37
		0001	Gain = 2.33	1001	Gain = 5.0
		0010	Gain = 2.5	1010	Gain = 5.83
		0011	Gain = 2.69	1011	Gain = 7.0
		0100	Gain = 2.92	1100	Gain = 8.74
		0101	Gain = 3.18	1101	Reserved
		0110	Gain = 3.5	1110	Reserved
		0111	Gain = 3.89	1111	Gain = 1.00

14.3.2 CMPn.CR Comparator 0/1/2/3 Control Register

Analog-front-end Comparator0/1/2/3 Control Registers are 8-bit registers.
AFE Comparator control registers. All four registers(AFECOMP0~AFECOMP3) have the same functions.

CMP0.CR=0x4000_B320,CMP1.CR =0x4000_B324
CMP2.CR =0x4000_B328, CMP3.CR =0x4000_B32C

7	6	5	4	3	2	1	0
			CMPEN			CINSEL	REFSEL
0	0	0	1	0	0	0	0
			RW			RW	RW

4	CMPEN	0	Comparator 0~3 Enable
		1	Comparator 0~3 Disable
1	CINSEL		Comparator input selection
		0	Input from OPAMP 0~3 each
		1	Input from external pin (see pin mux table)
0	REFSEL		Comparator reference selection
		0	Reserved
		1	REF input from external pin (see pin mux table)

When OPAMP is disable, OPAMP output is unknown(floating), so user should set(write 1) CINSELx to choose external input when OPAMP is inactive state.

14.3.3 CMP.DBR Comparator de-bounce Register

Analog-front-end Comparator Debounce Register is 32-bit register

CMP.DBR=0x4000_B330

31	30	29	28	27	26	25	24	23-16	15-12	11-8	7-4	3-0
								DBNCTB	C3DBNC	C2DBNC	C1DBNC	C0DBNC
0	0	0	0	0	0	0	0	0x00	0x0	0x0	0x0	0x0
								RW	RW	RW	RW	RW

23 16	DBNCTB[3:0]	Debounce time base counter System clock/(DBNCTB *2) becomes shift clock of debounce logic When DBNCTB is 0, system clock would be debounce clock.
15 0	CxDBNC[4:0]	Debounce shift Selection When it is 0x0, debounce function is disable Shift number of debounce logic is (CxDBNC + 1) when CxDBNC is more than 1.

14.3.4 CMP.ICR Comparator Interrupt Control Register

Analog-front-end Comparator Interrupt Control Register is 16-bit Register.

CMP.ICR=0x4000_B334

15	14	13	12	11	10	9	8	7-6	5-4	3-2	1-0
PPOL3	PPOL2	PPOL1	PPOL0	IPOL3	IPOL2	IPOL1	IPOL0	C3IMOD	C2IMOD	C1IMOD	C0IMOD
-	-	-	-	-	-	-	-	00	00	00	00
R	R	R	R	R	R	R	R	RW	RW	RW	RW

15 14 13 12	PPOL3 PPOL2 PPOL1 PPOL0	0	Comparator outs for PWM protection will not be inverted
		1	Comparator outs for PWM protection will be inverted (if debounce is enable, debounced output will be inverted)
11 10 9 8	IPOL3 IPOL2 IPOL1 IPOL0	0	When comparator output is high, IRQ bit is set (CxIMODE = 00)
		1	When comparator output is low, IRQ bit is set (CxIMODE = 00)
3 2 1 0	C3IMODE C2IMODE C1IMODE C0IMODE	00	Comparator interrupt mode IRQ at level output
		01	IRQ at rising edge of comparator output
		10	IRQ at falling edge of comparator output
		11	IRQ at both edge of comparator output

14.3.5 CMP.IER Comparator Interrupt Enable Register

Analog-front-end interrupt enable register is 8-bit register.

CMP.IER=0x4000_B338

7	6	5	4	3	2	1	0
				CMP3IE	CMP2IE	CMP1IE	CMP0IE
0	0	0	0	0	0	0	0
				RW	RW	RW	RW

3	CMP3IE	AFE comparator 3 interrupt enable 0 –interrupt disable 1 –interrupt enable
2	CMP2IE	AFE comparator 2 interrupt enable 0 –interrupt disable 1 –interrupt enable
1	CMP1IE	AFE comparator 1 interrupt enable 0 –interrupt disable 1 –interrupt enable
0	CMP0IE	AFE comparator 0 interrupt enable 0 –interrupt disable 1 –interrupt enable

14.3.6 CMP.SR Comparator Status Register

Analog-front-end Status register is 16-bit register.

CMP.SR=0x4000_B33C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C3RAW	C2RAW	C1RAW	C0RAW	C3OUT	C2OUT	C1OUT	C0OUT					C3IRQ	C2IRQ	C1IRQ	C0IRQ
-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R					RC1	RC1	RC1	RC1

15 12	C3RAW C2RAW C1RAW C0RAW	AFE comparator raw outputs These values come from comparator output pin (before debouncing)
11 8	C3OUT C2OUT C1OUT C0OUT	AFE comparator output monitor bit These values are debounced outputs.
3 0	C3IRQ C3IRQ C2IRQ C0IRQ	AFE comparator interrupt flag (0: no int / 1: int occurred) Write “1” to clear flag

SECTION 3.CHARACTERISTIC

CHAPTER 1. Electrical Characteristic

Electrical Characteristic

1.1 DC Characteristics

1.1.1 Absolute Maximum Ratings

Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions..

Table1.1. Absolute maximum rating

Parameter		Symbol	min	max	unit
Power Supply (V_{DD})		V_{DD}	-0.5	+6	V
Analog Power Supply (AV_{DD})		AV_{DD}	-0.5	+6	V
Input High Voltage			-	V_{DD}+0.5	V
Input Low Voltage			V_{SS}–0.5	-	V
Output Low Current per pin		I_{OL}	-	20	mA
Output Low Current Total	80-pin	$\sum I_{OL}$	-	100	mA
	64-pin	$\sum I_{OL}$	-	80	
Output High Current per pin		I_{OH}	-	-10	mA
Output High Current Total	80-pin	$\sum I_{OH}$	-	100	mA
	64-pin	$\sum I_{OH}$	-	80	
Input Main Clock Range			0.4	10	MHz
Operating Frequency			-	72	MHz
Storage Temperature		T_{ST}	-55	+125	℃
Operating Temperature		T_{OP}	-40	+85	℃

1.1.2 DC Characteristics

Table 1.2 Recommended Operating Condition

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Supply Voltage	VDD		3.0		5.5	V
Supply Voltage	AV_{DD}		3.0	5.0	5.5	V
Operating Frequency	f	OSC_{MAIN}	4		8	MHz
		OSC_{INT}		20		MHz
		PLL	4		72	MHz
Operating Temperature	T_{OP}	T_{OP}	-40		+85	℃

Table 1.3 DC Electrical Characteristics (VDD = +5V, Ta = 25 ℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Input Low Voltage	V_{IL}	Schmitt input	-	-	0. $2V_{DD}$	V
Input High Voltage	V_{IH}	Schmitt input	$0.8V_{DD}$	-	-	V
Output Low Voltage	V_{OL1}	I_{OL1} = 10mA All output ports except V_{OL2}	-	-	V_{SS} +1.0	V
	V_{OL2}	I_{OL2} = 3mA PA0-PA6,PB6-PB7, PC4,PC7,PC8,PC10- PC13,PD0-PD3, PD10,PD11,PD14, PD15	-	-	V_{SS} +1.0	V
Output High Voltage	V_{OH1}	I_{OH1} = -3mA All output ports except V_{OH2}	V_{DD} –1.0	-	-	V
	V_{OH2}	I_{OH2} = -1.2mA PA0-PA6,PB6-PB7, PC4,PC7,PC8,PC10- PC13,PD0-PD3, PD10,PD11,PD14, PD15	V_{DD} –1.0	-	-	V
Input High Leakage	I_{IH}				4	µA
Input Low Leakage	I_{IL}		-4			µA
Pull-up Resister	R_{PU}	R_{MAX}:V_{DD}=3.0V R_{MIN}:V_{DD}=5V	30	-	70	kΩ

1.1.3 Current Consumption

Table1.4 Current consumption in each mode (Temperature: +25℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Normal Operation	$I_{DD\ NORM}$	OSC_{RING} =RUN IOSC20=RUN OSC_{MAIN} =8MHz HCLK=72MHz	-	35	-	mA
Sleep Mode	$I_{DD\ SLEEP}$	OSC_{RING} =RUN IOSC20=RUN OSC_{MAIN} =STOP HCLK =RUN	-	3	-	mA

1.1.4 POR Electrical Characteristics

Table1.5 POR Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating Voltage	V_{DD18}		1.6	1.8	2.0	V
Operating Current	I_{DD}	Typ. <6µA If always on	-	60	-	nA
POR Set Level	V_{RISING}	V_{DD} rising (slow)	1.3	1.4	1.55	V
POR Reset Level	$V_{FALLING}$	V_{DD} falling (slow)	1.1	1.2	1.4	V

1.1.5 LVD Electrical Characteristics

Table1.6 LVD Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating Voltage	V_{DD}		1.7		5	V
Operating Current	I_{DD}	Typ. <6µA when always on	-	1	-	mA
LVD Set Level 0	V_{LVD0}	V_{DD} falling (slow)	1.6	1.8	2.0	V
LVD Set Level 1	V_{LVD1}	V_{DD} falling (slow)	2.0	2.2	2.5	V
LVD Set Level 2	V_{LVD2}	V_{DD} falling (slow)	2.5	2.7	3.0	V
LVD Set Level 3	V_{LVD3}	V_{DD} falling (slow)	3.9	4.3	4.6	V

1.1.6 VDC Electrical Characteristics

Table1.7VDC Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating Voltage	V_{DD}		3.0	-	5.5	V
VDC Output Voltage	V_{OUT}	@RUN	1.62	1.8	1.98	V
		@STOP	1.4	1.8	2.0	V
Regulation Current	I_{OUT}				100	mA
Drop-out Voltage	V_{DROP}	VDDVDC=3.0V IOUT=100mA	-	-	200	mV
Current Consumption	$I_{DD\ NORM}$	@RUN	-	100	150	μA
	$I_{DD\ STOP}$	@STOP	-	1	2	μA

1.1.7 External OSC Characteristics

Table1.8External OSC Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ	Max	unit
Operating Voltage	V_{DD}		3.0	-	5.5	V
IDD	I_{DD}	@4MHz/5V	-	240		μA
Frequency	f_{osc}		4	8	10	MHz
Output Voltage	V_{OUT}		1.2	2.4	-	V
Load Capacitance	C_L		5	22	35	pF

1.1.8 Internal RC OSC Characteristics

Table 1.9 Internal RC OSC Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ	Max	unit
Operating Voltage	V_{DD}		3.0		5.5	V
IDD	I_{OSC}	@20MHz	-	240		μA
Frequency	f_{IOSC}			20		MHz

1.1.9 PLL Electrical Characteristics

Table1.10PLL Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating Voltage	V_{DD}		3.0		5.5	V
Output Frequency	f_{OUT}		4		72	MHz
Operating Current	I_{DD}	@72MHz		1.3		mA
Duty	f_{DUTY}		40	-	60	%
P-P Jitter	JITTER	@Lock			500	Ps
VCO	VCO		30		72	MHz
Input Frequency	f_{IN}		4		8	MHz
Locking time	t_{LOCK}				1	ms

1.1.10 ADC Electrical Characteristics

Table 1.11ADC Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating Voltage	AV_{DD}		3.0	5	5.5	V
Reference Voltage	AV_{REF}		3.0	5	5.5	V
Resolution				12		Bit
Operating Current	AI_{DD}				2.8	mA
Analog Input Range			0		AV_{DD}	V
Conversion Rate				-	1.6	Msps
Operating Frequency	f_{ACLK}				25	MHz
DC Accuracy	INL			±2.5		LSB
	DNL			±1.0		LSB
Offset Error				±1.5		LSB
Full Scale Error				±1.5		LSB
SNDR	SNDR			68		dB
THD				-70		dB

1.1.11 OP-Amp Electrical Characteristics

Table 1.12 ADC Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating Voltage	AV_{DD}		3.0	5	5.5	V
Operating Current	AI_{DD}				2.2	mA
Analog Input Range			0		AV_{DD}-1.4	V
Slew Rate		@ C_L = 20pF		15		V/µs
Gain Error		Gain=2.19~4.37	-3		+3	%
		Gain=5.0~8.74	-4		+4	%
Common Mode Rejection Ratio			50	70		dB
Power Supply Rejection Ratio			40	70		dB
Gain Bandwidth		@C_L=20pF		16		MHz
Open Loop Voltage Gain				100		dB
Open Loop Phase Margin		@C_L=20pF		45		°
Closed Loop Phase Margin				70		°
Turn On time	t_{ON}			2		µs
Gain			2.19		8.74	

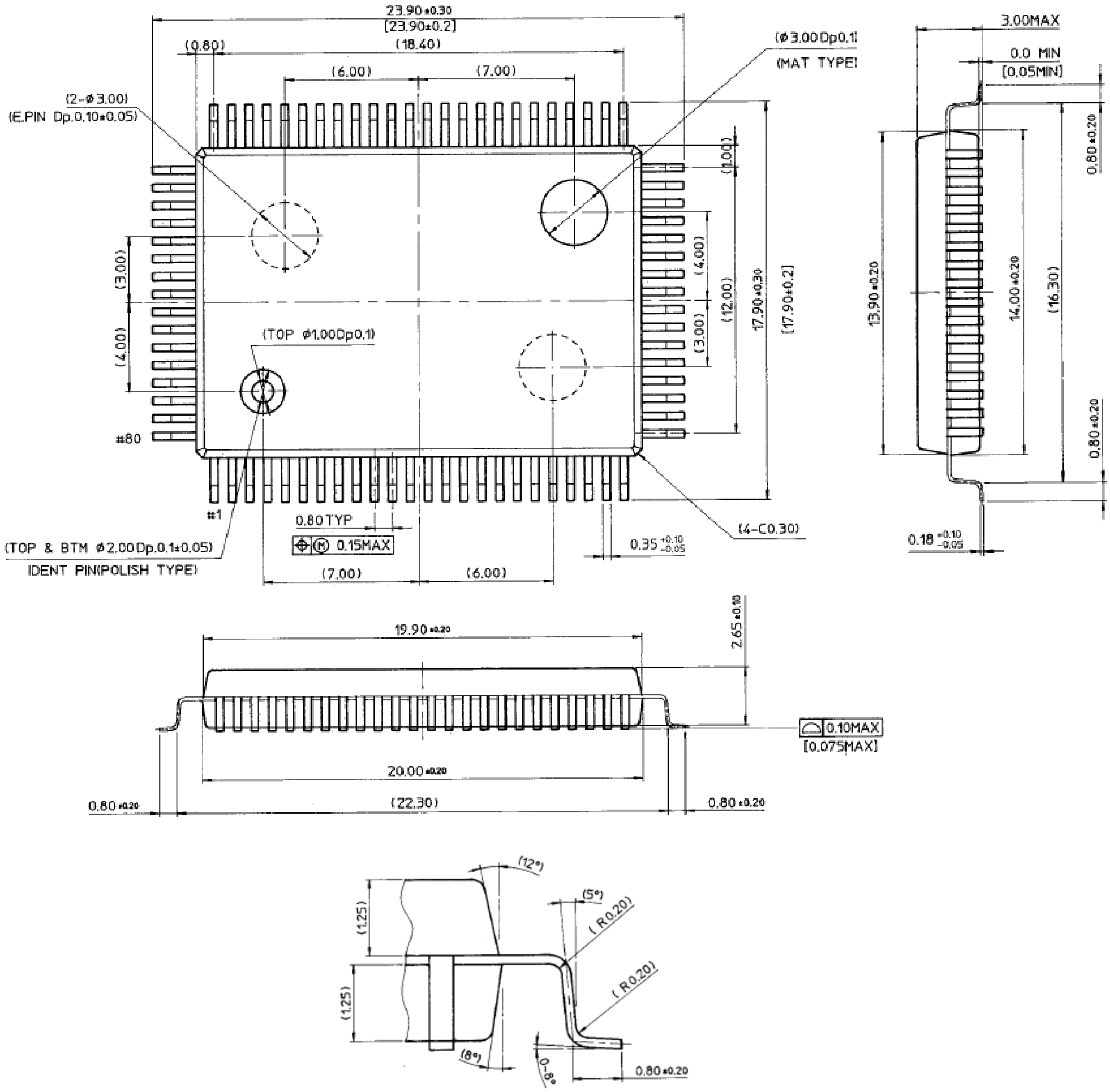
1.1.12 Comparator Electrical Characteristics

Table 1.13 Comparator Electrical Characteristics (Temperature: -40 ~ +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating Voltage	AV_{DD}		3.0	5	5.5	V
Analog Input Range	V_{IN}		AV_{SS}		AV_{DD}	V
Reference Input Range	V_{REF}		0.9		AV_{DD}-0.2	V
Input Offset Voltage			-4		+4	%
Response Time					1	µs

CHAPTER 2. Package

2.1 MQFP-80 Package dimension

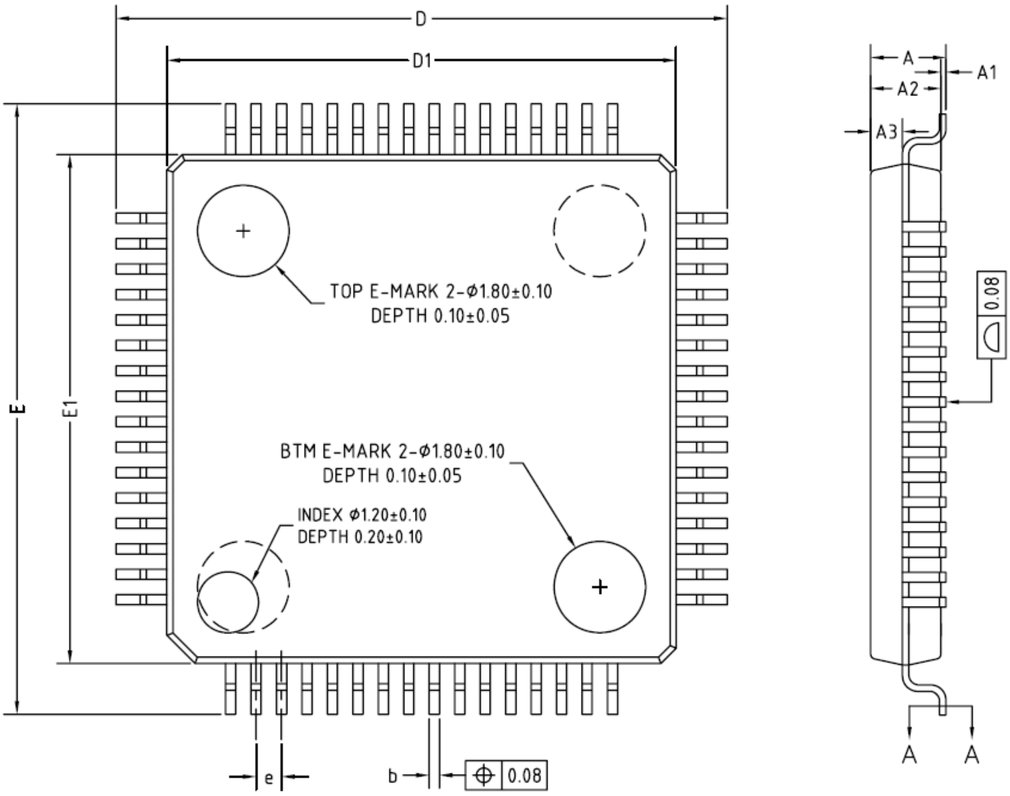


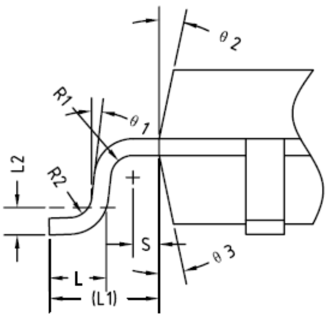
NOTES:

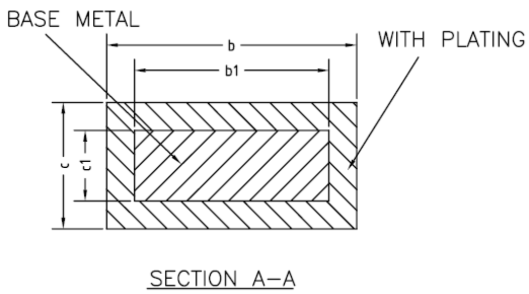
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026 BDD DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS

Figure 2.1. Package dimension (MQFP-80 14X20)

2.2 LQFP-80 Package dimension







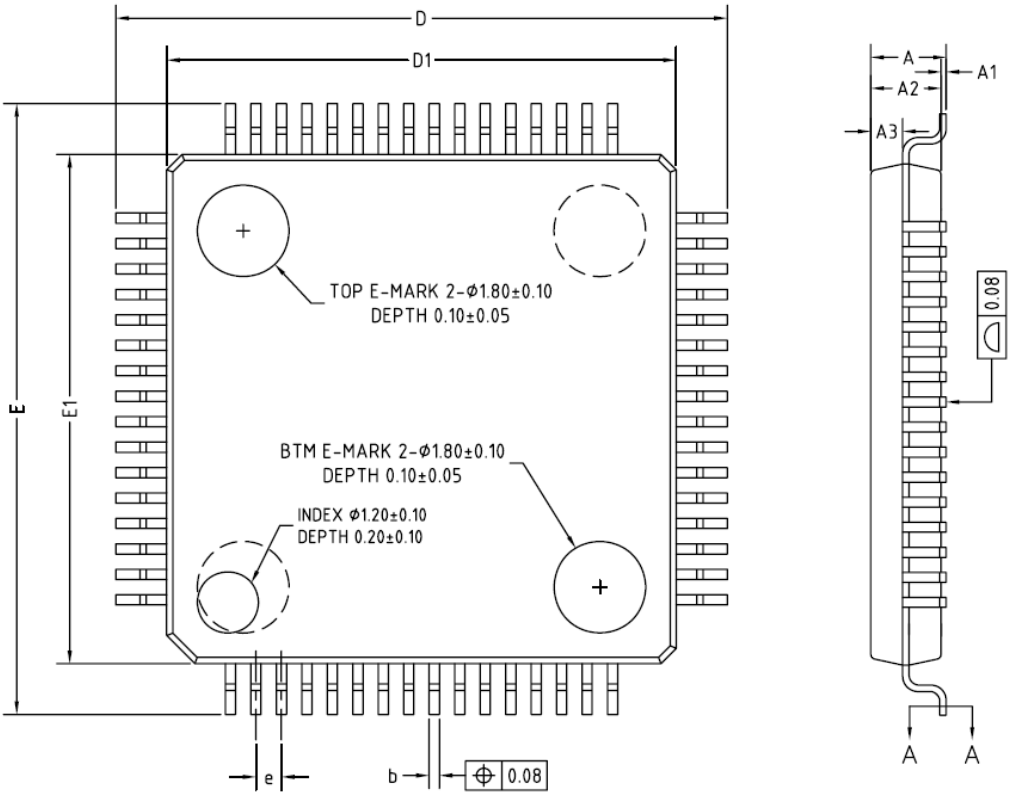
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

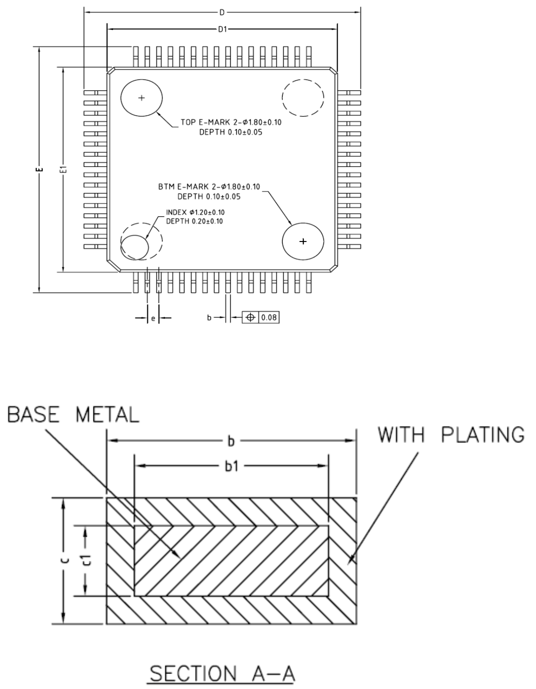
SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	–	–
R2	0.08	–	0.20
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026 BDD DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS

Figure 2.2. Package dimension (LQFP-80 12X12)

2.3 LQFP-64 Package dimension





COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e		0.50BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026 BDD DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS

Figure 2.3. Package dimension (LQFP-64 10X10)

Korea

Regional Office, Seoul
R&D, Marketing & Sales
8th Fl., 330, Yeongdong-daero,
Gangnam-gu, Seoul,
06177, Korea

Tel: +82-2-2193-2200
Fax: +82-2-508-6903
www.abovsemi.com

HQ, Ochang
R&D, QA, and Test Center
93, Gangni 1-gil, Ochang-eup, Cheongwon-gun,
Chungcheongbuk-do,28126, Korea

Tel: +82-43-219-5200
Fax: +82-43-217-3534
www.abovsemi.com

Domestic Sales Manager
Tel: +82-2-2193-2206
Fax: +82-2-508-6903
Email: sales_kr@abov.co.kr

Global Sales Manager
Tel: +82-2-2193-2281
Fax: +82-2-508-6903
Email: sales_gl@abov.co.kr

China Sales Manager
Tel: +86-755-8287-2205
Fax: +86-755-8287-2204
Email: sales_cn@abov.co.kr