A31G112, A31G111
User's Manual

General Purpose Cortex-M0+ Microcontroller
Flash 32KB, SRAM 4KB, ADC, LCD Driver

User's Manual Version 1.40

Introduction

This user's manual contains complete information for application developers who use A31G112 or A31G111 for their specific needs.

The A31G11x series is a 32-bit general purpose microcontroller for various appliances. To meet the requirements for the complexity and high performance in consumer electronics, the A31G11x series incorporates ARM's high-speed 32-bit Cortex-M0+ Core, and has a flash memory of up to 32 KB and an SRAM of 4 KB.

As shown in the following figure, the A31G11x series has various peripherals such as 16-bit timers, 32-bit timers, a 16-bit timer with 6-channel PWM, 12-bit ADC, CRC generator, UART, USART, I2C, LCD driver/controller, etc. The A31G11x series also has a POR, LVR, LVI, and an internal RC oscillator. The A31G11x series support sleep and deep sleep modes to reduce power consumption.

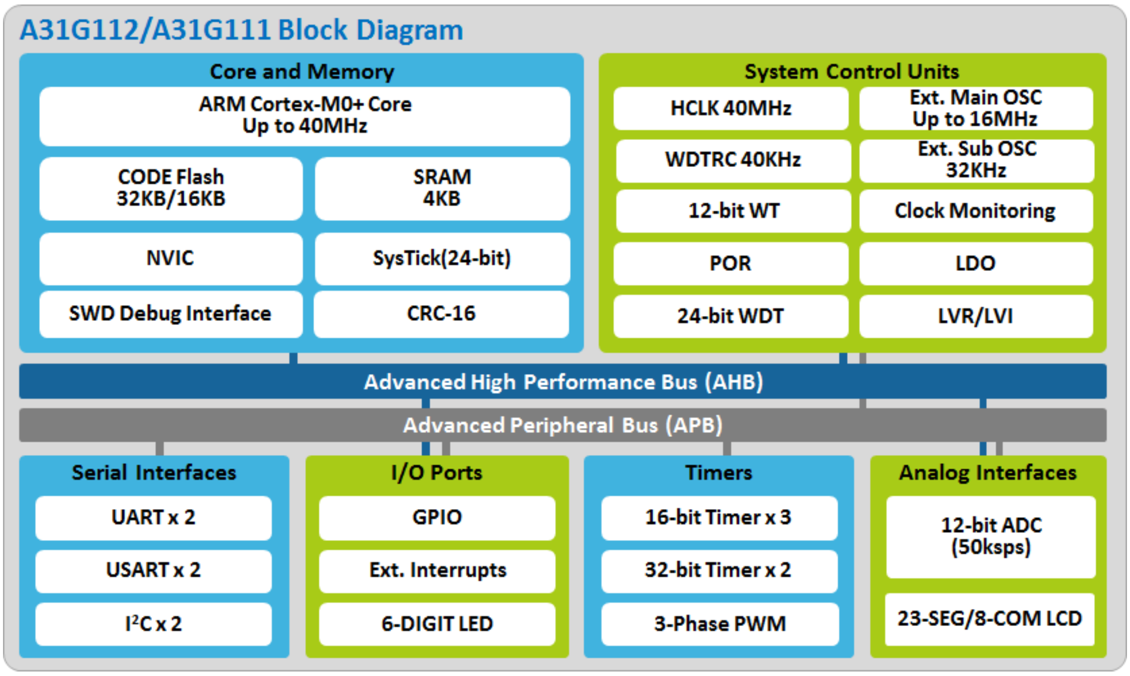

Figure 1. A31G11x series Block Diagram

Reference document

- A31G11X datasheet includes production data and features.
- A31G11x application note includes an overview of hardware implementation of A31G11x.

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1 Description

The A31G11x series is a microcontroller based on ARM Cortex-M0+ core with a flash memory of up to 32KB, and an SRAM of 4KB. Operation voltage of the device is 1.8V to 5.5V. It provides a highly flexible and cost effective solution for many embedded control applications.

The A31G11x series has 16-bit timers, 32-bit timers, a 16-bit timer with 6-channel PWM, 12-bit ADC, CRC generator, UART, USART, I2C, LCD driver/controller, etc. The A31G11x series also has a POR, LVR, LVI, and an internal RC oscillator. The A31G11x series support sleep and deep sleep modes to reduce power consumption.

1.1 Device overview

Table 1. A31G11x series features and peripheral counts

Device Peripheral	A31G11x
CPU	Cortex-M0+
Flash ROM (Kbytes)	32
SRAM (bytes)	4KB
LED Display Drive Capability	Max. 120mA of sink current capability for output of 6 pins (PD0 to PD5)
I/O	45 programmable
Timers	Watchdog timer
	Six general purpose timers — Periodic, one-shot, PWM, capture mode
LCD driver	• 23 segments and 8 commons • Duty selectable, resistor bias • 16-step contrast control
ADC	11-channel input, 12-bit ADC with 50ksps
CRC generator	16-bit CRC generator, CRC-16, CRC-CCITT
External communication ports	• 2 USARTs (UART + SPI) • 2 I^{2}C • 2 UART
System fail-safe function	Clock monitoring
Debug interface	SWD debug interface
Packages	• LQFP 48-0707 (0.5mm pitch) • MQFP 44-1010 (0.8mm pitch) • LQFP 32-0707 (0.8mm pitch) • QFN 32-0505 (0.5mm pitch) • TSSOP 28 (0.65mm pitch) • QFN 24-0404 (0.5mm pitch)
Operating temperature	• -40℃ to +85℃ (commercial grade) • -40℃ to +105℃ (Industrial grade)

1.2 Block diagram

Figure 2 shows a block diagram of A31G11x series.

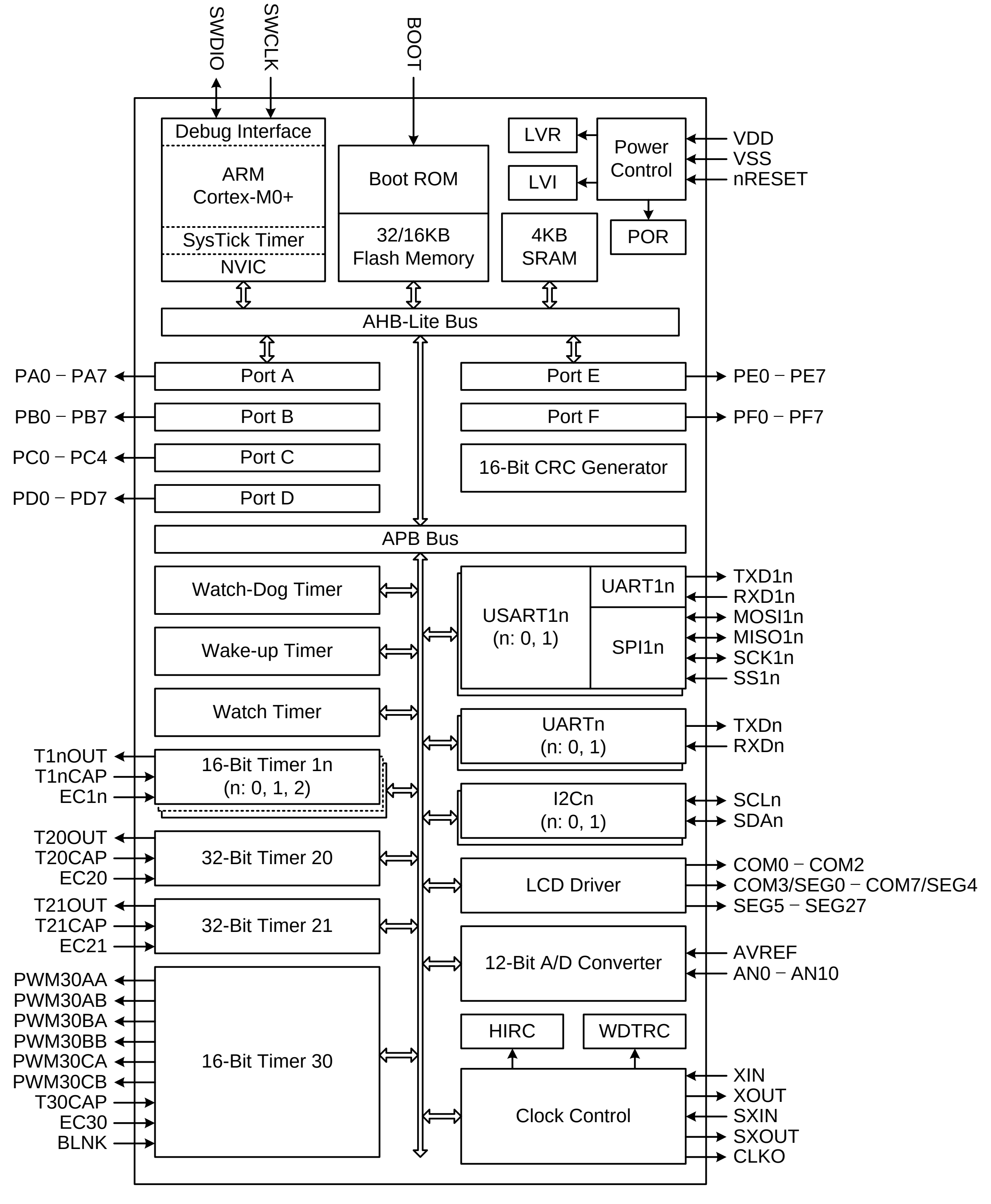


Figure 2. A31G11x series Block Diagram

1.3 Functional description

Main features of A31G11x series are summarized below:

1.3.1 ARM Cortex-M0+

Cortex-M0+ processor has very low gate count characteristic and high energy efficiency. It is developed for microcontrollers and deeply embedded applications that require an area-optimized and low-power processor.

The core system timer (SYSTICK) provides a simple 24-bit timer, which can be used for a real time operating system (RTOS). It can be used as a simple counter too.

The Cortex-M0+ processor implements the ARMv6-M Thumb instruction set, including a number of 32-bit instructions that use Thumb-2 technology. Hardware single-cycle multiplication is available. Integrated Nested Vectored Interrupt Controller (NVIC) provides deterministic interrupt handling, and SWD debugging features offer the MCU emulation.

1.3.2 Nested vector-interrupt controller (NVIC)

External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt.

The NVIC embedded in the Cortex-M0+ processor core is capable of processing low latency interrupts and efficient processing of late arriving interrupts. All NVIC registers are accessible only using word transfers.

1.3.3 32KB/16KB internal code flash memory

A31G11x series has built-in code flash memory of 32KB or 16KB. It supports self-programming feature, and supports ISP and JTAG programming in boot or debug mode.

1.3.4 4KB internal SRAM

On-chip 4KB SRAM is used as a working memory space and as a program code area temporarily.

1.3.5 Boot logic

A boot logic supports flash programming. The boot logic will be activated when the external boot pin was set to boot mode.

1.3.6 System Control Unit (SCU)

An SCU block manages internal power, clock, reset and operation mode. It also controls the analog blocks (Oscillator Block, VDC and LVR).

1.3.7 24-bit Watchdog timer (WDT)

A Watchdog timer monitors the system. It generates internal reset or interrupt to notice abnormal status of the system.

1.3.8 Multi-purpose 16-bit timer and 32-bit timer

Three-channel 16-bit and two-channel 32-bit general-purpose timers support the functions introduced below:

- Periodic timer mode
- Counter mode
- PWM mode
- Capture mode

1.3.9 16-bit Timer with 6 Channel PWMs

The 16-bit timer has 6 channels of PWMs for 3-phase motor application. 16-bit up/down counter with prescaler supports both triangular and sawtooth waveform.

The PWM has ability to generate internal ADC trigger signal to measure the signal on time.

Dead time insertion and emergency stop functionality make sure that the chip and the system are under a safe condition.

1.3.10 USART (UART and SPI)

USART supports UART and SPI mode. The A31G11x series has 2 channel USART modules.

Boot mode uses this USART block to download flash program.

1.3.11 Inter-Integrated Circuit interface (I2C)

A31G11x series has two channels of I2C block and supports up to 1MHz I2C communication. Master and slave modes are available.

1.3.12 Universal Asynchronous Receiver/Transmitter (UART)

A31G11x series has two channels of UART block. For accurate baud rate control, a fractional baud-rate generation feature is available.

1.3.13 General PORT I/Os (GPIO)

8-bit PA port, 8-bit PB port, 5-bit PC port, 8-bit PD port, 8-bit PE port, and 8-bit PF port are available and provide multiple functions.

- General I/O port
- External interrupt input port and on-chip input debounce filter
- Programmable pull-up, pull-down, and open-drain selection

1.3.14 12-bit Analog-to-Digital Converter (ADC)

An ADC can convert analog signal at a conversion rate of up to 50ksps. 11-channel analog MUX provides various combinations of data from external analog signals.

1.3.15 LCD driver/controller

A LCD driver supports an internal resistor bias, 16-step contrast control, automatic bias control, and various duties.

1.3.16 16-bit Cyclic Redundancy Check (CRC) generator

A31G11x series has two polynomials for the CRC generator: CRC-CCITT and CRC-16.

2 Pinouts and pin descriptions

In chapter 2, pinouts and pin descriptions of A31G11x series are introduced.

2.1 Pinouts

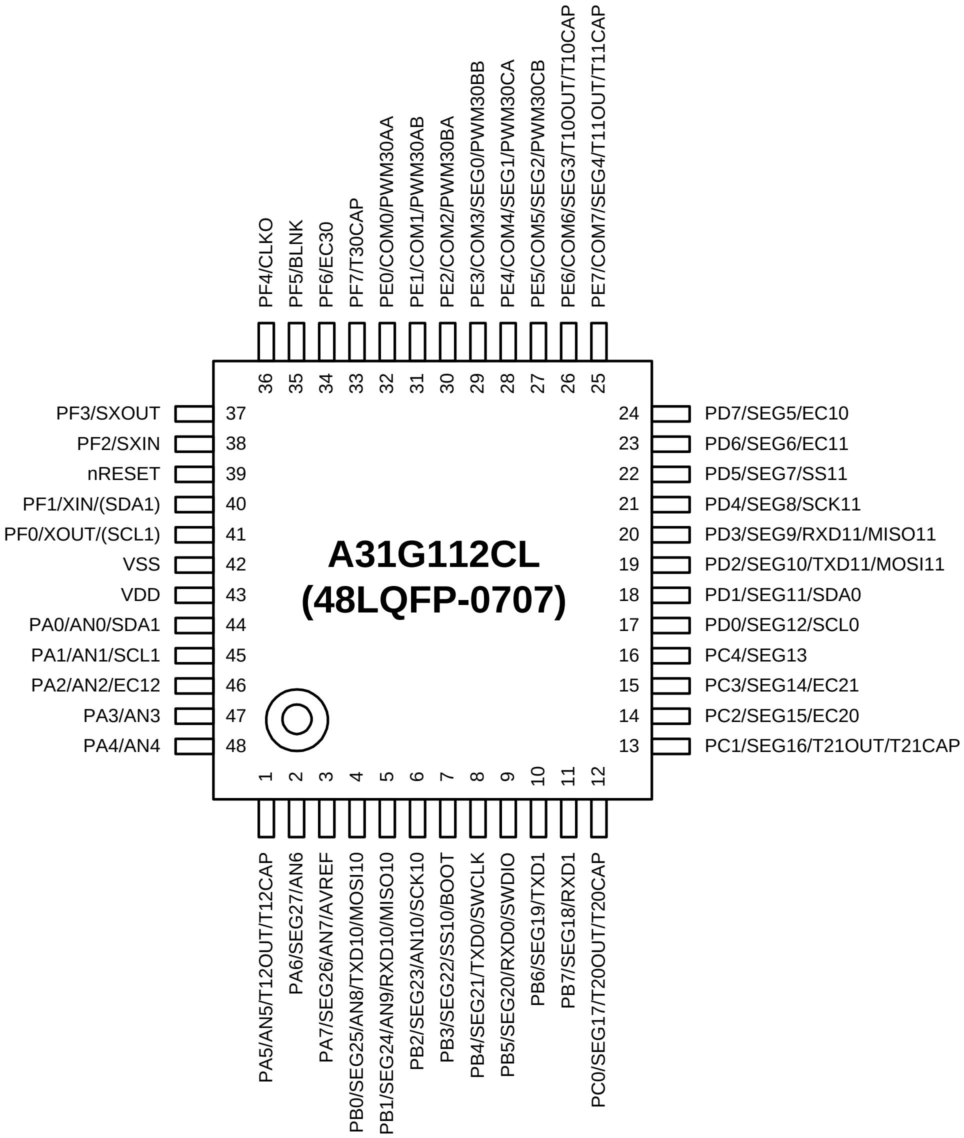
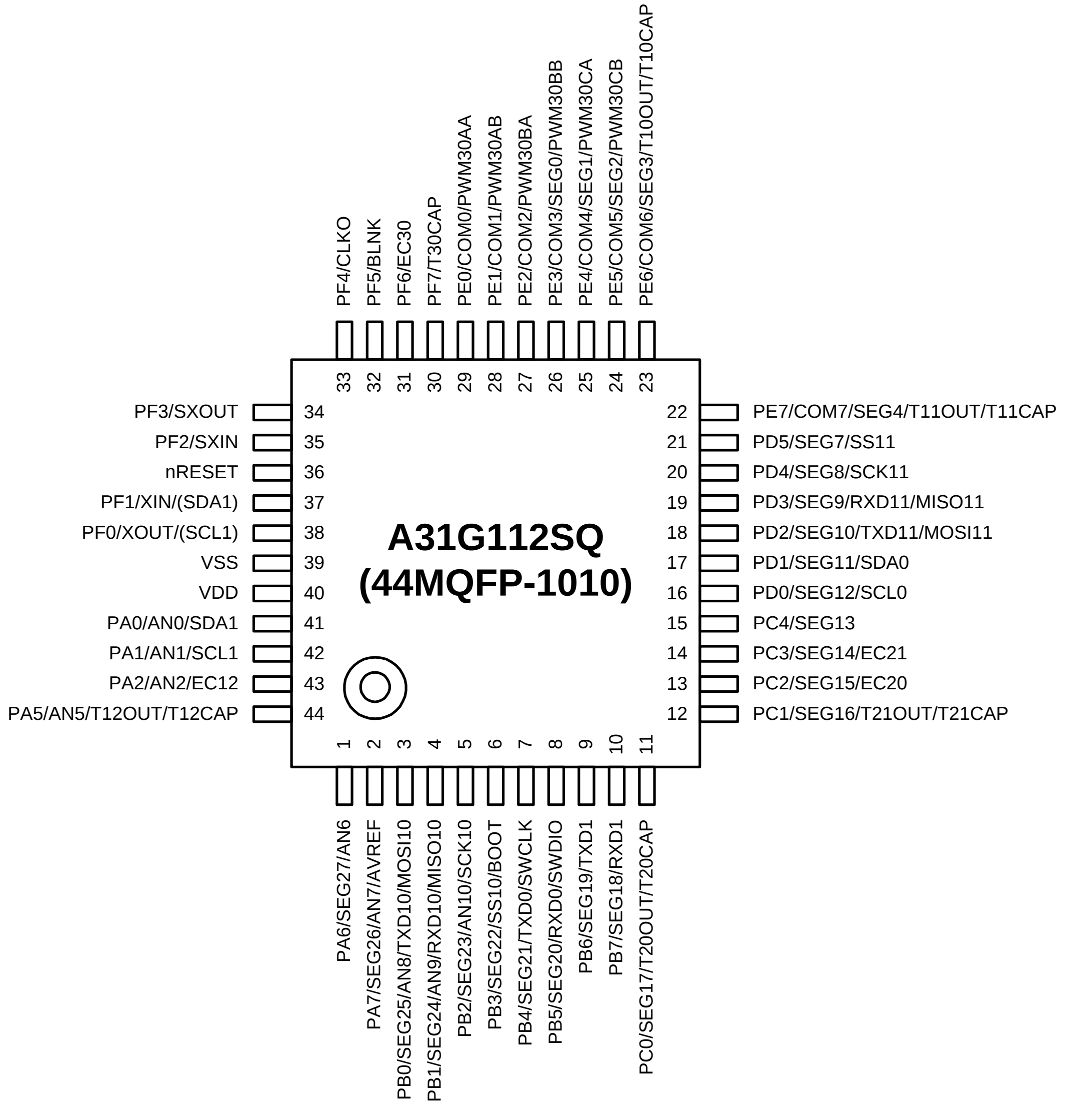
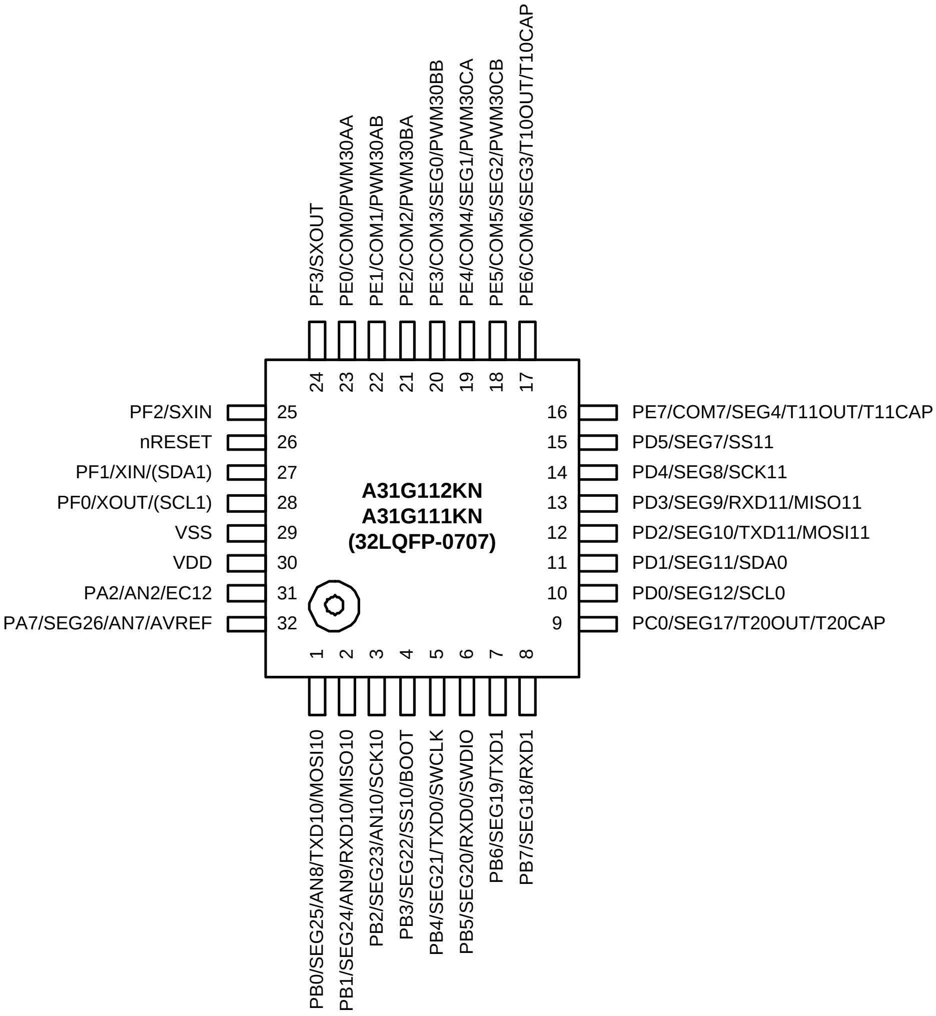


Figure 3. LQFP-48 Pinouts



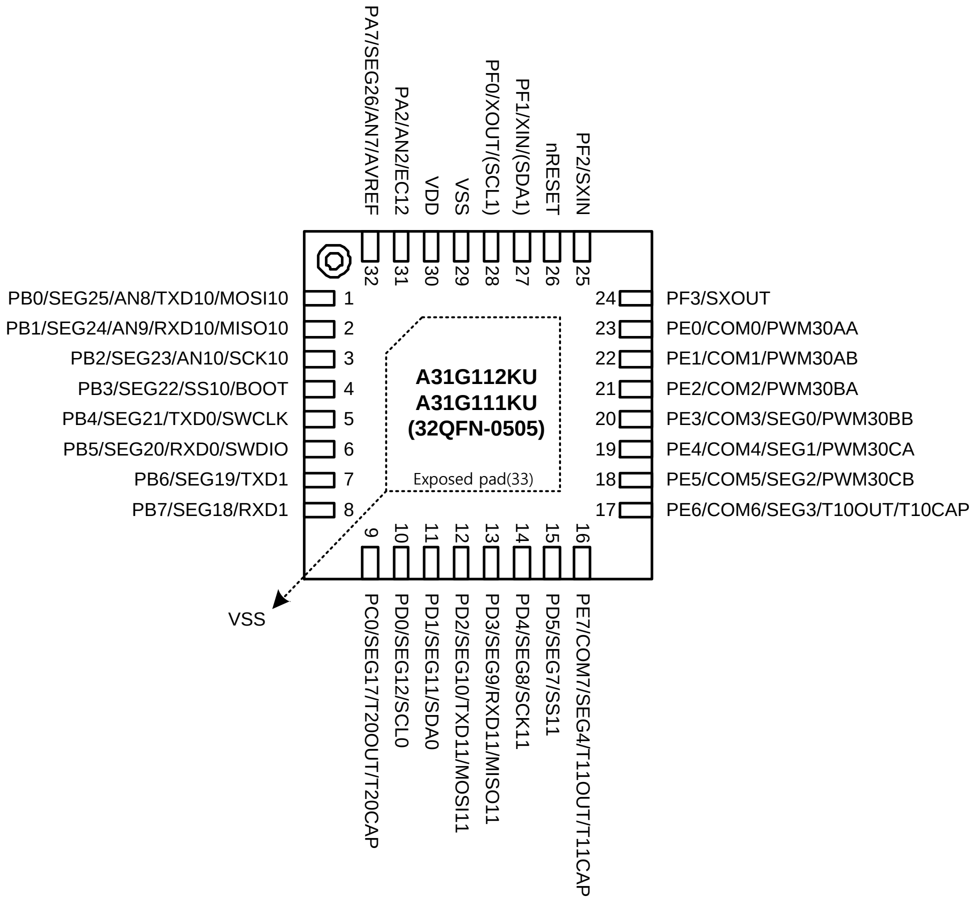
NOTE: The PA3-PA4 and PD6-PD7 pins should be selected as a push-pull output or an input with pullup or pull-down resistor by software control when the MQFP-44 package is used

Figure 4. MQFP-44 Pinouts



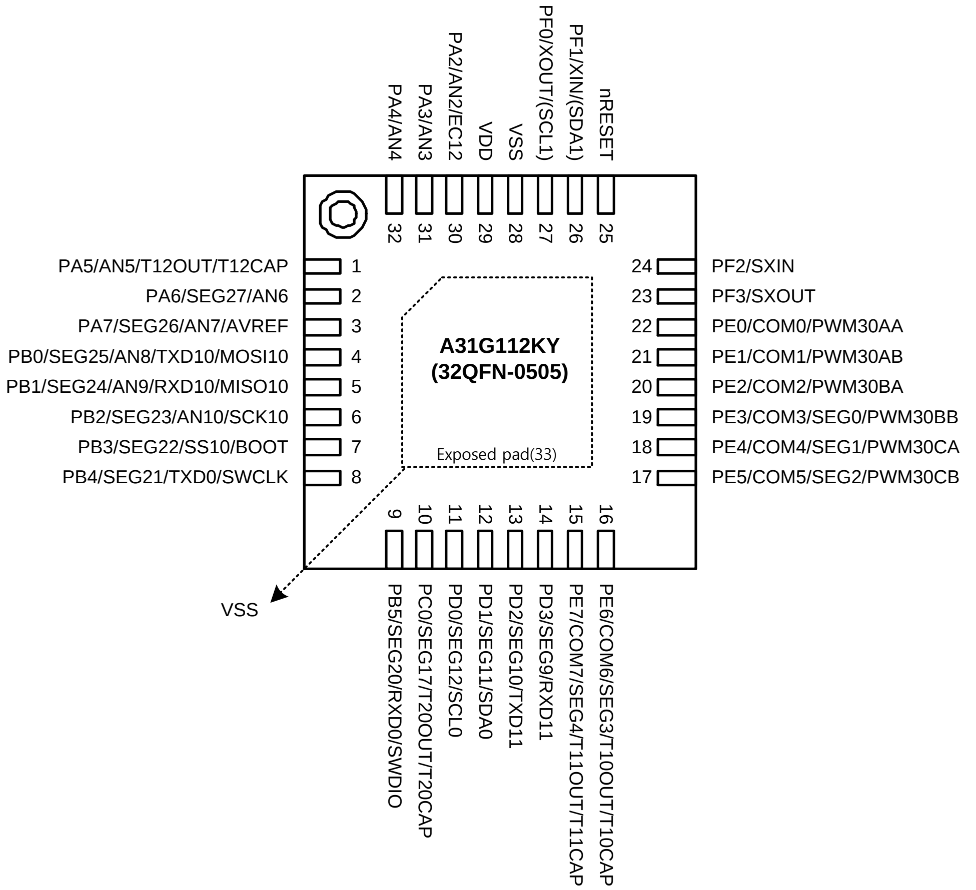
NOTE: The PA0-PA1, PA3-PA6, PC1-PC4, PD6-PD7, and PF4-PF7 pins should be selected as a push-pull output or an input with pullup or pull-down resistor by software control when the LQFP-32 package is used.

Figure 5. LQFP-32 Pinouts



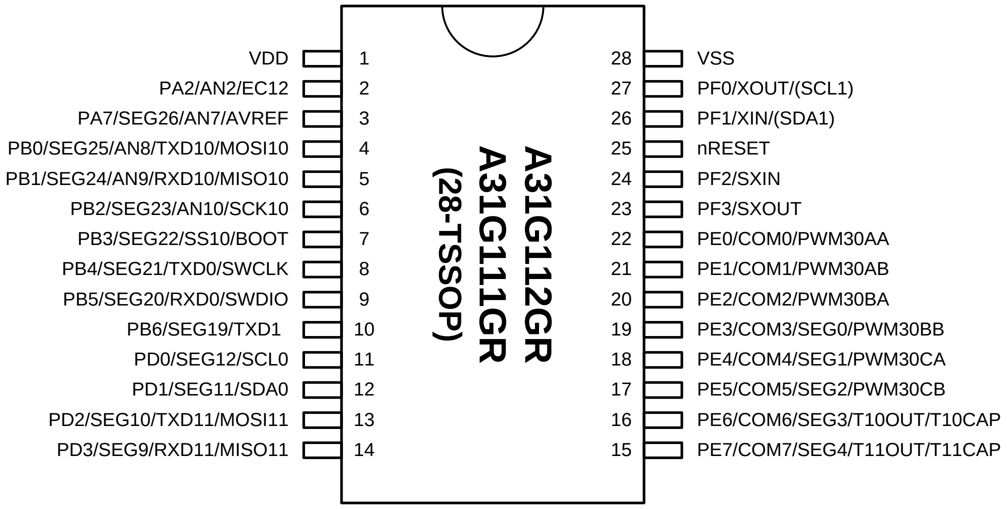
NOTE: The PA0-PA1, PA3-PA6, PC1-PC4, PD6-PD7, and PF4-PF7 pins should be selected as a push-pull output or an input with pullup or pull-down resistor by software control when the QFN-32(TYPE1) package is used.

Figure 6. QFN-32(TYPE1) Pinouts



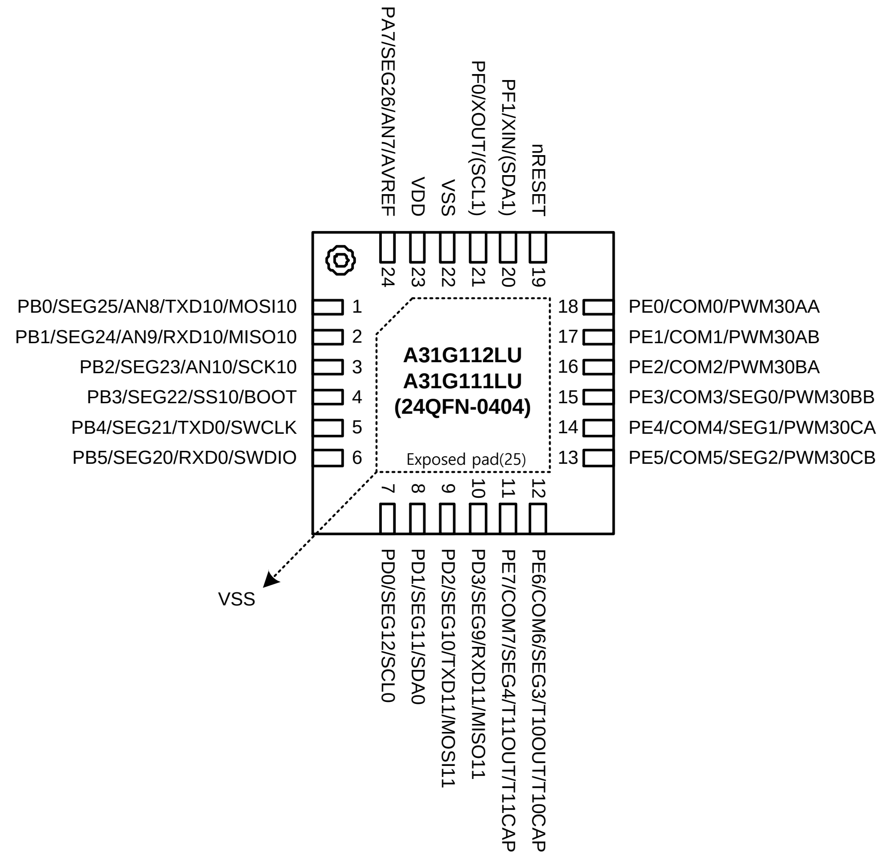
NOTE: The PA0-PA1, PB6-PB7, PC1-PC4, PD4-PD7, and PF4-PF7 pins should be selected as a push-pull output or an input with pullup or pull-down resistor by software control when the QFN-32(TYPE2) package is used.

Figure 7. QFN-32(TYPE2) Pinouts



NOTE: The PA0-PA1, PA3-PA6, PB7, PC0-PC4, PD4-PD7, and PF4-PF7 pins should be selected as a push-pull output or an input with pullup or pull-down resistor by software control when the TSSOP-28 package is used.

Figure 8. TSSOP-28 Pinouts



NOTE: The PA0-PA6, PB6-PB7, PC0-PC4, PD4-PD7, and PF2-PF7 pins should be selected as a push-pull output or an input with pullup or pull-down resistor by software control when the QFN-24 package is used.

Figure 9. QFN-24 Pinouts

2.2 Pin description

Table 2 shows pin configuration containing one pair of power/ground and other dedicated pins. Multi-function pins have up to five selections of functions including GPIO.

Table 2. Pin Description

Pin number							Pin name	Type	Description	Remark
LQFP-48	**MQFP-44**	**LQFP-32**	**QFN-32(1)**	**QFN-32(2)**	**TSSOP-28**	**QFN-24**				
1	44	-	-	1	-	-	PA5*	IOUDS	PORT A Bit 5 Input/Output	
							AN5	IA	A/D Converter Analog Input 5	
							T12OUT	O	Timer 12 Pulse Output	
							T12CAP	I	Timer 12 Capture Input	
2	1	-	-	2	-	-	PA6*	IOUDS	PORT A Bit 6 Input/Output	
							SEG27	O	LCD Segment Signal Output	
							AN6	IA	A/D Converter Analog Input 6	
3	2	32	32	3	3	24	PA7*	IOUDS	PORT A Bit 7 Input/Output	
							SEG26	O	LCD Segment Signal Output	
							AN7	IA	A/D Converter Analog Input 7	
							AVREF	IA	A/D Converter Reference Input	
4	3	1	1	4	4	1	PB0*	IOUDS	PORT B Bit 0 Input/Output	
							SEG25	O	LCD Segment Signal Output	
							AN8	IA	A/D Converter Analog Input 8	
							TXD10	O	UART Data Output	
							MOSI10	I/O	SPI Master Output, Slave Input	
5	4	2	2	5	5	2	PB1*	IOUDS	PORT B Bit 1 Input/Output	
							SEG24	O	LCD Segment Signal Output	
							AN9	IA	A/D Converter Analog Input 9	
							RXD10	I	UART Data Input	
							MISO10	I/O	SPI Master Input, Slave Output	
6	5	3	3	6	6	3	PB2*	IOUDS	PORT B Bit 2 Input/Output	
							SEG23	O	LCD Segment Signal Output	
							AN10	IA	A/D Converter Analog Input 10	
							SCK10	I/O	SPI Clock Input/Output	
7	6	4	4	7	7	4	PB3	IOUDS	PORT B Bit 3 Input/Output	
							SEG22	O	LCD Segment Signal Output	
							SS10	I	SPI Slave Select Input	
							BOOT*	I	Boot Mode Selection Input	Pull-up
8	7	5	5	8	8	5	PB4	IOUDS	PORT B Bit 4 Input/Output	
							SEG21	O	LCD Segment Signal Output	
							TXD0	O	UART Data Output	
							SWCLK*	I	SWD Clock Input	Pull-down

Table 2. Pin Description (continued)

Pin number							Pin name	Type	Description	Remark
LQFP-48	MQFP-44	LQFP-32	QFN-32(1)	QFN-32(2)	TSSOP-28	QFN-24				
9	8	6	6	9	9	6	PB5	IOUDS	PORT B Bit 5 Input/Output	
							SEG20	O	LCD Segment Signal Output	
							RXD0	I	UART Data Input	
							SWDIO*	I/O	SWD Data Input/Output	Pull-up
10	9	7	7	-	10	-	PB6*	IOUDS	PORT B Bit 6 Input/Output	
							SEG19	O	LCD Segment Signal Output	
							TXD1	O	UART Data Output	
11	10	8	8	-	-	-	PB7*	IOUDS	PORT B Bit 7 Input/Output	
							SEG18	O	LCD Segment Signal Output	
							RXD1	I	UART Data Input	
12	11	9	9	10	-	-	PC0*	IOUDS	PORT C Bit 0 Input/Output	
							SEG17	O	LCD Segment Signal Output	
							T20OUT	O	Timer 20 Pulse Output	
							T20CAP	I	Timer 20 Capture Input	
13	12	-	-	-	-	-	PC1*	IOUDS	PORT C Bit 1 Input/Output	
							SEG16	O	LCD Segment Signal Output	
							T21OUT	O	Timer 21 Pulse Output	
							T21CAP	I	Timer 21 Capture Input	
14	13	-	-	-	-	-	PC2*	IOUDS	PORT C Bit 2 Input/Output	
							SEG15	O	LCD Segment Signal Output	
							EC20	I	Timer 20 Event Count Input	
15	14	-	-	-	-	-	PC3*	IOUDS	PORT C Bit 3 Input/Output	
							SEG14	O	LCD Segment Signal Output	
							EC21	I	Timer 21 Event Count Input	
16	15	-	-	-	-	-	PC4*	IOUDS	PORT C Bit 4 Input/Output	
							SEG13	O	LCD Segment Signal Output	
17	16	10	10	11	11	7	PD0*	IOUDS	PORT D Bit 0 Input/Output	
							SEG12	O	LCD Segment Signal Output	
							SCL0	I/O	I2C Clock Input/Output	
18	17	11	11	12	12	8	PD1*	IOUDS	PORT D Bit 1 Input/Output	
							SEG11	O	LCD Segment Signal Output	
							SDA0	I/O	I2C Data Input/Output	
19	18	12	12	13	13	9	PD2*	IOUDS	PORT D Bit 2 Input/Output	
							SEG10	O	LCD Segment Signal Output	
							TXD11	O	UART Data Output	
							MOSI11	I/O	SPI Master Output, Slave Input	

Table 2. Pin Description (continued)

Pin number							Pin name	Type	Description	Remark
LQFP-48	MQFP-44	LQFP-32	QFN-32(1)	QFN-32(2)	TSSOP-28	QFN-24				
20	19	13	13	14	14	10	PD3*	IOUDS	PORT D Bit 3 Input/Output	
							SEG9	O	LCD Segment Signal Output	
							RXD11	I	UART Data Input	
							MISO11	I/O	SPI Master Input, Slave Output	
21	20	14	14	-	-	-	PD4*	IOUDS	PORT D Bit 4 Input/Output	
							SEG8	O	LCD Segment Signal Output	
							SCK11	I/O	SPI Clock Input/Output	
22	21	15	15	-	-	-	PD5*	IOUDS	PORT D Bit 5 Input/Output	
							SEG7	O	LCD Segment Signal Output	
							SS11	I	SPI Slave Select Input	
23	-	-	-	-	-	-	PD6*	IOUDS	PORT D Bit 6 Input/Output	
							SEG6	O	LCD Segment Signal Output	
							EC11	I	Timer 11 Event Count Input	
24	-	-	-	-	-	-	PD7*	IOUDS	PORT D Bit 7 Input/Output	
							SEG5	O	LCD Segment Signal Output	
							EC10	I	Timer 10 Event Count Input	
25	22	16	16	15	15	11	PE7*	IOUDS	PORT E Bit 7 Input/Output	
							COM7	O	LCD Common Signal Output	
							SEG4	O	LCD Segment Signal Output	
							T11OUT	O	Timer 11 Pulse Output	
							T11CAP	I	Timer 11 Capture Input	
26	23	17	17	16	16	12	PE6*	IOUDS	PORT E Bit 6 Input/Output	
							COM6	O	LCD Common Signal Output	
							SEG3	O	LCD Segment Signal Output	
							T10OUT	O	Timer 10 Pulse Output	
							T10CAP	I	Timer 10 Capture Input	
27	24	18	18	17	17	13	PE5*	IOUDS	PORT E Bit 5 Input/Output	
							COM5	O	LCD Common Signal Output	
							SEG2	O	LCD Segment Signal Output	
							PWM30CB	O	Timer 30 PWM Output	
28	25	19	19	18	18	14	PE4*	IOUDS	PORT E Bit 4 Input/Output	
							COM4	O	LCD Common Signal Output	
							SEG1	O	LCD Segment Signal Output	
							PWM30CA	O	Timer 30 PWM Output	
29	26	20	20	19	19	15	PE3*	IOUDS	PORT E Bit 3 Input/Output	
							COM3	O	LCD Common Signal Output	
							SEG0	O	LCD Segment Signal Output	
							PWM30BB	O	Timer 30 PWM Output	

Table 2. Pin Description (continued)

Pin number							Pin name	Type	Description	Remark
LQFP-48	MQFP-44	LQFP-32	QFN-32(1)	QFN-32(2)	TSSOP-28	QFN-24				
30	27	21	21	20	20	16	PE2*	IOUDS	PORT E Bit 2 Input/Output	
							COM2	O	LCD Common Signal Output	
							PWM30BA	O	Timer 30 PWM Output	
31	28	22	22	21	21	17	PE1*	IOUDS	PORT E Bit 1 Input/Output	
							COM1	O	LCD Common Signal Output	
							PWM30AB	O	Timer 30 PWM Output	
32	29	23	23	22	22	18	PE0*	IOUDS	PORT E Bit 0 Input/Output	
							COM0	O	LCD Common Signal Output	
							PWM30AA	O	Timer 30 PWM Output	
33	30	-	-	-	-	-	PF7*	IOUDS	PORT F Bit 7 Input/Output	
							T30CAP	I	Timer 30 Capture Input	
34	31	-	-	-	-	-	PF6*	IOUDS	PORT F Bit 6 Input/Output	
							EC30	I	Timer 30 Event Count Input	
35	32	-	-	-	-	-	PF5*	IOUDS	PORT F Bit 5 Input/Output	
							BLNK	I	External Sync Signal Input for T30 PWM	
36	33	-	-	-	-	-	PF4*	IOUDS	PORT F Bit 4 Input/Output	
							CLKO	O	System Clock Output	
37	34	24	24	23	23	-	PF3*	IOUDS	PORT F Bit 3 Input/Output	
							SXOUT	O	Sub Oscillator Output	
38	35	25	25	24	24	-	PF2*	IOUDS	PORT F Bit 2 Input/Output	
							SXIN	I	Sub Oscillator Input	
39	36	26	26	25	25	19	nRESET	Input	External Reset Input	Pull-up
40	37	27	27	26	26	20	PF1*	IOUDS	PORT F Bit 1 Input/Output	
							XIN	I	Main Oscillator Input	
							(SDA1)	I/O	I2C Data Input/Output	
41	38	28	28	27	27	21	PF0*	IOUDS	PORT F Bit 0 Input/Output	
							XOUT	O	Main Oscillator Output	
							(SCL1)	I/O	I2C Clock Input/Output	
42	39	29	29	28	28	22	VSS	P	Ground	
43	40	30	30	29	1	23	VDD	P	VDD	
44	41	-	-	-	-	-	PA0*	IOUDS	PORT A Bit 0 Input/Output	
							AN0	IA	A/D Converter Analog Input 0	
							SDA1	I/O	I2C Data Input/Output	
45	42	-	-	-	-	-	PA1*	IOUDS	PORT A Bit 1 Input/Output	
							AN1	IA	A/D Converter Analog Input 1	
							SCL1	I/O	I2C Clock Input/Output	

Table 2. Pin Description (continued)

Pin number							Pin name	Type	Description	Remark
LQFP-48	MQFP-44	LQFP-32	QFN-32(1)	QFN-32(2)	TSSOP-28	QFN-24				
46	43	31	31	30	2	-	PA2*	IOUDS	PORT A Bit 2 Input/Output	
							AN2	IA	A/D Converter Analog Input 2	
							EC12	I	Timer 12 Event Count Input	
47	-	-	-	31	-	-	PA3*	IOUDS	PORT A Bit 3 Input/Output	
							AN3	IA	A/D Converter Analog Input 3	
48	-	-	-	32	-	-	PA4*	IOUDS	PORT A Bit 4 Input/Output	
							AN4	IA	A/D Converter Analog Input 4	

NOTES:

1. *Notation: I=Input, O=Output, U=Pull-up, D=Pull-down, S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
2. (*) Selected pin function after reset condition
3. Pin order may be changed with revision notice.

3 CPU

A31G11x series uses Cortex® –M0+ as its CPU and includes an interrupt controller named NVIC.

3.1 Cortex®–M0+ core

The Cortex-M0+ processor is the most energy-efficient ARM processor available. It builds on the very successful Cortex-M0+ processor, retaining full instruction set and tool compatibility, while further reducing energy consumption and increasing performance.

Please refer to the technical reference manual "ARM DDI 0484C" provided by ARM for detail information of Cortex-M0+.

3.2 Interrupt controller

The Cortex-M0+ process has embedded an interrupt controller named NVIC (Nested Vector Interrupt Controller). A31G11x series has additional interrupt control block for controlling 32 interrupt sources generated by internal peripherals.

To use interrupts from internal peripherals, both the NVIC and the interrupt control block must be configured properly. This document describes only the peripheral interrupt controller. For more information about NVIC inside the Cortex-M0+ processor, please refer to the technical reference manual "ARM DDI 0484C" in ARM technical document site.

Table 3. Interrupt Vector Map

Priority	Vector Address	Interrupt Source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Address
-14	0x0000_0008	NMI Exception
-13	0x0000_000C	Hard Fault Exception
-12	0x0000_0010	Reserved
-11	0x0000_0014	
-10	0x0000_0018	
-9	0x0000_001C	
-8	0x0000_0020	
-7	0x0000_0024	
-6	0x0000_0028	

Table 3. Interrupt Vector Map (continued)

Priority	Vector Address	Interrupt Source
-5	0x0000_002C	SVCall Exception
-4	0x0000_0030	Reserved
-3	0x0000_0034	
-2	0x0000_0038	PenSV Exception
-1	0x0000_003C	SysTick Exception
0	0x0000_0040	LVI Interrupt
1	0x0000_0044	WUT Interrupt
2	0x0000_0048	WDT Interrupt
3	0x0000_004C	EINT0 Interrupt
4	0x0000_0050	EINT1 Interrupt
5	0x0000_0054	EINT2 Interrupt
6	0x0000_0058	EINT3 Interrupt
7	0x0000_005C	TIMER10 Interrupt
8	0x0000_0060	TIMER11 Interrupt
9	0x0000_0064	TIMER12 Interrupt
10	0x0000_0068	I2C0 Interrupt
11	0x0000_006C	USART10 Interrupt
12	0x0000_0070	WT Interrupt
13	0x0000_0074	TIMER30 Interrupt
14	0x0000_0078	I2C1 Interrupt
15	0x0000_007C	TIMER20 Interrupt
16	0x0000_0080	TIMER21 Interrupt
17	0x0000_0084	USART11 Interrupt
18	0x0000_0088	ADC Interrupt
19	0x0000_008C	UART0 Interrupt
20	0x0000_0090	UART1 Interrupt

Table 3. Interrupt Vector Map (continued)

Priority	Vector Address	Interrupt Source
21	0x0000_0094	Reserved
22	0x0000_0098	
23	0x0000_009C	
24	0x0000_00A0	
25	0x0000_00A4	
26	0x0000_00A8	
27	0x0000_00AC	
28	0x0000_00B0	
29	0x0000_00B4	
30	0x0000_00B8	
31	0x0000_00BC	

3.3 Registers

Base address and register map of the interrupt registers are shown in Table 4 and Table 5.

Table 4. Base Address of Interrupt Registers

Name	Base address
Interrupt register	0x4000_1000

Table 5. Interrupt Controller Register Map

Name	Offset	Type	Description	Reset Value
INTC_PnTRIG	0x0000-0x00FF	RW	Port n Interrupt Trigger Selection Register	0000_0000
INTC_PnCR	0x0100-0x01FF	RW	Port n Interrupt Control Register	0000_0000
INTC_PnFLAG	0x0200-0x02FF	RW	Port n Interrupt Flag Register	0000_0000
INTC_EINTxCONF1 INTC_EINTxCONF2	0x0300-0x03FF	RW	External Interrupt Configuration Register1,2	0000_0000
INTC_MSK	0x0400	RW	Interrupt Source Mask Register	0000_0000

NOTES:

1. n = B, C, E
2. x = 0 to 3

3.3.1 INTC_PnTRIG: port n interrupt trigger selection register

INTC_PnTRIG register is 32-bit size and accessible in 32/16/8-bit (n= B, C, E).

INTC_PBTRIG=0x4000_1004, INTC_PCTRIG=0x4000_1008
INTC_PETRIG=0x4000_1010

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								**ITRIG7**	**ITRIG6**	**ITRIG5**	**ITRIG4**	**ITRIG3**	**ITRIG2**	**ITRIG1**	**ITRIG0**
0x000000																								**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
–																								**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**

x	ITRIGx	Port n Interrupt Trigger Selection bit, x= 0 to 7	
		0	Edge trigger interrupt
		1	Level trigger interrupt

NOTE: The A31G11x series only has INTC_PnTRIG registers for PB0 – PB7, PC0 – PC3, and PE0 – PE3.

3.3.2 INTC_PnCR: port n interrupt control register

INTC_PnCR register is 32-bit size and accessible in 32/16/8-bit (n= B, C, E).

INTC_PBCR=0x4000_1104, INTC_PCCR=0x4000_1108
INTC_PECR=0x4000_1110

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
Reserved	**INTCTL7**	**INTCTL6**	**INTCTL5**	**INTCTL4**	**INTCTL3**	**INTCTL2**	**INTCTL1**	**INTCTL0**
0x0000	**0 0**	**0 0**	**0 0**	**0 0**	**0 0**	**0 0**	**0 0**	**0 0**
–	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**

2x+1 2x	INTCTLx	Port n Interrupt Control bits, x= 0 to 7	
		00	Disable external interrupt (The flag bit won't be set)
		01	Interrupt on falling edge or on low level
		10	Interrupt on rising edge or on high level
		11	Interrupt on both falling and rising edge, No level interrupt

NOTES:

1. The A31G11x series only has INTC_PnCR registers for PB0 – PB7, PC0 – PC3, and PE0 – PE3.
2. Do not write "11" to the corresponding INTCTLx[1:0] bits when the ITRIGx bit of INTC_PnTRIG is '1'. If so, it may cause a malfunction.

3.3.3 INTC_PnFLAG: port n interrupt flag register

INTC_PnFLAG register is 32-bit size and accessible in 32/16/8-bit (n= B, C, E).

INTC_PBFLAG=0x4000_1204, INTC_PCFLAG=0x4000_1208
INTC_PEFLAG=0x4000_1210

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Reserved	**FLAG7**	**FLAG6**	**FLAG5**	**FLAG4**	**FLAG3**	**FLAG2**	**FLAG1**	**FLAG0**
0x000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
–	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**

x	FLAGx	Port n Interrupt Flag bit, x: 0 to 7	
		0	No request occurred
		1	Request occurred. The bit is cleared to '0' when '1' is written.

NOTE: The A31G11x series only has INTC_PnFLAG registers for PB0 – PB7, PC0 – PC3, and PE0 – PE3.

3.3.4 INTC_EINTnCONF1: external interrupt n configuration register 1 (n= 0 to 3)

INTC_EINTnCONF1 register is 32-bit size and accessible in 32/16/8-bit.

INTC_EINT0CONF1=0x4000_1300, INTC_EINT1CONF1=0x4000_1304
INTC_EINT2CONF1=0x4000_1308, INTC_EINT3CONF1=0x4000_130C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF7				CONF6				CONF5				CONF4				CONF3				CONF2				CONF1				CONF0			
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RW				RW				RW				RW				RW				RW				RW				RW			

4x+3 4x	CONFx	Configuration bits for External Interrupt Group n, x: 0 to 7	
		0000	PAx (not used)
		0001	PBx
		0010	PCx
		0011	PDx (not used)
		0100	PEx
		Others	Reserved

NOTE: The A31G11x series only has external interrupts for PB0 – PB7, PC0 – PC3, and PE0 – PE3.

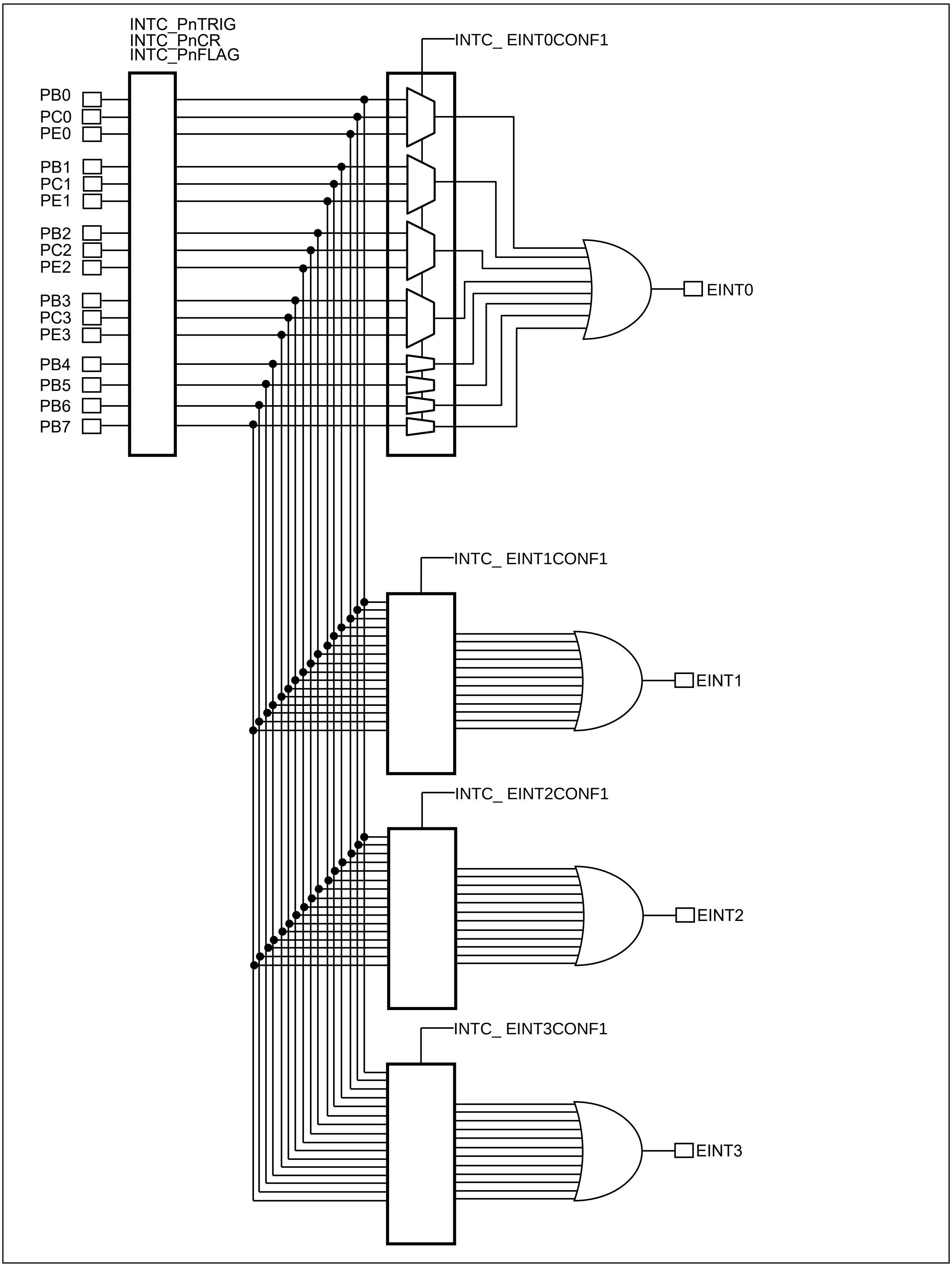


Figure 10. Configuration Map for External Interrupt 0/1/2/3 Group (n = B, C, E)

3.3.5 INTC_MSK: interrupt source mask register

INTC_MSK register is 32-bit size and accessible in 32/16/8-bit.

INTC_MSK=0x4000_1400

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IMSK31	IMSK30	IMSK29	IMSK28	IMSK27	IMSK26	IMSK25	IMSK24	IMSK23	IMSK22	IMSK21	IMSK20	IMSK19	IMSK18	IMSK17	IMSK16	IMSK15	IMSK14	IMSK13	IMSK12	IMSK11	IMSK10	IMSK9	IMSK8	IMSK7	IMSK6	IMSK5	IMSK4	IMSK3	IMSK2	IMSK1	IMSK0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

x	IMSKx	Interrupt Source Mask bit, x: 0 to 31	
		0	Mask. The corresponding interrupt is disabled.
		1	Unmask.

NOTES:

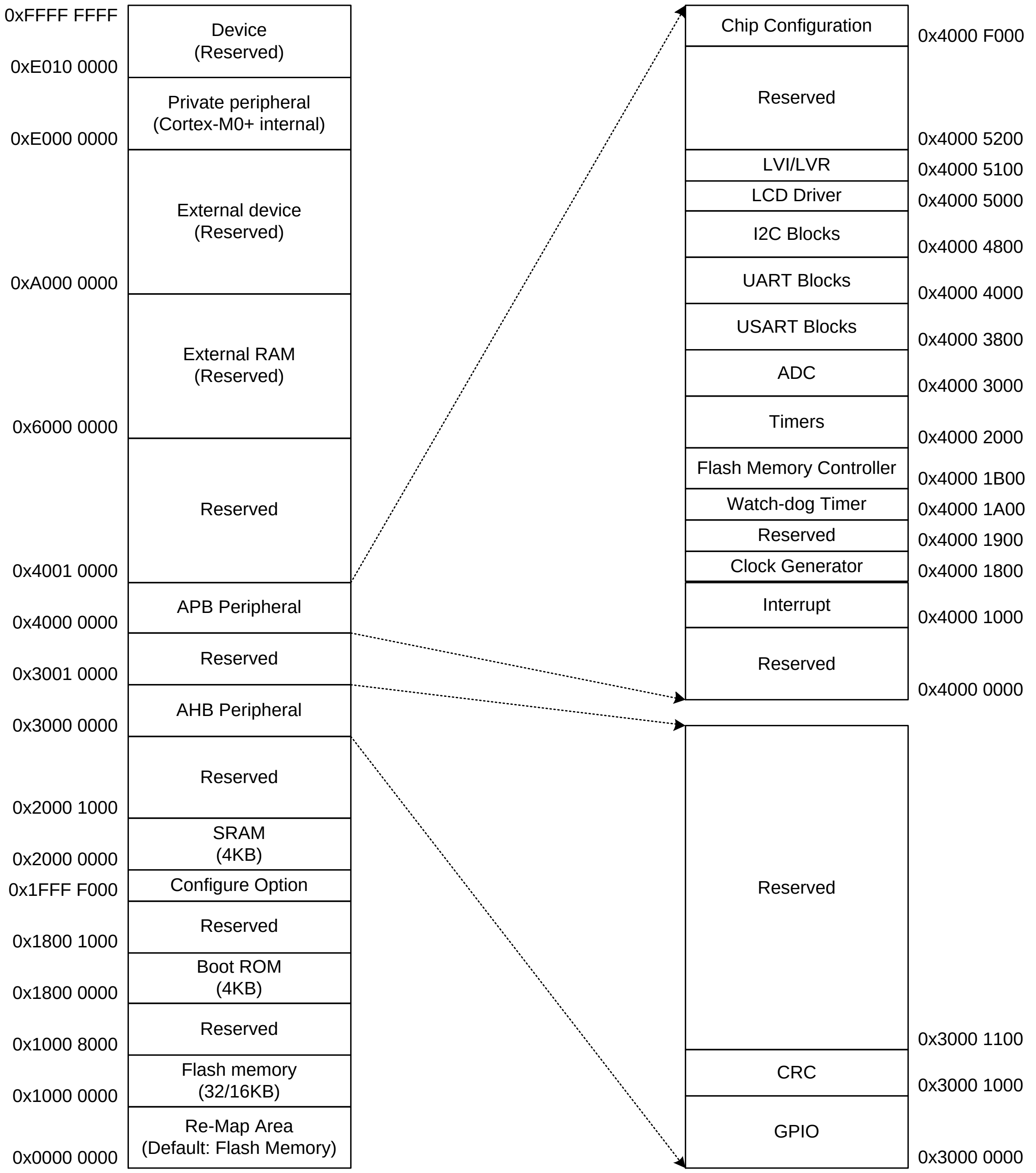
1. A mask interrupt source is not used as a wake-up source on “sleep”/”deep sleep” mode.
2. The corresponding interrupts of IMSKx are listed below:

Table 6. Corresponding Interrupts of IMSKx

Source Mask	INTERRUPT SOURCE NAME
IMSK0	LVI
IMSK1	WUT
IMSK2	WDT
IMSK3	EINT0
IMSK4	EINT1
IMSK5	EINT2
IMSK6	EINT3
IMSK7	TIMER10
IMSK8	TIMER11
IMSK9	TIMER12
IMSK10	I2C0
IMSK11	USART10
IMSK12	WT
IMSK13	TIMER30
IMSK14	I2C1
IMSK15	TIMER20
IMSK16	TIMER21
IMSK17	USART11
IMSK18	ADC
IMSK19	UART0
IMSK20	UART1
IMSK21	Reserved
IMSK22	
IMSK23	
IMSK24	
IMSK25	
IMSK26	
IMSK27	
IMSK28	
IMSK29	
IMSK30	
IMSK31	

4 Control memory organization

Figure 11 shows addressable memory space in memory map.



NOTES:

1. Access to the reserved area may cause malfunction.
2. The Boot ROM should be run at less than or equal to 30MHz.

Figure 11. Main Memory Map

4.1 Internal SRAM

A31G11x series has a block of 0-wait on-chip SRAM. Its size is 4KB, and its base address is 0x2000_0000. The SRAM's memory area is mainly for data memory and stack memory. It is possible to locate code area in the SRAM memory for fast operation or for flash erase or program operation for self-program.

This device does not support memory remapping. So jump and return is required to process the code in SRAM memory area.

4.2 Boot mode

4.2.1 Boot mode pins

A31G11x series has a Boot mode to program the internal flash memory. The Boot mode will be activated by setting a BOOT pin to "Low" level at reset timing (Normal operation mode is "High" level).

The Boot mode supports either UART boot or SPI boot. For the UART boot, TXD10/RXD10 ports are used. For the SPI boot, MOSI10/MISO10/SCK10/SS10 ports are used.

Table 7 introduces pins used in the Boot mode.

Table 7. Boot Mode Pin List

Block	Pin Name	Direction	Description
SYSTEM	nRESET	I	Reset Input signal
	BOOT/PB3	I	'0' to enter Boot mode
UART mode of USART10	RXD10/PB1	I	UART Boot Receive Data
	TXD10/PB0	O	UART Boot Transmit Data
SPI mode of USART10	SS10/PB3	I	SPI Boot Slave Selectable after Boot ROM
	SCK10/PB2	I	SPI Boot Clock Input
	MISO10/PB1	I	SPI Boot Data Input with function exchange
	MOSI10/PB0	O	SPI Boot Data Output with function exchange

4.2.2 Boot mode connection

A user can design target boards using any of Boot mode ports – UART or SPI mode of USART10. Examples of connection diagrams in the Boot mode are introduced in figures 12 and 13.

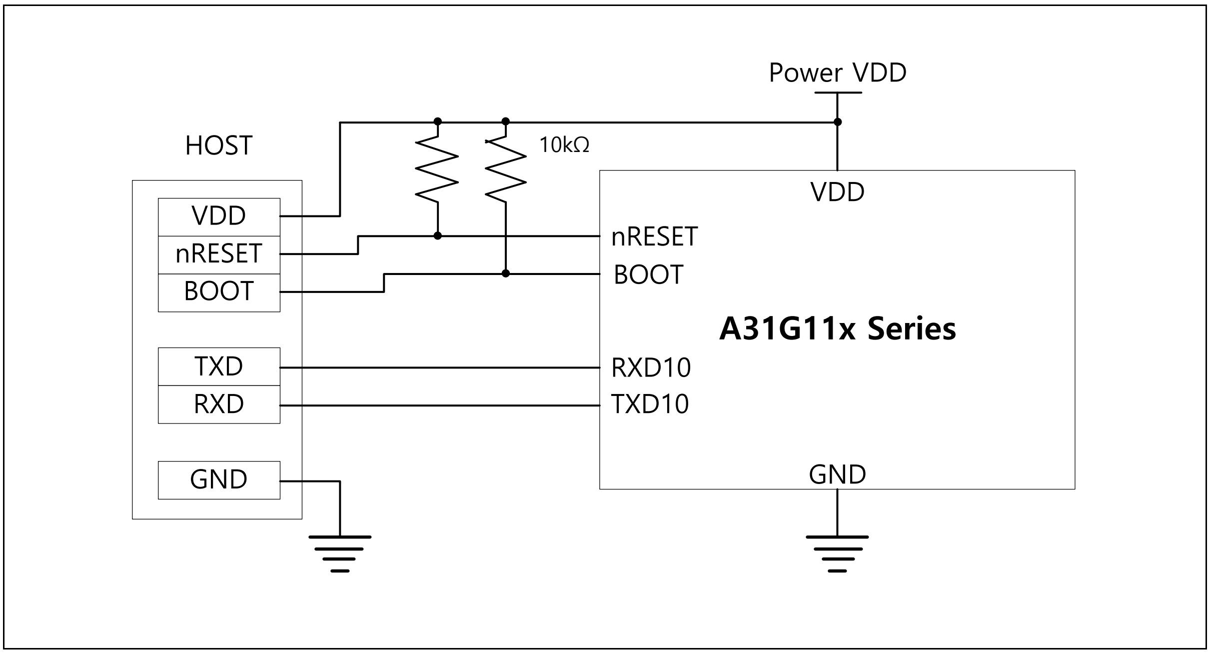


Figure 12. Connection Diagram of UART Boot

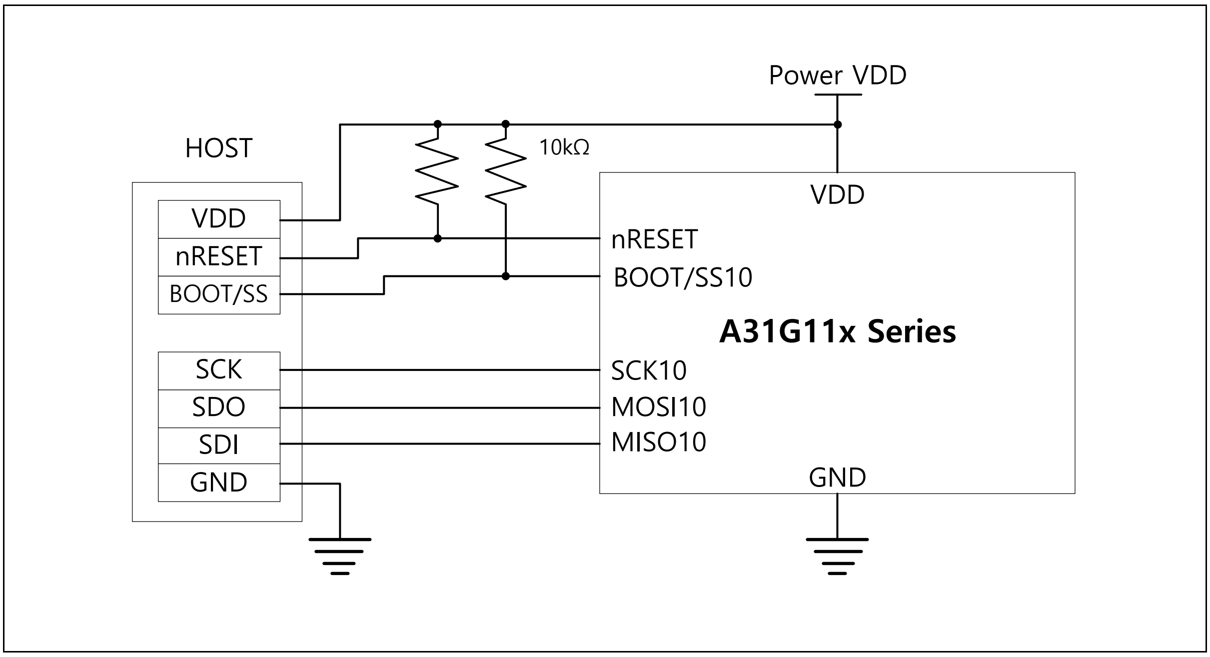


Figure 13. Connection Diagram of SPI Boot

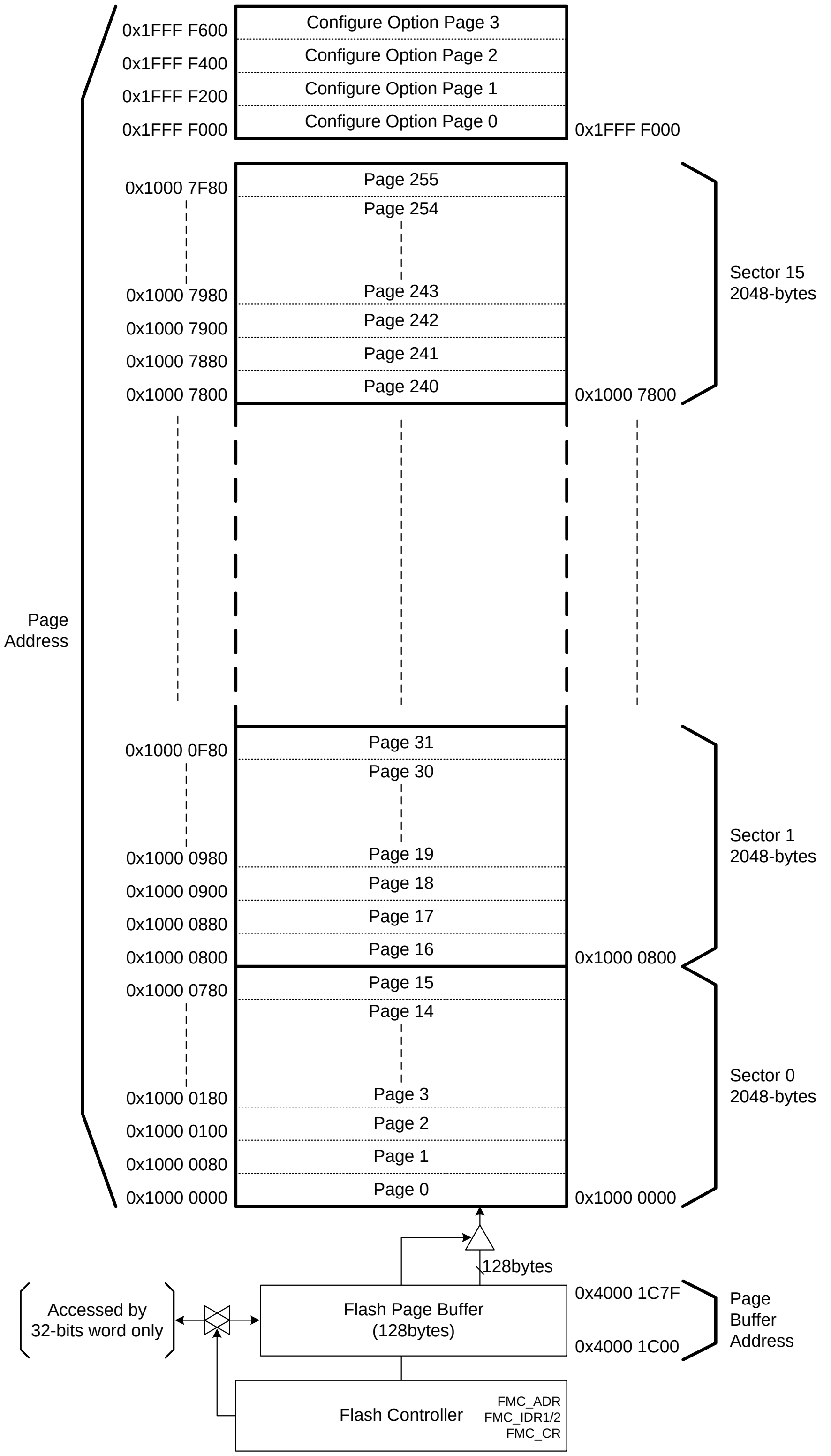
4.3 Flash memory

A31G11x series has an internal flash memory featuring the followings:

- 32KB or 16KB Flash code memory
- 32-bit read data bus width
- 128-byte page size
- Page erase and bulk erase available
- 128-byte unit program

Table 8. Internal Flash Memory Specification

Item	Description
Size	32KB
Start address	0x1000_0000
End address	0x1000_7FFF
Page size	128-byte
Total page count	256 pages
PGM unit	128-byte
Erase unit	128-byte or bulk



NOTES:

1. If any instruction other than 32-bit is used to write data to the buffer, wrong data will be written.
2. Each configure option page0/1/2/3 has 128bytes respectively.

Figure 14. Internal Flash Memory Block Diagram

4.3.1 Registers

Base address and register map of the Flash memory controller are shown in Table 9 and Table 10.

Table 9. Base Address of Flash Memory Controller

Name	Base address
Flash memory controller	0x4000_1B00

Table 10. Flash Memory Controller Register Map

Name	Offset	Type	Description	Reset Value
FMC_ADR	0x0000	RW	Flash Memory Address Register	0x5FFFFF80
FMC_IDR1	0x0004	RW	Flash Memory Identification Register 1	0x00000000
FMC_IDR2	0x0008	RW	Flash Memory Identification Register 2	0x00000000
FMC_CR	0x000C	RW	Flash Memory Control Register	0x00000000
FMC_BCR	0x0010	RW	Flash Memory Configure Area Bulk Erase Control Register	0x00000000
FMC_ERFLAG	0x0014	RW	Flash Memory Error Flag	0x00000000
FMC_PAGEBUF	0x0100-0x017F	WO	Flash Memory Page Buffer Area	0x00000000

4.3.1.1 FMC_ADR: flash memory address register

FMC_ADR register is used to remember the internal flash memory address. This register is 32-bit size.

FMC_ADR=0x4000_1B00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR																															
0x5FFF_FF80 RW																															

31 0	ADDR	Flash Memory Address Pointer. This register is reset to 0x5FFFFF80 immediately after a single operation.

NOTE: The LSB-2bits of the target flash address is always considered to "00b".

4.3.1.2 FMC_IDR1: flash memory identification register 1

FMC_IDR1 register is an internal flash memory identification register for flash mode. This register is 32-bit size.

FMC_IDR1=0x4000_1B04

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">ID1</td></tr>
<tr><td colspan="32">0x0000_0000
RW</td></tr>
</table>

31 0	ID1	Flash Memory Identification 1	
		0x08192A3B	Identification value for a flash mode
		Others	No identification value

4.3.1.3 FMC_IDR2: flash memory identification register 2

FMC_IDR2 register is an internal flash memory identification register for flash mode. This register is 32-bit size.

FMC_IDR2=0x4000_1B08

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">ID2</td></tr>
<tr><td colspan="32">0x0000_0000
RW</td></tr>
</table>

31 0	ID2	Flash Memory Identification 2	
		0x4C5D6E7F	Identification value for a flash mode
		Others	No identification value

NOTES:

1. The FMC_IDR1/2 registers are automatically cleared to logic 0x00000000 immediately after one time operation except “flash page buffer reset mode”.
2. The FMC_IDR1/2 registers should be written with correct values in turn.
3. If incorrect values are written to the FMC_IDR1/2 registers, the registers are cleared to logic 0x00000000.

4.3.1.4 FMC_CR: flash memory control register

FMC_CR register is an internal flash memory control register. This register is 32-bit size.

FMC_CR=0x4000_1B0C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WTIDKY																**FMKEY**								**FMBUSY**	**Reserved**			**FMOD**			
0x0000																**0x00**								**0**	**000**			**0000**			
WO																**RW**								**RO**	**-**			**RW**			

31	WTIDKY	Write Identification Key.	
16		When writing, write 0x6C93 to these bits, or else writing is ignored.	
15	FMKEY	Flash Memory Operation Area Selection.	
8		0x00	Selects no area but for flash, induces page buffer reset mode.
		0x38	Selects "configure option area" for flash memory erase/write.
		0xA4	Selects "flash memory area" for flash memory erase/write.
		Others	Not allowed. FMOPFLAG will be set.
7	FMBUSY	Flash Memory Operation Mode Busy.	
		0	No effect.
		1	Busy.
3	FMOD	Flash Memory Operation Mode Selection.	
0		0001	"Flash page buffer reset mode" and start regardless of the flash operation rule. (Clear all 128bytes page buffer to 0xFFFFFFFF)
		0010	"Flash page erase mode" and start when the flash operation rule is satisfied.
		0100	"Flash page write mode" and start when the flash operation rule is satisfied.
		1000	"Flash bulk erase mode" and start when the flash operation rule is satisfied.
		Others	Not allowed. FMOPFLAG will be set.

NOTES:

1. During a flash memory operation mode, the all interrupts are on disable regardless of enable bits.
2. The FMKEY[7:0] and FMOD[3:0] bits are automatically cleared to logic "0x00" immediately after a single operation.

4.3.1.5 FMC_BCR: flash memory configure area bulk erase control register

FMC_BCR register is used to permit bulk erase. This register is 32-bit size.

FMC_BCR=0x4000_1B10

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
WTIDKY	**Reserved**	**CNF3BEN**	**CNF2BEN**	**CNF1BEN**
0x0000	**0000**	**0000**	**0000**	**0000**
WO	**–**	**RW**	**RW**	**RW**

31	WTIDKY	Write Identification Key.	
16		When writing, write 0xC1BE to these bits, or else writing is ignored.	
11	CNF3BEN	Configure Option Page 3 Bulk Erase Enable.	
8		0x5	Permit “configure option page 3” erase at bulk erase
		Others	Protect “configure option page 3” erase at bulk erase
7	CNF2BEN	Configure Option Page 2 Bulk Erase Enable.	
4		0x5	Permit “configure option page 2” erase at bulk erase
		Others	Protect “configure option page 2” erase at bulk erase
3	CNF1BEN	Configure Option Page 1 Bulk Erase Enable.	
0		0x5	Permit “configure option page 1” erase at bulk erase
		Others	Protect “configure option page 1” erase at bulk erase

NOTE: This register is automatically cleared to logic “0x00” immediately after one time operation.

4.3.1.6 FMC_ERFLAG: flash memory error flag register

FMC_ERFLAG is 32-bit size, and accessible in 32/16/8-bit.

FMC_ERFLAG=0x4000_1B14

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2	1	0
Reserved		**INSTFLAG**	**FMOPFLAG**
0x000000	**000000**	**0**	**0**
–		**RW**	**RW**

1	INSTFLAG	Don’t care	
0	FMOPFLAG	Error bit of Flash Memory Operation Procedure. This bit is set to logic 1 if there is a wrong procedure for flash memory operation.	
		0	No wrong procedure.
		1	A wrong procedure occurred. The bit is cleared to ‘0’ when ‘1’ is written.

4.3.2 Procedure for flash memory operation

- The high frequency internal RC oscillator (HIRC) should be enabled by S/W for flash memory operation.
- The procedure will be cleared, the related registers will be reset, and FMOPFLAG will be set if wrong sequence is detected.
- The address range is 0x10000000 to 0x17FFFFFF when “flash memory area” is selected.
- The address range is 0x1FFFF000 to 0x1FFFFFFF when “configure option area” is selected.
- If the CPU is in the flash memory, the CPU will halt while the flash memory is programmed.
- The “configure option page 0” won’t be erased at flash bulk erase mode.
- The “configure option page 1/2/3” can be erased at flash bulk erase mode if the CNFxBEN has correct values
- The CPU should not be in the flash memory area on flash bulk erase mode.
- A write to the flash related register is ignored during flash operation.
- An NMI source should not be selected during flash memory operation is activated.
- The LVR should be enabled during flash memory operation is activated (Recommended: 2.28V over).
- The global interrupt should be disabled.
- The CPU should not enter sleep and deep sleep mode during flash erase/write mode.

4.3.2.1 Page Erase Procedure

1. Write 0x5FFFFFFF to FMC_ADR when the register is equal to 0x5FFFFF80.
2. Write 0x08192A3B to FMC_IDR1 register when the FMC_ADR register is equal to 0x5FFFFFFF.
3. Write 0x4C5D6E7F to FMC_IDR2 register when the FMC_ADR register is equal to 0x5FFFFFFF.
4. Write 0x6C930001 to FMC_CR register for page buffer reset when the FMC_ADR register is equal to 0x5FFFFFFF.
5. Clear page buffer (128bytes) by writing 0xFFFFFFFF repeatedly during the FMC_ADR register is 0x5FFFFFFF.
6. Write a page address to FMC_ADR register.
7. Read and check the FMC_IDR1 and FMC_IDR2 registers in turn.
8. Write 0x6C93A402 (flash memory area) or 0x6C933802 (configure option area) to FMC_CR register.
9. Check whether the FMBUSY bit is ‘0’ or not.
10. Verify the erased pages.

4.3.2.2 Byte/Page Write Procedure

1. Write 0x5FFFFFFF to FMC_ADR when the register is equal to 0x5FFFFF80.
2. Write 0x08192A3B to FMC_IDR1 register when the FMC_ADR register is equal to 0x5FFFFFFF.
3. Write 0x4C5D6E7F to FMC_IDR2 register when the FMC_ADR register is equal to 0x5FFFFFFF.

4. Write 0x6C930001 to FMC_CR register for page buffer reset when the FMC_ADR register is equal to 0x5FFFFFFF.
5. Write data to page buffer (any bytes) when the FMC_ADR register is equal to 0x5FFFFFFF.
6. Write a page address to FMC_ADR register.
7. Read and check the FMC_IDR1 and FMC_IDR2 registers in turn.
8. Write 0x6C93A404 (flash memory area) or 0x6C933804 (configure option area) to FMC_CR register.
9. Check whether the FMBUSY bit is '0' or not.
10. Verify the written pages.

4.3.2.3 Flash bulk Erase Procedure

1. Write 0x5FFFFFFF to FMC_ADR when the register is equal to 0x5FFFFF80.
2. Write 0x08192A3B to FMC_IDR1 register when the FMC_ADR register is equal to 0x5FFFFFFF.
3. Write 0x4C5D6E7F to FMC_IDR2 register when the FMC_ADR register is equal to 0x5FFFFFFF.
4. Write 0x6C930001 to FMC_CR register for page buffer reset when the FMC_ADR register is equal to 0x5FFFFFFF.
5. Write the value 0x5F9A30D7 to FMC_ADR register.
6. Read and check the FMC_IDR1 and FMC_IDR2 register in turn.
7. Write 0x6C93A408 to FMC_CR register.
8. Check whether the FMBUSY bit is '0' or not.
9. Verify all the pages of flash memory.

4.3.2.4 Flash Bulk Erase Procedure Including Configure Option Area.

1. Write 0x5FFFFFFF to FMC_ADR when the register is equal to 0x5FFFFF80.
2. Write 0x08192A3B to FMC_IDR1 register when the FMC_ADR register is equal to 0x5FFFFFFF.
3. Write 0x4C5D6E7F to FMC_IDR2 register when the FMC_ADR register is equal to 0x5FFFFFFF.
4. Write 0x6C930001 to FMC_CR register for page buffer reset when the FMC_ADR register is equal to 0x5FFFFFFF.
5. Write the value 0xC1BE0VVV to FMC_BCR register. If V==5, the corresponding option page will be erased.
6. Write the value 0x5F9A30D7 to FMC_ADR register.
7. Read and check the FMC_IDR1 and FMC_IDR2 register in turn.
8. Write 0x6C93A408 to FMC_CR register.
9. Check whether the FMBUSY bit is '0' or not.
10. Verify all the pages of flash memory.

4.4 Configure option area

Configuration option area of A31G11x series is used for system related trimming values, user option, and user data. The configure option area consists of four pages in the flash memory, which can be erased and written by the flash memory controller. This area can be read by any instruction.

The four pages of the configuration option area are listed in the followings:

- Page 0: System related trimming values
- Page 1: User option for read protection, watchdog timer, and LVR voltage level configurations
- Page 2: User data 0 area
- Page 3: User data 1 area

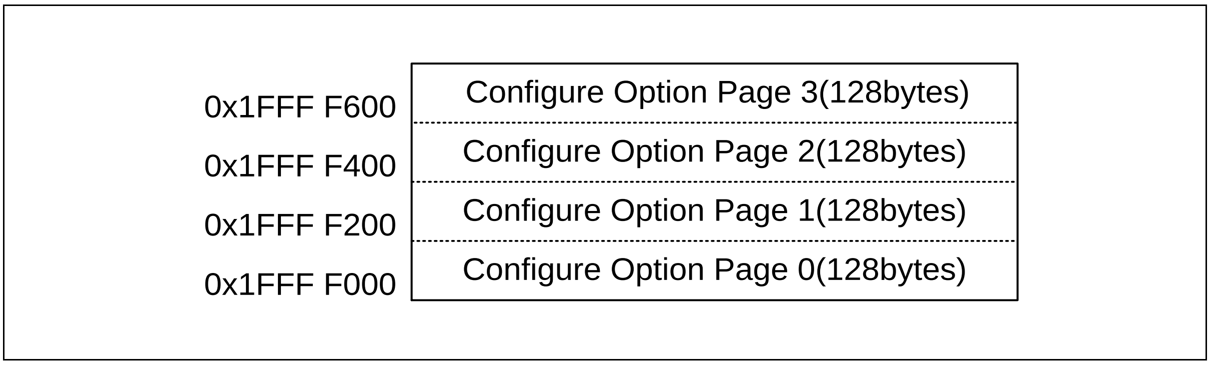


Figure 15. Configure Option Area Structure

4.4.1 Configuration option page

Base address of the configuration option area ranges from 0x1FFF_F000 to 0x1FFF_F600. The area map is shown in Table 11.

Table 11. Configuration Option Area Map

Page	**NAME**	**ADDRESS**	**DESCRIPTION**
0	-	0x1FFF_F000 to 0x1FFF_F07F	System Trimming Values
1	CONF_RPCNFIG	0x1FFF_F200	Configuration for Read Protection
	CONF_WDTCNFIG	0x1FFF_F20C	Configuration for Watch-Dog Timer
	CONF_LVRCNFIG	0x1FFF_F210	Configuration for Low Voltage Reset
	CONF_CNFIGWTP1	0x1FFF_F214	Erase/Write Protection for Configure Option Page 1/2/3
	CONF_FMWTP1	0x1FFF_F240	Erase/Write Protection for Flash Memory
2	**-**	0x1FFF_F400 to 0x1FFF_F47F	User Data Area 0
3	**-**	0x1FFF_F600 to 0x1FFF_F67F	User Data Area 1

4.4.1.1 CONF_RPCNFIG: Configuration for Read Protection

The configuration for the flash memory read protection is 32-bit. This is accessible in 32/16/8-bit.

CONF_RPCNFIG=0x1FFF_F200

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WTIDKY																												**Reserved**		**READP**	

31 4	WTIDKY	Write Identification Key These bits are the write key for “Read Protection”. So, The WTIDKY[27:0] should be kept with the 0x69C8A27. Otherwise, the read protection will be on level 2.	
1 0	READP	Read Protection for Flash Memory Area.	
		11	Read protection level 0, No restriction for read/erase/write.
		10	Read protection level 1, Not readable/erasable/writable by “Debug” Bulk erasable only by ”Debug” Readable/erasable/writable by “Instruction from Flash Memory and RAM”
		0x	Read protection level 2, Where x is don’t care Not readable/erasable/writable by “Debug”/”Instruction from RAM” Bulk erasable only by “Instruction from RAM”/”Debug” Readable/erasable/writable by “Instruction from Flash Memory”

NOTES:

1. The read protection level can be changed from lower level to higher level only.
2. The “Configure Option Page 1” cannot be erased by “Debug” unit on “read protection level 1/2” and by “Instruction from RAM” on “read protection level 2.
3. The configure option area may be read even if the “read protection” is on level 1 and 2.
4. A page unit erase/write except a bulk erase isn’t executable by “Instruction from RAM” regardless of the CONF_FMWTP1 register on read protection level 2.
5. A page unit erase/write except a bulk erase isn’t executable by “Debug” regardless of the CONF_FMWTP1 register on read protection level 1/2.
6. The read protection level will be ‘0’ on operation after bulk erase.

4.4.1.2 CONF_WDTCNFIG: Configuration for Watch-Dog Timer

The configuration for watchdog timer is 32-bit flash memory. This is accessible in 32/16/8-bit.

CONF_WDTCNFIG=0x1FFF_F20C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																**WRCMF**												**Reserved**	**WCLKMF**	**WRSTMF**	**WCNTMF**

15 4	WRCMF	Watchdog Timer RC Oscillator Master Configuration	
		0x96D	The WDTRC oscillation is decided by the WDTRCEN of SCU_CLKSRCR register
		0x2A7	Master enable WDTRC but disabled at deep sleep mode
		Others	Master enable WDTRC
		NOTE:	If the WDTRC is selected for MCLK by SCU_SCCR register when the bits are not 0x96D, the CPU cannot wake up at deep sleep mode. So, only sleep mode on the above case should be used for power down.
2	WCLKMF	Watchdog Timer Clock Selection Master Configuration	
		0	Watchdog timer clock is selected by the WDTCLK of SCU_PPCLKSR register
		1	Master selection WDTRC for watchdog timer clock
1	WRSTMF	Watchdog Timer Reset Enable Master Configuration	
		0	Master enable WDT reset
		1	Disable/Enable of WDT reset is decided by the RSTEN[5:0] of WDT_CR register
0	WCNTMF	Watchdog Timer Counter Enable Master Configuration	
		0	Master enable WDT counter
		1	Disable/Enable WDT counter is decided by the CNTEN[5:0] of WDT_CR register

4.4.1.3 CONF_LVRCNFIG: Configuration for Low Voltage Reset

The configuration for low voltage reset is 32-bit flash memory. This is accessible in 32/16/8-bit.

CONF_LVRCNFIG=0x1FFF_F210

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																**LVRENM**								**Reserved**				**LVRVS**			

15 8	LVRENM	LVR Reset Operation Control Master Configuration	
		0xAA	LVR operation is decided by the LVREN of SCU_LVRCR register
		Ohters	Master enable LVR operation
3 0	LVRVS	LVR Voltage Selection bits	
		1111	1.62V
		1110	Do not write.
		1101	Do not write.
		1100	Do not write.
		1011	2.00V
		1010	2.13V
		1001	2.28V
		1000	2.46V
		0111	2.67V
		0110	3.04V
		0101	3.20V
		0100	3.55V
		0011	3.75V
		0010	3.99V
		0001	4.25V
		0000	4.55V

4.4.1.4 CONF_CNFIGWTP1: Erase/Write Protection for Configure Option Page 1/2/3

The erase/write protection for configure option page is 32-bit flash memory. This is accessible in 32/16/8-bit.

CONF_CNFIGWTP1=0x1FFF_F214

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																												**Reserved**	**CP3WP**	**CP2WP**	**CP1WP**

2	CP3WP	Configure Option Page 3 Erase/Write Protection	
		0	Enable protection (Not erasable/writable by instruction)
		1	Disable protection (Erasable/writable by instruction)
1	CP2WP	Configure Option Page 2 Erase/Write Protection	
		0	Enable protection (Not erasable/writable by instruction)
		1	Disable protection (Erasable/writable by instruction)
0	CP1WP	Configure Option Page 1 Erase/Write Protection	
		0	Enable protection (Not erasable/writable by instruction)
		1	Disable protection (Erasable/writable by instruction)

NOTE: The configure option page which is protected cannot be erased by page unit.

4.4.1.5 CONF_FMWTP1 Erase/Write Protection for Flash Memory

The erase/write protection for flash memory is 32-bit flash memory. This is accessible in 32/16/8-bit.

CONF_FMWTP1=0x1FFF_F240

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																**SWTP15**	**SWTP14**	**SWTP13**	**SWTP12**	**SWTP11**	**SWTP10**	**SWTP9**	**SWTP8**	**SWTP7**	**SWTP6**	**SWTP5**	**SWTP4**	**SWTP3**	**SWTP2**	**SWTP1**	**SWTP0**

n	SWTPn	Flash Memory Erase/Write Protection bits, n: 0 to 15 (Sector 0 to Sector 15)	
		0	Protect “flash memory sector n erase/write”
		1	Permit “flash memory sector n erase/write”

5 SCU (System Control Unit)

A31G11x series has a built-in intelligent power control block, which manages analog blocks and operating modes. Internal reset and clock signals are controlled by SCU block to maintain optimized system performance and power dissipation.

5.1 SCU block diagram

Figure 16 shows the SCU block diagram.

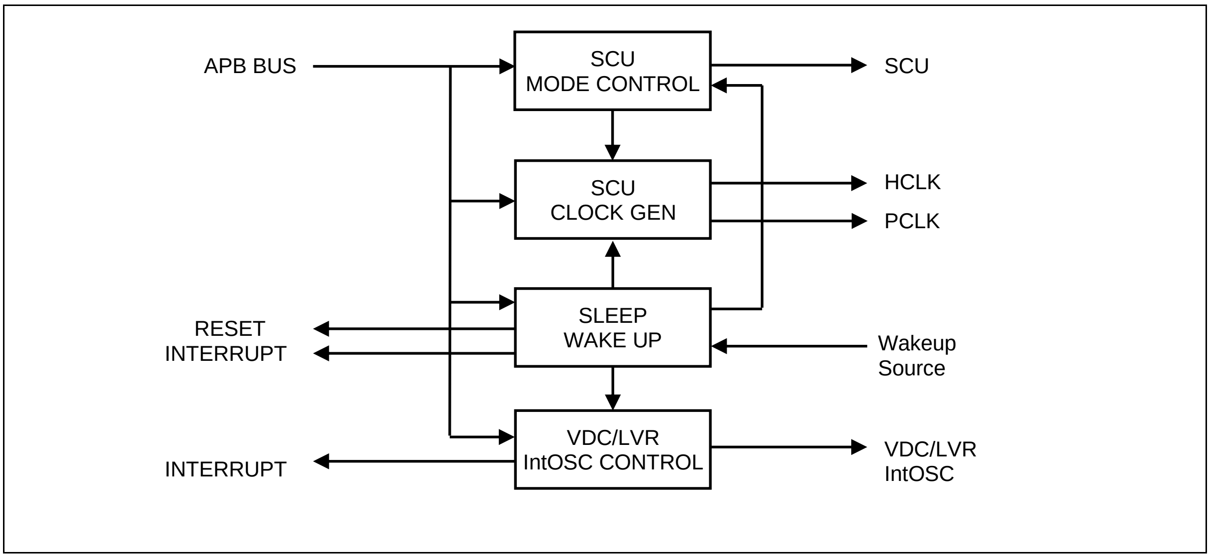


Figure 16. SCU Block Diagram

5.2 Clock system

A31G11x series has two main operating clocks. One is HCLK, which supplies the clock to the CPU and AHB bus system. The other one is PCLK, which supplies the clock to the peripheral systems.

Users can control the clock system variation by software. Figure 17 shows the clock system of A31G11x series and Table 12 shows the descriptions for clock sources.

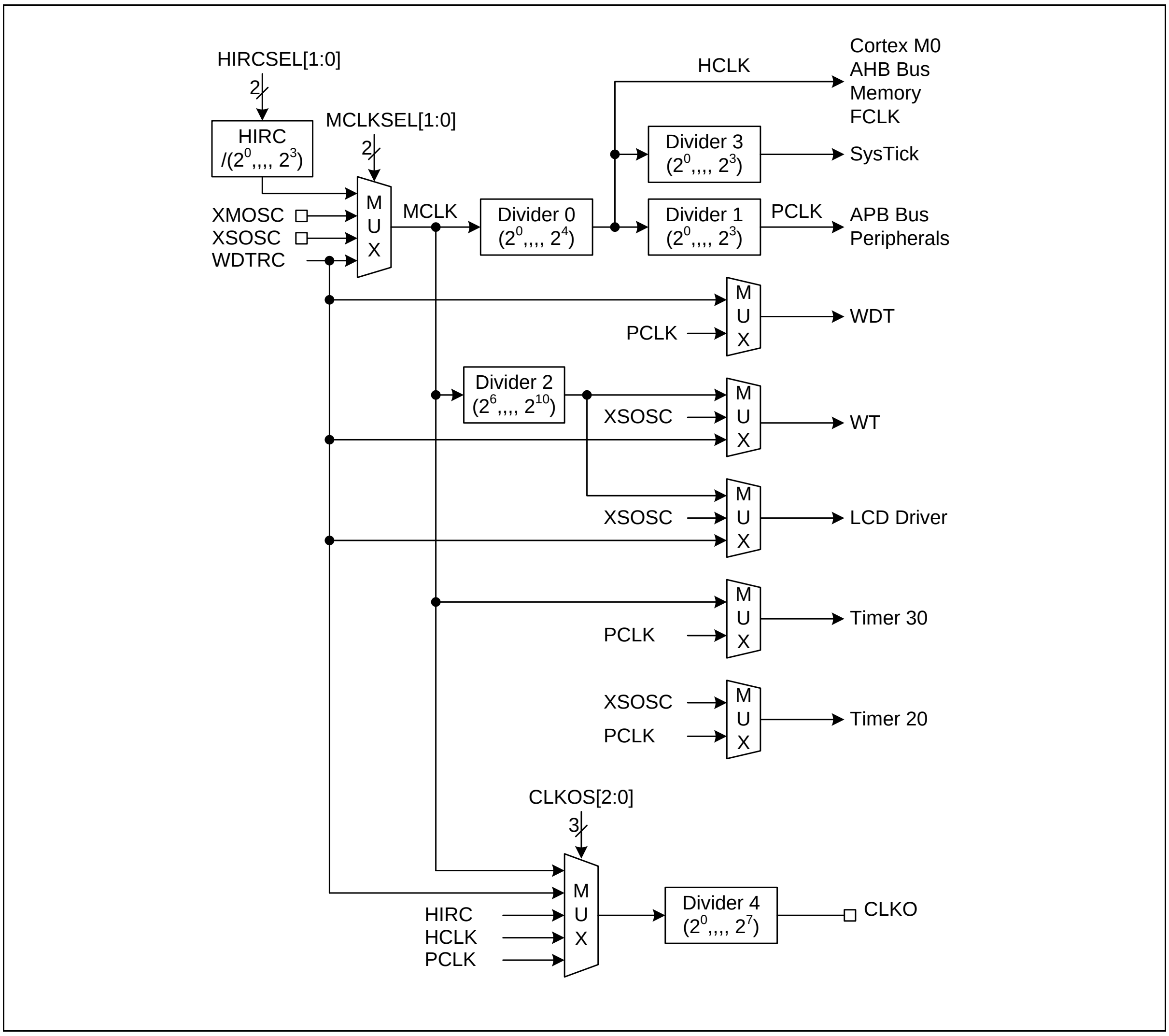


Figure 17. Clock Source Configuration

Each mux to switch clock source has a glitch-free circuit. So a clock can be switched without glitch risks. When you change the clock mux control, be sure both clock sources are alive. If either is not alive, clock change operation stops and system will shut down and not recover.

Table 12. Clock Sources

Clock name	Mnemonic	Frequency	Description
Main OSC	XMOSC	• X-TAL (2MHz to 16MHz) • External Clock (2MHz to 40MHz)	• External Main Crystal OSC • External Main Clock
Sub OSC	XSOSC	X-TAL (32.768kHz)	External Sub Crystal OSC
Internal RC OSC	HIRC	2.5MHz to 40MHz	High Frequency Internal RC OSC
WDT RC OSC	WDTRC	40kHz	Watchdog Timer RC OSC

5.2.1 HCLK clock domain

HCLK clock feeds the clock to the CPU and AHB bus. Cortex-M0+ CPU requires 2 clocks, FCLK and HCLK. FCLK is a free running clock and is always running except during power down mode. HCLK can be stopped during sleep mode.

The HCLK clock operates the BUS system and memory systems. Max BUS operating clock speed is 40MHz. HCLK frequency should be limited to a frequency of 40MHz or lower.

5.2.2 Miscellaneous clock domain

Various clock sources are required for each functional block. The SCU provides clock source selectivity with dedicated pre-scaler for each functional block. The clock selection mux does not support glitch-free function, so the clock is unpredictable during clock selection. Figure 18 shows the configurations for miscellaneous clocks.

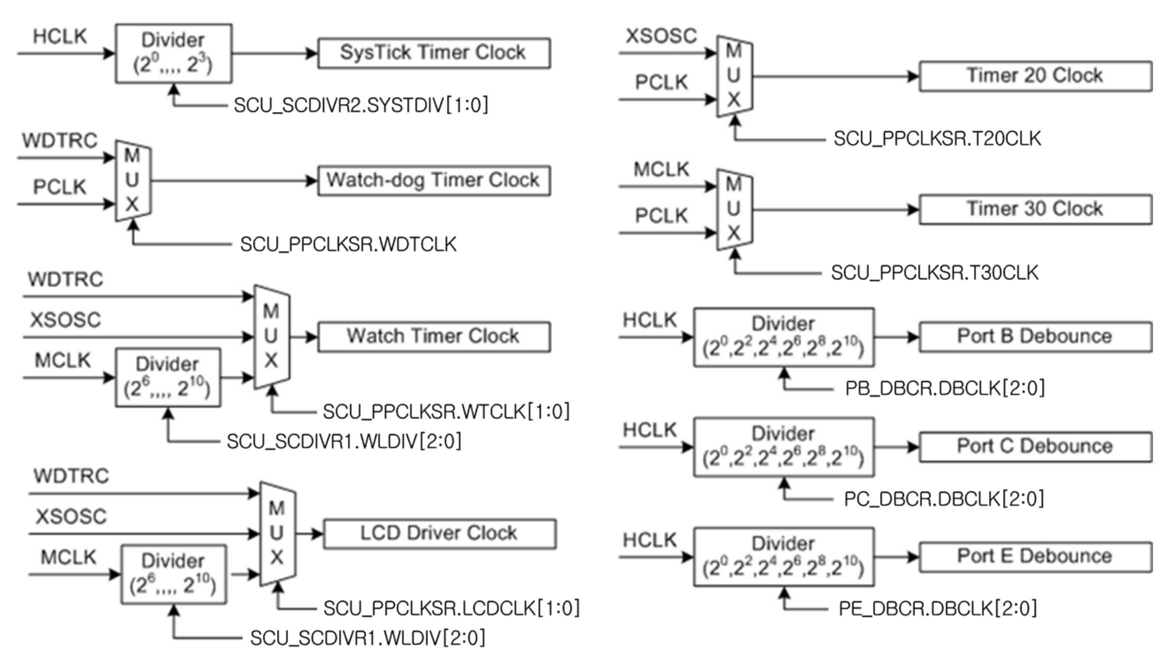


Figure 18. Miscellaneous Clock Configuration

5.2.3 PCLK clock domain

PCLK is the master clock for all the peripherals except for the CRC generator and ports. It can shut down during power down mode. Each peripheral clock is generated by SCU_PPCLKEN1 and SCU_PPCLKEN2 register set. Figure 17 illustrates the PCLK clock distributions. The peripherals are not accessible even by reading its registers until each PCLK clock of each block is enabled.

5.2.4 Clock configuration procedure

After power on the device, a default system clock is generated by HIRC (2.5MHz) clock. The HIRC is enabled by default during power up sequence. Other clock sources are enabled by user controls and configuration options with a system clock.

XMOSC and XSOSC clocks are enabled by XMOSCEN and XSOSCEN bits of SCU_CLKSRCR register respectively. Before enabling XMOSC and XSOSC blocks, the pin mux configuration should be set for XIN/XOUT and SXIN/SXOUT functions. PF0/PF1 and PF2/PF3 pins are shared by XMOSC’s XIN/XOUT function and XSOSC’s SXIN/SXOUT function – PF_MOD and PF_AFSR1 registers should be configured properly.

After enabling the XMOSC and XSOSC blocks, a user can check stability of crystal oscillation through a clock monitoring control register, SCU_CMONCR. It takes more than 1ms to ensure stable crystal oscillation before changing the system clock.

Figure 19 shows an example flow chart to configure the system clock to XMOSC and XSOSC clock.

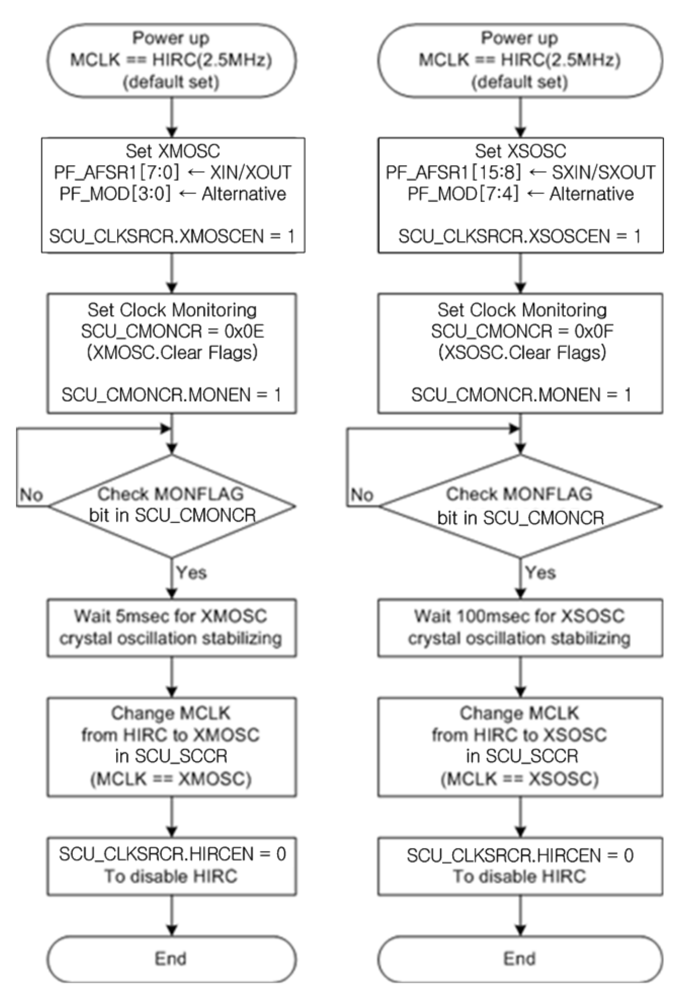


Figure 19. Clock Configuration Procedure

5.3 Reset

A31G11x series has two system resets. One is the cold reset by POR, which is effective during power up or down sequence. The other is the warm reset, generated by several reset sources. The reset event makes the device to turn back to its initial state.

The cold reset has only one reset source, which is POR, while the warm reset has several reset sources as shown below:

- nRESET pin
- WDT reset
- LVR reset
- MON reset
- S/W reset
- CPU request reset

5.3.1 Cold reset

The cold reset is one of important feature of the A31G11x series when it powers up. This characteristic will globally affect the system boot.

Internal VDC is enabled when VDD power is turned on. Internal VDD level slope follows the External VDD power slope. Internal POR trigger level is at 1.2V of the internal VDC voltage. At this time, boot operation begins.

Internal RC clock turns on and counts 4ms for internal VDC level to stabilize. At this time, external VDD voltage level should be bigger than initial LVR level (1.62V). After 4ms of counting, the CPU reset is released and operation begins.

Figure 20 shows waveform of power up sequence and internal reset.

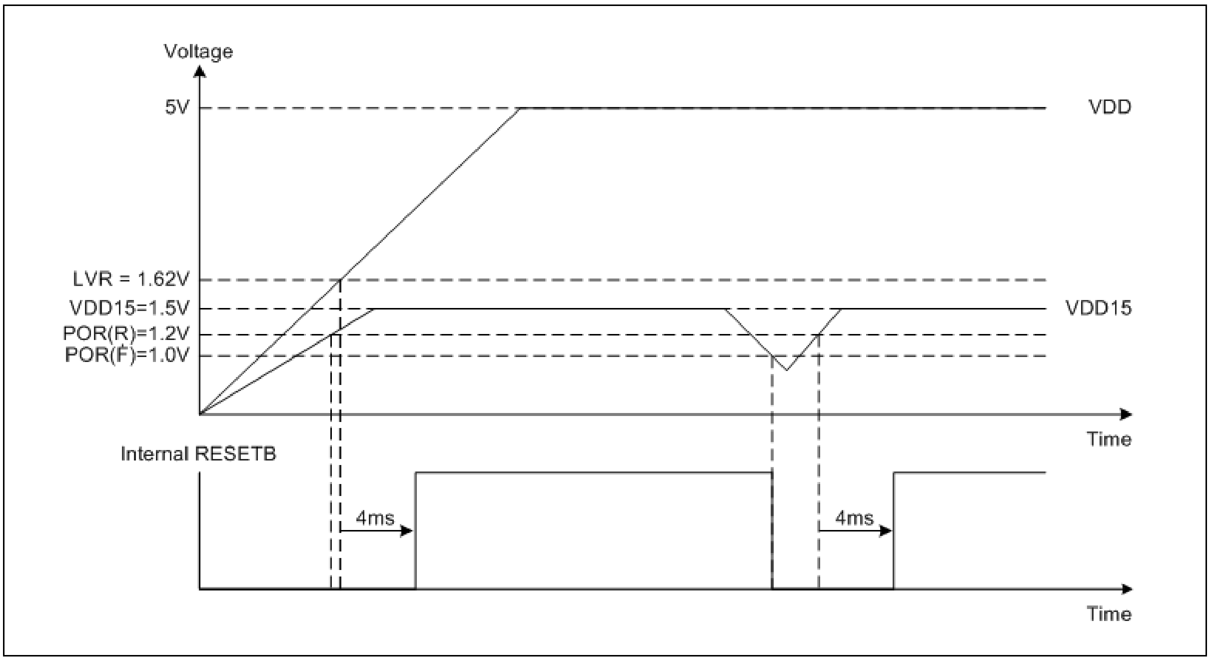


Figure 20. Power-up POR Sequence

A register SCU_RSTSSR shows the POR reset status. The last reset comes from the POR. SCU_RSTSSR.PORSTA is set to '1'. After power on, this bit is always '1' if the bit is not cleared by S/W. If abnormal internal voltage drop is detected during normal operation, the system will be reset and this bit also will be set to '1'.

When the cold reset is applied, the entire device returns to its initial state.

5.3.2 Warm reset

The warm reset event has several reset sources and some parts of the device return to their initial states when the warm reset takes place.

The warm reset status appears in a register SCU_RSTSSR. A reset for each peripheral block is controlled by a register SCU_PPRST. The reset can be masked independently.

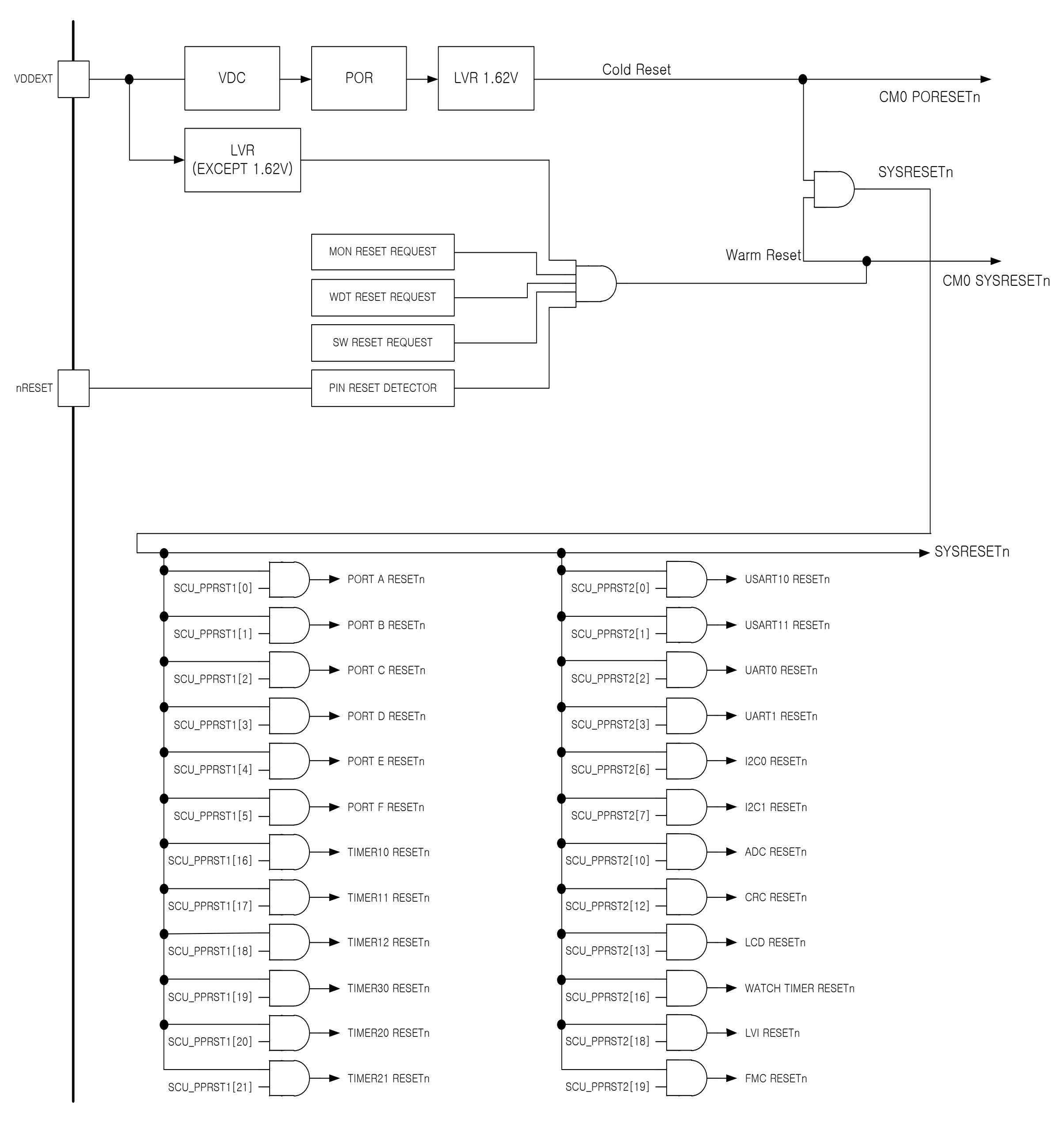


Figure 21. Reset Configuration

5.3.3 LVR reset

The LVR voltage level is set by a low voltage reset configuration register (CONF_LVRCNFIG) in the configuration option page 1.

LVR reset status appears in a register SCU_RSTSSR. The reset for LVR is controlled by a register SCU_LVRCR. The register is cleared to “0x00” on POR reset.

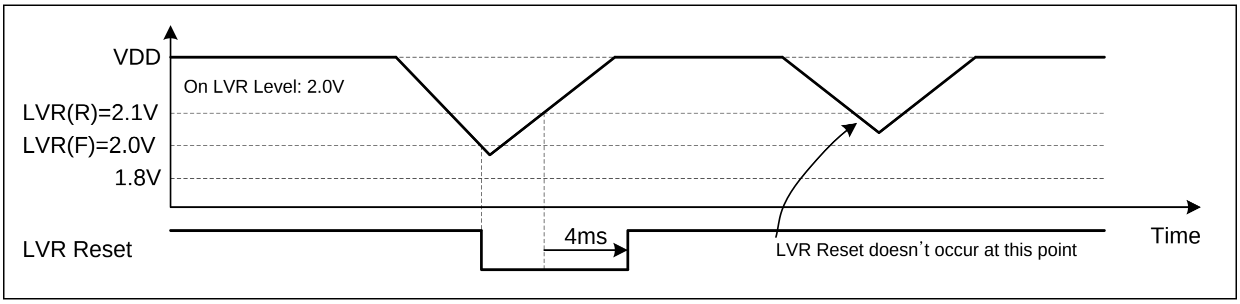


Figure 22. LVR Reset Timing Diagram

5.4 Operation mode

INIT mode is the initial state of the device when reset. At RUN mode, the chip runs at its max CPU performance with a high-speed clock system. At SLEEP and DEEP SLEEP mode, the chip runs at a low power consumption mode. The system saves power by halting the processor core and unused peripherals.

Figure 23 shows the operation mode transition diagram.

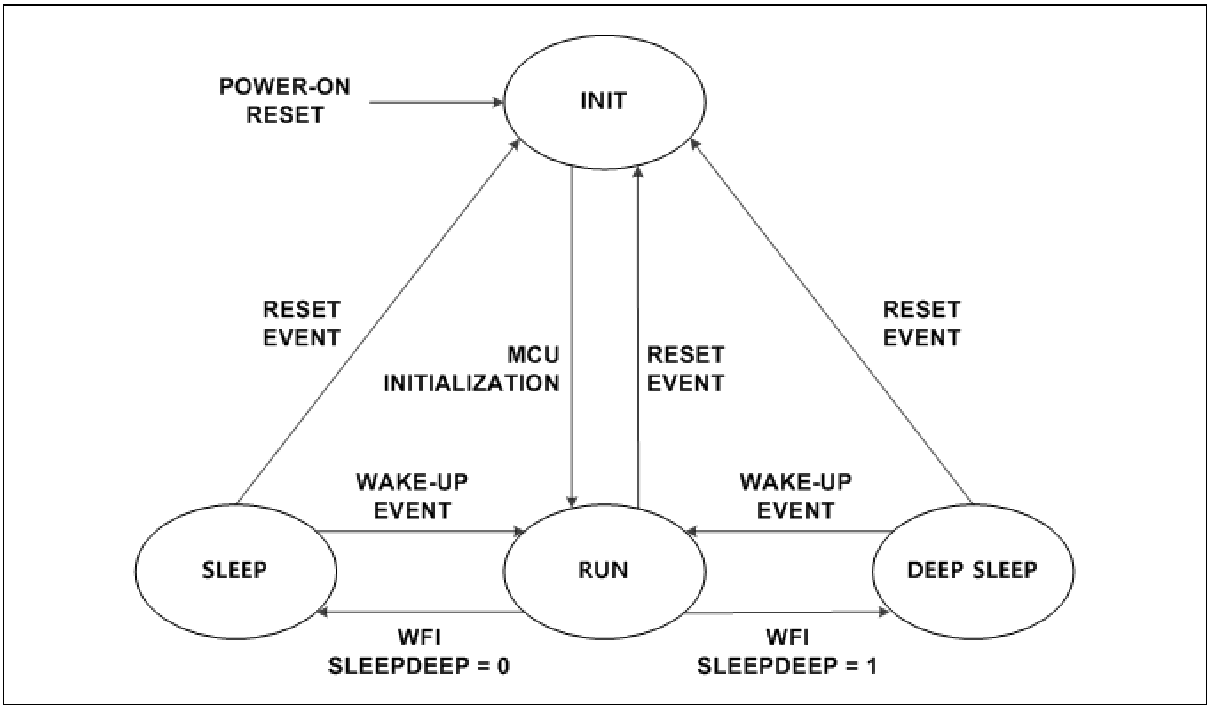


Figure 23. Operating Mode

5.4.1 Run mode

This mode is to operate CPU core and peripheral hardware with a high-speed clock. The device enters in the INIT state after reset, and then enters in the RUN mode.

5.4.2 Sleep mode

The device stops only CPU in this mode. Each peripheral function turns on by a function enable bit and a clock enable bit of the register SCU_PPCLKEN.

5.4.3 Deep sleep mode

The device stops not only CPU but also a selected system clock (MCLK) in this mode. Watch timer with sub clock and watchdog timer with WDTRC still operate in this mode.

Table 13. Functional table on current mode

IP	Main Run (IDD1)	Main Sleep (IDD2)	Sub Run (IDD3)	Sub Sleep (IDD4)	Deep Sleep (IDD5)
CPU	O	X	O	X	X
FLASH	O	X	O	X	X
SRAM	O	X	O	X	X
FMC	Optional	X	Optional	X	X
CRC	Optional	X	Optional	X	X
POR	O	O	O	O	O
LVR/LVI	Optional	Optional	Optional	Optional	Optional
GPIO	Optional	Optional	Optional	Optional	Optional
SCU	O	O	O	O	O
I2C	Optional	Optional	Optional	Optional	X
USART	Optional	Optional	Optional	Optional	Optional
UART	Optional	Optional	Optional	Optional	X
SysTick	Optional	Optional	Optional	Optional	X
T10 – T12	Optional	Optional	Optional	Optional	X
T20	Optional	Optional	Optional	Optional	Optional
T21	Optional	Optional	Optional	Optional	X
T30	Optional	Optional	Optional	Optional	X
WDT	Optional	Optional	Optional	Optional	Optional^{NOTE3}
WUT	O	O	O	O	X
ADC	Optional	Optional	X	X	X
LCD Driver	Optional	Optional	Optional	Optional	Optional
WT	Optional	Optional	Optional	Optional	Optional
HIRC	Optional	Optional	X	X	X
WDTRC	Optional	Optional	Optional	Optional	Optional
XMOSC	Optional	Optional	X	X	X
XSOSC	Optional	Optional	Optional	Optional	Optional

NOTES:

1. O: Enable, X: Disable, Optional: A function can be disabled/enabled by s/w.
2. It can be woken up from sleep and deep sleep modes by an interrupt source of the optional peripherals.
3. The watch-dog timer interrupt source can't be used as a wake-up source in the deep sleep mode. But the watch-dog timer can run in the deep sleep mode.

5.5 Pin description for SCU

Table 14. Pins and External Signals for SCU

PIN NAME	TYPE	DESCRIPTION
nRESET	I	External Reset Input
XIN/XOUT	OSC	External Crystal Oscillator for Main Clock
SXIN/SXOUT	OSC	External Crystal Oscillator for Sub Clock
CLKO	O	Clock Output Monitoring Signal

5.6 Registers

Base address and register map of SCU (chip configuration) are shown in Table 15 and Table 16.

Table 15. Base Address of SCU (Chip Configuration)

Name	Base address
SCU (chip configuration)	0x4000_F000

Table 16. SCU Register Map (Chip Configuration)

Name	Offset	Type	Description	Reset Value
SCU_VENDORID	0x0000	R	Vendor Identification Register	0x41424F56
SCU_CHIPID	0x0004	R	Chip Identification Register, Where n = 0 or 1.	0x4D31F00n
SCU_REVNR	0x0008	R	Revision Number Register	0x000000xx
–	–	–	Reserved	–
SCU_PMREMAP	0x0014	RW	Program Memory Remap Register	0x00000000
SCU_BTPSCR	0x0018	RW	Boot Pin Status and Control Register	0x000000xx
SCU_RSTSSR	0x001C	RW	Reset Source Status Register	0x000000xx
SCU_NMISRCR	0x0020	RW	NMI Source Selection Register	0x00000000
SCU_SWRSTR	0x0024	R	Software Reset Register	0x00000000
SCU_SRSTVR	0x0028	R	System Reset Validation Register	0x00000055
SCU_WUTCR	0x002C	RW	Wake-up Timer Control Register	0x00000000
SCU_WUTDR	0x0030	RW	Wake-up Timer Data Register	0x00000138
–	–	–	Reserved	–
SCU_HIRCTRM	0x00A8	RW	High Frequency Internal RC Trim Register (HIRCNFIG)	0x000000xx
SCU_WDTRCTRM	0x00AC	RW	Watchdog Timer RC Trim Register (WDTRCNFIG)	0x000000xx

NOTE: The CHIPID is written by H/W if the proper configure address is read.

Base address and register map of SCU (clock generation) are shown in Table 17 and Table 18.

Table 17. Base Address of SCU (Clock Generation)

Name	Base address
SCU (clock generation)	0x4000_1800

Table 18. SCU Register Map (Clock Generation)

Name	Offset	Type	Description	Reset Value
SCU_SCCR	0x0000	RW	System Clock Control Register	0x00000000
SCU_CLKSRCR	0x0004	RW	Clock Source Control Register	0x0000000C
SCU_SCDIVR1	0x0008	RW	System Clock Divide Register 1	0x00000000
SCU_SCDIVR2	0x000C	RW	System Clock Divide Register 2	0x00000000
SCU_CLKOCR	0x0010	RW	Clock Output Control Register	0x00000000
SCU_CMONCR	0x0014	RW	Clock Monitoring Control Register	0x00000000
SCU_PPCLKEN1	0x0020	RW	Peripheral Clock Enable Register 1	0x00000000
SCU_PPCLKEN2	0x0024	RW	Peripheral Clock Enable Register 2	0x00020000
SCU_PPCLKSR	0x0040	RW	Peripheral Clock Selection Register	0x00000000
SCU_PPRST1	0x0060	RW	Peripheral Reset Register 1	0x00000000
SCU_PPRST2	0x0064	RW	Peripheral Reset Register 2	0x00000000
SCU_XTFLSR	0x0080	RW	X-tal Filter Selection Register	0x00000005

Base address and register map of SCU (LVR/LVI) are shown in Table 19 and Table 20.

Table 19. Base Address of SCU (LVR/LVI)

Name	Base address
SCU (LVR/LVI)	0x4000_5100

Table 20. SCU Register Map (LVR/LVI)

Name	Offset	Type	Description	Reset Value
SCU_LVICR	0x0000	RW	Low Voltage Indicator Control Register	0x00000000
SCU_LVRCR	0x0004	RW	Low Voltage Reset Control Register	0x00000000

5.6.1 SCU_VENDORID: vendor ID register

SCU_VENDORID register shows Vendor identification information. This register is a 32-bit read-only register.

SCU_CIDR=0x4000_F000

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="32">VENDID</td></tr>
<tr><td colspan="32">0x4142_4F56</td></tr>
<tr><td colspan="32">RO</td></tr>
</table>

31 0	VENDID	Vendor Identification bits. 0x4142_4F56

5.6.2 SCU_CHIPID: chip ID register

SCU_CHIPID register shows chip identification information. This register is a 32-bit read-only register.

SCU_CHIPID=0x4000_F004

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="32">CHIPID</td></tr>
<tr><td colspan="32">0x4D31F000 or 0x4D31F001</td></tr>
<tr><td colspan="32">RO</td></tr>
</table>

31 0	CHIPID	Chip Identification bits.	
		0x4D31F000	A31G112 (32KB Flash ROM)
		0x4D31F001	A31G111 (16KB Flash ROM)

5.6.3 SCU_REVNR: revision number register

SCU_REVNR register is a 32-bit read-only register. This register is accessible in 32/16/8-bit.

SCU_REVNR=0x4000_F008

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="24">Reserved</td><td colspan="8">REVNO</td></tr>
<tr><td colspan="24">0x000000</td><td colspan="8">xx</td></tr>
<tr><td colspan="24">–</td><td colspan="8">RO</td></tr>
</table>

7 0	REVNO	Chip Revision Number. This value is assigned by the manufacturer.

5.6.4 SCU_PMREMAP: program memory remap register

SCU_PMREMAP register is 32-bit size.

SCU_PMREMAP=0x4000_F014

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">WTIDKY</td><td colspan="8">nPMREM</td><td colspan="8">PMREM</td></tr>
<tr><td colspan="16">0x0000</td><td colspan="8">0x00</td><td colspan="8">0x00</td></tr>
<tr><td colspan="16">WO</td><td colspan="8">WO</td><td colspan="8">RW</td></tr>
</table>

31 16	WTIDKY	Write Identification Key When writing, write 0xE2F1 to these bits, or else writing is ignored.	
15 8	nPMREM	Write Complement Key When writing, write the complement value of PMREM[7:0], or else writing is ignored.	
7 0	PMREM	Program Memory Remap.	
		0x69	Boot ROM is re-mapped to address 0x00000000. 0x10001000 of Flash memory is re-mapped to address 0x00001000.
		Others	Flash memory is re-mapped to address 0x00000000.
		NOTE: The remapped program memory can be accessed from the original address.	

5.6.5 SCU_BTPSCR: boot pin status and control register

SCU_BTPSCR register is 32-bit size and accessible in 32/16/8-bit.

SCU_BTPSCR=0x4000_F018

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="24">Reserved</td><td>Reserved</td><td colspan="2">BFIND</td><td colspan="4">Reserved</td><td>BTPSTA</td></tr>
<tr><td colspan="24">0x000000</td><td>0</td><td colspan="2">xx</td><td colspan="4">0000</td><td>x</td></tr>
<tr><td colspan="24">–</td><td>-</td><td colspan="2">RW</td><td colspan="4">-</td><td>RO</td></tr>
</table>

6 5	BFIND	BOOT Pin Function Indicator. The BFIND[1:0] bits are cleared to "00" by POR, the BFIND[1] bit is cleared to '0' by nRESET, and the bits are not cleared by other system reset. One of the two of the following must be set in the BFIND[1:0] bits to check whether ISP is needed or not.	
		10	Check the BOOT pin when the system resets by nRESET including POR.
		11	Check the BOOT pin when the system resets only by POR.
0	BTPSTA	BOOT Pin Status.	
		0	The BOOT pin is low level.
		1	The BOOT pin is high level.
		Note) This bit is always '1' if the BOOT pin is not selected for alternative function.	

NOTE: When a system reset occurs, the PB3 pin is configured as alternative function for BOOT, the pull-up resistor is enabled, and the debounce filter is enabled.

5.6.6 SCU_RSTSSR: reset source status register

SCU_RSTSSR register shows reset source information when reset event is occurred. '1' implies a reset event exists, while '0' means a reset event does not exist for a corresponding reset source.

When a reset source is detected, '1' is written into the corresponding bit position and reset status will be cleared.

SCU_RSTSSR register is 32-bit size and accessible in 32/16/8-bit.

SCU_RSTSSR=0x4000_F01C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								**Reserved**		**MONSTA**	**SWSTA**	**EXTSTA**	**WDTSTA**	**LVRSTA**	**PORSTA**
0x000000																								**00**		**x**	**x**	**x**	**x**	**x**	**x**
-																								**-**		**RW**	**RW**	**RW**	**RW**	**RW**	**RW**

5	MONSTA	Clock Monitoring Reset Status.	
		0	Not detected
		1	Clock monitoring reset is detected. The bit is cleared to '0' when '1' is written.
4	SWSTA	Software Reset Status.	
		0	Not detected
		1	Software reset is detected. The bit is cleared to '0' when '1' is written.
3	EXTSTA	External Pin Reset Status.	
		0	Not detected
		1	External pin reset is detected. The bit is cleared to '0' when '1' is written.
2	WDTSTA	Watchdog Timer Reset Status.	
		0	Not detected
		1	Watchdog timer reset is detected. The bit is cleared to '0' when '1' is written.
1	LVRSTA	LVR Reset Status.	
		0	Not detected
		1	LVR reset is detected. The bit is cleared to '0' when '1' is written.
0	PORSTA	POR Reset Status.	
		0	Not detected
		1	POR reset is detected. The bit is cleared to '0' when '1' is written.

NOTES:

1. The PORSTA bit is set to '1' and the other bits are cleared to '0' when power-on reset occurs.
2. The corresponding reset status bit may be set to '1' if any reset signal is asserted during power-on reset takes place. For example, The EXTSTA bit may be set if the external reset is asserted during POR.

5.6.7 SCU_NMISRCR: NMI source selection register

SCU_NMISRCR is the non-maskable interrupt configuration register, which can be set by software. SCU_NMISRCR register is 32-bit size, and accessible in 32/16/8-bit.

SCU_NMISRCR=0x4000_F020

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7	6	5	4 3 2 1 0
Reserved	**NMICON**	**MONINT**	**Reserved**	**NMISRC**
0x000000	**0**	**0**	**0**	**00000**
-	**RW**	**RW**	**-**	**RW**

7	NMICON	Non-Maskable Interrupt (NMI) Control.	
		0	Disable NMI
		1	Enable NMI
6	MONINT	Clock Monitoring Interrupt Selection.	
		0	Non-select clock monitoring interrupt for NMI source
		1	Select clock monitoring interrupt for NMI source
4 0	NMISRC	Non-Maskable Interrupt Source Selection. Select one of the interrupt sources 0 to 31 for NMI source.	

NOTE: The interrupt source which is selected for NMI should be disabled in NVIC to avoid both generation of the normal and NMI interrupts.

5.6.8 SCU_SWRSTR: software reset register

SCU_SWRSTR register is 32-bit size.

SCU_SWRSTR=0x4000_F024

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
WTIDKY	**Reserved**	**SWRST**
0x0000	**0x00**	**0x00**
WO	-	**WO**

31 16	WTIDKY	Write Identification Key When writing, write 0x9EB3 to these bits, or else writing is ignored.	
7 0	SWRST	Software Reset (System Reset)	
		0x2D	A software reset will be generated for all peripheral and core.
		Others	No effect

5.6.9 SCU_SRSTVR: system reset validation register

SCU_SRSTVR register is 32-bit size, and accessible in 32/16/8-bit.

SCU_SRSTVR=0x4000_F028

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved	**VALID**
0x000000	**0x55**
-	**RO**

7 0	VALID	System Reset Validation.	
		0x55	System reset is O.K.
		Others	A weak system reset. A system reset must be generated by S/W

5.6.10 SCU_WUTCR: wake-up timer control register

Wake-up timer always works on operating mode. This timer gives a stable time for clock generation during Power on and Deep sleep mode release. The main purpose of this timer is periodical tick timer or a wake-up source.

SCU_WUTCR register is 32-bit size, and accessible in 32/16/8-bit.

SCU_WUTCR=0x4000_F02C

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7	6 5 4 3 2	1	0
Reserved	**WUTIEN**	**Reserved**	**CNTRLD**	**WUTIFLAG**
0x000000	**0**	**00000**	**0**	**0**
–	**RW**	**-**	**RW**	**RW**

7	WUTIEN	Wake-up Timer Interrupt Enable bit	
		0	Disable wake-up timer interrupt
		1	Enable wake-up timer interrupt
1	CNTRLD	Counter Reload bit	
		0	No effect
		1	Reload data to counter (Automatically cleared to '0' after operation)
0	WUTIFLAG	Wake-up Timer Interrupt Flag bit	
		0	No request occurred
		1	Request occurred. The bit is cleared to '0' when '1' is written.

5.6.11 SCU_WUTDR: wake-up timer data register

SCU_WUTDR register is 32-bit size and accessible in 32/16/8-bit.

SCU_WUTDR=0x4000_F030

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Reserved	**WUTDATA**
0x0000	**0x0138**
–	**RW**

15 0	WUTDATA	Wake-up Timer Data. The range is 0x0001 to 0xFFFF. **NOTE**: Its value should be set to at least more than 150µs.

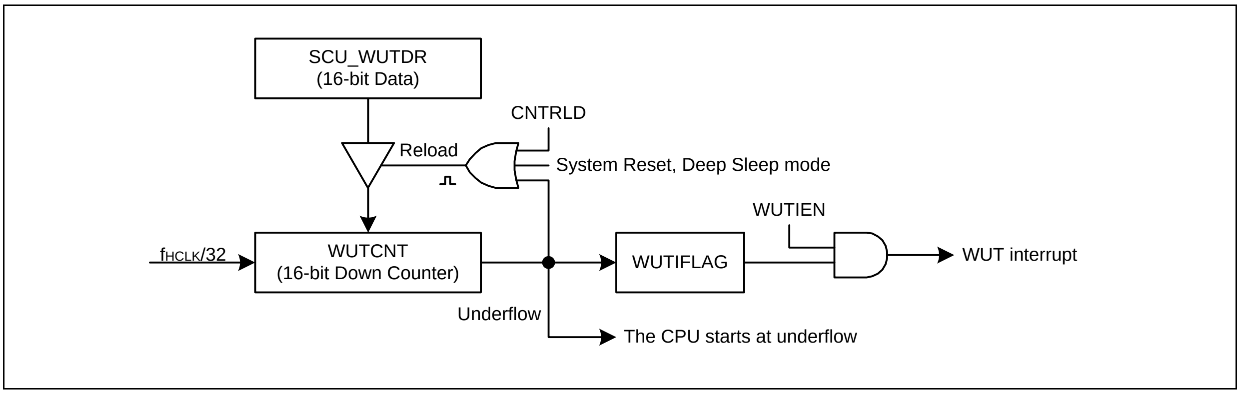


Figure 24. Wake-up Timer Block Diagram

5.6.12 SCU_HIRCTRM: high frequency internal RC trim register

SCU_HIRCTRM register may be used for user trimming of HIRC by s/w. This register is 32-bit size.

SCU_HIRCTRM=0x4000_F0A8

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">WTIDKY</td><td colspan="8">nTRMH</td><td colspan="3">CTRMH</td><td colspan="5">FTRMH</td></tr>
<tr><td colspan="16">0x0000</td><td colspan="8">xx</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr>
<tr><td colspan="16">WO</td><td colspan="8">WO</td><td colspan="3">RO</td><td colspan="5">RW</td></tr>
</table>

31 16	WTIDKY	Write Identification Key When writing, write 0xA6B5 to these bits, or else writing is ignored.
15 8	nTRMH	Write Complement Key When writing, write the complement value of LSB(CTRMH+FTRMH), or else writing is ignored.
7 5	CTRMH	Factory HIRC Coarse Trim. These bits are fixed by manufacturer and read from "Configure Option Page 0" when the system resets.
4 0	FTRMH	Factory HIRC Fine Trim. These bits are fixed by manufacturer and read from "Configure Option Page 0" when a system reset occurs. These bits provide a user programmable trimming value on operation. The range is -16 to +15, the FTRMH[4] is sign bit, and the frequency is changed by about 140kHz steps.

5.6.13 SCU_WDTRCTRM: watchdog timer RC trim register

SCU_WDTRCTRM register may be used for user trimming of WDTRC by s/w. This register is 32-bit size.

SCU_WDTRCTRM=0x4000_F0AC

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="16">WTIDKY</td><td colspan="8">nTRMW</td><td colspan="4">CTRMW</td><td>Reserved</td><td colspan="3">FTRMW</td></tr>
<tr><td colspan="16">0x0000</td><td colspan="8">xx</td><td>x</td><td>x</td><td>x</td><td>x</td><td>0</td><td>x</td><td>x</td><td>x</td></tr>
<tr><td colspan="16">WO</td><td colspan="8">WO</td><td colspan="4">RW</td><td>–</td><td colspan="3">RW</td></tr>
</table>

31 16	WTIDKY	Write Identification Key When writing, write 0x4C3D to these bits, or else writing is ignored.
15 8	nTRMW	Write Complement Key When writing, write the complement value of LSB(CTRMW+FTRMW), otherwise the write is ignored.
7 4	CTRMW	Factory WDTRC Coarse Trim. These bits are fixed by manufacturer and read from “Configure Option Page 0” when the system resets. These bits provide a user-programmable trimming value on operation. The range is -8 to +7, the CTRMW[3] is sign bit, and the frequency is changed by about 4kHz steps.
2 0	FTRMW	Factory WDTRC Fine Trim. These bits are fixed by manufacturer and read from “Configure Option Page 0” when the system resets. These bits provide a user-programmable trimming value on operation. The range is -4 to +3, the FTRMW[2] is sign bit, and the frequency is changed by about 1.1kHz steps.

5.6.14 SCU_SCCR: system clock control register

A31G11x series has multiple clock sources to generate internal operating clocks. SCU_SCCR register controls such a clock source.

This register is 32-bit size.

SCU_SCCR=0x4000_1800

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2	1 0
WTIDKY	**Reserved**		**MCLKSEL**
0x0000	**0x00**	**0 0 0 0 0 0**	**0 0**
WO	**–**	**–**	**RW**

31	WTIDKY	Write Identification Key	
16		When writing, write 0x570A to these bits, or else writing is ignored.	
1	MCLKSEL	Main Clock Selection, MCLK	
0		00	High frequency Internal RC oscillator (40MHz), HIRC
		01	External main oscillator (2 – 40MHz), XMOSC
		10	External sub oscillator (32.768kHz), XSOSC
		11	Internal watchdog timer RC oscillator (40kHz), WDTRC

NOTES:

1. The MCLKSEL bits will not be changed on selecting the clock which is disabled by SCU_CLKSRCR register.
2. If the MCLKSEL bits are "10" or "11", the HDIV[2:0] bits of SCU_SCDIVR1 register should be "100" for non-divided system clock.

5.6.15 SCU_CLKSRCR: clock source control register

A31G11x series has multiple clock sources to generate internal operating clocks. SCU_CLKSRCR register controls each clock source.

This register is 32-bit size.

SCU_CLKSRCR=0x4000_1804

<table>
<tr><td colspan="16">31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">WTIDKY</td><td colspan="2">Reserved</td><td colspan="2">HIRCSEL</td><td colspan="3">Reserved</td><td>XMFRNG</td><td colspan="4">Reserved</td><td>WDTRCEN</td><td>HIRCEN</td><td>XMOSCEN</td><td>XSOSCEN</td></tr>
<tr><td colspan="16">0x0000</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td colspan="16">WO</td><td>-</td><td>-</td><td colspan="2">RW</td><td>-</td><td>-</td><td>-</td><td>RW</td><td>-</td><td>-</td><td>-</td><td>-</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td></tr>
</table>

31 16	WTIDKY	Write Identification Key	
		When writing, write 0xA507 to these bits, or else writing is ignored.	
13 12	HIRCSEL	HIRC Frequency Selection bits	
		00	40MHz HIRC
		01	20MHz HIRC
		10	10MHz HIRC
		11	5MHz HIRC
8	XMFRNG	Main Oscillator Type and Frequency Range Selection bit	
		0	x-tal for XMOSC, 2 to 16MHz
		1	External clock for XMOSC, 2MHz to 40MHz
3	WDTRCEN	WDTRC Enable bit, Watchdog timer RC oscillator	
		0	Disable WDTRC
		1	Enable WDTRC
2	HIRCEN	HIRC Enable bit, High frequency internal RC oscillator	
		0	Disable HIRC
		1	Enable HIRC
1	XMOSCEN	XMOSC Enable bit, External main oscillator	
		0	Disable XMOSC
		1	Enable XMOSC
0	XSOSCEN	XSOSC Enable bit, External sub oscillator	
		0	Disable XSOSC
		1	Enable XSOSC

NOTE: The clock selected as a main system clock by SCU_SCCR register will not be changed by the corresponding bit.

5.6.16 SCU_SCDIVR1: system clock divide register 1

SCU_SCDIVR1 register is 32-bit size and accessible in 32/16/8-bit.

SCU_SCDIVR1=0x4000_1808

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																									**WLDIV**			**Reserved**	**HDIV**		
0x000000																									**0**	**0**	**0**	**0**	**0**	**0**	**0**
–																									**RW**			**–**	**RW**		

6 4	WLDIV	Clock Divide bits for Watch Timer and LCD Driver, Divider 2 (Refer to figure 17)	
		000	MCLK÷64
		001	MCLK÷128
		010	MCLK÷256
		011	MCLK÷512
		100	MCLK÷1024
		others	Reserved
2 0	HDIV	Clock Divide bits for HCLK, Divider 0 (Refer to figure 17)	
		000	MCLK÷16
		001	MCLK÷8
		010	MCLK÷4
		011	MCLK÷2
		100	MCLK÷1
		others	Reserved (MCLK÷1)

NOTES:

1. If the selected MCLK is XSOSC or WDTRC, the HDIV[2:0] bits should be set to “100”.
2. The frequency range of HCLK should be 2.5 to 40[MHz] by s/w while the HIRC is the system clock.

5.6.17 SCU_SCDIVR2: system clock divide register 2

SCU_SCDIVR2 register is 32-bit size and accessible in 32/16/8-bit.

SCU_SCDIVR2=0x4000_180C

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="26">Reserved</td><td colspan="2">SYSTDIV</td><td colspan="2">Reserved</td><td colspan="2">PDIV</td></tr>
<tr><td colspan="26">0x000000</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="26">–</td><td colspan="2">RW</td><td>–</td><td>–</td><td colspan="2">RW</td></tr>
</table>

5 4	SYSTDIV	Clock Divide bits for SysTick Timer, Divider 3 (Refer to figure 17)	
		00	HCLK÷1
		01	HCLK÷2
		10	HCLK÷4
		11	HCLK÷8
1 0	PDIV	Clock Divide bits for PCLK, Divider 1 (Refer to figure 17)	
		00	HCLK÷1
		01	HCLK÷2
		10	HCLK÷4
		11	HCLK÷8

NOTE: If the selected MCLK is XSOSC or WDTRC, the PDIV[1:0] should be set to “00”.

5.6.18 SCU_CLKOCR: clock output control register

A31G11x series can drive the clock from a selected clock (CLKOS) with a dedicated post divider.

SCU_CLKOCR register is 32-bit size and accessible in 32/16/8-bit.

SCU_CLKOCR=0x4000_1810

31–8	7	6	5	4	3	2	1	0
Reserved	**CLKOEN**	**POLSEL**	**CLKODIV**			**CLKOS**		
0x000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
-	**RW**	**RW**	**RW**			**RW**		

7	CLKOEN	Clock Output Enable bit	
		0	Disable clock output
		1	Enable clock output
6	POLSEL	Clock Output Polarity Selection bit when disable	
		0	Low level during disable
		1	High level during disable
5 3	CLKODIV	Output Clock Divide bits, Divider 4 (Refer to figure 17)	
		000	"Selected clock"÷1
		001	"Selected clock"÷2
		010	"Selected clock"÷4
		011	"Selected clock"÷8
		100	"Selected clock"÷16
		101	"Selected clock"÷32
		110	"Selected clock"÷64
		111	"Selected clock"÷128
2 0	CLKOS	Clock Output Selection bits	
		000	MCLK
		001	WDTRC
		010	HIRC
		011	HCLK
		100	PCLK
		others	Reserved (None)

5.6.19 SCU_CMONCR: clock monitoring control register

Internal clock can be monitored by using internal WDTRC for security purpose.

SCU_CMONCR register is 32-bit size and accessible in 32/16/8-bit.

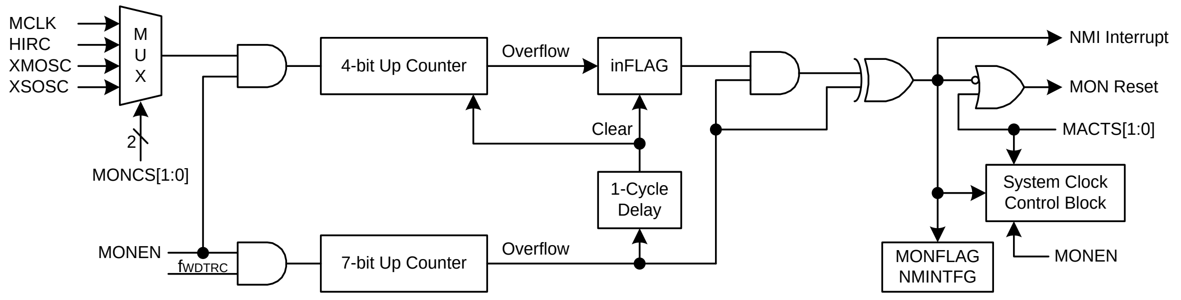
SCU_CMONCR=0x4000_1814

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Reserved	**MONEN**	**MACTS**		**Reserved**	**MONFLAG**	**NMINTFG**	**MONCS**	
0x000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
–	**RW**	**RW**		**-**	**RW**	**RW**	**RW**	

7	MONEN	Clock Output Enable bit	
		0	Disable clock monitoring
		1	Enable clock monitoring
		NOTE: When this bit is reset to ‘0’, the block clears the 4/7-bit counter, inFLAG, and flags.	
6 5	MACTS	Clock Monitoring Action Selection bits	
		00	No action by clock monitoring, but flags will be set/cleared on condition
		01	Reset generation by clock monitoring
		10	The system clock will be changed to the WDTRC regardless of MCLKSEL[1:0] bits of system clock control register (SCU_SCCR) only when the MCLK is selected for monitoring.
		11	Not used
3	MONFLAG	Clock Monitoring Result Flag bit	
		0	The clock under monitoring is not ready.
		1	The clock under monitoring is ready. This bit is cleared to ‘0’ when ‘1’ is written.
2	NMINTFG	Clock Monitoring Interrupt Flag bit (only when the MCLK is selected for monitoring)	
		0	No request occurred
		1	Request occurred. The bit is cleared to ‘0’ when ‘1’ is written.
		NOTE: When the bit is set, the system clock must be switched to WDTRC by S/W.	
1 0	MONCS	Monitored Clock Selection bits	
		00	MCLK
		01	HIRC
		10	XMOSC
		11	XSOSC

NOTES:

1. The block should be enabled after disable to clear the internal status for new clock monitoring.
2. This block must be disabled by S/W before entering deep sleep mode.
3. When the “clock monitoring” function is disabled by S/W, the following sequence is required.
   - First, the MACTS bits should be cleared to “00b”.
   - Second, the MONEN bit must be cleared to “0b”.



NOTE: WDTRC should be enabled to use this block since it is the watch clock for monitoring.

Figure 25. Clock Monitoring Circuit Diagram

5.6.20 SCU_PPCLKEN1: peripheral clock enable register 1

To use a certain peripheral unit, its clock should be activated by writing '1' to the corresponding bit in SCU_PPCLKEN1/SCU_PPCLKEN2 register. Until enabling the clock, the peripheral does not operate properly. To stop the clock of the peripheral unit, write '0' to the corresponding bit in the SCU_PPCLKEN1/PPCLKEN2 register.

SCU_PPCLKEN1 register is 32-bit size and accessible in 32/16/8-bit.

SCU_PPCLKEN1=0x4000_1820

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										T21CLKE	T20CLKE	T30CLKE	T12CLKE	T11CLKE	T10CLKE	Reserved										PFCLKE	PECLKE	PDCLKE	PCCLKE	PBCLKE	PACLKE
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	RW	RW	RW	RW	RW	RW	-	-	-	-	-	-	-	-	-	-	RW	RW	RW	RW	RW	RW

21	T21CLKE	TIMER21 clock enable
20	T20CLKE	TIMER20 clock enable
19	T30CLKE	TIMER30 clock enable
18	T12CLKE	TIMER12 clock enable
17	T11CLKE	TIMER11 clock enable
16	T10CLKE	TIMER10 clock enable
5	PFCLKE	Port F clock enable
4	PECLKE	Port E clock enable
3	PDCLKE	Port D clock enable
2	PCCLKE	Port C clock enable
1	PBCLKE	Port B clock enable
0	PACLKE	Port A clock enable

NOTE: The peripheral registers may not be read/written by software when the peripheral clock is disabled.

5.6.21 SCU_PPCLKEN2: peripheral clock enable register 2

SCU_PPCLKEN2 register is 32-bit size and accessible in 32/16/8-bit.

SCU_PPCLKEN2=0x4000_1824

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												FMCLKE	LVICLKE	WDTCLKE	WTCLKE	Reserved		LCDCLKE	CRCLKE	Reserved	ADCLKE	Reserved		I2C1CLKE	I2C0CLKE	Reserved		UT1CLKE	UT0CLKE	UST11CLKE	UST10CLKE
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	RW	RW	RW	RW	-	-	RW	RW	-	RW	-	-	RW	RW	-	-	RW	RW	RW	RW

19	FMCLKE	Flash Memory Control clock enable
18	LVICLKE	LVI (Low Voltage Indicator) clock enable
17	WDTCLKE	WDT (Watchdog Timer) clock enable. The WDTRC won’t be disabled if the clock is enabled by watchdog timer configuration register (CONF_WDTCNFIG) in “configure option page 1”
16	WTCLKE	WT (Watch Timer) clock enable
13	LCDCLKE	LCD Controller clock enable
12	CRCLKE	CRC (Cyclic Redundancy Check) clock enable
10	ADCLKE	ADC (Analog to Digital Converter) clock enable
7	I2C1CLKE	I2C1 (Inter-integrated Circuit) clock enable
6	I2C0CLKE	I2C0 (Inter-integrated Circuit) clock enable
3	UT1CLKE	UART1 clock enable
2	UT0CLKE	UART0 clock enable
1	UST11CLKE	USART11 clock enable
0	UST10CLKE	USART10 clock enable

NOTE: The peripheral registers may not be read/written by software when the peripheral clock is disabled.

5.6.22 SCU_PPCLKSR: peripheral clock selection register

SCU_PPCLKSR register is 32-bit size and accessible in 32/16/8-bit.

SCU_PPCLKSR=0x4000_1840

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="11">Reserved</td><td>T20CLK</td><td colspan="2">Reserved</td><td>T30CLK</td><td colspan="9">Reserved</td><td colspan="2">LCDCLK</td><td>Reserved</td><td colspan="2">WTCLK</td><td colspan="2">Reserved</td><td>WDTCLK</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">00</td><td>0</td><td colspan="2">00</td><td colspan="2">00</td><td>0</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>RW</td><td></td><td></td><td>RW</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>RW</td><td>RW</td><td>-</td><td>RW</td><td>RW</td><td>-</td><td>-</td><td>RW</td></tr>
</table>

20	T20CLK	Timer 20 Clock Selection.	
		0	XSOSC clock
		1	PCLK clock
17	T30CLK	Timer 30 Clock Selection.	
		0	MCLK clock
		1	PCLK clock
7 6	LCDCLK	LCD Driver Clock Selection.	
		00	A clock of the MCLK which is divided by divider 2 (Refer to figure 17)
		01	XSOSC clock
		10	WDTRC clock
		11	Reserved
4 3	WTCLK	Watch Timer Clock Selection.	
		00	A clock of the MCLK which is divided by divider 2 (Refer to figure 17)
		01	XSOSC clock
		10	WDTRC clock
		11	Reserved
		NOTE: These bits should be changed while the WTEN bit of watch timer control register (WT_CR) is '0'.	
0	WDTCLK	Watchdog Timer Clock Selection.	
		0	WDTRC clock
		1	PCLK clock

5.6.23 SCU_PPRST1: peripheral reset register 1

SCU_PPRST1/PPRST2 register can make a peripheral reset. If a specific bit in this register is set to '1', the peripheral corresponded with this bit occurs a reset event and the registers of the peripheral are initialized with reset values.

SCU_PPRST1 register is 32-bit size and accessible in 32/16/8-bit.

SCU_PPRST1=0x4000_1860

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										T21RST	T20RST	T30RST	T12RST	T11RST	T10RST	Reserved										PFRST	PERST	PDRST	PCRST	PBRST	PARST
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	RW	RW	RW	RW	RW	RW	-	-	-	-	-	-	-	-	-	-	RW	RW	RW	RW	RW	RW

21	T21RST	Timer 21 Reset bit	
		0	No effect
		1	Reset Timer 21, Cleared by software
20	T20RST	Timer 20 Reset bit	
		0	No effect
		1	Reset Timer 20, Cleared by software
19	T30RST	Timer 30 Reset bit	
		0	No effect
		1	Reset Timer 30, Cleared by software
18	T12RST	Timer 12 Reset bit	
		0	No effect
		1	Reset Timer 12, Cleared by software
17	T11RST	Timer 11 Reset bit	
		0	No effect
		1	Reset Timer 11, Cleared by software
16	T10RST	Timer 10 Reset bit	
		0	No effect
		1	Reset Timer 10, Cleared by software
5	PFRST	Port F Reset bit	
		0	No effect
		1	Reset Port F, Cleared by software
4	PERST	Port E Reset bit	
		0	No effect
		1	Reset Port E, Cleared by software
3	PDRST	Port D Reset bit	
		0	No effect
		1	Reset Port D, Cleared by software
2	PCRST	Port C Reset bit	
		0	No effect
		1	Reset Port C, Cleared by software
1	PBRST	Port B Reset bit	
		0	No effect
		1	Reset Port B, Cleared by software
0	PARST	Port A Reset bit	
		0	No effect
		1	Reset Port A, Cleared by software

5.6.24 SCU_PPRST2: peripheral reset register 2

SCU_PPRST2 register is 32-bit size and accessible in 32/16/8-bit.

SCU_PPRST2=0x4000_1864

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												FMCRST	LVIRST	Reserved	WTRST	Reserved		LCDRST	CRRST	Reserved	ADRST	Reserved		I2C1RST	I2C0RST	Reserved		UT1RST	UT0RST	UST11RST	UST10RST
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-	-	RW	RW	-	RW	-	-	RW	RW	-	RW	-	-	RW	RW	-	-	RW	RW	RW	RW

19	FMCRST	FMCRST Reset bit	
		0	No effect
		1	Reset flash memory control, Cleared by software, Ignored during flash operation
18	LVIRST	LVI (Low Voltage Indicator) Reset bit	
		0	No effect
		1	Reset LVI, Cleared by software
16	WTRST	WT (Watch Timer) Reset bit	
		0	No effect
		1	Reset WT, Cleared by software
13	LCDRST	LCD Controller Reset bit	
		0	No effect
		1	Reset LCD Controller, Cleared by software
12	CRRST	CRC (Cyclic Redundancy Check) Reset bit	
		0	No effect
		1	Reset CRC, Cleared by software
10	ADRST	ADC (Analog to Digital Converter) Reset bit	
		0	No effect
		1	Reset ADC, Cleared by software
7	I2C1RST	I2C1 (Inter-integrated Circuit) Reset bit	
		0	No effect
		1	Reset I2C1, Cleared by software
6	I2C0RST	I2C0 (Inter-integrated Circuit) Reset bit	
		0	No effect
		1	Reset I2C0, Cleared by software
3	UT1RST	UART1 Reset bit	
		0	No effect
		1	Reset UART1 , Cleared by software
2	UT0RST	UART0 Reset bit	
		0	No effect
		1	Reset UART0 , Cleared by software
1	UST11RST	USART11 Reset bit	
		0	No effect
		1	Reset USART11 , Cleared by software
0	UST10RST	USART10 Reset bit	
		0	No effect
		1	Reset USART10 , Cleared by software

5.6.25 SCU_XTFLSR: X-tal filter selection register

SCU_XTFLSR register is used to improve noise immunity of the main x-tal. This register should be set to a proper value for corresponding x-tal frequency.

SCU_XTFLSR register is 32-bit size and accessible in 32/16/8-bit.

SCU_XTFLSR=0x4000_1880

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WTIDKY	**Reserved**													**XRNS**		
0x0000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**
WO	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**RW**	**RW**	**RW**

31 16	WTIDKY	Write Identification Key	
		When writing, write 0x9B37 to these bits, or else writing is ignored	
2 0	XRNS	External Main Oscillator Filter Selection.	
		000	x-tal ≤ 4.5MHz
		001	4.5MHz < x-tal ≤ 6.5MHz
		010	6.5MHz < x-tal ≤ 8.5MHz
		011	8.5MHz < x-tal ≤ 10.5MHz
		100	10.5MHz < x-tal ≤ 12.5MHz
		101	12.5MHz < x-tal ≤ 16.5MHz
		Others	Reserved

NOTE: The External Main Oscillator range (XRNS) should be changed when the IRC is selected as the system clock.

5.6.26 SCU_LVICR: low voltage indicator control register

SCU_LVICR register is 32-bit size and accessible in 32/16/8-bit.

SCU_LVICR=0x4000_5100

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7	6	5	4	3 2 1 0
Reserved	**LVIEN**	**Reserved**	**LVINTEN**	**LVIFLAG**	**LVIVS**
0x000000	**0**	**0**	**0**	**0**	**0000**
-	**RW**	**-**	**RW**	**RW**	**RW**

7	LVIEN	LVI Enable.	
		0	Disable low voltage indicator.
		1	Enable low voltage indicator.
5	LVINTEN	LVI Interrupt Enable.	
		0	Disable low voltage indicator interrupt.
		1	Enable low voltage indicator interrupt.
4	LVIFLAG	LVI Interrupt Flag.	
		0	No request occurred.
		1	Request occurred. The bit is cleared to '0' when '1' is written.
3 0	LVIVS	LVI Voltage Selection.	
		0011	Do not write.
		0100	2.00V
		0101	2.13V
		0110	2.28V
		0111	2.46V
		1000	2.67V
		1001	3.04V
		1010	3.20V
		1011	3.55V
		1100	3.75V
		1101	3.99V
		1110	4.25V
		1111	4.55V
		Others	Not available.

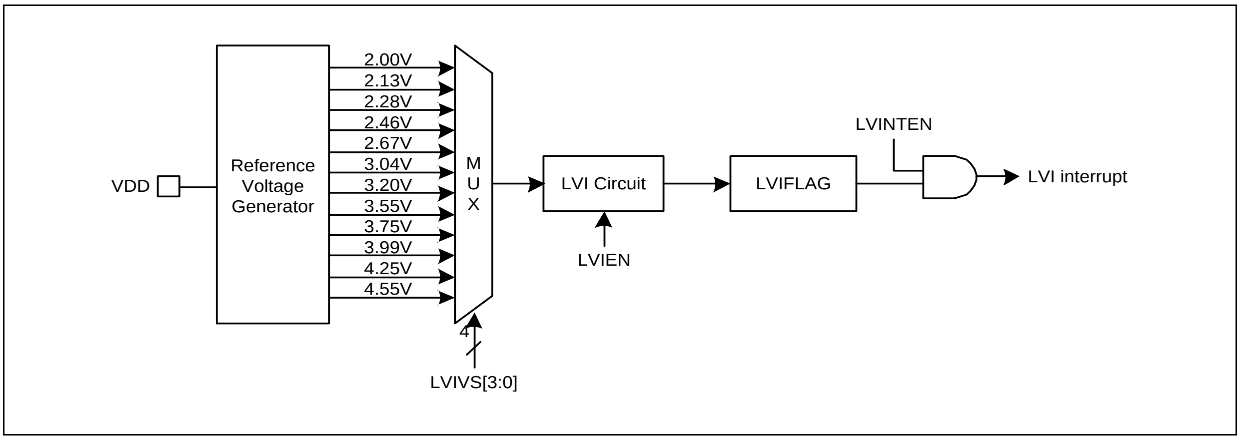


Figure 26. LVI Block Diagram

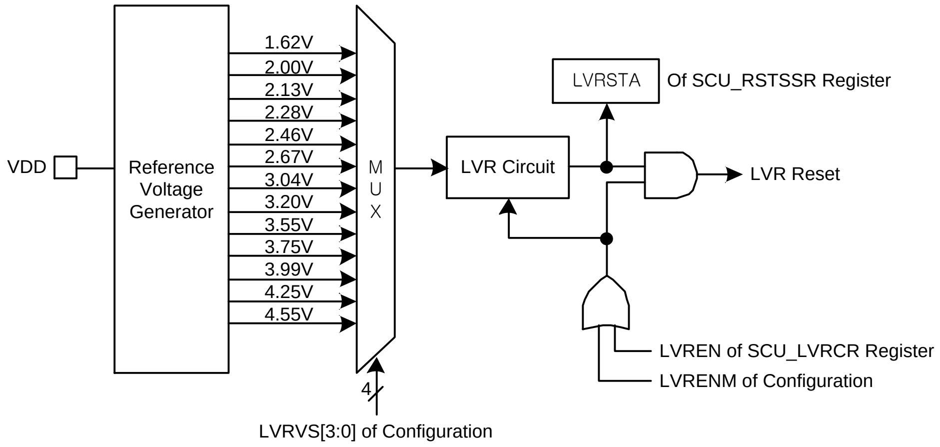
5.6.27 SCU_LVRCR: low voltage reset control register

SCU_LVRCR register is 32-bit size and accessible in 32/16/8-bit.

SCU_LVRCR=0x4000_5104

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved	**LVREN**
0x000000	**0x00**
–	**RW**

7 0	LVREN	LVR Enable. These bits are cleared to 0x00 by POR only and retained by other reset signals.	
		0x55	Disable low voltage reset.
		Others	Enable low voltage reset.



NOTE: Voltage level of LVR is set by the low voltage reset configuration register (CONF_LVRCNFIG) in the configure option page 1.

Figure 27. LVR Block Diagram

6 PCU and GPIO

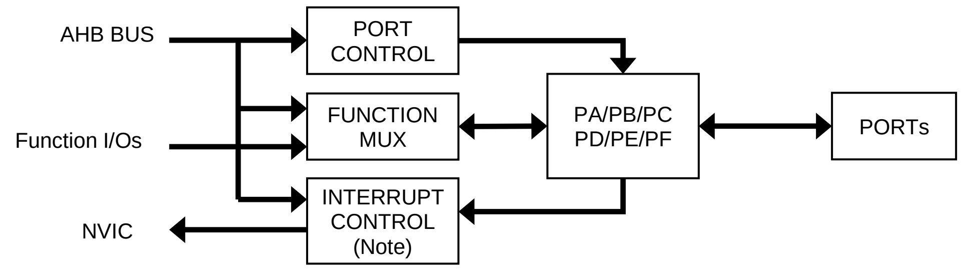
PCU (Port Control Unit) configures and controls external I/Os as shown below:

- It configures the direction of external signals of each pin.
- It sets Interrupt trigger mode for each pin.
- It manages internal pull-up and pull-down register control and open drain control.

Most pins, except for dedicated function pins, can be used as GPIO (General Purpose I/O) ports. The GPIO block controls the GPIO as shown below:

- It selects output signal level (H/L).
- It controls external interrupt interface.
- It enables or disables the pull-ups and the pull-downs.

6.1 PCU and GPIO block diagrams



NOTE: Refer to the Chapter 3.2 Interrupt controller.

Figure 28. PCU Block Diagram

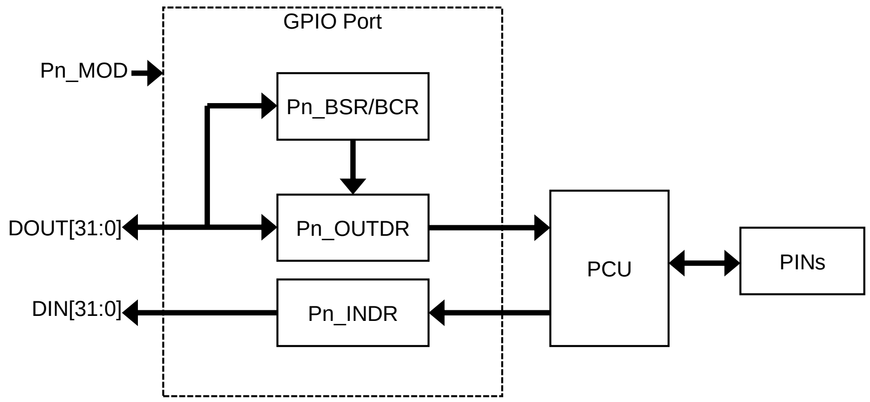


Figure 29. GPIO Block Diagram

6.2 I/O port block diagram

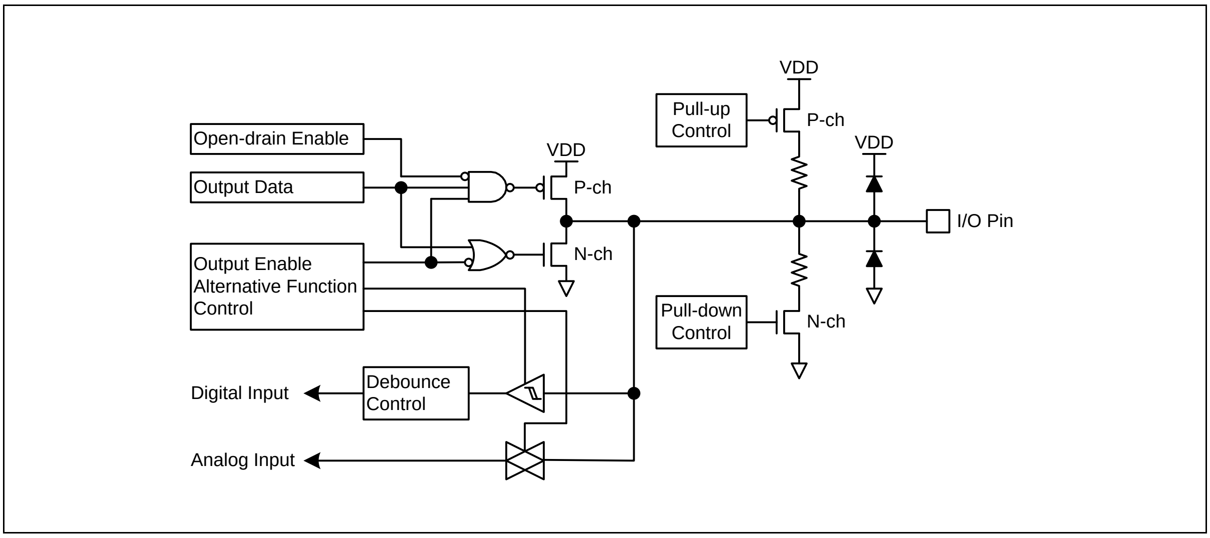


Figure 30. I/O Port Block Diagram (External Interrupt I/O pins)

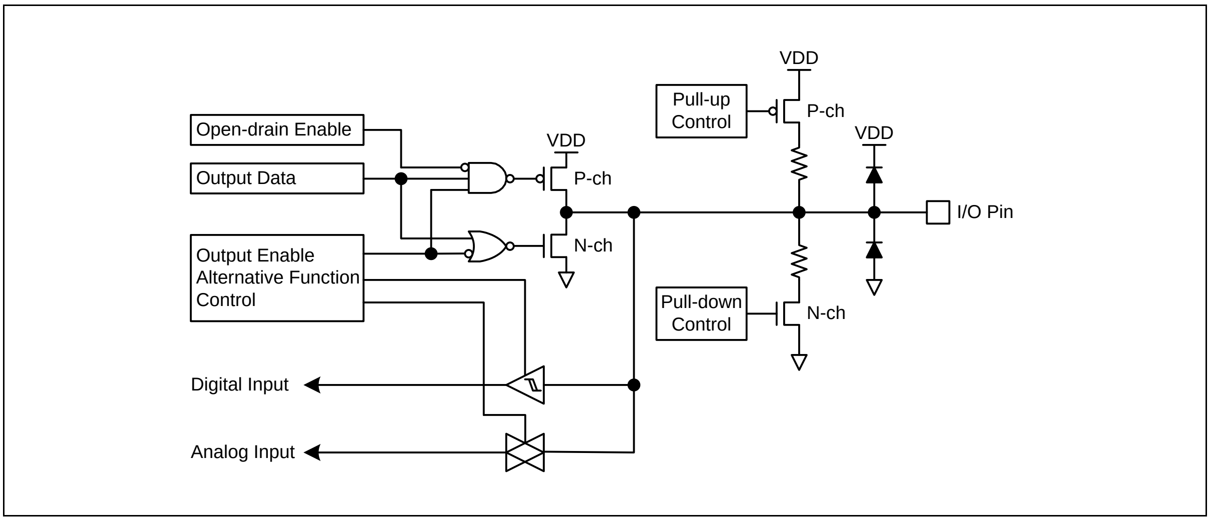


Figure 31. I/O Port Block Diagram (General I/O pins)

6.3 Pin multiplexing

GPIO pins support alternative functions. Table 21 shows pin multiplexing information.

Table 21. GPIO Alternative Functions

PORT	**PIN**	**FUNCTION**				
		AF0	**AF1**	**AF2**	**AF3**	**AF4**
PA	0	–	SDA1	–	AN0	–
	1	–	SCL1	–	AN1	–
	2	–	EC12	–	AN2	–
	3	–	–	–	AN3	–
	4	–	–	–	AN4	–
	5	–	T12OUT	T12CAP	AN5	–
	6	SEG27	–	–	AN6	–
	7	SEG26	–	–	AN7	AVREF
PB	0	SEG25	TXD10	MOSI10	AN8	–
	1	SEG24	RXD10	MISO10	AN9	–
	2	SEG23	–	SCK10	AN10	–
	3	SEG22	BOOT	SS10	–	–
	4	SEG21	TXD0	SWCLK	–	–
	5	SEG20	RXD0	SWDIO	–	–
	6	SEG19	TXD1	–	–	–
	7	SEG18	RXD1	–	–	–
PC	0	SEG17	T20OUT	T20CAP	–	–
	1	SEG16	T21OUT	T21CAP	–	–
	2	SEG15	EC20	–	–	–
	3	SEG14	EC21	–	–	–
	4	SEG13	–	–	–	–
PD	0	SEG12	SCL0	–	–	–
	1	SEG11	SDA0	–	–	–
	2	SEG10	TXD11	MOSI11	–	–
	3	SEG9	RXD11	MISO11	–	–
	4	SEG8	–	SCK11	–	–
	5	SEG7	–	SS11	–	–
	6	SEG6	EC11	–	–	–
	7	SEG5	EC10	–	–	–

Table 21. GPIO Alternative Functions (continued)

PORT	PIN	FUNCTION				
		AF0	AF1	AF2	AF3	AF4
PE	0	COM0	PWM30AA	–	–	–
	1	COM1	PWM30AB	–	–	–
	2	COM2	PWM30BA	–	–	–
	3	COM3/SEG0	PWM30BB	–	–	–
	4	COM4/SEG1	PWM30CA	–	–	–
	5	COM5/SEG2	PWM30CB	–	–	–
	6	COM6/SEG3	T10OUT	T10CAP	–	–
	7	COM7/SEG4	T11OUT	T11CAP	–	–
PF	0	XOUT	(SCL1)	–	–	–
	1	XIN	(SDA1)	–	–	–
	2	SXIN	–	–	–	–
	3	SXOUT	–	–	–	–
	4	CLKO	–	–	–	–
	5	–	BLNK	–	–	–
	6	–	EC30	–	–	–
	7	–	–	T30CAP	–	–

NOTES:

1. An unused pin shouldn't be configured as an input floating.
2. After reset, the PB3 pin is configured as BOOT alternative function and the internal pull-up is activated.
3. After reset, the PB4 and PB5 pins are configured as SWCLK and SWDIO alternative functions, and the internal pull-down on SWCLK and the internal pull-up on SWDIO are activated.
4. The PE3 – PE7 are automatically configured as common or segment signal according to the duty of the LCD control register when the pins are selected as alternative functions for common/segment.
5. The SWCLK and SWDIO pins shouldn't be changed as other alternative functions by software during the pins are connected with debugger host.

6.4 Registers

Base address and register map of PCU and GPIO block are shown in Table 22 and Table 23.

Table 22. Base Address of Port

Port name	Address range	Size (bytes)	Description
PA	0x3000 0000 – 0x3000 00FF	256	General Purpose I/O Port A
PB	0x3000 0100 – 0x3000 01FF	256	General Purpose I/O Port B
PC	0x3000 0200 – 0x3000 02FF	256	General Purpose I/O Port C
PD	0x3000 0300 – 0x3000 03FF	256	General Purpose I/O Port D
PE	0x3000 0400 – 0x3000 04FF	256	General Purpose I/O Port E
PF	0x3000 0500 – 0x3000 05FF	256	General Purpose I/O Port F

Table 23. PCU and GPIO Register Map

Name	Offset	Type	Description	Reset Value
Pn_MOD	0x0000	RW	Port n mode register	0x00000000
Pn_TYP	0x0004	RW	Port n output type selection register	0x00000000
Pn_AFSR1	0x0008	RW	Port n alternative function selection register 1	0x00000000
Pn_AFSR2	0x000C	RW	Port n alternative function selection register 2	0x00000000
Pn_PUPD	0x0010	RW	Port n pull-up/down resistor selection register	0x00000000
Pn_INDR	0x0014	RO	Port n input data register	0x0000xxxx
Pn_OUTDR	0x0018	RW	Port n output data register	0x00000000
Pn_BSR	0x001C	WO	Port n output bit set register	0x00000000
Pn_BCR	0x0020	WO	Port n output bit clear register	0x00000000
Pn_OUTDMSK	0x0024	RW	Port n output data mask register	0x00000000
Pn_DBCR	0x0028	RW	Port n debounce control register	0x00000000

NOTES:

1. Where n=A, B, C, D, E, and F.
2. For exception, the reset value of PB_MOD, PB_AFSR1, PB_PUPD, PB_DBCR register is 0x0A80, 0x00221000, 0x0640, 0x0008 respectively.

6.4.1 Pn_MOD: port n mode register

Pn_MOD register selects one from input mode and output mode for each port pin. Each pin can be configured as an input pin, an output pin or an Alternative Function pin.

This register is 32-bit size and accessible in 32/16/8-bit. (n = A to F).

PA_MOD=0x3000_0000, PB_MOD=0x3000_0100, PC_MOD=0x3000_0200
PD_MOD=0x3000_0300, PE_MOD=0x3000_0400, PF_MOD=0x3000_0500

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
Reserved	**MODE7**	**MODE6**	**MODE5**	**MODE4**	**MODE3**	**MODE2**	**MODE1**	**MODE0**
0x0000	**00**	**00**	**00**	**00**	**00**	**00**	**00**	**00**
–	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**

2x+1 2x	MODEx	Port n Mode Selection bits, x: 0 to 7	
		00	Input mode
		01	Output mode
		10	Alternative function mode
		11	Reserved

NOTES:

1. The MODEx bits for PF0 – PF3 won't be changed while the corresponding clock (XMOSC/XSOSC) is working as the system clock (MCLK).
2. For exception, 0x0A80 is the reset value of PB_MOD register for alternative function of SWDIO, SWCLK, and BOOT pins.

6.4.2 Pn_TYP: port n output type selection register

Pn_TYP register selects an output type of a port pin from Push-pull output and Open-drain output.

This register is 32-bit size and accessible in 32/16/8-bit. (n = A to F)

PA_TYP=0x3000_0004, PB_TYP=0x3000_0104, PC_TYP=0x3000_0204
PD_TYP=0x3000_0304, PE_TYP=0x3000_0404, PF_TYP=0x3000_0504

31–8	7	6	5	4	3	2	1	0
Reserved	**TYP7**	**TYP6**	**TYP5**	**TYP4**	**TYP3**	**TYP2**	**TYP1**	**TYP0**
0x000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
–	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**

x	TYPx	Port n Output Type Selection bit, x: 0 to 7	
		0	Push-pull output
		1	Open-drain output

6.4.3 PA_AFSR1: port A alternative function selection register 1

PA_AFSR1 register must be set properly before using the port. Otherwise, the port may not function properly.

This register is 32-bit size and accessible in 32/16/8-bit.

PA_AFSR1=0x3000_0008

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
AFSR7	**AFSR6**	**AFSR5**	**AFSR4**	**AFSR3**	**AFSR2**	**AFSR1**	**AFSR0**
0000	**0000**	**0000**	**0000**	**0000**	**0000**	**0000**	**0000**
RW	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**

4x+3 4x	AFSRx	Port A Alternative Function Selection bits, x: 0 to 7	
		0000	Alternative Function 0 (AF0)
		0001	Alternative Function 1 (AF1)
		0010	Alternative Function 2 (AF2)
		0011	Alternative Function 3 (AF3)
		0100	Alternative Function 4 (AF4)
		Others	Reserved

Table 24. Functions of PA Port

PORT	PIN	FUNCTION				
		AF0	AF1	AF2	AF3	AF4
PA	0	–	SDA1	–	AN0	–
	1	–	SCL1	–	AN1	–
	2	–	EC12	–	AN2	–
	3	–	–	–	AN3	–
	4	–	–	–	AN4	–
	5	–	T12OUT	T12CAP	AN5	–
	6	SEG27	–	–	AN6	–
	7	SEG26	–	–	AN7	AVREF

6.4.4 PB_AFSR1: port B alternative function selection register 1

PB_AFSR1 register must be set properly before using the port. Otherwise, the port may not function properly.

This register is 32-bit size and accessible in 32/16/8-bit.

PB_AFSR1=0x3000_0108

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
AFSR7	AFSR6	AFSR5	AFSR4	AFSR3	AFSR2	AFSR1	AFSR0
0000	0000	0010	0010	0001	0000	0000	0000
RW	RW	RW	RW	RW	RW	RW	RW

4x+3 4x	AFSRx	Port B Alternative Function Selection bits, x: 0 to 7	
		0000	Alternative Function 0 (AF0)
		0001	Alternative Function 1 (AF1)
		0010	Alternative Function 2 (AF2)
		0011	Alternative Function 3 (AF3)
		0100	Alternative Function 4 (AF4)
		Others	Reserved

NOTE: The PB3, PB4, and PB5 pins are configured as BOOT, SWCLK, and SWDIO alternative functions after reset.

Table 25. Functions of PB Port

PORT	PIN	FUNCTION				
		AF0	AF1	AF2	AF3	AF4
PB	0	SEG25	TXD10	MOSI10	AN8	–
	1	SEG24	RXD10	MISO10	AN9	–
	2	SEG23	–	SCK10	AN10	–
	3	SEG22	BOOT	SS10	–	–
	4	SEG21	TXD0	SWCLK	–	–
	5	SEG20	RXD0	SWDIO	–	–
	6	SEG19	TXD1	–	–	–
	7	SEG18	RXD1	–	–	–

6.4.5 PC_AFSR1: port C alternative function selection register 1

PC_AFSR1 register must be set properly before using the port. Otherwise, the port may not function properly.

This register is 32-bit size and accessible in 32/16/8-bit.

PC_AFSR1=0x3000_0208

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
AFSR7	AFSR6	AFSR5	AFSR4	AFSR3	AFSR2	AFSR1	AFSR0
0000	0000	0000	0000	0000	0000	0000	0000
RW	RW	RW	RW	RW	RW	RW	RW

4x+3 4x	AFSRx	Port C Alternative Function Selection bits, x: 0 to 7	
		0000	Alternative Function 0 (AF0)
		0001	Alternative Function 1 (AF1)
		0010	Alternative Function 2 (AF2)
		0011	Alternative Function 3 (AF3)
		0100	Alternative Function 4 (AF4)
		Others	Reserved

Table 26. Functions of PC Port

PORT	PIN	FUNCTION				
		AF0	AF1	AF2	AF3	AF4
PC	0	SEG17	T20OUT	T20CAP	–	–
	1	SEG16	T21OUT	T21CAP	–	–
	2	SEG15	EC20	–	–	–
	3	SEG14	EC21	–	–	–
	4	SEG13	–	–	–	–

6.4.6 PD_AFSR1: port D alternative function selection register 1

PD_AFSR1 register must be set properly before using the port. Otherwise, the port may not function properly.

This register is 32-bit size and accessible in 32/16/8-bit.

PD_AFSR1=0x3000_0308

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
AFSR7	**AFSR6**	**AFSR5**	**AFSR4**	**AFSR3**	**AFSR2**	**AFSR1**	**AFSR0**
0000	**0000**	**0000**	**0000**	**0000**	**0000**	**0000**	**0000**
RW	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**

4x+3 4x	AFSRx	Port D Alternative Function Selection bits, x: 0 to 7	
		0000	Alternative Function 0 (AF0)
		0001	Alternative Function 1 (AF1)
		0010	Alternative Function 2 (AF2)
		0011	Alternative Function 3 (AF3)
		0100	Alternative Function 4 (AF4)
		Others	Reserved

Table 27. Functions of PD Port

PORT	PIN	FUNCTION				
		AF0	AF1	AF2	AF3	AF4
PD	0	SEG12	SCL0	–	–	–
	1	SEG11	SDA0	–	–	–
	2	SEG10	TXD11	MOSI11	–	–
	3	SEG9	RXD11	MISO11	–	–
	4	SEG8	–	SCK11	–	–
	5	SEG7	–	SS11	–	–
	6	SEG6	EC11	–	–	–
	7	SEG5	EC10	–	–	–

6.4.7 PE_AFSR1: port E alternative function selection register 1

PE_AFSR1 register must be set properly before using the port. Otherwise, the port may not function properly.

This register is 32-bit size and accessible in 32/16/8-bit.

PE_AFSR1=0x3000_0408

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
AFSR7	**AFSR6**	**AFSR5**	**AFSR4**	**AFSR3**	**AFSR2**	**AFSR1**	**AFSR0**
0000	**0000**	**0000**	**0000**	**0000**	**0000**	**0000**	**0000**
RW	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**

4x+3 4x	AFSRx	Port E Alternative Function Selection bits, x: 0 to 7	
		0000	Alternative Function 0 (AF0)
		0001	Alternative Function 1 (AF1)
		0010	Alternative Function 2 (AF2)
		0011	Alternative Function 3 (AF3)
		0100	Alternative Function 4 (AF4)
		Others	Reserved

Table 28. Functions of PE Port

PORT	PIN	FUNCTION				
		AF0	AF1	AF2	AF3	AF4
PE	0	COM0	PWM30AA	–	–	–
	1	COM1	PWM30AB	–	–	–
	2	COM2	PWM30BA	–	–	–
	3	COM3/SEG0	PWM30BB	–	–	–
	4	COM4/SEG1	PWM30CA	–	–	–
	5	COM5/SEG2	PWM30CB	–	–	–
	6	COM6/SEG3	T10OUT	T10CAP	–	–
	7	COM7/SEG4	T11OUT	T11CAP	–	–

6.4.8 PF_AFSR1: port F alternative function selection register 1

PF_AFSR1 register must be set properly before using the port. Otherwise, the port may not function properly.

This register is 32-bit size and accessible in 32/16/8-bit.

PF_AFSR1=0x3000_0508

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
AFSR7	**AFSR6**	**AFSR5**	**AFSR4**	**AFSR3**	**AFSR2**	**AFSR1**	**AFSR0**
0000	**0000**	**0000**	**0000**	**0000**	**0000**	**0000**	**0000**
RW	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**

4x+3 4x	AFSRx	Port F Alternative Function Selection bits, x: 0 to 7	
		0000	Alternative Function 0 (AF0)
		0001	Alternative Function 1 (AF1)
		0010	Alternative Function 2 (AF2)
		0011	Alternative Function 3 (AF3)
		0100	Alternative Function 4 (AF4)
		Others	Reserved

NOTE: The AFSRx bits for PF0 – PF3 cannot be changed when the corresponding clock (XMOSC/XSOSC) is selected as the system clock (MCLK).

Table 29. Functions of PF Port

PORT	PIN	FUNCTION				
		AF0	AF1	AF2	AF3	AF4
PF	0	XOUT	(SCL1)	–	–	–
	1	XIN	(SDA1)	–	–	–
	2	SXIN	–	–	–	–
	3	SXOUT	–	–	–	–
	4	CLKO	–	–	–	–
	5	–	BLNK	–	–	–
	6	–	EC30	–	–	–
	7	–	–	T30CAP	–	–

6.4.9 Pn_PUPD: port n Pull-up/down resistor selection register

Every pin of the port has an on-chip pull-up/down resistor, which can be configured by Pn_PUPD registers.

This register is 32-bit size and accessible in 32/16/8-bit. (n = A to F).

PA_PUPD=0x3000_0010, PB_PUPD=0x3000_0110, PC_PUPD=0x3000_0210
PD_PUPD=0x3000_0310, PE_PUPD=0x3000_0410, PF_PUPD=0x3000_0510

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
Reserved	**PUPD7**	**PUPD6**	**PUPD5**	**PUPD4**	**PUPD3**	**PUPD2**	**PUPD1**	**PUPD0**
0x0000	**00**	**00**	**00**	**00**	**00**	**00**	**00**	**00**
–	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**

2x+1 2x	PUPDx	Port n Pull-up/down Resistor Selection bits, x: 0 to 7	
		00	Disable pull-up/down resistor
		01	Enable pull-up resistor
		10	Enable pull-down resistor
		11	Reserved

NOTES:

1. The pull-up/down resistor of PF0 – PF3 are automatically disabled regardless of the corresponding PUPDx value if the pins are configured as alternative function pins for x-tal (XIN, XOUT, SXIN, and SXOUT).
2. For exception, 0x0000_0640 is the reset value of PB_PUPD register for pull-up resistor of SWDIO/BOOT and pull-down resistor of SWCLK.

6.4.10 Pn_INDR: port n input data register

Each pin level status can be read in the Pn_INDR register. Except for analog input and alternative mode output, the pin level can be detected in the Pn_INDR register.

This register is 32-bit size and accessible in 32/16/8-bit. (n = A to F).

PA_INDR=0x3000_0014, PB_INDR=0x3000_0114, PC_INDR=0x3000_0214
PD_INDR=0x3000_0314, PE_INDR=0x3000_0414, PF_INDR=0x3000_0514

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Reserved	**INDR7**	**INDR6**	**INDR5**	**INDR4**	**INDR3**	**INDR2**	**INDR1**	**INDR0**
0x000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
–	**RO**	**RO**	**RO**	**RO**	**RO**	**RO**	**RO**	**RO**

x	INDRx	Port n Input Data bit, x: 0 to 7

6.4.11 Pn_OUTDR: port n output data register

When a pin is set as an output in GPIO mode, output level of the pin is defined by Pn_OUTDR registers.

This register is 32-bit size and accessible in 32/16/8-bit. (n = A to F).

PA_OUTDR=0x3000_0018, PB_OUTDR=0x3000_0118, PC_OUTDR=0x3000_0218
PD_OUTDR=0x3000_0318, PE_OUTDR=0x3000_0418, PF_OUTDR=0x3000_0518

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="24">Reserved</td><td>OUTDR7</td><td>OUTDR6</td><td>OUTDR5</td><td>OUTDR4</td><td>OUTDR3</td><td>OUTDR2</td><td>OUTDR1</td><td>OUTDR0</td></tr>
<tr><td colspan="24">0x000000</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="24">-</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td></tr>
</table>

x	OUTDRx	Port n Output Data bit, x: 0 to 7. The OUTDR bits can be individually set/cleared by writing to the Pn_BSR/Pn_BCR register.

6.4.12 Pn_BSR: port n output bit set register

Pn_BSR are used for controlling each bit of the Pn_OUTDR register. Writing a ‘1’ into the specific bit position will set a corresponding bit of Pn_OUTDR to ‘1’. Writing ‘0’ in the register has no effect.

This register is 32-bit size and accessible in 32/16/8-bit. (n = A to F)

PA_BSR=0x3000_001C, PB_BSR=0x3000_011C, PC_BSR=0x3000_021C
PD_BSR=0x3000_031C, PE_BSR=0x3000_041C, PF_BSR=0x3000_051C

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="24">Reserved</td><td>BSR7</td><td>BSR6</td><td>BSR5</td><td>BSR4</td><td>BSR3</td><td>BSR2</td><td>BSR1</td><td>BSR0</td></tr>
<tr><td colspan="24">0x000000</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="24">-</td><td>WO</td><td>WO</td><td>WO</td><td>WO</td><td>WO</td><td>WO</td><td>WO</td><td>WO</td></tr>
</table>

x	BSRx	Port n Output Set bit, x: 0 to 7. These bits are always read to 0x00.	
		0	No effect
		1	Set the corresponding OUTDRx bit (Automatically cleared to 0)

6.4.13 Pn_BCR: port n output bit clear register

Pn_BCR are used for controlling each bit of Pn_OUTDR register. Writing a ‘1’ into the specific bit will set a corresponding bit of Pn_OUTDR to ‘0’. Writing ‘0’ in this register has no effect.

This register is 32-bit size and accessible in 32/16/8-bit. (n = A to F).

PA_BCR=0x3000_0020, PB_BCR=0x3000_0120, PC_BCR=0x3000_0220
PD_BCR=0x3000_0320, PE_BCR=0x3000_0420, PF_BCR=0x3000_0520

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Reserved	**BCR7**	**BCR6**	**BCR5**	**BCR4**	**BCR3**	**BCR2**	**BCR1**	**BCR0**
0x000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
-	**WO**	**WO**	**WO**	**WO**	**WO**	**WO**	**WO**	**WO**

x	BCRx	Port n Output Clear bit, x: 0 to 7. These bits are always read to 0x00.	
		0	No effect
		1	Clear the corresponding OUTDRx bit (Automatically cleared to 0)

6.4.14 Pn_OUTDMSK: port n output data mask register

Pn_OUTDMSK are used for protecting each bit of Pn_OUTDR register. Writing a ‘1’ into the specific bit will protect a corresponding bit of Pn_OUTDR. Writing ‘0’ in this register is unmask.

This register is 32-bit size and accessible in 32/16/8-bit. (n = A to F).

PA_OUTDMSK=0x3000_0024, PB_OUTDMSK=0x3000_0124, PC_OUTDMSK=0x3000_0224
PD_OUTDMSK=0x3000_0324, PE_OUTDMSK=0x3000_0424, PF_OUTDMSK=0x3000_0524

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Reserved	**OUTDMSK7**	**OUTDMSK6**	**OUTDMSK5**	**OUTDMSK4**	**OUTDMSK3**	**OUTDMSK2**	**OUTDMSK1**	**OUTDMSK0**
0x000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
-	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**

x	OUTDMSKx	Port n Output Data Mask bit, x: 0 to 7.	
		0	Unmask. The corresponding OUTDRx bit can be changed.
		1	Mask. The corresponding OUTDRx bit is protected.

6.4.15 Pn_DBCR: port n debounce control register

This register is 32-bit size and accessible in 32/16/8-bit. (n = A to E).

PA_DBCR=0x3000_0028, PB_DBCR=0x3000_0128, PC_DBCR=0x3000_0228
PD_DBCR=0x3000_0328, PE_DBCR=0x3000_0428, PF_DBCR=0x3000_0528

31 30 29 28 27 26 25 24	23 22 21 20 19	18 17 16	15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Reserved		**DBCLK**	**Reserved**	**DBEN7**	**DBEN6**	**DBEN5**	**DBEN4**	**DBEN3**	**DBEN2**	**DBEN1**	**DBEN0**
0x00	**00000**	**000**	**0x00**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
–	**–**	**RW**	**–**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**

18 16	DBCLK	Port n Debounce Filter Sampling Clock Selection bits	
		000	HCLK/1
		001	HCLK/4
		010	HCLK/16
		011	HCLK/64
		100	HCLK/256
		101	HCLK/1024
		110	Reserved
		111	Reserved
x	DBENx	Port n Debounce Enable bit, x: 0 to 7.	
		0	Disable debounce filter
		1	Enable debounce filter

NOTES:

1. If a level is not detected on an enabled pin three or more times in a row at the sampling clock, the signal is eliminated as noise.
2. The port debounce should be disabled before deep sleep mode.
3. The A31G11x series has debounce filters for only PB0 – PB7, PC0 – PC3, and PE0 – PE3.
4. The debounce of the BOOT Pin enables on system reset.
5. For exception, 0x08 is the reset value of PB_DBCR register.

6.5 Functional description

When input function of an I/O port is used by the Pin Control Register, output function of the I/O port is disabled.

Each port function is configured by the Alternative Function Selection Register respectively.

The Input Data Register captures current data on the I/O pin or debounced input data at every GPIO clock cycle.

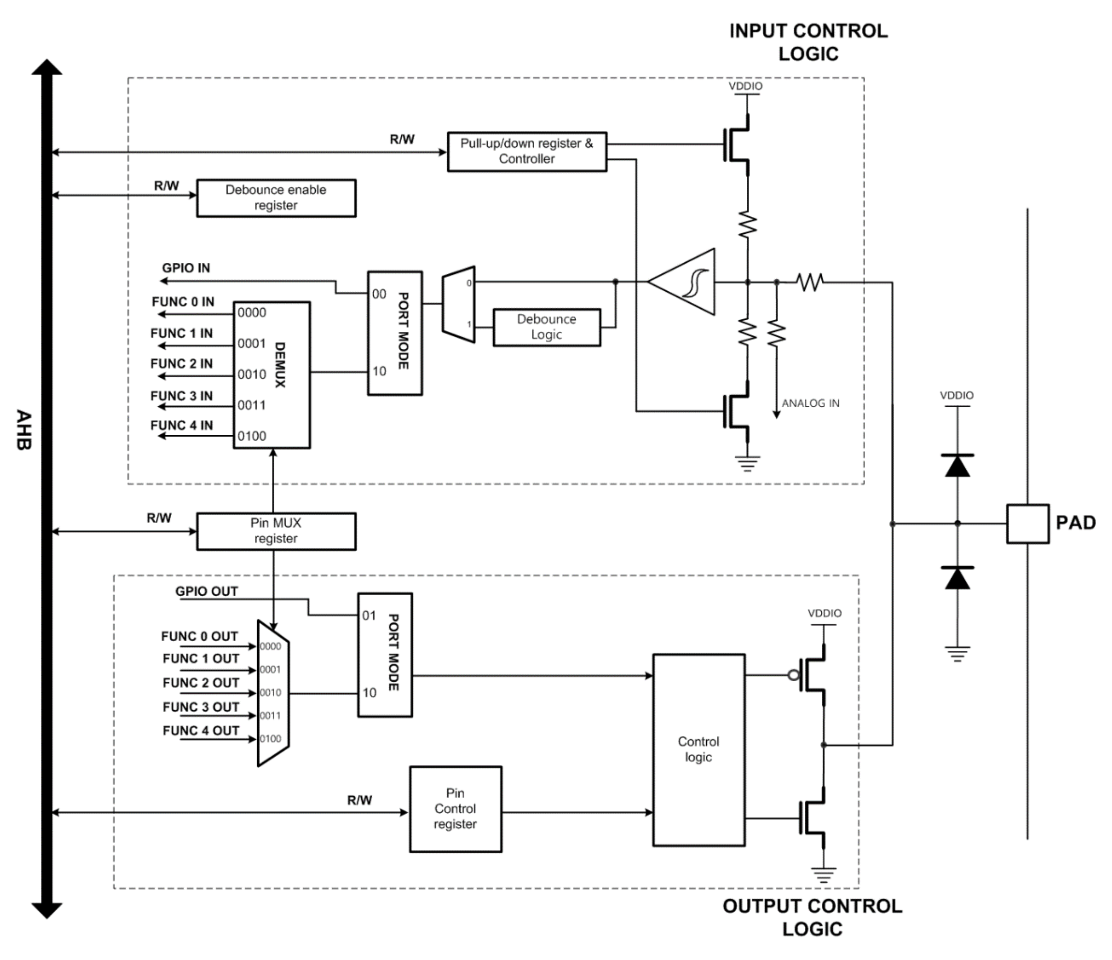


Figure 32. Port Structure Block Diagram

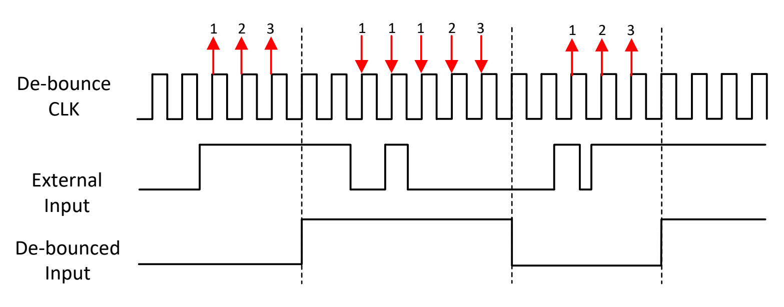


Figure 33. Debounce Function Timing Diagram

When an I/O port is configured as an output, the value written to the GPIO Output Data Register is output on the I/O Pin. When the Bit Set Register is set, the GPIO Output Data Register is set to High. When the Bit Clr Register is set, the GPIO Output Data Register is set to Low. The Input Data Register captures current data on the I/O pin or debounced input data at every GPIO clock cycle.

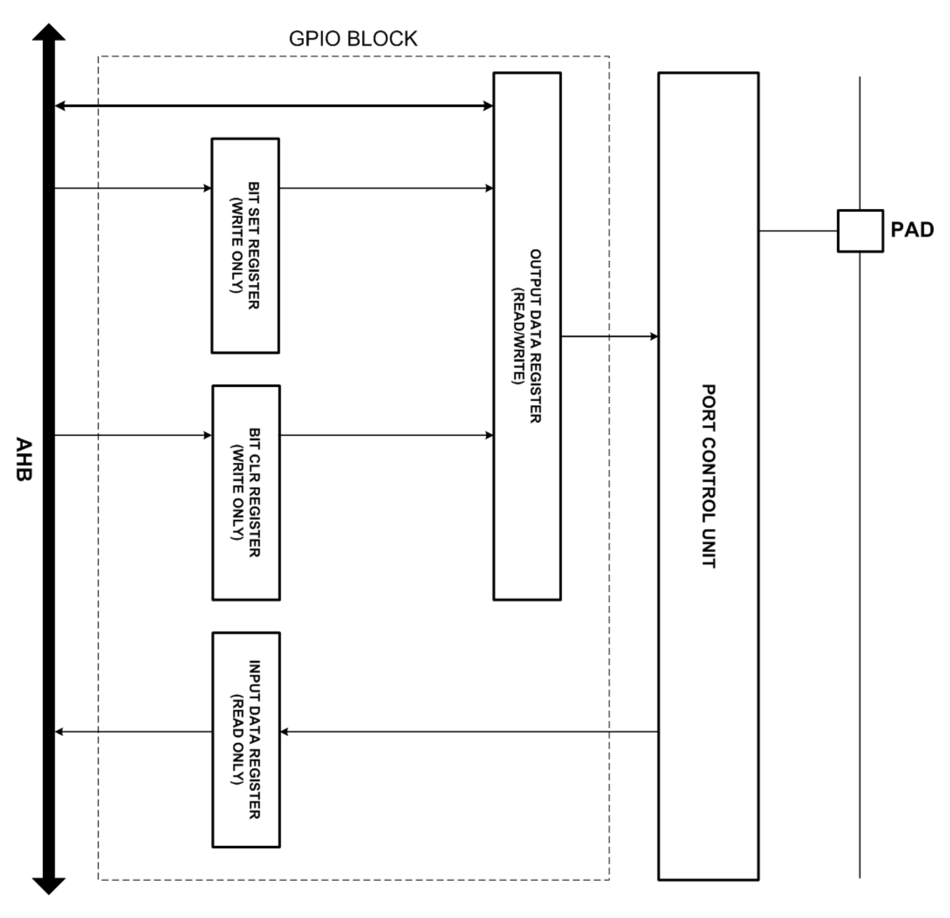


Figure 34. GPIO Block Diagram

7 WDT

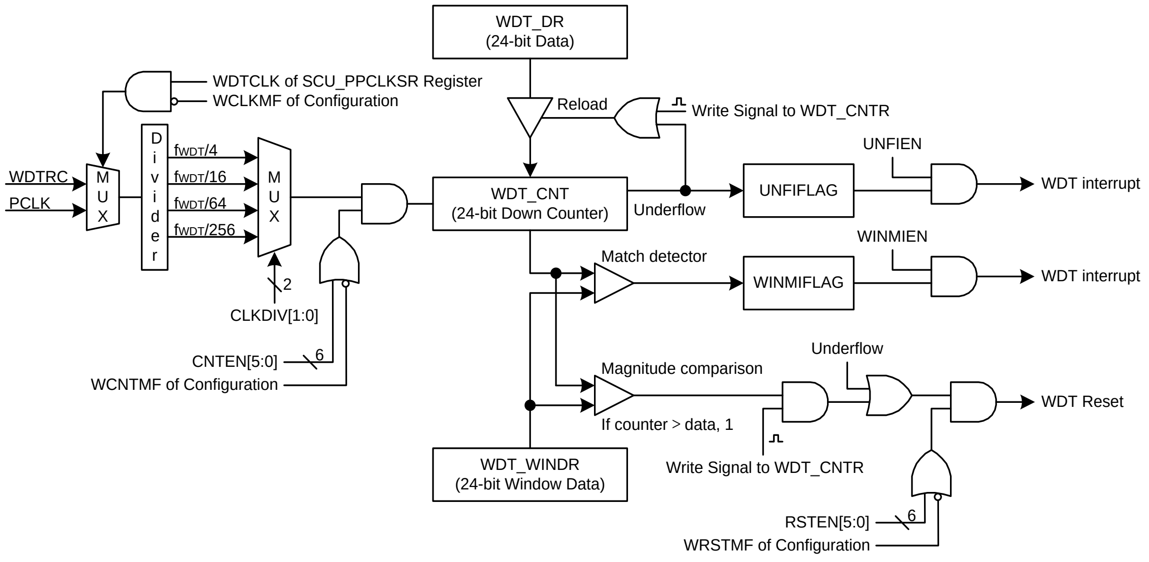
WDT (Watchdog Timer) rapidly detects CPU malfunctions such as endless loops caused by noise and returns the CPU to the normal state. WDT signal for malfunction detection can be used as either a CPU reset or an interrupt request.

When the WDT is not being used for malfunction detection, it can be used as a timer to generate interrupts at fixed intervals. When WDT_CNT value reaches WDT_WINDR value, a watchdog interrupt can be generated. The underflow time of the WDT can be set by WDT_DR. If an underflow occurs, an internal reset may be generated. The WDT operates at 40kHz which is the embedded RC oscillator's clock.

WDT operations are introduced below:

- 24-bit down counter (WDT_CNT)
- Reset or periodic interrupt selection
- Count clock selection
- Watchdog overflow output signal
- Counter window function

7.1 WDT block diagram



NOTES:

1. When a reload signal is generated, the WDT_DR value is reloaded to WDT_CNT register, after 1-clock delay, with the clock selected by the CLKDIV bits.
2. The watch-dog timer interrupt sources can't be used as a wake-up source in the deep sleep mode.

Figure 35. WDT Block Diagram

7.2 Registers

Base address and register map of WDT are shown in Table 30 and Table 31.

Table 30. Base Address of WDT

Name	Base address
WDT	0x4000_1A00

Table 31. WDT Register Map

Name	Offset	Type	Description	Reset Value
WDT_CR	0x0000	RW	Watchdog Timer Control Register	0x00000000
WDT_SR	0x0004	RW	Watchdog Timer Status Register	0x00000080
WDT_DR	0x0008	RW	Watchdog Timer Data Register	0x00000FFF
WDT_CNT	0x000C	RO	Watchdog Timer Counter Register	0x00000FFF
WDT_WINDR	0x0010	RW	Watchdog Timer Window Data Register	0x00001FFF
WDT_CNTR	0x0014	WO	Watchdog Timer Counter Reload Register	0x00000000

7.2.1 WDT_CR: watchdog timer control register

WDT module should be configured properly before running. The WDT module can reset the system or assert an interrupt signal to the system.

This register is 32-bit size.

WDT_CR=0x4000_1A00

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8 7 6 5 4	3	2	1 0
WTIDKY	**RSTEN**	**CNTEN**	**WINMIEN**	**UNFIEN**	**CLKDIV**
0x0000	**000000**	**000000**	**0**	**0**	**00**
WO	**RW**	**RW**	**RW**	**RW**	**RW**

31 16	WTIDKY	Write Identification Key.	
		When writing, write 0x5A69 to these bits, or else writing is ignored.	
15 10	RSTEN	Watchdog Timer Reset Enable.	
		0x25	Disable watchdog timer reset.
		Others	Enable watchdog timer reset.
9 4	CNTEN	Watchdog Timer Counter Enable.	
		0x1A	Disable watchdog timer counter.
		Others	Enable watchdog timer counter.
3	WINMIEN	Watchdog Timer Window Match Interrupt Enable.	
		0	Disable window data match interrupt.
		1	Enable window data match interrupt.
2	UNFIEN	Watchdog Timer Underflow Interrupt Enable.	
		0	Disable watchdog timer underflow interrupt.
		1	Enable watchdog timer underflow interrupt.
1 0	CLKDIV	Watchdog Timer Clock Divider. The watchdog timer clock is selected by SCU_PPCLKSR[0] bit of clock generation and CONF_WDTCNFIG[2] bit of configure option page 1.	
		00	fWDT/4
		01	fWDT/16
		10	fWDT/64
		11	fWDT/256

7.2.2 WDT_SR: watchdog timer status register

WDT_SR register is 32-bit size and accessible in 32/16/8-bit.

WDT_SR=0x4000_1A04

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7	6 5 4 3 2	1	0
Reserved	**DBGCNTEN**	**Reserved**	**WINMIFLAG**	**UNFIFLAG**
0x000000	**1**	**00000**	**0**	**0**
–	**RW**	**–**	**RW**	**RW**

7	DBGCNTEN	Watchdog Timer Counter Enable bit when the core is halted in debug mode.
		0 The watchdog timer counter continues operation even if the core is halted.
		1 The watchdog timer counter stops when the core is halted.
		NOTE: This bit is set to '1' by POR reset.
1	WINMIFLAG	Watchdog Timer Window Match Interrupt Flag.
		0 No request occurred.
		1 Request occurred. The bit is cleared to '0' when '1' is written.
0	UNFIFLAG	Watchdog Timer Underflow Interrupt Flag.
		0 No request occurred.
		1 Request occurred. The bit is cleared to '0' when '1' is written.

7.2.3 WDT_DR: watchdog timer data register

WDT_DR register is used to update WDT_CNT register.

This register is 32-bit size.

WDT_DR=0x4000_1A08

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Reserved	**DATA**
0x00	**0x000FFF**
–	**RW**

23 0	DATA	Watchdog Timer Data. The range is 0x000000 to 0xFFFFFF.

NOTE: Once any value is written to this data register, the register cannot be changed until system reset.

7.2.4 WDT_CNT: watchdog timer counter register

WDT_CNT register represents current count value of the 32-bit down counter. When the counter value reaches 0, an interrupt or a reset will be asserted.

This register is 32-bit size.

WDT_CNT=0x4000_1A0C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved	**CNT**		
0x00	**0x000FFF**		
–	**RO**		

23 0	CNT	Watchdog Timer Counter

7.2.5 WDT_WINDR: watchdog timer window data register

WDT_WINDR register is used to compare to WDT_CNT for WINDOW function.

This register is 32-bit size.

WDT_WINDR=0x4000_1A10

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved	**WDATA**		
0x00	**0x001FFF**		
-	**RW**		

23 0	WDATA	Watchdog Timer Window Data. The range is 0x000000 to 0xFFFFFF.

NOTE: Once any value is written to this window data register, the register cannot be changed until system reset.

7.2.6 WDT_CNTR: watchdog timer counter reload register

WDT_CNTR register is used to generate a reload signal. When a reload signal is generated, the WDT_DR value is reloaded to WDT_CNT.

This register is 32-bit size.

WDT_CNTR=0x4000_1A14

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved	**CNTR**
0x000000	**0x00**
-	**WO**

7 0	CNTR	Watchdog Timer Counter Reload bits.	
		0x6A	Reload the WDT_DR value to watchdog timer counter and re-start. (Automatically cleared to "0x00" after operation)
		Others	No effect

7.3 Functional description

Watchdog timer count can be enabled by CNTEN (WDT_CR[9:4]) set as any value other than 0x1A. As the WDT activates, the down counter will start counting from the load value. If the RSTEN (WDT_CR[15:10]) is set as any value other than 0x25, WDT reset would be asserted when the WDT counter value reaches 0 (underflow event) from WDT_DR value.

Before WDT counter reaches 0, software can write 0x6A to WDT_CNTR register in order to reload WDT counter when the counter value is less than or equal to the value of window data register. WDT reset may be asserted if the reload occurs when counter > window data.

7.3.1 Timing diagram

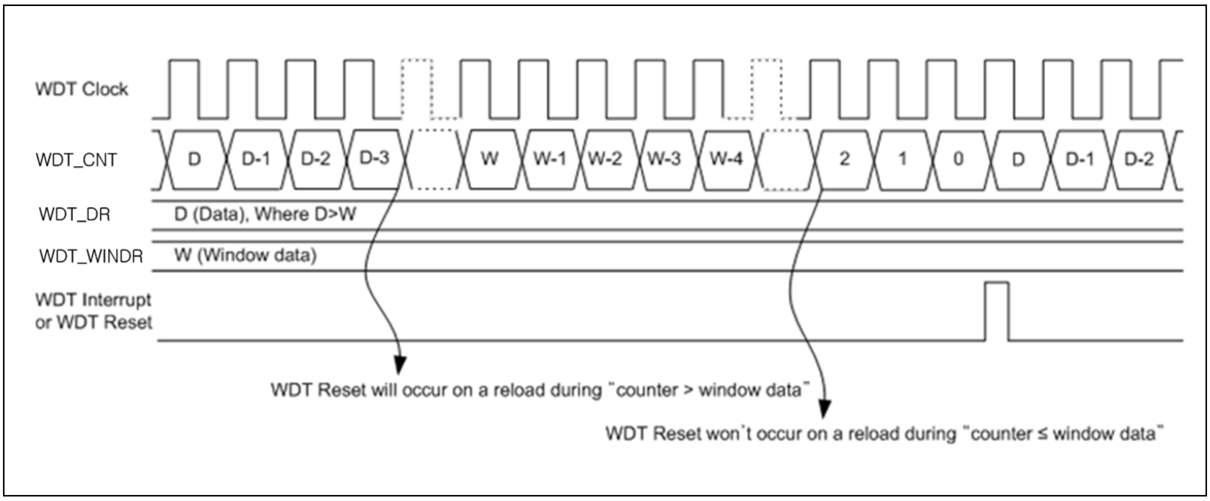


Figure 36. WDT Interrupt and WDT Reset Timing Diagram

7.3.2 Pre-scale table

The WDT includes a 24-bit down counter with programmable pre-scaler to define different time-out intervals.

Clock sources of the WDT can be WDTRC or PCLK. The PCLK can be selected by setting WDTCLK (SCU_PPCLKSR[0]) to '1'. Then CONF_WDTCNFIG[2] bit of configure option page 1 is cleared to logic '0'.

A WDT counter can be set as a base clock by controlling a 2-bit pre-scaler CLKDIV [1:0] in the WDT_CR register. The maximum pre-scaled value is "clock source frequency/256". The pre-scaled WDT counter clock frequency values are listed in Table 32.

Selectable clock source (40kHz ~ 40MHz) and time-out interval at a single count

Time-out period = (Load Value + 1) * (1/pre-scaled WDT counter clock frequency)

*Time out period (when the Load Value reaches 0, underflow flag is set to '1')

Table 32. Pre-scaled WDT Counter Clock Frequency

Clock source	WDTCLKIN	WDTCLKIN/4	WDTCLKIN/16	WDTCLKIN/64	WDTCLKIN/256
WDTRC	40kHz	10kHz	2.5kHz	0.625kHz	0.156kHz
PCLK	PCLK	PCLK/4	PCLK/16	PCLK/64	PCLK/256

8 WATCH TIMER

WT (WATCH TIMER) has a function for RTC (Real Time Clock) operation. It is generally used for RTC design. The internal structure of the watch timer consists of the clock source select circuit, timer counter circuit, output select circuit and watch timer control register. To operate the watch timer, determine the input clock source, output interval and set WTEN as '1' in watch timer control register (WT_CR). It is able to operate simultaneously or individually. To stop the WT, clear the WTEN bit in the WT_CR register. Even when the CPU is in STOP mode, sub clock stays alive and the WT can continue operation. The WT_CR can control WT clear and set Interval value at writing, and can read 12-bit WT counter value at reading. The WT features the followings:

- 14-bit Divider
- 12-bit up-counter
- RTC function

8.1 WT block diagram

Figure 37 shows a block diagram of the WT block.

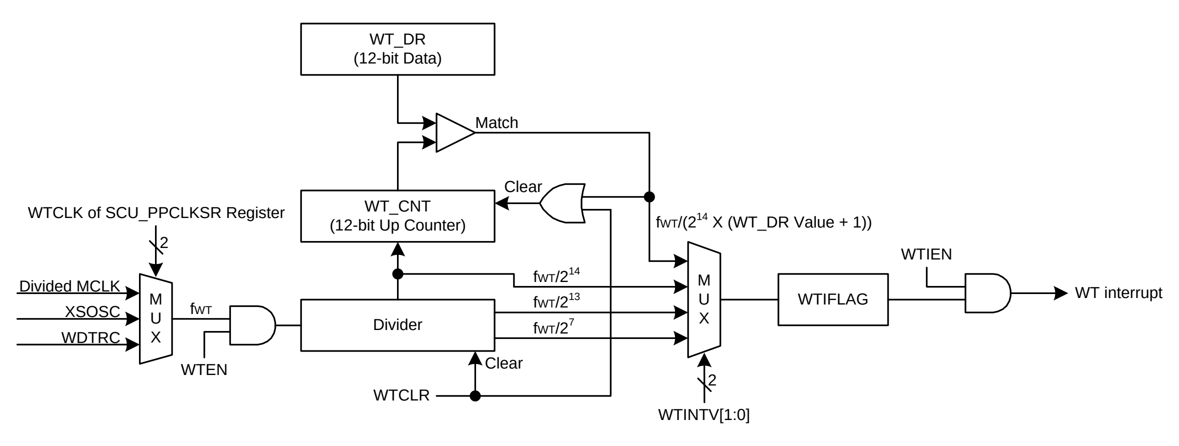


Figure 37. WT Block Diagram

8.2 Registers

Base address and register map of the WT are shown in Table 33 and Table 34.

Table 33. Base Address of WT

Name	Base address
WT	0x4000_2000

Table 34. WT Register Map

Name	Offset	Type	Description	Reset Value
WT_CR	0x0000	RW	WT Control Register	0x00000000
WT_DR	0x0004	RW	WT Data Register	0x00000FFF
WT_CNT	0x0008	RO	WT Counter Register	0x00000000

8.2.1 WT_CR: WT control register

WT_CR register is 32-bit size and accessible in 32/16/8-bit.

WT_CR=0x4000_2000

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Reserved	**WTEN**	**Reserved**	**WTINTV**		**WTIEN**	**Reserved**	**WTIFLAG**	**WTCLR**
0x000000	**0**	**0**	**00**		**0**	**0**	**0**	**0**
-	**RW**	**-**	**RW**		**RW**	**-**	**RW**	**RW**

7	WTEN	Watch Timer Operation Enable.	
		0	Disable watch timer operation.
		1	Enable watch timer operation.
5 4	WTINTV	Watch Timer Interval Selection.	
		00	fWT/2^7
		01	fWT/2^{13}
		10	fWT/2^{14}
		11	fWT/(2^{14}x(WT_DR value + 1))
		NOTE: These bits should be changed while WTEN bit is '0'.	
3	WTIEN	Watch Timer Interrupt Enable.	
		0	Disable watch timer interrupt.
		1	Enable watch timer interrupt.
1	WTIFLAG	Watch Timer Interrupt Flag.	
		0	No request occurred.
		1	Request occurred. The bit is cleared to '0' when '1' is written.
0	WTCLR	Watch Timer Counter and Divider Clear.	
		0	No effect.
		1	Clear the counter and divider (Automatically cleared to '0' after operation)

8.2.2 WT_DR: WT data register

WT_DR register is 32-bit size and accessible in 32/16-bit.

WT_DR=0x4000_2004

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="20">Reserved</td><td colspan="12">WTDATA</td></tr>
<tr><td colspan="20">0x00000</td><td colspan="12">0xFFF</td></tr>
<tr><td colspan="20">–</td><td colspan="12">RW</td></tr>
</table>

11 0	WTDATA	Watch Timer Data. The range is 0x001 to 0xFFF.

8.2.3 WT_CNT: WT counter register

WT_CNT register is 32-bit size and accessible in 32/16-bit.

WT_CNT=0x4000_2008

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="20">Reserved</td><td colspan="12">CNT</td></tr>
<tr><td colspan="20">0x00000</td><td colspan="12">0x000</td></tr>
<tr><td colspan="20">–</td><td colspan="12">RO</td></tr>
</table>

11 0	CNT	Watch Timer Counter.

9 Timer counter 10/11/12

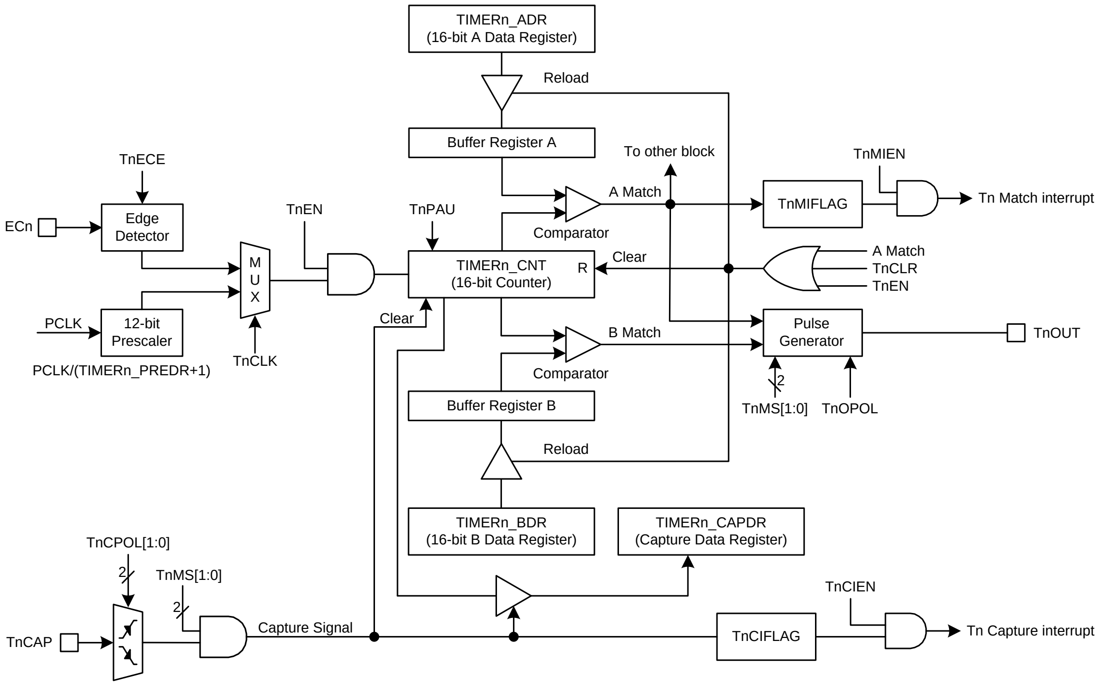
The timer block comprises 3 channels of 16-bit general purpose timers. Each has an independent 16-bit counter and a dedicated prescaler that feeds counting clock. They support periodic timer, PWM pulse, one-shot and capture mode.

One more optional free-run timer is provided. The main purpose of this timer is a periodical tick timer or a wake-up source. The timer counter 10/11/12 features the followings:

- 16-bit up-counter and 12-bit prescaler
- Periodic timer, One-shot timer, PWM pulse, and Capture mode
- Synchronous start and clear function

9.1 Timer counter 10/11/12 block diagram

Figure 38 shows the block diagram of a timer block unit.



NOTES:

1. TnEN bit is automatically cleared to logic "0b" after one pulse is generated at a PPG one-shot mode.
2. After the TnEN bit is set, counting of TIMERn_CNT may be delayed 2 clocks or more.

Figure 38. Timer Counter n Block Diagram (n = 10, 11 and 12)

9.2 Pin description for timer counter 10/11/12

Table 35. Pins and External Signals for Timer Counter n (n = 10, 11 and 12)

PIN NAME	TYPE	DESCRIPTION
ECn	I	External clock input
TnCAP	I	Capture input
TnOUT	O	PWM/one-shot output

9.3 Registers

Base address and register map of the Timer 10/11/12 are shown in Table 36 and Table 37.

Table 36. Base Address of Timer 10/11/12

Name	Base address	Size	Description
TIMER10	0x4000_2100	256	Timer/Counter 10
TIMER11	0x4000_2200	256	Timer/Counter 11
TIMER12	0x4000_2300	256	Timer/Counter 12

Table 37. Timer Register Map (n = 10, 11 and 12)

Name	Offset	Type	Description	Reset value
TIMERn_CR	0x00	RW	Timer/Counter n Control Register	0x00000000
TIMERn_ADR	0x04	RW	Timer/Counter n A Data Register	0x0000FFFF
TIMERn_BDR	0x08	RW	Timer/Counter n B Data Register	0x0000FFFF
TIMERn_CAPDR	0x0C	RO	Timer/Counter n Capture Data Register	0x00000000
TIMERn_PREDR	0x10	RW	Timer/Counter n Prescaler Data Register	0x0000FFFF
TIMERn_CNT	0x14	RO	Timer/Counter n Counter Register	0x00000000

9.3.1 TIMERn_CR: timer/counter n control register

Timer module should be configured properly before running. The timer should be configured with the appropriate value in TIMERn_CR register for designated operating mode. After configuring this register, a user can start or stop the timer function by using this register.

TIMERn_CR register is 32-bit size and accessible in 32/16/8-bit (n = 10, 11 and 12).

TIMER10_CR=0x4000_2100, TIMER11_CR=0x4000_2200, TIMER12_CR=0x4000_2300

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15	14	13 12	11	10 9	8	7 6	5	4	3	2	1	0
Reserved	**TnEN**	**TnCLK**	**TnMS**	**TnECE**	**Reserved**	**TnOPOL**	**TnCPOL**	**TnMIEN**	**TnCIEN**	**TnMIFLAG**	**TnCIFLAG**	**TnPAU**	**TnCLR**
0x0000	**0**	**0**	**00**	**0**	**00**	**0**	**00**	**0**	**0**	**0**	**0**	**0**	**0**
–	**RW**	**RW**	**RW**	**RW**	**-**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**

15	TnEN	Timer n Operation Enable.
		0 Disable timer n operation.
		1 Enable timer n operation. (Counter clear and start)
14	TnCLK	Timer n Clock Selection.
		0 Select an internal prescaler clock.
		1 Select an external clock.
		NOTE: This bit should be changed while TnEN bit is '0'.
13 12	TnMS	Timer n Operation Mode Selection.
		00 Timer/Counter mode. (TnOUT: toggle at A-match)
		01 Capture mode. (The A-match interrupt can occur)
		10 PPG one-shot mode. (TnOUT: Programmable pulse output)
		11 PPG repeat mode. (TnOUT: Programmable pulse output)
		NOTE: This bit should be changed while TnEN bit is '0'.
11	TnECE	Timer n External Clock Edge Selection.
		0 Select falling edge of external clock.
		1 Select rising edge of external clock.
8	TnOPOL	TnOUT Polarity Selection.
		0 Start high. (TnOUT is low level at disable)
		1 Start low. (TnOUT is high level at disable)
7 6	TnCPOL	Timer n Capture Polarity Selection.
		00 Capture on falling edge.
		01 Capture on rising edge.
		10 Capture on both falling and rising edge.
		11 Reserved.
5	TnMIEN	Timer n Match Interrupt Enable.
		0 Disable timer n match interrupt.
		1 Enable timer n match interrupt.
4	TnCIEN	Timer n Capture Interrupt Enable.
		0 Disable timer n capture interrupt.
		1 Enable timer n capture interrupt.
3	TnMIFLAG	Timer n Match Interrupt Flag.
		0 No request occurred.
		1 Request occurred. The bit is cleared to '0' when '1' is written.

2	TnCIFLAG	Timer n Capture Interrupt Flag.	
		0	No request occurred.
		1	Request occurred. The bit is cleared to '0' when '1' is written.
1	TnPAU	Timer n Counter Temporary Pause Control.	
		0	Continue counting.
		1	Temporary pause.
0	TnCLR	Timer n Counter and Prescaler Clear.	
		0	No effect.
		1	Clear timer n counter and prescaler. (Automatically cleared to '0' after operation)

9.3.2 TIMERn_ADR: timer/counter n A data register

TIMERn_ADR register is 32-bit size and accessible in 32/16/8-bit (n = 10, 11 and 12).

TIMER10_ADR=0x4000_2104, TIMER11_ADR=0x4000_2204, TIMER12_ADR=0x4000_2304

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Reserved	**ADATA**
0x0000	**0xFFFF**
-	**RW**

15 0	ADATA	Timer/Counter n A Data. The range is 0x0002 to 0xFFFF.

NOTE: Do not write "0x0000" in the TIMERn_ADR register under PPG mode.

9.3.3 TIMERn_BDR: timer/counter n B data register

TIMERn_BDR register is 32-bit size and accessible in 32/16/8-bit (n = 10, 11 and 12).

TIMER10_BDR=0x4000_2108, TIMER11_BDR=0x4000_2208, TIMER12_BDR=0x4000_2308

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Reserved	**BDATA**
0x0000	**0xFFFF**
–	**RW**

15 0	BDATA	Timer/Counter n B Data. The range is 0x0000 to 0xFFFF.

9.3.4 TIMERn_CAPDR: timer/counter n capture data register

TIMERn_CAPDR register is 32-bit size and accessible in 32/16/8-bit (n = 10, 11 and 12).

TIMER10_CAPDR=0x4000_210C, TIMER11_CAPDR=0x4000_220C, TIMER12_CAPDR=0x4000_230C

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">Reservd</td><td colspan="16">CAPD</td></tr>
<tr><td colspan="16">0x0000</td><td colspan="16">0x0000</td></tr>
<tr><td colspan="16">–</td><td colspan="16">RO</td></tr>
</table>

15 0	CAPD	Timer/Counter n Capture Data.

9.3.5 TIMERn_PREDR: timer/counter n prescaler data register

TIMERn_PREDR register is 32-bit size and accessible in 32/16/8-bit (n = 10, 11 and 12).

TIMER10_PREDR=0x4000_2110, TIMER11_PREDR=0x4000_2210, TIMER12_PREDR=0x4000_2310

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="20">Reserved</td><td colspan="12">PRED</td></tr>
<tr><td colspan="20">0x00000</td><td colspan="12">0xFFF</td></tr>
<tr><td colspan="20">–</td><td colspan="12">RW</td></tr>
</table>

11 0	PRED	Timer/Counter n Prescaler Data.

9.3.6 TIMERn_CNT: timer/counter n counter register

TIMERn_CNT register is 32-bit size and accessible in 32/16/8-bit (n = 10, 11 and 12).

TIMER10_CNT=0x4000_2114, TIMER11_CNT=0x4000_2214, TIMER12_CNT=0x4000_2314

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Reservd	**CNT**
0x0000	**0x0000**
-	**RO**

15 0	CNT	Timer/Counter n Counter.

9.4 Functional description

9.4.1 Timer counter 10/11/12

Timer/counter n can use an internal or an external clock source (ECn). A clock selection logic can select a clock source and it is controlled by clock selection bits (TnCLK).

- Timer n clock source: {PCLK/(TIMERn_PREDR+1)}, ECn

In Capture mode, by TnCAP, data is captured into a corresponding capture data register (TIMERn_CAPDR). Timer n outputs the comparison result between counter and data register through TnOUT port in Timer/counter mode. Also, timer n output PWM waveform through TnOUT port under PPG mode. (n = 10, 11 and 12)

Table 38. Timer n Operating Modes (n = 10, 11 and 12)

TnEN	Alternative Mode	TnMS	TIMERn_PREDR	Timer n
1	TIMER10: PE_AFSR1[27:24] = 0x1 TIMER11: PE_AFSR1[31:28] = 0x1 TIMER12: PA_AFSR1[23:20] = 0x1	00	0xXXX	Timer/Counter Mode
1	TIMER10: PE_AFSR1[27:24] = 0x2 TIMER11: PE_AFSR1[31:28] = 0x2 TIMER12: PA_AFSR1[23:20] = 0x2	01	0xXXX	Capture Mode
1	TIMER10: PE_AFSR1[27:24] = 0x1 TIMER11: PE_AFSR1[31:28] = 0x1 TIMER12: PA_AFSR1[23:20] = 0x1	10	0xXXX	PPG Mode (one-shot mode)
1		11	0xXXX	PPG Mode (repeat mode)

9.4.2 16-bit Timer/counter mode

16-bit Timer/counter mode is selected by control register as shown in Figure 39. The 16-bit timer has a counter register and a data register. The counter register is increased by internal or external clock input. Timer n can use an input clock with 12-bit prescaler division rates (TIMERn_PREDR) and an external clock (ECn). When the values of TIMERn_CNT and TIMERn_ADR are the same in the timer n, a match signal is generated and the interrupt of Timer n takes place.

The TIMERn_CNT values are automatically cleared by the match signal. It can also be cleared by software (TnCLR).

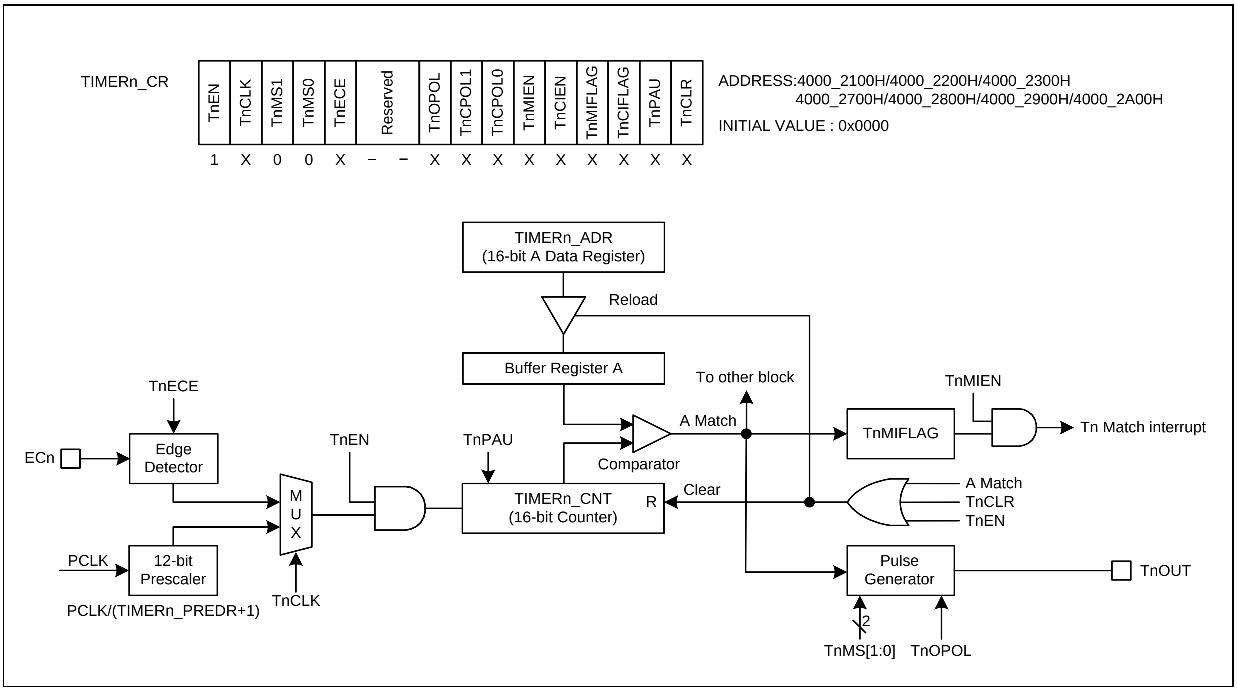


Figure 39. 16-bit Timer/Counter Mode for Timer n (n = 10, 11 and 12)

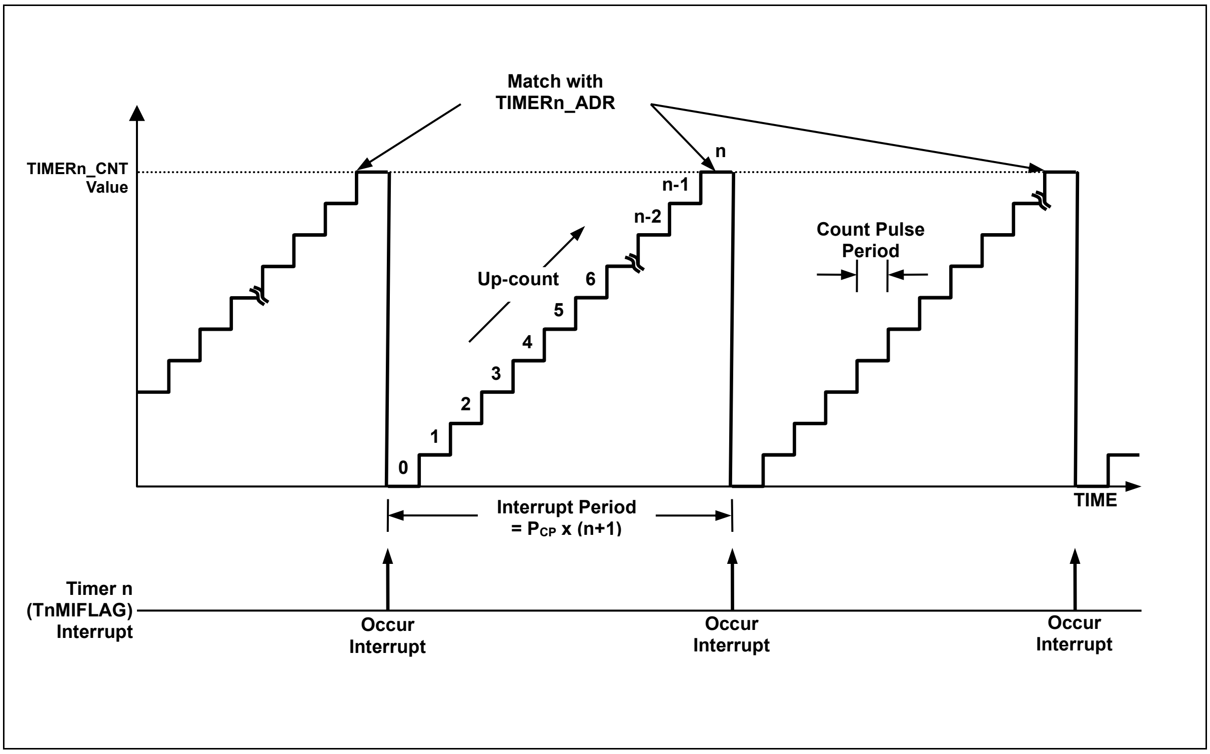


Figure 40. 16-bit Timer/Counter n Example (n = 10, 11 and 12)

9.4.3 16-bit Capture mode

Timer n Capture mode is evoked by configuring TnMS[1:0] as '01'. The internal clock can be used as a clock source. It basically has the same function as the 16-bit timer/counter mode and an interrupt takes place when TIMERn_CNT becomes equal to TIMERn_ADR.

This timer interrupt in Capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer. The capture result is loaded into TIMERn_CAPDR. In the timer n capture mode, timer n output (TnOUT) waveform is not available.

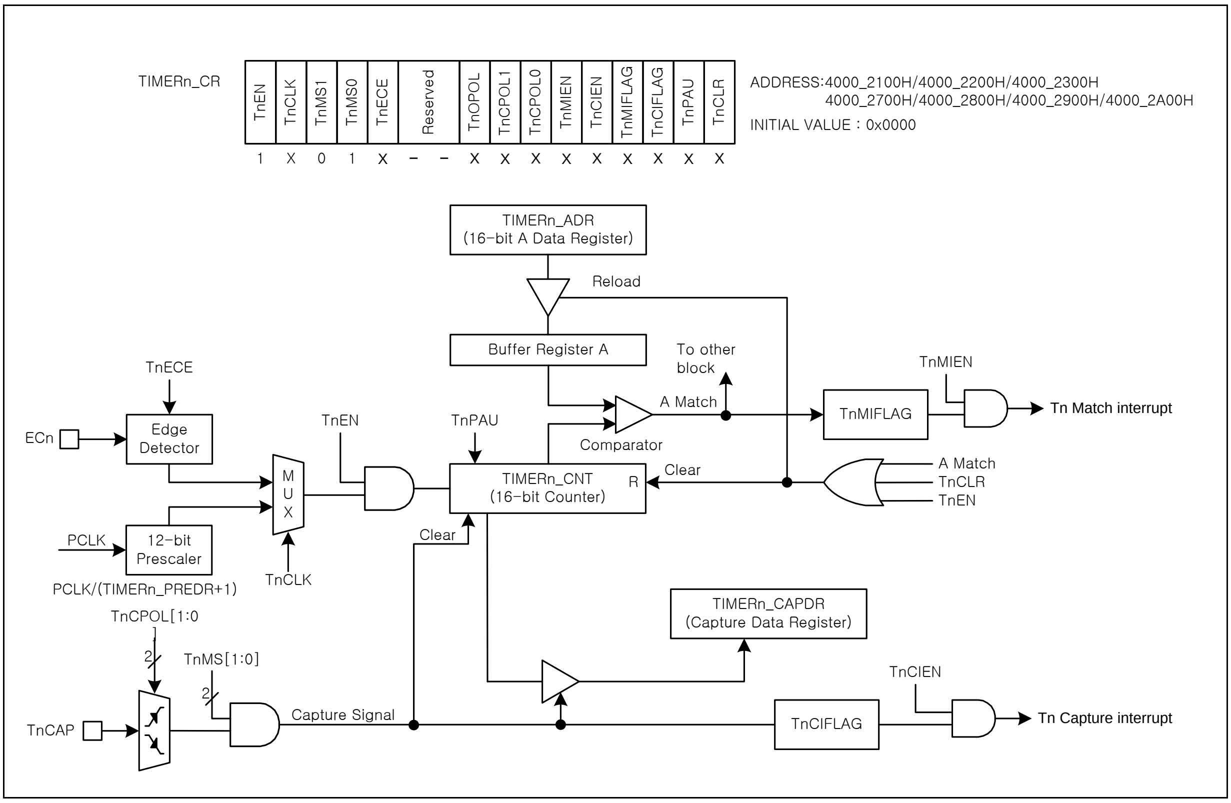


Figure 41. 16-bit Capture Mode for Timer n (n = 10, 11 and 12)

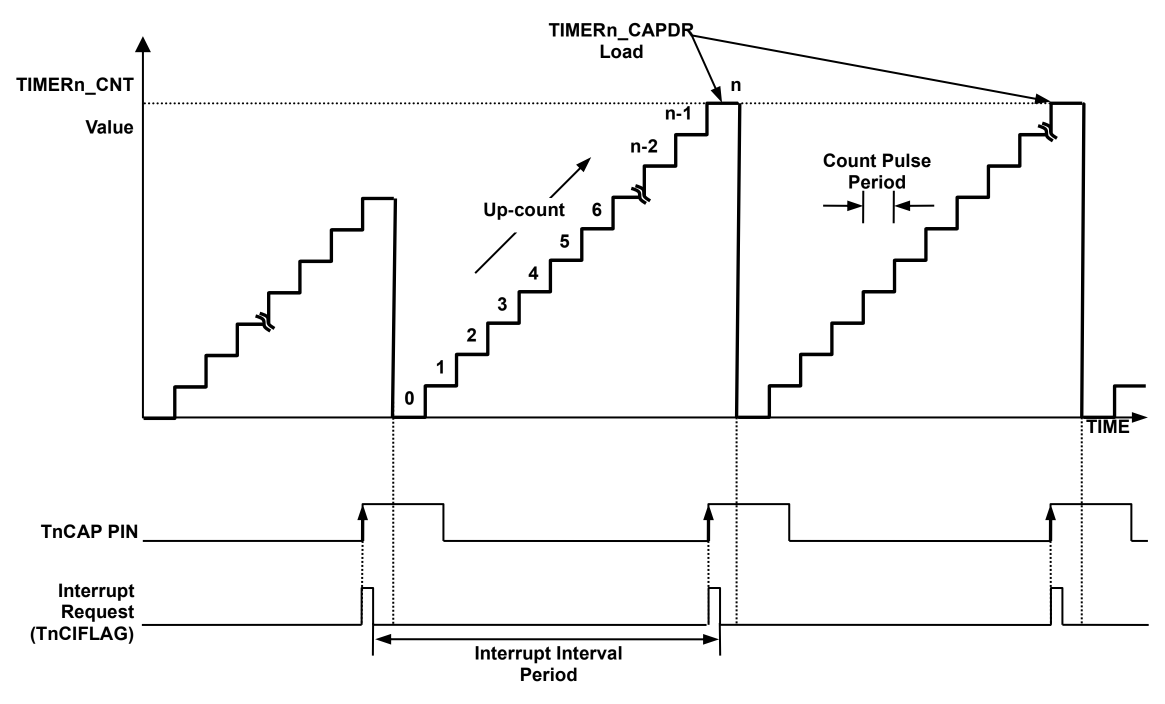


Figure 42. 16-bit Capture Mode for Timer n (n = 10, 11 and 12)

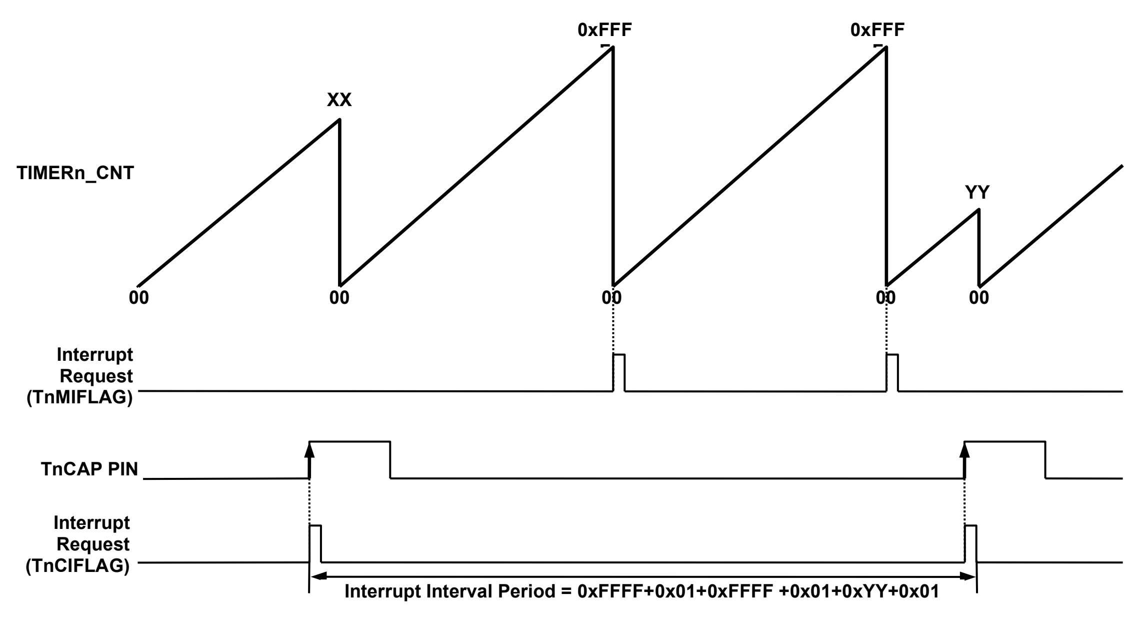
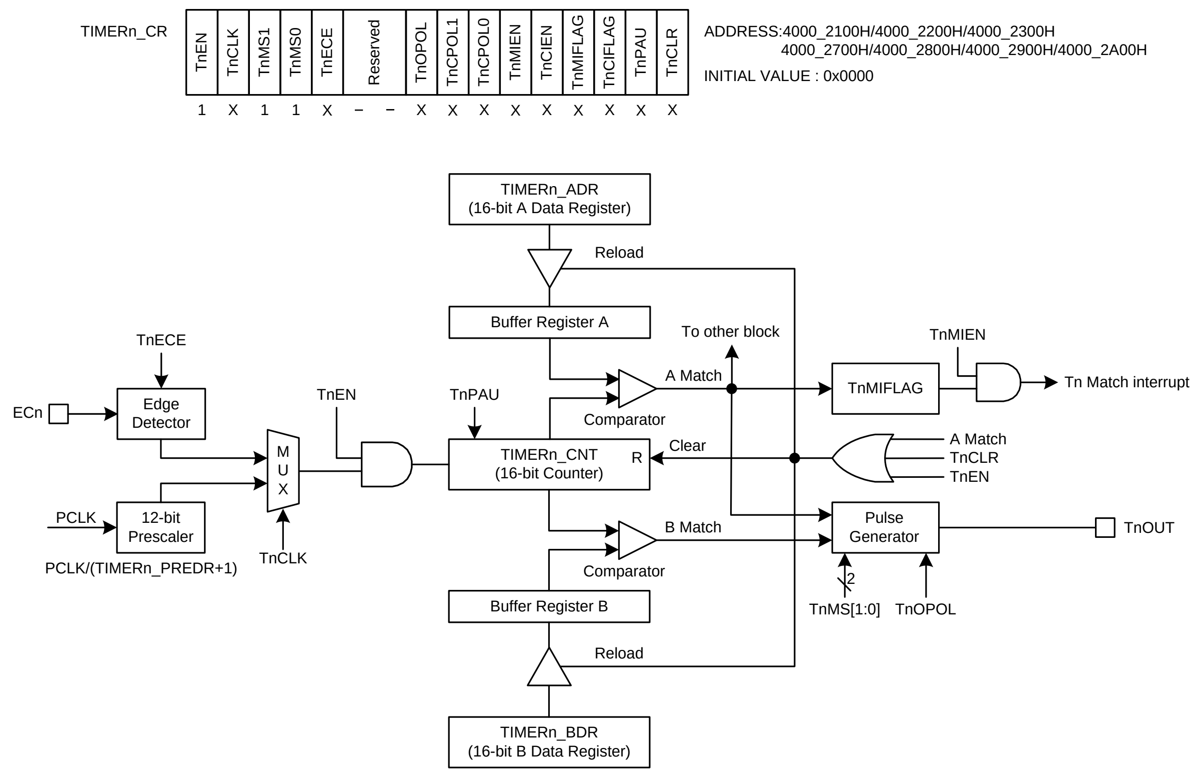


Figure 43. Express Timer Overflow in Capture Mode (n = 10, 11 and 12)

9.4.4 16-bit PPG mode

Timer n has a PPG (Programmable Pulse Generation) function. In PPG mode, the TnOUT pin generates PWM output of up to 16-bit resolution. This pin should be configured as a PWM output by setting Px_AFSR1, Px_AFSR2 to 'AF1'. The period of PWM output is determined by the TIMERn_ADR. The duty of PWM output is determined by TIMERn_BDR. (x = A to F)



NOTE: The TnEN is automatically cleared to logic '0' after one pulse is generated in PPG one-shot mode.

Figure 44. 16-bit PPG Repeat and One-shot Mode for Timer n (n = 10, 11 and 12)

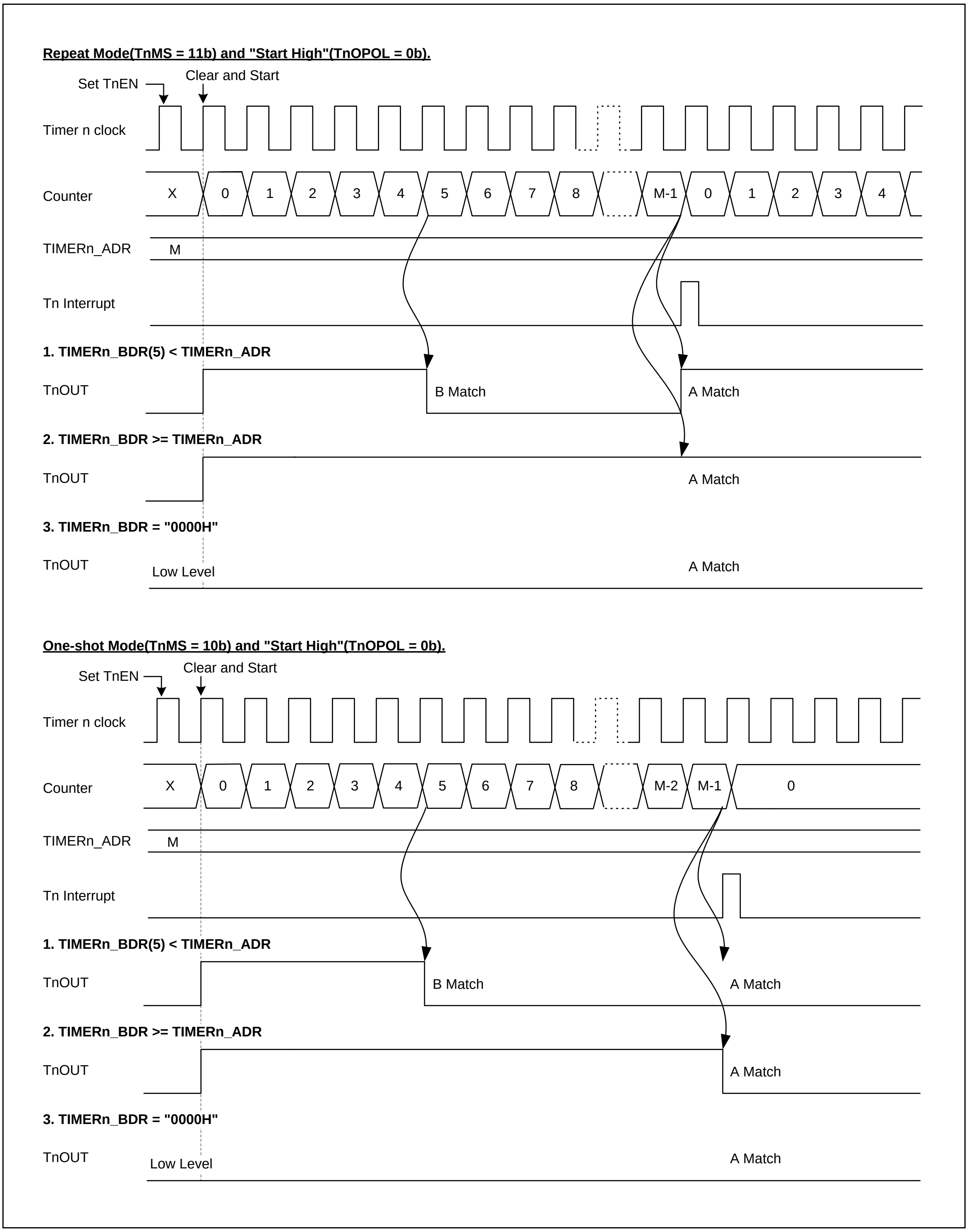


Figure 45. 16-bit PPG Mode Timing chart for Timer n (n = 10, 11 and 12)

10 Timer counter 20

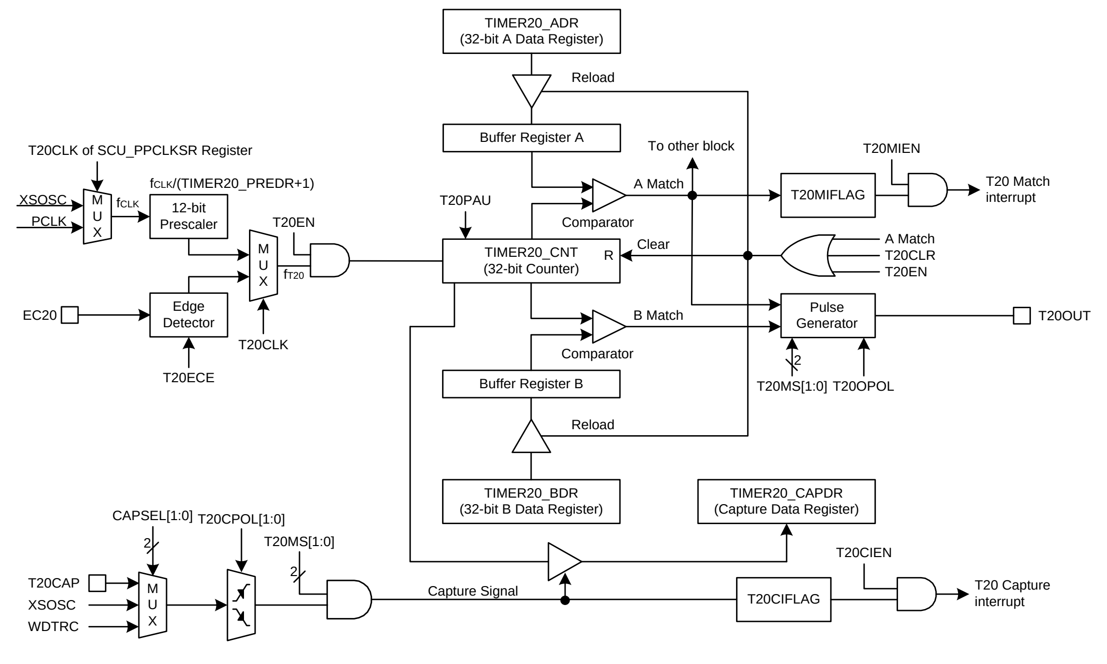
A timer block comprises a single channel 32-bit general purpose timer. This timer has an independent 32-bit counter and a dedicated prescaler that feeds counting clock. It supports periodic timer, PWM pulse, one-shot timer and capture mode.

One more optional free-run timer is provided. Main purpose of this timer is a periodical tick timer or a wake-up source. The Timer counter 20 features the followings:

- 32-bit up-counter and 12-bit prescaler
- Periodic timer, One-shot timer, PWM pulse, and Capture mode
- Synchronous start and clear function

10.1 Timer counter 20 block diagram

Figure 46 shows the block diagram of a timer block unit.



NOTES:

1. T20EN is automatically cleared to logic '0' after one pulse is generated in PPG one-shot mode.
2. After T20EN bit is set, counting of TIMER20_CNT may be delayed by 2 clocks or more.

Figure 46. Timer Counter 20 Block Diagram

10.2 Pin description for Timer counter 20

Table 39. Pins and External Signals for Timer Counter 20

PIN NAME	TYPE	DESCRIPTION
EC20	I	External clock input
T20CAP	I	Capture input
T20OUT	O	PWM/one-shot output

10.3 Registers

Base address and register map of the Timer 20 are shown in Table 40 and Table 41.

Table 40. Base Address of Timer 20

Name	Base address
TIMER20	0x4000_2500

Table 41. Timer Register Map

Name	Offset	Type	Description	Reset value
TIMER20_CR	0x0000	RW	Timer/Counter 20 Control Register	0x00000000
TIMER20_ADR	0x0004	RW	Timer/Counter 20 A Data Register	0xFFFFFFFF
TIMER20_BDR	0x0008	RW	Timer/Counter 20 B Data Register	0xFFFFFFFF
TIMER20_CAPDR	0x000C	RO	Timer/Counter 20 Capture Data Register	0x00000000
TIMER20_PREDR	0x0010	RW	Timer/Counter 20 Prescaler Data Register	0x00000FFF
TIMER20_CNT	0x0014	RO	Timer/Counter 20 Counter Register	0x00000000

10.3.1 TIMER20_CR: timer/counter 20 control register

Timer module should be configured properly before running. Once target purpose is defined, the timer can be configured in the TIMER20_CR register. After configuring this register, a user can start or stop the timer function by using this register.

TIMER20_CR register is 32-bit size and accessible in 32/16/8-bit.

TIMER20_CR=0x4000_2500

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15	14	13 12	11	10 9	8	7 6	5	4	3	2	1	0
Reserved	**T20EN**	**T20CLK**	**T20MS**	**T20ECE**	**CAPSEL**	**T20OPOL**	**T20CPOL**	**T20MIEN**	**T20CIEN**	**T20MIFLAG**	**T20CIFLAG**	**T20PAU**	**T20CLR**
0x0000	**0**	**0**	**00**	**0**	**00**	**0**	**00**	**0**	**0**	**0**	**0**	**0**	**0**
–	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**

15	T20EN	Timer 20 Operation Enable.	
		0	Disable timer 20 operation.
		1	Enable timer 20 operation. (Counter clear and start)
14	T20CLK	Timer 20 Clock Selection.	
		0	Select an internal prescaler clock.
		1	Select an external clock.
		NOTE:	This bit should be changed while T20EN bit is '0'.
13 12	T20MS	Timer 20 Operation Mode Selection.	
		00	Timer/Counter mode. (T20OUT: toggle at A-match)
		01	Capture mode. (The A-match interrupt can occur)
		10	PPG one-shot mode. (T20OUT: Programmable pulse output)
		11	PPG repeat mode. (T20OUT: Programmable pulse output)
		NOTE:	This bit should be changed while T20EN bit is '0'.
11	T20ECE	Timer 20 External Clock Edge Selection.	
		0	Select falling edge of external clock.
		1	Select rising edge of external clock.
10 9	CAPSEL	Timer 20 Capture Signal Selection.	
		00	Select an external capture signal.
		01	Select the XSOSC (External sub oscillator) signal.
		10	Select the WDTRC (Watchdog timer RC oscillator) signal.
		11	Not used
		NOTE:	This bit should be changed while T20EN bit is '0'.
8	T20OPOL	T20OUT Polarity Selection.	
		0	Start high. (T20OUT is low level at disable)
		1	Start low. (T20OUT is high level at disable)
7 6	T20CPOL	Timer 20 Capture Polarity Selection.	
		00	Capture on falling edge.
		01	Capture on rising edge.
		10	Capture on both falling and rising edge.
		11	Reserved.
5	T20MIEN	Timer 20 Match Interrupt Enable.	
		0	Disable timer 20 match interrupt.
		1	Enable timer 20 match interrupt.

4	T20CIEN	Timer 20 Capture Interrupt Enable.	
		0	Disable timer 20 capture interrupt.
		1	Enable timer 20 capture interrupt.
3	T20MIFLAG	Timer 20 Match Interrupt Flag bit.	
		0	No request occurred.
		1	Request occurred. The bit is cleared to ‘0’ when ‘1’ is written.
2	T20CIFLAG	Timer 20 Capture Interrupt Flag bit.	
		0	No request occurred.
		1	Request occurred. The bit is cleared to ‘0’ when ‘1’ is written.
1	T20PAU	Timer 20 Counter Temporary Pause Control bit.	
		0	Continue counting.
		1	Temporary pause.
0	T20CLR	Timer 20 Counter and Prescaler Clear bit.	
		0	No effect.
		1	Clear timer 20 counter and prescaler. (Automatically cleared to ‘0’ after operation)

10.3.2 TIMER20_ADR: timer/counter 20 A data register

TIMER20_ADR register is 32-bit size and accessible in 32/16/8-bit.

TIMER20_ADR=0x4000_2504

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">ADATA</td></tr>
<tr><td colspan="32">0xFFFFFFFF</td></tr>
<tr><td colspan="32">RW</td></tr>
</table>

31 0	ADATA	Timer/Counter 20 A Data. The range is 0x00000002 to 0xFFFFFFFF. **NOTE**: Do not write "0x00000000" in the TIMER20_ADR register under PPG mode.

10.3.3 TIMER20_BDR: Timer/Counter 20 B Data Register

TIMER20_BDR register is 32-bit size and accessible in 32/16/8-bit.

TIMER20_BDR=0x4000_2508

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">BDATA</td></tr>
<tr><td colspan="32">0xFFFFFFFF</td></tr>
<tr><td colspan="32">RW</td></tr>
</table>

31 0	BDATA	Timer/Counter 20 B Data. The range is 0x00000000 to 0xFFFFFFFF.

10.3.4 TIMER20_CAPDR: Timer/Counter 20 Capture Data Register

TIMER20_CAPDR register is 32-bit size and accessible in 32/16/8-bit.

TIMER20_CAPDR=0x4000_250C

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CAPD</td></tr>
<tr><td colspan="32">0x00000000</td></tr>
<tr><td colspan="32">RO</td></tr>
</table>

31 0	CAPD	Timer/Counter 20 Capture Data.

10.3.5 TIMER20_PREDR: Timer/Counter 20 Prescaler Data Register

TIMER20_PREDR register is 32-bit size and accessible in 32/16/8-bit.

TIMER20_PREDR=0x4000_2510

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="20">Reserved</td><td colspan="12">PRED</td></tr>
<tr><td colspan="20">0x00000</td><td colspan="12">0xFFF</td></tr>
<tr><td colspan="20">–</td><td colspan="12">RW</td></tr>
</table>

11 0	PRED	Timer/Counter 20 Prescaler Data.

10.3.6 TIMER20_CNT: Timer/Counter 20 Counter Register

TIMER20_CNT register is 32-bit size and accessible in 32/16/8-bit.

TIMER20_CNT=0x4000_2514

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">CNT</td></tr>
<tr><td colspan="32">0x00000000</td></tr>
<tr><td colspan="32">RO</td></tr>
</table>

31 0	CNT	Timer/Counter 20 Counter.

10.4 Functional description

10.4.1 Timer counter 20

Timer/counter 20 can use an internal or an external clock as a clock source (EC20). A clock selection logic selects the clock source and the clock selection logic is controlled by clock selection bits (T20CLK).

- TIMER 20 clock sources are listed as followings:
  - PCLK/(TIMER20_PREDR +1)
  - XSOSC/(TIMER20_PREDR +1)
  - EC20

In capture mode, by T20CAP, XSOSC or WDTRC data is captured into input capture data register (TIMER20_CAPDR). Timer 20 outputs the comparison result between counter and data register through T20OUT port in Timer/counter mode. In addition, Timer 20 outputs PWM waveform through T20OUT port in PPG mode.

Table 42. Timer 20 Operating Modes

T20EN	Alternative mode	T20MS[1:0]	TIMER20_PREDR	Timer 20
1	PC_AFSR1[3:0] = 0x1	00	0xXXX	32-bit Timer/Counter Mode
1	PC_AFSR1[3:0] = 0x2	01	0xXXX	32-bit Capture Mode
1	PC_AFSR1[3:0] = 0x1	10	0xXXX	32-bit PPG Mode(one-shot mode)
1	PC_AFSR1[3:0] = 0x1	11	0xXXX	32-bit PPG Mode(repeat mode)

10.4.2 32-bit Timer/counter mode

32-bit Timer/counter mode is selected by control register as shown in Figure 47. The 32-bit timer has a counter register and a data register. The counter register is increased by internal or external clock input. Timer 20 can use an input clock with 12-bit prescaler division rates (TIMER20_PREDR) and an external Clock (EC20). When the values of TIMER20_CNT and TIMER20_ADR are the same in the timer 20, a match signal is generated and the interrupt of Timer 20 takes place. The TIMER20_CNT values are automatically cleared by match signal. It can also be cleared by software (T20CLR).

The TIMER20_CNT values are automatically cleared by match signal. It can also be cleared by software (T20CLR).

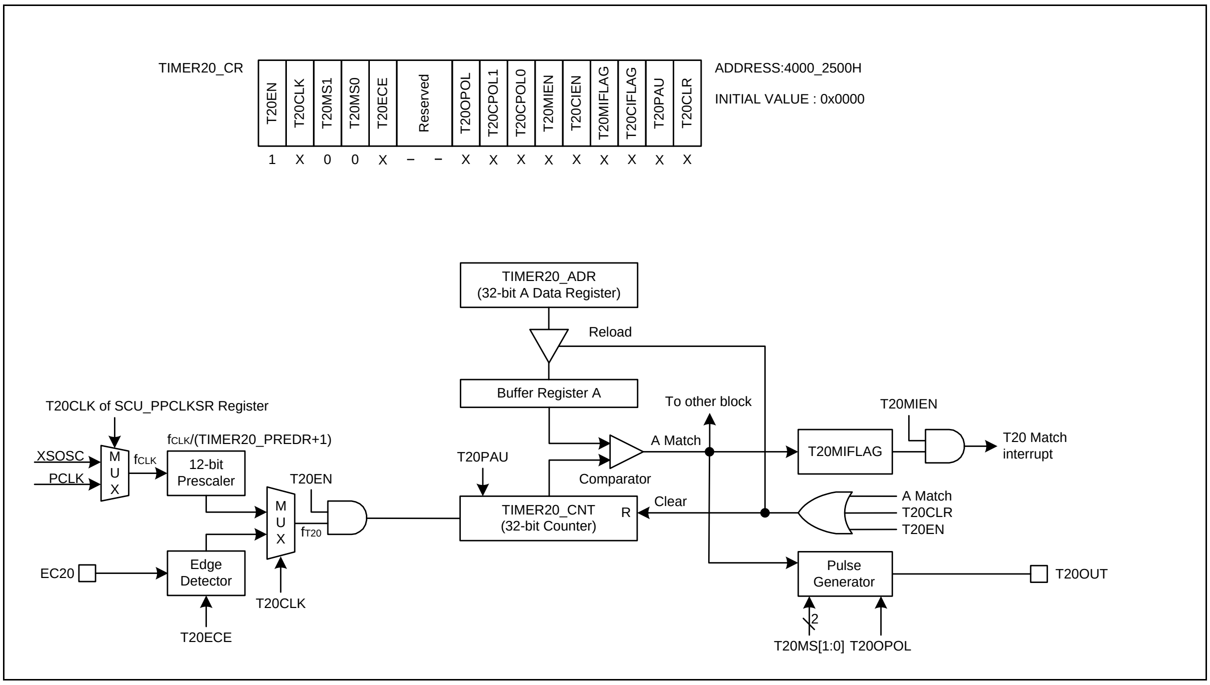


Figure 47. 32-bit Timer/Counter Mode for Timer 20

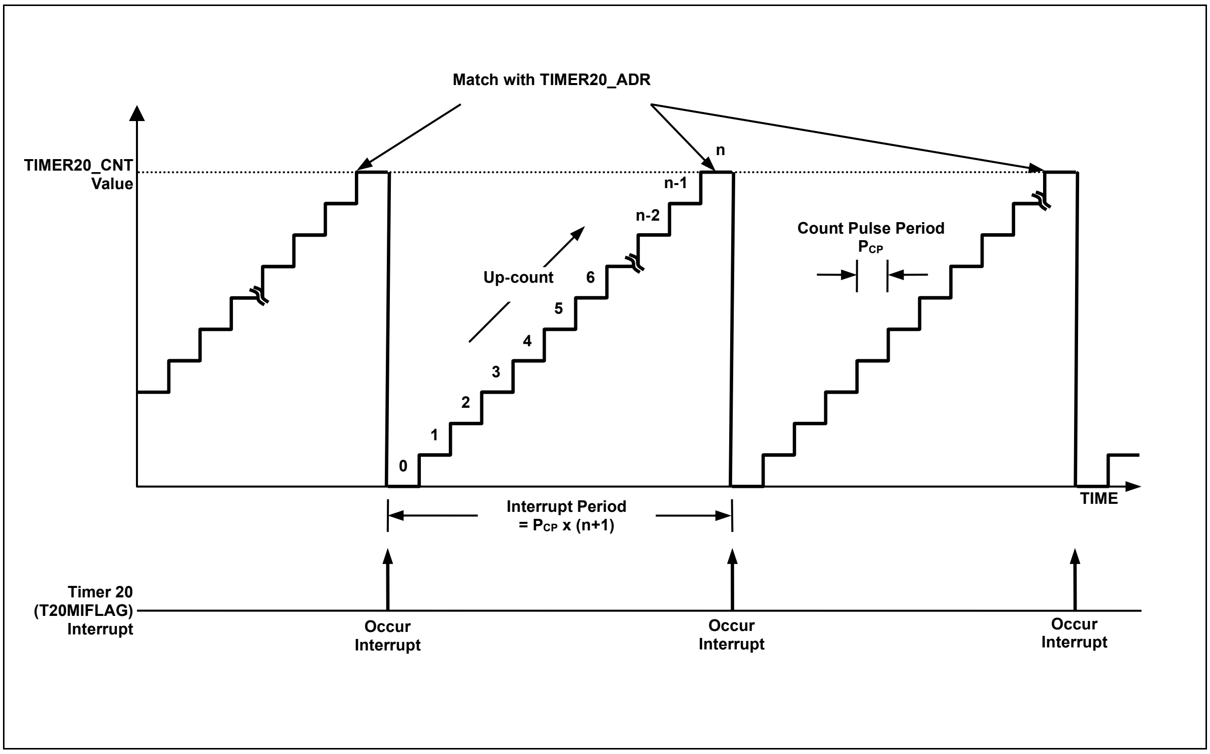


Figure 48. 32-bit Timer/Counter 20 Example

10.4.3 32-bit Capture mode

Timer 20 Capture mode is evoked by configuring T20MS[1:0] as '01'. The internal clock can be used as a clock source. It basically has the same function as the 32-bit timer/counter mode and an interrupt takes place when TIMER20_CNT becomes equal to TIMER20_ADR. TIMER20_CNT values are cleared by software (T20CLR).

This timer interrupt in Capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer. The capture result is loaded into TIMER20_CAPDR. In the timer 20 capture mode, timer 20 output (T20OUT) waveform is not available.

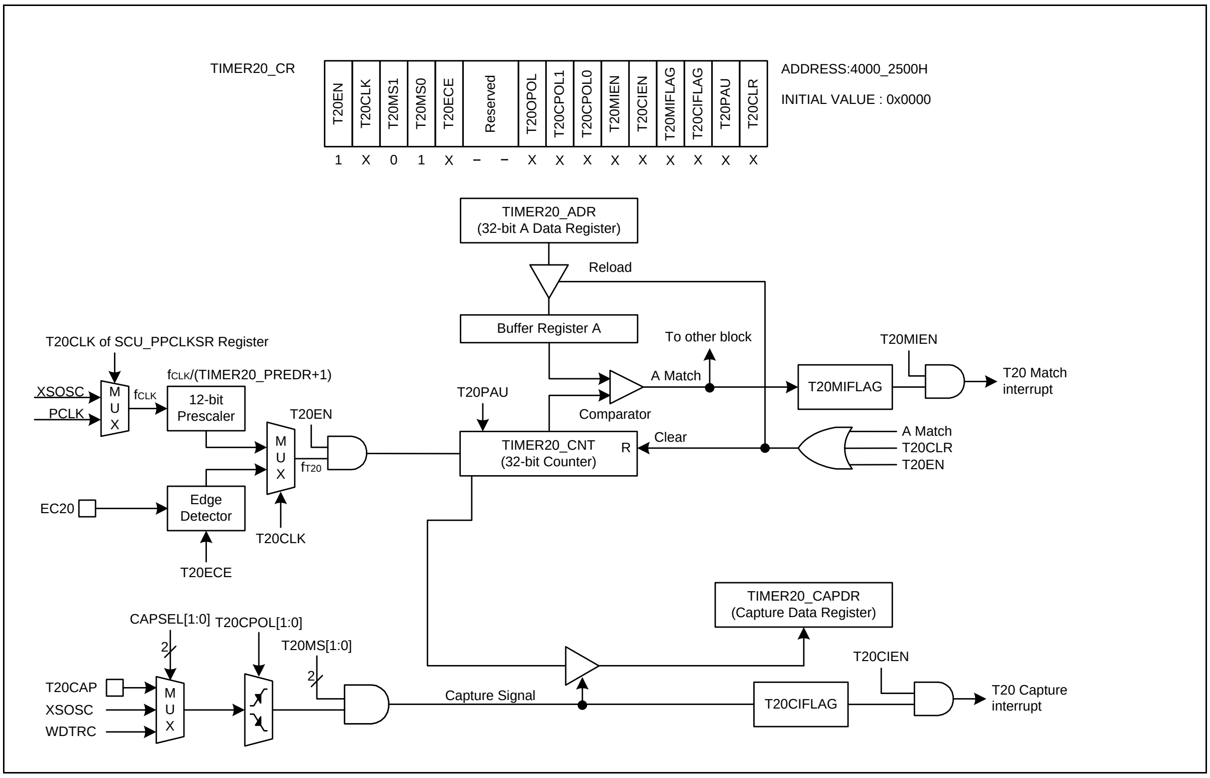


Figure 49. 32-bit Capture Mode for Timer 20

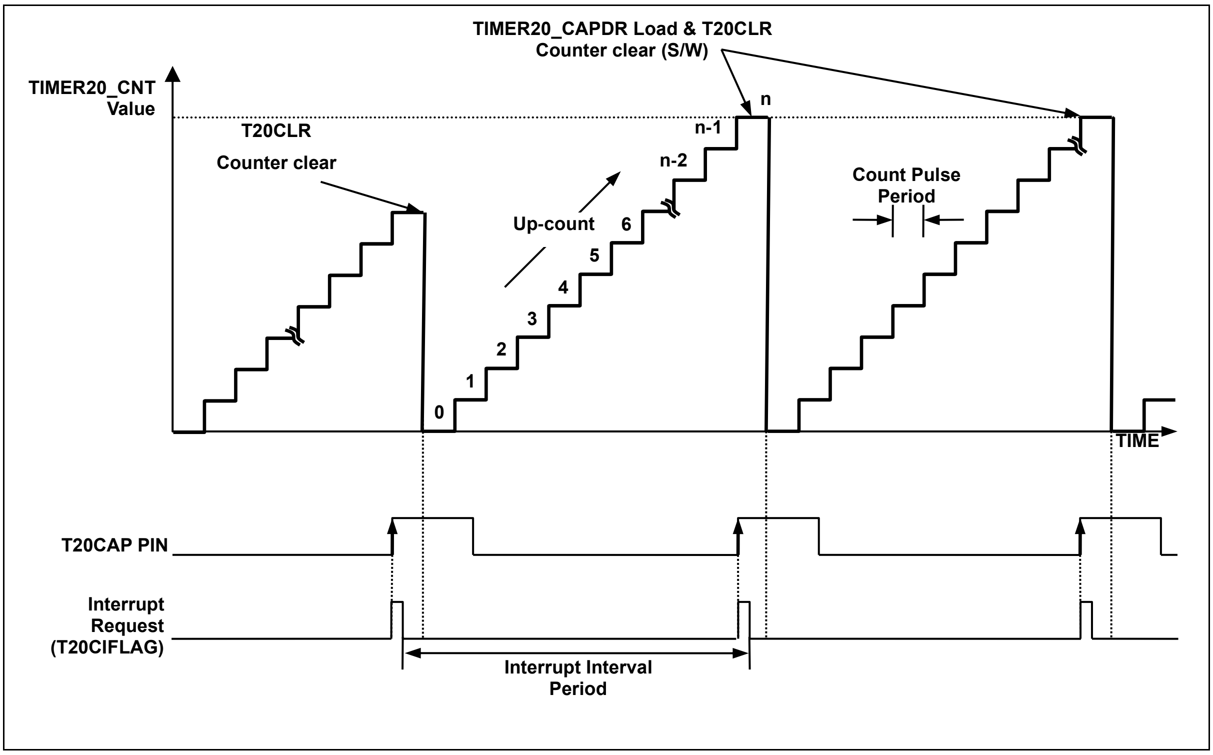


Figure 50. 32-bit Capture Mode for Timer 20

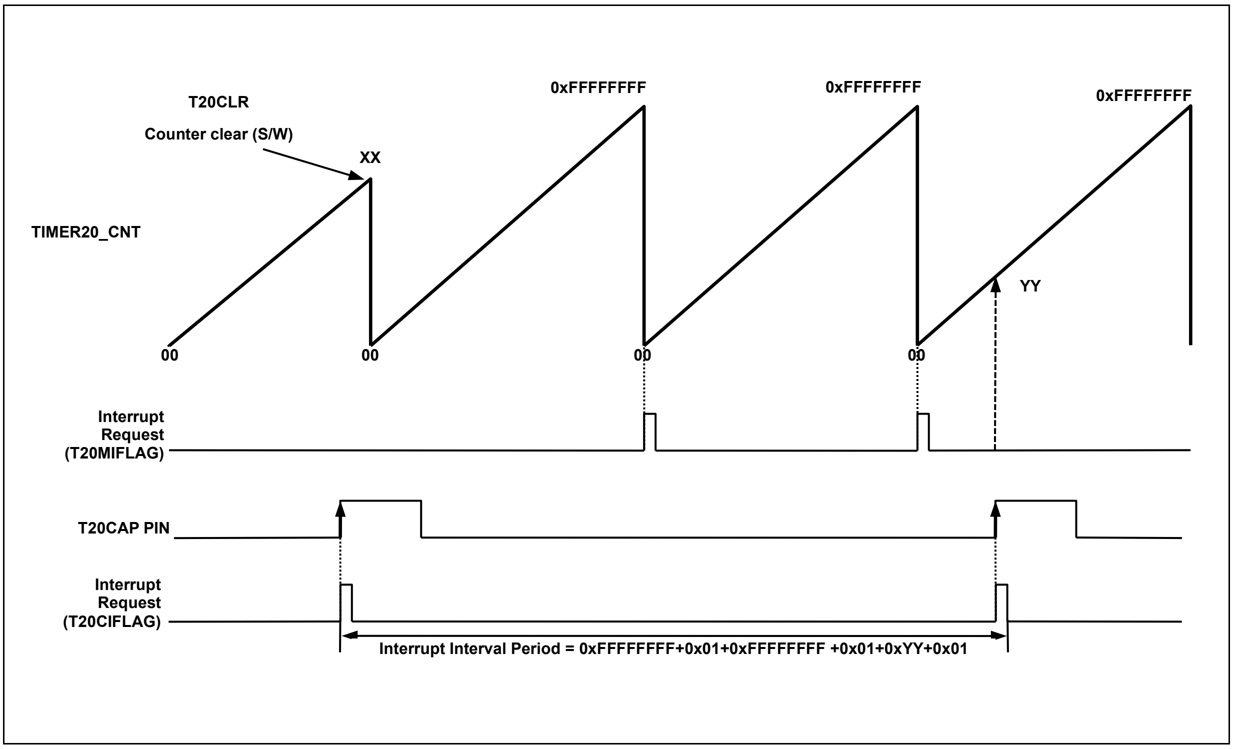
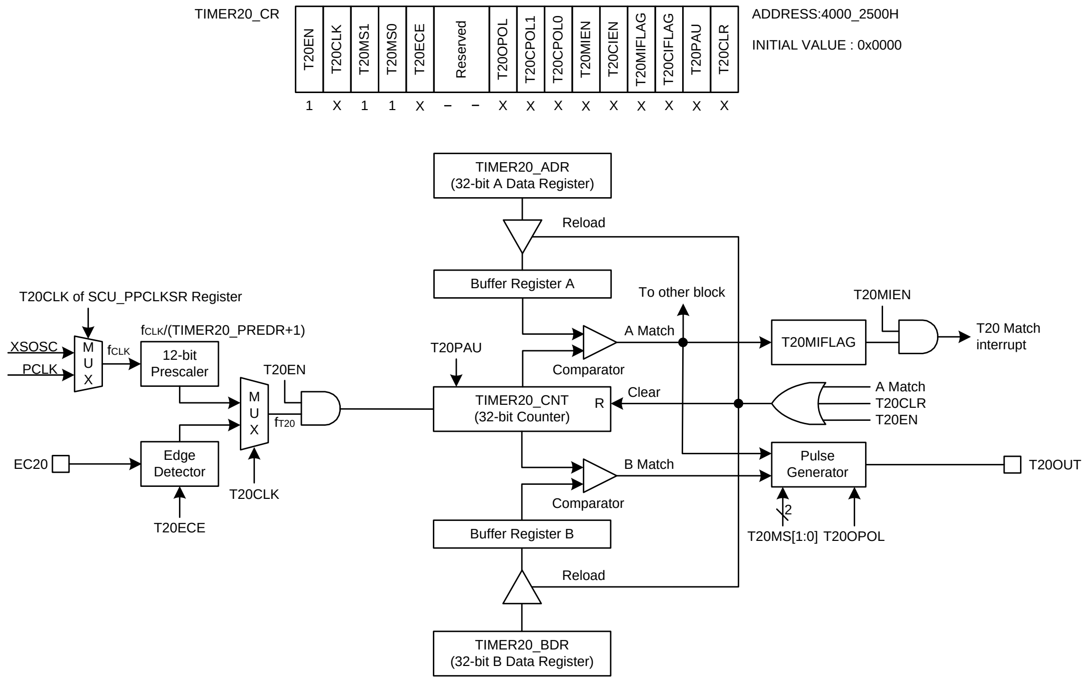


Figure 51. Express Timer Overflow in Capture Mode

10.4.4 32-bit PPG mode

Timer 20 has a PPG (Programmable Pulse Generation) function. In PPG mode, the T20OUT pin generates PWM output of up to 32-bit resolution. This pin should be configured as a PWM output by setting PC_AFSR1[3:0] to 'AF1'. The period of PWM output is determined by the TIMER20_ADR. The duty of PWM output is determined by TIMER20_BDR.



NOTE: The T20EN is automatically cleared to logic '0' after one pulse is generated in PPG one-shot mode.

Figure 52. 32-bit PPG Repeat and One-shot Mode for Timer 20

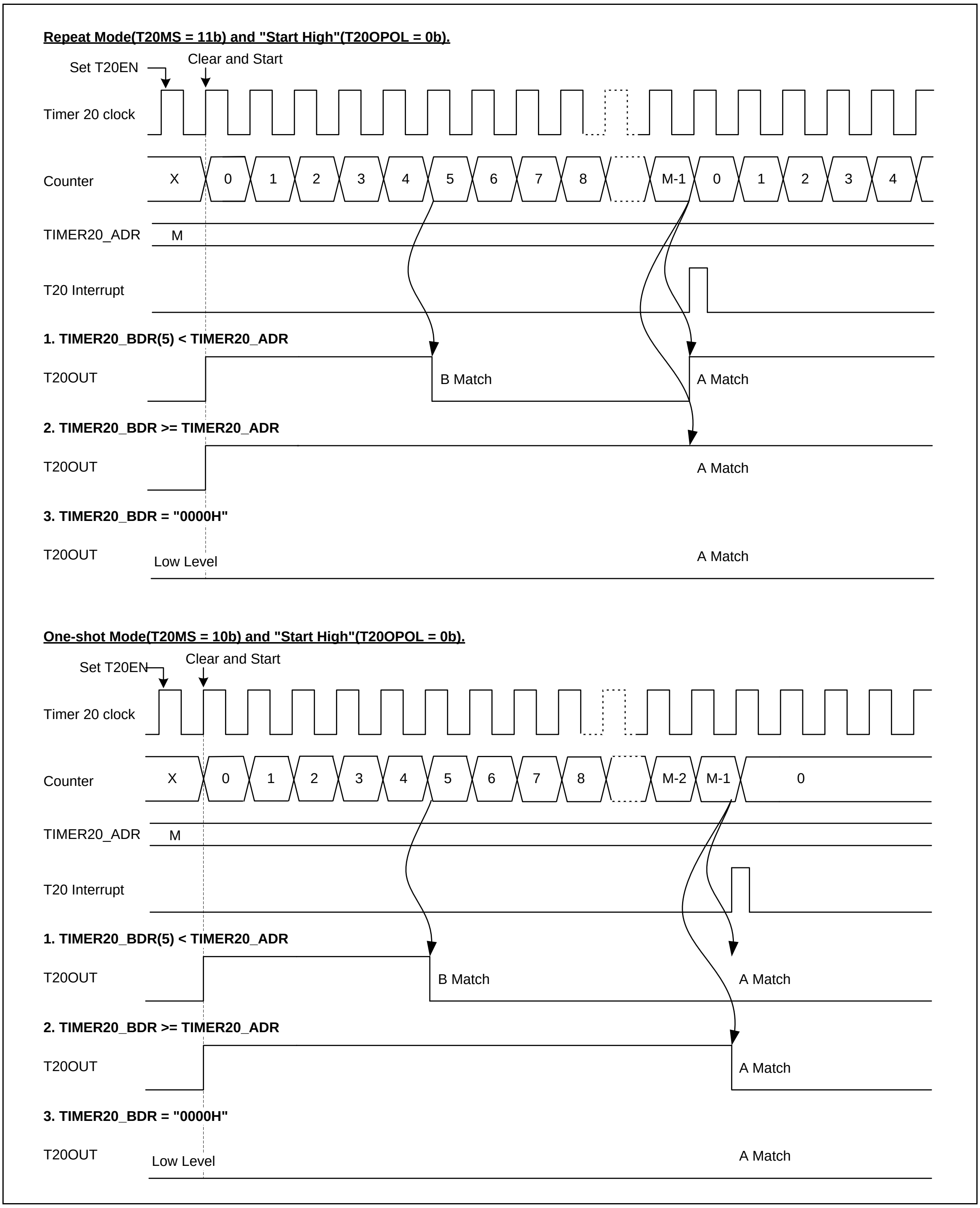


Figure 53. 32-bit PPG Mode Timing chart for Timer 20

11 Timer counter 21

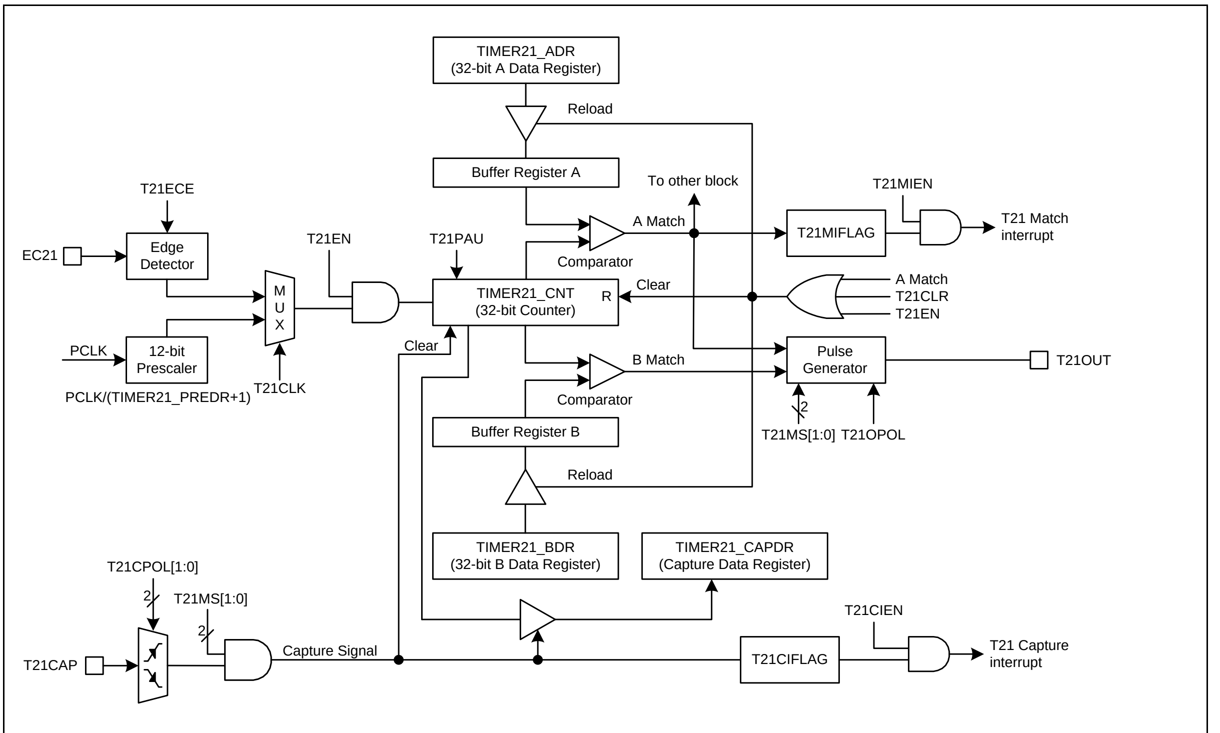
A timer block comprises a single channel 32-bit general purpose timer. This timer has an independent 32-bit counter and a dedicated prescaler that feeds counting clock. It supports periodic timer, PWM pulse, one-shot timer and capture mode.

One more optional free-run timer is provided. Main purpose of this timer is a periodical tick timer or a wake-up source. The Timer counter 21 features the followings:

- 32-bit up-counter and 12-bit prescaler
- Periodic timer, One-shot timer, PWM pulse, and Capture mode
- Synchronous start and clear function

11.1 Timer counter 21 block diagram

Figure 54 shows the block diagram of a timer block unit.



NOTES:

1. T21EN is automatically cleared to logic '0' after one pulse is generated in PPG one-shot mode.
2. After T21EN bit is set, counting of TIMER21_CNT may be delayed by 2 clocks or more.

Figure 54. Timer Counter 21 Block Diagram

11.2 Pin description for Timer counter 21

Table 43. Pins and External Signals for Timer Counter 21

PIN NAME	TYPE	DESCRIPTION
EC21	I	External clock input
T21CAP	I	Capture input
T21OUT	O	PWM/one-shot output

11.3 Registers

Base address and register map of the Timer 21 are shown in Table 44 and Table 45.

Table 44. Base Address of Timer 21

Name	Base address
TIMER21	0x4000_2600

Table 45. Timer Register Map

Name	Offset	Type	Description	Reset value
TIMER21_CR	0x0000	RW	Timer/Counter 21 Control Register	0x00000000
TIMER21_ADR	0x0004	RW	Timer/Counter 21 A Data Register	0xFFFFFFFF
TIMER21_BDR	0x0008	RW	Timer/Counter 21 B Data Register	0xFFFFFFFF
TIMER21_CAPDR	0x000C	RO	Timer/Counter 21 Capture Data Register	0x00000000
TIMER21_PREDR	0x0010	RW	Timer/Counter 21 Prescaler Data Register	0x00000FFF
TIMER21_CNT	0x0014	RO	Timer/Counter 21 Counter Register	0x00000000

11.3.1 TIMER21_CR: timer/counter 21 control register

Timer module should be configured properly before running. Once target purpose is defined, the timer can be configured in the TIMER21_CR register. After configuring this register, a user can start or stop the timer function by using this register.

TIMER21_CR register is 32-bit size and accessible in 32/16/8-bit.

TIMER21_CR=0x4000_2600

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	**T21EN**	**T21CLK**	**T21MS**		**T21ECE**	**Reserved**		**T21OPOL**	**T21CPOL**		**T21MIEN**	**T21CIEN**	**T21MIFLAG**	**T21CIFLAG**	**T21PAU**	**T21CLR**
0x0000	**0**	**0**	**00**		**0**	**00**		**0**	**00**		**0**	**0**	**0**	**0**	**0**	**0**
–	**RW**	**RW**	**RW**		**RW**	**-**		**RW**	**RW**		**RW**	**RW**	**RW**	**RW**	**RW**	**RW**

15	T21EN	Timer 21 Operation Enable.
		0 Disable timer 21 operation.
		1 Enable timer 21 operation. (Counter clear and start)
14	T21CLK	Timer 21 Clock Selection.
		0 Select an internal prescaler clock.
		1 Select an external clock.
		Note) 1. This bit should be changed while T21EN bit is '0'.
13 12	T21MS	Timer 21 Operation Mode Selection.
		00 Timer/Counter mode. (T21OUT: toggle at A-match)
		01 Capture mode. (The A-match interrupt can occur)
		10 PPG one-shot mode. (T21OUT: Programmable pulse output)
		11 PPG repeat mode. (T21OUT: Programmable pulse output)
		Note) 1. This bit should be changed while T21EN bit is '0'.
11	T21ECE	Timer 21 External Clock Edge Selection.
		0 Select falling edge of external clock.
		1 Select rising edge of external clock.
8	T21OPOL	T21OUT Polarity Selection.
		0 Start high. (T21OUT is low level at disable)
		1 Start low. (T21OUT is high level at disable)
7 6	T21CPOL	Timer 21 Capture Polarity Selection.
		00 Capture on falling edge.
		01 Capture on rising edge.
		10 Capture on both falling and rising edge.
		11 Reserved.
5	T21MIEN	Timer 21 Match Interrupt Enable.
		0 Disable timer 21 match interrupt.
		1 Enable timer 21 match interrupt.
4	T21CIEN	Timer 21 Capture Interrupt Enable.
		0 Disable timer 21 capture interrupt.
		1 Enable timer 21 capture interrupt.
3	T21MIFLAG	Timer 21 Match Interrupt Flag.
		0 No request occurred.
		1 Request occurred. The bit is cleared to '0' when '1' is written.

2	T21CIFLAG	Timer 21 Capture Interrupt Flag.	
		0	No request occurred.
		1	Request occurred. The bit is cleared to ‘0’ when ‘1’ is written.
1	T21PAU	Timer 21 Counter Temporary Pause Control.	
		0	Continue counting.
		1	Temporary pause.
0	T21CLR	Timer 21 Counter and Prescaler Clear.	
		0	No effect.
		1	Clear timer 21 counter and prescaler. (Automatically cleared to ‘0’ after operation)

11.3.2 TIMER21_ADR: timer/counter 21 A data register

TIMER21_ADR register is 32-bit size and accessible in 32/16/8-bit.

TIMER21_ADR=0x4000_2604

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
ADATA			
0xFFFFFFFF			
RW			

31 0	ADATA	Timer/Counter 21 A Data. The range is 0x00000002 to 0xFFFFFFFF. **NOTE**: Do not write "0x00000000" in the TIMER21_ADR register under PPG mode.

11.3.3 TIMER21_BDR: Timer/Counter 21 B Data Register

TIMER21_BDR register is 32-bit size and accessible in 32/16/8-bit.

TIMER21_BDR=0x4000_2608

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
BDATA			
0xFFFFFFFF			
RW			

31 0	BDATA	Timer/Counter 21 B Data. The range is 0x00000000 to 0xFFFFFFFF.

11.3.4 TIMER21_CAPDR: Timer/Counter 21 Capture Data Register

TIMER21_CAPDR register is 32-bit size and accessible in 32/16/8-bit.

TIMER21_CAPDR=0x4000_260C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPD			
0x00000000			
RO			

31 0	CAPD	Timer/Counter 21 Capture Data.

11.3.5 TIMER21_PREDR: Timer/Counter 21 Prescaler Data Register

TIMER21_PREDR register is 32-bit size and accessible in 32/16/8-bit.

TIMER21_PREDR=0x4000_2610

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				PRED											
0x00000																				0xFFF											
–																				RW											

11 0	PRED	Timer/Counter 21 Prescaler Data.

11.3.6 TIMER21_CNT: Timer/Counter 21 Counter Register

TIMER21_CNT register is 32-bit size and accessible in 32/16/8-bit.

TIMER21_CNT=0x4000_2614

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT																															
0x00000000																															
RO																															

31 0	CNT	Timer/Counter 21 Counter.

11.4 Functional description

11.4.1 Timer counter 21

Timer/counter 21 can use an internal or an external clock as a clock source (EC21). A clock selection logic selects the clock source and the clock selection logic is controlled by clock selection bits (T21CLK).

- TIMER 21 clock sources are listed as followings:
  - PCLK/(TIMER21_PREDR +1)
  - EC21

In capture mode, by T21CAP, data is captured into input capture data register (TIMER21_CAPDR). Timer 21 outputs the comparison result between counter and data register through T21OUT port in Timer/counter mode. In addition, Timer 21 outputs PWM waveform through T21OUT port in PPG mode.

Table 46. Timer 21 Operating Modes

T21EN	Alternative mode	T21MS[1:0]	TIMER21_PREDR	Timer 21
1	PC_AFSR1[7:4] = 0x1	00	0xXXX	32-bit Timer/Counter Mode
1	PC_AFSR1[7:4] = 0x2	01	0xXXX	32-bit Capture Mode
1	PC_AFSR1[7:4] = 0x1	10	0xXXX	32-bit PPG Mode(one-shot mode)
1	PC_AFSR1[7:4] = 0x1	11	0xXXX	32-bit PPG Mode(repeat mode)

11.4.2 32-bit Timer/counter mode

32-bit Timer/counter mode is selected by control register as shown in Figure 55. The 32-bit timer has a counter register and a data register. The counter register is increased by internal or external clock input. Timer 21 can use an input clock with 12-bit prescaler division rates (TIMER21_PREDR) and an external Clock (EC21). When the values of TIMER21_CNT and TIMER21_ADR are the same in the timer 21, a match signal is generated and the interrupt of Timer 21 takes place. The TIMER21_CNT values are automatically cleared by match signal. It can also be cleared by software (T21CLR).

The TIMER21_CNT values are automatically cleared by match signal. It can also be cleared by software (T21CLR).

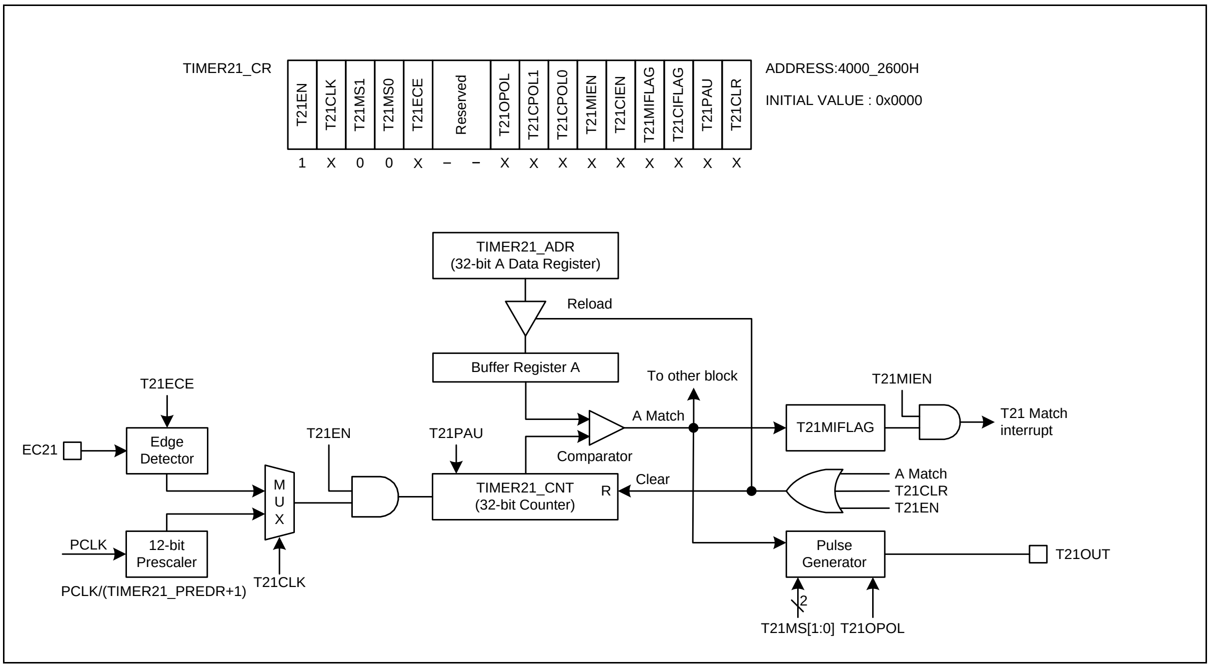


Figure 55. 32-bit Timer/Counter Mode for Timer 21

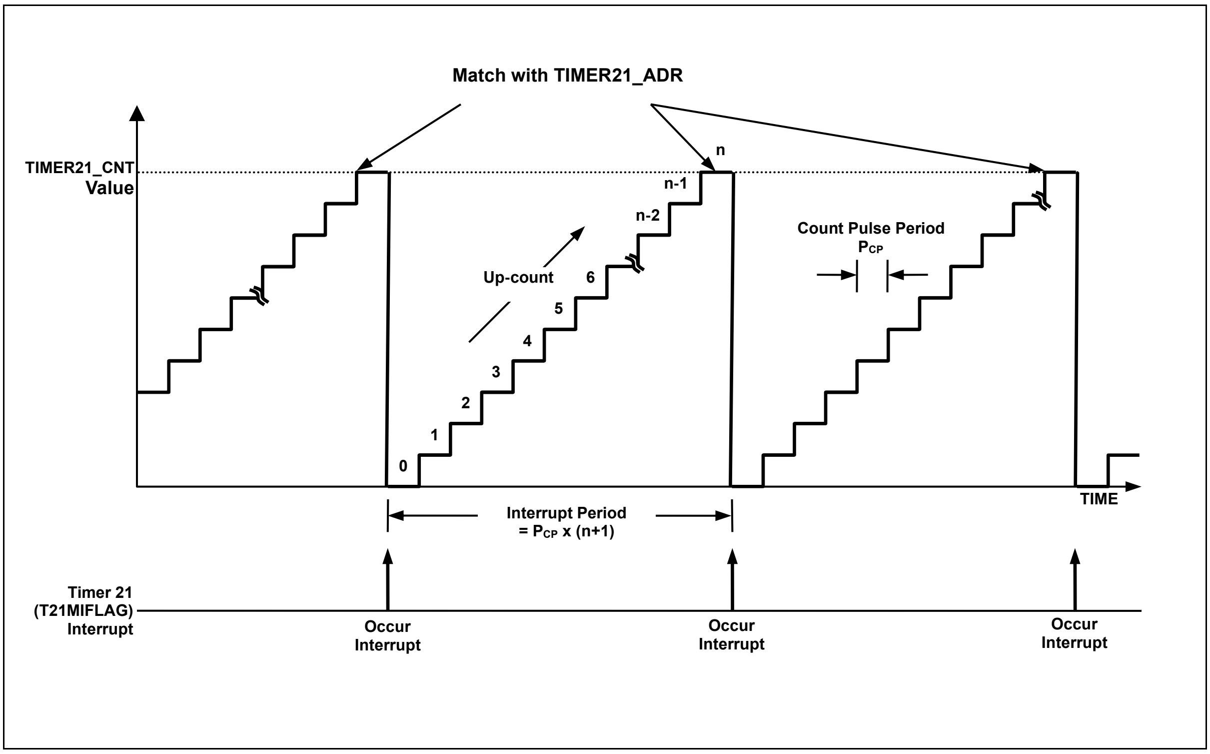


Figure 56. 32-bit Timer/Counter 21 Example

11.4.3 32-bit Capture mode

Timer 21 Capture mode is evoked by configuring T21MS[1:0] as '01'. The internal clock can be used as a clock source. It basically has the same function as the 32-bit timer/counter mode and an interrupt takes place when TIMER21_CNT becomes equal to TIMER21_ADR. TIMER21_CNT values are cleared by software (T21CLR).

This timer interrupt in Capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer. The capture result is loaded into TIMER21_CAPDR. In the timer 21 capture mode, timer 21 output (T21OUT) waveform is not available.

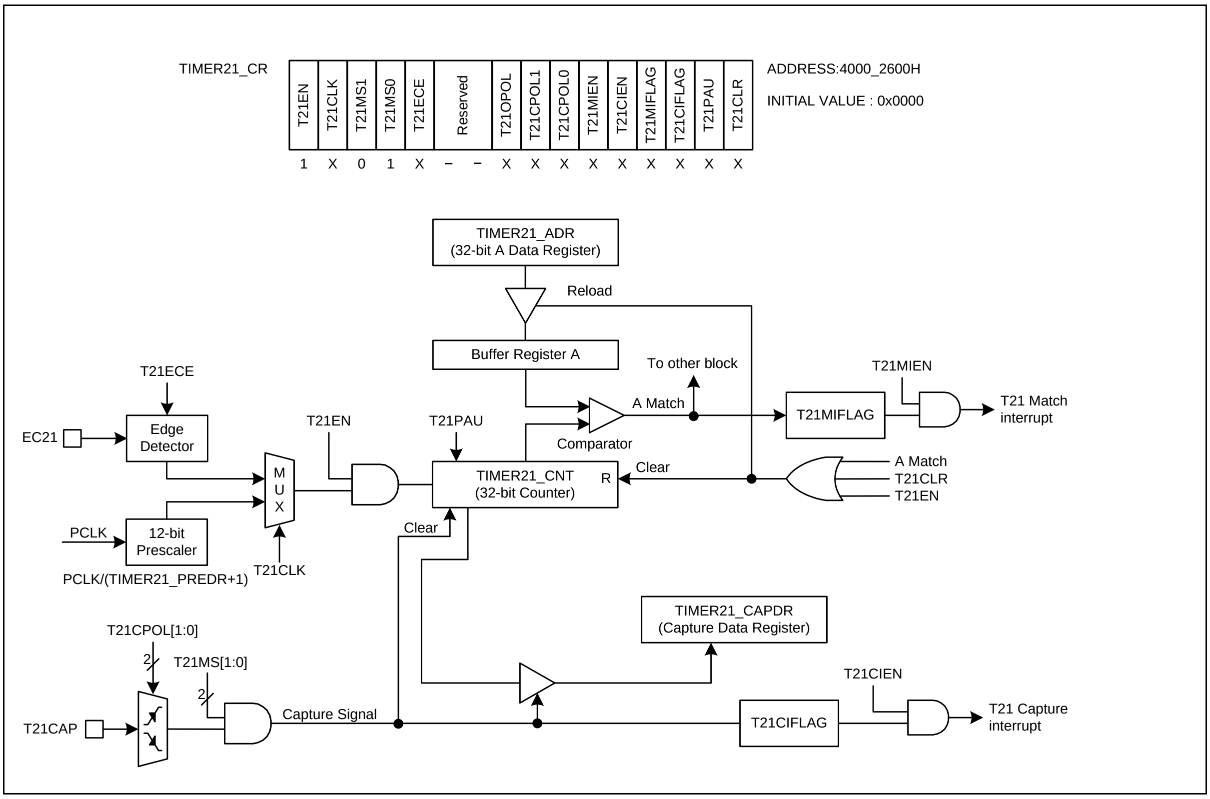


Figure 57. 32-bit Capture Mode for Timer 21

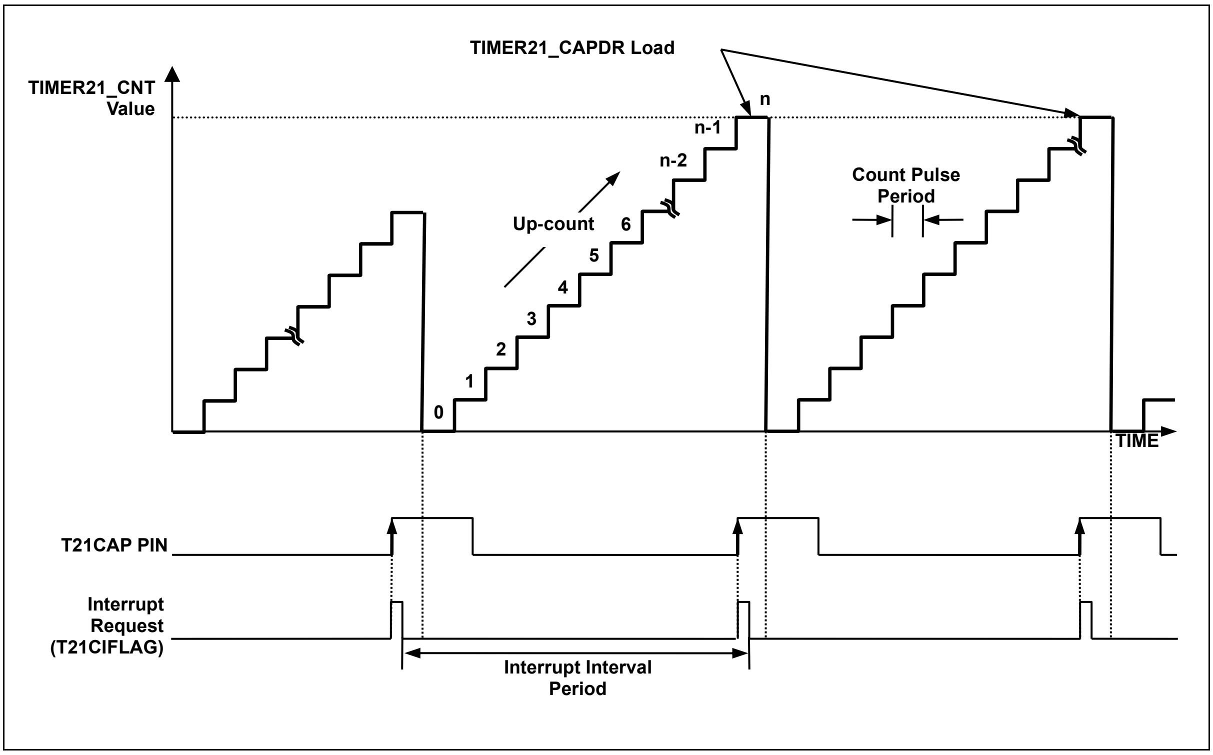


Figure 58. 32-bit Capture Mode for Timer 21

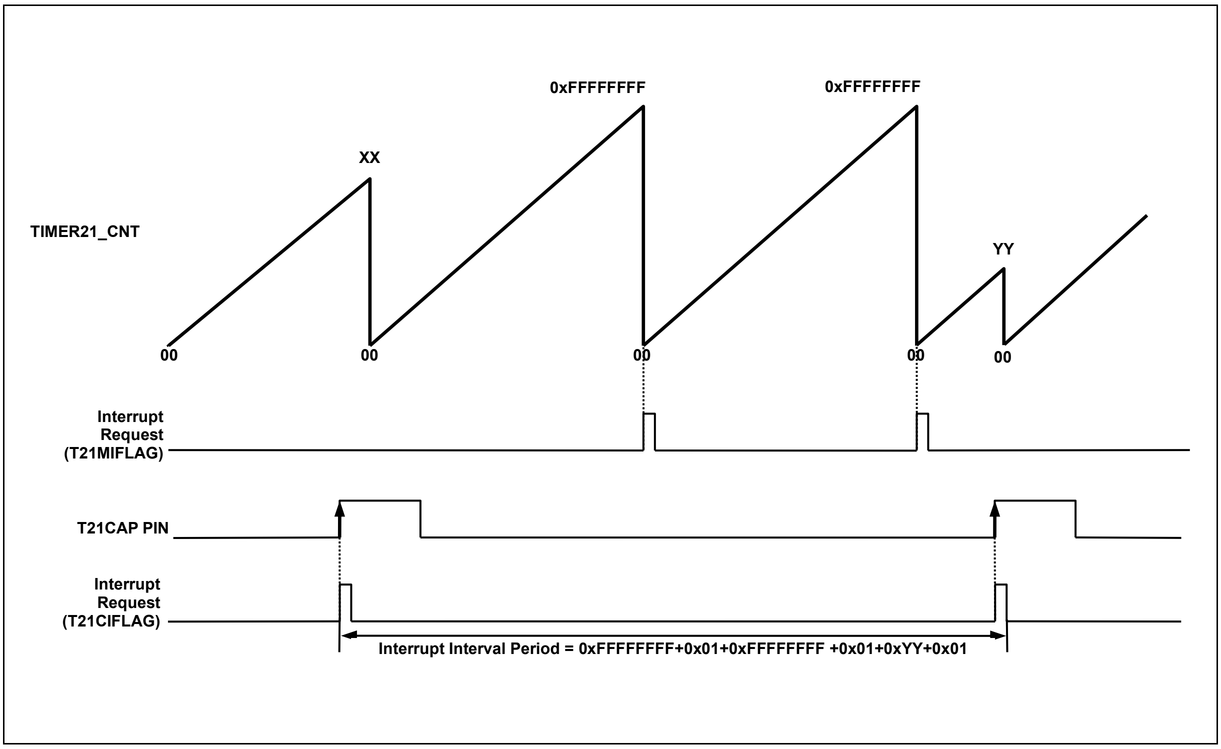
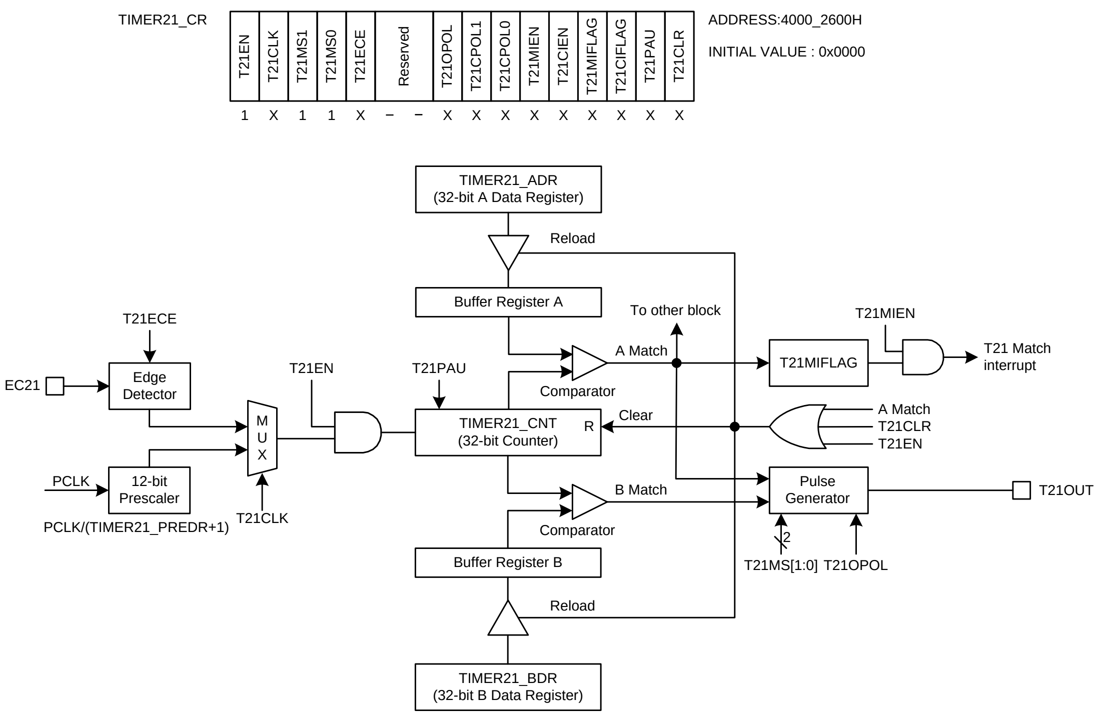


Figure 59. Express Timer Overflow in Capture Mode

11.4.4 32-bit PPG mode

Timer 21 has a PPG (Programmable Pulse Generation) function. In PPG mode, the T21OUT pin generates PWM output of up to 32-bit resolution. This pin should be configured as a PWM output by setting PC_AFSR1[7:4] to 'AF1'. The period of PWM output is determined by the TIMER21_ADR. The duty of PWM output is determined by TIMER21_BDR.



NOTE: The T21EN is automatically cleared to logic '0' after one pulse is generated in PPG one-shot mode.

Figure 60. 32-bit PPG Repeat and One-shot Mode for Timer 21

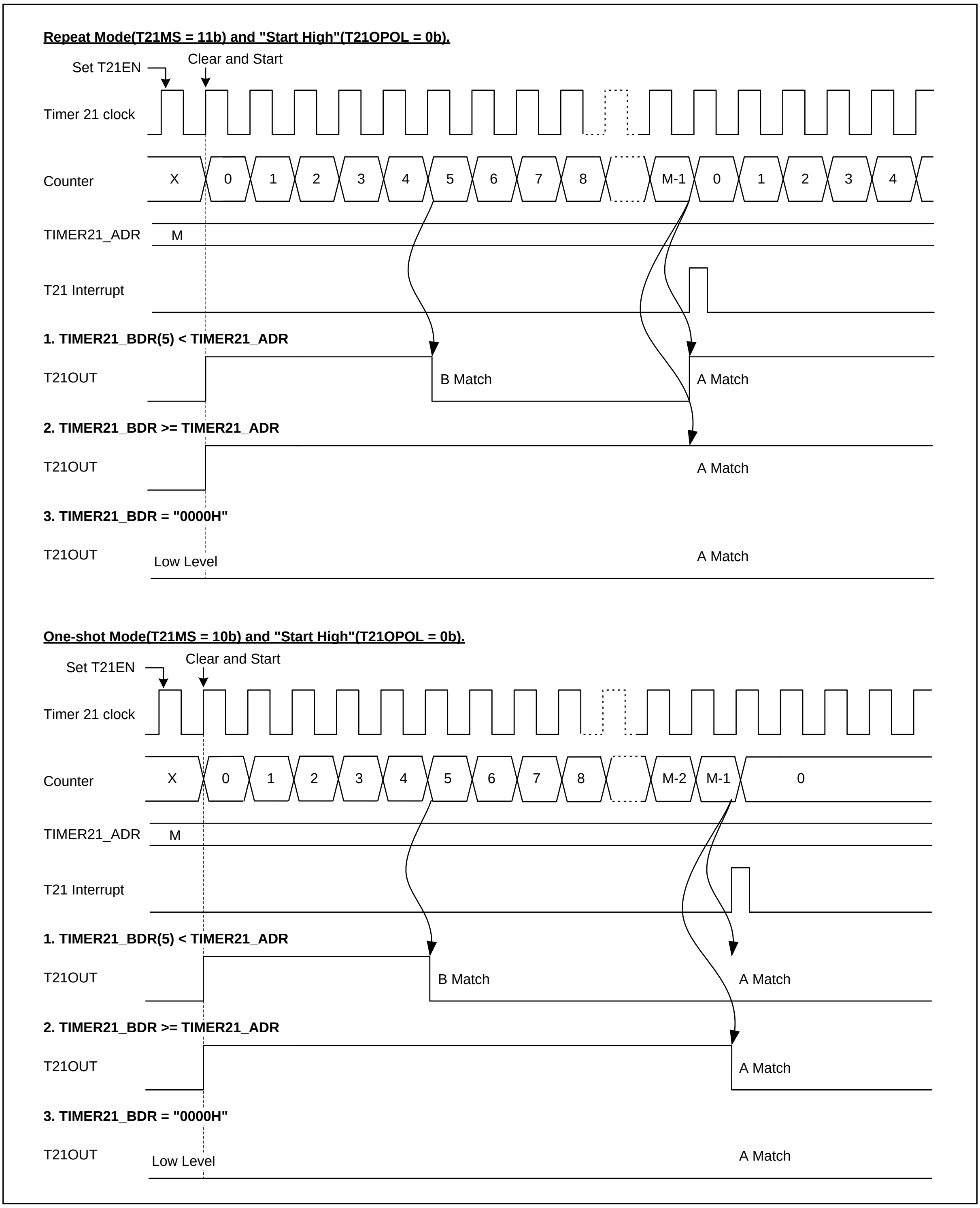


Figure 61. 32-bit PPG Mode Timing chart for Timer 21

12 Timer counter 30

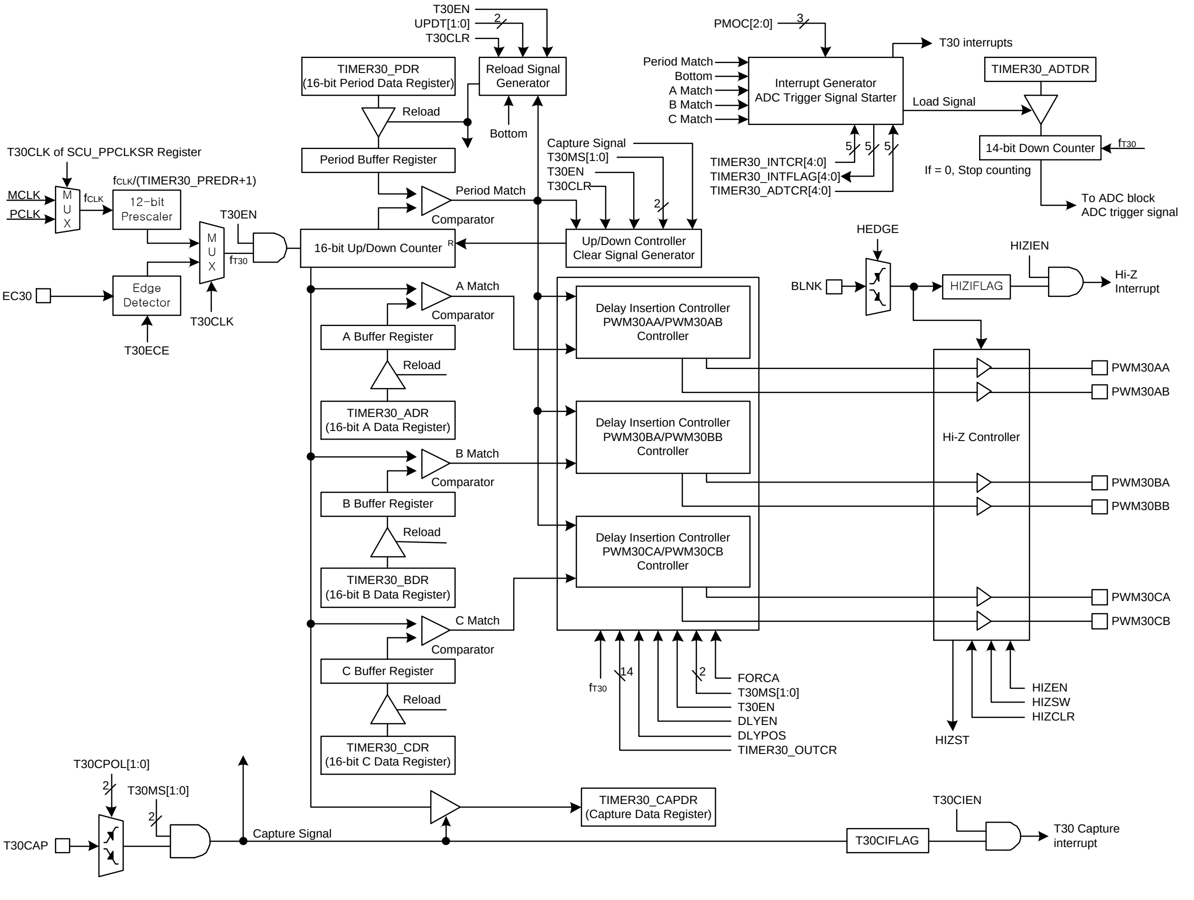
A timer counter 30 is a 16-bit timer with 3-phase PWM function. It has ADC triggering feature for motor control.

The Timer counter 30 features the followings:

- 16-bit up/down-counter and 12-bit prescaler
- Periodic timer, Back-to-Back timer, and Capture mode

12.1 Timer counter 30 block diagram

Figure 62 shows the block diagram of a timer block unit.



NOTES:

1. The Period/A/B/C match interrupts, except Bottom, can occur in the interval mode.
2. The Period match interrupt can occur in capture mode.
3. The 16-bit up/down counter in capture mode is cleared to “0x0000” after the counter value is loaded to the TIMER30_CAPDR register at valid edge.
4. The HIZSW (high-impedance output software setting) bit can be used for debugging mode. That is, all T30PWM outputs can be high-impedance state by setting the HIZSW bit to ‘1’ through debugger UI.
5. After the T30EN bit is set, counting of TIMER30_CNT may be delayed by 2 clocks or more.

Figure 62. Timer Counter 30 Block Diagram

12.2 Pin description for Timer counter 30

Table 47. Pins and External Signals for Timer Counter 30

PIN NAME	TYPE	DESCRIPTION
EC30	I	External clock input
T30CAP	I	Capture input
PWM30AA	O	PWM output
PWM30AB	O	PWM output
PWM30BA	O	PWM output
PWM30BB	O	PWM output
PWM30CA	O	PWM output
PWM30CB	O	PWM output

12.3 Registers

Base address and register map of the Timer 30 are shown in Table 48 and Table 49.

Table 48. Base Address of Timer 30

Name	Base address
TIMER30	0x4000_2400

Table 49. Timer Register Map

Name	Offset	Type	Description	Reset value
TIMER30_CR	0x0000	RW	Timer/Counter 30 Control Register	0x00000000
TIMER30_PDR	0x0004	RW	Timer/Counter 30 Period Data Register	0x0000FFFF
TIMER30_ADR	0x0008	RW	Timer/Counter 30 A Data Register	0x0000FFFF
TIMER30_BDR	0x000C	RW	Timer/Counter 30 B Data Register	0x0000FFFF
TIMER30_CDR	0x0010	RW	Timer/Counter 30 C Data Register	0x0000FFFF
TIMER30_CAPDR	0x0014	RO	Timer/Counter 30 Capture Data Register	0x00000000
TIMER30_PREDR	0x0018	RW	Timer/Counter 30 Prescaler Data Register	0x00000FFF
TIMER30_CNT	0x001C	RO	Timer/Counter 30 Counter Register	0x00000000
TIMER30_OUTCR	0x0020	RW	Timer/Counter 30 Output Control Register	0x00000000
TIMER30_DLY	0x0024	RW	Timer/Counter 30 PWM Output Delay Data Register	0x00000000
TIMER30_INTCR	0x0028	RW	Timer/Counter 30 Interrupt Control Register	0x00000000
TIMER30_INTFLAG	0x002C	RW	Timer/Counter 30 Interrupt Flag Register	0x00000000
TIMER30_HIZCR	0x0030	RW	Timer/Counter 30 High-Impedance Control Register	0x00000000
TIMER30_ADTCR	0x0034	RW	Timer/Counter 30 ADC Trigger Control Register	0x00000000
TIMER30_ADTDR	0x0038	RW	Timer/Counter 30 ADC Trigger Generator Data Register	0x00000000

12.3.1 TIMER30_CR: timer/counter 30 control register

Timer module should be configured properly before running. Once target purpose is defined, the timer can be configured in the TIMER30_CR register. After configuring this register, a user can start or stop the timer function by using this register.

TIMER30_CR register is 32-bit size and accessible in 32/16/8-bit.

TIMER30_CR=0x4000_2400

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15	14	13 12	11	10	9	8	7 6	5 4	3 2 1	0
Reserved	**T30EN**	**T30CLK**	**T30MS**	**T30ECE**	**FORCA**	**DLYEN**	**DLYPOS**	**T30CPOL**	**UPDT**	**PMOC**	**T30CLR**
0x0000	**0**	**0**	**00**	**0**	**0**	**0**	**0**	**00**	**00**	**000**	**0**
-	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**

15	T30EN	Timer 30 Operation Enable.	
		0	Disable timer 30 operation.
		1	Enable timer 30 operation. (Counter clear and start)
14	T30CLK	Timer 30 Clock Selection.	
		0	Select an internal prescaler clock.
		1	Select an external clock.
		NOTE:	This bit should be changed while T30EN bit is '0'.
13 12	T30MS	Timer 30 Operation Mode Selection.	
		00	Interval mode. (All match interrupts can occur)
		01	Capture mode. (The Period-match interrupt can occur)
		10	Back-to-back mode. (All interrupts can occur)
		11	Not used.
		NOTE:	This bit should be changed while T30EN bit is '0'.
11	T30ECE	Timer 30 External Clock Edge Selection.	
		0	Select falling edge of external clock.
		1	Select rising edge of external clock.
10	FORCA	Timer 30 Output Mode Selection. This bit should be changed while T30EN is '0'.	
		0	6-Channel mode (The PWM30xA/PWM30xB pins are outputs according to the TIMER30_xDR registers, respectively)
		1	Force A-Channel mode (All PWM30xA/PWM30xB pins are outputs according only to the TIMER30_ADR register)
9	DLYEN	Delay Time Insertion Enable.	
		0	Disable delay time insertion to the PWM30xA/PWM30xB.
		1	Enable delay time insertion to the PWM30xA/PWM30xB.
8	DLYPOS	Delay Time Insertion Position.	
		0	Insert in front of PWM30xA and behind PWM30xB pins.
		1	Insert behind PWM30xA and in front of PWM30xB pins.
7 6	T30CPOL	Timer 30 Capture Polarity Selection.	
		00	Capture on falling edge.
		01	Capture on rising edge.
		10	Capture on both falling and rising edge.
		11	Reserved

5 4	UPDT	Data Reload Time Selection.	
		00	Update data to buffer at the time of writing.
		01	Update data to buffer at period match.
		10	Update data to buffer at bottom.
		11	Not used.
3 1	PMOC	Period Match Interrupt Occurrence Selection.	
		000	Once every period match.
		001	Once every 2 period match.
		010	Once every 3 period match.
		011	Once every 4 period match.
		100	Once every 5 period match.
		101	Once every 6 period match.
		110	Once every 7 period match.
		111	Once every 8 period match.
		NOTE: A period match counter will be cleared to 0x00 when the T3nCLR bit is set.	
0	T30CLR	Timer 30 Counter and Prescaler Clear.	
		0	No effect.
		1	Clear timer 30 counter and prescaler (Automatically cleared to '0' after operation)

12.3.2 TIMER30_PDR: timer/counter 30 Period data register

TIMER30_PDR register is 32-bit size and accessible in 32/16/8-bit.

TIMER30_PDR=0x4000_2404

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">Reserved</td><td colspan="16">PDATA</td></tr>
<tr><td colspan="16">0x0000</td><td colspan="16">0xFFFF</td></tr>
<tr><td colspan="16">–</td><td colspan="16">RW</td></tr>
</table>

15 0	PDATA	Timer/Counter 30 Period Data. The range is 0x0002 to 0xFFFF.

12.3.3 TIMER30_ADR: timer/counter 30 A data register

TIMER30_ADR register is 32-bit size and accessible in 32/16/8-bit.

TIMER30_ADR=0x4000_2408

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">Reservd</td><td colspan="16">ADATA</td></tr>
<tr><td colspan="16">0x0000</td><td colspan="16">0xFFFF</td></tr>
<tr><td colspan="16">-</td><td colspan="16">RW</td></tr>
</table>

15 0	ADATA	Timer/Counter 30 A Data. The range is 0x0000 to 0xFFFF.

12.3.4 TIMER30_BDR: Timer/Counter 30 B Data Register

TIMER30_BDR register is 32-bit size and accessible in 32/16/8-bit.

TIMER30_BDR=0x4000_240C

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">Reservd</td><td colspan="16">BDATA</td></tr>
<tr><td colspan="16">0x0000</td><td colspan="16">0xFFFF</td></tr>
<tr><td colspan="16">-</td><td colspan="16">RW</td></tr>
</table>

15 0	BDATA	Timer/Counter 30 B Data. The range is 0x0000 to 0xFFFF.

12.3.5 TIMER30_CDR: Timer/Counter 30 C Data Register

TIMER30_CDR register is 32-bit size and accessible in 32/16/8-bit.

TIMER30_CDR=0x4000_2410

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="16">Reservd</td><td colspan="16">CDATA</td></tr>
<tr><td colspan="16">0x0000</td><td colspan="16">0xFFFF</td></tr>
<tr><td colspan="16">-</td><td colspan="16">RW</td></tr>
</table>

15 0	CDATA	Timer/Counter 30 C Data. The range is 0x0000 to 0xFFFF.

12.3.6 TIMER30_CAPDR: Timer/Counter 30 Capture Data Register

TIMER30_CAPDR register is 32-bit size and accessible in 32/16/8-bit.

TIMER30_CAPDR=0x4000_2414

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="16">Reservd</td><td colspan="16">CAPD</td></tr>
<tr><td colspan="16">0x0000</td><td colspan="16">0x0000</td></tr>
<tr><td colspan="16">-</td><td colspan="16">RO</td></tr>
</table>

15 0	CAPD	Timer/Counter 30 Capture Data.

12.3.7 TIMER30_PREDR: Timer/Counter 30 Prescaler Data Register

TIMER30_PREDR register is 32-bit size and accessible in 32/16/8-bit.

TIMER30_PREDR=0x4000_2418

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="20">Reserved</td><td colspan="12">PRED</td></tr>
<tr><td colspan="20">0x00000</td><td colspan="12">0xFFF</td></tr>
<tr><td colspan="20">–</td><td colspan="12">RW</td></tr>
</table>

11 0	PRED	Timer/Counter 30 Prescaler Data.

12.3.8 TIMER30_CNT: Timer/Counter 30 Counter Register

TIMER30_CNT register is 32-bit size and accessible in 32/16/8-bit.

TIMER30_CNT=0x4000_241C

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Reservd	**CNT**
0x0000	**0x0000**
-	**RO**

15 0	CNT	Timer/Counter 30 Counter.

12.3.9 TIMER30_OUTCR: Timer/Counter 30 Output Control Register

TIMER30_OUTCR register is 32-bit size and accessible in 32/16/8-bit.

TIMER30_OUTCR=0x4000_2420

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">WTIDKY</td><td>POLB</td><td>POLA</td><td>PABOE</td><td>PBBOE</td><td>PCBOE</td><td>PAAOE</td><td>PBAOE</td><td>PCAOE</td><td>Reserved</td><td>LVLAB</td><td>LVLBB</td><td>LVLCB</td><td>Reserved</td><td>LVLAA</td><td>LVLBA</td><td>LVLCA</td></tr>
<tr><td colspan="16">0x0000</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="16">WO</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>-</td><td>RW</td><td>RW</td><td>RW</td><td>-</td><td>RW</td><td>RW</td><td>RW</td></tr>
</table>

31	WTIDKY	Write Identification Key.	
16		When writing, write 0xE06C to these bits, or else writing is ignored.	
15	POLB	PWM30xB Output Polarity Selection. (x : A, B and C)	
		0	Low level start. (The PWM30xB pins are started with low level after counting)
		1	High level start. (The PWM30xB pins are started with high level after counting)
14	POLA	PWM30xA Output Polarity Selection. (x : A, B and C)	
		0	Low level start. (The PWM30xA pins are started with low level after counting)
		1	High level start. (The PWM30xA pins are started with high level after counting)
13	PABOE	PWM30AB Output Enable.	
		0	Disable output.
		1	Enable output.
12	PBBOE	PWM30BB Output Enable.	
		0	Disable output.
		1	Enable output.
11	PCBOE	PWM30CB Output Enable.	
		0	Disable output.
		1	Enable output.
10	PAAOE	PWM30AA Output Enable.	
		0	Disable output.
		1	Enable output.
9	PBAOE	PWM30BA Output Enable.	
		0	Disable output.
		1	Enable output.
8	PCAOE	PWM30CA Output Enable.	
		0	Disable output.
		1	Enable output.
6	LVLAB	Configure PWM30AB output When Disable.	
		0	Low level
		1	High level
5	LVLBB	Configure PWM30BB output When Disable.	
		0	Low level
		1	High level
4	LVLCB	Configure PWM30CB output When Disable.	
		0	Low level
		1	High level

2	LVLAA	Configure PWM30AA output When Disable.	
		0	Low level
		1	High level
1	LVLBA	Configure PWM30BA output When Disable.	
		0	Low level
		1	High level
0	LVLCA	Configure PWM30CA output When Disable.	
		0	Low level
		1	High level

12.3.10 TIMER30_DLY: Timer/Counter 30 PWM Output Delay Data Register

TIMER30_DLY register is 32-bit size and accessible in 32/16/8-bit.

TIMER30_DLY=0x4000_2424

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="22">Reservd</td><td colspan="10">DLY</td></tr>
<tr><td colspan="22">0x00000</td><td colspan="10">0x000</td></tr>
<tr><td colspan="22">–</td><td colspan="10">RW</td></tr>
</table>

9 0	DLY	Timer/Counter 30 PWM Delay Data. Delay time: (DLY[9:0]+1)÷fT30

12.3.11 TIMER30_INTCR: Timer/Counter 30 Interrupt Control Register

TIMER30_INTCR register is 32-bit size and accessible in 32/16/8-bit.

TIMER30_INTCR=0x4000_2428

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																									**HIZIEN**	**T30CIEN**	**T30BTIEN**	**T30PMIEN**	**T30AMIEN**	**T30BMIEN**	**T30CMIEN**
0x000000																									**0**	**0**	**0**	**0**	**0**	**0**	**0**
–																									**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**

6	HIZIEN	Timer 30 Output High-Impedance Interrupt Enable.
		0 Disable timer 30 output high-impedance interrupt.
		1 Enable timer 30 output high-impedance interrupt.
5	T30CIEN	Timer 30 Capture Interrupt Enable.
		0 Disable timer 30 capture interrupt.
		1 Enable timer 30 capture interrupt.
4	T30BTIEN	Timer 30 Bottom Interrupt Enable.
		0 Disable timer 30 bottom interrupt.
		1 Enable timer 30 bottom interrupt.
3	T30PMIEN	Timer 30 Period Match Interrupt Enable.
		0 Disable timer 30 period interrupt.
		1 Enable timer 30 period interrupt.
2	T30AMIEN	Timer 30 A-ch Match Interrupt Enable.
		0 Disable timer 30 A-ch match interrupt.
		1 Enable timer 30 A-ch match interrupt.
1	T30BMIEN	Timer 30 B-ch Match Interrupt Enable.
		0 Disable timer 30 B-ch match interrupt.
		1 Enable timer 30 B-ch match interrupt.
0	T30CMIEN	Timer 30 C-ch Match Interrupt Enable.
		0 Disable timer 30 C-ch match interrupt.
		1 Enable timer 30 C-ch match interrupt.

12.3.12 TIMER30_INTFLAG: Timer/Counter 30 Interrupt Flag Register

TIMER30_INTFLAG register is 32-bit size and accessible in 32/16/8-bit.

TIMER30_INTFLAG=0x4000_242C

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7	6	5	4	3	2	1	0
Reserved	**HIZIFLAG**	**T30CIFLAG**	**T30BTIFLAG**	**T30PMIFLAG**	**T30AMIFLAG**	**T30BMIFLAG**	**T30CMIFLAG**
0x000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**
-	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**

6	HIZIFLAG	Timer 30 Output High-Impedance Interrupt Flag.	
		0	No request occurred.
		1	Request occurred. The bit will be cleared to '0' when '1' is written to this bit.
5	T30CIFLAG	Timer 30 Capture Interrupt Flag.	
		0	No request occurred.
		1	Request occurred. The bit will be cleared to '0' when '1' is written to this bit.
4	T30BTIFLAG	Timer 30 Bottom Interrupt Flag.	
		0	No request occurred.
		1	Request occurred. The bit will be cleared to '0' when '1' is written to this bit.
3	T30PMIFLAG	Timer 30 Period Match Flag Enable.	
		0	No request occurred.
		1	Request occurred. The bit will be cleared to '0' when '1' is written to this bit.
2	T30AMIFLAG	Timer 30 A-ch Match Interrupt Flag.	
		0	No request occurred.
		1	Request occurred. The bit will be cleared to '0' when '1' is written to this bit.
1	T30BMIFLAG	Timer 30 B-ch Match Interrupt Flag.	
		0	No request occurred.
		1	Request occurred. The bit will be cleared to '0' when '1' is written to this bit.
0	T30CMIFLAG	Timer 30 C-ch Match Interrupt Flag.	
		0	No request occurred.
		1	Request occurred. The bit will be cleared to '0' when '1' is written to this bit.

12.3.13 TIMER30_HIZCR: Timer/Counter 30 High-Impedance Control Register

TIMER30_HIZCR register is 32-bit size and accessible in 32/16/8-bit.

TIMER30_HIZCR=0x4000_2430

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="24">Reserved</td><td>HIZEN</td><td colspan="2">Reserved</td><td>HIZSW</td><td>Reserved</td><td>HEDGE</td><td>HIZSTA</td><td>HIZCLR</td></tr>
<tr><td colspan="24">0x000000</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="24">–</td><td>RW</td><td colspan="2">-</td><td>RW</td><td>-</td><td>RW</td><td>RO</td><td>RW</td></tr>
</table>

7	HIZEN	PWM30xA/PWM30xB Output High-Impedance Enable.	
		0	Disable to control the output high-impedance.
		1	Enable to control the output high-impedance.
4	HIZSW	High-Impedance Output Software Setting.	
		0	No effect.
		1	PWM30xA/PWM30xB pins go into high impedance. (Automatically cleared to '0' after operation)
2	HEDGE	High-Impedance Edge Selection.	
		0	Falling edge of the BLNK pin.
		1	Rising edge of the BLNK pin.
1	HIZSTA	High-Impedance Status.	
		0	Indicates that the pins are not under a Hi-Z state.
		1	Indicates that the pins are under a Hi-Z state.
0	HIZCLR	High-Impedance Output Clear.	
		0	No effect.
		1	Clear high-impedance output. (The PWM30xA/PWM30xB pins returns as output and this bit is automatically cleared to '0' after operation)

NOTE: Where x = A, B, and C.

12.3.14 TIMER30_ADTCR: Timer/Counter 30 ADC Trigger Control Register

TIMER30_ADTCR register is 32-bit size and accessible in 32/16/8-bit.

TIMER30_ADTCR=0x4000_2434

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5	4	3	2	1	0
Reserved	**T30BTTG**	**T30PMTG**	**T30AMTG**	**T30BMTG**	**T30CMTG**
0x000000	**0**	**0**	**0**	**0**	**0**
–	**RW**	**RW**	**RW**	**RW**	**RW**

4	T30BTTG	Select Timer 30 Bottom for ADC Trigger Signal Generator.	
		0	Disable ADC trigger signal generator by bottom.
		1	Enable ADC trigger signal generator by bottom.
3	T30PMTG	Select Timer 30 Period Match for ADC Trigger Signal Generator.	
		0	Disable ADC trigger signal generator by period match.
		1	Enable ADC trigger signal generator by period match.
2	T30AMTG	Select Timer 30 A-ch Match for ADC Trigger Signal Generator.	
		0	Disable ADC trigger signal generator by A-ch match.
		1	Enable ADC trigger signal generator by A-ch match.
1	T30BMTG	Select Timer 30 B-ch Match for ADC Trigger Signal Generator.	
		0	Disable ADC trigger signal generator by B-ch match.
		1	Enable ADC trigger signal generator by B-ch match.
0	T30CMTG	Select Timer 30 C-ch Match for ADC Trigger Signal Generator.	
		0	Disable ADC trigger signal generator by C-ch match.
		1	Enable ADC trigger signal generator by C-ch match.

NOTES:

1. A trigger signal generation is not related to the PMOC[2:0] bits of TIMER30_CR register.
2. If several sources for trigger are selected, a signal can be lost in case the trigger generation counter is reloaded by another signal.

12.3.15 TIMER30_ADTDR: Timer/Counter 30 ADC Trigger Generator Data Register

TIMER30_ADTDR register is 32-bit size and accessible in 32/16/8-bit.

TIMER30_ADTDR=0x4000_2438

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14	13 12 11 10 9 8 7 6 5 4 3 2 1 0
Reservd	**ADTDATA**
0x0000	**0x0000**
-	**RW**

13 0	ADTDATA	Timer/Counter 30 ADC Trigger Generation Data. Trigger time: (ADTDATA[13:0]+2)÷fT30

12.4 Functional description

12.4.1 Timer counter 30

Timer/counter 30 can use an internal or an external clock as a clock source (EC30). A clock selection logic selects the clock source and the clock selection logic is controlled by clock selection bits (T30CLK).

- TIMER 30 clock sources are listed as followings:
  - PCLK/(TIMER30_PREDR +1)
  - MCLK/(TIMER30_PREDR +1)
  - EC30

In capture mode, by T30CAP, data is captured into input capture data register (TIMER30_CAPDR). The PWM waveform to PWM30AA, PWM30AB, PWM30BA, PWM30BB, PWM30CA, PWM3CB Port(6-channel).

Table 50. Timer 30 Operating Modes

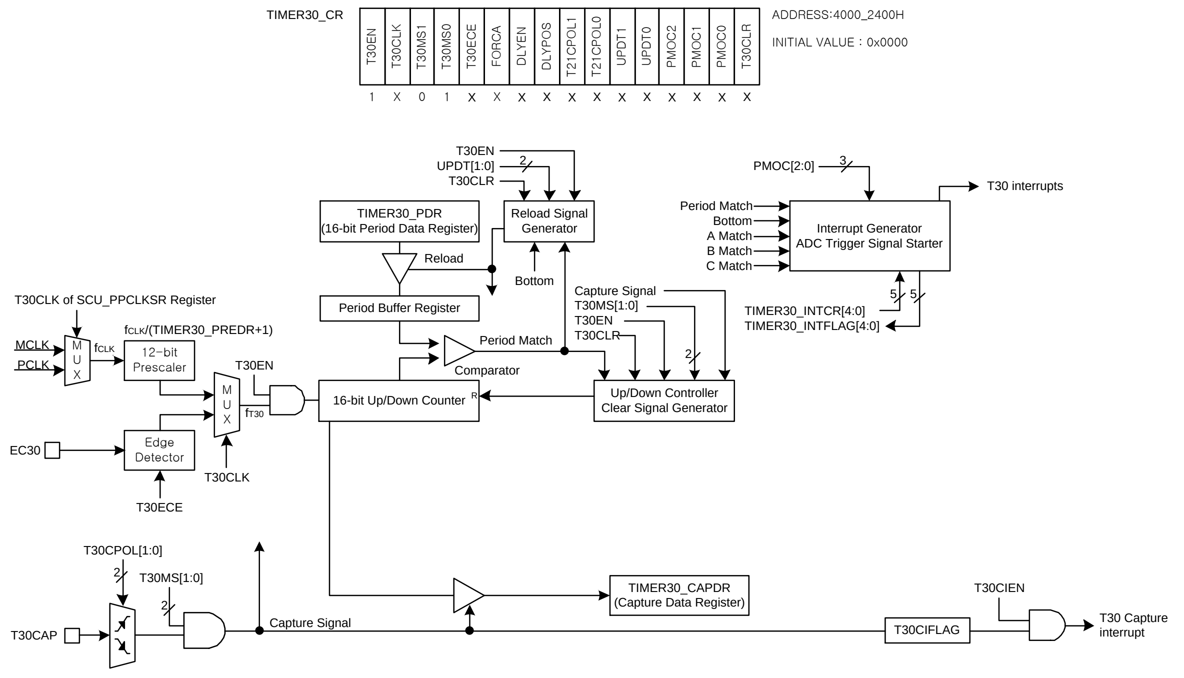
T30EN	T30MS[1:0]	TIMER30_PREDR	Timer 30
1	00	0xXXX	16-bit Timer/Counter Mode
1	01	0xXXX	16-bit Capture Mode
1	10	0xXXX	16-bit back-to-back Mode

12.4.2 Timer 30 capture mode

16-bit timer 30 capture mode is set by T30MS[1:0] as ‘01’. The clock source can use the internal or external clock input. It basically has the same function as the 16-bit interval mode and an interrupt takes place when T30 16-bit up/down counter is equal to TIMER30_PDR. The T30 16-bit up/down counter values are automatically cleared by match signal. It can also be cleared by software (T30CLR).

This timer interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of timer.

The capture result is loaded into TIMER30_CAPDR.



NOTES:

1. The Period match only can occur in capture mode.
2. The 16-bit up/down counter in capture mode is cleared to “0x0000” after the counter value is loaded to the TIMER30_CAPDR register at valid edge.

Figure 63. 16-bit Capture Mode for Timer 30

12.4.3 Timer 30 interval mode

Interval mode is set by T30MS[1:0] as ‘00’. The timer 30 has a counter and a data register. The 16-bit up/down counter is increased by internal or external clock input. The timer 30 can use an input clock with 12-bit prescaler division rates (TIMER30_PREDR[11:0]). When the value of T30 16-bit up/down counter and the value of TIMER30_PDR are identical in timer 30, a match signal is generated and the period match interrupt of timer 30 is occurred. The period match interrupt can take place at every 1, 2, 3, 4, 5, 6, 7, or 8 period match (PMOC[2:0]). The 16-bit up/down counter value is automatically cleared by match signal. It can also be cleared by software (T30CLR).

The timer 30 Interval mode can be used for BLDC motor control. It has 6-channel pins that generate PWM outputs up to 16-bit resolution. When the value of 16-bit up/down counter and TIMER30_PDR are identical in timer 30, a period match signal is generated and the period match interrupt of timer 30 takes place. The timer 30 A, B, and C match signals are generated and the A, B, and C match interrupts of timer 30 take place, when the 16-bit counter value are identical to the value of TIMER30_xDR. The period and duty of the PWM output is determined by the TIMER30_PDR (PWM period register), and TIMER30_xDR (each channel PWM duty register).

PWM Period = [TIMER30_PDR] X Source Clock

PWM Duty(A-ch) = [TIMER30_ADR] X Source Clock

PWM Duty(B-ch) = [TIMER30_BDR] X Source Clock

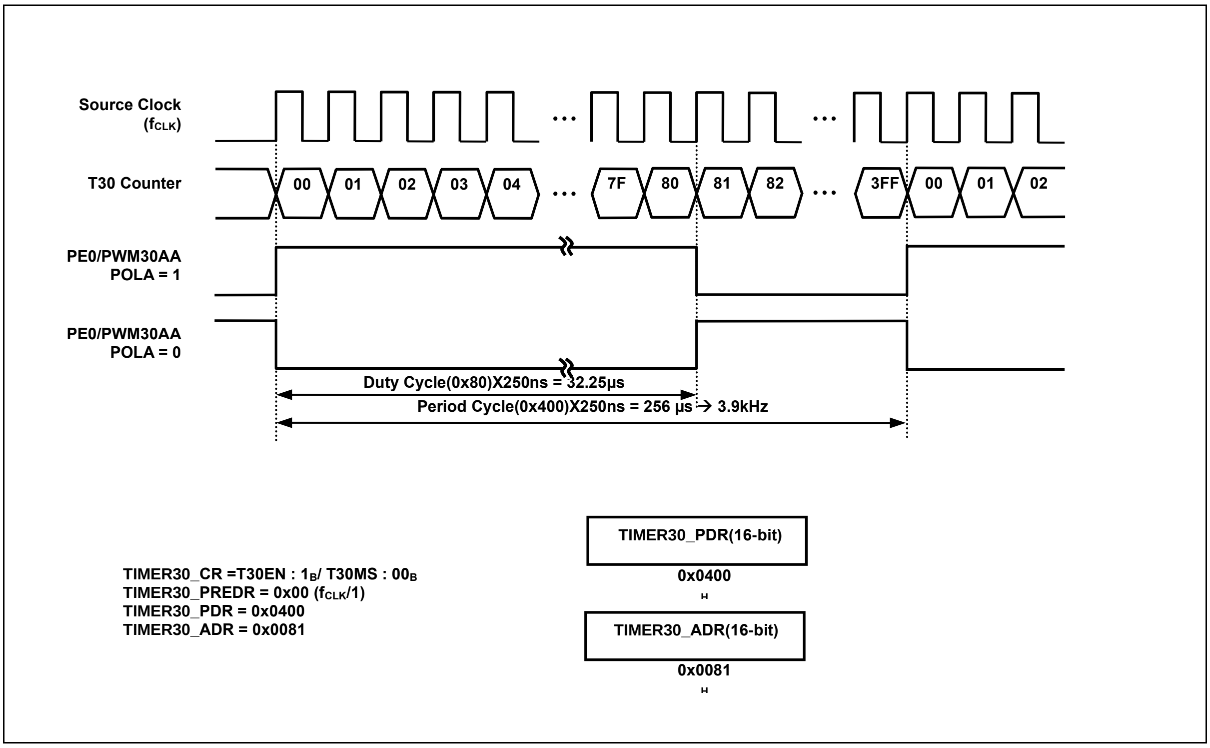
PWM Duty(C-ch) = [TIMER30_CDR] X Source Clock

The POLA/POLB bit of TIMER30_OUTCR register decides the polarity of PWM output. If the POLA/POLB bit is set to ‘1’, the PWM30xA/PWM30xB output is high level start and if the POLA/POLB bit is cleared to ‘0’, the PWM30xA/PWM30xB output is low level start, respectively.

Table 51. PWM Channel Polarity

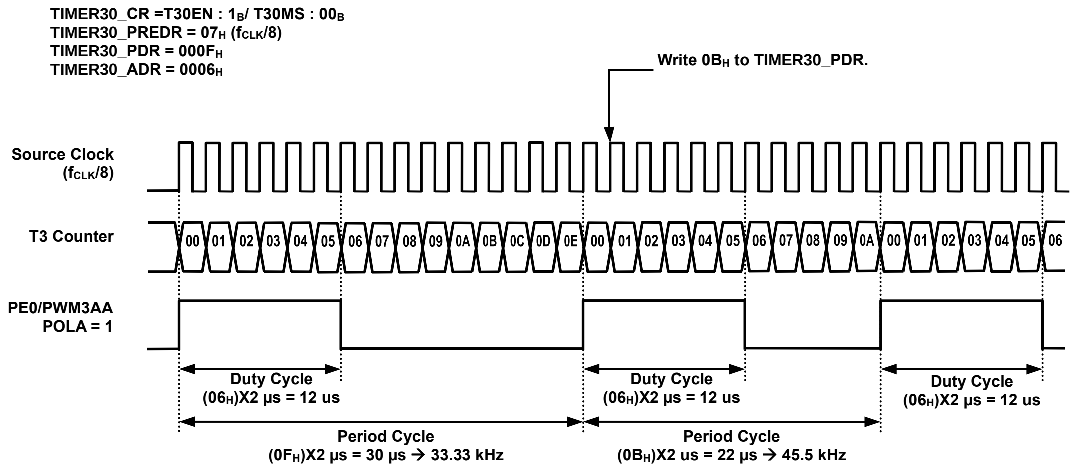
PxAOE	PxBOE	POLA	POLB	PWM3xA Pin Output	PWM3xB Pin Output
1	1	0	0	Low level start	Low level start
		0	1	Low level start	High level start
		1	0	High level start	Low level start
		1	1	High level start	High level start

NOTE: Where x = A, B, and C.



TIMER30_CR =T30EN : 1_B/ T30MS : 00_B
TIMER30_PREDR = 0x00 (f_{CLK}/1)
TIMER30_PDR = 0x0400
TIMER30_ADR = 0x0081

Figure 64. Example of PWM at 4 MHz



NOTE: The example shows when data reload time is chosen as the time of writing mode (UPDT[1:0] = "00").

Figure 65. Example of Changing the Period in Absolute Duty Cycle at 4 MHz

12.4.3.1 Data reload time selection

Data reload time can be selected from "update data to buffer at the time of writing", "update data to buffer at period match", or "update data to buffer at bottom".

12.4.3.2 PWM output delay

Using the DLYEN bit, DLYPOS bit, and TIMER30_DLY register can delay the PWM output. When DLYPOS is set to '0', the delay inserts in front of PWM30xA and behind PWM30xB pins. When DLYPOS is set to '1', the delay inserts behind PWM30xA and in front of PWM30xB pins. The settings of DLYEN bit, DLYPOS bit, and TIMER30_DLY register apply identically to all PWM channels.

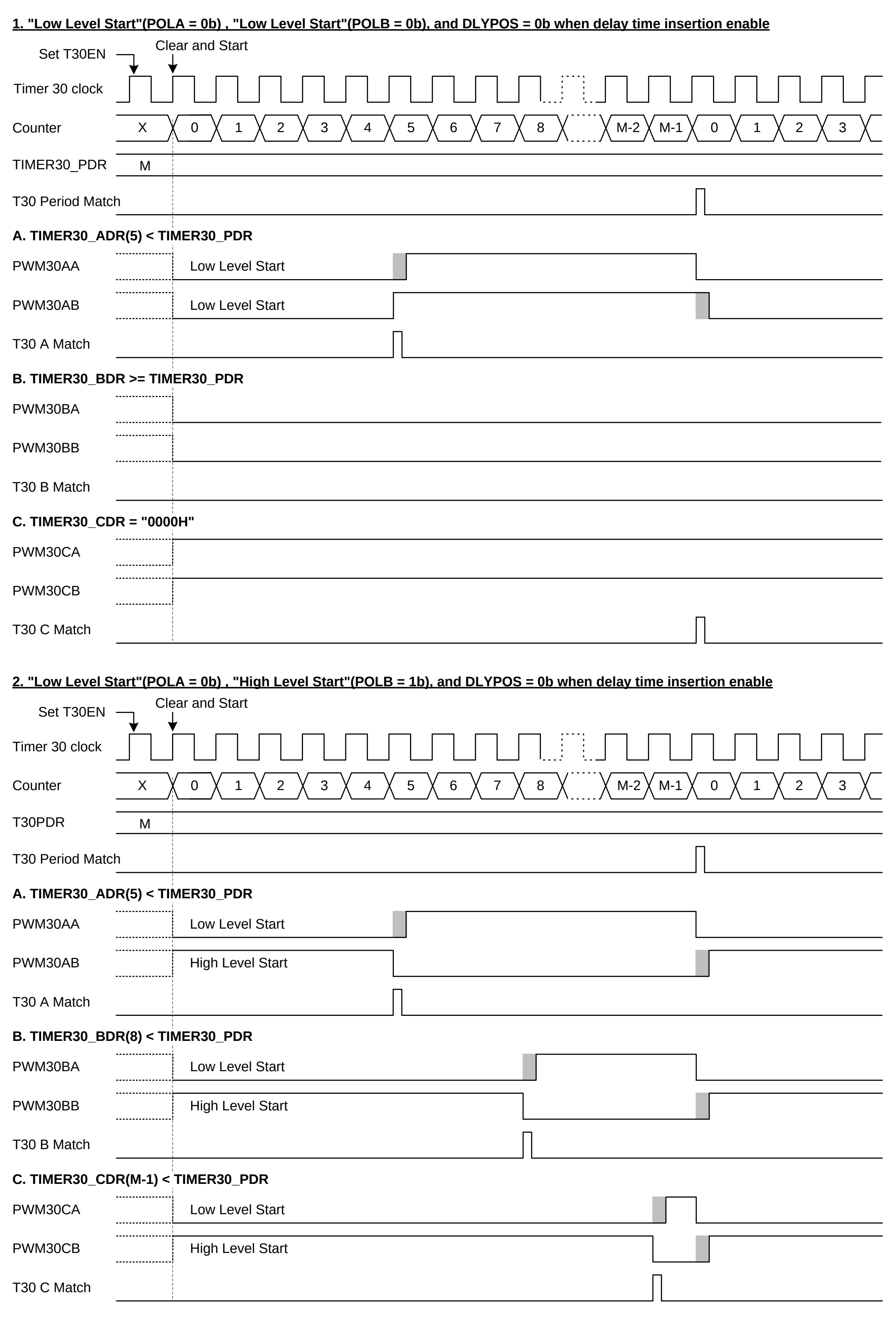
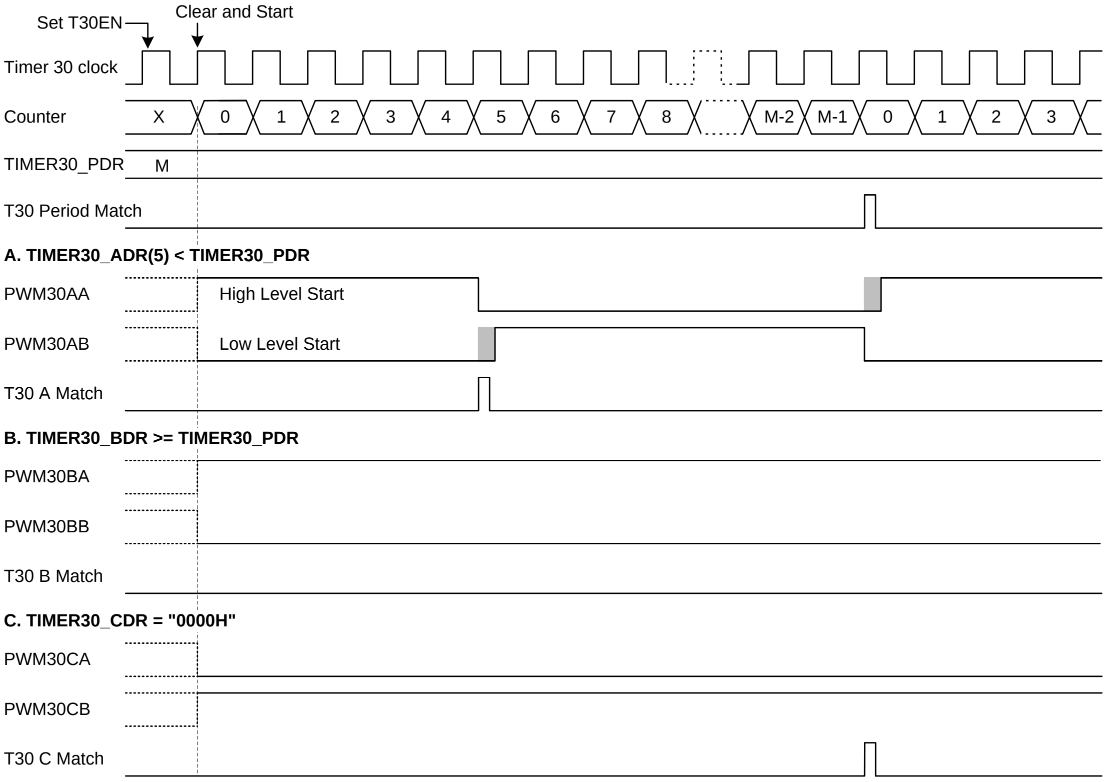


Figure 66. Interval Mode Timing Chart With "DLYPOS = 0"

1. "High Level Start"(POLA = 1b) , "Low Level Start"(POLB = 0b), and DLYPOS = 1b when delay time insertion enable



2. "High Level Start"(POLA = 1b) , "High Level Start"(POLB = 1b), and DLYPOS = 1b when delay time insertion enable

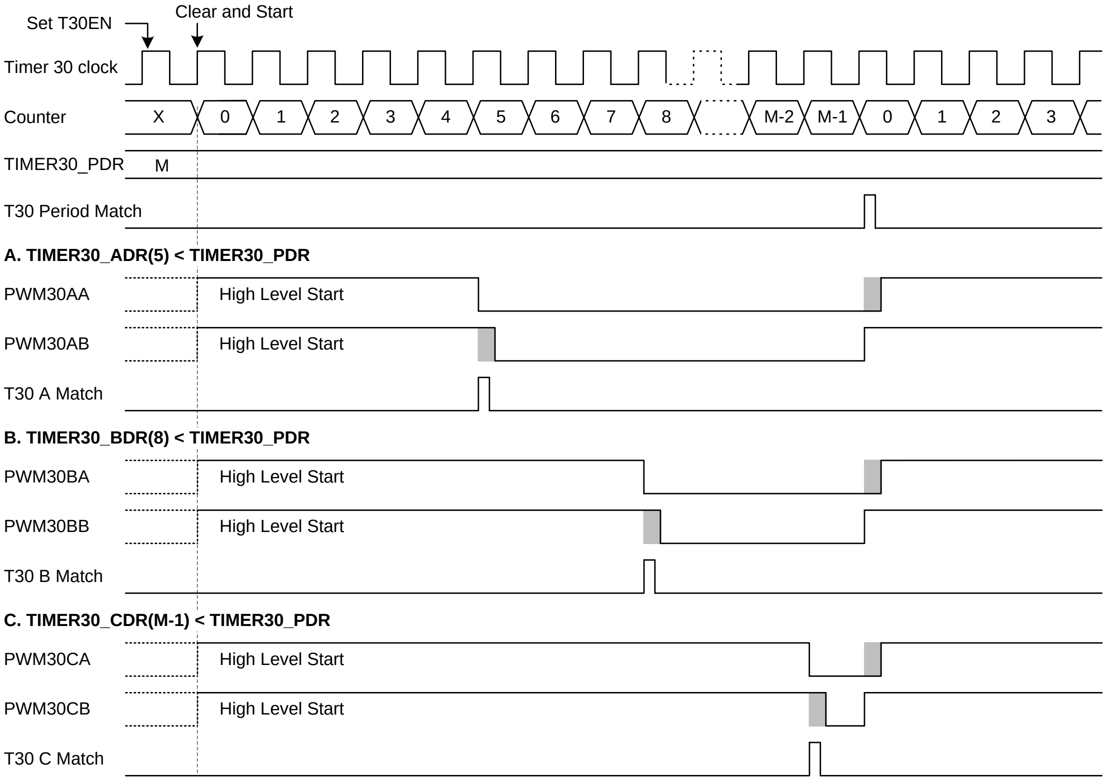


Figure 67. Interval Mode Timing Chart With “DLYPOS = 1

12.4.3.3 Back-to-Back Mode

Back-to-back mode is set by T30MS[1:0] as '10'. In the back-to-back mode, the 16-bit up/down counter repeats up/down count. In fact, the effective duty and period becomes twofold the register set values. If the TIMER30_PDR's data value is set to "0x3210", 16-bit up/down counter will increment until it reaches 0x3210. At this point, a period match signal is generated and the period match interrupt takes place. Then the 16-bit up/down counter will decrement until it reaches 0x0000. At this point, the bottom interrupt takes place. It repeats in this manner.

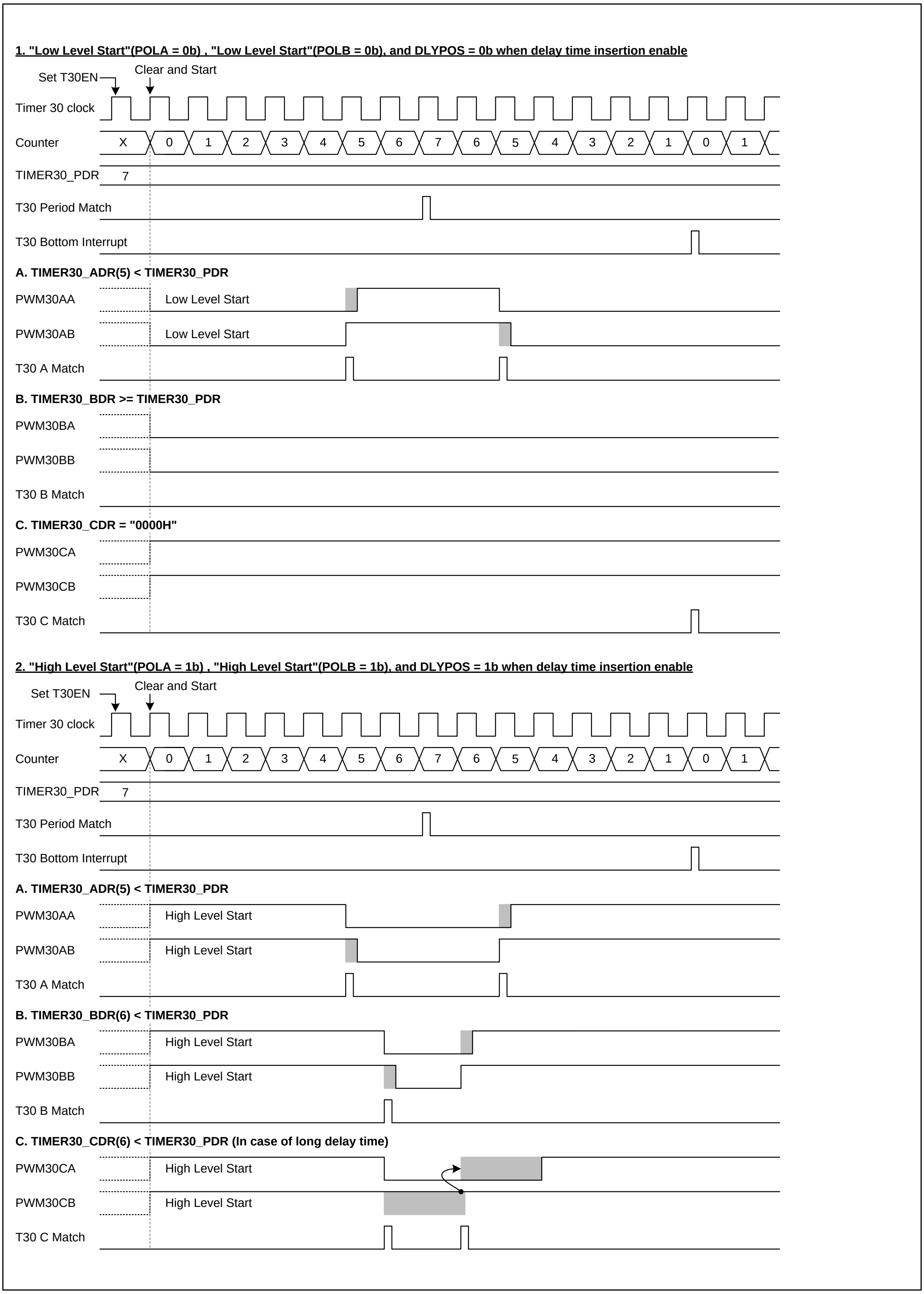


Figure 68. Back-to-Back Mode Timing Chart

12.4.3.4 Emergency protective function

This protective function is used for emergency stop, when the PWM30xA/PWM30xB output high-impedance enable bit, HIZEN, is enabled. When the signal on the external BLNK input pin goes active (falling or rising edge triggered), the PWM30xA/PWM30xB ports are immediately disabled and a high-impedance interrupt takes place. The TIMER30_HIZCR register is used for high-impedance control. The high-impedance source is the external BLNK input pin. The high-impedance edge can be selected by HEDGE bit as falling or rising edge. If the HIZST read value is '1', it indicates that the pins are under high-impedance state. To return from high-impedance state, the HIZCLR bit should be set to '1'. If HIZSW bit is set to '1', PWM30xA/PWM30xB pins go into high impedance state by software. It can be used for debugging. (x: A, B and C)

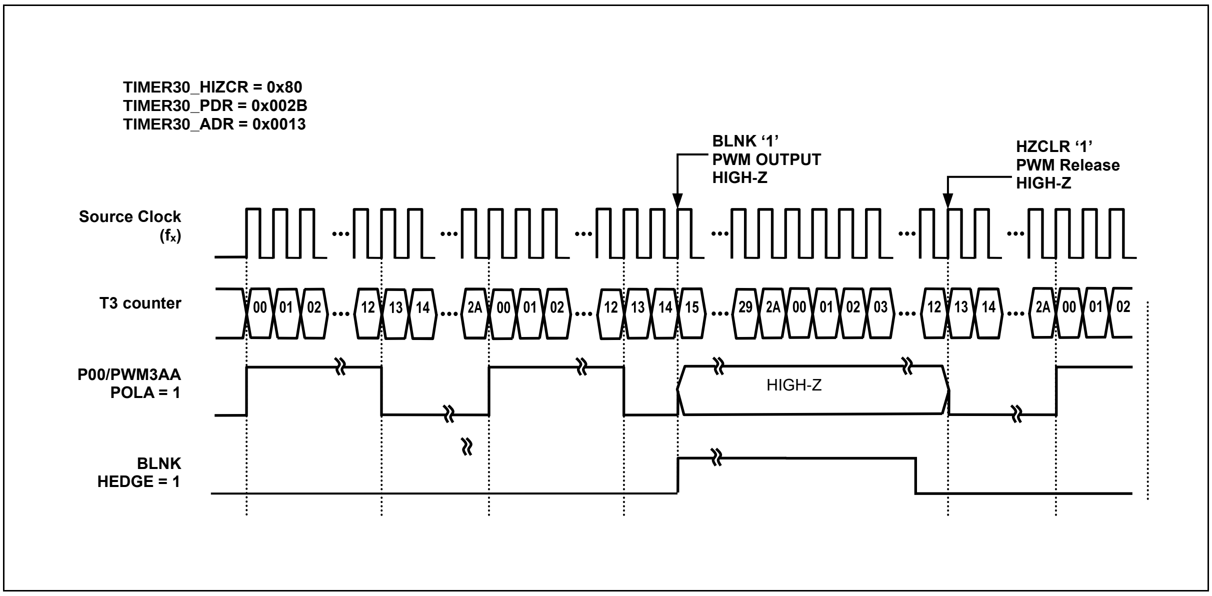


Figure 69. Example of PWM External Synchronization with BLNK Input (x: A, B and C)

12.4.3.5 FORCE A-Channel Mode

If FORCA bit is set to '1', it is possible to enable or disable all PWM output pins through PWM outputs generated from A-ch duty counter. Please note that the inversion outputs of A, B, C channel have the same A-ch output waveform.

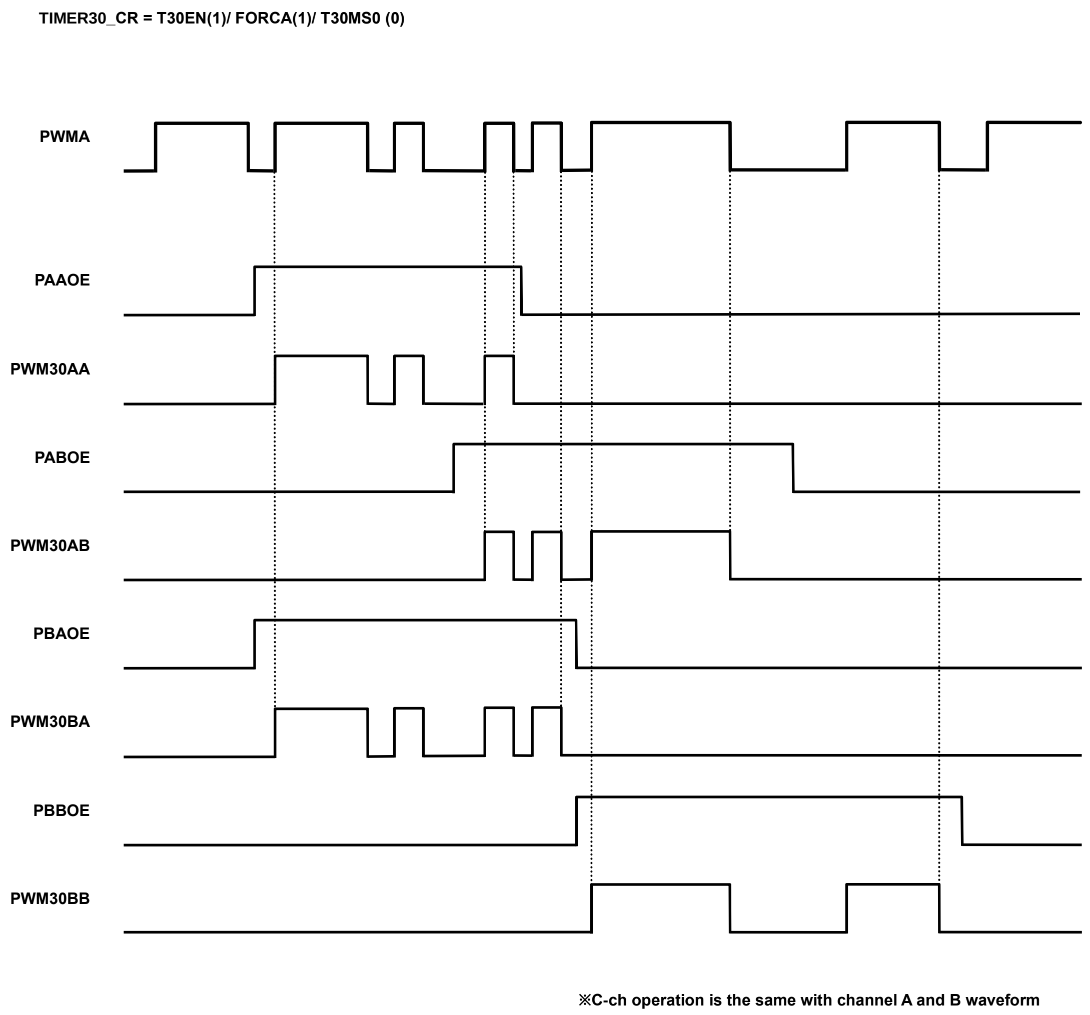


Figure 70. Example of Force A-Channel Mode

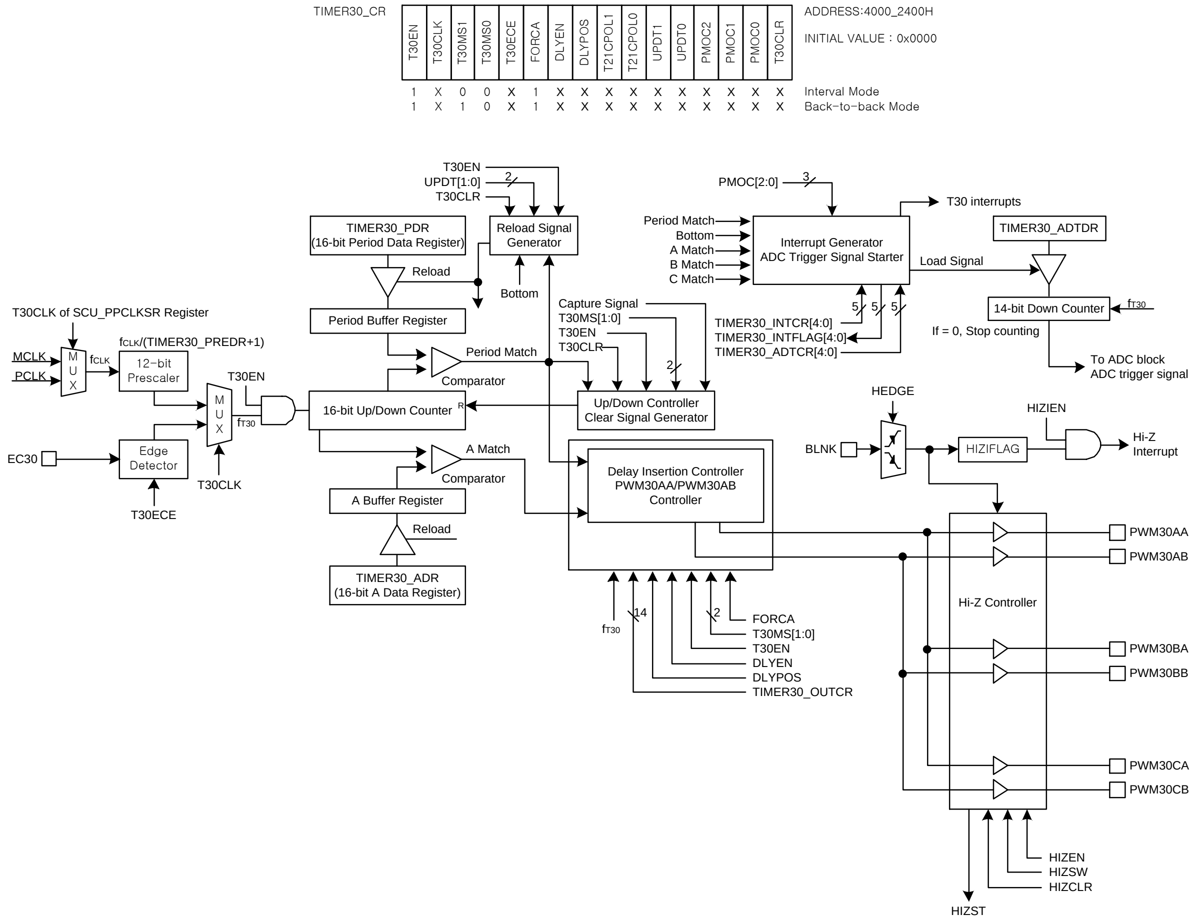


Figure 71. Force A-Channel Mode

12.4.3.6 6-Channel Mode

If FORCA bit is set to '0', it is possible to enable or disable PWM output pin and inversion output pin through the duty counter of each channel. The inversion output is the reverse phase of the PWM output. A AA/AB output of the A-channel duty register, a BA/BB output of the B-channel duty register, a CA/CB output of the C-channel duty register are controlled respectively.

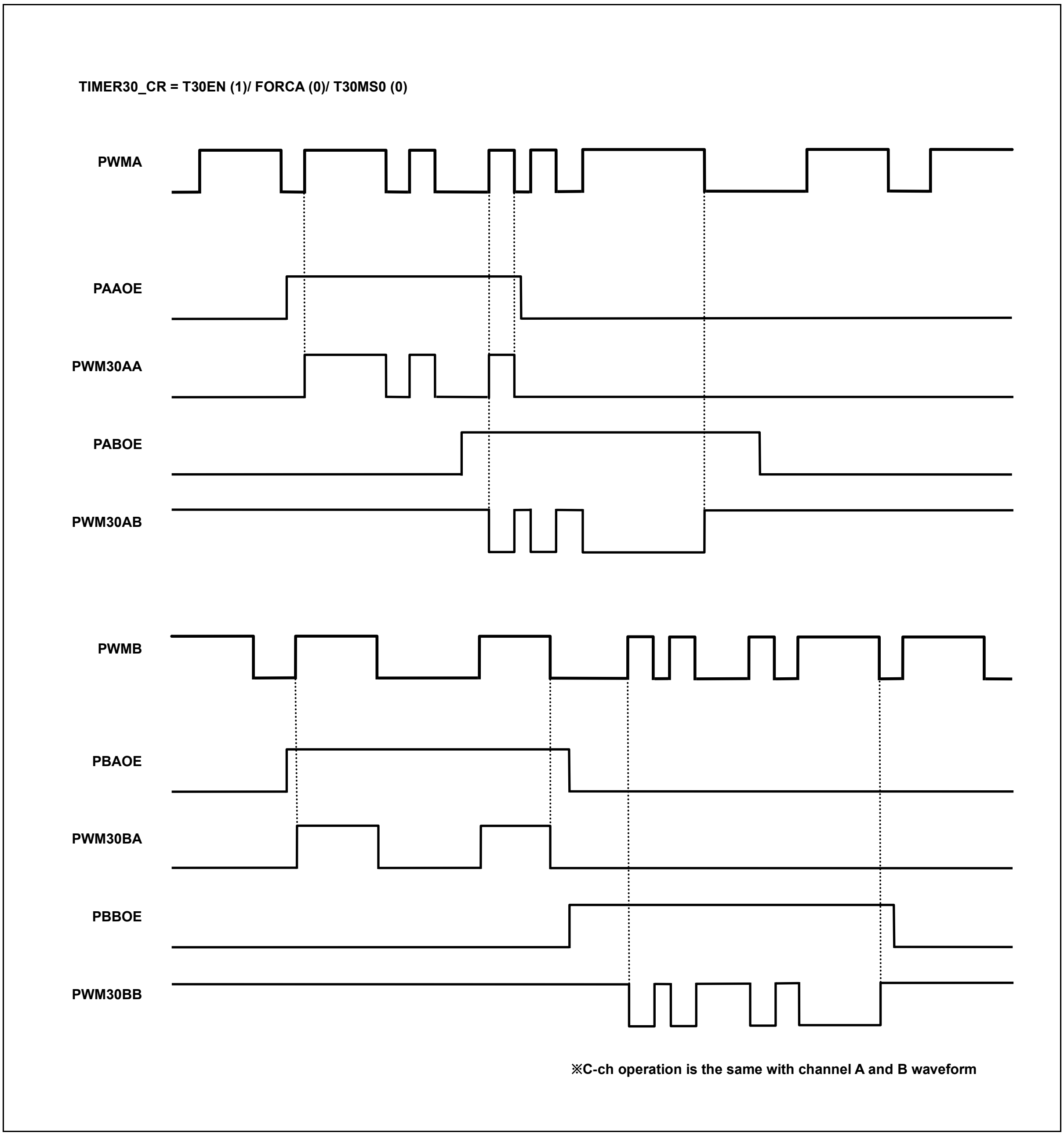


Figure 72. Example of 6-Channel Mode

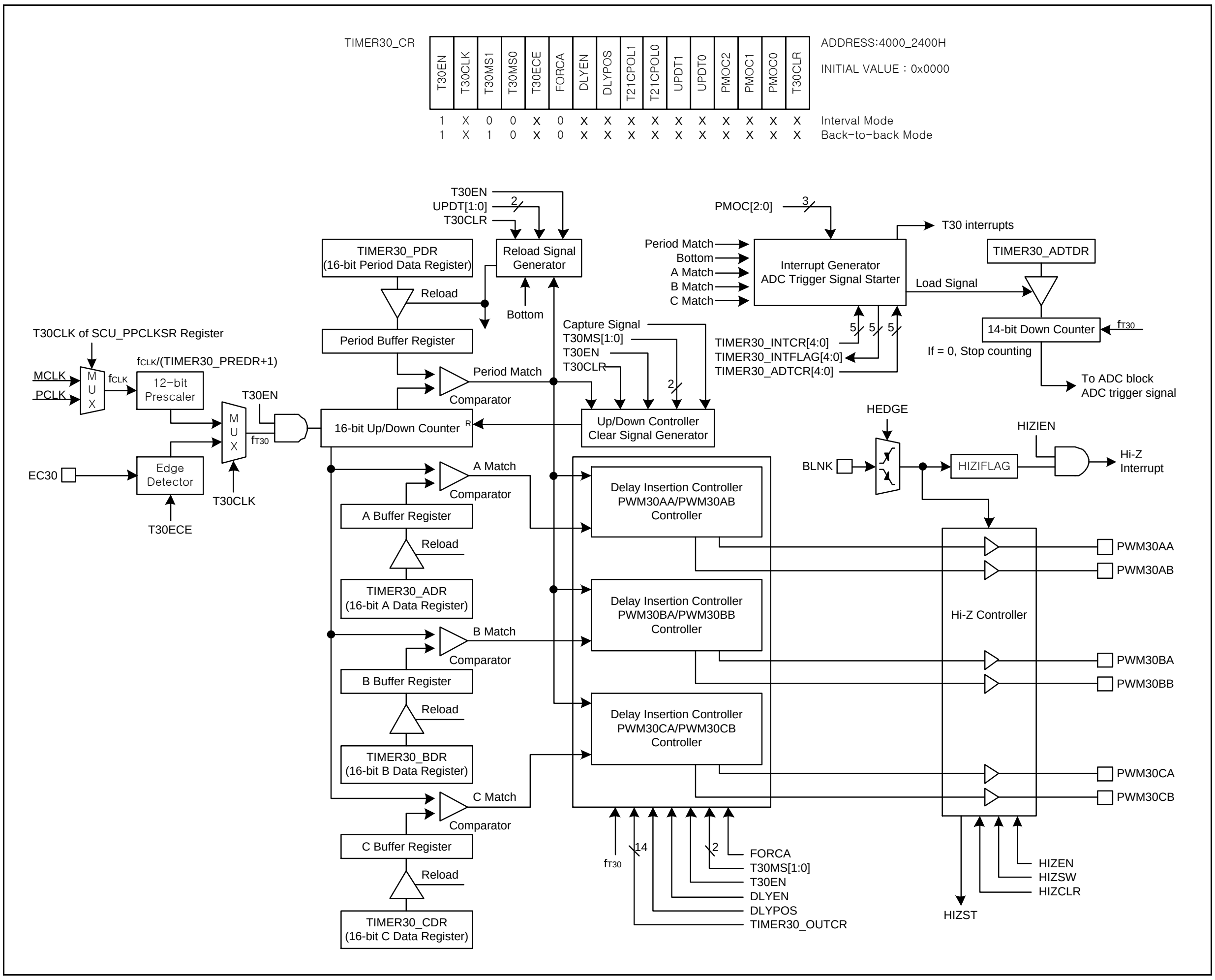


Figure 73. 6-Channel Mode

13 12-bit A/D Converter

ADC (Analog-to-Digital Converter) of A31G11x series allows conversion of an analog input signal to a corresponding 12-bit digital value. Its A/D module has eleven analog inputs as shown in Figure 74. Output of the multiplexer is the input into the converter, which generates the result through successive approximation.

The A/D module has three registers such as a control register (ADC_CR), a data register (ADC_DR), and a prescaler data register (ADC_PREDR). The channels to be converted are selected by setting ADSEL[3:0]. The register ADC_DR contains the results of the A/D conversion. When the conversion is completed, the result is loaded into the ADC_DR, A/D conversion status bit ADCIFLAG is set to '1', and the A/D interrupt is set. During A/D conversion, ADCIFLAG bit is read as '0'. Main features of the ADC are listed in the followings:

- 11-channel of analog inputs
- S/W (ADST), Timer trigger (T10/11/12 A match, ADC trigger signal from T30) support
- Conversion time: 58 clocks
- 5-bit Prescaler

13.1 12-bit ADC block diagram

Figure 74 shows a block diagram of an ADC block.

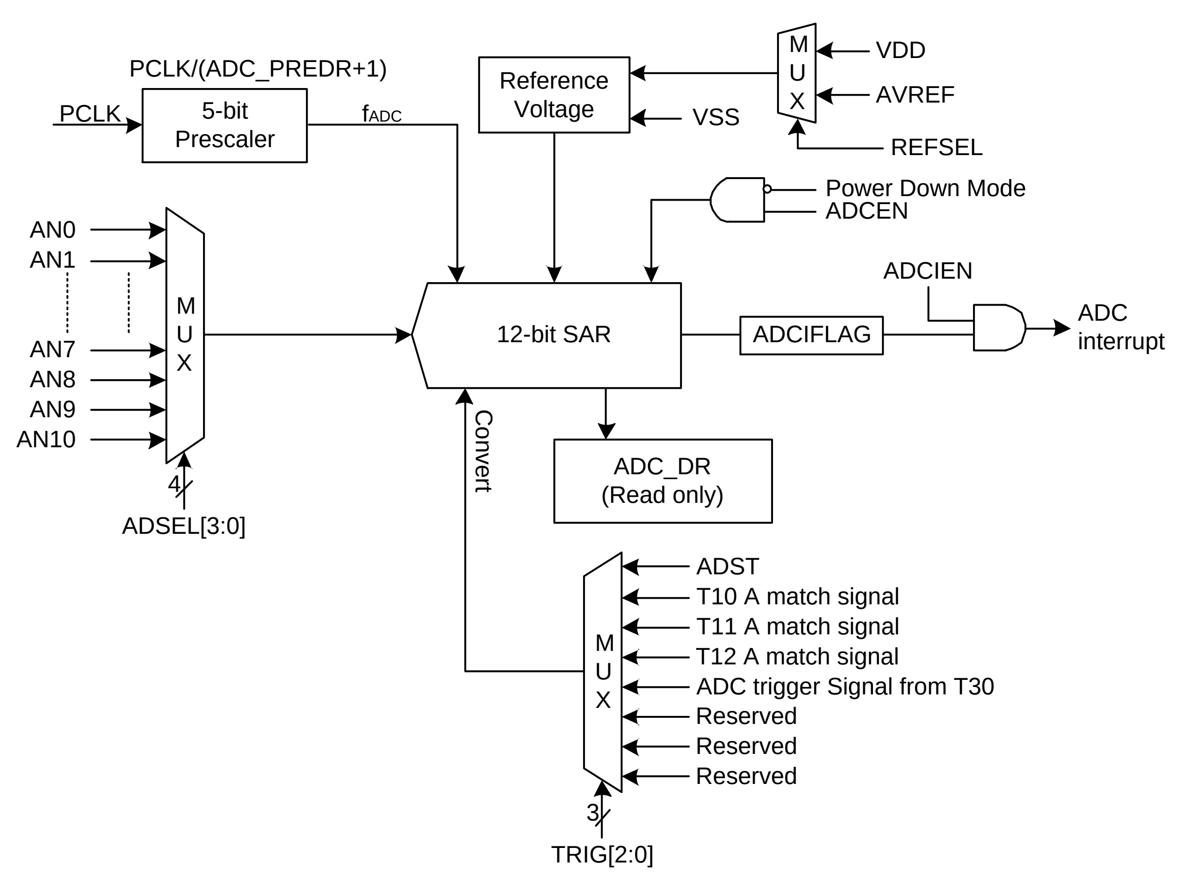


Figure 74. 12-bit ADC Block Diagram

13.2 Pin description for 12-bit ADC

Table 52. Pins and External Signals for 12-bit ADC

PIN NAME	TYPE	DESCRIPTION
VDD	P	Analog/Digital Power
VSS	P	Analog/Digital GND
AVREF	P	Analog Reference Voltage
AN0	A	ADC Input 0
AN1	A	ADC Input 1
AN2	A	ADC Input 2
AN3	A	ADC Input 3
AN4	A	ADC Input 4
AN5	A	ADC Input 5
AN6	A	ADC Input 6
AN7	A	ADC Input 7
AN8	A	ADC Input 8
AN9	A	ADC Input 9
AN10	A	ADC Input 10

NOTE: Where A=Analog, P= Power

13.3 Registers

Base address and register map of the ADC are shown in Table 53 and Table 54.

Table 53. Base Address of ADC

Name	Base address
ADC	0x4000_3000

Table 54. ADC Register Map

Name	Offset	Type	Description	Reset value
ADC_CR	0x0000	RW	A/D Converter Control Register	0x00000000
ADC_DR	0x0004	RO	A/D Converter Data Register	Unknown
ADC_PREDR	0x0008	RW	A/D Converter Prescaler Data Register	0x0000000F

13.3.1 ADC_CR: A/D converter control register

A/D Converter module should be configured properly before running.

ADC_CR register is 32-bit size and accessible in 32/16/8-bit.

ADC_CR=0x4000_3000

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15	14	13 12 11	10	9	8	7 6	5	4	3 2 1 0
Reserved	**ADCEN**	**Reserved**	**TRIG**	**REFSEL**	**Reserved**	**ADST**	**Reserved**	**ADCIEN**	**ADCIFLAG**	**ADSEL**
0x0000	**0**	**0**	**000**	**0**	**0**	**0**	**00**	**0**	**0**	**0000**
–	**RW**	**RW**	**RW**	**RW**	**-**	**RW**	**-**	**RW**	**RW**	**RW**

15	ADCEN	ADC Module Enable. (The ADC is automatically disabled at power down mode)	
		0	Disable ADC module operation.
		1	Enable ADC module operation.
13 11	TRIG	ADC Trigger Signal Selection.	
		000	ADST.
		001	Timer 10 A-match signal.
		010	Timer 11 A-match signal.
		011	Timer 12 A-match signal.
		100	ADC trigger signal from timer 30
		Others	Reserved
10	REFSEL	ADC Reference Selection.	
		0	Select analog power. (VDD)
		1	Select external reference. (AVREF)
8	ADST	ADC Conversion Start. This bit is automatically cleared to '0' after operation.	
		0	No effect.
		1	Trigger signal generation for conversion start.
5	ADCIEN	ADC Interrupt Enable.	
		0	Disable ADC interrupt.
		1	Enable ADC interrupt.
4	ADCIFLAG	ADC Interrupt Flag.	
		0	No request occurred.
		1	Request occurred. The bit is cleared to '0' when '1' is written.
3 0	ADSEL	A/D Converter Channel Selection.	
		0000	AN0
		0001	AN1
		0010	AN2
		0011	AN3
		0100	AN4
		0101	AN5
		0110	AN6
		0111	AN7
		1000	AN8
		1001	AN9
		1010	AN10
		Others	Reserved

13.3.2 ADC_DR: A/D converter data register

ADC_DR register is 32-bit size and accessible in 32/16/8-bit.

ADC_DR=0x4000_3004

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="20">Reserved</td><td colspan="12">ADDATA</td></tr>
<tr><td colspan="20">0x00000</td><td colspan="12">0xXXX</td></tr>
<tr><td colspan="20">-</td><td colspan="12">RO</td></tr>
</table>

11 0	ADDATA	A/D Converter Result Data.

13.3.3 ADC_PREDR: A/D converter prescaler data register

ADC_PREDR register is 32-bit size and accessible in 32/16/8-bit.

ADC_PREDR=0x4000_3008

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="27">Reserved</td><td colspan="5">PRED</td></tr>
<tr><td colspan="27">0x000000</td><td colspan="5">01111</td></tr>
<tr><td colspan="27">–</td><td colspan="5">RW</td></tr>
</table>

4 0	PRED	A/D Converter Prescaler Data.

NOTES:

1. The prescaler sets the A/D conversion clock. The frequency of A/D converter should be less than 3MHz because the conversion time needs at least 20µs.
2. If the A/D frequency is more than 3MHz, malfunction may occur.

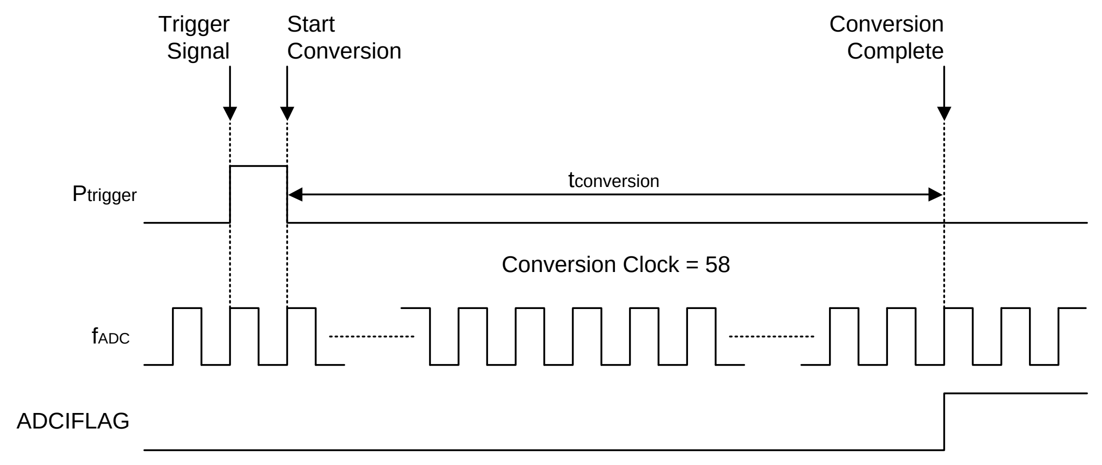
13.4 Functional description

13.4.1 ADC conversion timing

The A/D conversion process requires 4 steps (4 clock edges) to convert each bit and 10 clocks to set up A/D conversion. Therefore, total of 58 clocks are required to complete a 12-bit conversion: When the frequency of A/D converter is 1MHz, one clock cycle is 1μs. Each bit conversion requires 4 clocks. The conversion rate is calculated as follows:

4 clocks/bit × 12 bits + set-up time = 58 clocks,

58 clock × 1 μs = 58 μs at 1MHz



NOTE: The conversion time needs more than 20μs when VDD ≥ 4.0V, is 30μs when VDD ≥ 3.0V and is 60 μs when VDD ≥ 2.7V.

Figure 75. 12-bit ADC Converter Timing Chart

14 USART 10/11

USART (Universal Synchronous and Asynchronous serial Receiver and Transmitter) is a highly flexible serial communication device. The USART of A31G11x series features the followings:

- Full Duplex Operation. (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation
- Baud Rate Generator
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits
- Odd or Even Parity Generation, and Parity Check Supported by Hardware.
- Data OverRun Detection
- Framing Error Detection
- Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion
- Double Speed Asynchronous communication mode

14.1 USART 10/11 block diagram

Figure 76 shows a block diagram of the UART block.

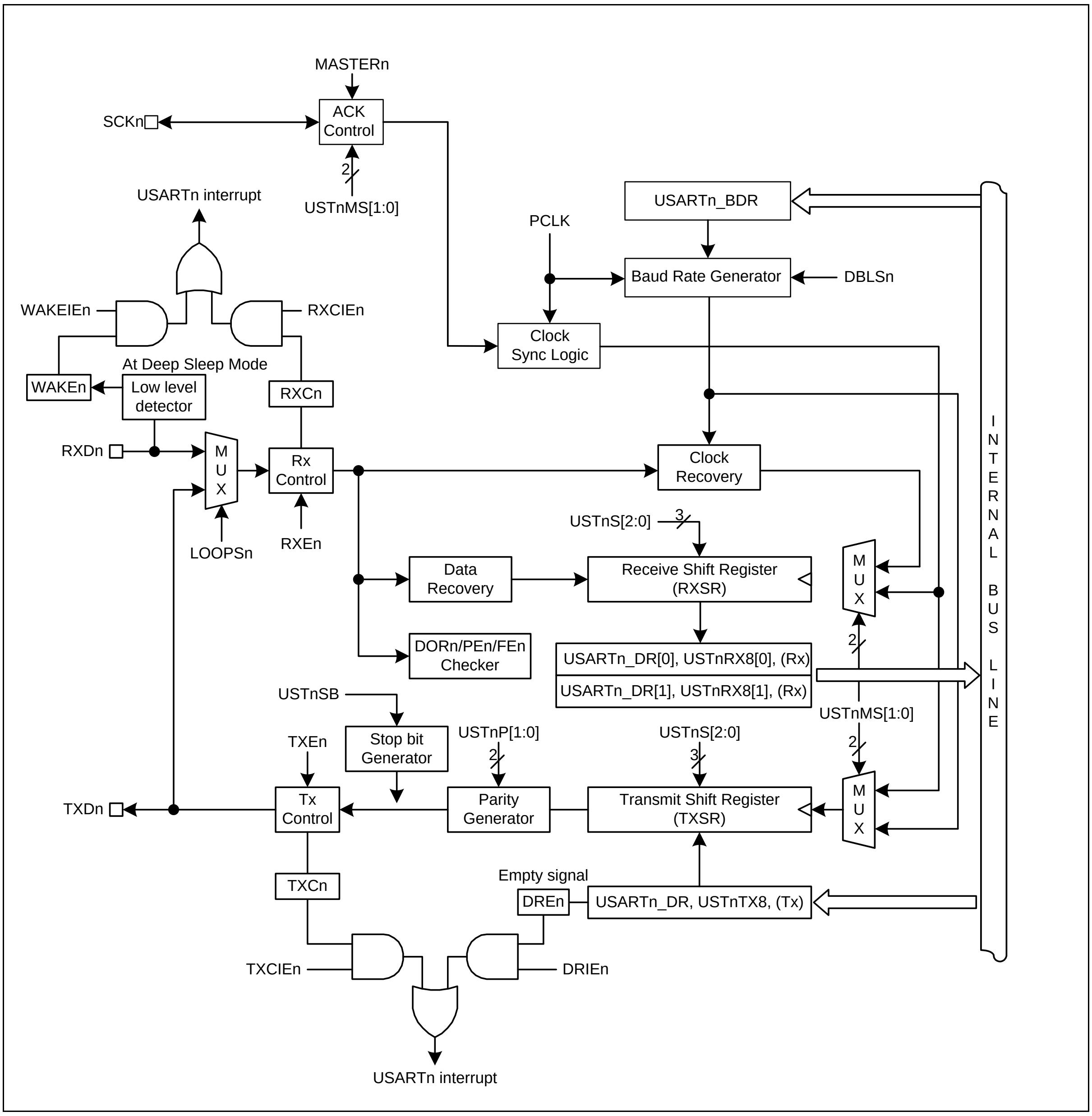
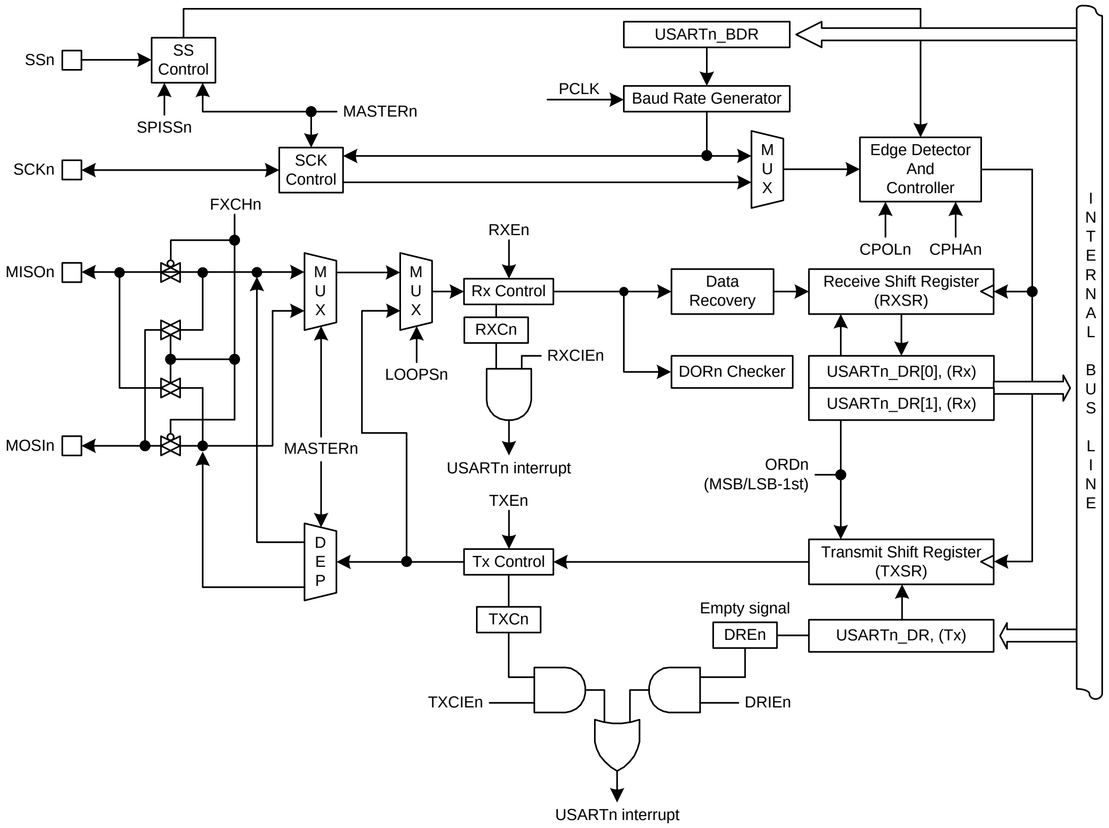


Figure 76. UART n Block Diagram of USART (n = 10 and 11)

Figure 77 shows a block diagram of the SPI block.



NOTES:

1. After the transmitting, the next transmission should be started after one clock of the SPI clock.
2. In SPI mode, both MOSI1n and MISO1n should be configured as alternative function pins.

Figure 77. SPIn Block Diagram of USART (n = 10 and 11)

14.2 Pin description for USART 10/11

Table 55. Pins and External Signals for USART 10/11

PIN NAME	TYPE	DESCRIPTION
TXDn	O	UART Channel n transmit output
RXDn	I	UART Channel n receive input
SSn	I/O	SPIn Slave select input / output
SCKn	I/O	SPIn Serial clock input / output
MOSIn	I/O	SPIn Serial data (Master output, Slave input)
MISOn	I/O	SPIn Serial data (Master input, Slave output)

14.3 Registers

Base address and register map of the USART 10/11 are shown in Table 56 and Table 57.

Table 56. Base Address of USART 10/11

Name	Base address	Size	Description
USART 10	0x4000_3800	256	USART 10 block (UART 10 + SPI 10)
USART 11	0x4000_3900	256	USART 11 block (UART 11 + SPI 11)

Table 57. USART n Register Map (n = 10 and 11)

Name	Offset	Type	Description	Reset value
USARTn_CR1	0x00	RW	USARTn control register 1	0x00000000
USARTn_CR2	0x04	RW	USARTn control register 2	0x00000000
USARTn_ST	0x0C	RW	USARTn status register	0x00000080
USARTn_BDR	0x10	RW	USARTn baud rate generation register	0x00000FFF
USARTn_DR	0x14	RW	USARTn data register	0x00000000

14.3.1 USARTn_CR1: USARTn control register 1

USART module should be configured properly before running.

USARTn_CR1 register is 32-bit size and accessible in 32/16/8-bit. (n = 10 and 11)

USART10_CR1=0x4000_3800, USART11_CR1=0x4000_3900

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14	13 12	11 10 9	8	7	6	5	4	3	2	1	0
Reserved		USTnMS	USTnP	USTnS	ORDn	CPOLn	CPHAn	DRIEn	TXCIEn	RXCIEn	WAKEIEn	TXEn	RXEn
0x0000		00	00	000	0	0	0	0	0	0	0	0	0
–		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

15	USTnMS	USARTn Operation Mode Selection.			
14		00	Asynchronous Mode. (UART)		
		01	Synchronous Mode.		
		10	Reserved.		
		11	SPI mode		
13	USTnP	Selects Parity Generation and Check method. (only UART mode)			
12		00	No parity.		
		01	Reserved.		
		10	Even parity.		
		11	Odd parity.		
11	USTnS	Selects the length of data bit in a frame at Asynchronous or Synchronous mode.			
9		000	5 bit.		
		001	6 bit.		
		010	7 bit.		
		011	8 bit.		
		111	9 bit.		
		Others	Reserved.		
8	ORDn	Selects the first data bit to be transmitted. (only SPI mode)			
		0	LSB-first.		
		1	MSB-first.		
7	CPOLn	Selects the clock polarity of ACK in synchronous or SPI mode.			
		0	TXD Change @Rising Edge, RXD Change @Falling Edge.		
		1	TXD Change @Falling Edge, RXD Change @Rising Edge.		
6	CPHAn	CPOLn and this bit determine if data are sampled on the leading or the trailing edge of SCK. (only SPI mode)			
		CPOLn	CPHAn	Leading edge	Trailing edge
		0	0	Sample (Rising)	Setup (Falling)
		0	1	Setup (Rising)	Sample (Falling)
		1	0	Sample (Falling)	Setup (Rising)
		1	1	Setup (Falling)	Sample (Rising)
5	DRIEn	Transmit Data Register Empty Interrupt Enable.			
		0	Disable transmit data empty interrupt.		
		1	Enable transmit data empty interrupt.		
4	TXCIEn	Transmit Complete Interrupt Enable.			
		0	Disable transmit complete interrupt.		
		1	Enable transmit complete interrupt.		
3	RXCIEn	Receive Complete Interrupt Enable.			
		0	Disable receive complete interrupt.		
		1	Enable receive complete interrupt.		

2	WAKEIEn	Asynchronous Wake-up Interrupt Enable in Deep Sleep Mode. When device is in deep sleep mode, if RXDn goes to low level, an interrupt can be requested to wake-up system (only UART mode). This bit should be cleared to ‘0’ to receive Rx data.	
		0	Disable asynchronous wake-up interrupt.
		1	Enable asynchronous wake-up interrupt. (Only used for wake-up)
1	TXEn	Enables the Transmitter unit. **NOTE**: The TXEn bit should be set to '1' while USTnEN bit is ‘0’.	
		0	Transmitter is disabled.
		1	Transmitter is enabled.
0	RXEn	Enables the Receiver unit. **NOTE**: The RXEn bit should be set to '1' while USTnEN bit is ‘0’.	
		0	Receiver is disabled.
		1	Receiver is enabled.

NOTE: The CPOLn and CPHAn bits should be changed while TXEn and RXEn bits are ‘0’

14.3.2 USARTn_CR2: USARTn control register 2

USART module should be configured properly before running.

USARTn_CR2 register is 32-bit size and accessible in 32/16/8-bit. (n = 10 and 11)

USART10_CR2=0x4000_3804, USART11_CR2=0x4000_3904

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10	9	8	7	6	5	4	3	2	1	0
Reserved	**USTnEN**	**DBLSn**	**MASTERn**	**LOOPSn**	**DISSCKn**	**USTnSSEN**	**FXCHn**	**USTnSB**	**USTnTX8**	**USTnRX8**
0x00000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
-	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**	**RO**

9	USTnEN	Enable USARTn block. This bit can be cleared to '0b' during the corresponding TXEn and RXEn bits are all '0b'.	
		0	Disable USARTn block.
		1	Enable USARTn block.
8	DBLSn	Selects receiver sampling rate. (only asynchronous mode)	
		0	Normal asynchronous operation.
		1	Double speed asynchronous operation.
7	MASTERn	Selects master or slave in SPIn or Synchronous mode and controls the direction of SCKn pin.	
		0	Slave operation. (External clock for SCKn)
		1	Master operation. (Internal clock for SCKn)
6	LOOPSn	Control the Loop Back mode of USARTn for test mode.	
		0	Normal operation.
		1	Loop back mode
5	DISSCKn	In synchronous mode operation, selects the waveform of SCKn output.	
		0	SCKn is free-running while USARTn is enabled in synchronous master mode.
		1	SCKn is active while any frame is transferring.
4	USTnSSEN	This bit controls the SSn pin operation. (only SPI mode)	
		0	Disable.
		1	Enable.
3	FXCHn	SPIn port function exchange control. (only SPI mode)	
		0	No effect.
		1	Exchange MOSIn and MISOn function.
2	USTnSB	Selects the length of stop bit in Asynchronous or Synchronous mode.	
		0	1 Stop bit.
		1	2 Stop bit.
1	USTnTX8	The ninth bit of data frame in Asynchronous or Synchronous mode of operation. Write this bit first before loading the USARTn_DR register	
		0	MSB (9th bit) to be transmitted is '0'.
		1	MSB (9th bit) to be transmitted is '1'.
0	USTnRX8	The ninth bit of data frame in Asynchronous or Synchronous mode of operation. Read this bit before reading the receive buffer (only UART mode)	
		0	MSB (9th bit) to be received is '0'.
		1	MSB (9th bit) to be received is '1'.

14.3.3 USARTn_ST: USARTn status register

USARTn_ST register is 32-bit size and accessible in 32/16/8-bit. (n = 10 and 11)

USART10_ST=0x4000_380C, USART11_ST=0x4000_390C

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Reserved	**DREn**	**TXCn**	**RXCn**	**WAKEn**	**Reserved**	**DORn**	**FEn**	**PEn**
0x000000	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
-	**RW**	**RW**	**RO**	**RW**	**-**	**RO**	**RW**	**RW**

7	DREn	Transmit Data Register Empty Interrupt Flag. The DRE flag indicates if the transmit data register (USARTn_DR) is ready to receive new data. If DRE is '1', the data register is empty and ready to be written.	
		0	Transmit buffer is not empty.
		1	Transmit buffer is empty. This bit is cleared to '0' when '1' is written.
6	TXCn	Transmit Complete Interrupt Flag. This flag is set when the entire frame in the transmit shift register has been shifted out and there is no new data currently present in the transmit buffer.	
		0	No request occurred.
		1	Transmit buffer is empty and the data in transmit shift register is shifted out completely. This bit is cleared to '0' when '1' is written.
5	RXCn	Receive Complete Interrupt Flag. This flag is set when there are unread data in the receive buffer and cleared when all the data in the receive buffer are read.	
		0	There is no data unread in the receive buffer.
		1	There are more than 1 unread data in the receive buffer.
4	WAKEn	Asynchronous Wake-up Interrupt Flag. This flag is set when the RXD pin is detected as low while the CPU is in deep sleep mode. (only UART mode)	
		0	No request occurred.
		1	Request occurred. The bit is cleared to '0' when '1' is written.
2	DORn	This bit is set if data OverRun takes place. While this bit is set, the incoming data frame is ignored. This flag is valid until the receive buffer is read.	
		0	No Data OverRun.
		1	Data OverRun detected.
1	FEn	This bit is set if the first stop bit of next character in the receive buffer is detected as '0'. This bit is valid until the receive buffer is read. (only UART mode)	
		0	No Frame Error.
		1	Frame Error detected.
0	PEn	This bit is set if the next character in the receive buffer has a Parity Error while parity is checked. This bit is valid until the receive buffer is read. (only UART mode)	
		0	No Parity Error.
		1	Parity Error detected.

14.3.4 USARTn_BDR: USARTn baud rate generation register

USARTn_BDR register is 32-bit size and accessible in 32/16/8-bit. (n = 10 and 11)

USART10_BDR=0x4000_3810, USART11_BDR=0x4000_3910

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				**BDATA**											
0x00000																				**0xFFF**											
-																				**RW**											

11 0	BDATA	The value in this register is used to generate internal baud rate in UART mode or to generate SCK clock in SPI mode. To prevent malfunction, do not write '0' in UART mode and do not write '0' or '1' in synchronous or SPI mode.

14.3.5 USARTn_DR: USARTn data register

USARTn_DR register is 32-bit size and accessible in 32/16/8-bit. (n = 10 and 11)

USART10_DR=0x4000_3814, USART11_DR=0x4000_3914

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								**DATA**							
0x000000																								**0x00**							
–																								**RW**							

7 0	DATA	The USART Transmit buffer and Receive buffer share the same I/O address with this DATA register. The Transmit Data Buffer is the destination for data written to the USARTn_DR register. Reading the USARTn_DR register returns the contents of the Receive Buffer. Write to this register only when the DRE flag is set. In SPI master mode, the SCK clock is generated when data are written to this register. **NOTE**: This byte will not be written when the block is disabled or when both TXEn and RXEn bits are '0'.

14.4 Functional description

The USART comprises clock generator, transmitter and receiver. The clock generation logic consists of synchronization logic for external clock input used by synchronizing or SPI slave operation, and the baud rate generator for asynchronous or master (synchronous or SPI) operation.

The Transmitter consists of a single write buffer, a serial shift register, parity generator and control logic for handling different serial frame formats. The write buffer allows continuous transfer of data without any delay between frames. The receiver is the most complex part of the UART module due to its clock and data recovery units. The recovery unit is used for asynchronous data reception. In addition to the recovery unit, the receiver includes a parity checker, a shift register, a two-level receive FIFO (USARTn_DR) and control logic. The receiver supports the same frame formats as the transmitter and can detect frame error, data overrun and parity errors. (n = 10 and 11)

14.4.1 USART clock generation

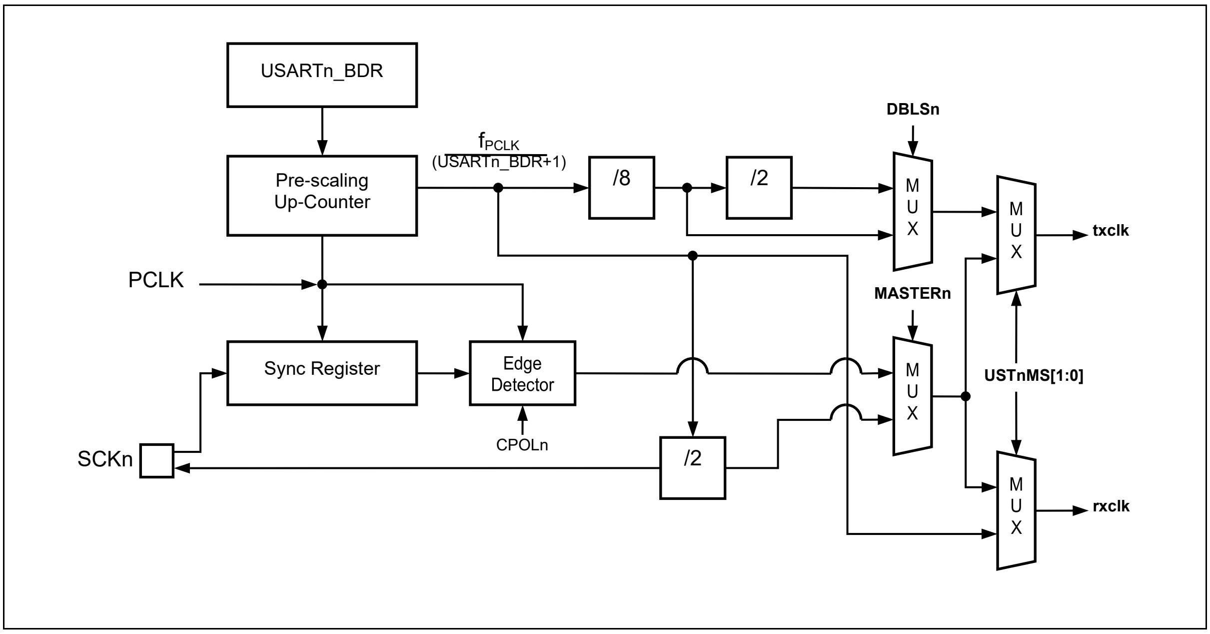


Figure 78. Clock Generation Block Diagram (USART, n = 10 and 11)

The clock generation logic generates the base clock for the transmitter and receiver. The USART supports four modes of clock operation, which are Normal asynchronous mode, Double speed asynchronous mode, Master synchronous mode and Slave synchronous mode.

The clock generation scheme for master SPI and slave SPI mode is the same as master synchronous and slave synchronous operation mode. The USTnMS[1:0] bits in USARTn_CR1 register selects asynchronous or synchronous operation. Asynchronous double speed mode is controlled by the DBLS bit in the USARTn_CR2 register.

The MASTER bit in USARTn_CR2 register controls whether the clock source is internal (master mode, output pin) or external (slave mode, input pin). The SCKn pin is active only when the USART operates in synchronous or SPI mode.

Table 58 shows the equations for calculating the baud rate (in bps).

Table 58. Equations for Calculating USART Baud Rate Register Settings (n = 10 and 11)

Operating Mode	**Equation for Calculating Baud Rate**
Asynchronous Normal Mode (DBLSn=0)	Baud Rate = PCLK/(16(USARTn_BDR+1))
Asynchronous Double Speed Mode (DBLSn=1)	Baud Rate = PCLK/(8(USARTn_BDR+1))
Synchronous or SPI Master Mode	Baud Rate = PCLK/(2(USARTn_BDR+1))

14.4.2 External clock (SCKn)

External clock is used in the Synchronous mode or in the SPI slave mode. External clock input from the SCKn pin is sampled by the synchronization logic to remove meta-stability. The output from the synchronization logic must be passed through an edge detector before it is used by the transmitter and the receiver. This process introduces two CPU clock period delay. The maximum frequency of the external SCKn pin is limited up to 2.5MHz.

14.4.3 Synchronous mode operation

External clock is used in the Synchronous mode or in the SPI slave mode. When the Synchronous or the SPI mode is used, the SCKn pin will be used as either clock input (slave) or clock output (master).

Data sampling and transmission are issued on different edges of SCKn clock respectively. For example, if data input on RXDn (MISOn in SPI mode) pin is sampled on the rising edge of SCKn clock, data output on TXDn (MOSIn in SPI mode) pin is altered on the falling edge.

The CPOLn bit in USARTn_CR1 register selects which SCKn clock edge is used for data sampling and which is used for data change. As shown in Figure 79 below, when CPOLn is zero, the data will be changed at rising SCKn edge and sampled at falling SCKn edge.

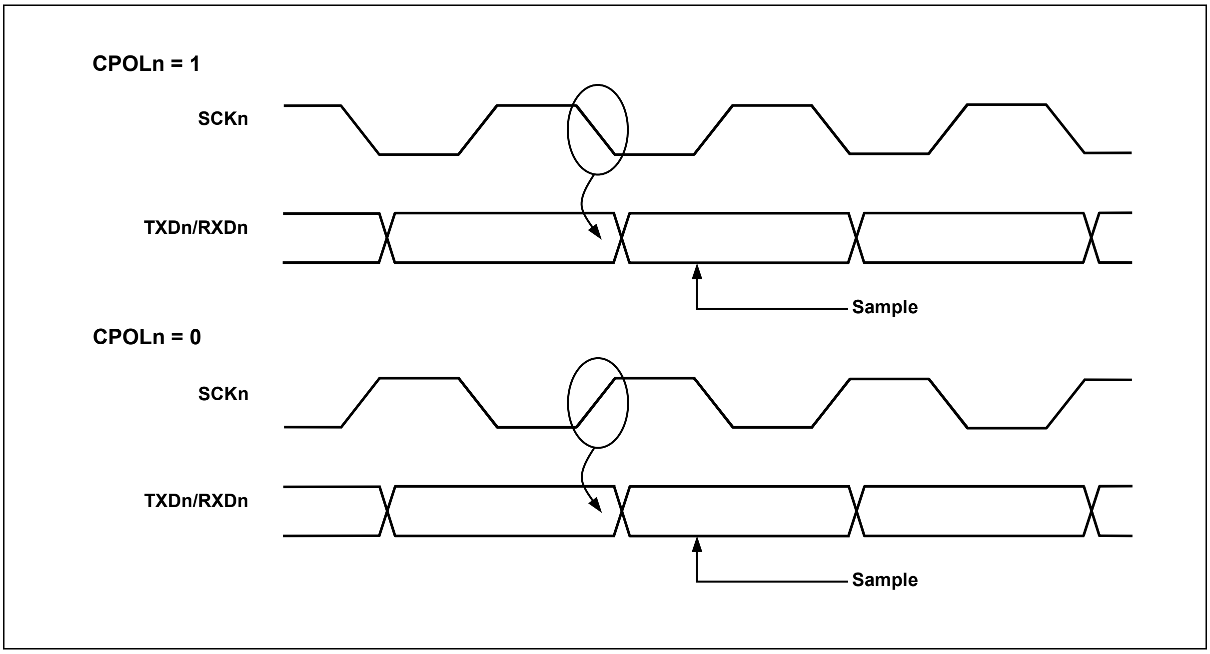


Figure 79. Synchronous Mode SCKn Timing (USART, n = 10 and 11)

14.4.4 UART data format

A serial frame is defined to be one character of data bits with synchronization bits (start and stop bits), and optionally a parity bit for error detection. The USART supports all 30 combinations of the followings as valid frame formats.

- 1 start bit
- 5, 6, 7, 8 or 9 data bits
- No, even or odd parity bit.
- 1 or 2 stop bits.

A frame starts with the start bit followed by the least significant data bit (LSB). Then the next data bits, up to nine, follow, ending with the most significant bit (MSB). If a parity function is enabled, the parity bit is inserted between the last data bit and the stop bit. A high-to-low transition on data pin is considered as a start bit.

When a complete frame is transmitted, it can be directly followed by a new frame, or the communication line can be set to an idle state. The idle state means high state of data pin. Figure 80 shows a possible combination of the frame formats. Bits inside brackets are optional.

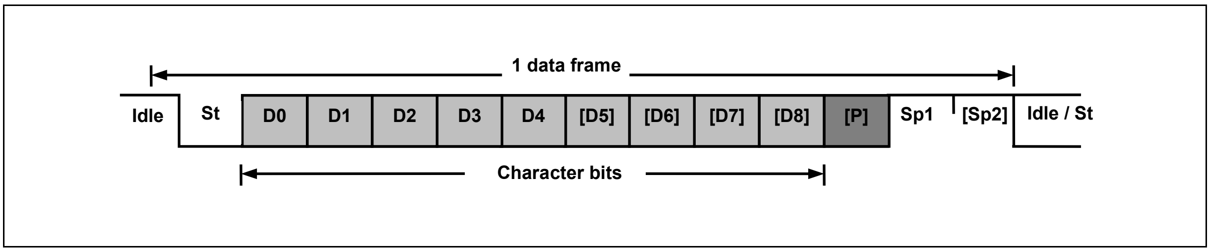


Figure 80. Frame Format (UART)

1 data frame consists of the following bits

- Idle: No communication on communication line (TXDn/RXDn)
- St: Start bit (low)
- Dm: Data bits (0 to 8)

- P: Parity bit (even parity, odd parity, no parity)
- Sp: Stop bit (1 bit or 2 bits)

The frame format used by the UART is set by USTnS[2:0], USTnP[1:0] bits in the USARTn_CR1 register and USTnSB bit in the USARTn_CR2 register. The transmitter and the receiver use the same values. (n = 10 and 11)

14.4.5 UART parity bit

The parity bit is calculated by doing an exclusive-OR of all data bits. If odd parity is used, the result of the exclusive-OR is inverted. The parity bit is located between the MSB and the first stop bit of a serial frame.

- Peven = Dm-1 ^ … ^ D3 ^ D2 ^ D1 ^ D0 ^ 0
- Podd = Dm-1 ^ … ^ D3 ^ D2 ^ D1 ^ D0 ^ 1
- Peven: Parity bit using even parity
- Podd: Parity bit using odd parity
- Dm: Data bit n of the character

14.4.6 UART transmitter

The UART transmitter is enabled by setting TXEn bit in the USARTn_CR1 register. When the Transmitter is enabled, the TXDn pin should be set to TXDn function for the serial output pin in UART mode by the GPIO registers. Baud-rate, operation mode and frame format must be set up before starting any transmission. In Synchronous operation mode, the SCKn pin is used for transmission clock, so it should be selected to do SCKn function by the GPIO registers. (n = 10 and 11)

14.4.6.1 UART sending TX data

A data transmission is initiated by loading data to the transmit data register (USARTn_DR register I/O location). The data to be written in transmit data register is moved to the shift register when the shift register is ready to send a new frame. The shift register is loaded with the new data if it is in idle state or immediately after the last stop bit of the previous frame is transmitted. When the shift register is loaded to the new data, it will transfer one complete frame according to the settings of the control registers. If 9-bit characters are used in the Asynchronous or the Synchronous operation mode, the 9th bit must be written to USTnTX8 bit in USARTn_CR2 register before it is loaded to the transmit buffer (USARTn_DR register). (n = 10 and 11)

14.4.6.2 UART transmitter flag and interrupt

The UART transmitter has two flags that indicate its state. One is USART data register empty flag (DREn) and the other is transmit completion flag (TXCn). Both flags can be used as interrupt sources.

DREn flag indicates whether the transmit buffer is ready to receive new data. This bit is set when the transmit buffer is empty and cleared when the transmit buffer contains data to be transmitted but has not yet been moved into the shift register.

When the data register empty interrupt enable (DRIEn) bit in USARTnCR1 register is set and the global interrupt is enabled, USARTn_ST status register empty interrupt is generated while DREn flag is set.

Transmit complete (TXCn) flag bit is set when the entire frame in the transmit shift register has been shifted out. The TXCn flag can be cleared by writing '1' to TXCn bit in the USARTn_ST register.

When transmit complete interrupt enable (TXCIEn) bit in the USARTn_CR1 register is set and the global interrupt is enabled, UART transmit complete interrupt is generated while TXCn flag is set. (n = 10 and 11)

14.4.6.3 UART parity generator

The parity generator calculates the parity bit for the serial frame data to be sent. When parity bit is enabled (USTnP1=1), the transmitter control logic inserts the parity bit between the MSB and the first stop bit of the frame to be sent. (n = 10 and 11)

14.4.6.4 UART disabling transmitter

Disabling the transmitter by clearing the TXEn bit will not become effective until the current transmission is completed. When the transmitter is disabled, the TXDn pin can be used as a normal general purpose I/O (GPIO). (n = 10 and 11)

14.4.7 UART receiver

The UART receiver is enabled by setting RXEn bit in the USARTn_CR1 register. When the receiver is enabled, the RXDn pin should be set to RXDn function for the serial input pin in the UART mode by the GPIO registers. Baud-rate, operation mode and frame format must be set before serial reception. In Synchronous or SPI operation mode, the SCKn pin is used as a transfer clock input, so it should be selected to do SCKn function by the GPIO registers. (n = 10 and 11)

14.4.7.1 UART receiving RX data

When the UART is in Synchronous mode or in Asynchronous mode, the receiver starts data reception if it detects a valid start bit (LOW) on RXDn pin. Each bit after the start bit is sampled at predefined baud-rate (asynchronous) or at sampling edge of SCKn (synchronous), and shifted into the receive shift register until the first stop bit of a frame is received. Even if there is a second stop bit in the frame, the second stop bit is ignored by the receiver. That is, receiving the first stop bit means that a complete serial frame is presented in the receiver shift register and contents of the shift register are to be moved into the receive buffer. The receive buffer is read by reading the USARTn_DR register.

If 9-bit characters are used (USTnS[2:0] = "111"), the ninth bit is stored in the USTnRX8 bit position in the USARTn_CR2 register. The ninth bit must be read from the USTnRX8 bit before reading the low 8 bits from the USARTn_DR register. Likewise, the error flags, FEn, DORn, and PEn, must be read before reading the data from USARTn_DR register. It is because error flags are stored in the same FIFO position of the receive buffer. (n = 10 and 11)

14.4.7.2 UART receiver Flag and interrupt

The UART receiver has a flag that indicates the receiver's state. The receive complete (RXCn) flag indicates whether there are unread data in the receive buffer. This flag is set when there is unread data in the receive buffer and cleared when the receive buffer is empty. If the receiver is disabled (RXEn=0), the receiver buffer is flushed and the RXCn flag is cleared.

When the receive complete interrupt enable (RXCIEn) bit in the USARTn_CR1 register is set and global interrupt is enabled, the UART receiver complete interrupt is generated while RXCn flag is set.

The UART receiver has three error flags, which are frame error (FEn), data overrun (DORn) and parity error (PEn). These error flags can be read from the USARTn_ST register. As received data are stored in the 2-level receive buffer, these error flags are also stored in the same position of receive buffer. Therefore, before reading received data from USARTn_DR register, USARTn_ST register should be read first, which contains error flags.

The frame error (FEn) flag indicates state of the first stop bit. The FEn flag is '0' when the stop bit was correctly detected as '1', while the FEn flag is '1' when the stop bit was incorrect, i.e. detected as '0'. This flag can be used for detecting out-of-sync conditions between data frames.

The data overrun (DORn) flag indicates data loss due to a full receive buffer condition. DORn occurs when the receive buffer is full, and another new data is presented in the receive shift register to be stored into the receive buffer. After the DORn flag is set, all the incoming data are lost. To avoid data loss or to clear this flag, receive buffer must be read.

The parity error (PEn) flag indicates that the frame in the receive buffer had a parity error during reception. If parity check function is not enabled (USTnP1=0), the PEn bit is always read as '0'. (n = 10 and 11)

14.4.7.3 UART parity checker

If parity bit is enabled (USTnP1=1), the parity checker calculates the parity of the data bits in incoming frame and compares the result with the parity bit from the received serial frame. (n = 10 and 11)

14.4.7.4 UART disabling receiver

Unlike the transmitter, the receiver becomes inactive immediately after it is disabled by clearing RXEn bit. When the receiver is disabled, the receiver flushes the receive buffer, the remaining data in the buffer is all reset, and the RXDn pin can be used as a normal general purpose I/O (GPIO). (n = 10 and 11)

14.4.7.5 Asynchronous data reception

To receive asynchronous data frame, the USART includes a clock and data recovery unit. The clock recovery logic is used for synchronizing the internally generated baud-rate clock to the incoming asynchronous serial frame on the RXDn pin. The data recovery logic samples and filters the incoming bits with a low pass filter, and removes the noise of RXDn pin.

Figure 81 illustrates the sampling process of the start bit of an incoming frame. The sampling rate is 16 times the baud-rate in normal mode and 8 times the baud-rate for double speed mode (DBLSn=1). The horizontal arrows show the synchronization variation due to the asynchronous sampling process. Note that larger time variation is seen using the double speed mode. (n = 10 and 11)

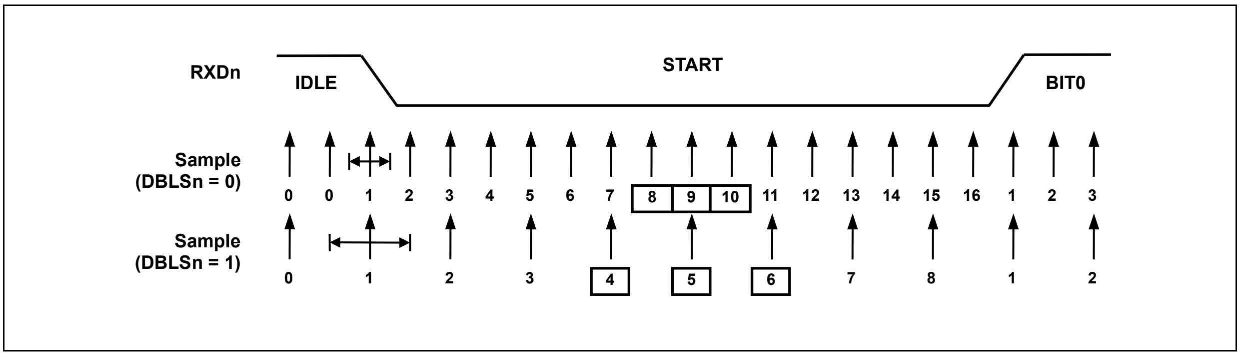


Figure 81. Asynchronous Start Bit Sampling (n = 10 and 11)

When the receiver is enabled (RXEn=1), the clock recovery logic tries to find a high-to-low transition on the RXDn line, which is the start bit condition. After detecting the high-to-low transition on RXDn line, the clock recovery logic uses samples 8, 9 and 10 for normal mode to detect whether valid start bit is received. If more than 2 samples have logical low level, it is considered that a valid start bit is detected and the internally generated clock is synchronized to the incoming data frame. Then the data recovery can begin. The synchronization process is repeated for each start bit.

As described above, when the receiver clock is synchronized to the start bit, the data recovery can begin. Data recovery process is almost the same as clock recovery process.

The data recovery logic samples each incoming bit 16 times for normal mode and 8 times for double speed mode, and uses sample 8, 9 and 10 to decide data value. If more than 2 samples have low levels, the received bit is considered as a logic '0' and if more than 2 samples have high levels, the received bit is considered as a logic '1'. The data recovery process is then repeated until a complete frame is received, including the first stop bit. The decided bit value is stored in the receive shift register in order. Note that the Receiver only uses the first stop bit of a frame. Internally, after receiving the first stop bit, the receiver is in idle state and waits to find the start bit. (n = 10 and 11)

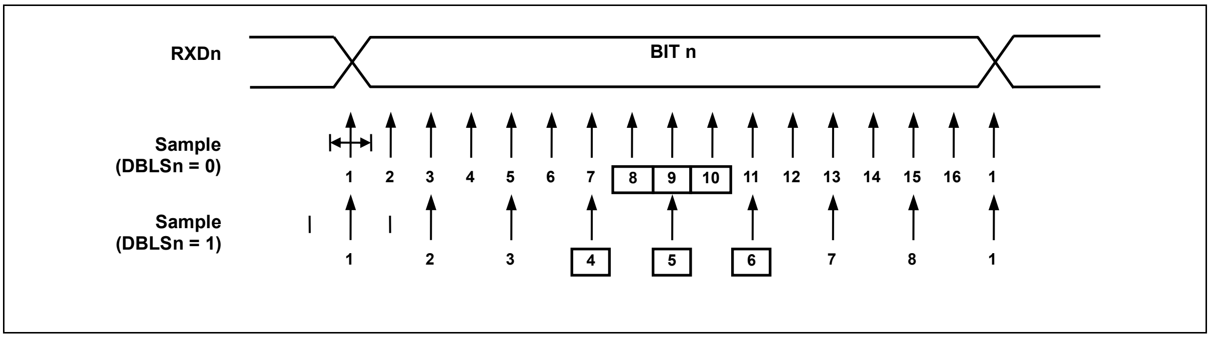


Figure 82. Asynchronous Sampling of Data and Parity Bit (n = 10 and 11)

The process for detecting stop bit is the same as clock and data recovery process. That is, if 2 or more samples of 3 center values have high level, correct stop bit is detected, or else a frame error (FEn) flag is set. After deciding whether the first stop bit is valid or not, the receiver goes to idle state and monitors the RXDn line to check whether a valid high to low transition is detected (start bit detection). (n = 10 and 11)

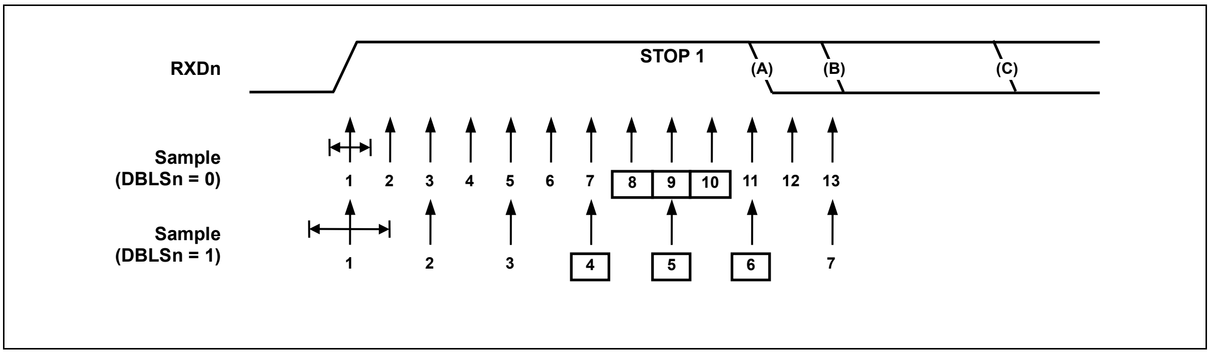


Figure 83. Stop Bit Sampling and Next Start Bit Sampling (n = 10 and 11)

14.4.8 SPI mode

The USART can be set to operate in industrial standard SPI compliant mode. The SPI mode has the following features

- Full Duplex, Three-wire synchronous data transfer.
- Mater and Slave Operation.
- Supports all four SPI modes of operation (mode 0, 1, 2, and 3).
- Selectable LSB first or MSB first data transfer.
- Double buffered transmit and receive.
- Programmable transmit bit rate.

When the SPI mode is enabled by configuring USTnMS[1:0] as ”11”, the slave select (SSn) pin becomes active LOW input in Slave mode operation if USTnSSEN bit is set to ‘1’. The SSn function is not automatically controlled in master mode operation even if USTnSSEN bit is set to ‘1’.

Note that during SPI mode of operation, the pin RXDn is renamed as MISOn and TXDn is renamed as MOSIn for compatibility to other SPI devices. (n = 10 and 11)

14.4.9 SPI clock formats and timing

To accommodate a wide variety of synchronous serial peripherals from different manufacturers, the USART has a clock polarity bit (CPOLn) and a clock phase control bit (CPHAn) to select one of four clock formats for data transfers. CPOLn selectively inserts an inverter in series with the clock. CPHAn chooses between two different clock phase relationships between the clock and data. Note that CPHAn and CPOLn bits in USTnCR0 register have different meanings according to the USTnMS[1:0] bits, which decide the operating mode of USART.

Table 59 shows four combinations of CPOLn and CPHAn for SPI mode 0, 1, 2, and 3. (n = 10 and 11)

Table 59. CPOL Functionality (n = 10 and 11)

SPIn Mode	CPOLn	CPHAn	Leading Edge	Trailing Edge
0	0	0	Sample (Rising)	Setup (Falling)
1	0	1	Setup (Rising)	Sample (Falling)
2	1	0	Sample (Falling)	Setup (Rising)
3	1	1	Setup (Falling)	Sample (Rising)

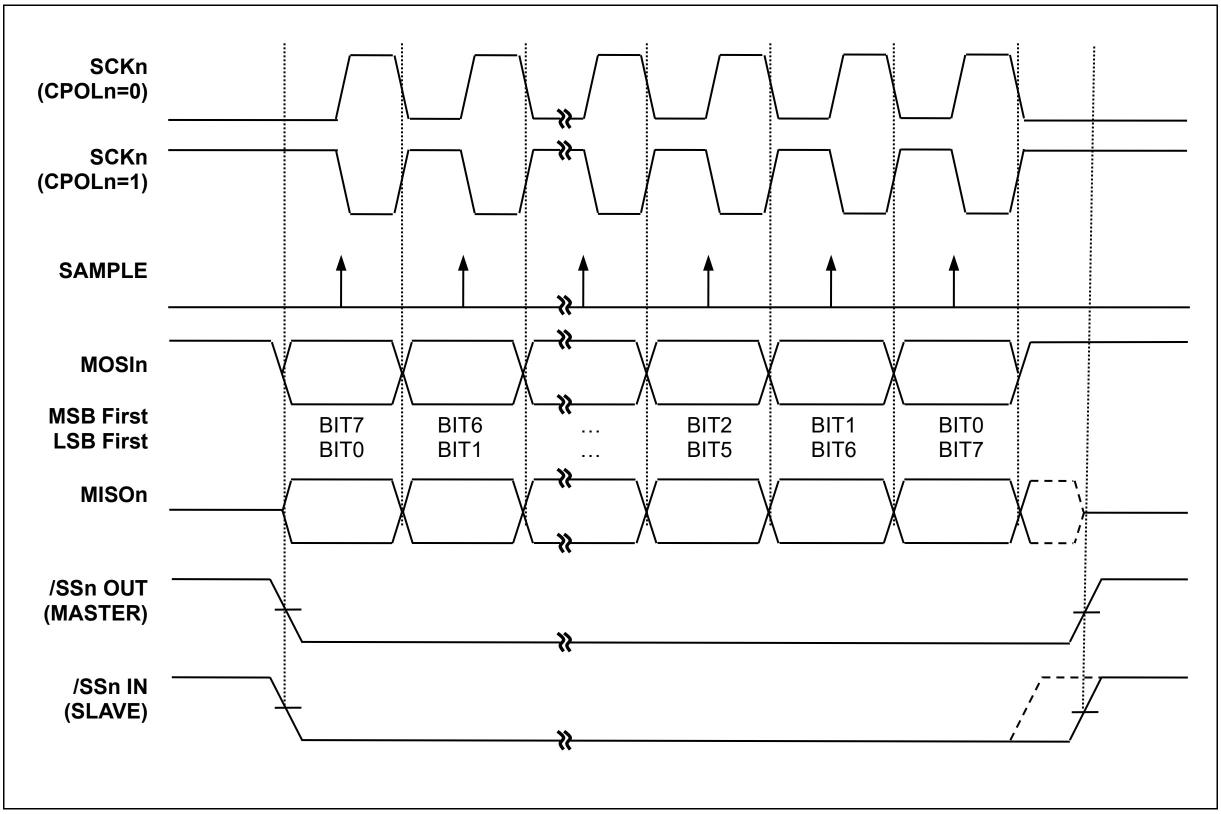


Figure 84. USART SPIn Clock Formats when CPHAn=0 (n = 10 and 11)

When CPHAn=0, the slave begins to drive its MISOn output with the first data bit value when SSn goes to active low. The first SCKn edge causes both the master and the slave to sample the data bit value on their MISOn and MOSIn inputs, respectively. At the second SCKn edge, the USART shifts the second data bit value out to the MOSIn and MISOn outputs of the master and slave, respectively. Unlike the case of CPHAn=1, when CPHAn=0, the slave's SSn input must go to its inactive high level between transfers. This is because the slave can prepare the first data bit when it detects falling edge of SSn input. (n = 10 and 11)

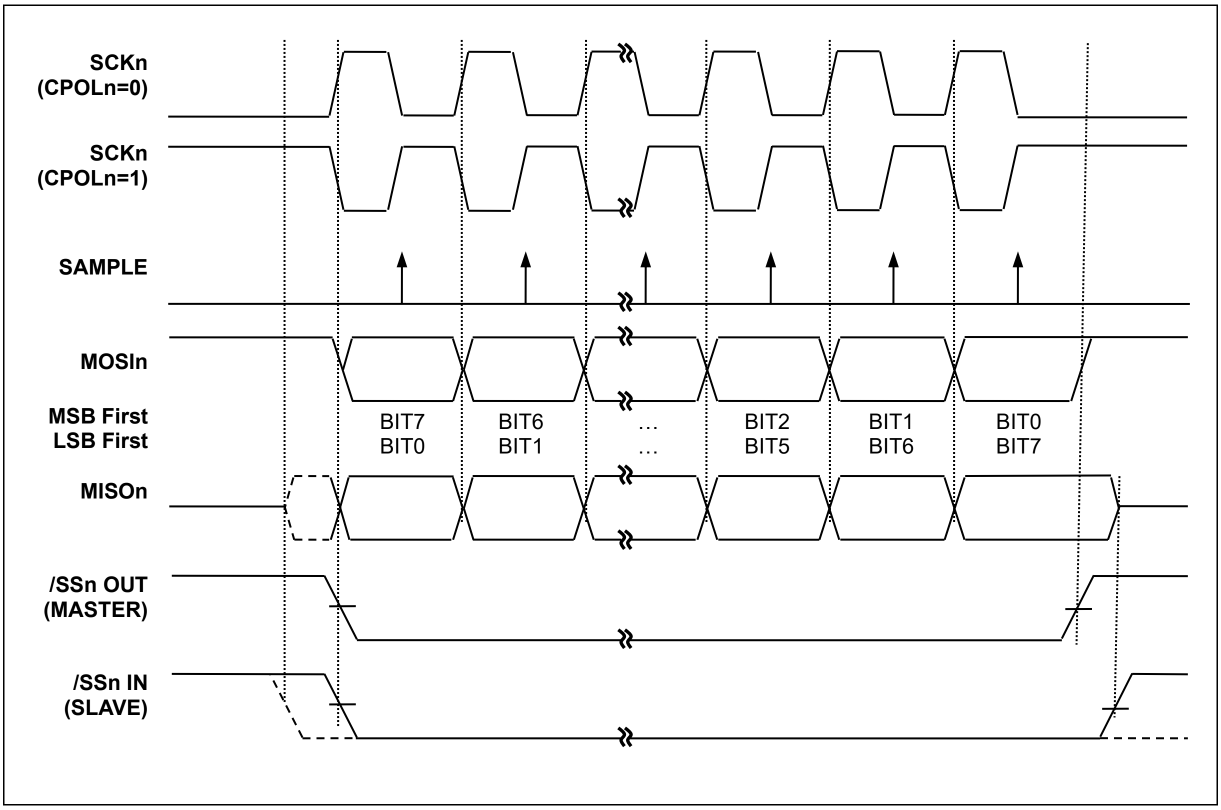


Figure 85. USART SPIn Clock Formats when CPHAn=1 (n = 10 and 11)

When CPHAn=1, the slave begins to drive its MISOn output when SSn goes active low, but the data is not defined until the first SCKn edge. The first SCKn edge shifts the first bit of data from the shifter onto the MOSIn output of the master and the MISOn output of the slave. The next SCKn edge causes both the master and slave to sample the data bit value on their MISOn and MOSIn inputs, respectively. At the third SCKn edge, the USART shifts the second data bit value out to the MOSIn and MISOn output of the master and slave respectively. When CPHAn=1, the slave's SSn input is not required to go to its inactive high level between transfers.

Because the SPIn logic reuses USART resources, SPIn mode of operation is similar to that of synchronous or asynchronous operation. A SPIn transfer is initiated by checking for the USART Data Register Empty flag (DREn=1) and then writing a byte of data to the USARTn_DR Register. In master mode of operation, even when transmission is not enabled (TXEn=0), writing data to the USARTn_DR register is necessary because the clock SCKn is generated from the transmitter block.

15 UART 0/1

There are built-in 2-channel of UART module (Universal Asynchronous Receiver/Transmitter) in A31G11x series. UART operation status including error status can be read from a status register.

A prescaler, which generates proper baud rate, exists for each UART channel. The prescaler can divide the UART clock source, PCLK, from 3 to 65535. Then, baud rate is generated using a 1:16 clock and an 8-bit precision clock tuning function.

The UART 0/1 of A31G11x series features the followings:

- Compatible with 16450
- Configurable standard asynchronous control bit (start, stop, and parity)
- Programmable 16-bit fractional baud generator
- Programmable serial communication
- 5-, 6-, 7- or 8- bit data transfer
- Even, odd, or no-parity bit insertion and detection
- 1-, 1.5- or 2-stop bit-insertion and detection
- 16-bit baud rate generation with 8-bit fraction control
- Hardware inter-frame delay function
- Stop bit error detection
- Detail status register

15.1 UART 0/1 block diagram

Figure 86 shows a block diagram of the UART block.

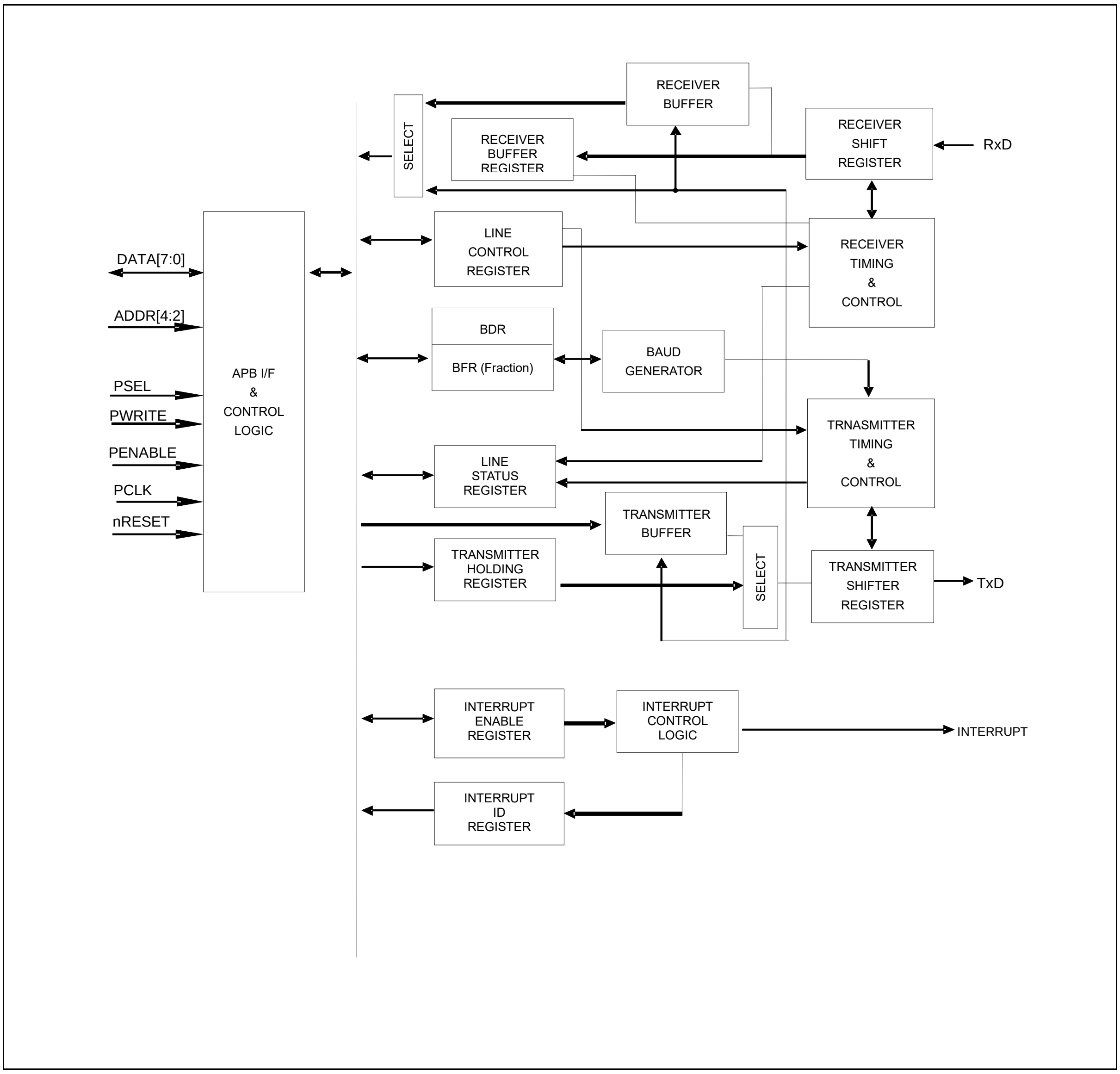


Figure 86. UART 0/1 Block Diagram

15.2 Pin description for UART 0/1

Table 60. Pins and External Signals for UART 0/1

PIN NAME	TYPE	DESCRIPTION
TXD0	O	UART Channel 0 transmit output
RXD0	I	UART Channel 0 receive input
TXD1	O	UART Channel 1 transmit output
RXD1	I	UART Channel 1 receive input

15.3 Registers

Base address and register map of the UART are shown in Table 61 and Table 62.

Table 61. Base Address of UART

Name	Base address	Size	Description
UART0	0x4000_4000	256	UART0 Block
UART1	0x4000_4100	256	UART1 Block

Table 62. UART n Register Map (n = 0 and 1)

Name	Offset	Type	Description	Reset value
UARTn_RBR	0x00	RO	UARTn Receive Data Buffer Register	0x00000000
UARTn_THR	0x00	WO	UARTn Transmit Data Hold Register	0x00000000
UARTn_IER	0x04	RW	UARTn Interrupt Enable Register	0x00000000
UARTn_IIR	0x08	RO	UARTn Interrupt ID Register	0x00000001
UARTn_LCR	0x0C	RW	UARTn Line Control Register	0x00000000
UARTn_DCR	0x10	RW	UARTn Data Control Register	0x00000000
UARTn_LSR	0x14	RO	UARTn Line Status Register	0x00000060
UARTn_BDR	0x20	RW	UARTn Baud Rate Divisor Latch Register	0x00000000
UARTn_BFR	0x24	RW	UARTn Baud Rate Fractional Counter Value	0x00000000
UARTn_IDTR	0x30	RW	UARTn Inter-frame Delay Time Register	0x000000C0

15.3.1 UARTn_RBR: UARTn receive data buffer register

Received data will be read from UARTn_RBR register. The maximum length of data is 8 bits. The last data received will stay in this register until a new byte is received.

UARTn_RBR register is 32-bit size and accessible in 32/16/8-bit. (n = 0 and 1)

UART0_RBR=0x4000_4000, UART1_RBR=0x4000_4100

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	**7 6 5 4 3 2 1 0**
Reserved	**RBR**
0x000000	**0x00**
-	**RO**

7 0	RBR	UARTn Receive Data Buffer.

15.3.2 UARTn_THR: UARTn transmit data hold register

UARTn_THR register is 32-bit size and accessible in 32/16/8-bit. (n = 0 and 1)

UART0_THR=0x4000_4000, UART1_THR=0x4000_4100

31 … 8	7 … 0
Reserved	**THR**
0x000000	**0x00**
-	**WO**

7 0	THR	UARTn Transmit Data Hold.

15.3.3 UARTn_IER: UARTn interrupt enable register

UARTn_IER register is 32-bit size and accessible in 32/16/8-bit. (n = 0 and 1)

UART0_IER=0x4000_4004, UART1_IER=0x4000_4104

31 … 4	3	2	1	0
Reserved	**TXEIE**	**RLSIE**	**THREIE**	**DRIE**
0x0000000	**0**	**0**	**0**	**0**
-	**RW**	**RW**	**RW**	**RW**

3	TXEIE	Transmit Register Empty Interrupt Enable.	
		0	Disable transmit register empty interrupt.
		1	Enable transmit register empty interrupt.
2	RLSIE	Receiver Line Status Interrupt Enable.	
		0	Disable receiver line status interrupt.
		1	Enable receiver line status interrupt.
1	THREIE	Transmit Holding Register Empty Interrupt Enable.	
		0	Disable transmit hold register empty interrupt.
		1	Enable transmit hold register empty interrupt.
0	DRIE	Data Receive Interrupt Enable.	
		0	Disable data receive interrupt.
		1	Enable data receive interrupt.

15.3.4 UARTn_IIR: UARTn interrupt ID register

UARTn_IIR register is 32-bit size and accessible in 32/16/8-bit. (n = 0 and 1)

UART0_IIR=0x4000_4008, UART1_IIR=0x4000_4108

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																											**TXE**	**Reserved**	**IID**		**IPEN**
0x000000																											**0**	**0**	**00**		**1**
-																											**RO**	-	**RO**		**RO**

4	TXE	Transmit Complete Interrupt Source ID.
2 1	IID	UARTn Interrupt ID. **NOTE**: The UARTn supports 3-priority interrupt generation and the interrupt source ID register shows one interrupt source which has highest priority among pending interrupts. The priority is defined as below. — Receive line status interrupt. — Receive data ready interrupt and Character timeout interrupt. — Transmit hold register empty interrupt.
0	IPEN	Interrupt Pending. 0 Interrupt is pending. 1 No interrupt is pending.

Table 63. Interrupt ID and Control of UARTn_IIR

Priority	TXE	IID		IPEN	Interrupt sources		
	Bit 4	**Bit 2**	**Bit 1**	**Bit 0**	**Interrupt**	**Interrupt condition**	**Interrupt clear**
-	0	0	0	1	None	-	-
1	0	1	1	0	Receiver Line Status	Overrun, Parity, Framing or Break Error	Read LSR register
2	0	1	0	0	Receiver Data Available	Receive data is available.	Read receive register or read IIR register
3	0	0	1	0	Transmitter Holding Register Empty	Transmit buffer empty	Write transmit hold register or read IIR register
4	1	X	X	X	Transmitter Register Empty	Transmit register empty	Write transmit hold register or read IIR register

NOTE: After check the above bits, Read data buffer to avoid losing interrupt source.

15.3.5 UARTn_LCR: UARTn line control register

UARTn_LCR register is 32-bit size and accessible in 32/16/8-bit. (n = 0 and 1)

UART0_LCR=0x4000_400C, UART1_LCR=0x4000_410C

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7	6	5	4	3	2	1 0
Reserved	**BREAK**	**STICKP**	**PARITY**	**PEN**	**STOPBIT**	**DLEN**
0x000000	**0**	**0**	**0**	**0**	**0**	**00**
-	**RW**	**RW**	**RW**	**RW**	**RW**	**RW**

6	BREAK	Transfer Break Control. The TXDn pin will be driven at low state to notice the alert to the receiver.	
		0	Normal transfer mode.
		1	Break transmit mode.
5	STICKP	Force Parity. This bit is effective when the PEN bit is set to '1'.	
		0	Disable parity stuck.
		1	Enable parity stuck. A parity is always the value of the PARITY bit.
4	PARITY	Parity Mode and Parity Stuck Selection.	
		0	Odd parity mode.
		1	Even parity mode.
3	PEN	Parity Bit Transfer Enable.	
		0	Disable parity transfer.
		1	Enable parity transfer.
2	STOPBIT	Stop Bit Length Selection.	
		0	1 stop bit.
		1	1.5 or 2 stop bit. 1.5 stop bit in case of 5-bit data and 2 stop bit in case of 6/7/8-bit data.
1 0	DLEN	Data Length Selection.	
		00	5-bit data length
		01	6-bit data length
		10	7-bit data length
		11	8-bit data length

Parity bit will be generated according to bit 3,4,5 of UARTn_LCR register. Table 64 shows the variation of parity bit generation.

Table 64. Interrupt ID and control of UARTn_LCR

STICKP	PARITY	PEN	Parity
X	X	0	No Parity
0	0	1	Odd Parity
0	1	1	Even Parity
1	0	1	Force parity as '1'
1	1	1	Force parity as '0'

15.3.6 UARTn_DCR: UARTn data control register

UARTn_DCR register is 32-bit size and accessible in 32/16/8-bit. (n = 0 and 1)

UART0_DCR=0x4000_4010, UART1_DCR=0x4000_4110

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																											**LBON**	**RXINV**	**TXINV**	**Reserved**	
0x000000																											**0**	**0**	**0**	**00**	
-																											**RW**	**RW**	**RW**	**-**	

4	LBON	Local Loopback Test Mode Enable.	
		0	Normal mode.
		1	Local loopback mode. TXDn connected to RXDn internally.
3	RXINV	Receive Data Inversion Selection.	
		0	Normal receive data input.
		1	Inverted receive data input.
2	TXINV	Transmit Data Inversion Selection.	
		0	Normal transmit output.
		1	Inverted transmit output.

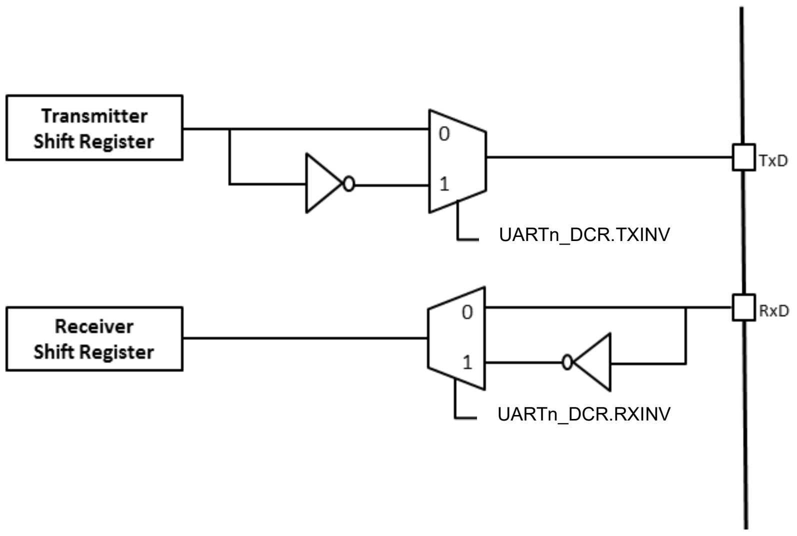


Figure 87. Data Inversion Control Diagram

15.3.7 UARTn_LSR: UARTn line status register

UARTn_LSR register is 32-bit size and accessible in 32/16/8-bit. (n = 0 and 1)

UART0_LSR=0x4000_4014, UART1_LSR=0x4000_4114

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="25">Reserved</td><td>TEMT</td><td>THRE</td><td>BI</td><td>FE</td><td>PE</td><td>OE</td><td>DR</td></tr>
<tr><td colspan="25">0x000000</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="25">-</td><td>RO</td><td>RO</td><td>RO</td><td>RO</td><td>RO</td><td>RO</td><td>RO</td></tr>
</table>

6	TEMT	Transmit Empty.	
		0	Transmit register has data or is transmitting.
		1	Transmit register is empty.
5	THRE	Transmit Holding Empty.	
		0	Transmit hold register is not empty.
		1	Transmit hold register is empty
		NOTE: This bit will be set to '1' when it starts transmission.	
4	BI	Break Condition Indication.	
		0	Normal status.
		1	Break condition is detected.
3	FE	Frame Error Indicator.	
		0	No frame error.
		1	Frame error takes place. The receive character did not have a valid stop.
2	PE	Parity Error Indicator.	
		0	No parity error.
		1	Parity error takes place. The receive character does not have correct parity information.
1	OE	Overrun Error Indicator.	
		0	No overrun error.
		1	Overrun error takes place. Additional data arrived while RHR is full.
0	DR	Data Receive Indicator.	
		0	No data in receive hold register.
		1	Data has been received and is saved in the receive hold register.

This register provides the status of data transfers between transmitter and receiver. A user can check the line status from this register. Bit 1,2,3,4 will raise the line status interrupt when RLSIE bit in UARTn_IER register is set. Other bits can generate interrupts when their interrupt enable bits in UARTn_IER register are set.

15.3.8 UARTn_BDR: UARTn baud rate divisor latch register

UARTn_BDR register is 32-bit size and accessible in 32/16/8-bit. (n = 0 and 1)

UART0_BDR=0x4000_4020, UART1_BDR=0x4000_4120

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved		**BDR**	
0x0000		**0x0000**	
-		**RW**	

15 0	BDR	Baud Rate Divider Latch Value Baud rate = fUARTnCLK/(16 x BDR[15:0] x 2). NOTE: The UART block will not work if BDR[15:0] < 0x0003.

To establish communication with the UART channel, baud rate should be set properly. The programmable baud rate generator provides divider number from 3 to 65535. Expected baud rate should be written to the 16-bit divider register (UARTn_BDR). $UART_{clock}$ is PCLK.

Baud rate calculation formula is as follows:

$$\mathrm{BDR} = \frac{UART_{clock}}{16 \times BaudRate \times 2}$$

In case of 40MHz $UART_{clock}$ speed, the divider value and error rate is shown in table

Table 65. Example of Baud Rate Calculation (without BFR)

$UART_{clock}$= 40MHz		
Baud rate	**Divider**	**Error (%)**
1200	1041	0.06%
2400	520	0.16%
4800	260	0.16%
9600	130	0.16%
19200	65	0.16%
38400	32	1.73%
57600	21	3.34%
115200	10	8.51%

15.3.9 UARTn_BFR: UARTn baud rate fraction counter register

UARTn_BFR register is 32-bit size and accessible in 32/16/8-bit. (n = 0 and 1)

UART0_BFR=0x4000_4024, UART1_BFR=0x4000_4124

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved	**BFR**
0x000000	**0x00**
-	**RW**

7 0	BFR	Fraction Counter value.	
		0	Disable fraction counter.
		N	Fraction compensation mode under operation. Fraction counter is incremented by FCNT.
		NOTE: 8-bit fractional counter will count up by FCNT value every (baud rate)/16 period and whenever fractional counter overflow is happen, the divisor value will increment by 1. So this period will be compensated. Then next period, the divisor value will return to original set value.	

Table 66. Example of Baud Rate Calculation

UART$_{clock}$ = 40MHz			
Baud rate	**Divider**	**FCNT**	**Error (%)**
1200	1041	170	0.00%
2400	520	213	0.00%
4800	260	106	0.00%
9600	130	53	0.00%
19200	65	26	0.00%
38400	32	141	0.00%
57600	21	179	0.01%
115200	10	217	0.03%

$$\mathrm{FCNT} = \mathrm{Float} * 256$$

FCNT value can be calculated using the above equation. For example, when the target baud rate is 4800 bps and UART$_{clock}$ is 40MHz, the BDR value is 260.4167. The integer 260 is be the BDR value and floating number 0.4167 lead to an FNCT value as follows:

FCNT = 0.4167 * 256 = 106.6667, and thus the FCNT value is 106.

8-bit fractional counter will count up by FCNT value every (baud rate)/16 periods and whenever fractional counter overflow takes place, the divisor value will increment by 1 and compensate this period. Then, the divisor value will return to its original value.

15.3.10 UARTn_IDTR: UARTn inter-frame delay time register

UARTn_IDTR register is 32-bit size and accessible in 32/16/8-bit. (n = 0 and 1)

UART0_IDTR=0x4000_4030, UART1_IDTR=0x4000_4130

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								SMS	DMS	Reserved			WAITVAL		
0x000000																								1	1	000			000		
-																								RW	RW	-			RW		

7	SMS	Start Bit Multi Sampling Enable.	
		0	Multi sampling is disabled for start bit, Single sampling will be done at 8/16 baud rate for the start bit.
		1	Multi sampling is enabled for start bit. Sampling is done 3 times at 7/16, 8/16, and 9/16 baud rate. Dominant value among 3 samples will be selected for the start bit.
6	DMS	Data Bit Multi sampling enable.	
		0	Multi sampling is disabled for data bit, Single sampling will be done at 8/16 baud rate for the data bit.
		1	Multi sampling is enabled for data bit. Sampling is done 3 times at 7/16, 8/16, and 9/16 baud rate. Dominant value among 3 samples will be selected for the data bit.
2	WAITVAL	Wait Time Value. Dummy delay can be inserted between 2 Continuous Transmits.	
0		Wait Time = WAITVAL[2:0]/(Baud Rate)	

15.4 Functional description

The UART module is compatible with 16450 UART. Additionally, fractional baud rate compensation logic is provided. It does not have an internal FIFO block.

15.4.1 Receiver sampling timing

The UART of A31G11x series operates at the following timing as shown in Figure 88.

If falling edge is detected on the receive line, the UART considers it as a start bit. From then on, the UART oversamples 1-bit 16 times and detects the bit value at the 7th sample.

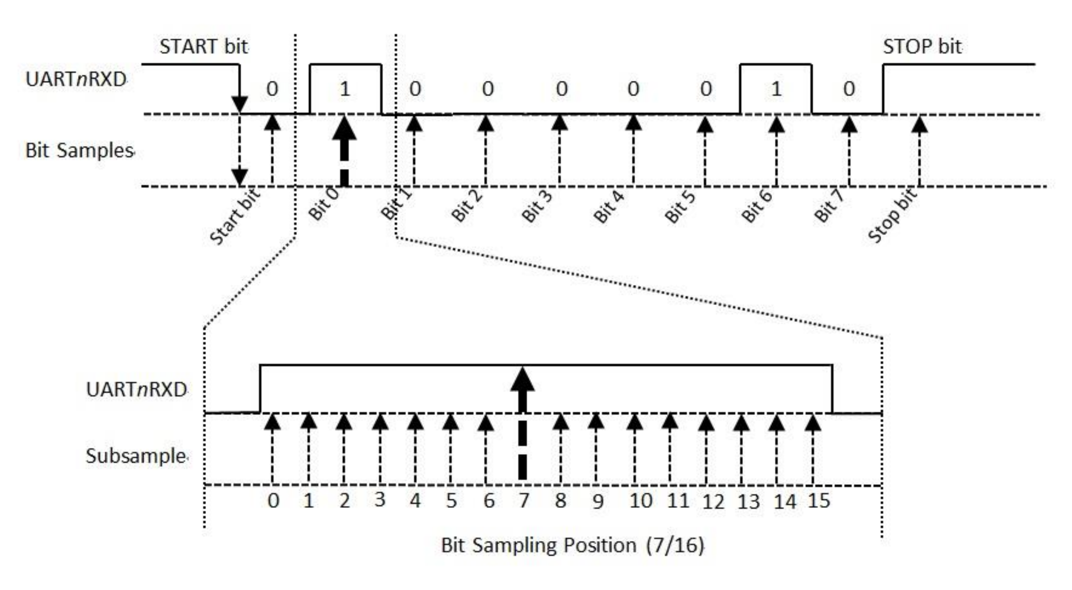


Figure 88. Sampling Timing of UART Receiver

It is recommended to enable debounce settings in the PCU block to enhance the immunity to external glitch noise.

15.4.2 Transmitter

The transmitter has a data transmission function. The start bit, data bits, optional parity bit, and stop bit shift in series, the least significant bit shifting first.

The number of data bit is selected in DLEN[1:0] in the UARTn_LCR register. The parity bit is set according to the PARITY and PEN bits in the UARTn_LCR register. If the parity type is even, the parity bit depends on one-bit sum of all data bits. For odd parity, the parity bit is an inverted sum of all data bits. The number of stop bits is selected in the STOPBIT in the UARTn_LCR register.

The example of transmission data format is introduced in Figure 89.

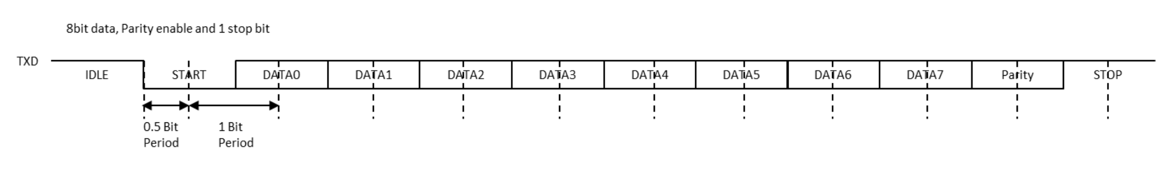


Figure 89. Transmission Data Format Example

15.4.3 Inter-frame delay transmission

The inter-frame delay function allows the transmitter to insert an idle state on the TXD line between 2 characters. The width of the idle state is defined in WAITVAL field of the UARTn_IDTR register. When this field is set as 0, no time-delay is generated. Otherwise, the transmitter holds a high level on TXD after each transmitted character during the number of bit periods defined in WAITVAL field.

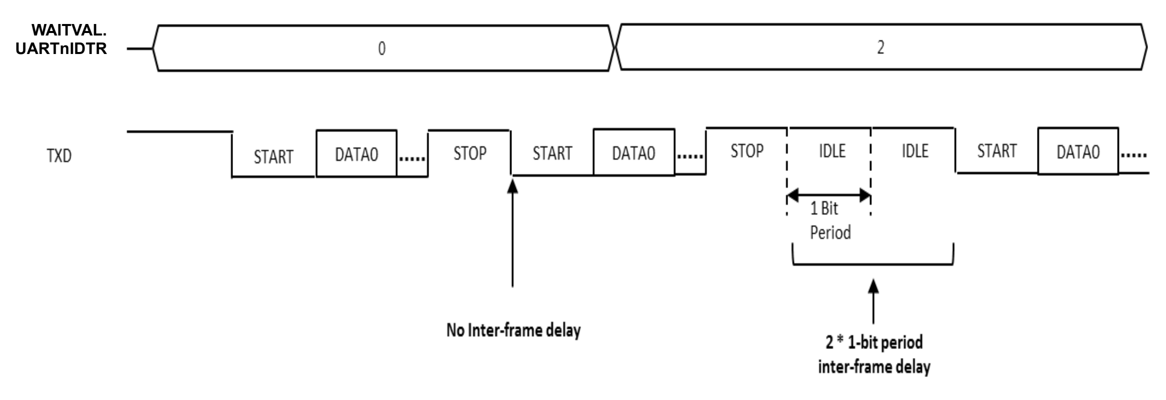


Figure 90. Inter-frame Delay Timing Diagram

15.4.4 Transmit interrupt

The transmission operation makes some kind of interrupt flags. When transmitter hold register is empty, the THRE interrupt flag will be raised. When transmitter shifter register is empty, the TXE interrupt flag will be raised. User can select an interrupt timing that works the best for the application.

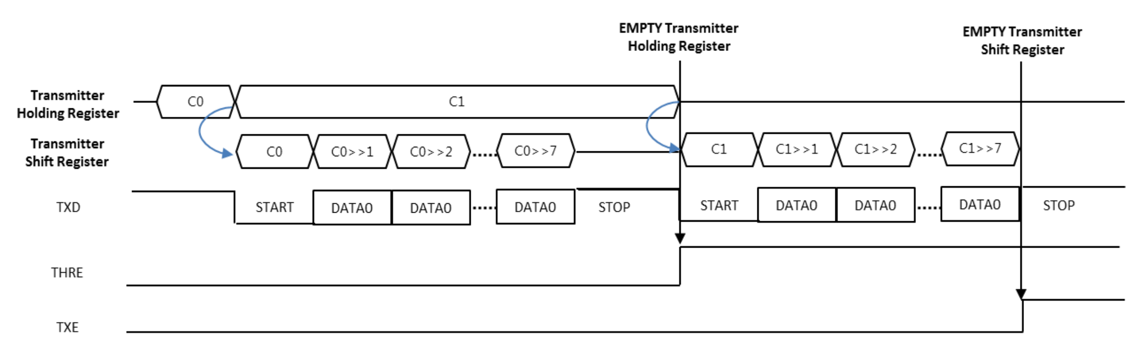


Figure 91. Transmit Interrupt Timing Diagram

16 I2C 0/1 interface

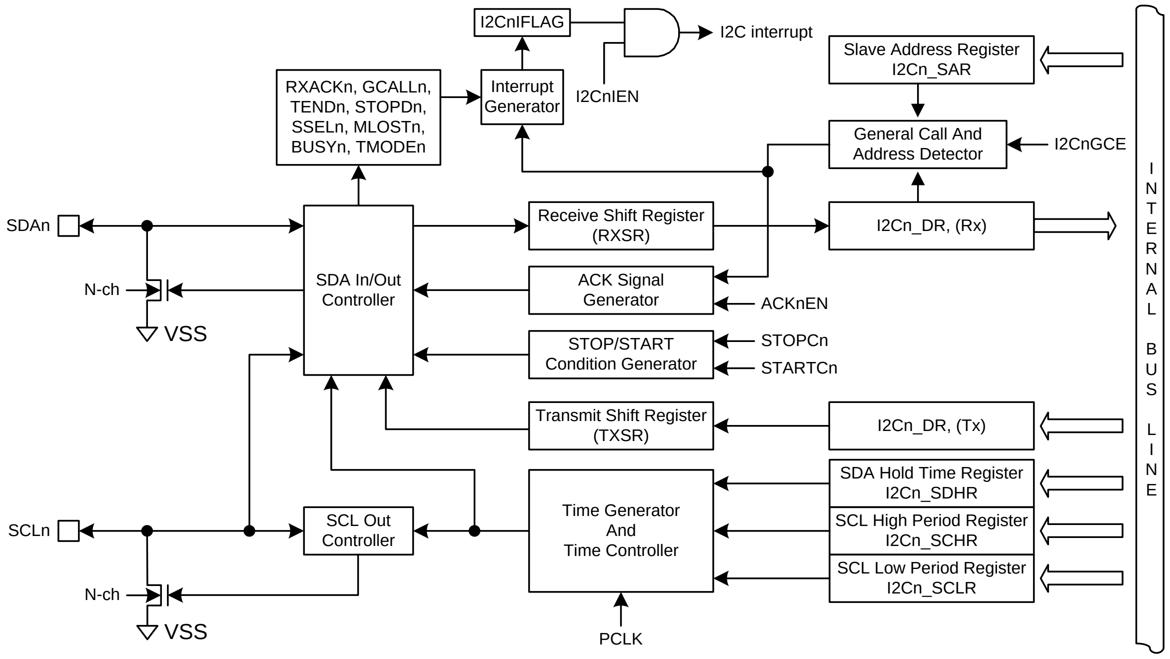
I2C is one of industrial standard serial communication protocols, which uses 2 bus lines, Serial Data Line (SDAn) and a Serial Clock Line (SCLn), to exchange data. Because both SDAn and SCLn lines are open-drain output, each line needs a pull-up resistor (n = 0 and 1).

The I2C 0/1 of A31G11x series features the followings:

- Compatible with I2C bus standard
- Multi-master operation
- Up to 1MHz data transfer read speed
- 7-bit address
- Support two slave addresses
- Both master and slave operation
- Bus busy detection

16.1 I2C 0/1 block diagram

Figure 92 shows a block diagram of the I2C block.



NOTE: When the corresponding port of I2C is a sub-function for SCLn/SDAn pin, the SCLn/SDAn pins are automatically set as N-channel open-drain outputs and the input latch is read when reading the pins. The corresponding pull-up resistor is determined by the control register.

Figure 92. I2C Block Diagram (n = 0 and 1)

16.2 Pin description for I2C 0/1

Table 67. Pins and External Signals for I2C (n = 0 and 1)

PIN NAME	TYPE	DESCRIPTION
SCLn	I/O	I2C channel n Serial clock bus line (open-drain)
SDAn	I/O	I2C channel n Serial data bus line (open-drain)

16.3 Registers

Base address and register map of the I2C 0/1 are shown in Table 68 and Table 69.

Table 68. Base Address of I2C Interface

Name	Base address	Size	Description
I2C0	0x4000_4800	256	I2C0 Block
I2C1	0x4000_4900	256	I2C1 Block

Table 69. I2C Register Map (n = 0 and 1)

Name	Offset	Type	Description	Reset Value
I2Cn_CR	0x00	RW	I2Cn Control Register	0x00000000
I2Cn_ST	0x04	RW	I2Cn Status Register	0x00000000
I2Cn_SAR1	0x08	RW	I2Cn Slave Address Register 1	0x00000000
I2Cn_SAR2	0x0C	RW	I2Cn Slave Address Register 2	0x00000000
I2Cn_DR	0x10	RW	I2Cn Data Register	0x00000000
I2Cn_SDHR	0x14	RW	I2Cn SDA Hold Time Register	0x00000001
I2Cn_SCLR	0x18	RW	I2Cn SCL Low Period Register	0x0000003F
I2Cn_SCHR	0x1C	RW	I2Cn SCL High Period Register	0x0000003F

16.3.1 I2Cn_CR: I2Cn control register

The register can be set to configure I2C operation mode activate I2C transactions.

I2Cn_CR register is 32-bit size and accessible in 32/16/8-bit. (n = 0 and 1)

I2C0_CR=0x4000_4800, I2C1_CR=0x4000_4900

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								**I2CnEN**	**TXDLYENBn**	**I2CnIEN**	**I2CnIFLAG**	**ACKnEN**	**IMASTERn**	**STOPCn**	**STARTCn**
0x000000																								**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
-																								**RW**	**RW**	**RW**	**RO**	**RW**	**RO**	**RW**	**RW**

7	I2CnEN	Activate I2Cn Block.	
		0	Disable I2Cn block.
		1	Enable I2Cn block.
6	TXDLYENBn	I2Cn_SDHR Register Control.	
		0	Enable I2Cn_SDHR register.
		1	Disable I2Cn_SDHR register.
5	I2CnIEN	I2Cn Interrupt Enable.	
		0	Disable I2Cn interrupt.
		1	Enable I2Cn interrupt.
4	I2CnIFLAG	I2Cn Interrupt Flag. This bit is cleared when all interrupt source bits in the I2Cn_ST register are cleared to '0'.	
		0	No request occurred.
		1	Request occurred.
3	ACKnEN	Controls ACK signal generation at ninth SCL period.	
		0	No ACK signal is generated. (SDA = 1)
		1	ACK signal is generated. (SDA = 0)
		NOTES: ACK signal is output (SDA = 0) for the following 3 cases. — When received address packet is equal to SLAn[6:0] bits in I2Cn_SAR1/I2Cn_SAR2 register. — When received address packet is equal to value 0x00 with GCALLn enabled. — When I2Cn operates as a receiver (master or slave)	
2	IMASTERn	Represents Operation Mode of I2Cn. This bit is cleared to '0' on STOP condition.	
		0	I2Cn is in slave mode.
		1	I2Cn is in master mode.
1	STOPCn	STOP Condition Generation When I2Cn is master.	
		0	No effect.
		1	Generate STOP condition.
0	STARTCn	START Condition Generation When I2Cn is master.	
		0	No effect.
		1	Generate START or Repeated START condition.

16.3.2 I2Cn_ST: I2Cn status register

I2Cn_ST register is 32-bit size and accessible in 32/16/8-bit. (n = 0 and 1)

I2C0_ST=0x4000_4804, I2C1_ST=0x4000_4904

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="24">Reserved</td><td>GCALLn</td><td>TENDn</td><td>STOPDn</td><td>SSELn</td><td>MLOSTn</td><td>BUSYn</td><td>TMODEn</td><td>RXACKn</td></tr>
<tr><td colspan="24">0x000000</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="24">-</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RO</td><td>RW</td></tr>
</table>

7	GCALLn		This bit has different meaning depending on whether I2C is master or slave. When I2C is a master, this bit represents whether it received AACK (address ACK) from slave.
		0	No AACK is received. (Master mode)
		1	AACK is received (Master mode). It may be set to '1' after address transmission.
			When I2C is a slave, this bit is used to indicate general call.
		0	General call address is not detected. (Slave mode)
		1	General call address is detected. (Slave mode)
6	TENDn		This bit is set when 1-byte of data is transferred completely.
		0	1 byte of data is not completely transferred.
		1	1 byte of data is completely transferred.
5	STOPDn		This bit is set when a STOP condition is detected.
		0	A STOP condition is not detected.
		1	A STOP condition is detected.
4	SSELn		This bit is set when I2C is addressed by other master.
		0	I2C is not selected as a slave.
		1	I2C is addressed by other master and acts as a slave.
3	MLOSTn		This bit represents the result of bus arbitration in master mode.
		0	I2C maintains bus mastership.
		1	I2C has lost bus mastership during arbitration process.
2	BUSYn		This bit reflects bus status.
		0	I2C bus is idle, so a master can issue a START condition.
		1	I2C bus is busy.
1	TMODEn		This bit is used to indicate whether I2C is transmitter or receiver.
		0	I2C is a receiver.
		1	I2C is a transmitter.
0	RXACKn		This bit shows the state of ACK signal.
		0	No ACK is received.
		1	ACK is received at ninth SCL period.

NOTES:

1. The GCALLn, TENDn, STOPDn, SSELn, and MLOSTn bits can be source of interrupt.
2. When an I2C interrupt occurs except for deep sleep mode, the SCL line is held low. To release SCL, Clear to "0b" all interrupt source bits in I2Cn_ST register.
3. The GCALLn, TENDn, STOPDn, SSELn, MLOSTn, and RXACKn bits are cleared when '1' is written to the corresponding bit.

16.3.3 I2Cn_SAR1: I2Cn slave address register 1

I2Cn_SAR1 register is 32-bit size and accessible in 32/16/8-bit. (n = 0 and 1)

I2C0_SAR1=0x4000_4808, I2C1_SAR1=0x4000_4908

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="24">Reserved</td><td colspan="7">SLAn</td><td>GCALLnEN</td></tr>
<tr><td colspan="24">0x000000</td><td colspan="7">0000000</td><td>0</td></tr>
<tr><td colspan="24">-</td><td colspan="7">RW</td><td>RW</td></tr>
</table>

7 1	SLAn	These bits configure the slave address 1 in slave mode.	
0	GCALLnEN	This bit decides whether I2Cn allows general call address or not in I2Cn slave mode.	
		0	Ignore general call address.
		1	Allow general call address.

16.3.4 I2Cn_SAR2: I2Cn slave address register 2

I2Cn_SAR2 register is 32-bit size and accessible in 32/16/8-bit. (n = 0 and 1)

I2C0_SAR2=0x4000_480C, I2C1_SAR2=0x4000_490C

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="24">Reserved</td><td colspan="7">SLAn</td><td>GCALLnEN</td></tr>
<tr><td colspan="24">0x000000</td><td colspan="7">0000000</td><td>0</td></tr>
<tr><td colspan="24">-</td><td colspan="7">RW</td><td>RW</td></tr>
</table>

7 1	SLAn	These bits configure the slave address 2 in slave mode.	
0	GCALLnEN	This bit decides whether I2Cn allows general call address or not in I2Cn slave mode.	
		0	Ignore general call address.
		1	Allow general call address.

16.3.5 I2Cn_DR: I2Cn data register

I2Cn_DR register is 32-bit size and accessible in 32/16/8-bit. (n = 0 and 1)

I2C0_DR=0x4000_4810, I2C1_DR=0x4000_4910

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="24">Reserved</td><td colspan="8">DATA</td></tr>
<tr><td colspan="24">0x000000</td><td colspan="8">0x00</td></tr>
<tr><td colspan="24">-</td><td colspan="8">RW</td></tr>
</table>

7 0	DATA	The I2Cn_DR Transmit buffer and Receive buffer share the same I/O address with this DATA register. The Transmit Data Buffer is the destination for data written to the I2Cn_DR register. Reading the I2Cn_DR register returns the contents of the Receive Buffer.

16.3.6 I2Cn_SDHR: I2Cn SDA hold time register

I2Cn_SDHR register is 32-bit size and accessible in 32/16/8-bit. (n = 0 and 1)

I2C0_SDHR=0x4000_4814, I2C1_SDHR=0x4000_4914

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="20">Reserved</td><td colspan="12">HLDT</td></tr>
<tr><td colspan="20">0x00000</td><td colspan="12">0x001</td></tr>
<tr><td colspan="20">-</td><td colspan="12">RW</td></tr>
</table>

11 0	HLDT	This register is used to control SDA output timing from the falling edge of SCL. Note that SDA is changed after tPCLK X (I2Cn_SDHR+2). In master mode, load half the value of I2Cn_SCLR to this register to make SDA switch in the middle of SCL. In slave mode, configure this register regarding the frequency of SCL from master. The SDA is changed after tPCLK X (I2Cn_SDHR+2) in master mode. So, to ensure proper operation in slave mode, the value tPCLK X (I2Cn_SDHR + 2) must be smaller than the period of SCL.

16.3.7 I2Cn_SCLR: I2Cn SCL low period register

I2Cn_SCLR register is 32-bit size and accessible in 32/16/8-bit. (n = 0 and 1)

I2C0_SCLR=0x4000_4818, I2C1_SCLR=0x4000_4918

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="20">Reserved</td><td colspan="12">SCLL</td></tr>
<tr><td colspan="20">0x00000</td><td colspan="12">0x03F</td></tr>
<tr><td colspan="20">-</td><td colspan="12">RW</td></tr>
</table>

11 0	SCLL	This register defines the low period of SCL in master mode. The base clock is PCLK and the period is calculated by the formula: tPCLK X (4 X I2Cn_SCLR + 2) where tPCLK is the period of PCLK.

16.3.8 I2Cn_SCHR: I2Cn SCL high period register

I2Cn_SCHR register is 32-bit size and accessible in 32/16/8-bit. (n = 0 and 1)

I2C0_SCHR=0x4000_481C, I2C1_SCHR=0x4000_491C

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="20">Reserved</td><td colspan="12">SCLH</td></tr>
<tr><td colspan="20">0x00000</td><td colspan="12">0x03F</td></tr>
<tr><td colspan="20">-</td><td colspan="12">RW</td></tr>
</table>

11 0	SCLH	This register defines the high period of SCL in master mode. The base clock is PCLK and the period is calculated by the formula: tPCLK X (4 X I2Cn_SCHR + 2) where tPCLK is the period of PCLK.

16.4 Functional description

16.4.1 I2C bit transfer

The data on the SDAn line must be stable during HIGH period of the clock, SCLn. The HIGH or LOW state of the data line can only change when the clock signal on the SCLn line is LOW. The exceptions are START(S), repeated START(Sr), and STOP(P) condition, where data line changes when clock line is high.

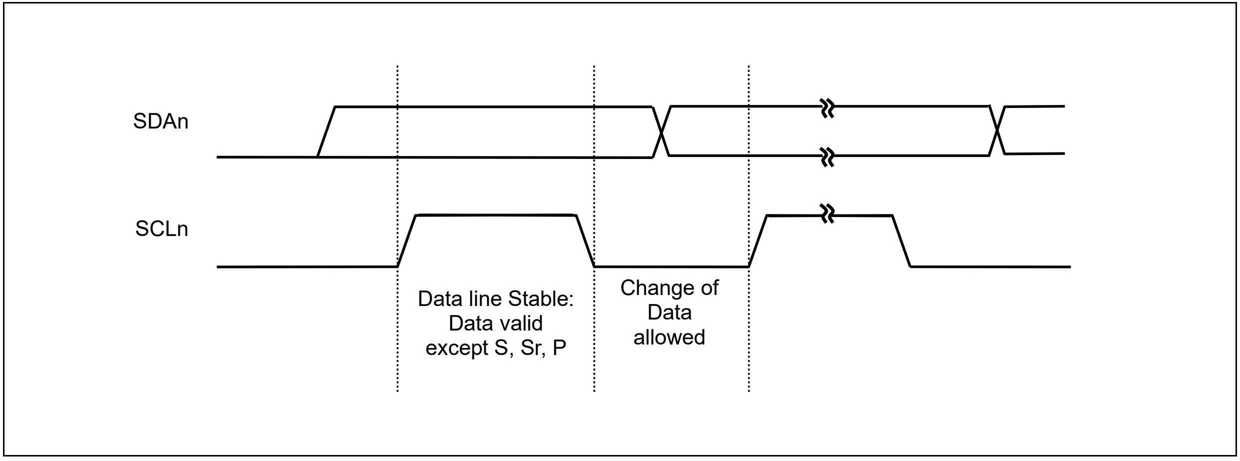


Figure 93. I2C Bus bit transfer (n = 0 and 1)

16.4.2 START/Repeated START/STOP

One master can issue a START (S) condition to detect other devices connected to the SCLn, SDAn lines that will use the bus. A STOP (P) condition is generated by the master to release the bus lines so that other devices can use it.

A high to low transition on the SDAn line while SCLn is high defines a START (S) condition.

A low to high transition on the SDAn line while SCLn is high defines a STOP (P) condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after START condition. The bus is considered to be free again after STOP condition, i.e., the bus is busy between START and STOP condition. If a repeated START condition (Sr) is generated instead of STOP condition, the bus stays in busy mode. So, the START and repeated START conditions are functionally identical.

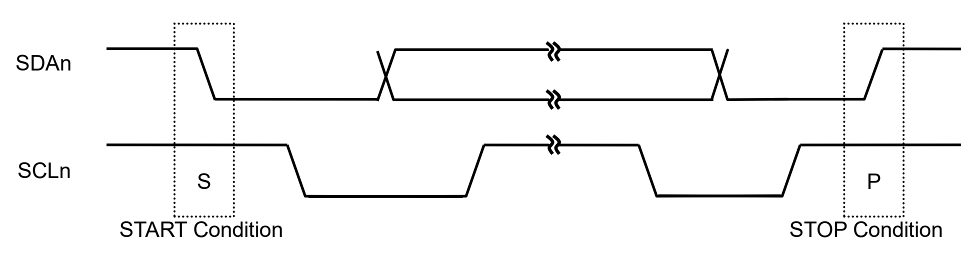


Figure 94. START and STOP condition (n = 0 and 1)

16.4.3 Data transfer

Every byte on the SDAn line must be 8-bits long, but the number of bytes that can be transmitted per transfer is unlimited. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCLn LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCLn.

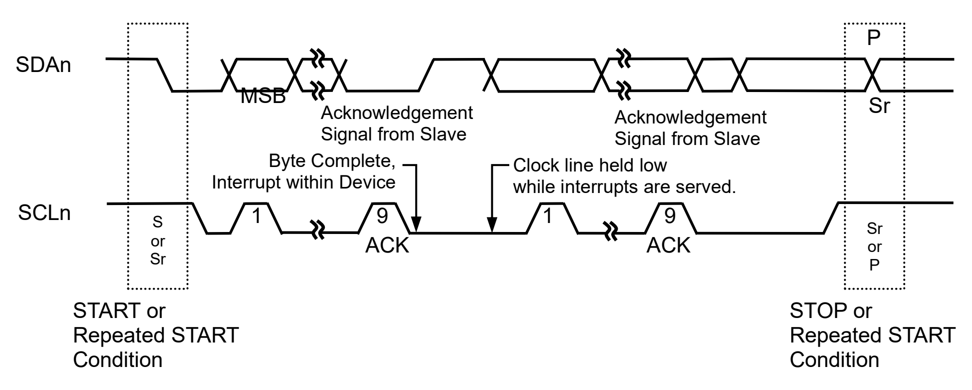


Figure 95. I2C Bus data transfer (n = 0 and 1)

16.4.4 Acknowledge

An acknowledge clock pulse is generated by the master. The transmitter releases the SDAn line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDAn line during the acknowledge clock pulse so that it remains stable at LOW during the HIGH period of this clock pulse. When a slave is addressed by a master (Address Packet), and if it is unable to receive or transmit because it is performing some real time function, the data line must be left HIGH by the slave. In addition, when a slave addressed by a master is unable to receive more data bits, the slave receiver must release the SDAn line (Data Packet). The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

If a master receiver is involved in a transfer, it must signal the end of data to the slave transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave transmitter must release the data line to allow the master to generate a STOP or repeated START condition.

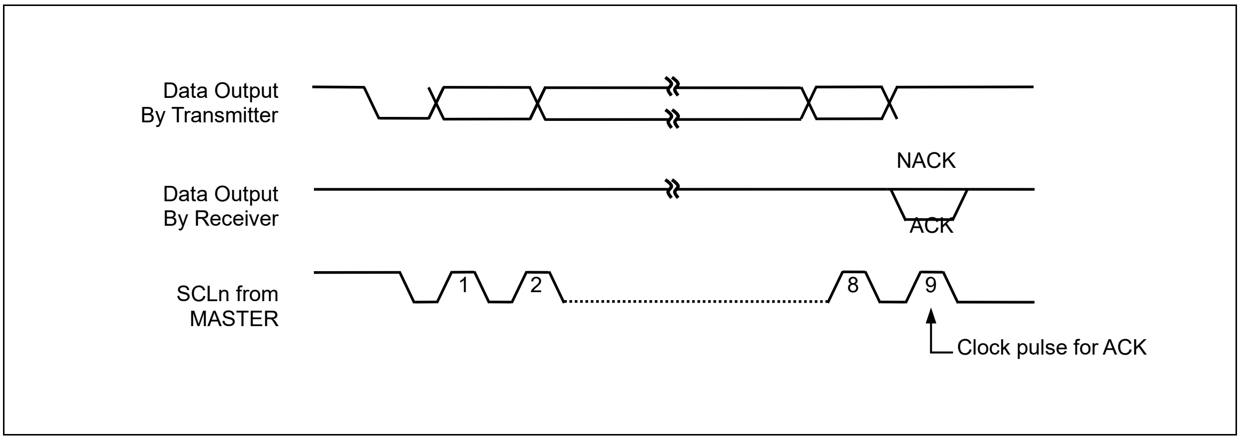


Figure 96. I2C bus acknowledge (n = 0 and 1)

16.4.5 Synchronization/ Arbitration

Clock synchronization is performed using the wired-AND connection of I2C interfaces to the SCLn line. This means that a HIGH to LOW transition on the SCLn line will cause the devices concerned to start counting off their LOW period and it will hold the SCLn line in that state until the clock HIGH state is reached. However the LOW to HIGH transition of this clock may not change the state of the SCLn line if another clock is still within its LOW period. In this way, a synchronized SCLn clock is generated with its LOW period determined by the device with the longest clock LOW period, and its HIGH period determined by the one with the shortest clock HIGH period.

A master may start a transfer only if the bus is free. Two or more masters may generate a START condition. Arbitration takes place on the SDAn line, while the SCLn line is at the HIGH level, in such a way that a master that transmits a HIGH level, while another master that transmits a LOW level, will switch off its DATA output state because the level on the bus does not correspond to its own level. Arbitration continues for many bits until a winning master gets the ownership of I2C bus. Its first stage is comparison of the address bits.

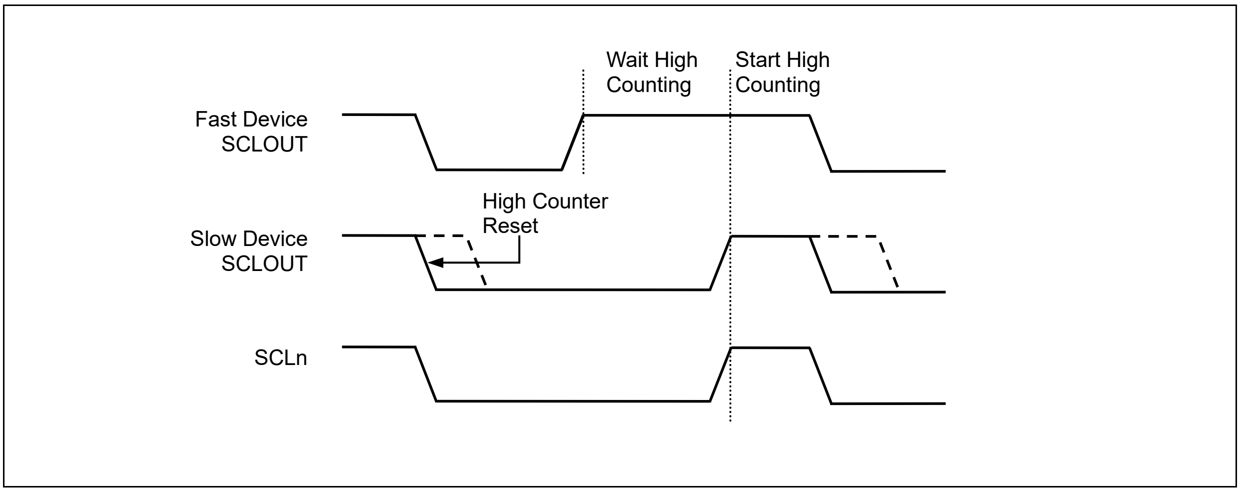


Figure 97. Clock synchronization during the arbitration procedure (n = 0 and 1)

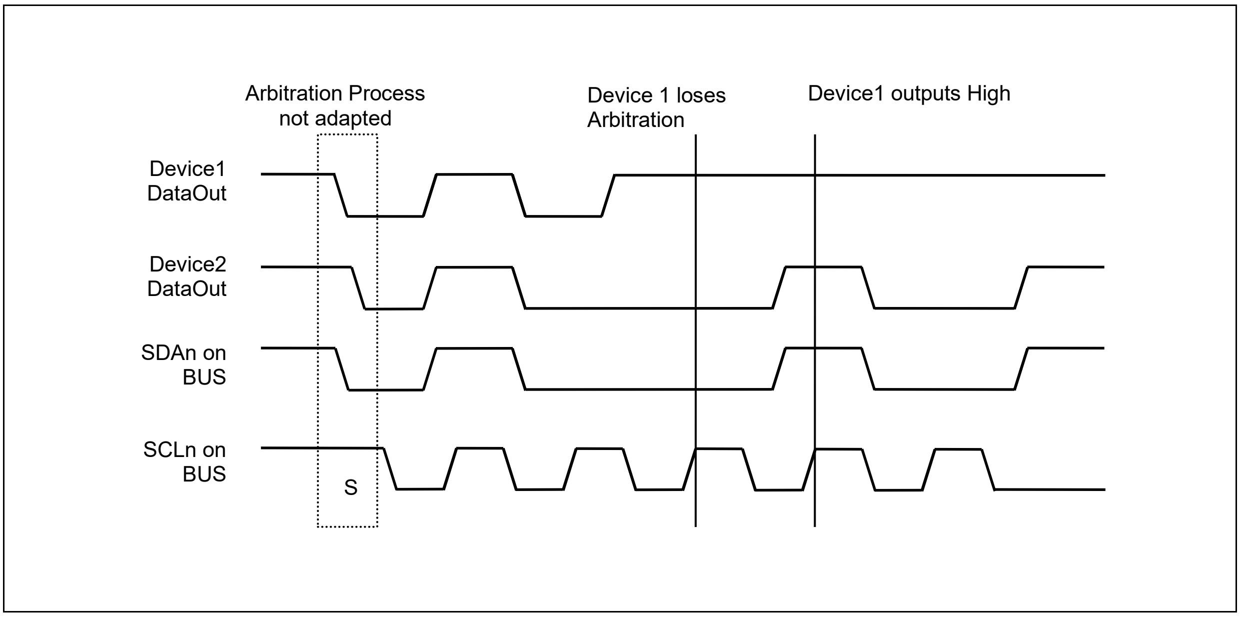


Figure 98. Arbitration procedure between two masters (n = 0 and 1)

16.5 I2C operation

The I2C is byte-oriented and interrupt-based. Interrupts are issued after all bus events except for the transmission of a START condition. Since I2C is interrupt based, the application software is free to carry on with other operations during an I2C byte transfer.

Note that when an I2C interrupt is generated, I2CnIFLAG flag in I2Cn_CR register is set, and it is cleared when all interrupt source bits in the I2Cn_ST register are cleared to '0'. When I2C interrupt occurs, the SCLn line is held at LOW until all interrupt source bits in I2Cn_ST register are cleared to '0'. When the I2CnIFLAG flag is set, the I2Cn_ST contains a value indicating the current state of the I2C bus. According to the value in I2Cn_ST, software can decide what to do next.

I2C can operate in 4 modes: master/slave, transmitter/receiver. The operating mode is configured by a winning master. A more detailed explanation follows below. (n = 0 and 1)

16.5.1 Master transmitter

To operate I2C as a master transmitter, follow the recommended steps below.

1. Enable I2C by setting I2CnEN bit in I2Cn_CR. This provides main clock to the peripheral.
2. Load SLA+W into the I2Cn_DR, where SLA is the address of slave device and W is the transfer direction from the viewpoint of master. For master transmitter, W is '0'. Note that I2Cn_DR is used for both address and data.
3. Configure baud rate by writing desired value to both I2Cn_SCLR and I2Cn_SCHR for the Low and High period of SCLn line.
4. Configure the I2Cn_SDHR to decide when SDAn changes value from falling edge of SCLn. If SDA should change in the middle of SCLn LOW period, load half the value of I2Cn_SCLR to the I2Cn_SDHR.
5. Set the STARTCn bit in I2Cn_CR. This transmits a START condition. Also, configure how to handle interrupt and ACK signal. When the STARTCn bit is set, 8-bit data in I2Cn_DR is transmitted out according to the baud-rate.
6. This is ACK signal processing stage for address packet transmitted by master. When 7-bit address and 1-bit transfer direction is transmitted to target slave device, the master can know whether the slave acknowledged or not in the 9th high period of SCLn. If the master gains bus mastership, I2C generates GCALL interrupt regardless of receiving ACK from the slave device. When I2C loses bus mastership during arbitration process, the MLOSTn bit in I2Cn_ST is set, and I2C waits in idle state or can be operated as an addressed slave.

   To operate as a slave when the MLOSTn bit in I2Cn_ST is set, the ACKnEN bit in I2Cn_CR must be set and the received 7-bit address must match the SLAn bits in I2Cn_SAR1/2. In this case, I2C operates as a slave transmitter or a slave receiver (go to appropriate section). In this stage, I2C holds the SCLn LOW. The reason for this is to decide whether I2C should continue serial transfer or stop communication. The following steps continue, assuming that I2C does not lose mastership during the first data transfer.

   I2C (Master) can choose one of the following cases regardless of receiving ACK signal from slave.

   A. Master receives ACK signal from slave, so continues data transfer since slave can receive more data from master. In this case, load data to transmit to I2Cn_DR.

   B. Master stops data transfer even if it receives ACK signal from slave. In this case, set the STOPC bit in I2Cn_CR.

   C. Master transmits repeated START condition without checking ACK signal. In this case, load SLA+R/W into the I2Cn_DR and set STARTCn bit in I2Cn_CR.

After doing any of the actions above, clear all interrupt source bits in I2Cn_ST to '0' to release SCLn line. In case of A, move to step 7. In case of B, move to step 9 to handle STOP interrupt. In case of C, move to step 6 after transmitting the data in I2Cn_DR, and if transfer direction bit is '1', go to master receiver section.

7. 1-Byte of data is transmitted. During data transfer, bus arbitration continues.
8. This is ACK signal processing stage for data packet transmitted by master. I2C holds the SCLn LOW. When I2C loses bus mastership while transmitting data to arbitrate other masters, the MLOSTn bit in I2Cn_ST is set. If then, I2C waits in idle state. When the data in I2Cn_DR is transmitted completely, I2C generates TENDn interrupt.

   I2C can choose one of the following cases regardless of receiving ACK signal from slave.

   A. Master receives ACK signal from slave, so continues data transfer since slave can receive more data from master. In this case, load data to transmit to I2Cn_DR.
   B. Master stops data transfer even if it receives ACK signal from slave. In this case, set the STOPCn bit in I2Cn_CR.
   C. Master transmits repeated START condition without checking ACK signal. In this case, load SLA+R/W into the I2Cn_DR and set the STARTCn bit in I2Cn_CR.

   After doing any of the actions above, clear all interrupt source bits in I2Cn_ST to '0' to release SCL line. In case of A, move to step 7. In case of B, move to step 9 to handle STOP interrupt. In case of C, move to step 6 after transmitting the data in I2CDR, and if transfer direction bit is '1', go to master receiver section.
9. This is the final step for master transmitter function of I2C, handling STOP interrupt. The STOP bit indicates that data transfer between master and slave is over. To clear I2Cn_ST, write "0xff" to I2Cn_ST. After this, I2C enters idle state.

16.5.2 Master receiver

To operate I2C in master receiver, follow the recommended steps below.

1. Enable I2C by setting I2CnEN bit in I2Cn_CR. This provides main clock to the peripheral.
2. Load SLA+R into the I2Cn_DR, where SLA is address of slave device and R is transfer direction from the viewpoint of the master. For master receiver, R is '1'. Note that I2Cn_DR is used for both address and data.
3. Configure baud rate by writing desired value to both I2Cn_SCLR and I2Cn_SCHR for the Low and High period of SCLn line.
4. Configure the I2Cn_SDHR to decide when SDAn changes value from falling edge of SCLn. If SDAn should change in the middle of SCLn LOW period, load half the value of I2Cn_SCLR to the I2Cn_SDHR.
5. Set the STARTCn bit in I2Cn_CR. This transmits a START condition. Also, configure how to handle interrupt and ACK signal. When the STARTCn bit is set, 8-bit data in I2Cn_DR is transmitted out according to the baud-rate.
6. This is ACK signal processing stage for address packet transmitted by master. When 7-bit address and 1-bit transfer direction is transmitted to target slave device, the master can know whether the slave acknowledged or not in the 9th high period of SCLn. If the master gains bus mastership, I2C generates GCALL interrupt regardless of receiving ACK from the slave device. When I2C loses bus mastership during arbitration process, the MLOSTn bit in I2Cn_ST is set, and I2C waits in idle state or can be operated as an addressed slave.

   To operate as a slave when the MLOSTn bit in I2Cn_ST is set, the ACKnEN bit in I2Cn_CR must be set, and the received 7-bit address must equal to the SLAn bits in I2Cn_SAR1/2. In this case, I2C operates as a slave transmitter or a slave receiver (go to appropriate section). In this stage, I2C holds the SCLn LOW. The reason for this is to decide whether I2C should continue serial transfer or stop communication. The following steps continue, assuming that I2C does not lose mastership during the first data transfer.

I2C (Master) can choose one of the following cases according to the reception of ACK signal from slave.

A. Master receives ACK signal from slave, so continues data transfer since slave can prepare and transmit more data to master. Configure ACKnEN bit in I2Cn_CR to decide whether I2C should Acknowledges the next data to be received or not.

B. Master stops data transfer since it receives no ACK signal from slave. In this case, set the STOPCn bit in I2Cn_CR.

C. Master transmits repeated START condition due to lack of ACK signal from slave. In this case, load SLA+R/W into the I2Cn_DR and set STARTCn bit in I2Cn_CR.

After doing any of the actions above, clear all interrupt source bits in I2Cn_ST to '0' to release SCLn line. In case of A, move to step 7. In case of B, move to step 9 to handle STOP interrupt. In case of C, move to step 6 after transmitting the data in I2Cn_DR, and if transfer direction bit is '0', go to master transmitter section.

7. 1-Byte of data is received.

8. This is ACK signal processing stage for data packet transmitted by slave. I2C holds the SCLn LOW. When 1-Byte of data is received completely, I2C generates TENDn interrupt.

   I2C can choose one of the following cases according to the RXACKn flag in I2Cn_ST.

   A. Master continues receiving data from slave. To do this, set ACKnEN bit in I2Cn_CR to acknowledge the next data to be received.

   B. Master wants to terminate data transfer when it receives next data by not generating ACK signal. This can be done by clearing ACKnEN bit in I2Cn_CR.

   C. Since no ACK signal is detected, master terminates data transfer. In this case, set the STOPCn bit in I2Cn_CR.

   D. No ACK signal is detected, and master transmits repeated START condition. In this case, load SLA+R/W into the I2Cn_DR and set the STARTCn bit in I2Cn_CR.

   After doing any of the actions above, clear all interrupt source bits in I2Cn_ST to '0' to release SCLn line. In case of A and B, move to step 7. In case of C, move to step 9 to handle STOP interrupt. In case of D, move to step 6 after transmitting the data in I2Cn_DR, and if transfer direction bit is '0', go to master transmitter section.

9. This is the final step for master receiver function of I2C, handling STOP interrupt. The STOP bit indicates that data transfer between master and slave is over. To clear I2Cn_ST, write "0xff" value to I2Cn_ST. After this, I2C enters idle state.

16.5.3 Slave transmitter

To operate I2C in slave transmitter, follow the recommended steps below.

1. If the operating clock (HCLK) of the system is slower than that of SCLn, load value 0x00 into I2Cn_SDHR to make SDAn change within one system clock period from the falling edge of SCLn. Note that the hold time of SDAn is calculated by SDAH x period of HCLK where SDAH is multiple of number of HCLK coming from I2Cn_SDHR. When the hold time of SDAn is longer than the period of HCLK, I2C (slave) cannot transmit serial data properly.
2. Enable I2C by setting I2CnIEN bit and I2CnEN bit in I2Cn_CR. This provides main clock to the peripheral.
3. When a START condition is detected, I2C receives one byte of data and compares it with SLAn bits in I2Cn_SAR1/2. If the GCALLnEN bit in I2Cn_SAR1/2 is enabled, I2C compares the received data with value 0x00, the general call address.
4. If the received address does not match SLAn bits in I2CnSAR, I2C enters idle state, i.e, waits for another START condition. Otherwise, if the address equals to SLAn bits and the ACKnEN bit is enabled, I2C generates SSELn interrupt and the SCLn line is held LOW. Note that even if the address matches SLAn bits, when the ACKnEN bit is disabled, I2C enters idle state. When SSELn interrupt occurs, load transmit data to I2Cn_DR and clear all interrupt source bits in I2Cn_ST to '0' to release SCLn line.
5. 1-Byte of data is transmitted.
6. In this step, I2C generates TENDn interrupt and holds the SCLn line LOW regardless of receiving ACK signal from master. Slave can select one of the following cases.

   A. No ACK signal is detected and I2C waits STOP or repeated START condition.

   B. ACK signal from master is detected. Load data to transmit into I2Cn_DR.

   After doing any of the actions above, clear all interrupt source bits in I2Cn_ST to '0' to release SCLn line. In case of A, move to step 7 to terminate communication. In case of B, move to step 5. In either case, a repeated START condition can be detected. For that case, move step 4.
7. This is the final step for slave transmitter function of I2C, handling STOP interrupt. The STOPCn bit indicates that data transfer between master and slave is over. To clear I2Cn_ST, write "0xff" to I2Cn_ST. After this, I2C enters idle state.

16.5.4 Slave receiver

To operate I2C in slave receiver, follow the recommended steps below.

1. If the operating clock (HCLK) of the system is slower than that of SCLn, load value 0x00 into I2Cn_SDHR to make SDAn change within one system clock period from the falling edge of SCLn. Note that the hold time of SDAn is calculated by SDAH x period of HCLK where SDAH is multiple of number of HCLK coming from I2Cn_SDHR. When the hold time of SDAn is longer than the period of HCLK, I2C (slave) cannot transmit serial data properly.
2. Enable I2C by setting I2CnIEN bit in I2Cn_CR. This provides main clock to the peripheral.
3. When a START condition is detected, I2C receives one byte of data and compares it with SLA bits in I2CSAR. If the GCALLnEN bit in I2Cn_SAR1/2 is enabled, I2C compares the received data with value 0x00, the general call address.
4. If the received address does not match SLAn bits in I2Cn_SAR1/2, I2C enters idle state i.e., waits for another START condition. Otherwise, if the address match SLAn bits and the ACKnEN bit is enabled, I2C generates SSELn interrupt and the SCLn line is held LOW. Note that even if the address equals to SLA bits, when the ACKnEN bit is disabled, I2C enters idle state. When SSELn interrupt occurs and I2C is ready to receive data, clear all interrupt source bits in I2Cn_ST to '0' to release SCLn line.
5. 1-Byte of data is received.
6. In this step, I2C generates TENDn interrupt and holds the SCLn line LOW regardless of receiving ACK signal from master. Slave can select one of the following cases.

   A. No ACK signal is detected (ACKnEN=0) and I2C waits STOP or repeated START condition.

   B. ACK signal is detected (ACKnEN=1) and I2C can continue to receive data from master.

   After doing any of the actions above, clear all interrupt source bits in I2Cn_ST to '0' to release SCLn line. In case of A, move to step 7 to terminate communication. In case of B, move to step 5. In either case, a repeated START condition can be detected. For that case, move to step 4.
7. This is the final step for slave receiver function of I2C, handling STOP interrupt. The STOPCn bit indicates that data transfer between master and slave is over. To clear I2Cn_ST, write "0xff" to I2Cn_ST. After this, I2C enters idle state.

17 LCD driver

LCD driver of A31G11x series includes an LCD control register (LCD_CR) and an LCD driver bias and contrast control register (LCD_BCCR). LCLK[1:0] of the LCD_CR determines frequency of COM signal scanning each segment output. A RESET clears the LCD_CR and sets the LCD_BCCR to logic '0'.

LCD display can continue its operation even during Sleep mode and Deep sleep mode if it uses a selected clock for LCD driver.

A clock and duty of the LCD driver is initialized by hardware whenever a value is written to the control register. So, it is recommended not to rewrite the LCD_CR frequently.

17.1 LCD driver block diagram

Figure 99 shows a block diagram of the LCD driver block.

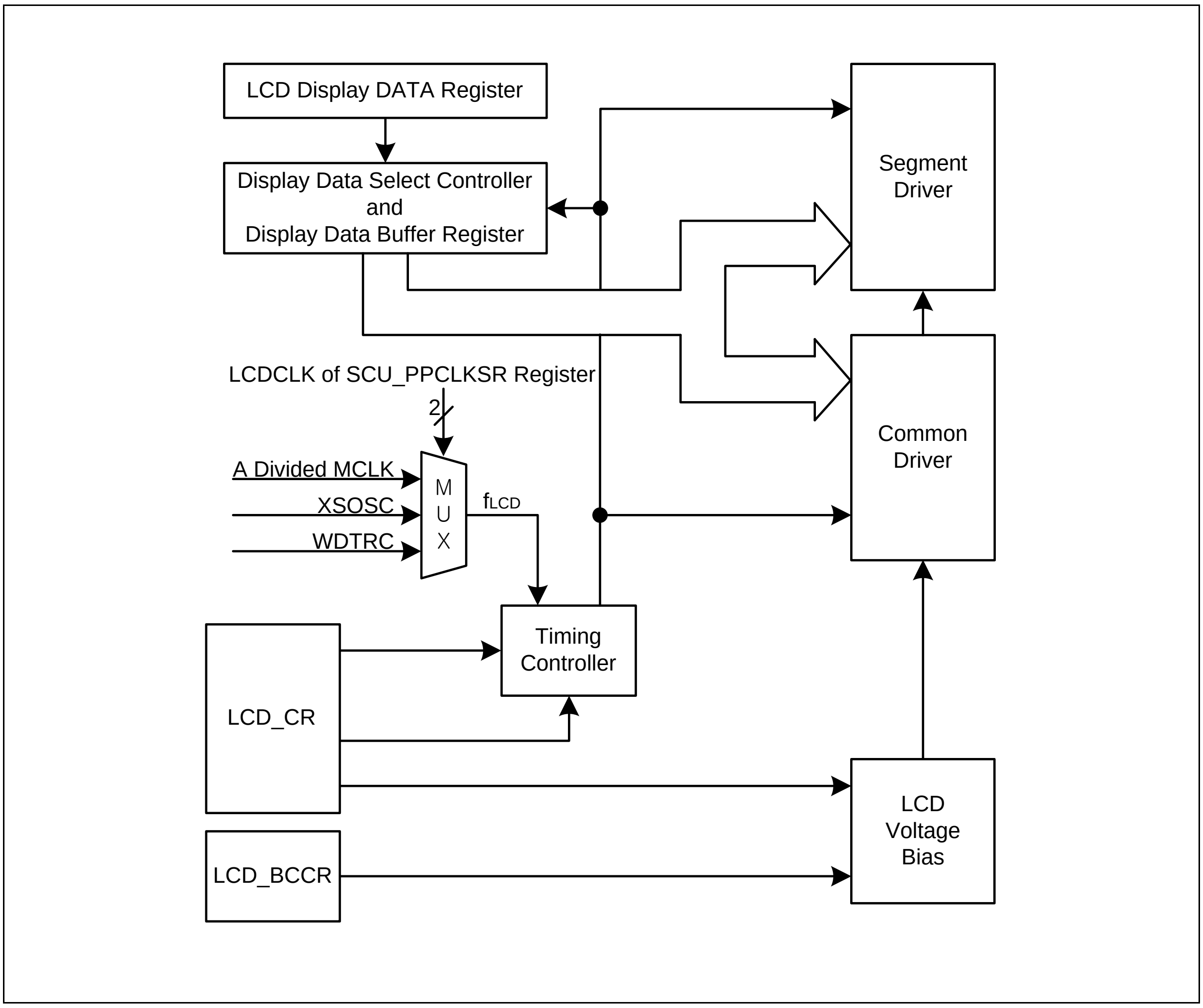


Figure 99. LCD Driver Block Diagram

17.2 Pin description for LCD driver

Table 70. Pins and External Signals for LCD Driver

PIN NAME	TYPE	DESCRIPTION
COM0 to COM7	O	LCD common signal outputs
SEG0 to SEG27	O	LCD segment signal outputs

17.3 Registers

Base address and register map of the LCD driver are shown in Table 71 and Table 72.

Table 71. Base Address of LCD Driver

Name	Base address
LCD	0x4000_5000

Table 72. LCD Driver Register Map

Name	Offset	Type	Description	Reset Value
LCD_CR	0x0000	RW	LCD driver control register	0x00000000
LCD_BCCR	0x0004	RW	LCD automatic bias and contrast control register	0x00000000
LCD_DR0 to DR27	0x0010 to 0x002B	RW	LCD display data register 0 to 27	Unknown

17.3.1 LCD_CR: LCD driver control register

LCD_CR register is 32-bit size and accessible in 32/16/8-bit.

LCD_CR=0x4000_5000

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="24">Reserved</td><td colspan="2">IRSEL</td><td colspan="3">DBS</td><td colspan="2">LCLK</td><td>DISP</td></tr>
<tr><td colspan="24">0x000000</td><td colspan="2">00</td><td colspan="3">000</td><td colspan="2">00</td><td>0</td></tr>
<tr><td colspan="24">-</td><td colspan="2">RW</td><td colspan="3">RW</td><td colspan="2">RW</td><td>RW</td></tr>
</table>

7 6	IRSEL	Internal LCD Bias Dividing Resistor Selection.	
		00	RLCD3: 105/105/80[kΩ] @(1/2)/(1/3)/(1/4) bias.
		01	RLCD1: 10/10/10[kΩ] @(1/2)/(1/3)/(1/4) bias.
		10	RLCD2: 66/66/50[kΩ] @(1/2)/(1/3)/(1/4) bias.
		11	RLCD4: 320/320/240[kΩ] @(1/2)/(1/3)/(1/4) bias.
5 3	DBS	LCD Duty and Bias Selection.	
		000	1/8 duty, 1/4 bias.
		001	1/6 duty, 1/4 bias.
		010	1/5 duty, 1/3 bias.
		011	1/4 duty, 1/3 bias.
		100	1/3 duty, 1/3 bias.
		101	1/3 duty, 1/2 bias
		Others	Reserved.
2 1	LCLK	LCD Clock Selection (When fLCD = 32.768kHz).	
		00	128Hz.
		01	256Hz.
		10	512Hz.
		11	1024Hz.
0	DISP	LCD Display Control.	
		0	Display off.
		1	Normal display on.

17.3.2 LCD_BCCR: LCD automatic bias and contrast control register

LCD_BCCR register is 32-bit size and accessible in 32/16/8-bit.

LCD_BCCR=0x4000_5004

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13	12	11	10 9 8	7 6	5	4	3 2 1 0
Reserved	**Reserved**	**LCDABC**	**Reserved**	**BMSEL**	**Reserved**	**LCTEN**	**Reserved**	**VLCD**
0x0000	**000**	**0**	**0**	**000**	**00**	**0**	**0**	**0000**
–	**-**	**RW**	**-**	**RW**	**-**	**RW**	**-**	**RW**

12	LCDABC	LCD Automatic Bias Control.	
		0	LCD automatic bias is off.
		1	LCD automatic bias is on.
10 8	BMSEL	"Bias Mode A" Time Selection. Refer to the figure "LCD automatic bias control".	
		000	"Bias Mode A" for 1-clock of fLCD.
		001	"Bias Mode A" for 2-clock of fLCD.
		010	"Bias Mode A" for 3-clock of fLCD.
		011	"Bias Mode A" for 4-clock of fLCD.
		100	"Bias Mode A" for 5-clock of fLCD.
		101	"Bias Mode A" for 6-clock of fLCD.
		110	"Bias Mode A" for 7-clock of fLCD.
		111	"Bias Mode A" for 8-clock of fLCD.
5	LCTEN	LCD Driver Contrast Control.	
		0	Disable LCD driver contrast.
		1	Enable LCD driver contrast.
3 0	VLCD	VLC0 Voltage Control when the contrast is enabled.	
		0000	VLC0 = VDD x 16/31 step
		0001	VLC0 = VDD x 16/30 step
		0010	VLC0 = VDD x 16/29 step
		0011	VLC0 = VDD x 16/28 step
		0100	VLC0 = VDD x 16/27 step
		0101	VLC0 = VDD x 16/26 step
		0110	VLC0 = VDD x 16/25 step
		0111	VLC0 = VDD x 16/24 step
		1000	VLC0 = VDD x 16/23 step
		1001	VLC0 = VDD x 16/22 step
		1010	VLC0 = VDD x 16/21 step
		1011	VLC0 = VDD x 16/20 step
		1100	VLC0 = VDD x 16/19 step
		1101	VLC0 = VDD x 16/18 step
		1110	VLC0 = VDD x 16/17 step
		1111	VLC0 = VDD x 16/16 step

NOTES:

1. The above LCD contrast step is based on 1/3 bias with 66kΩ RLCD and on 1/4 bias with 50kΩ RLCD.
2. The LCD driver contrast control bit (LCTEN) should be cleared to '0' when the LCD automatic bias control bit (LCDABC) is set to '1'.

17.3.3 LCD_DRx: LCD display data register x (x = 0 to 27)

LCD_DRx register is 32-bit size and accessible in 32/16/8-bit. (n = 0 to 6)

LCD_DRx=0x4000_5010 to 0x4000_502B

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
LCD_DR(4xn+3)	**LCD_DR(4xn+2)**	**LCD_DR(4xn+1)**	**LCD_DR(4xn+0)**
0x00	**0x00**	**0x00**	**0x00**
RW	**RW**	**RW**	**RW**

31 24	LCD_DR(4xn+3)	LCD Display Data.
23 16	LCD_DR(4xn+2)	LCD Display Data.
15 8	LCD_DR(4xn+1)	LCD Display Data.
7 0	LCD_DR(4xn+0)	LCD Display Data.

17.4 LCD display RAM organization

Display data are stored in display data area. The display data stored to the display data area (address 0x4000_5010-0x4000_502B) are read automatically and are sent to the LCD driver by hardware. The LCD driver generates the segment and common signals in accordance to the display data and driving method. Therefore, display patterns can be changed by simply overwriting the contents of the display data area with a program.

Figure 100 shows the correspondence between the display data area and the COM/SEG pins. The LCD is turned on when the display data is '1' and turned off when it is '0'.

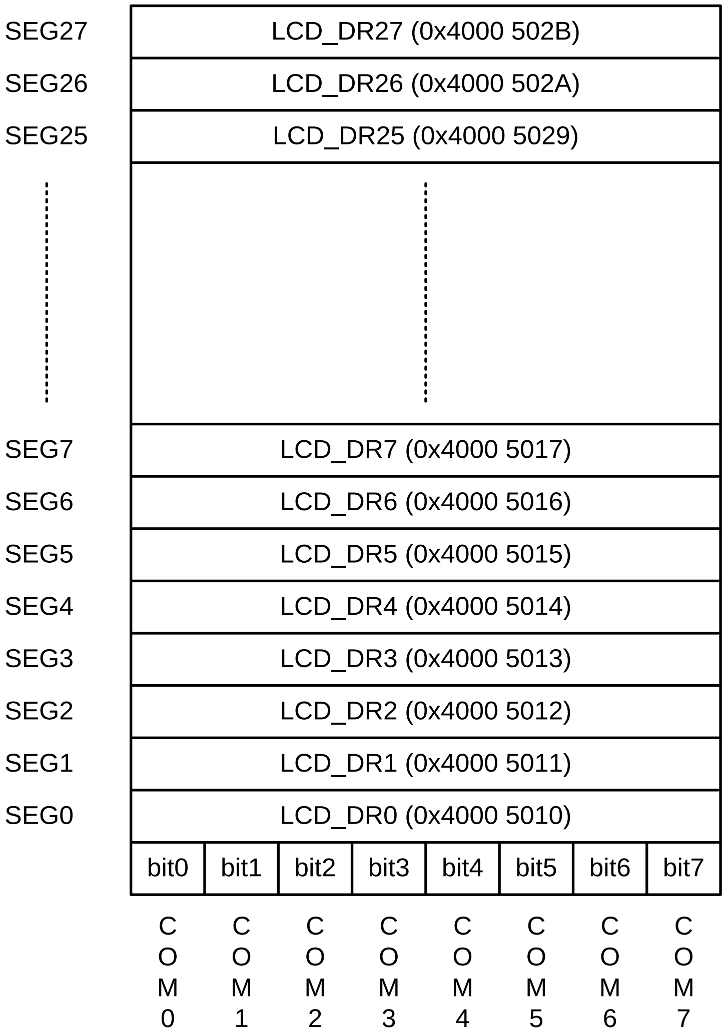


Figure 100. LCD Display RAM Organization

17.5 LCD signal waveform

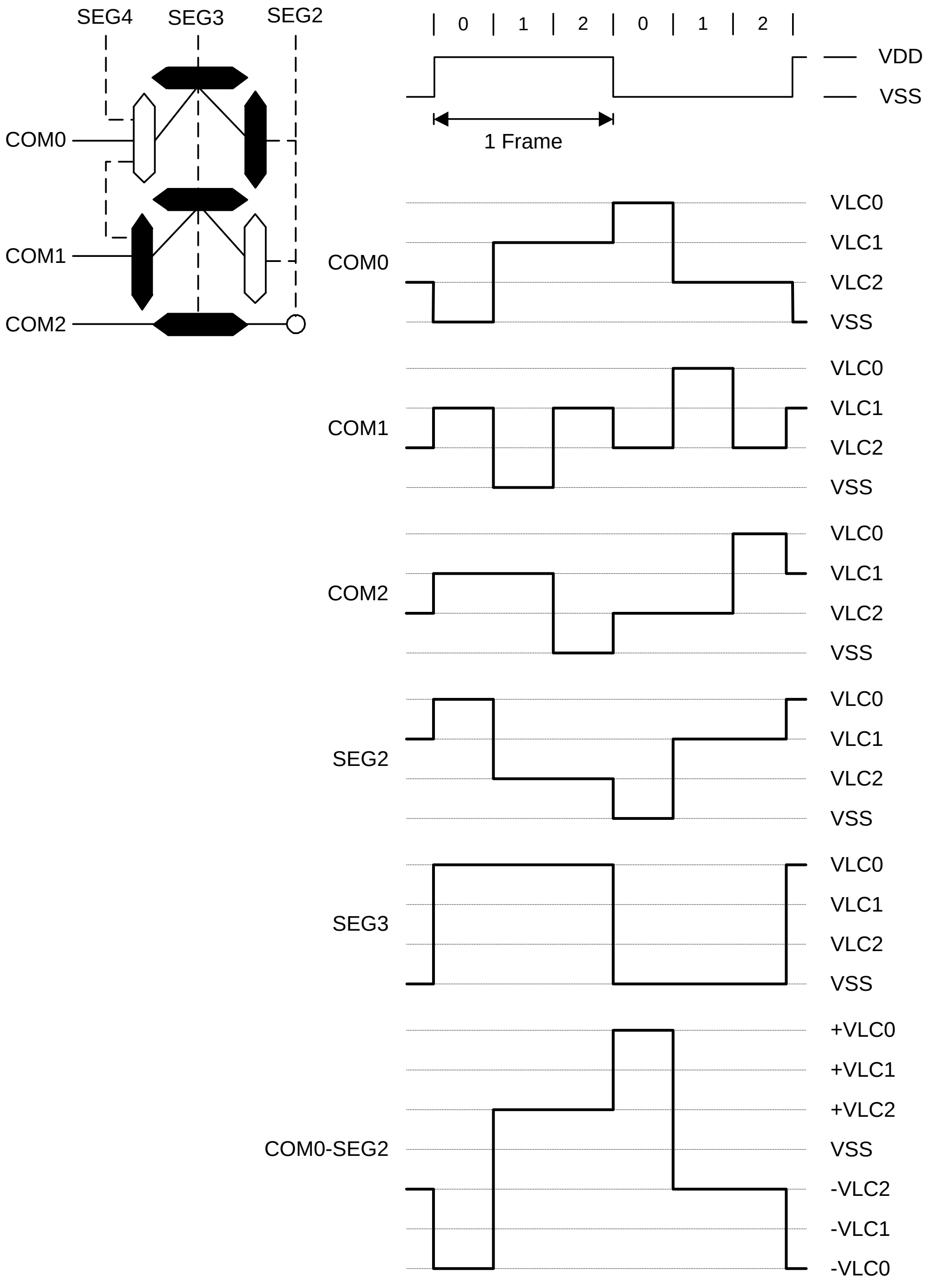


Figure 101. LCD Signal Waveforms (1/3 Duty, 1/3 Bias)

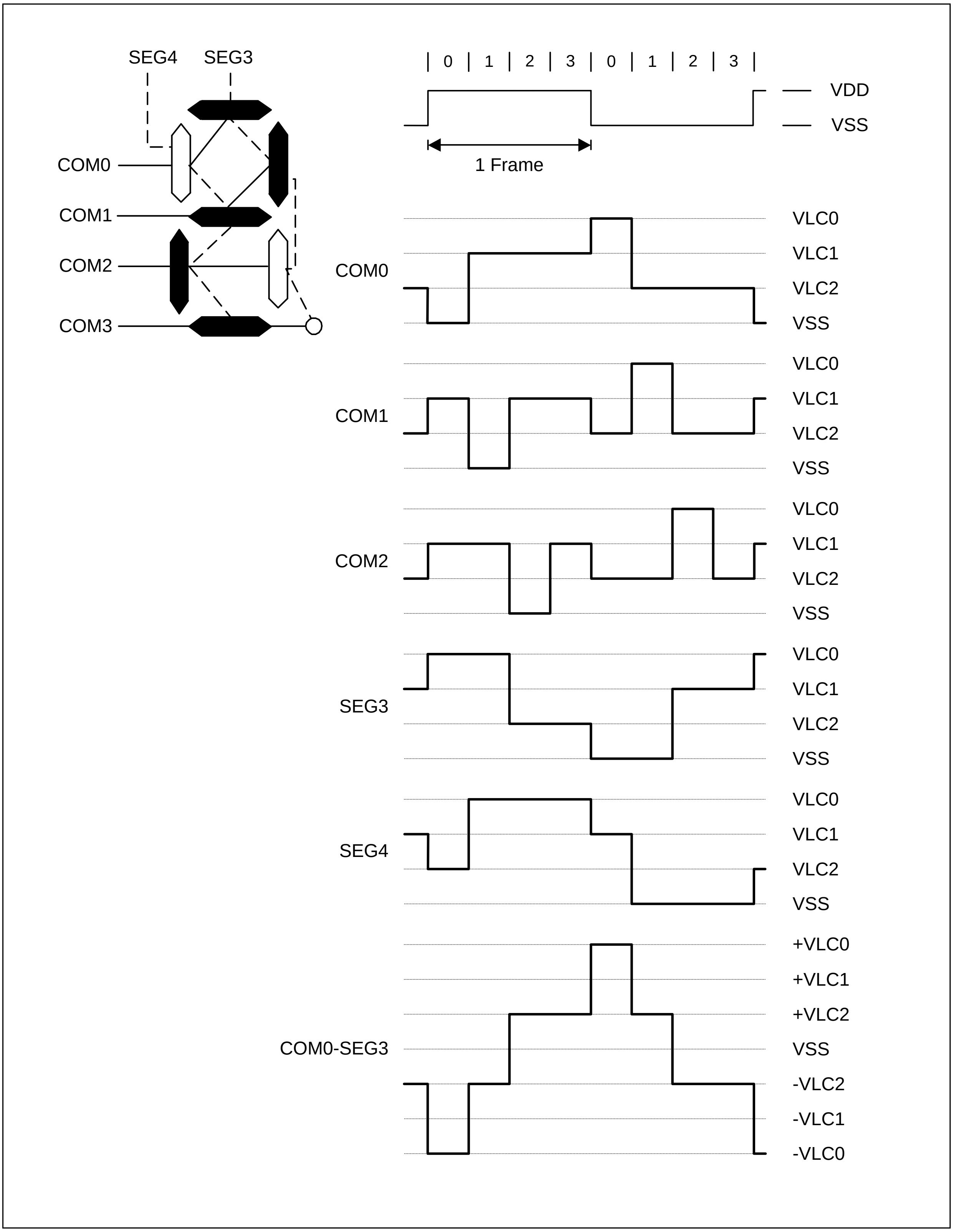


Figure 102. LCD Signal Waveforms (1/4 Duty, 1/3 Bias)

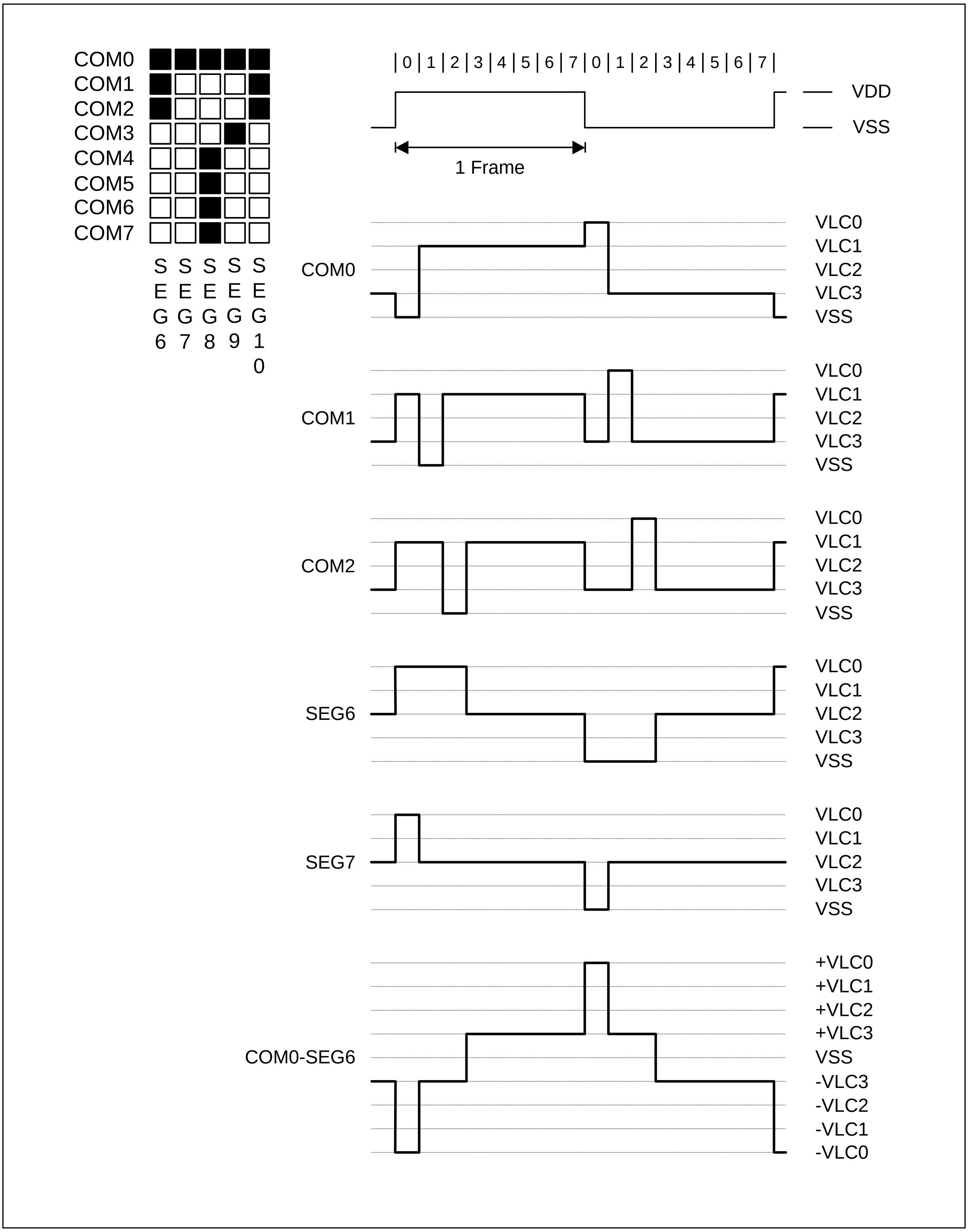
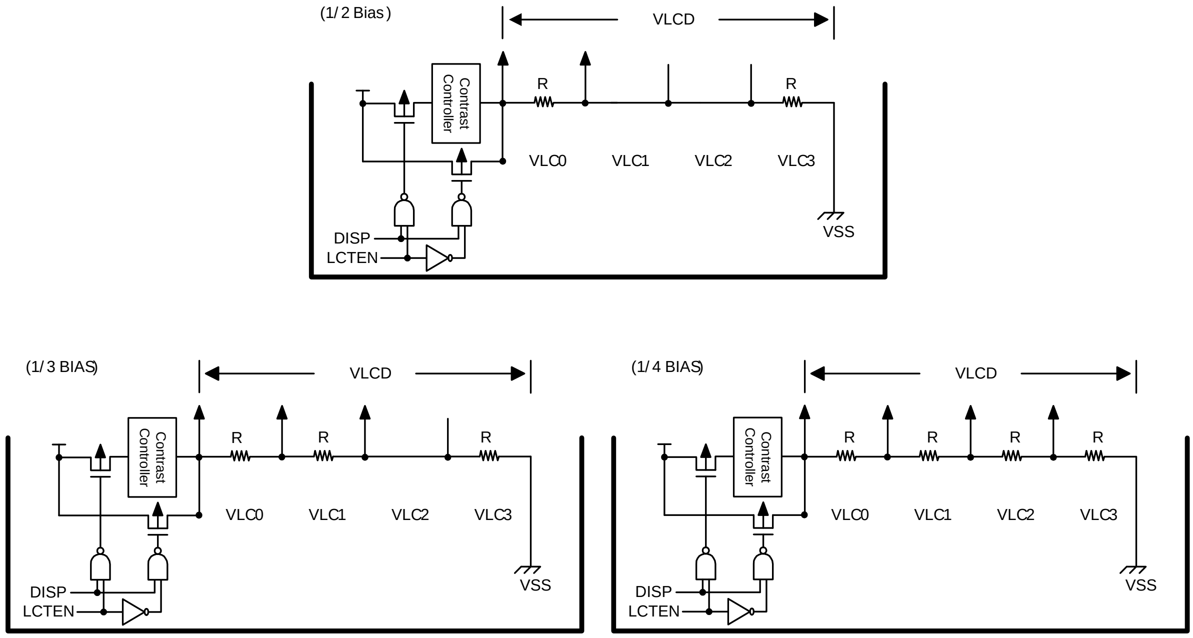


Figure 103. LCD Signal Waveforms (1/8 Duty, 1/4 Bias)

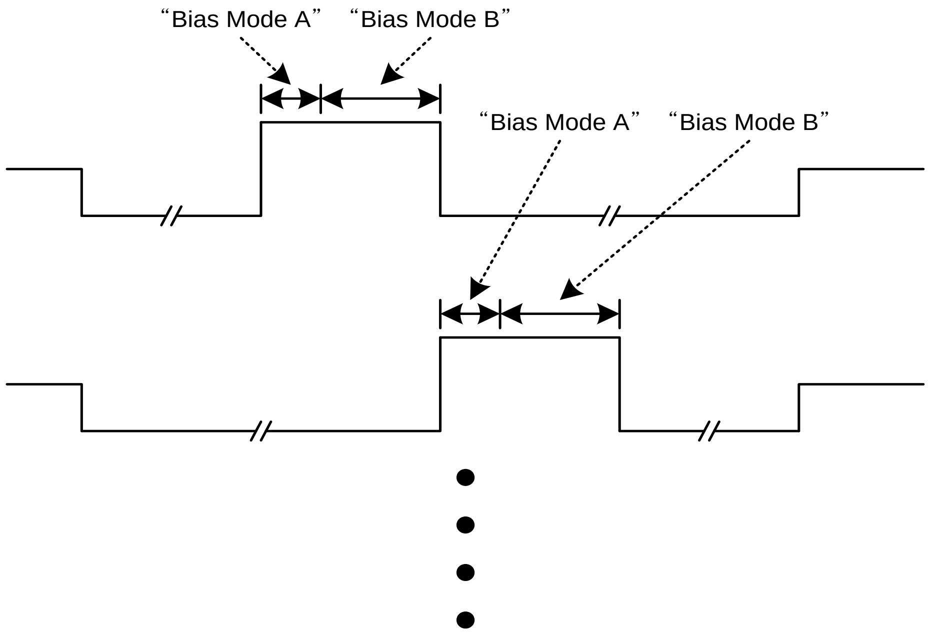
17.6 Internal resistor bias connection



NOTE: The above figures are for the internal resistor bias connection.

Figure 104. Internal Resistor Bias Connection

17.7 LCD Automatic Bias Control Timing



NOTES: Refer to below when the LCD automatic bias is on

1. “Bias Mode A”: Always RLCD1 (10kΩ).
2. “Bias Mode B”: An LCD bias dividing resistor, which is selected by IRSEL[1:0] bits

Figure 105. LCD Automatic Bias Control Timing Diagram

18 CRC and checksum

A CRC (cyclic redundancy check) generator is used to obtain 16-bit CRC code of Flash ROM and any data stream.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of functional safety standards, they offer means of verifying Flash memory's integrity.

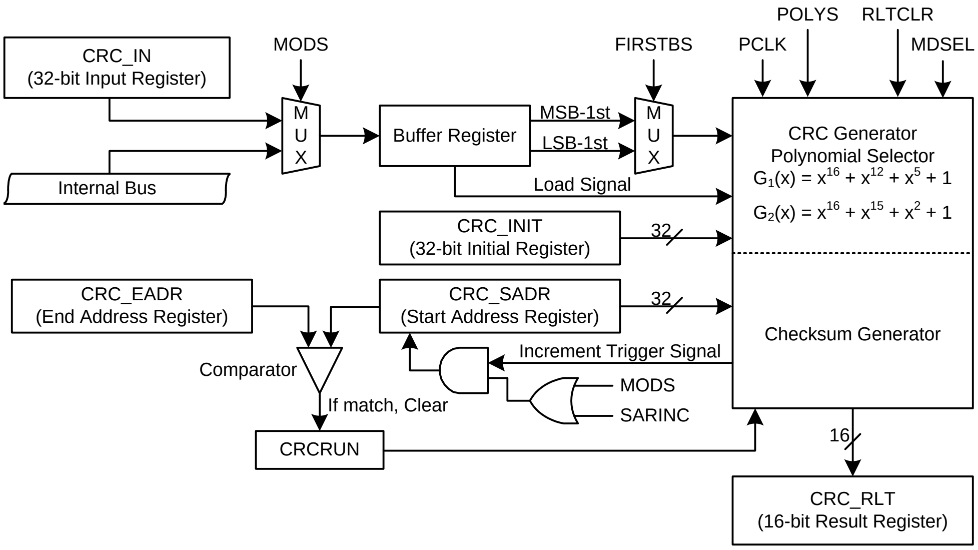
The CRC generator helps computing the signature of the software during runtime, comparing with a reference signature.

A CRC generator of A31G11x series has following features:

- Auto CRC and User CRC Mode
- Supports CRC-CCITT ($G_1(x) = x^{16} + x^{12} + x^5 + 1$)
- Supports CRC-16 ($G_2(x) = x^{16} + x^{15} + x^2 + 1$)
- CRC and Checksum mode
- CRC/Checksum Start Address Auto Increment (User mode only)

18.1 CRC and checksum block diagram

Figure 106 shows a block diagram of the CRC and checksum interface block.



NOTES:

1. The operation is finished after calculating from the CRC_SADR to the CRC_EADR on auto mode or SARINC=1.
2. The CRC_SADR and CRC_EADR are the same value after completion.
3. The end address (CRC_EADR) must be greater than the start address (CRC_SADR) by at least 4.
4. The CRC_SADR/CRC_EADR on the "Auto mode" should have any value in flash memory area (0x10000000 to 0x10007FFF).
5. The CPU will be held at "Auto Mode" if the CPU is in the flash memory and the global interrupt should be disabled by software.
6. The HCLK frequency should be less than or equal to 20MHz in "Auto mode" by CRC_CR.MODS bit.
7. On auto mode run, the CRC_CR register cannot be written and the CRC_RLT register cannot be read.

Figure 106. CRC and Checksum Block Diagram

18.2 Registers

Base address and register map of the CRC and checksum block are shown in Table 73 and Table 74.

Table 73. Base Address of CRC

Name	Base address
CRC	0x3000_1000

Table 74. CRC Register Map

Name	Offset	Type	Description	Reset Value
CRC_CR	0x0000	RW	CRC/Checksum Control Register	0x00000000
CRC_IN	0x0004	RW	CRC/Checksum Input Data Register	0x00000000
CRC_RLT	0x0008	RO	CRC/Checksum Result Data Register	0x0000FFFF
CRC_INIT	0x000C	RW	CRC/Checksum Initial Data Register	0x00000000
CRC_SADR	0x0010	RW	CRC/Checksum Start Address Register	0x10000000
CRC_EADR	0x0014	RW	CRC/Checksum End Address Register	0x1000FFFC

18.2.1 CRC_CR: CRC control register

CRC_CR register is 32-bit size and accessible in 32/16/8-bit.

CRC_CR=0x3000_1000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								MODS	RLTCLR	MDSEL	POLYS	SARINC	Reserved	FIRSTBS	CRCRUN
0x000000																								0	0	0	0	0	0	0	0
-																								RW	RW	RW	RW	RW	-	RW	RW

7	MODS	User/Auto Mode Selection.	
		0	User mode. (Calculate every data written to the CRC_IN register)
		1	Auto mode. (Calculate till CRC_SADR == CRC_EADR)
6	RLTCLR	CRC/Checksum Result Data Register (CRC_RLT) Initialization.	
		0	No effect.
		1	Initialize the CRC_RLT register with the value of CRC_INIT (This bit is automatically cleared to '0' after operation)
5	MDSEL	CRC/Checksum Selection.	
		0	Select CRC.
		1	Select checksum.
4	POLYS	Polynomial Selection. (CRC only)	
		0	Select CRC-CCITT ($G_1(x) = x^{16} + x^{12} + x^5 + 1$)
		1	Select CRC-16 ($G_2(x) = x^{16} + x^{15} + x^2 + 1$)
3	SARINC	CRC/Checksum Start Address Auto Increment Control. (User mode only)	
		0	No effect.
		1	The CRC/Checksum start address register is incremented by '4' every data written to the CRC_IN register.
1	FIRSTBS	First Shifted-in Selection. (CRC only)	
		0	MSB-1st.
		1	LSB-1st.
0	CRCRUN	CRC/Checksum Start Control and Busy.	
		0	Not busy. The CRC operation can be finished by writing '0' to this bit while running.
		1	Start CRC operation. This bit is automatically cleared to '0' when

	the value of CRC_SADR register reaches the value of CRC_EADR register.
	NOTE) The 5 “NOP instruction” should be executed immediately after this bit becomes ‘1’.

NOTES:

1. The CRC_RLT register and the CRC/Checksum block should be initialized by writing ‘1’ to the RLTCLR bit before a new CRC/Checksum calculation.
2. The CRCRUN bit should be set to ‘1’ last time after setting appropriate values to the registers.
3. On the user mode, it will be calculated every writing data to the CRC_IN register during CRCRUN==1.
4. On the user mode with SARINC==0, the block is finished by writing ‘0’ to the CRCRUN bit.
5. It is prohibited writing any data to the CRC_IN register during CRCRUN==0.
6. The checksum is calculated by byte unit.
   — Ex) On 0x34A7E991, CRC_RLT = 0x34 + 0xA7 + 0xE9 + 0x91.
7. The 5 “NOP Instruction” should follow immediately after CRCRUN bit is set to ‘1’.

18.2.2 CRC_IN: CRC input data register

CRC_IN register is 32-bit size.

CRC_IN=0x3000_1004

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
INDATA			
0x00000000			
RW			

31 0	INDATA	CRC Input Data.

NOTE: The CRC_IN register should be written in 1-word (32-bit).

18.2.3 CRC_RLT: CRC result data register

CRC_RLT register is 32-bit size and accessible in 32/16/8-bit.

CRC_RLT=0x3000_1008

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved		RLTDATA	
0x0000		0xFFFF	
–		RO	

15 0	RLTDATA	CRC Result Data.

18.2.4 CRC_INIT: CRC initial data register

CRC_INIT register is 32-bit size and accessible in 32/16/8-bit.

CRC_INIT=0x3000_100C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved		**INIDATA**	
0x0000		**0x0000**	
–		**RW**	

15 0	INIDATA	CRC Initial Data.

18.2.5 CRC_SADR: CRC start address register

CRC_SADR register is 32-bit size and accessible in 32/16/8-bit.

CRC_SADR=0x3000_1010

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2	1 0
SADR				**Don't care**
0x10000000				**00**
RW				**-**

31 2	SADR	CRC Start Address.
1 0	-	Don't care.

NOTE: The LSB 7-bit of the end address should be "0x00" on "Auto mode".

18.2.6 CRC_EADR: CRC end address register

CRC_EADR register is 32-bit size and accessible in 32/16/8-bit.

CRC_EADR=0x3000_1014

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="30">EADR</td><td colspan="2">Don’t care</td></tr>
<tr><td colspan="30">0x1000FFFC</td><td colspan="2">00</td></tr>
<tr><td colspan="30">RW</td><td colspan="2">-</td></tr>
</table>

31 2	EADR	CRC End Address.
1 0	-	Don’t care.

NOTE: The LSB-7bits of the end address should be “0x7C” on “Auto mode”.

18.3 Functional description

18.3.1 CRC polynomial structure

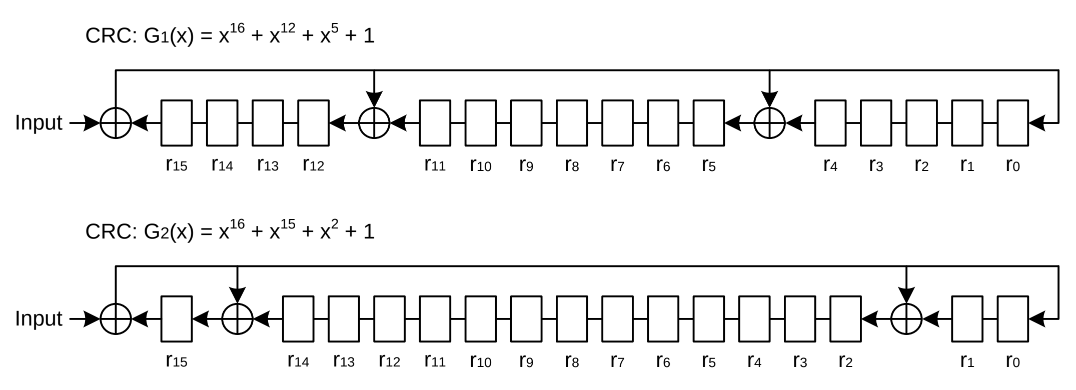


Figure 107. CRC Polynomial Structure

18.3.2 The CRC operation procedure in auto CRC/checksum mode

1. CRC/Checksum Clock Enable
2. Set CRC start address register. (CRC_SADR)
3. Set CRC end address register. (CRC_EADR)
4. Set CRC initial data register. (CRC_INIT)
5. Global interrupt Disable.
6. Select CRC(HCLK) Clock. (HCLK should be less than or equal to 20MHz during CRC/Checksum auto mode)
7. Select Auto CRC/Checksum Mode and CRC.
8. CRC operation starts. (CRCRUN = 1)
9. Read the CRC result.
10. Global interrupt Enable.

18.3.3 The CRC operation procedure in user CRC/checksum mode

1. CRC/Checksum Clock Enable
2. Set CRC start address register. (CRC_SADR)
3. Set CRC end address register. (CRC_EADR)
4. Set CRC initial data register. (CRC_INIT)
5. Select User CRC/Checksum Mode and CRC
6. CRC operation starts. (CRCRUN = 1)
7. Input CRC Data at CRC_IN.
8. Check CRC is finished on Start Address Auto Increment or Compare Start address and End address in order to check CRC end point.
9. Repeat 8 and 9 until CRC end point.

10. CRC Stop and read CRC result.

19 Electrical characteristics

Unless otherwise specified, test conditions for DC characteristics are as shown in the followings:

- T_A = - 40 °C to +85°C(Commercial grade) or T_A = - 40 °C to + 105°C(Industrial grade)
- VDD = 1.8 to 5.5V

NOTE: Refer to Figure 128. A31G11x series Numbering Nomenclature for device part number by Commercial grade.

19.1 Absolute maximum ratings

Absolute maximum ratings are limiting values of operating and environmental conditions, which should not be exceeded under the worst possible conditions.

Table 75. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply voltage	VDD	-0.3 to +6.5	V	–
Normal pin	V_I	-0.3 to VDD +0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3 to VDD +0.3	V	
	I_{OH}	-18	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	ΣI_{OH}	-150	mA	Maximum current (ΣI_{OH})
	I_{OL}	140	mA	Maximum current sunk by (I_{OL} per I/O pin)
	ΣI_{OL}	170	mA	Maximum current (ΣI_{OL})
Total power dissipation	P_T	850	mW	–
Storage temperature	T_{STG}	-65 to +150	°C	–

19.2 Recommended operating conditions

Table 76. Recommended Operating Conditions

Parameter	Symbol	Conditions			Min	Max	Units
Operating voltage	VDD	fx = 32 to 38kHz	Sub Clock		1.8	5.5	V
		fx = 2.0 to 4.2MHz	Main Clock	Ceramic	2.2	5.5	
		fx = 2.0 to 16MHz		Crystal	2.7	5.5	
		fx = 2.0 to 40MHz	External Clock		3.0	5.5	
		fx = 40kHz	Internal RC		1.8	5.5	
		fx = 2.5 to 40MHz			1.8	5.5	
Operating temperature	T_{OPR}	VDD = 1.8 to 5.5V (Commercial grade)			-40	85	°C
		VDD = 1.8 to 5.5V (Industrial grade)			-40	105	

19.3 ADC characteristics

Table 77. ADC Characteristics

(VDD = 2.2V to 5.5V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Resolution	–	–		–	12	–	bit
Integral non-linearity	INL	AVREF=2.7V – 5.5V, T_A = 25 °C		–	–	±5	LSB
Differential non-linearity	DNL			–	–	±1	
Zero offset error	ZOE			–	–	±4	
Full scale error	FSE			–	–	±8	
Conversion time	t_{CONV}	AVREF=4.0V – 5.5V		20	–	–	µs
		AVREF=3.0V – 5.5V		30	–	–	
		AVREF=2.7V – 5.5V		60	–	–	
Analog input voltage	V_{AN}	–		VSS	–	AVREF	V
Analog reference voltage	AVREF	–		2.2	–	VDD	V
ADC input leakage current	I_{AN}	AVREF=5.0V		–	–	2	µA
ADC current	I_{ADC}	Enable	VDD=5.0V	–	1	2	mA
		Disable		–	–	0.1	µA

NOTES:

1. Zero offset error is a difference between 0x000 and the converted output for zero input voltage (VSS).
2. Full scale error is a difference between 0xFFF and the converted output for top input voltage (VDD).
3. If AVREF is less than 2.7V, the resolution degrades by 1-bit whenever AVREF drops 0.1V.
   (It is recommended that the clock of ADC is 0.5MHz under 2.7V)

19.4 Power-on reset characteristics

Table 78. Power-on Reset Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Reset release level	V_{POR}	–	–	1.2	–	V
Hysteresis	△V	–	–	0.2	–	V
VDD voltage rising time	t_R	0.2V to 2.0V	0.05	–	100	V/ms
POR current	I_{POR}	–	–	0.1	–	µA

19.5 Low voltage reset characteristics

Table 79. Low Voltage Reset Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Detection level	V_{LVR}	Falling edge voltage		–	1.62	1.77	V
				1.85	2.00	2.15	
				1.98	2.13	2.28	
				2.13	2.28	2.43	
				2.31	2.46	2.61	
				2.47	2.67	2.87	
				2.84	3.04	3.24	
				3.00	3.20	3.40	
				3.35	3.55	3.75	
				3.45	3.75	4.05	
				3.69	3.99	4.29	
				3.95	4.25	4.55	
				4.25	4.55	4.85	
Hysteresis	△V	–		–	100	200	mV
Minimum pulse width	t_{LW}	–		100	–	–	µs
LVR current	I_{LVR}	Enable, All mode	VDD = 5V	–	10.0	20.0	µA
		Disable		–	–	0.1	

19.6 Low voltage indicator characteristics

Table 80. Low Voltage Indicator Characteristics

<table>
<tr><th>Parameter</th><th>Symbol</th><th colspan="2">Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Units</th></tr>
<tr><td rowspan="12">Detection level</td><td rowspan="12">V_{LVI}</td><td colspan="2" rowspan="12">Falling edge voltage</td><td>1.85</td><td>2.00</td><td>2.15</td><td rowspan="12">V</td></tr>
<tr><td>1.98</td><td>2.13</td><td>2.28</td></tr>
<tr><td>2.13</td><td>2.28</td><td>2.43</td></tr>
<tr><td>2.31</td><td>2.46</td><td>2.61</td></tr>
<tr><td>2.47</td><td>2.67</td><td>2.87</td></tr>
<tr><td>2.84</td><td>3.04</td><td>3.24</td></tr>
<tr><td>3.00</td><td>3.20</td><td>3.40</td></tr>
<tr><td>3.35</td><td>3.55</td><td>3.75</td></tr>
<tr><td>3.45</td><td>3.75</td><td>4.05</td></tr>
<tr><td>3.69</td><td>3.99</td><td>4.29</td></tr>
<tr><td>3.95</td><td>4.25</td><td>4.55</td></tr>
<tr><td>4.25</td><td>4.55</td><td>4.85</td></tr>
<tr><td>Hysteresis</td><td>$\triangle V$</td><td colspan="2">–</td><td>–</td><td>–</td><td>200</td><td>mV</td></tr>
<tr><td>Minimum pulse width</td><td>t_{LW}</td><td colspan="2">–</td><td>100</td><td>–</td><td>–</td><td>µs</td></tr>
<tr><td rowspan="2">LVI current</td><td rowspan="2">I_{LVI}</td><td>Enable, All mode</td><td rowspan="2">VDD = 5V</td><td>–</td><td>10.0</td><td>20.0</td><td rowspan="2">µA</td></tr>
<tr><td>Disable</td><td>–</td><td>–</td><td>0.1</td></tr>
</table>

19.7 High frequency internal RC oscillator characteristics

Table 81. High Frequency Internal RC Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{HIRC}	VDD = 1.8V to 5.5V	–	40	–	MHz
Accuracy	–	T_A = 0 °C to + 50 °C	–	–	±1.5	%
		T_A = -40 °C to +85 °C(Commercial grade)	–	–	±3.5	
		T_A = -40 °C to +105 °C(Industrial grade)	–	–	±4.5	
Clock duty ratio	T_{OD}	–	40	50	60	%
Stabilization time	t_{HFS}	–	–	–	100	µs
IRC current	I_{HIRC}	Enable	–	500	–	µA
		Disable	–	–	0.1	µA

19.8 Internal watchdog timer RC oscillator characteristics

Table 82. Internal Watchdog Timer RC Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{WDTRC}	–	36	40	44	kHz
Stabilization time	t_{WDTS}	–	–	–	1	ms
WDTRC current	I_{WDTRC}	Enable	–	3	6	µA
		Disable	–	–	0.1	

19.9 LCD voltage characteristics

Table 83. LCD Voltage Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
LCD voltage	VLC0	LCD contrast disabled, 1/4 bias		Typx0.95	VDD	Typx1.05	V
		LCD contrast enabled, 1/4 bias, No Panel load	VLCD[3:0]=0x00	Typx0.94	VDD x16/31	Typx1.06	V
			VLCD[3:0]=0x01		VDD x16/30		
			VLCD[3:0]=0x02		VDD x16/29		
			VLCD[3:0]=0x03		VDD x16/28		
			VLCD[3:0]=0x04		VDD x16/27		
			VLCD[3:0]=0x05		VDD x16/26		
			VLCD[3:0]=0x06		VDD x16/25		
			VLCD[3:0]=0x07		VDD x16/24		
			VLCD[3:0]=0x08		VDD x16/23		
			VLCD[3:0]=0x09		VDD x16/22		
			VLCD[3:0]=0x0A		VDD x16/21		
			VLCD[3:0]=0x0B		VDD x16/20		
			VLCD[3:0]=0x0C		VDD x16/19		
			VLCD[3:0]=0x0D		VDD x16/18		
			VLCD[3:0]=0x0E		VDD x16/17		
			VLCD[3:0]=0x0F		VDD x16/16		
LCD mid bias voltage(NOTE)	VLC1	VDD = 2.7V to 5.5V, LCD clock = 0Hz, 1/4 bias, No panel load		Typ-0.2	3/4xVLC0	Typ+0.2	V
	VLC2			Typ-0.2	2/4xVLC0	Typ+0.2	
	VLC3			Typ-0.2	1/4xVLC0	Typ+0.2	
LCD driver output impedance	R_{LO}	VLCD=3V		–	5	10	kΩ
LCD bias dividing resistor	RLCD1	1/4 bias, TA=25°C		7.0	10	13.0	kΩ
	RLCD2			35	50	65	
	RLCD3			56	80	104	
	RLCD4			168	240	312	

NOTE: It is the middle output voltage when the VDD and the VLC0 node are connected.

19.10 DC electrical characteristics

Table 84. DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input High Voltage	V_{IH}	All input pins, nRESET		0.8VDD	–	VDD	V
Input Low Voltage	V_{IL}	All input pins, nRESET		–	–	0.2VDD	V
Input hysteresis	△V	All input pins, nRESET, VDD=3V		100	200	–	mV
Output High Voltage	V_{OH1}	VDD=4.5V, I_{OH1} = – 2mA, All output pins except V_{OH2}		VDD-1.0	–	–	V
	V_{OH2}	VDD=4.5V, T_A=25°C, I_{OH2} = – 15mA, PE		VDD-2.0	–	–	
Output Low Voltage	V_{OL1}	VDD=4.5V, I_{OL1} = 10mA, All output pins except V_{OL2}		–	–	1.0	V
	V_{OL2}	VDD=4.5V, I_{OL2} = 120mA, PD0-PD5		–	1.5	3.0	
Input high leakage current	I_{IH}	All Input ports		–	–	1	µA
Input low leakage current	I_{IL}	All Input ports		– 1	–	–	µA
Pull-up resistor	R_{PU}	V_I=0V, T_A=25°C, All Input ports	VDD=5V	25	50	100	kΩ
			VDD=3V	50	100	200	
		V_I=0V, T_A=25°C, RESETB	VDD=5V	150	250	400	
			VDD=3V	300	500	700	
Pull-down resistor	R_{PD}	V_I=VDD, T_A=25°C, All Input ports	VDD=5V	13	25	50	kΩ
			VDD=3V	25	50	100	
OSC feedback resistor	R_{X1}	XIN=VDD, XOUT=VSS, T_A=25°C, VDD=5V		600	1,200	2,000	kΩ
	R_{X2}	SXIN=VDD, SXOUT=VSS, T_A=25°C, VDD=5V		2.5	5	10	MΩ

19.11 Supply current characteristics

Table 85. Supply Current Characteristics

Parameter	Symbol	Conditions		Typ	Max	Units
Supply current	IDD1 (run)	f_{HIRC} = 40MHz	VDD=5V±10%	6.5	13.0	mA
		f_{HIRC} = 20MHz	VDD=5V±10%	4.0	8.0	
		f_{XIN} = 16MHz	VDD=5V±10%	5.0	10.0	
			VDD=3V±10%	3.5	7.0	
	I_{DD2} (sleep)	f_{HIRC} = 40MHz	VDD=5V±10%	4.0	8.0	mA
		f_{HIRC} = 20MHz	VDD=5V±10%	2.5	5.0	
		f_{XIN} = 16MHz	VDD=5V±10%	3.2	6.4	
			VDD=3V±10%	2.0	4.0	
	I_{DD3}	f_{SUB} = 32.768kHz or f_{WDTRC} = 40kHz, VDD=3V±10%, TA=25°C	Sub run	90	180	uA
	I_{DD4}		Sub sleep	7.5	15.0	
	I_{DD5}	Deep sleep, VDD=5V±10%, TA=25°C		0.5	3.0	

NOTES:

1. fXIN is an external main oscillator, fSUB is an external sub oscillator, fHIRC is a high frequency internal RC oscillator, and fx is the selected system clock.
2. All supply current items don't include the current of an internal watch-dog timer RC (WDTRC) oscillator and peripheral blocks.
3. All supply current items include the current of the power-on reset (POR) block.

19.12 AC characteristics

Table 86. AC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RESETB input low width	t_{RST}	VDD = 5 V	10	–	–	µs
Interrupt input high, low width	t_{IWH}, t_{IWL}	All interrupts, VDD = 5 V	100	–	–	ns
External counter input high, low pulse width	t_{ECWH}, t_{ECWL}	VDD = 5 V All external counter input	100	–	–	
External counter transition time	t_{REC}, t_{FEC}	ECn, VDD = 5 V All external counter input	–	–	20	

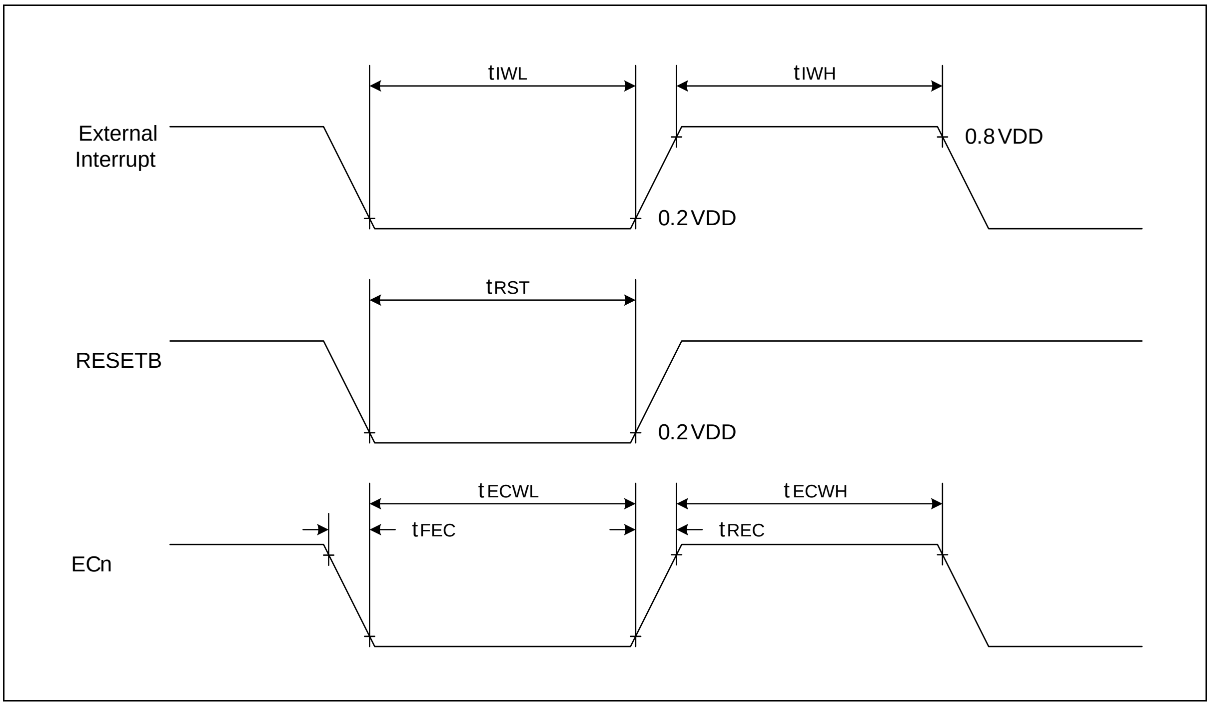


Figure 108. AC Timing

19.13 SPI characteristics

Table 87. SPI Characteristics

(VDD = 2.7V to 5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Clock Pulse Period	t_{SCK}	Internal SCK source	400	–	–	ns
Input Clock Pulse Period		External SCK source	400	–	–	
Output clock high, low pulse width	t_{SCKH}, t_{SCKL}	Internal SCK source	180	–	–	
Input clock high, low pulse width		External SCK source	180	–	–	
First output clock delay time	t_{FOD}	Internal/External SCK source	200	–	–	
Output clock delay time	t_{DS}	–	–	–	100	
Input setup time	t_{DIS}	–	180	–	–	
Input hold time	t_{DIH}	–	180	–	–	

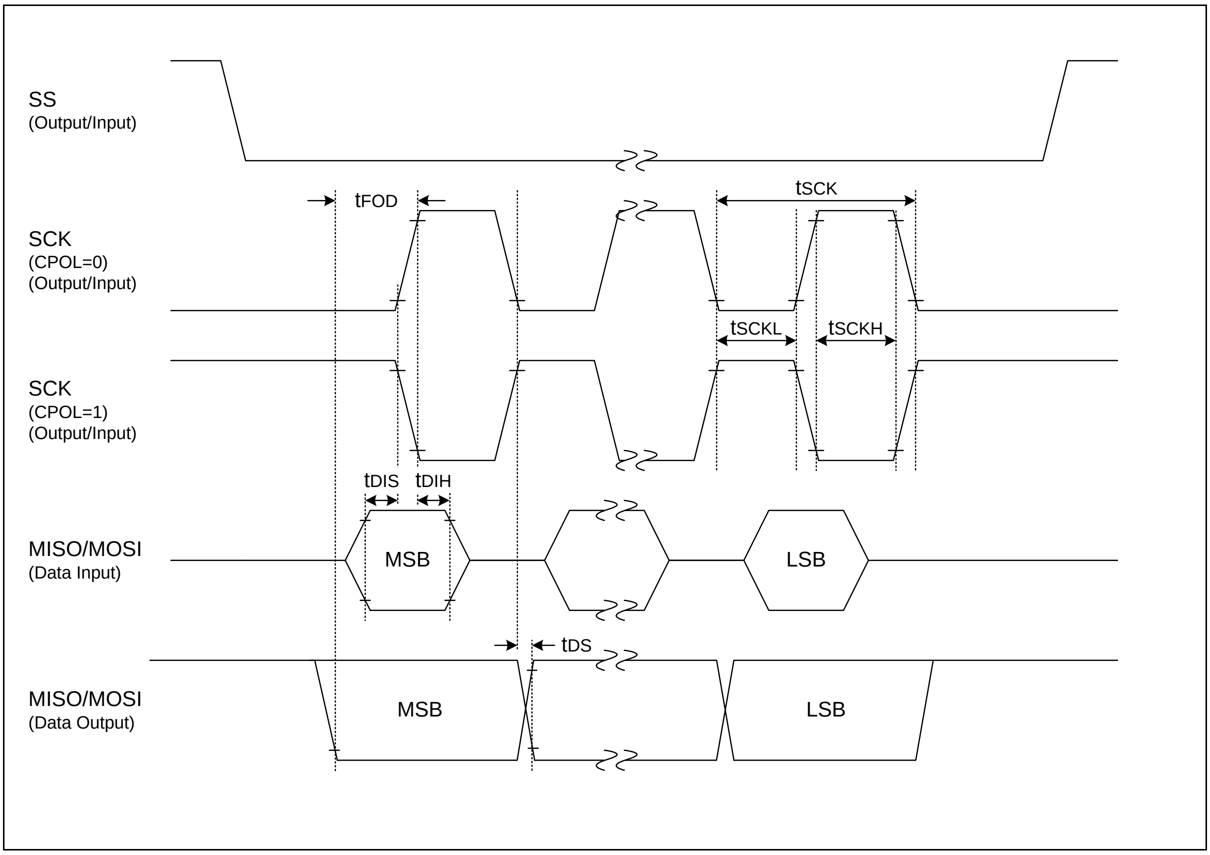


Figure 109. SPI Timing

19.14 I2C characteristics

Table 88. I2C Characteristics

Parameter	**Symbol**	**Standard**		**Fast**		**Fast Plus**		**Units**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	
I2C operating voltage	–	VDD ≥ 1.8V		VDD ≥ 2.0V		VDD ≥ 2.7V		–
Clock frequency	t_{SCL}	0	100	0	400	0	1000	kHz
Clock high pulse width	t_{SCLH}	4.0	–	0.6	–	0.26	–	µs
Clock low pulse width	t_{SCLL}	4.7	–	1.3	–	0.5	–	
Bus free time	t_{BF}	4.7	–	1.3	–	0.5	–	
Start condition setup time	t_{STSU}	4.7	–	0.6	–	0.26	–	
Start condition hold time	t_{STHD}	4.0	–	0.6	–	0.26	–	
Stop condition setup time	t_{SPSU}	4.0	–	0.6	–	0.26	–	
Stop condition hold time	t_{SPHD}	4.0	–	0.6	–	0.26	–	
Output Valid from Clock	t_{VD}	0	–	0	–	0	–	
Data input hold time	t_{DIH}	0	–	0	1.0	0	0.45	
Data input setup time	t_{DIS}	250	–	100	–	50	–	ns

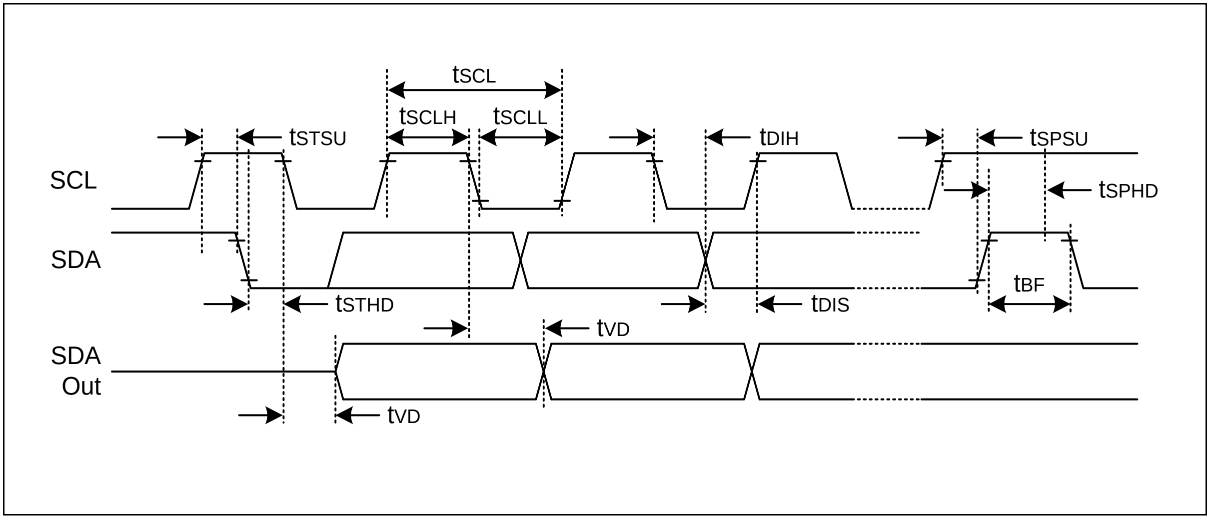


Figure 110. I2C Timing

19.15 UART timing characteristics

Table 89. UART Timing Characteristics (PCLK=11.1MHz)

Parameter	Symbol	Min	Typ	Max	Units
Serial port clock cycle time	t_{SCK}	1,250	tCPU x 16	1,650	ns
Output data setup to clock rising edge	t_{S1}	590	tCPU x 13	–	
Clock rising edge to input data valid	t_{S2}	–	–	590	
Output data hold after clock rising edge	t_{H1}	tCPU – 50	tCPU	–	
Input data hold after clock rising edge	t_{H2}	0	–	–	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	470	tCPU x 8	970	

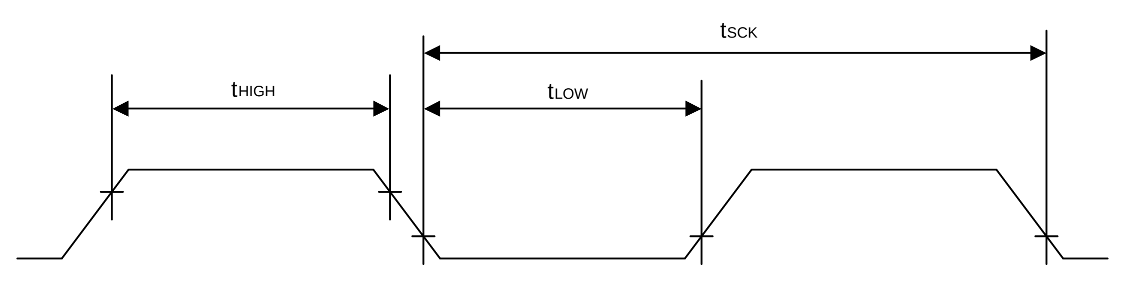


Figure 111. UART Timing Characteristics

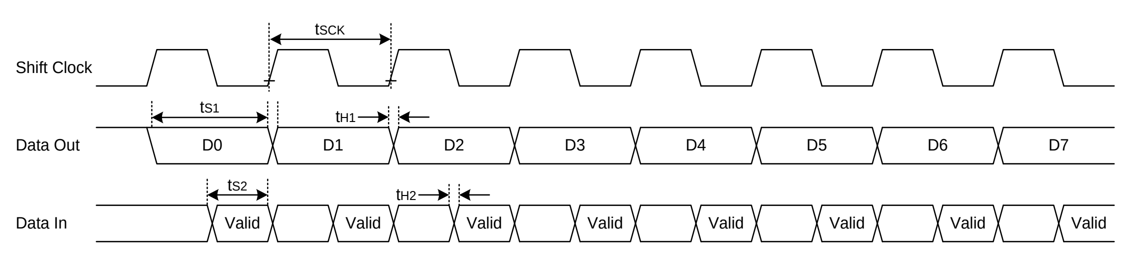


Figure 112. Timing Waveform of UART Module

19.16 Data retention voltage in Stop mode

Table 90. Data Retention Voltage in Stop Mode

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	• V_{DDDR} = 1.8V (T_A=25°C) • Deep sleep mode	–	–	1	µA

19.17 Internal flash characteristics

Table 91. Internal Flash Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Page write time	t_{FSW}	–		–	3.0	3.5	ms
Page erase time	t_{FSE}	–		–	3.0	3.5	
Chip erase time	t_{FCE}	–		–	3.0	3.5	
Flash program voltage	V_{PGM}	On erase/write		2.0	–	5.5	V
System clock frequency	f_{HCLK}	–		2.0	–	–	MHz
Endurance of Write/Erase	NF_{WE}	• Page 0 to 255 • Configure Option Page 1	T_A=25 °C, Page unit	10,000	–	–	Cycles
		Configure Option Page 2/3		100,000			
Retention time	t_{RT}			10	–	–	Years

19.18 Input/output capacitance

Table 92. Input/Output Capacitance

(VDD = 0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input capacitance	C_{IN}	• f=1MHz • Unmeasured pins are connected VSS	–	–	10	pF
Output capacitance	C_{OUT}					
I/O capacitance	C_{IO}					

19.19 Main oscillator characteristics

Table 93. Main Oscillator Characteristics

(VDD = 2.2V to 5.5V)

Oscillator	Parameter	Conditions	Min	Typ	Max	Units
Crystal	Main oscillation frequency	2.7 V to 5.5 V	2.0	–	16.0	MHz
Ceramic Oscillator	Main oscillation frequency	2.2 V to 5.5 V	2.0	–	4.2	
		2.7 V to 5.5 V	2.0	–	16.0	
External Clock	XIN input frequency	3.0 V to 5.5 V	2.0	–	40.0	MHz
	External Clock Duty Ratio	–	–	50	–	%

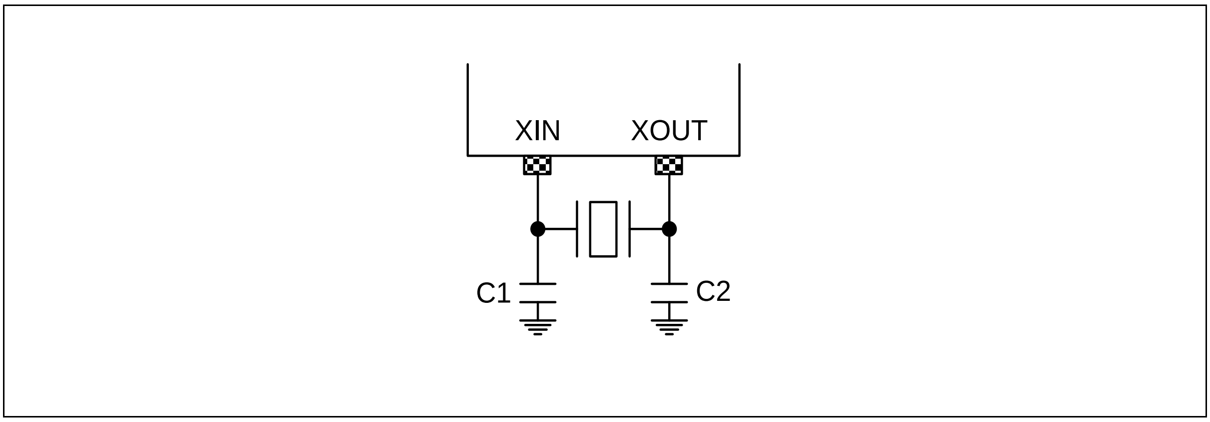


Figure 113. Crystal/Ceramic Oscillator

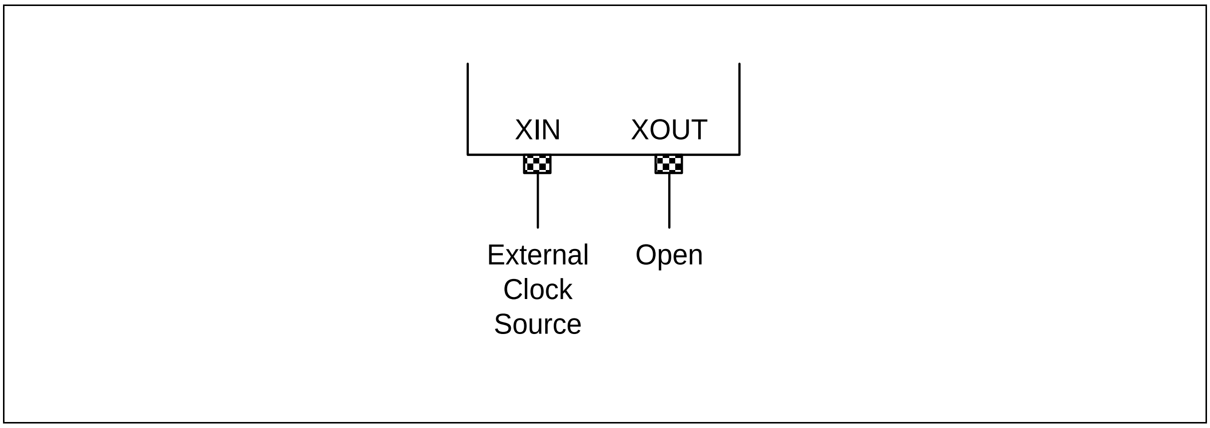


Figure 114. External Clock

19.20 Sub-oscillator characteristics

Table 94. Sub-oscillator Characteristics

Oscillator	Parameter	Conditions	Min	Typ	Max	Units
Crystal	Sub oscillation frequency	–	32	32.768	38	kHz
External Clock	SXIN input frequency		32	–	38	

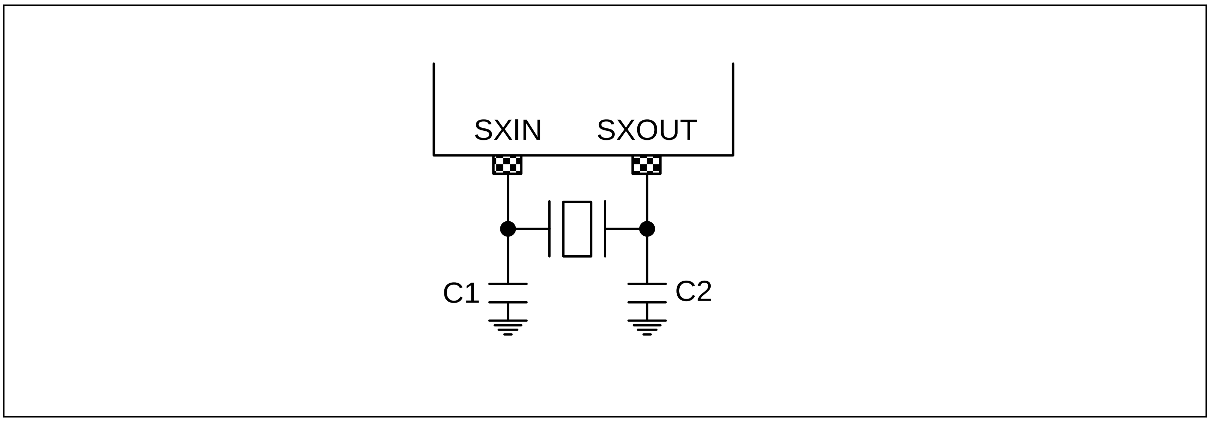


Figure 115. Crystal Oscillator

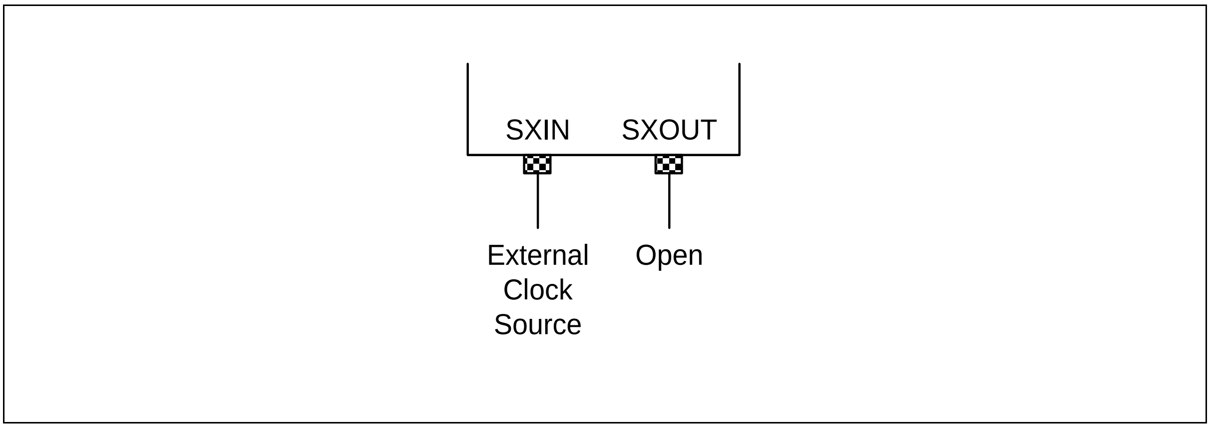


Figure 116. External Clock

19.21 Main oscillation stabilization time

Table 95. Main Oscillation Stabilization Time

Oscillator	Conditions		Min	Typ	Max	Unit
Crystal	• f_{XIN} ≥ 2MHz • Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	VDD = 2.7V to 5.5V	–	–	60	ms
Ceramic		VDD = 2.2V to 5.5V	–	–	10	
External clock	• f_{XIN} = 2.0 to 40MHz • XIN input high and low width (t_{XL}, t_{XH})		12.5	–	250	ns

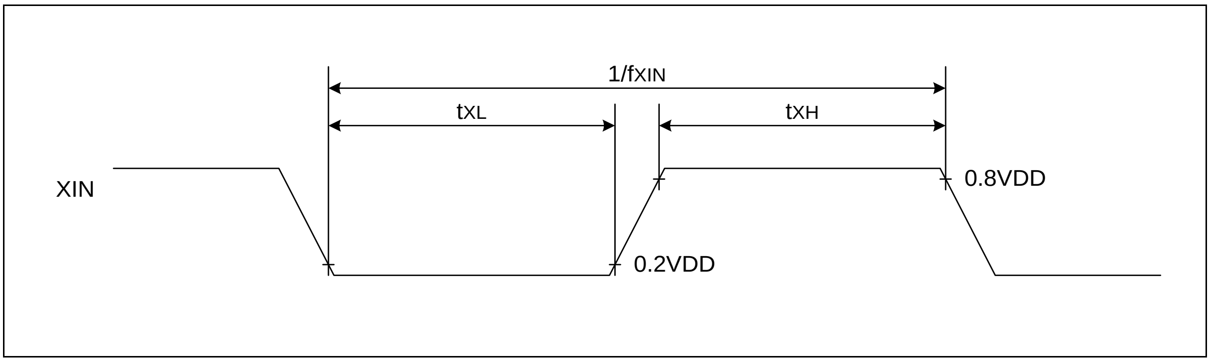


Figure 117. Clock Timing Measurement at XIN

19.22 Sub-oscillation stabilization time

Table 96. Sub-oscillation Stabilization Time

Oscillator	Conditions	Min	Typ.	Max	Units
Crystal	–	–	–	10	sec
	VDD=3V, T_A=25 °C	–	0.7	1.5	
External clock	SXIN input high and low width (t_{XL}, t_{XH})	5	–	15	µs

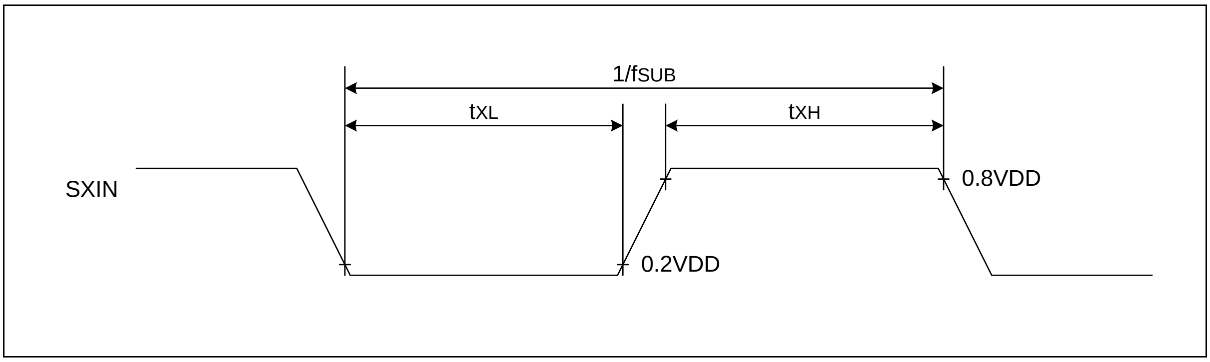


Figure 118. Clock Timing Measurement at SXIN

19.23 Operating voltage range

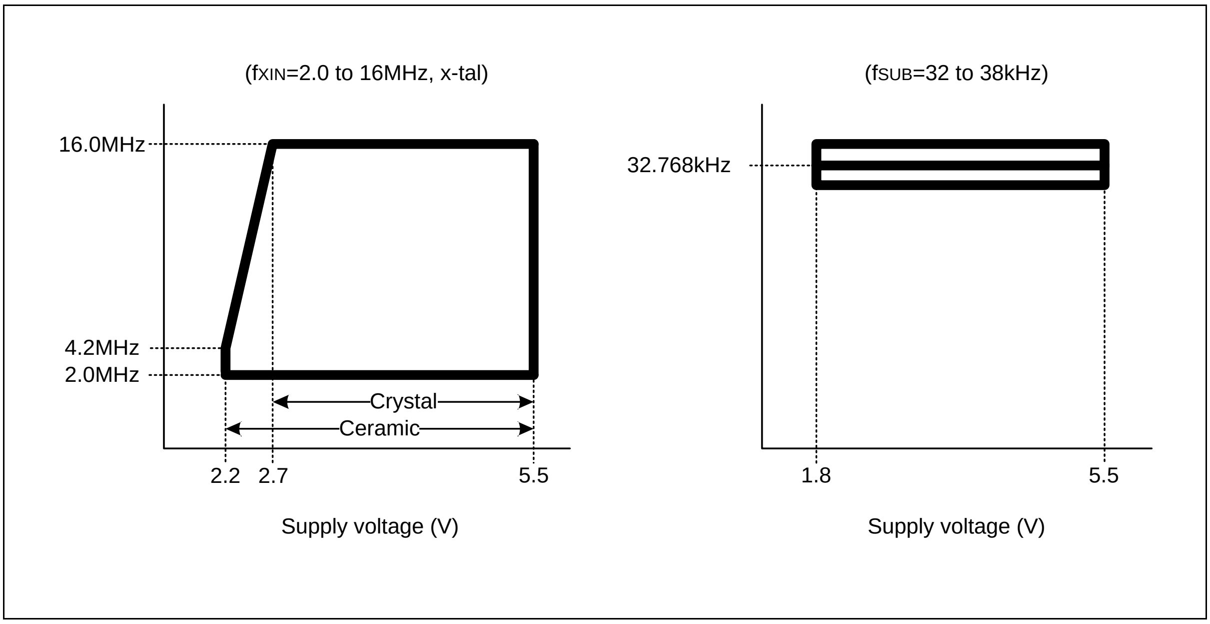


Figure 119. Operating Voltage Range

19.24 Recommended circuit and layout

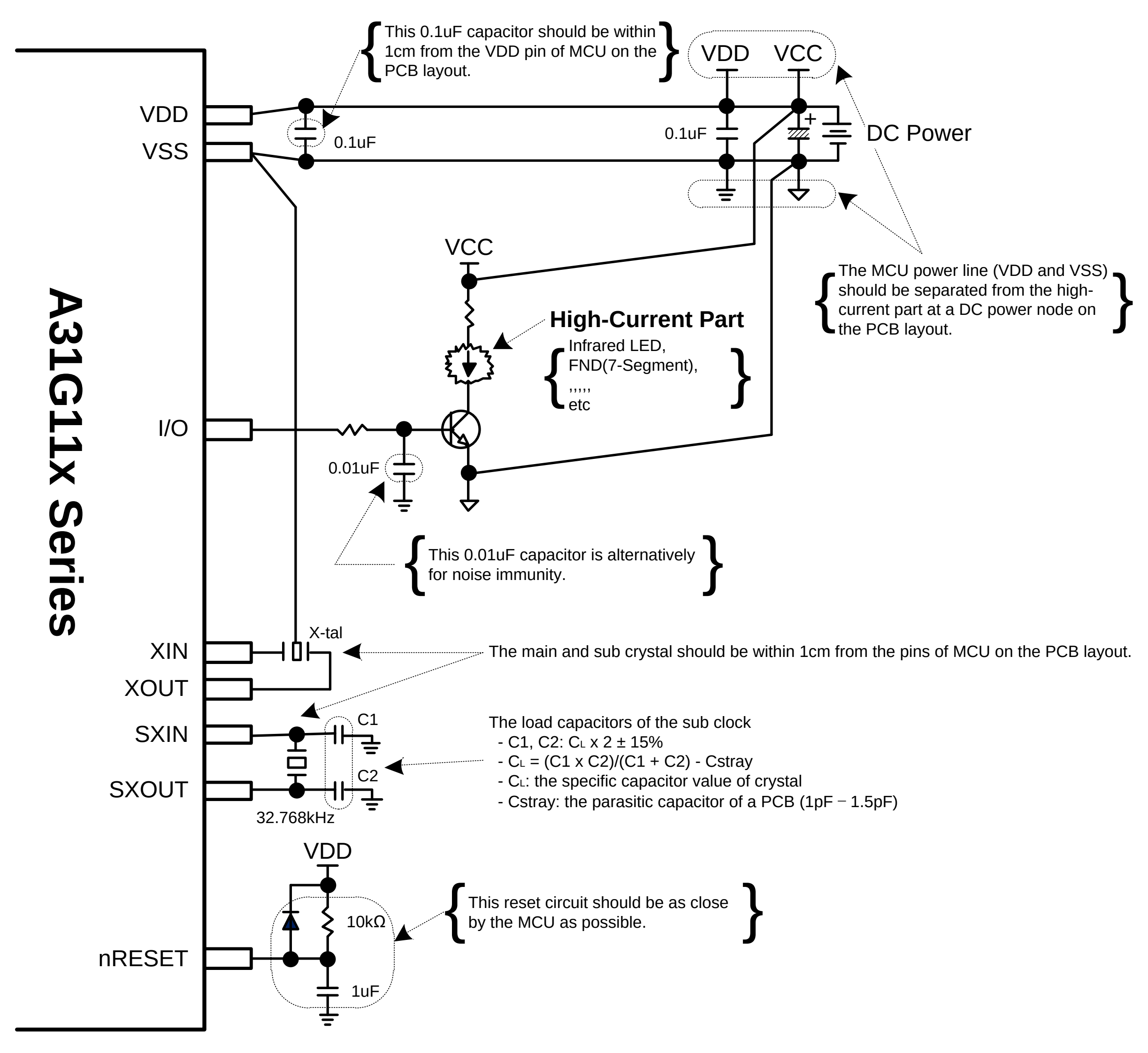
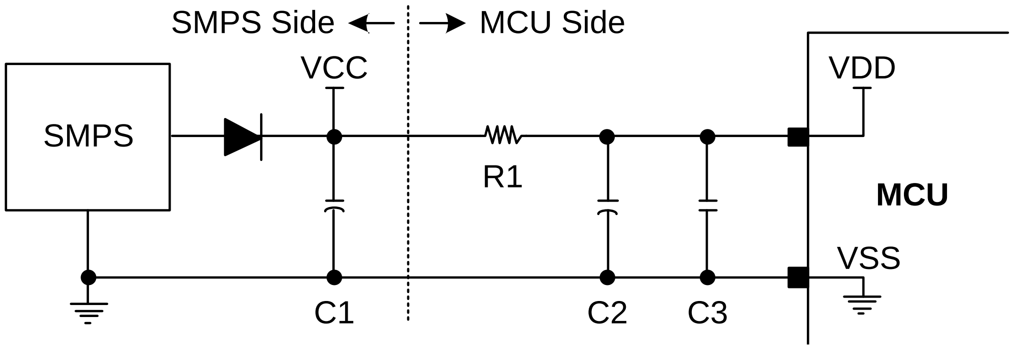


Figure 120. Recommended Circuit and Layout



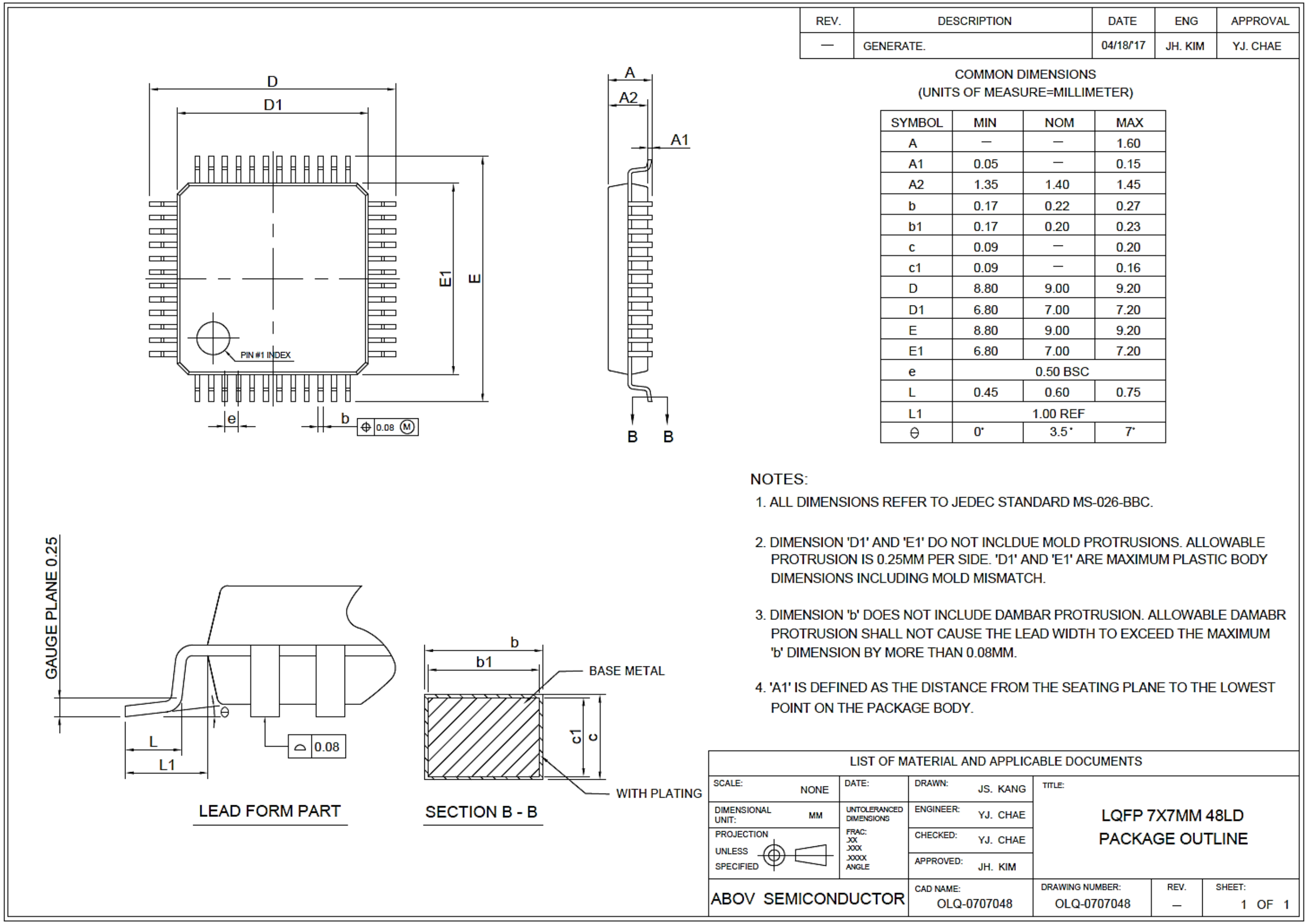
NOTES:

1. Capacitor C1 is to flatten out the voltage of the SMPS power, VCC.
   - Recommended C1: 470uF/25V more
2. Resistor R1 and capacitor C2 are the RC filter for VDD and suppress the ripple of VCC.
   - Recommended R1: 10Ω - 20Ω
   - Recommended C2: 47uF/25V more
   - The R1 and C2 should be as close by the C3 as possible.
3. Capacitor C3 is used for temperature compensation because an electrolytic capacitor becomes worse characteristics at low temperature.
   - Recommended C3: ceramic capacitor 2.2uF more.
   - C3 should be within 1cm from VDD pin of MCU on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc.) when the SMPS supplies the VDD of MCU.

Figure 121. Recommended Circuit and Layout with SMPS Power

20 Package information

20.1 48 LQFP package information



REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/18/'17	JH. KIM	YJ. CHAE

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e		0.50 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026-BBC.
2. DIMENSION 'D1' AND 'E1' DO NOT INCLDUE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. 'D1' AND 'E1' ARE MAXIMUM PLASTIC BODY DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMABR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 'b' DIMENSION BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

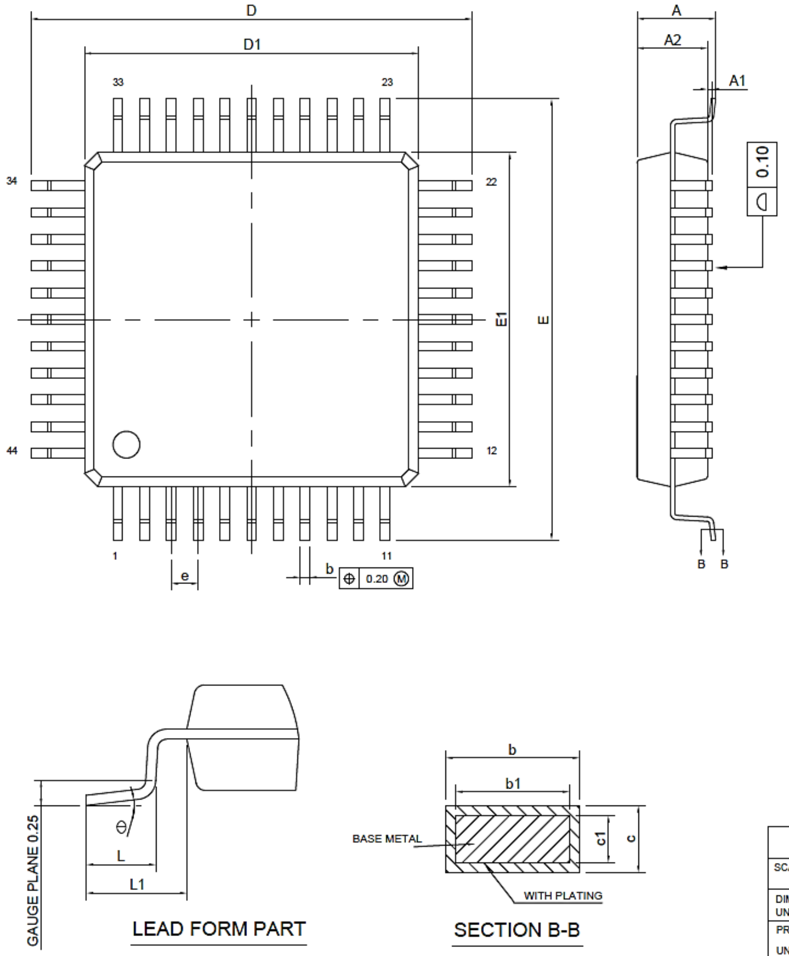
LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE
DIMENSIONAL UNIT: MM
PROJECTION UNLESS SPECIFIED
DATE:
UNTOLERANCED DIMENSIONS FRAC: .XX .XXX .XXXX ANGLE
DRAWN: JS. KANG
ENGINEER: YJ. CHAE
CHECKED: YJ. CHAE
APPROVED: JH. KIM
TITLE: LQFP 7X7MM 48LD PACKAGE OUTLINE
ABOV SEMICONDUCTOR
CAD NAME: OLQ-0707048
DRAWING NUMBER: OLQ-0707048
REV. —
SHEET: 1 OF 1

Figure 122. 48 LQFP 07 x 07 Package Outline

20.2 44 MQFP package information

REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/18/'17	JH. KIM	YJ. CHAE



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	2.45
A1	0.00	—	0.25
A2	1.80	2.10	2.20
b	0.28	—	0.45
b1	0.28	0.35	0.41
c	0.11	—	0.23
c1	0.11	0.15	0.19
D	12.90	13.20	13.50
D1	9.80	10.00	10.20
E	12.90	13.20	13.50
E1	9.80	10.00	10.20
e		0.80BSC	
L	0.60	—	1.03
L1		1.60 BSC	
θ	0°	—	8°

NOTES:

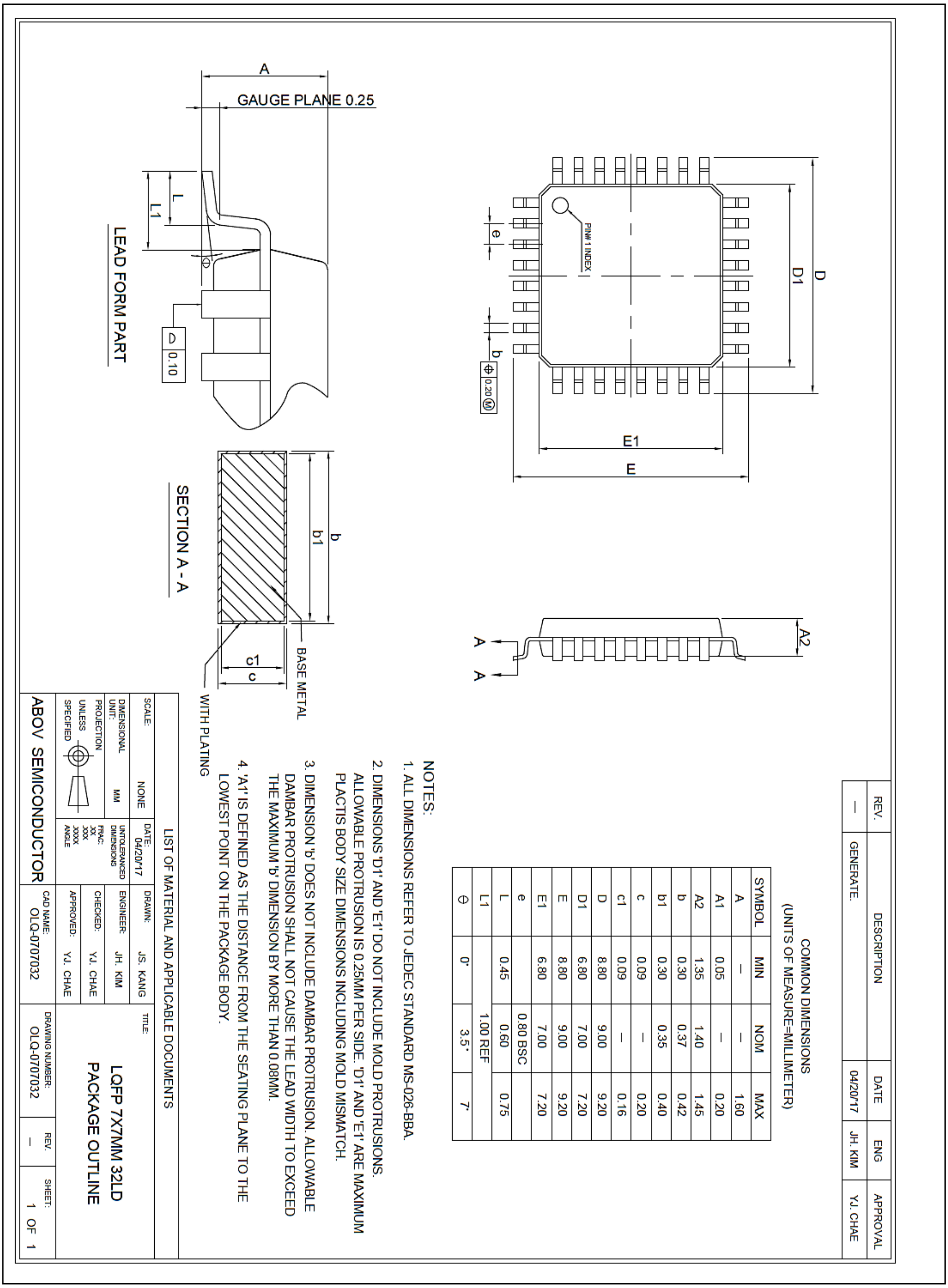
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-022-AB.
2. DIMENSIONS 'D1' AND 'E1' DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. DIMENSIONS 'D1' AND 'E1' DO INCLUDE MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'b' MAXIMUM BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE
DIMENSIONAL UNIT: MM
PROJECTION UNLESS SPECIFIED
DATE: 04/18/'17
UNTOLERANCED DIMENSIONS
FRAC:
.XX
.XXX
.XXXX
ANGLE
DRAWN: JS. KANG
ENGINEER: JH. KIM
CHECKED: YJ. CHAE
APPROVED: YJ. CHAE
TITLE: MQFP 10X10MM 44LD PACKAGE OUTLINE
ABOV SEMICONDUCTOR
CAD NAME: OMQ-1010044
DRAWING NUMBER: OMQ-1010044
REV. —
SHEET: 1 OF 1

Figure 123. 44 MQFP 10 x 10 Package Outline

20.3 32 LQFP package information



REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/20/'17	JH. KIM	YJ. CHAE

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.20
A2	1.35	1.40	1.45
b	0.30	0.37	0.42
b1	0.30	0.35	0.40
c	0.09	—	0.20
c1	0.09	—	0.16
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e		0.80 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

NOTES:

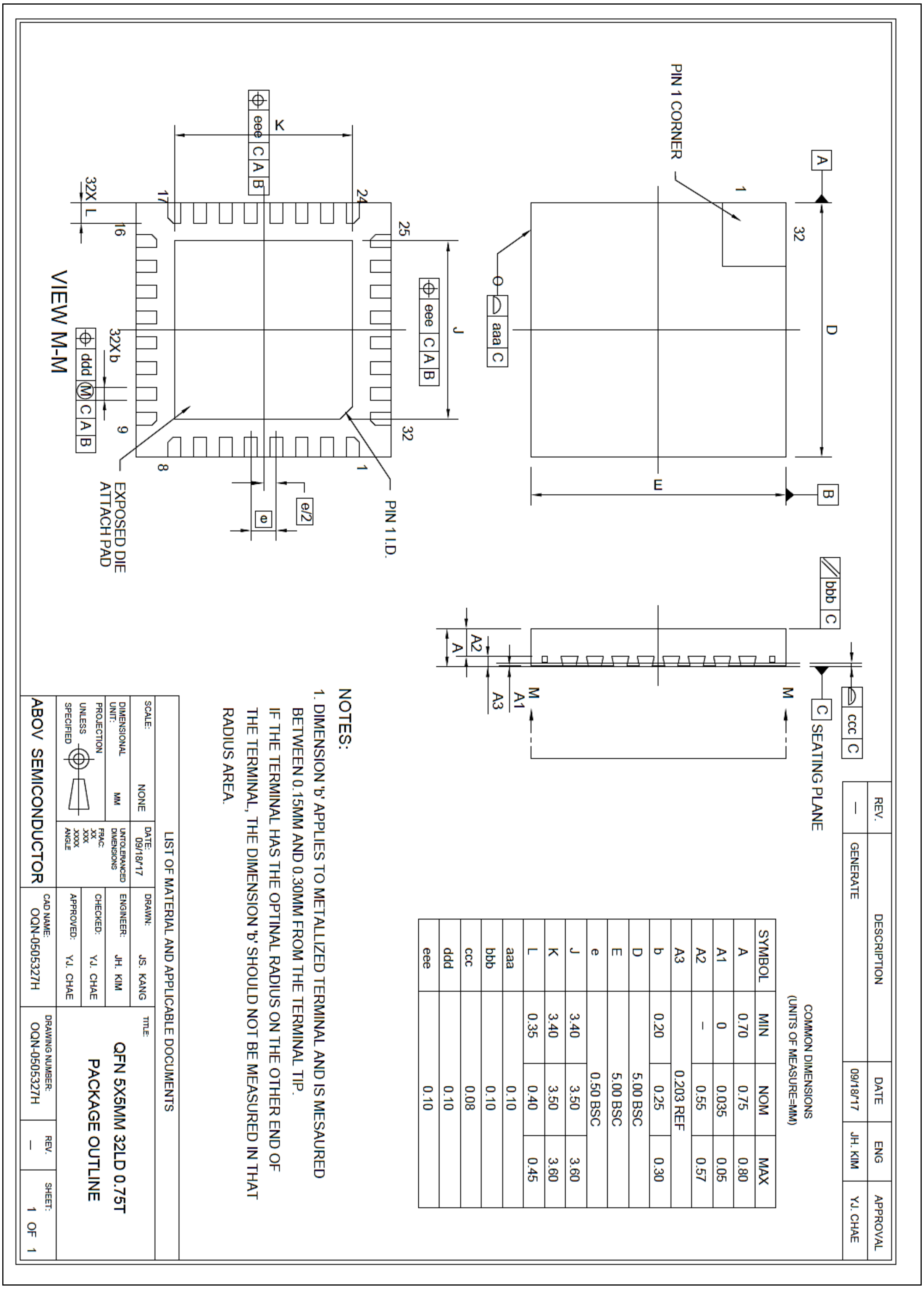
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026-BBA.
2. DIMENSIONS 'D1' AND 'E1' DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. 'D1' AND 'E1' ARE MAXIMUM PLACTIS BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 'b' DIMENSION BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE
DATE: 04/20/'17
DRAWN: JS. KANG
TITLE: LQFP 7X7MM 32LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM
UNTOLERANCED DIMENSIONS
ENGINEER: JH. KIM
PROJECTION UNLESS SPECIFIED
FRAC: .X .XX .XXX .XXXX ANGLE
CHECKED: YJ. CHAE
APPROVED: YJ. CHAE
ABOV SEMICONDUCTOR
CAD NAME: OLQ-0707032
DRAWING NUMBER: OLQ-0707032
REV: —
SHEET: 1 OF 1

Figure 124. 32 LQFP 07 x 07 Package Outline

20.4 32 QFN package information



COMMON DIMENSIONS
(UNITS OF MEASURE=MM)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.035	0.05
A2	–	0.55	0.57
A3		0.203 REF	
b	0.20	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
J	3.40	3.50	3.60
K	3.40	3.50	3.60
L	0.35	0.40	0.45
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.10	

REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE	09/18/17	JH. KIM	YJ. CHAE

NOTES:

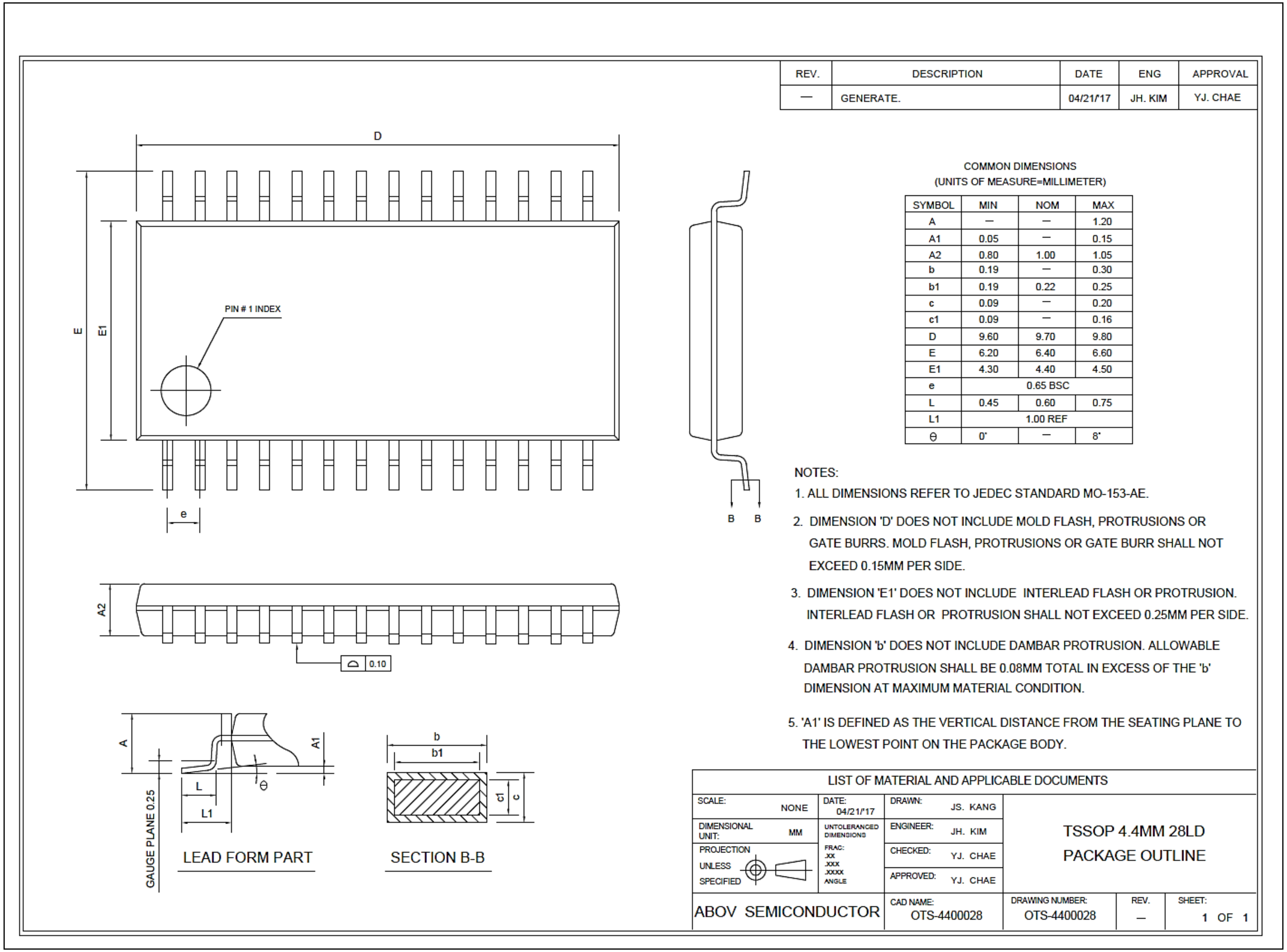
1. DIMENSION 'b' APPLIES TO METALLIZED TERMINAL AND IS MESAURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTINAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION 'b' SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE
DATE: 09/18/17
DRAWN: JS. KANG
TITLE: QFN 5X5MM 32LD 0.75T PACKAGE OUTLINE
DIMENSIONAL UNIT: MM
UNTOLERANCED DIMENSIONS FRAC: .XX .XXX .XXXX ANGLE
ENGINEER: JH. KIM
PROJECTION UNLESS SPECIFIED
CHECKED: YJ. CHAE
APPROVED: YJ. CHAE
ABOV SEMICONDUCTOR
CAD NAME: OQN-0505327H
DRAWING NUMBER: OQN-0505327H
REV. —
SHEET: 1 OF 1

Figure 125. 32 QFN 05 x 05 Package Outline

20.5 28 TSSOP package information



REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/21/'17	JH. KIM	YJ. CHAE

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
b1	0.19	0.22	0.25
c	0.09	—	0.20
c1	0.09	—	0.16
D	9.60	9.70	9.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	—	8°

NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD MO-153-AE.
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURR SHALL NOT EXCEED 0.15MM PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.
4. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. 'A1' IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE
DATE: 04/21/'17
DRAWN: JS. KANG
DIMENSIONAL UNIT: MM
UNTOLERANCED DIMENSIONS
ENGINEER: JH. KIM
PROJECTION
FRAC:
.XX
.XXX
.XXXX
ANGLE
CHECKED: YJ. CHAE
UNLESS SPECIFIED
APPROVED: YJ. CHAE

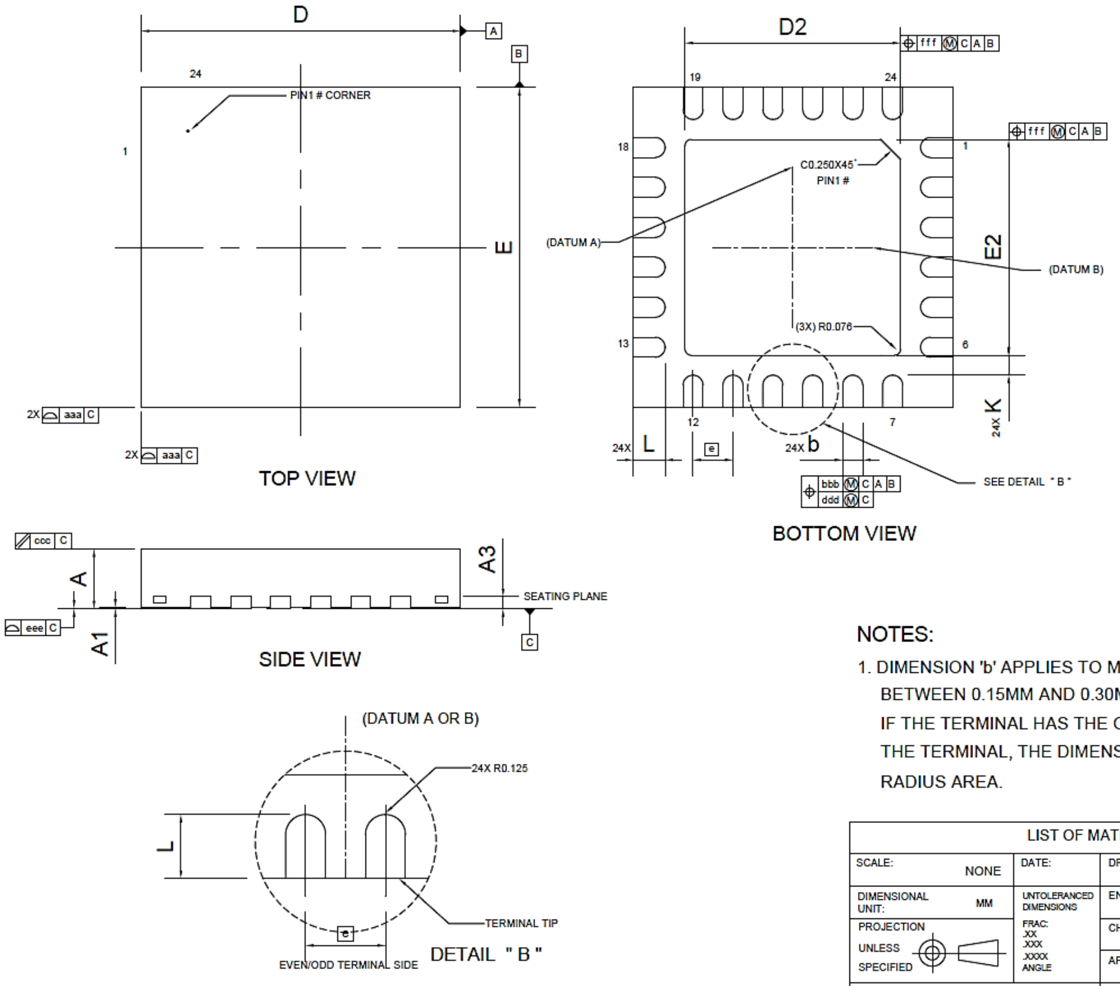
TSSOP 4.4MM 28LD
PACKAGE OUTLINE

ABOV SEMICONDUCTOR
CAD NAME: OTS-4400028
DRAWING NUMBER: OTS-4400028
REV. —
SHEET: 1 OF 1

Figure 126. 28 TSSOP Package Outline

20.6 24 QFN package information

REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE	09/18/'17	JH. KIM	YJ. CHAE



COMMON DIMENSIONS
(UNITS OF MEASURE=MM)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	–	0.20 REF	–
b	0.18	0.25	0.30
D		4.00 BSC	
E		4.00 BSC	
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	–	–
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
f f f		0.10	

NOTES:

1. DIMENSION 'b' APPLIES TO METALLIZED TERMINAL AND IS MESAURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTINAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION 'b' SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE:	DRAWN: JS. KANG	TITLE: QFN 4X4MM 24LD 0.75T PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS	ENGINEER: JH. KIM	
PROJECTION UNLESS SPECIFIED	FRAC: .XX .XXX .XXXX ANGLE	CHECKED: YJ. CHAE	
		APPROVED: YJ. CHAE	
ABOV SEMICONDUCTOR		CAD NAME: OQN-040424A	DRAWING NUMBER: OQN-040424A REV. — SHEET: 1 OF 1

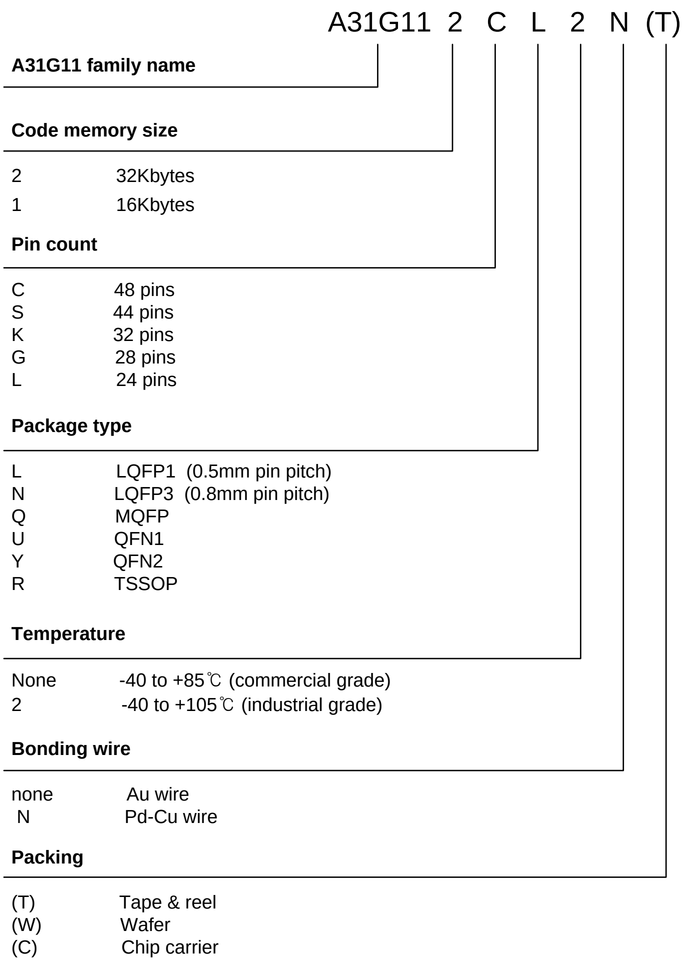
Figure 127. 24 QFN 04 x 04 Package Outline

21 Ordering information

Table 97. A31G11x series Ordering Information

Part Number	Flash	SRAM	USART	UART	I2C	TIMER	ADC	I/O	Package
A31G112CL	32KB	4KB	2	2	2	6	11 ch	45	48LQFP
A31G112SQ*	32KB	4KB	2	2	2	6	9 ch	41	44MQFP
A31G112KN*	32KB	4KB	2	2	2	6	5 ch	29	32LQFP
A31G112KU*	32KB	4KB	2	2	2	6	5 ch	29	32QFN
A31G112KY*	32KB	4KB	2(UART: 2, SPI: 1)	1	2	6	9 ch	29	32QFN
A31G112GR*	32KB	4KB	1	1	2	6	5 ch	25	28TSSOP
A31G112LU*	32KB	4KB	1	1	2	6	4 ch	21	24QFN
A31G111KN*	16KB	4KB	2	2	2	6	5 ch	29	32LQFP
A31G111KU*	16KB	4KB	2	2	2	6	5 ch	29	32QFN
A31G111GR*	16KB	4KB	1	1	2	6	5 ch	25	28TSSOP
A31G111LU*	16KB	4KB	1	1	2	6	4 ch	21	24QFN

* For available options or further information on the devices with "*" marks, please contact the ABOV Sales Office.



A31G11 2 C L 2 N (T)

A31G11 family name

Code memory size

2	32Kbytes
1	16Kbytes

Pin count

C	48 pins
S	44 pins
K	32 pins
G	28 pins
L	24 pins

Package type

L	LQFP1 (0.5mm pin pitch)
N	LQFP3 (0.8mm pin pitch)
Q	MQFP
U	QFN1
Y	QFN2
R	TSSOP

Temperature

None	-40 to +85℃ (commercial grade)
2	-40 to +105℃ (industrial grade)

Bonding wire

none	Au wire
N	Pd-Cu wire

Packing

(T)	Tape & reel
(W)	Wafer
(C)	Chip carrier

NOTE: For more information on any aspect of this device, please contact your nearest distributor or ABOV sales offices.

Figure 128. A31G11x series Numbering Nomenclature

22 Development tools

This chapter introduces wide range of development tools for A31G11x series. ABOV offers software tools, debuggers, and programmers to help a user in generating right results to match target applications. ABOV supports entire development ecosystem of the customers.

22.1 Compiler

ABOV semiconductor does not provide any compiler for A31G11x series. However, since A31G11x series have ARM's high-speed 32-bit Cortex-M0+ Cores for their CPU, you can use all kinds of third party's standard compiler such as Keil C Compiler. These compilers' output debug information can be integrated with our A-Link and A-Link Pro. Please visit our website www.abovsemi.com for more information regarding the A-Link and A-Link Pro.

22.2 Debugger

The A-Link and A-Link Pro support ABOV Semiconductor's A31G11x series MCU emulation in SWD Interface. The A-Link and A-Link Pro use two wires interfacing between PC and MCU, which is attached to user's system. The A-Link and A-Link Pro can read or change the value of MCU's internal memory and I/O peripherals. In addition, the A-Link and A-Link Pro control MCU's internal debugging logic. This means A-Link and A-Link Pro control emulation, step run, monitoring and many more functions regarding debugging.

The A-Link and A-Link Pro run underneath MS operating system such as MS-Windows NT/ 2000/ XP/ Vista/ 7/ 8/ 8.1/ 10 (32-bit, 64-bit).

Programming information using the A-Link and A-Link Pro are provided in Figure 129. More detailed information about the A-Link and A-Link Pro, please visit our website www.abovsemi.com and download the debugger S/W and documents.

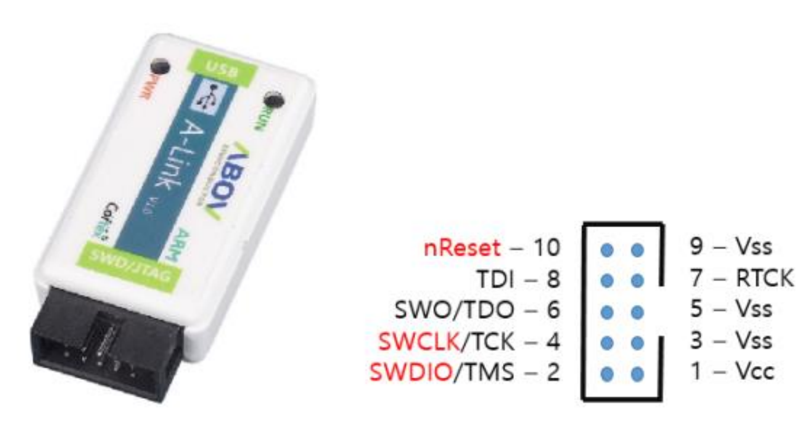


Figure 129. A-Link and Pin Descriptions

22.3 Programmer

E-PGM+

E-PGM+ is a single programmer, and allows a user to program on the device directly.

- Support ABOV devices
- 2~5 times faster than S-PGM+
- Main controller: 32-bit MCU @ 72MHz
- Buffer memory: 1MB

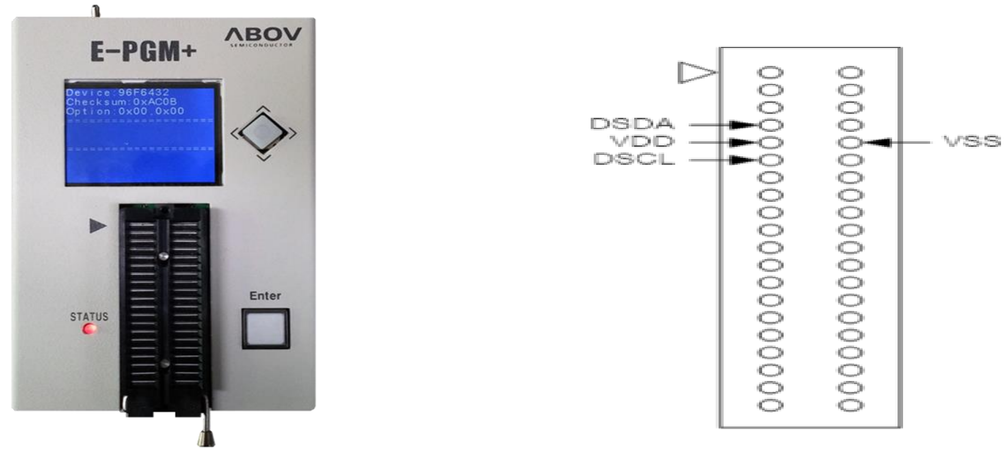


Figure 130. E-PGM+ (Single Writer) and Pin Descriptions

Gang programmer

E-Gang4 and E-Gang6 allows a user to program on multiple devices at a time. They run not only in PC controlled mode but also in standalone mode without PC control. USB interface is available and it is easy to connect to the handler.

Figure 131. E-Gang4 and E-Gang6 (for Mass Production)

22.4 SWD debug mode and E-PGM+ connection

Connections for SWD debugger interface or E-PGM+ is described in figure 115.

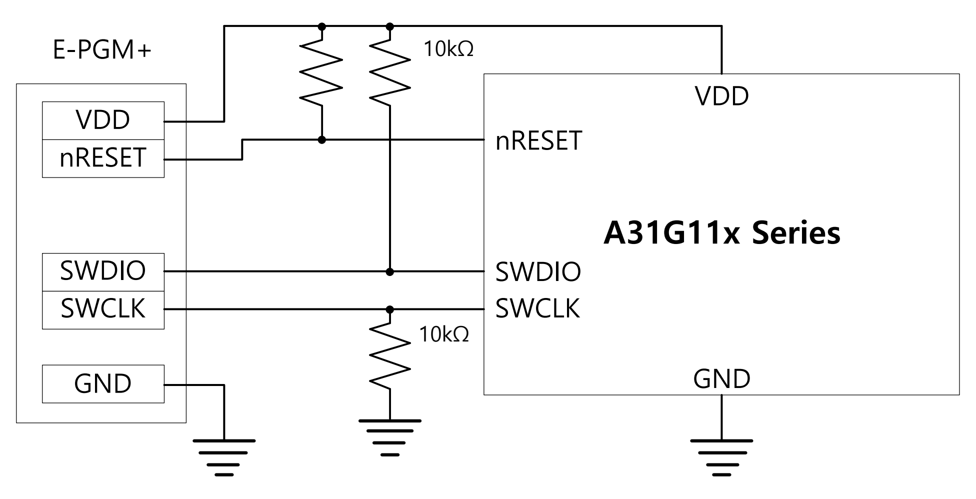


Figure 132. Connection between A31G11x series and E-PGM+ using SWD Debugger Interface

Revision history

Date	Version	Description
Dec.30, 2016	1.0.0	1st creation
Feb.24, 2017	1.1.0	Modify incorrect grammar as a whole. Add a Section 3, chapter 2.1.24 Recommended Circuit and Layout. Add a Section 3, chapter 2.1.25 Recommended Circuit and Layout with SMPS Power.
Mar.15, 2017	1.1.1	Section 2, Chapter 1.6.7 NMISRCR.NMISRC bit description modify Section 2, Figure 15.2 title modify
Jul.12, 2017	1.1.2	Typos modify
Nov.28, 2017	1.1.3	Add a IDD6 in Section3, chapter 2.1.11 Supply Current Charateristics.
Dec.11, 2017	1.1.4	Format Standardization. Remove a IDD6 in Section3, chapter 2.1.11 Supply Current Charateristics.
Jan.18, 2018	1.1.5	Add Package Naming Rule
Aug.23, 2018	1.2.0	Change Flash Endurance Times Remove LVR 1.68V/1.77V/1.88V, LVI 1.88V Modify Notes of Clock Monitoring Circuit Diagram in SYSTEM CONTROL UNIT. Modify Notes of Figure 10.1 Block diagram in TIMER COUNTER 30. Update All Package Dimension Remove Special Test in Device Nomenclature Update Operating Temperature Typos modify
Nov.26, 2019	1.2.1	Add a package type, "A31G112KY(32 QFN)". Add a table, "Section 2, Table 1.2 Functional table on current mode". Add notes, "Section 2, Chapter 12. USART 10/11, Figure 12.2 SPIn Block diagram". Change value, "Section 3, Chapter 2.1.4 Power-On Reset Characteristics". Add a item, "Section 3, Chapter 2.1.17 Internal Flash ROM Characteristics". Modify note, "Section 2, Chapter 16.2.1 CRC Control Register". Typos modify.
Jan.16, 2020	1.2.2	Add notes, "Section 1, Chapter 1. OVERVIEW, Figure 1.3 ~ Figure 1.8". Modify a figure, "Section 1, Chapter 3. BOOT MODE, Figure 3.3". Typos modify
Apr.09, 2020	1.30	Applied a new format to this document.
Nov.30, 2020	1.31	Add a note about disabling "clock monitoring function", "Chapter 5.6.19 SCU_CMONCR", clock monitoring control register. Add notes about TXEn bit and RXEn bit, "Chapter 14.3.1 USARTn_CR1" USARTn control register 1.
Jun.24, 2021	1.32	Modify Exposed pad connection of QFN packages
Oct.28, 2022	1.40	Change the document format.

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