A31T214/216
User's Manual

32-bit Cortex-M0+ based Touch Sensing Microcontroller

User's Manual Version 1.10

Introduction

This user's manual contains complete information for application developers who use A31T214/216 series for their specific needs. To meet the requirements for the complexity and high performance in consumer electronics, A31T214/216 incorporates the ARM's high-speed 32-bit Cortex-M0+ Core, and flash memory of up to 256KB and SRAM of 16KB. Building on the very successful Cortex-M0+ processor, the ARM® Cortex®-M0+ retains full instruction set and tool compatibility, while further reducing energy consumption and increasing performance.

In addition, A31T214/216 series includes 16-bit/32-bit timers, Watch timer, 12-bit ADC, CRC generator, USART, I2C, SPI, and DMA. It also has a POR, LVR, LVI, and an internal RC oscillator.

A31T214/216 series supports SLEEP/ POWER DOWN mode to reduce power consumption. It supports operation voltage of 1.8V to 5.5V.

Since A31T214/216 series provides highly flexible and cost effective solutions for many embedded control applications, it can be used for various appliances such as home electronics.

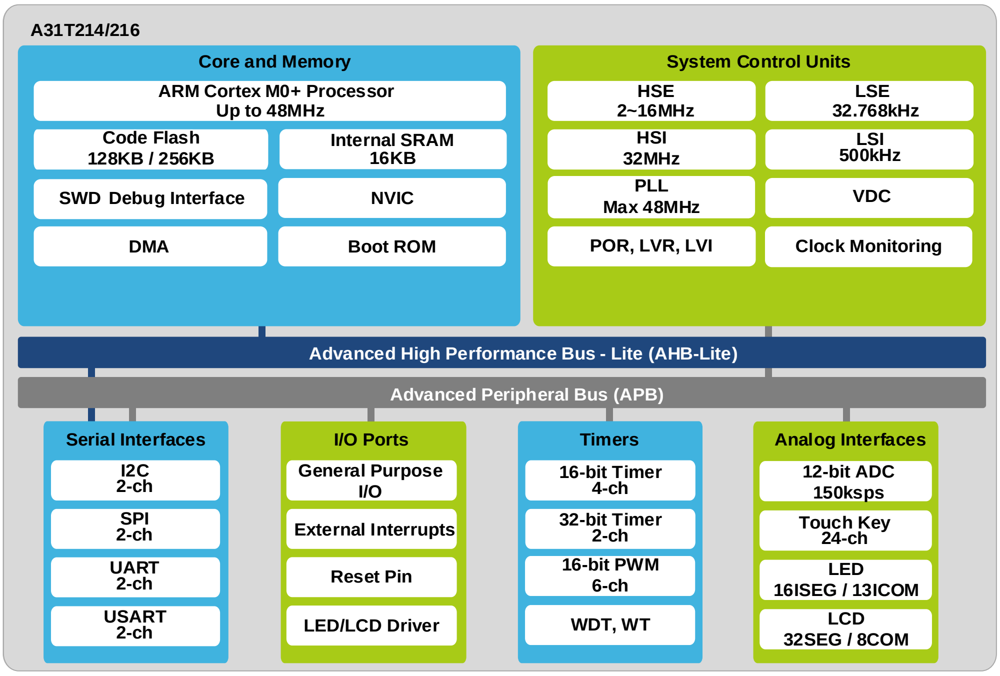

Figure 1. A31T214/216 Block Diagram

Reference document

- Document 'DDI 0484C' is provided by ARM and contains information of Cortex-M0+.
- A31T214/216 Datasheet is provided by ABOV and available at www.abovsemi.com.

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1 Description

A31T214/216 series is a 32-bit touch sensing microcontroller with up to 256Kbytes of flash memory. This powerful microcontroller provides effective solutions to various electrical appliances which require both low power consumption and high performance.

1.1 Device overview

In this section, features of A31T214/216 and peripheral counts are introduced.

Table 1. A31T214/216 Device Features and Peripheral Counts

Peripherals		Description
Core	CPU	• High Performance Low-Power Cortex-M0+ Core • 32-bit ARM Cortex-M0+ CPU
	Interrupt	• NVIC (Nested-Vectored Interrupt Controller) • Up to 32 peripheral interrupts supported.
Memory	Code flash	• A31T214: 128Kbytes code flash memory • A31T216: 256Kbytes code flash memory
	SRAM	• 16 Kbytes SRAM
System Control Unit (SCU)	Operating frequency	• Up to 48MHz
	Clock	• High speed internal oscillator (HSI): 32MHz • Low speed internal oscillator (LSI): 500kHz • External main oscillator (HSE): 2MHz to 16MHz • External sub-oscillator (LSE): 32.768kHz • Phase-locked loop (PLL) frequency generator generates a high-speed clock (up to 48MHz)

Table 1. A31T214/216 Device Features and Peripheral Counts (continued)

Peripherals		Description
System Control Unit (SCU)	Clock monitoring	• System Fail-Safe function by Clock Monitoring — External main oscillator(HSE) — External sub oscillator(LSE) — Main system clock (MCLK)
	Operating mode	• RUN mode • SLEEP mode • Power-Down mode
	Reset	• nRESET pin reset • Core reset • Software reset • POR (Power On Reset) • LVR (Low Voltage Reset) • WDTR (Watch Dog Timer Reset) • Reset due to clock oscillating error
General Purpose I/O (GPIO)		• 64-Pin: 60-Ports • 48-Pin: 44-Ports • 44-Pin: 40-Ports • 40-Pin: 38-Ports
Direct Memory Access controller (DMA)		• 4-ch Direct Memory Access (DMA) channels
Watch Timer (WT)		• 12-bit counter: 1-ch
Watchdog Timer (WDT)		• 24-bit down counter timer: 1-ch • Reset and periodic interrupts are supported
TIMER	Timer1x	• 16bit: 4-ch — Periodic timer mode, One-shot timer mode, PWM pulse mode, Capture mode
	Timer2x	• 32bit: 2-ch — Periodic timer mode, One-shot timer mode, PWM pulse mode, Capture mode
PWM	Timer30	• 16bit: 6-ch — Periodic timer mode, Back-to-Back mode, Capture mode

Table 1. A31T214 and A31T216 Device Features and Peripheral Counts (continued)

Peripherals		Description
Communication function	USART	• 2-ch
	UART	• 2-ch
	SPI	• 2-ch
	I2C	• 2-ch
ADC		• 12-bit ADC: 150ksps
Capacitive touch switch		• Capacitive Touch Switch — 24-ch (64-pin) — 24-ch (48-pin) — 21-ch (44-pin) — ESD 4K, CS10V
LED Driver		• 16ISEG / 13ICOM (64-pin) — T-type Max (13COM X 12SEG), M-type Max (8COM X 8SEG) • 16ISEG / 13ICOM (48-pin) — T-type Max (13COM X 12SEG), M-type Max (8COM X 8SEG) • 14ISEG / 11ICOM (44-pin) — T-type Max (11COM X 10SEG), M-type Max (7COM X 7SEG) • 16ISEG / 13ICOM (40-pin) — T-type Max (13COM X 12SEG), M-type Max (7COM X 7SEG)
LCD Driver		• 32SEG / 8COM, Max pin [8COM X 27SEG] (64-pin) • 20SEG / 6COM, Max pin [6COM X 17SEG] (48-pin) • 18SEG / 6COM, Max pin [6COM X 15SEG] (44-pin) • 15SEG / 6COM, Max pin [6COM X 12SEG] (40-pin)
CRC calculator (CRC)		• CRC-CCITT, CRC-16
Operating voltage		• 1.8V to 5.5V
Operating temperature		• -40℃ to +105℃
Package		• Four types of package options — 64/48/44-LQFP — 40-QFN

1.2 Block diagram

In Figure 2, A31T214/216 devices with peripherals are described in block diagram.

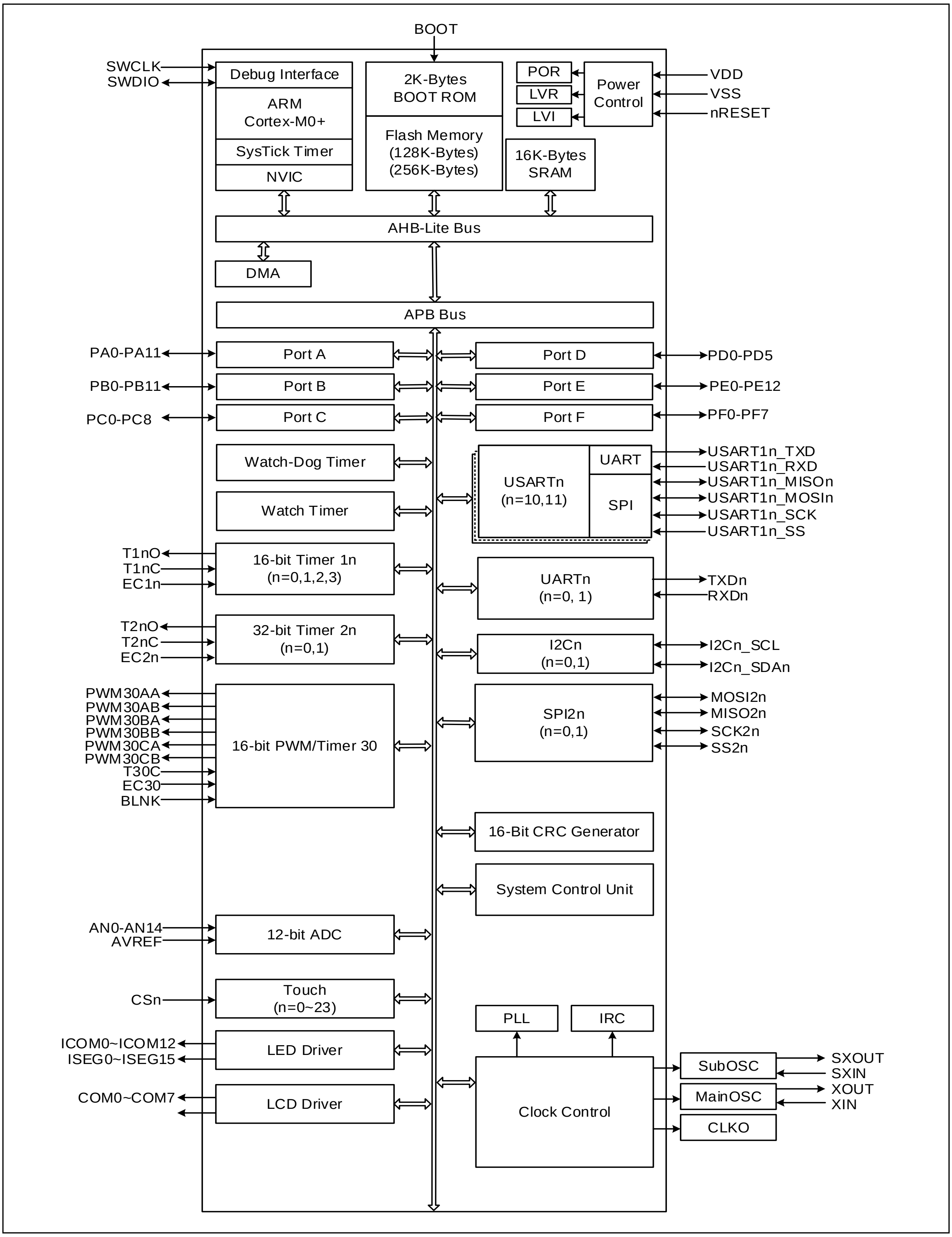


Figure 2. A31T214/216 Block Diagram

2 Pinouts and pin descriptions

A31T214/216 devices' pinouts and pin descriptions are introduced in the following sections.

2.1 Pinouts

2.1.1 A31T21xRLN (64 LQFP)

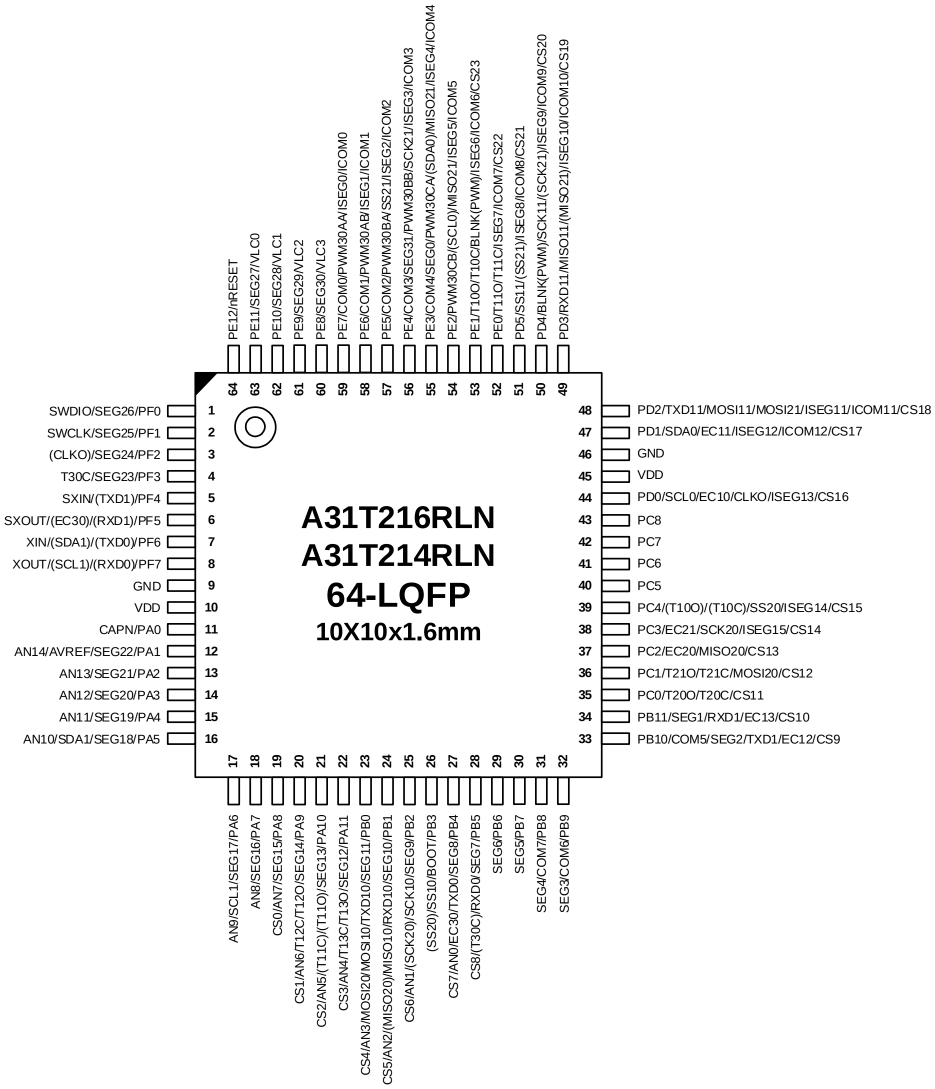

A31T216RLN
A31T214RLN
64-LQFP
10X10x1.6mm
1 SWDIO/SEG26/PF0
2 SWCLK/SEG25/PF1
3 (CLKO)/SEG24/PF2
4 T30C/SEG23/PF3
5 SXIN/(TXD1)/PF4
6 SXOUT/(EC30)/(RXD1)/PF5
7 XIN/(SDA1)/(TXD0)/PF6
8 XOUT/(SCL1)/(RXD0)/PF7
9 GND
10 VDD
11 CAPN/PA0
12 AN14/AVREF/SEG22/PA1
13 AN13/SEG21/PA2
14 AN12/SEG20/PA3
15 AN11/SEG19/PA4
16 AN10/SDA1/SEG18/PA5
17 AN9/SCL1/SEG17/PA6
18 AN8/SEG16/PA7
19 CS0/AN7/SEG15/PA8
20 CS1/AN6/T12C/T12O/SEG14/PA9
21 CS2/AN5/(T11C)/(T11O)/SEG13/PA10
22 CS3/AN4/T13C/T13O/SEG12/PA11
23 CS4/AN3/MOSI20/MOSI10/TXD10/SEG11/PB0
24 CS5/AN2/(MISO20)/MISO10/RXD10/SEG10/PB1
25 CS6/AN1/(SCK20)/SCK10/SEG9/PB2
26 (SS20)/SS10/BOOT/PB3
27 CS7/AN0/EC30/TXD0/SEG8/PB4
28 CS8/(T30C)/RXD0/SEG7/PB5
29 SEG6/PB6
30 SEG5/PB7
31 SEG4/COM7/PB8
32 SEG3/COM6/PB9
33 PB10/COM5/SEG2/TXD1/EC12/CS9
34 PB11/SEG1/RXD1/EC13/CS10
35 PC0/T20O/T20C/CS11
36 PC1/T21O/T21C/MOSI20/CS12
37 PC2/EC20/MISO20/CS13
38 PC3/EC21/SCK20/ISEG15/CS14
39 PC4/(T10O)/(T10C)/SS20/ISEG14/CS15
40 PC5
41 PC6
42 PC7
43 PC8
44 PD0/SCL0/EC10/CLKO/ISEG13/CS16
45 VDD
46 GND
47 PD1/SDA0/EC11/ISEG12/ICOM12/CS17
48 PD2/TXD11/MOSI11/MOSI21/ISEG11/ICOM11/CS18
49 PD3/RXD11/MISO11/(MISO21)/ISEG10/ICOM10/CS19
50 PD4/BLNK(PWM)/SCK11/(SCK21)/ISEG9/ICOM9/CS20
51 PD5/SS11/(SS21)/ISEG8/ICOM8/CS21
52 PE0/T11O/T11C/ISEG7/ICOM7/CS22
53 PE1/T10O/T10C/BLNK(PWM)/ISEG6/ICOM6/CS23
54 PE2/PWM30CB/(SCL0)/MISO21/ISEG5/ICOM5
55 PE3/COM4/SEG0/PWM30CA/(SDA0)/MISO21/ISEG4/ICOM4
56 PE4/COM3/SEG31/PWM30BB/SCK21/ISEG3/ICOM3
57 PE5/COM2/PWM30BA/SS21/ISEG2/ICOM2
58 PE6/COM1/PWM30AB/ISEG1/ICOM1
59 PE7/COM0/PWM30AA/ISEG0/ICOM0
60 PE8/SEG30/VLC3
61 PE9/SEG29/VLC2
62 PE10/SEG28/VLC1
63 PE11/SEG27/VLC0
64 PE12/nRESET

Figure 3. LQFP 64 Pinouts

2.1.2 A31T21xCLN (48 LQFP)

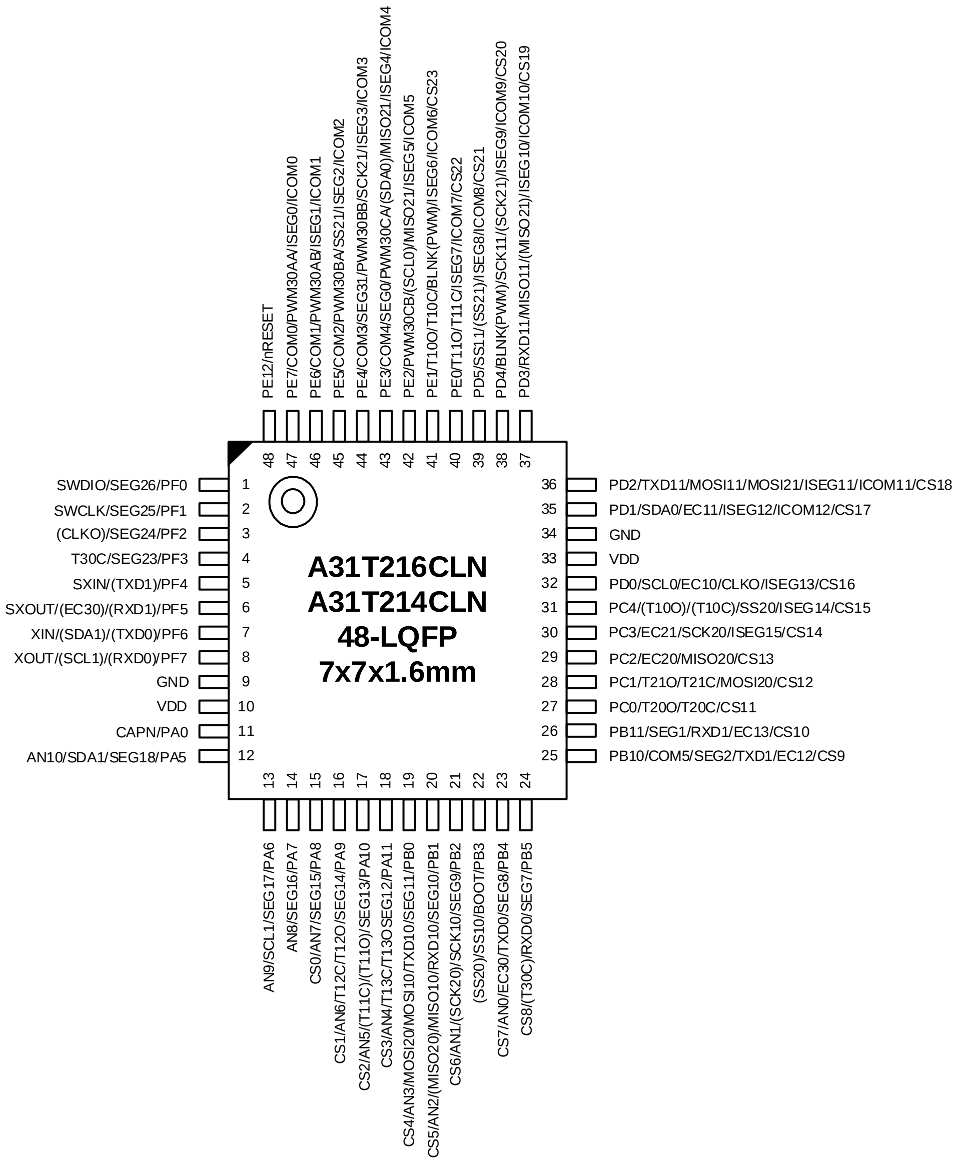

A31T216CLN
A31T214CLN
48-LQFP
7x7x1.6mm
1 SWDIO/SEG26/PF0
2 SWCLK/SEG25/PF1
3 (CLKO)/SEG24/PF2
4 T30C/SEG23/PF3
5 SXIN/(TXD1)/PF4
6 SXOUT/(EC30)/(RXD1)/PF5
7 XIN/(SDA1)/(TXD0)/PF6
8 XOUT/(SCL1)/(RXD0)/PF7
9 GND
10 VDD
11 CAPN/PA0
12 AN10/SDA1/SEG18/PA5
13 AN9/SCL1/SEG17/PA6
14 AN8/SEG16/PA7
15 CS0/AN7/SEG15/PA8
16 CS1/AN6/T12C/T12O/SEG14/PA9
17 CS2/AN5/(T11C)/(T11O)/SEG13/PA10
18 CS3/AN4/T13C/T13O SEG12/PA11
19 CS4/AN3/MOSI20/MOSI10/TXD10/SEG11/PB0
20 CS5/AN2/(MISO20)/MISO10/RXD10/SEG10/PB1
21 CS6/AN1/(SCK20)/SCK10/SEG9/PB2
22 (SS20)/SS10/BOOT/PB3
23 CS7/AN0/EC30/TXD0/SEG8/PB4
24 CS8/(T30C)/RXD0/SEG7/PB5
25 PB10/COM5/SEG2/TXD1/EC12/CS9
26 PB11/SEG1/RXD1/EC13/CS10
27 PC0/T20O/T20C/CS11
28 PC1/T21O/T21C/MOSI20/CS12
29 PC2/EC20/MISO20/CS13
30 PC3/EC21/SCK20/ISEG15/CS14
31 PC4/(T10O)/(T10C)/SS20/ISEG14/CS15
32 PD0/SCL0/EC10/CLKO/ISEG13/CS16
33 VDD
34 GND
35 PD1/SDA0/EC11/ISEG12/ICOM12/CS17
36 PD2/TXD11/MOSI11/MOSI21/ISEG11/ICOM11/CS18
37 PD3/RXD11/MISO11/(MISO21)/ISEG10/ICOM10/CS19
38 PD4/BLNK(PWM)/SCK11/(SCK21)/ISEG9/ICOM9/CS20
39 PD5/SS11/(SS21)/ISEG8/ICOM8/CS21
40 PE0/T11O/T11C/ISEG7/ICOM7/CS22
41 PE1/T10O/T10C/BLNK(PWM)/ISEG6/ICOM6/CS23
42 PE2/PWM30CB/(SCL0)/MISO21/ISEG5/ICOM5
43 PE3/COM4/SEG0/PWM30CA/(SDA0)/MISO21/ISEG4/ICOM4
44 PE4/COM3/SEG31/PWM30BB/SCK21/ISEG3/ICOM3
45 PE5/COM2/PWM30BA/SS21/ISEG2/ICOM2
46 PE6/COM1/PWM30AB/ISEG1/ICOM1
47 PE7/COM0/PWM30AA/ISEG0/ICOM0
48 PE12/nRESET

Figure 4. LQFP 48 Pinouts

2.1.3 A31T21xSNN (44 LQFP)

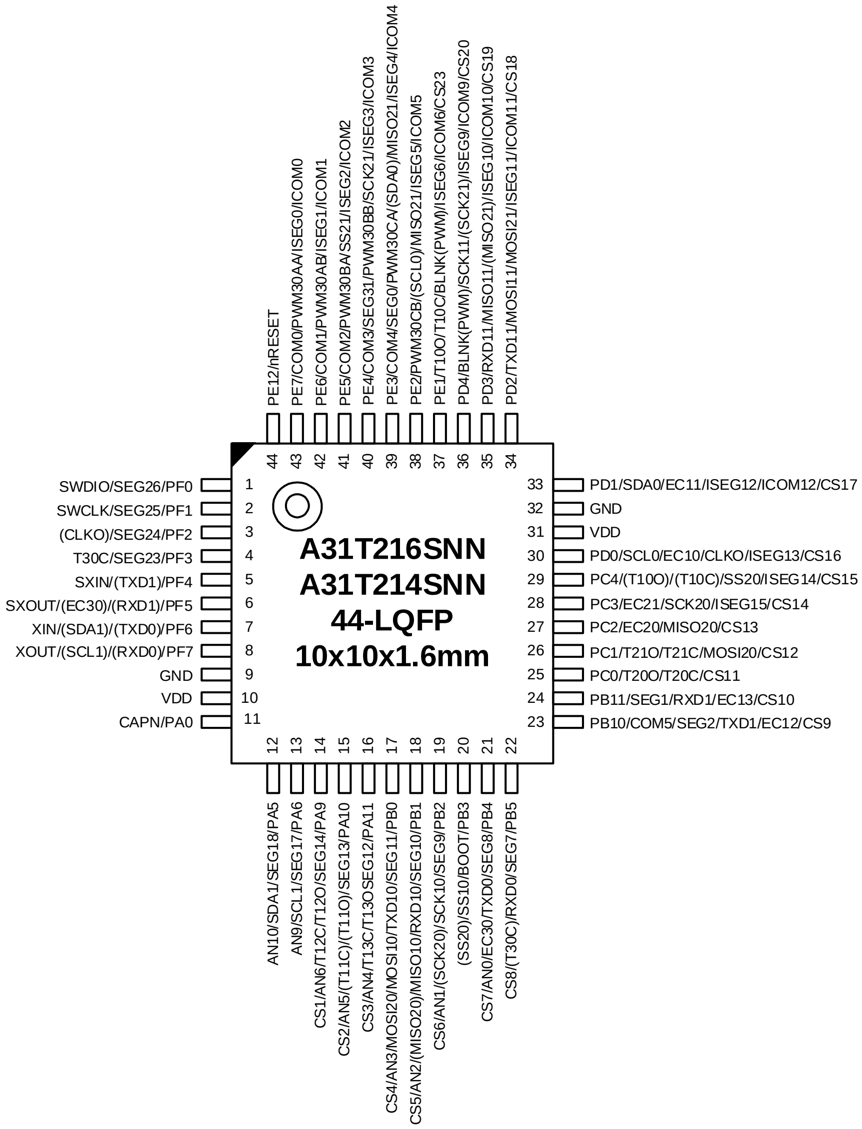

PE12/nRESET
PE7/COM0/PWM30AA/ISEG0/ICOM0
PE6/COM1/PWM30AB/ISEG1/ICOM1
PE5/COM2/PWM30BA/SS21/ISEG2/ICOM2
PE4/COM3/SEG31/PWM30BB/SCK21/ISEG3/ICOM3
PE3/COM4/SEG0/PWM30CA/(SDA0)/MISO21/ISEG4/ICOM4
PE2/PWM30CB/(SCL0)/MISO21/ISEG5/ICOM5
PE1/T10O/T10C/BLNK(PWM)/ISEG6/ICOM6/CS23
PD4/BLNK(PWM)/SCK11/(SCK21)/ISEG9/ICOM9/CS20
PD3/RXD11/MISO11/(MISO21)/ISEG10/ICOM10/CS19
PD2/TXD11/MOSI11/MOSI21/ISEG11/ICOM11/CS18
44
43
42
41
40
39
38
37
36
35
34
SWDIO/SEG26/PF0
1
SWCLK/SEG25/PF1
2
(CLKO)/SEG24/PF2
3
T30C/SEG23/PF3
4
SXIN/(TXD1)/PF4
5
SXOUT/(EC30)/(RXD1)/PF5
6
XIN/(SDA1)/(TXD0)/PF6
7
XOUT/(SCL1)/(RXD0)/PF7
8
GND
9
VDD
10
CAPN/PA0
11
A31T216SNN
A31T214SNN
44-LQFP
10x10x1.6mm
33
PD1/SDA0/EC11/ISEG12/ICOM12/CS17
32
GND
31
VDD
30
PD0/SCL0/EC10/CLKO/ISEG13/CS16
29
PC4/(T10O)/(T10C)/SS20/ISEG14/CS15
28
PC3/EC21/SCK20/ISEG15/CS14
27
PC2/EC20/MISO20/CS13
26
PC1/T21O/T21C/MOSI20/CS12
25
PC0/T20O/T20C/CS11
24
PB11/SEG1/RXD1/EC13/CS10
23
PB10/COM5/SEG2/TXD1/EC12/CS9
12
13
14
15
16
17
18
19
20
21
22
AN10/SDA1/SEG18/PA5
AN9/SCL1/SEG17/PA6
CS1/AN6/T12C/T12O/SEG14/PA9
CS2/AN5/(T11C)/(T11O)/SEG13/PA10
CS3/AN4/T13C/T13OSEG12/PA11
CS4/AN3/MOSI20/MOSI10/TXD10/SEG11/PB0
CS5/AN2/(MISO20)/MISO10/RXD10/SEG10/PB1
CS6/AN1/(SCK20)/SCK10/SEG9/PB2
(SS20)/SS10/BOOT/PB3
CS7/AN0/EC30/TXD0/SEG8/PB4
CS8/(T30C)/RXD0/SEG7/PB5

Figure 5. LQFP 44 Pinouts

2.1.4 A31T21xIUN (40 QFN)

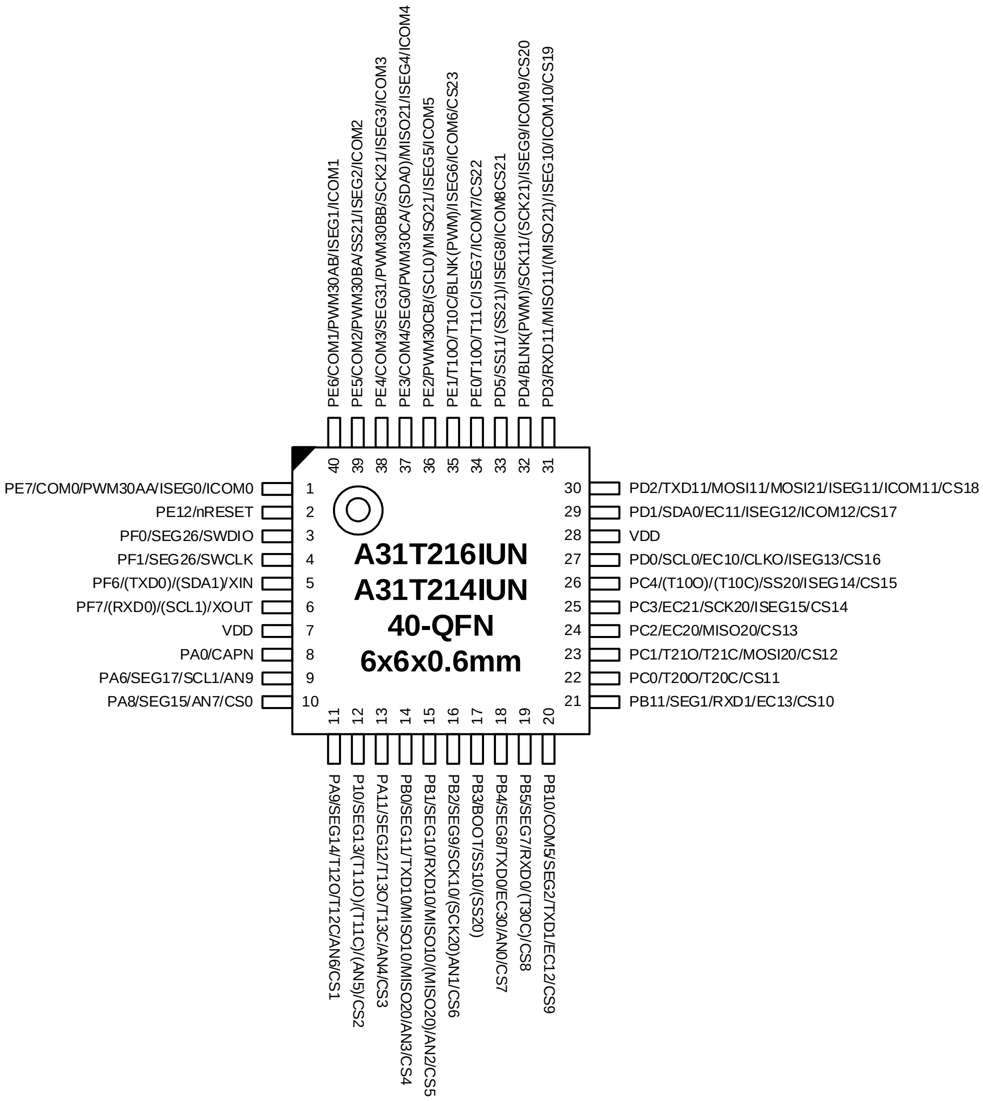

PE6/COM1/PWM30AB/ISEG1/ICOM1
PE5/COM2/PWM30BA/SS21/ISEG2/ICOM2
PE4/COM3/SEG31/PWM30BB/SCK21/ISEG3/ICOM3
PE3/COM4/SEG0/PWM30CA/(SDA0)/MISO21/ISEG4/ICOM4
PE2/PWM30CB/(SCL0)/MISO21/ISEG5/ICOM5
PE1/T10O/T10C/BLNK(PWM)/ISEG6/ICOM6/CS23
PE0/T10O/T11C/ISEG7/ICOM7/CS22
PD5/SS11/(SS21)/ISEG8/ICOM8CS21
PD4/BLNK(PWM)/SCK11/(SCK21)/ISEG9/ICOM9/CS20
PD3/RXD11/MISO11/(MISO21)/ISEG10/ICOM10/CS19
40
39
38
37
36
35
34
33
32
31
PE7/COM0/PWM30AA/ISEG0/ICOM0
PE12/nRESET
PF0/SEG26/SWDIO
PF1/SEG26/SWCLK
PF6/(TXD0)/(SDA1)/XIN
PF7/(RXD0)/(SCL1)/XOUT
VDD
PA0/CAPN
PA6/SEG17/SCL1/AN9
PA8/SEG15/AN7/CS0
1
2
3
4
5
6
7
8
9
10
A31T216IUN
A31T214IUN
40-QFN
6x6x0.6mm
30
29
28
27
26
25
24
23
22
21
PD2/TXD11/MOSI11/MOSI21/ISEG11/ICOM11/CS18
PD1/SDA0/EC11/ISEG12/ICOM12/CS17
VDD
PD0/SCL0/EC10/CLKO/ISEG13/CS16
PC4/(T10O)/(T10C)/SS20/ISEG14/CS15
PC3/EC21/SCK20/ISEG15/CS14
PC2/EC20/MISO20/CS13
PC1/T21O/T21C/MOSI20/CS12
PC0/T20O/T20C/CS11
PB11/SEG1/RXD1/EC13/CS10
11
12
13
14
15
16
17
18
19
20
PA9/SEG14/T12O/T12C/AN6/CS1
P10/SEG13/(T11O)/(T11C)/(AN5)/CS2
PA11/SEG12/T13O/T13C/AN4/CS3
PB0/SEG11/TXD10/MISO10/MISO20/AN3/CS4
PB1/SEG10/RXD10/MISO10/(MISO20)/AN2/CS5
PB2/SEG9/SCK10/(SCK20)AN1/CS6
PB3/BOOT/SS10/(SS20)
PB4/SEG8/TXD0/EC30/AN0/CS7
PB5/SEG7/RXD0/(T30C)/CS8
PB10/COM5/SEG2/TXD1/EC12/CS9

Figure 6. QFN 40 Pinouts

2.2 Pin description

Pin configuration information in Table 2 contains two pairs of power/ground and other dedicated pins. These multi-function pins have up to ten selections of functions including GPIO. Configuration including pin ordering can be changed without notice.

Table 2. Pin Description

Pin no.				Pin name	Type	Description	Remark
64-pin	48-pin	44-pin	40-pin				
1	1	1	3	PF0	IOUDS	PORT F Bit 0 Input/Output	
				SEG26	O	LCD Segment Signal 26 Output	
				SWDIO*	I/O	SWD Data Input/Output	Pull-Up
2	2	2	4	PF1	IOUDS	PORT F Bit 1 Input/Output	
				SEG25	O	LCD Segment Signal 25 Output	
				SWCLK*	I	SWD Clock Input	Pull-Up
3	3	3	-	PF2*	IOUDS	PORT F Bit 2 Input/Output	
				SEG24	O	LCD Segment Signal 24 Output	
				(CLKO)	O	System Clock Output	
4	4	4	-	PF3*	IOUDS	PORT F Bit 3 Input/Output	
				SEG23	O	LCD Segment Signal 23 Output	
				T30C	I	Timer 30 Clock/Capture Input	
5	5	5	-	PF4*	IOUDS	PORT F Bit 4 Input/Output	
				(TXD1)	O	UART Channel 1 TXD Output	
				SXIN	I	Sub Oscillator Input	
6	6	6	-	PF5*	IOUDS	PORT F Bit 5 Input/Output	
				(RXD1)	I	UART Channel 1 RXD Input	
				(EC30)	I	Timer 30 Event Count Input	
				SXOUT	O	Sub Oscillator Output	
7	7	7	5	PF6*	IOUDS	PORT F Bit 6 Input/Output	
				(TXD0)	O	UART Channel 0 TXD Output	
				(SDA1)	I/O	I2C Channel 1 SDA In/Out	
				XIN	I	Main Oscillator Input	
8	8	8	6	PF7*	IOUDS	PORT F Bit 7 Input/Output	
				(RXD0)	I	UART Channel 0 RXD Input	
				(SCL1)	I/O	I2C Channel 1 SCL In/Out	
				XOUT	O	Main Oscillator Output	
9	9	9	-	GND	P	GND	
10	10	10	7	VDDEXT	P	VDD	
11	11	11	8	PA0*	IOUDS	PORT A Bit 0 Input/Output	
				CAPN	I/O	Modulation Cap	
12	-	-	-	PA1*	IOUDS	PORT A Bit 1 Input/Output	
				SEG22	O	LCD Segment Signal 22 Output	
				AN14/ AVREF	IA	Analog Input 14 A/D Converter Reference Input	

Table 2. Pin Description (continued)

Pin no.				Pin name	Type	Description	Remark
64-pin	48-pin	44-pin	40-pin				
13	-	-	-	PA2*	IOUDS	PORT A Bit 2 Input/Output	
				SEG21	O	LCD Segment Signal 21 Output	
				AN13	IA	Analog Input 13	
14	-	-	-	PA3*	IOUDS	PORT A Bit 3 Input/Output	
				SEG20	O	LCD Segment Signal 20 Output	
				AN12	IA	Analog Input 12	
15	-	-	-	PA4*	IOUDS	PORT A Bit 4 Input/Output	
				SEG19	O	LCD Segment Signal 19 Output	
				AN11	IA	Analog Input 11	
16	12	12	-	PA5*	IOUDS	PORT A Bit 5 Input/Output	
				SEG18	O	LCD Segment Signal 18 Output	
				SDA1	I/O	I2C Channel 1 SDA In/Out	
				AN10	IA	Analog Input 10	
17	13	13	9	PA6*	IOUDS	PORT A Bit 6 Input/Output	
				SEG17	O	LCD Segment Signal 17 Output	
				SCL1	I/O	I2C Channel 1 SCL In/Out	
				AN9	IA	Analog Input 9	
18	14	-	-	PA7*	IOUDS	PORT A Bit 7 Input/Output	
				SEG16	O	LCD Segment Signal 16 Output	
				AN8	IA	Analog Input 8	
19	15	-	10	PA8*	IOUDS	PORT A Bit 8 Input/Output	
				SEG15	O	LCD Segment Signal 15 Output	
				AN7	IA	Analog Input 7	
				CS0	IA	Capacitive Touch Switch Input 0	
20	16	14	11	PA9*	IOUDS	PORT A Bit 9 Input/Output	
				SEG14	O	LCD Segment Signal 14 Output	
				T12O	O	Timer 12 Output	
				T12C	I	Timer 12 Capture Input	
				AN6	IA	Analog Input 6	
				CS1	IA	Capacitive Touch Switch Input 1	
21	17	15	12	PA10*	IOUDS	PORT A Bit 10 Input/Output	
				SEG13	O	LCD Segment Signal 13 Output	
				(T11O)	O	Timer 11 Output	
				(T11C)	I	Timer 11 Capture Input	
				AN5	IA	Analog Input 5	
				CS2	IA	Capacitive Touch Switch Input 2	
22	18	16	13	PA11*	IOUDS	PORT A Bit 11 Input/Output	
				SEG12	O	LCD Segment Signal 12 Output	
				T13O	O	Timer 13 Output	
				T13C	I	Timer 13 Capture Input	
				AN4	IA	Analog Input 4	
				CS3	IA	Capacitive Touch Switch Input 3	
23	19	17	14	PB0*	IOUDS	PORT B Bit 0 Input/Output	
				SEG11	O	LCD Segment Signal 11 Output	

Table 2. Pin Description (continued)

Pin no.				Pin name	Type	Description	Remark
64-pin	48-pin	44-pin	40-pin				
				TXD10	O	UART Channel 10 TXD Output	
				MOSI10	I/O	SPI Channel 10 Master Out/Slave In	
				(MOSI20)	I/O	SPI Channel 20 Master Out/Slave In	
				AN3	IA	Analog Input 3	
				CS4	IA	Capacitive Touch Switch Input 4	
24	20	18	15	PB1*	IOUDS	PORT B Bit 1 Input/Output	Input
				SEG10	O	LCD Segment Signal 10 Output	
				RXD10	I	UART Channel 10 RXD Input	
				MISO10	I/O	SPI Channel 10 Master In/Slave Out	
				(MISO20)	I/O	SPI Channel 20 Master In/Slave Out	
				AN2	IA	Analog Input 9	
				CS5	IA	Capacitive Touch Switch Input 5	
25	21	19	16	PB2*	IOUDS	PORT B Bit 2 Input/Output	
				SEG9	O	LCD Segment Signal 9 Output	
				SCK10	I/O	SPI10 Data Clock Input/Output	
				(SCK20)	I/O	SPI20 Data Clock Input/Output	
				AN1	IA	Analog Input 1	
				CS6	IA	Capacitive Touch Switch Input 6	
26	22	20	17	PB3	IOUDS	PORT B Bit 3 Input/Output	
				BOOT*	I	Boot mode selection Input	Pull-Up
				SS10	I/O	SPI Channel 10 Slave Select signal	
				(SS20)	I/O	SPI Channel 20 Slave Select signal	
27	23	21	18	PB4*	IOUDS	PORT B Bit 4 Input/Output	
				SEG8	O	LCD Segment Signal 8 Output	
				TXD0	O	UART Channel 0 TXD Output	
				EC30	I	Timer 30 Event Count Input	
				AN0	IA	Analog Input 0	
				CS7	IA	Capacitive Touch Switch Input 7	
28	24	22	19	PB5*	IOUDS	PORT B Bit 5 Input/Output	
				SEG7	O	LCD Segment Signal 7 Output	
				RXD0	I	UART Channel 0 RXD Input	
				(T30C)	I	Timer 30 Capture Input	
				CS8	IA	Capacitive Touch Switch Input 8	
29	-	-	-	PB6*	IOUDS	PORT B Bit 6 Input/Output	
				SEG6	O	LCD Segment Signal 6 Output	
30	-	-	-	PB7*	IOUDS	PORT B Bit 7 Input/Output	
				SEG5	O	LCD Segment Signal 5 Output	
31	-	-	-	PB8*	IOUDS	PORT B Bit 8 Input/Output	
				COM7/ SEG4	O	LCD Common Signal 7 Output LCD Segment Signal 4 Output	
32	-	-	-	PB9*	IOUDS	PORT B Bit 9 Input/Output	
				COM6/ SEG3	O	LCD Common Signal 6 Output LCD Segment Signal 3 Output	
33	25	23	20	PB10*	IOUDS	PORT B Bit 10 Input/Output	
				COM5/	O	LCD Common Signal 5 Output	

Table 2. Pin Description (continued)

Pin no.				Pin name	Type	Description	Remark
64-pin	48-pin	44-pin	40-pin				
				SEG2		LCD Segment Signal 2 Output	
				TXD1	O	UART Channel 1 TXD Output	
				EC12	I	Timer 12 Event Count Input	
				CS9	IA	Capacitive Touch Switch Input 9	
34	26	24	21	PB11*	IOUDS	PORT B Bit 11 Input/Output	
				SEG1	O	LCD Segment Signal 1 Output	
				RXD1	I	UART Channel 1 RXD Input	
				EC13	I	Timer 13 Event Count Input	
				CS10	IA	Capacitive Touch Switch Input 10	
35	27	25	22	PC0*	IOUDS	PORT C Bit 0 Input/Output	
				T20O	O	Timer 20 Output	
				T20C	I	Timer 20 Capture Input	
				CS11	IA	Capacitive Touch Switch Input 11	
36	28	26	23	PC1*	IOUDS	PORT C Bit 1 Input/Output	
				T21O	O	Timer 21 Output	
				T21C	I	Timer 21 Capture Input	
				MOSI20	I/O	SPI Channel 20 Master Out/Slave In	
				CS12	IA	Capacitive Touch Switch Input 12	
37	29	27	24	PC2*	IOUDS	PORT C Bit 2 Input/Output	
				EC20	I	Timer 20 Event Count Input	
				MISO20	I/O	SPI Channel 20 Master In/Slave Out	
				CS13	IA	Capacitive Touch Switch Input 13	
38	30	28	25	PC3*	IOUDS	PORT C Bit 3 Input/Output	
				EC21	I	Timer 21 Event Count Input	
				SCK20	I/O	SPI20 Data Clock Input/Output	
				ISEG15/ CS14	O IA	LED Segment Signal 15 Output Capacitive Touch Switch Input 14	
39	31	29	26	PC4*	IOUDS	PORT C Bit 4 Input/Output	
				(T10O)	O	Timer 10 Output	
				(T10C)	I	Timer 10 Capture Input	
				SS20	I/O	SPI Channel 20 Slave Select signal	
				ISEG14/ CS15	O IA	LED Segment Signal 14 Output Capacitive Touch Switch Input 15	
40	-	-	-	PC5*	IOUDS	PORT C Bit 5 Input/Output	
41	-	-	-	PC6*	IOUDS	PORT C Bit 6 Input/Output	
42	-	-	-	PC7*	IOUDS	PORT C Bit 7 Input/Output	
43	-	-	-	PC8*	IOUDS	PORT C Bit 8 Input/Output	
44	32	30	27	PD0*	IOUDS	PORT D Bit 0 Input/Output	Input Pull-Up
				SCL0	I/O	I2C Channel 0 SCL In/Out	
				EC10	I	Timer 10 Event Count Input	
				CLKO	O	System Clock Output	
				ISEG13/ CS16	O IA	LED Segment Signal 13 Output Capacitive Touch Switch Input 16	
45	33	31	28	VDDEXT	P	VDD	

Table 2. Pin Description (continued)

Pin no.				Pin name	Type	Description	Remark
64-pin	48-pin	44-pin	40-pin				
46	34	32	-	GND	P	GND	
47	35	33	29	PD1*	IOUDS	PORT D Bit 1 Input/Output	Input Pull-Up
				SDA0	I/O	I2C Channel 0 SDA In/Out	
				EC11	I	Timer 11 Event Count Input	
				ISEG12/ ICOM12/ CS17	O O IA	LED Segment Signal 12 Output LED Common Signal 12 Output Capacitive Touch Switch Input 17	
48	36	34	30	PD2*	IOUDS	PORT D Bit 2 Input/Output	
				TXD11	O	UART Channel 11 TXD Output	
				MOSI11	I/O	SPI Channel 11 Master Out/Slave In	
				(MOSI21)	I/O	SPI Channel 21 Master Out/Slave In	
				ISEG11/ ICOM11/ CS18	O O IA	LED Segment Signal 11 Output LED Common Signal 11 Output Capacitive Touch Switch Input 18	
49	37	35	31	PD3*	IOUDS	PORT D Bit 3 Input/Output	
				RXD11	I	UART Channel 11 RXD Input	
				MISO11	I/O	SPI Channel 11 Master In/Slave Out	
				(MISO21)	I/O	SPI Channel 21 Master In/Slave Out	
				ISEG10/ ICOM10/ CS19	O O IA	LED Segment Signal 10 Output LED Common Signal 10 Output Capacitive Touch Switch Input 19	
50	38	36	32	PD4*	IOUDS	PORT D Bit 4 Input/Output	
				BLNK(PWM)	I	External Sync Signal Input for T30 PWM	
				SCK11	I/O	SPI11 Data Clock Input/Output	
				(SCK21)	I/O	SPI21 Data Clock Input/Output	
				ISEG9/ ICOM9/ CS20	O O IA	LED Segment Signal 9 Output LED Common Signal 9 Output Capacitive Touch Switch Input 20	
51	39	-	33	PD5*	IOUDS	PORT D Bit 5 Input/Output	
				SS11	I/O	SPI Channel 11 Slave Select signal	
				(SS21)	I/O	SPI Channel 21 Slave Select signal	
				ISEG8/ ICOM8/ CS21	O O IA	LED Segment Signal 8 Output LED Common Signal 8 Output Capacitive Touch Switch Input 21	
52	40	-	34	PE0*	IOUDS	PORT E Bit 0 Input/Output	
				T11O	O	Timer 11 Output	
				T11C	I	Timer 11 Clock/Capture Input	
				ISEG7/ ICOM7/ CS22	O O IA	LED Segment Signal 7 Output LED Common Signal 7 Output Capacitive Touch Switch Input 22	
53	41	37	35	PE1*	IOUDS	PORT E Bit 1 Input/Output	
				T10O	O	Timer 10 Output	
				T10C	I	Timer 10 Capture Input	

Table 2. Pin Description (continued)

Pin no.				Pin name	Type	Description	Remark
64-pin	48-pin	44-pin	40-pin				
				BLNK(PWM)	I	External Sync Signal Input for T30 PWM	
				ISEG6/ ICOM6/ CS23	O O IA	LED Segment Signal 6 Output LED Common Signal 6 Output Capacitive Touch Switch Input 23	
54	42	38	36	PE2*	IOUDS	PORT E Bit 2 Input/Output	
				PWM30CB	O	Timer 30 PWM Output	
				(SCL0)	I/O	I2C Channel 0 SCL In/Out	
				MOSI21	I/O	SPI Channel 21 Master Out/Slave In	
				ISEG5/ ICOM5	O	LED Segment Signal 5 Output LED Common Signal 5 Output	
55	43	39	37	PE3*	IOUDS	PORT E Bit 3 Input/Output	
				COM4/ SEG0	O	LCD Common Signal 4 Output LCD Segment Signal 0 Output	
				PWM30CA	O	Timer 30 PWM Output	
				(SDA0)	I/O	I2C Channel 0 SDA In/Out	
				MISO21	I/O	SPI Channel 21 Master In/Slave Out	
				ISEG4/ ICOM4	O	LED Segment Signal 4 Output LED Common Signal 4 Output	
56	44	40	38	PE4*	IOUDS	PORT E Bit 4 Input/Output	
				COM3/ SEG31	O	LCD Common Signal 3 Output LCD Segment Signal 31 Output	
				PWM30BB	O	Timer 30 PWM Output	
				SCK21	I/O	SPI21 Data Clock Input/Output	
				ISEG3/ ICOM3	O	LED Segment Signal 3 Output LED Common Signal 3 Output	
57	45	41	39	PE5*	IOUDS	PORT E Bit 5 Input/Output	
				COM2	O	LCD Common Signal 2 Output	
				PWM30BA	O	Timer 30 PWM Output	
				SS21	I/O	SPI Channel 21 Slave Select signal	
				ISEG2/ ICOM2	O	LED Segment Signal 2 Output LED Common Signal 2 Output	
58	46	42	40	PE6*	IOUDS	PORT E Bit 6 Input/Output	
				COM1	O	LCD Common Signal 1 Output	
				PWM30AB	O	Timer 30 PWM Output	
				ISEG1/ ICOM1	O	LED Segment Signal 1 Output LED Common Signal 1 Output	
59	47	43	1	PE7*	IOUDS	PORT E Bit 7 Input/Output	
				COM0	O	LCD Common Signal 0 Output	
				PWM30AA	O	Timer 30 PWM Output	
				ISEG0/ ICOM0	O	LED Segment Signal 0 Output LED Common Signal 0 Output	
60	-	-	-	PE8*	IOUDS	PORT E Bit 8 Input/Output	
				SEG30	O	LCD Segment Signal 30 Output	
				VLC3	IA	External LCD Voltage bias 3	

Table 2. Pin Description (continued)

Pin no.				Pin name	Type	Description	Remark
64-pin	48-pin	44-pin	40-pin				
61	-	-	-	PE9*	IOUDS	PORT E Bit 9 Input/Output	
				SEG29	O	LCD Segment Signal 29 Output	
				VLC2	IA	External LCD Voltage bias 2	
62	-	-	-	PE10*	IOUDS	PORT E Bit 10 Input/Output	
				SEG28	O	LCD Segment Signal 28 Output	
				VLC1	IA	External LCD Voltage bias 1	
63	-	-	-	PE11*	IOUDS	PORT E Bit 11 Input/Output	
				SEG27	O	LCD Segment Signal 27 Output	
				VLC0	IA	External LCD Voltage bias 0	
64	48	44	2	PE12	IOUDS	PORT E Bit 12 Input/Output	
				nRESET*	IU	External Reset Input	Pull-Up

NOTES:

1. I=Input, O=Output, U=Pull-up, D=Pull-down, S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
2. The * means 'selected pin function after reset condition'.
3. Pin order may be changed with revision notice.

3 System and memory overview

3.1 System architecture

Main system of A31T214/216 series consists of the followings:

- ARM® Cortex® -M0+ core
- General purpose DMA
- Internal SRAM
- Internal Flash memory

3.1.1 Cortex-M0+ core

The ARM® Cortex®-M0+ processor is the most energy-efficient ARM processor available. It builds on the very successful Cortex-M0+ processor, retaining full instruction set and tool compatibility, while further reducing energy consumption and increasing performance. Document “DDI 0484C” from ARM provides detail information of Cortex-M0+.

3.1.2 Interrupt controller

Table 3. Interrupt Vector Map

Priority	Vector address	Interrupt source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Address
-14	0x0000_0008	NMI Handler
-13	0x0000_000C	Hard Fault Handler
-12	0x0000_0010	Reserved
-11	0x0000_0014	
-10	0x0000_0018	
-9	0x0000_001C	
-8	0x0000_0020	
-7	0x0000_0024	
-6	0x0000_0028	
-5	0x0000_002C	SVCall Handler
-4	0x0000_0030	Reserved
-3	0x0000_0034	
-2	0x0000_0038	PenSV Handler
-1	0x0000_003C	SysTick Handler
0	0x0000_0040	LVI
1	0x0000_0044	SYSCLKFAIL
2	0x0000_0048	WDT
3	0x0000_004C	GPIOA, GPIOB
4	0x0000_0050	GPIOC, GPIOD
5	0x0000_0054	GPIOE
6	0x0000_0058	GPIOF
7	0x0000_005C	TIMER10
8	0x0000_0060	TIMER11
9	0x0000_0064	TIMER12
10	0x0000_0068	I2C0
11	0x0000_006C	USART10
12	0x0000_0070	WT
13	0x0000_0074	TIMER30
14	0x0000_0078	I2C1
15	0x0000_007C	TIMER20
16	0x0000_0080	TIMER21

Table 3. Interrupt Vector Map (continued)

Priority	Vector address	Interrupt source
17	0x0000_0084	USART11
18	0x0000_0088	ADC
19	0x0000_008C	UART0
20	0x0000_0090	UART1
21	0x0000_0094	TIMER13
22	0x0000_0098	Reserved
23	0x0000_009C	Reserved
24	0x0000_00A0	Reserved
25	0x0000_00A4	SPI20
26	0x0000_00A8	SPI21
27	0x0000_00AC	Reserved
28	0x0000_00B0	LED
29	0x0000_00B4	TOUCH
30	0x0000_00B8	Reserved
31	0x0000_00BC	CRC

NOTES:

1. Each interrupt has an associated priority-level register. Each of them is 2 bits wide, occupying the two MSBs of the Interrupt Priority Level Registers. Each Interrupt Priority Level Register occupies 1 byte (8 bits).NVIC registers in the Cortex-M0+ processor can only be accessed using word-size transfers, so for each access, four Interrupt Priority Level Registers are accessed at the same time.

   ** __NVIC_PRIO_BITS = 2

2. Figure 7 is a caution when using Peripheral Interrupts. Interrupt don't work if only peripheral interrupts are enabled. Enable the function in core to enable interrupt.

   * __enable_irq > NVIC_EnableIRQ(Peripheral) > Each Peripheral Interrupt

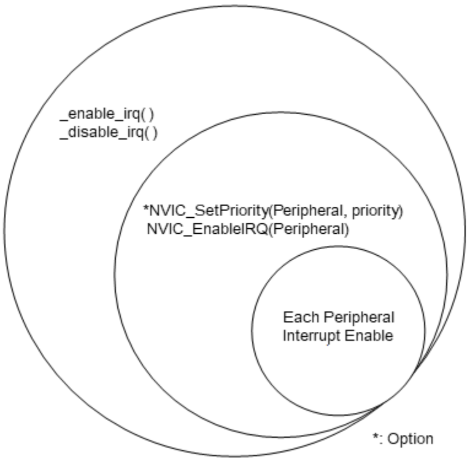


Figure 7. Interrupt Block Diagram

3.2 Memory organization

Program memory, data memory, registers and I/O ports are organized in the same address space.

3.2.1 Register boundary address

Table 4 gives the boundary addresses of peripherals in A31T214/216 series.

Table 4. A31T214/216 Memory Boundary Addresses

Boundary address	Memory area	Register description
0x4000_0000	SCU	
0x4000_5100	LVI/LVR	
0x4000_1000/1100/1200/1300/1400/1500	PCU A/B/C/D/E/F	
0x4000_0100	Flash controller	
0x2000_0000	Internal SRAM	
0x4000_0400/0410/0420/0430	DMACH0/1/2/3	
0x4000_1A00	WDT	
0x4000_2000	WT	
0x4000_2100/2200/2300/2700	Timer 10/11/12/13	
0x4000_2500/2600	Timer 20/21	
0x4000_2400	Timer 30	
0x4000_3800/3900	USART 10/11	
0x4000_4000/4100	UART 0/1	
0x4000_4800/4900	I2C 0/1	
0x4000_4C00/4D00	SPI 20/21	
0x4000_3000	12-bit ADC	
0x4000_3600	TOUCH	
0x4000_5000	LCD	
0x4000_6000	LED	
0x4000_0300	CRC	

3.2.2 Memory map

Figure 8 shows addressable memory space in memory map.

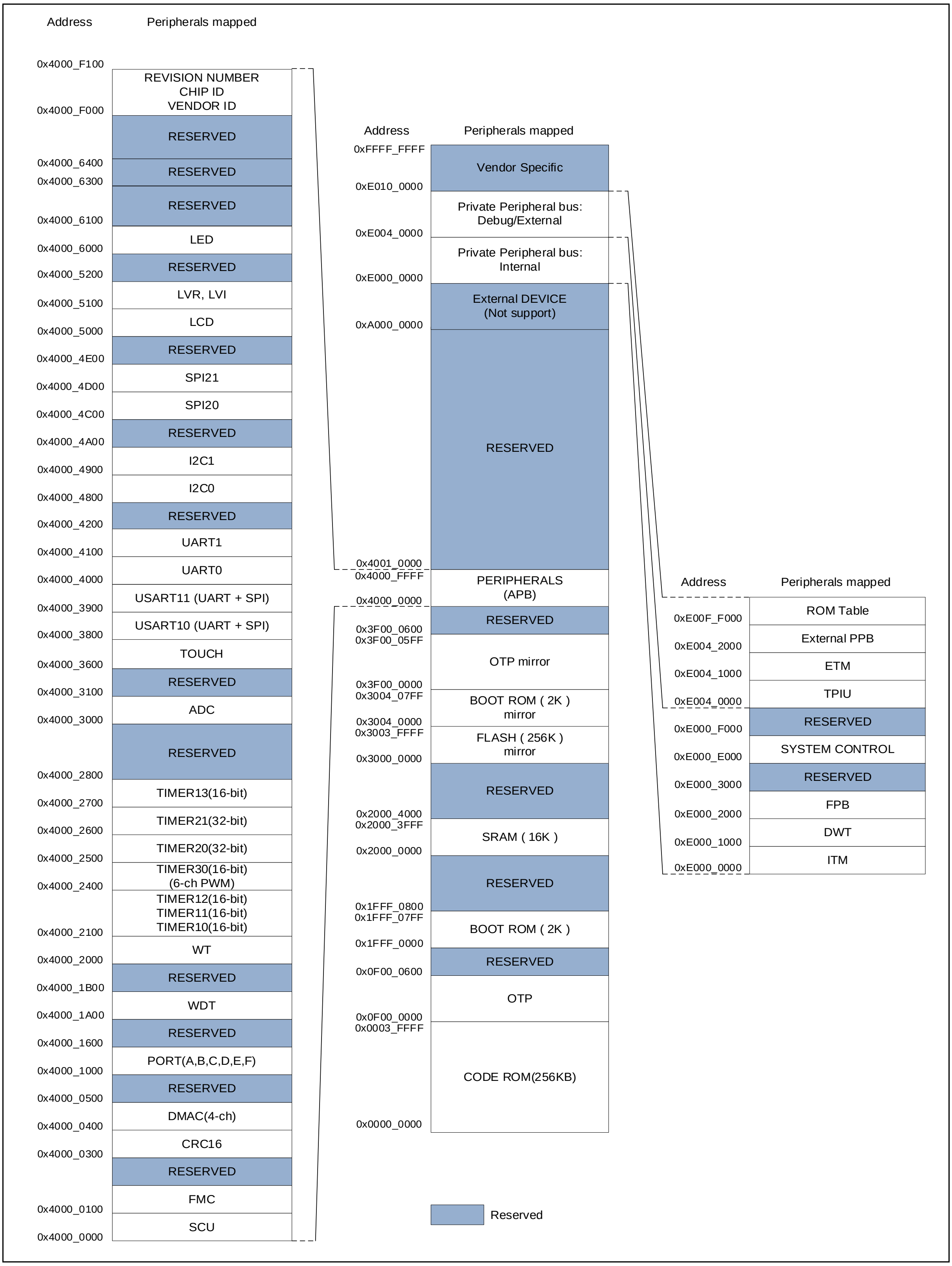


Figure 8. Memory Map (A31T216)

3.2.3 Embedded SRAM

A31T214/216 series has a block of 0-wait on-chip SRAM, and 0x2000_0000 is base address of the 16KB SRAM. SRAM memory area is usually used for data memory and stack memory. Sometimes the code is dumped into the SRAM memory for fast operation or flash erase/programming operation. This device does not support memory remap strategy. So jump and return are required to perform the code in SRAM memory area.

3.2.4 Flash memory overview

A31T214/216 series provides internal 128KB/256KB code flash memory and its controller. This is enough to control the general system. Self-programming is available and ISP and SWD programming is also supported in boot or debugging mode.

Instruction and data cache buffer are present and overcome the low bandwidth flash memory. CPU can access flash memory with one wait state up to 20MHz bus frequency.

3.2.5 Boot mode

Boot mode pins

A31T214/216 series has a boot mode option to program internal flash memory. Boot mode can be entered by setting BOOT pin to 'L' at reset timing (Normal state is 'H').

Boot mode supports UART boot:

- UART boot uses USART10_TXD/USART10_RXD port.

The pins for boot mode are listed in Table 5.

Table 5. Boot Mode Pin List

Block	Pin name	Dir.	Description
SYSTEM	nRESET	I	Reset Input signal
	nBOOT / PB3	I	'Low' to enter Boot mode
UART mode of USART10	USART10_RXD / PB1	I	USART10 Boot Receive Data
	USART10_TXD / PB0	O	USART10 Boot Transmit Data

Boot mode connections

User can design a target board using any of boot mode ports such as UART mode of USART10. Sample connection diagrams of boot mode are introduced in the following figures:

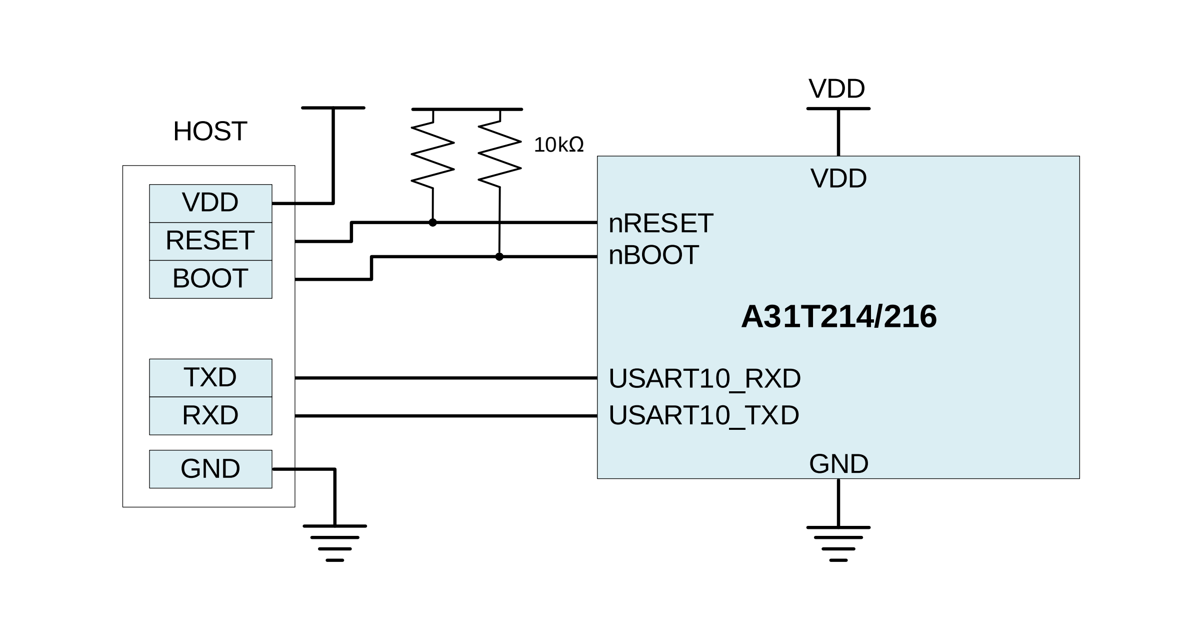


Figure 9. Connection Diagram of UART10 Boot

SWD mode connections

A user can use SWD mode for writing with E-PGM+. This mode can be used for writing & debugging.

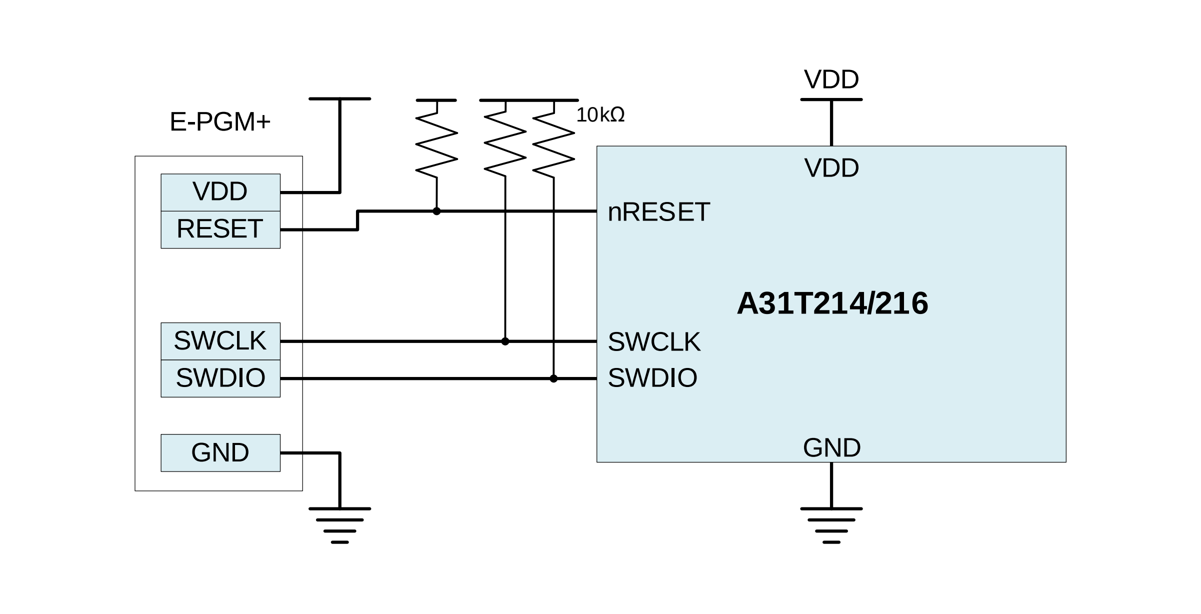


Figure 10. Connection Diagram of E-PGM+ and SWD Port

4 System Control Unit (SCU)

A31T214/216 series has a built-in intelligent power control block which manages system analog blocks and operating modes. System Control Unit (SCU) block controls an internal reset and clock signals to maintain optimize system performance and power dissipation.

Four pins in Table 6 are assigned for the SCU block.

Table 6. SCU Pins

Pin name	Type	Description
nRESET	I	External Reset Input
XIN/XOUT	OSC	External Crystal Oscillator
SXIN/SXOUT	OSC	External sub-Crystal Oscillator
CLKO	O	Clock Output Monitoring Signal

4.1 SCU block diagram

In this section, SCU block diagram is introduced in Figure 11.

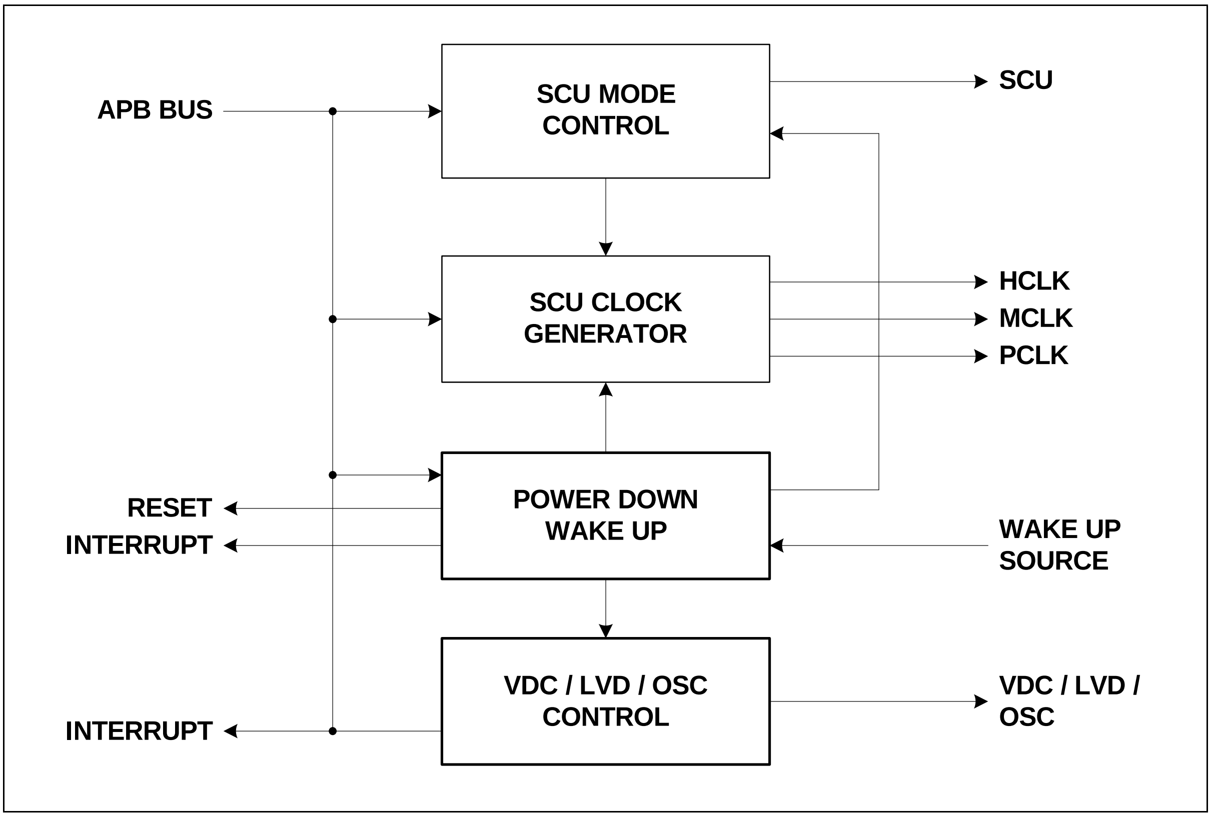


Figure 11. SCU Block Diagram

4.2 Clock system

A31T214/216 series has two main operating clocks. One is HCLK which produces a clock signal both for CPU and AHB bus system. The other is PCLK which produces a clock signal for peripheral systems.

A user can keep the clock system variation under software control. Through Figure 12 and Table 7, users learn about the clock system of A31T214/216 devices and clock sources.

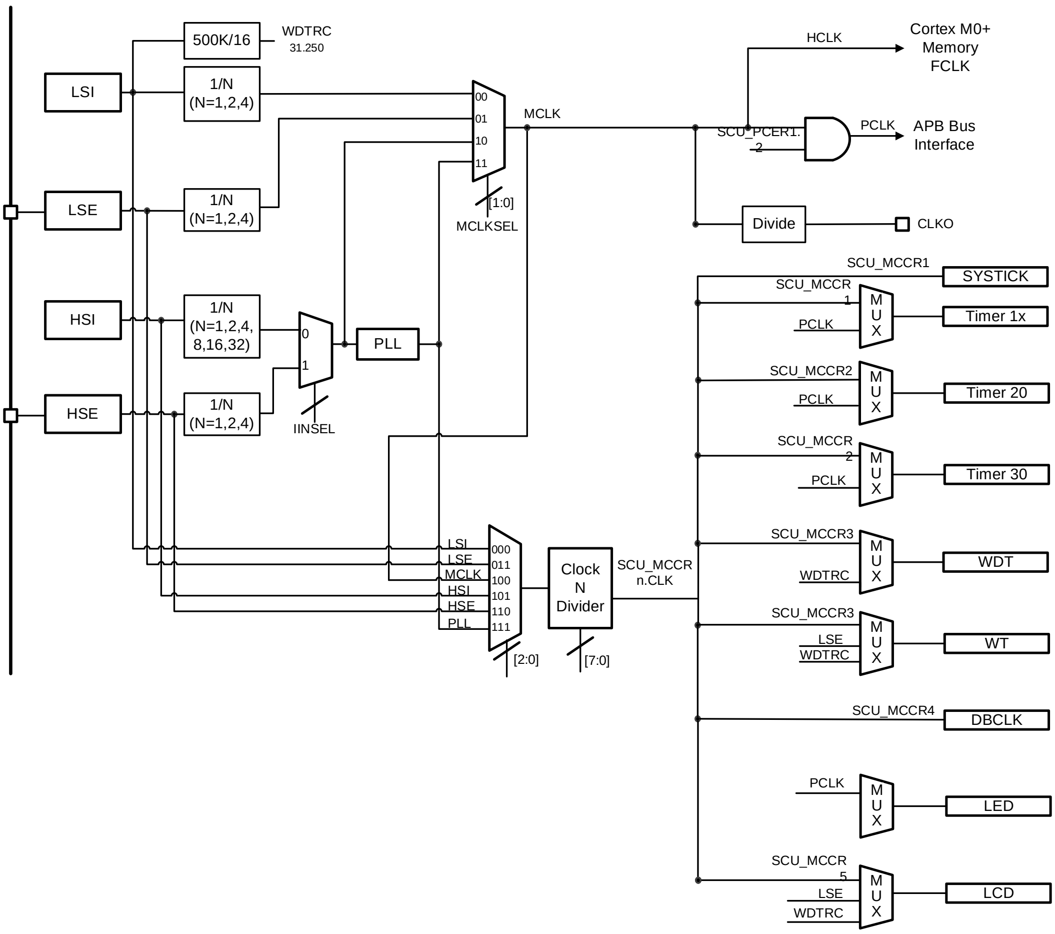


Figure 12. Clock Tree Configuration

All multiplexers switching clock sources have a glitch-free circuit in each. So a clock can be switched without glitch risks. When a user tries to change a clock mux control, both of clock sources must be alive. If one of them is not alive, clock change operation is stopped and system will be halted and not be recovered.

Table 7. Clock Sources

Clock name	Frequency	Description
HSE	2-16MHz	High Speed External Oscillator
LSE	32.768kHz	Low Speed External Oscillator
HSI	32MHz	High Speed Internal OSC
LSI	500kHz	Low Speed Internal OSC

4.2.1 HCLK clock domain

HCLK clock feeds the clock to the CPU and the AHB bus. Cortex-M0+ CPU requires 2 clocks related with FCLK and HCLK. FCLK is free running clock and it is always running except in power down mode. HCLK can be stopped in SLEEP mode and power down mode.

BUS system and memory systems are operated by MCLK clock. Maximum bus operating clock speed is 48MHz.

4.2.2 PCLK clock domain

PCLK is the master clock of all peripherals. Each peripheral clock is enabled by SCU_PCER1, and SCU_PCER2 registers can be used by each peripheral. Before enabling the PCLK input clock of each block, it can’t be accessible even reading its registers. It can be stopped in power down mode.

4.2.3 Clock configuration procedure

After powering up, the default system clock is fed by LSI (500kHz) clock. By default LSI is enabled at power up sequence. The other clock sources will be enabled by user controls with the LSI system clock.

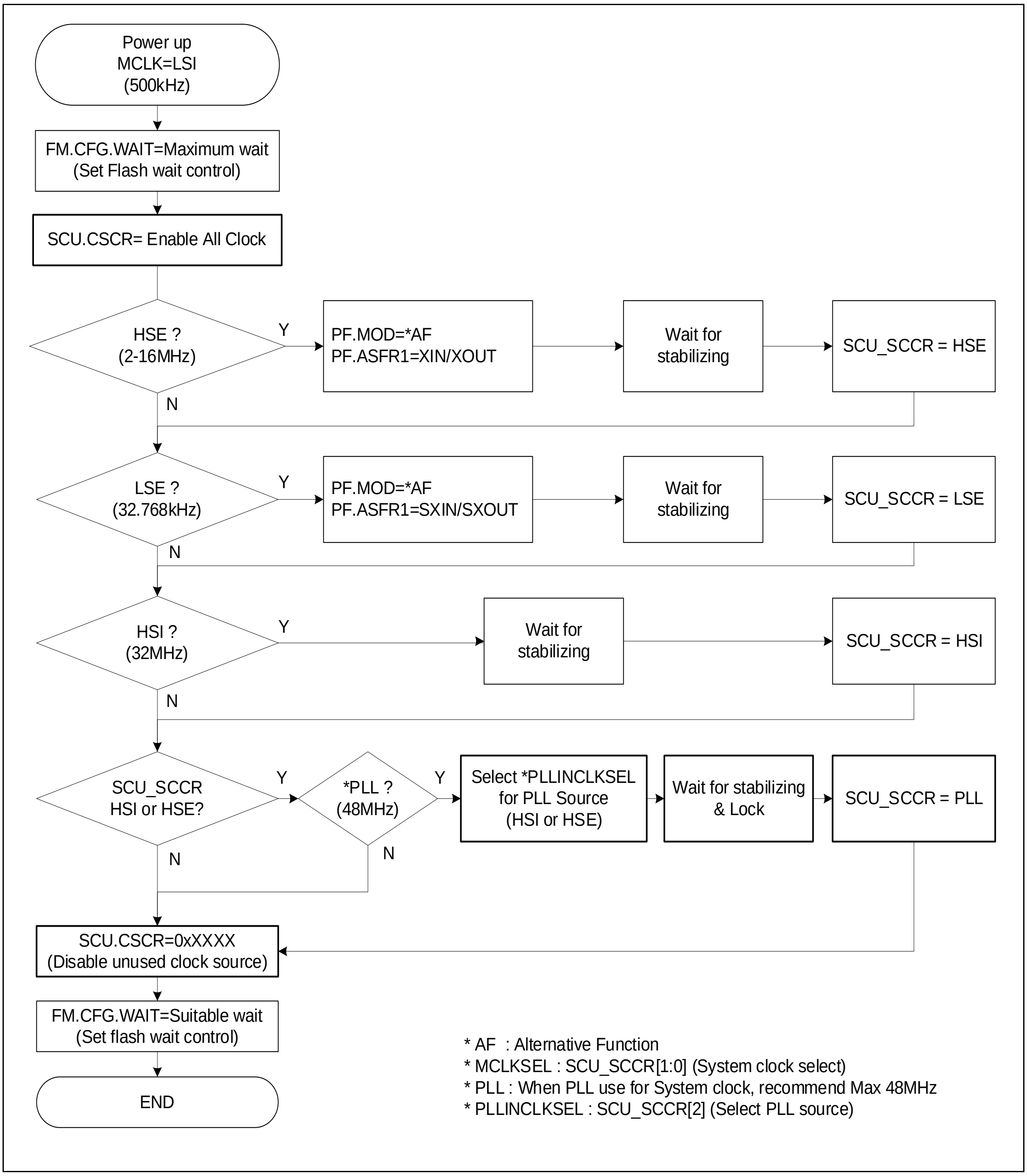
HSI (32MHz) clock can be enabled by SCU_CSCR register.

HSE (2-16MHz) clock can be enabled by SCU_CSCR register. Prior to enable the HSE block, the pin mux configuration should be set for XIN, XOUT function. PF6 and PF7 pins are shared with HSE’s XIN and XOUT function – PF_MOD and PF_AFSR1 registers should be configured properly. After enabling the HSE block, you must wait for more than 5ms time to ensure stable operation of crystal oscillation.

LSE (32.768kHz) clock can be enabled by SCU_CSCR register. Prior to enable the LSE block, the pin mux configuration should be set for SXIN, SXOUT function. PF4 and PF5 pins are shared with LSE's SXIN and SXOUT function – PF_MOD and PF_AFSR1 registers should be configured properly.

After enabling the LSE block, you must wait for more than 10ms time to ensure stable operation of crystal oscillation. You can change an MCLK by using the SCU_SCCR register.

You can find an example flow chart configuring the system clock in Figure 13.



* AF : Alternative Function
* MCLKSEL : SCU_SCCR[1:0] (System clock select)
* PLL : When PLL use for System clock, recommend Max 48MHz
* PLLINCLKSEL : SCU_SCCR[2] (Select PLL source)

Figure 13. Clock Change Procedure

When you speed up the system clock to the maximum operating frequency, you should check flash wait control configuration. Flash read access time is one of limitation factor for performance. The wait control recommendation is suggested in Table 8.

Table 8. Flash Wait Control Recommendation

FM.CFG.WAIT	FLASH Access Wait	Available Max System clock frequency
000	0 clock wait	Up to 20MHz
001	1 clock wait	Up to 40MHz
010	2 clock wait	Up to 48MHz
011	3 clock wait	Up to 48MHz
100	4 clock wait	Up to 48MHz
11x	5 clock wait	Up to 48MHz

4.3 Reset

A31T214/216 series has two system reset options. One is cold reset that is effective during power up or down sequence. The other is warm reset which is generated by several reset sources. A reset event makes a chip to turn to an initial state. Reset sources of the cold reset and the warm reset are listed in Table 9.

Table 9. Reset Sources of Cold Reset and Warm Reset

	Cold reset	Warm reset
Reset sources	• POR	• nRESET Pin • WDT reset • LVD reset • MCLK Fail reset • HSE Fail reset • S/W reset • CPU request reset

4.3.1 Cold reset

Cold reset is an important feature of a chip when power is up. This characteristic will affect overall system boot. Internal VDC is enabled when VDD power is turn on. Internal POR trigger level is 1.4V of VDD voltage out level, and boot operation is started at this point. The LSI clock is enabled and counts 4.25msec time for internal VDC level stabilizing. In this time, VDD voltage level should be over than initial LVR level (1.6V). After 4.25msec counting, the cold reset is released and counts 0.4msec time for warm reset synchronizing. After releasing both cold and warm reset, BOOTROM and CPU are running. Figure 14 shows power up sequence and internal reset waveforms.

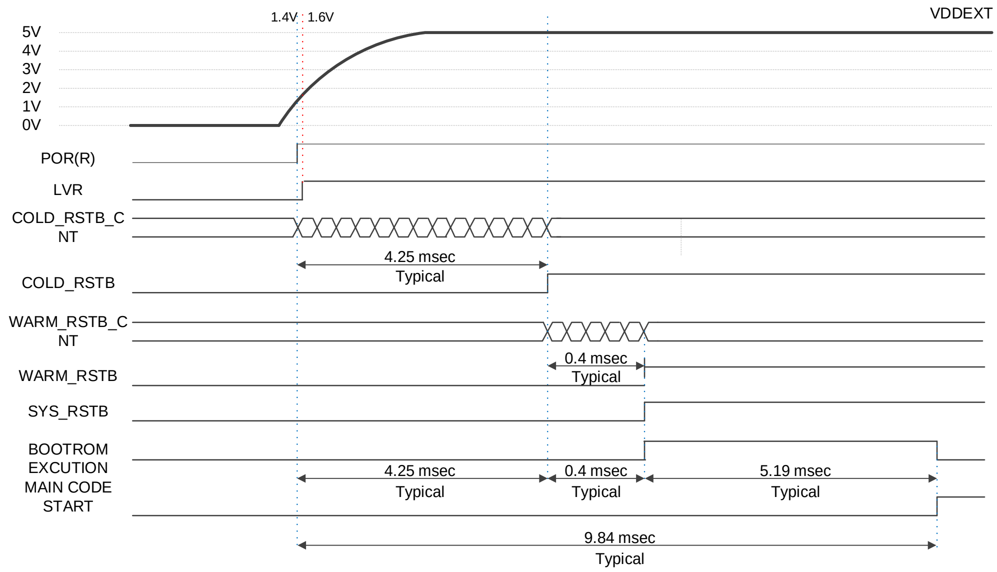


Figure 14. Power-up Procedure

4.3.2 Warm reset

Warm reset event has several reset sources and some parts of chip returns to an initial state when the warm reset condition is occurred.

The warm reset source is controlled by SCU_RSER register and the status is appeared in SCU_RSSR register. The reset for each peripheral blocks is controlled by SCU_PRER register. The reset can be masked independently.

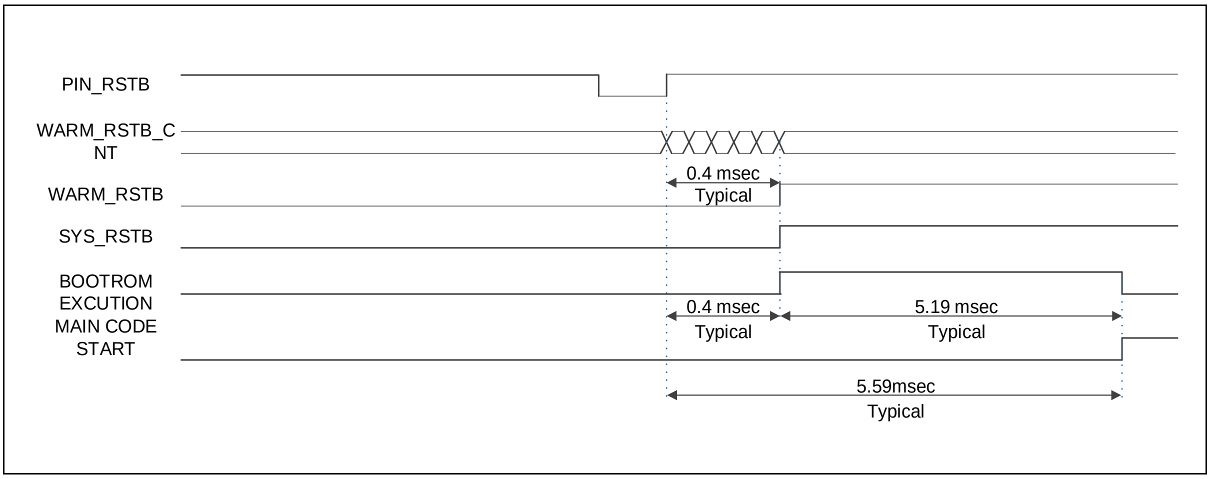


Figure 15. Warm Reset Diagram

4.3.3 LVR reset

Voltage level of LVR is set by low voltage reset configuration register (SCULV_LVRCNFIG). Reset status of the LVR is shown in SCU_RSSR register. The LVR reset is controlled by SCULV_LVRCR register, which is cleared to “0x00” by POR reset.

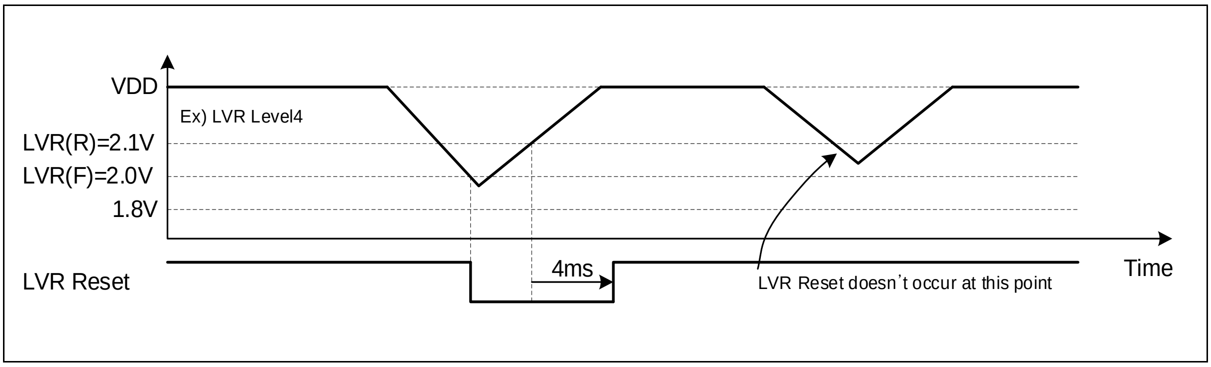


Figure 16. LVR Reset Timing Diagram

4.3.4 Reset tree

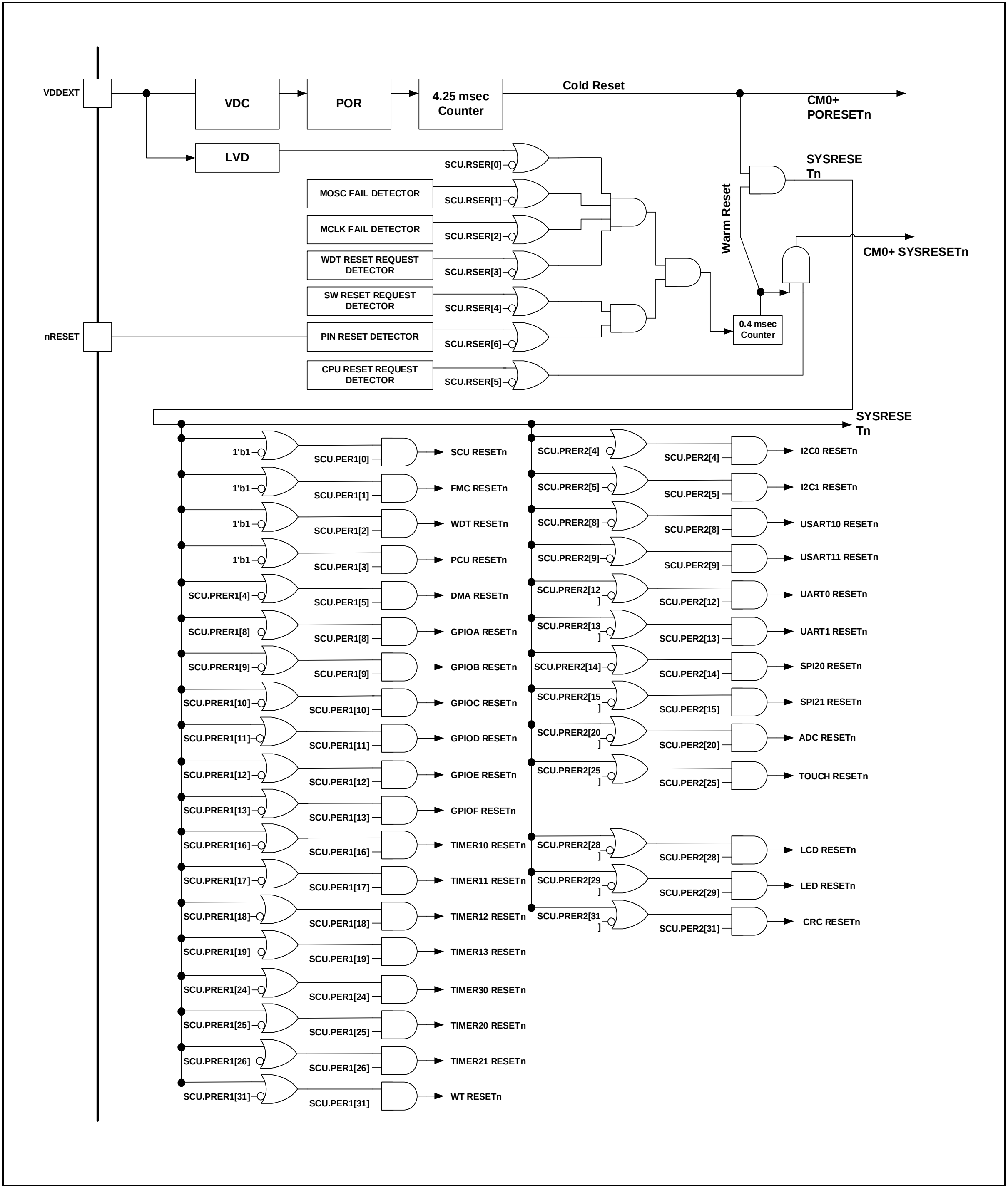
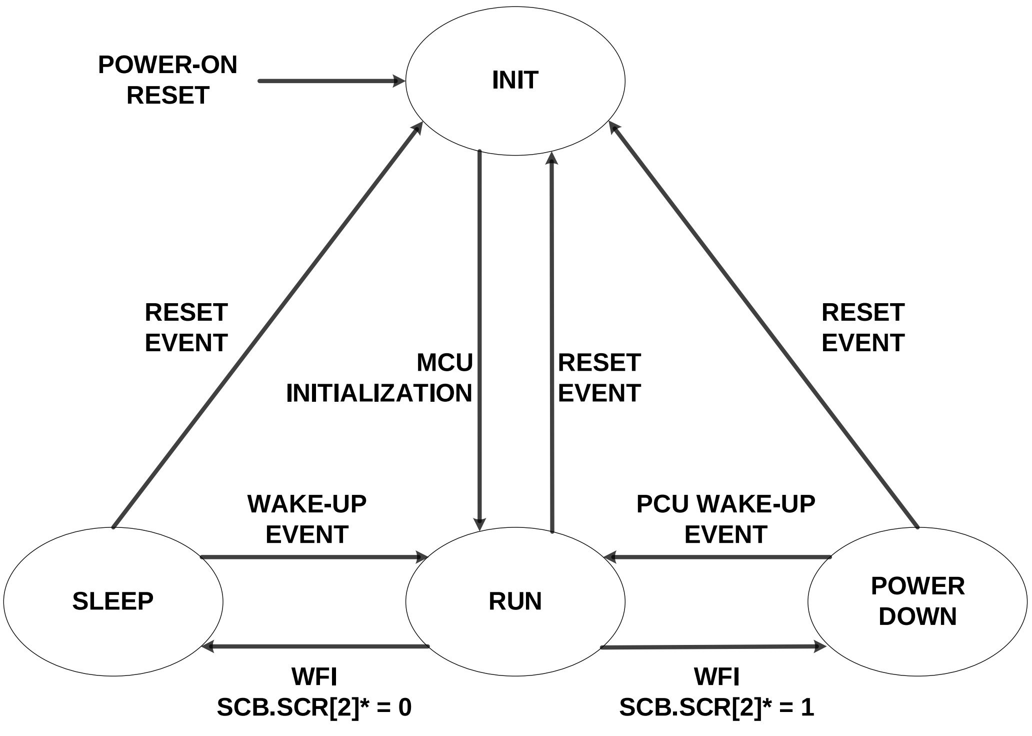


Figure 17. Reset Tree Configuration

4.4 Operation mode

INIT mode is an initial state of the chip when a reset is asserted. In RUN mode, CPU shows the maximum performance with high-speed clock system. SLEEP mode and Power Down modes can be used as a low power consumption mode. In the low power consumption mode, power is effectively managed to reduce power consumption by halting processor core and unused peripherals. Figure 18 describes transition between the operation modes.



*note) SCB.SCR is System Control Register in System Control Block

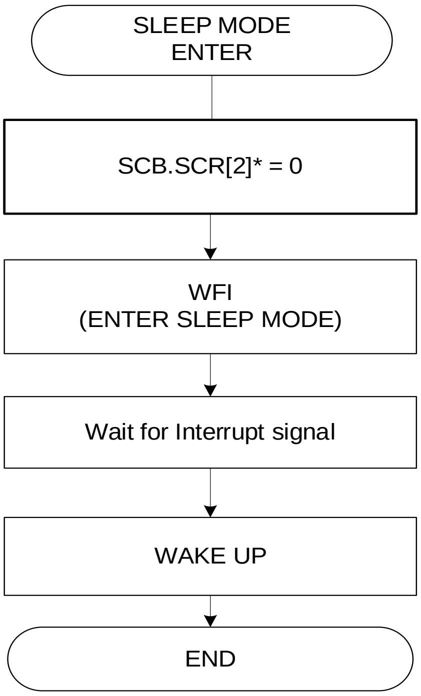
Figure 18. Transition between Operation Modes

4.4.1 RUN mode

In RUM mode, CPU and the peripheral hardware operate with a high-speed clock. After a reset followed by INIT state, the system enters in the RUN mode.

4.4.2 SLEEP mode

Only CPU is stopped in this mode. Each peripheral function can be enabled by the function enable and clock enable bit in the PER and PCER register.



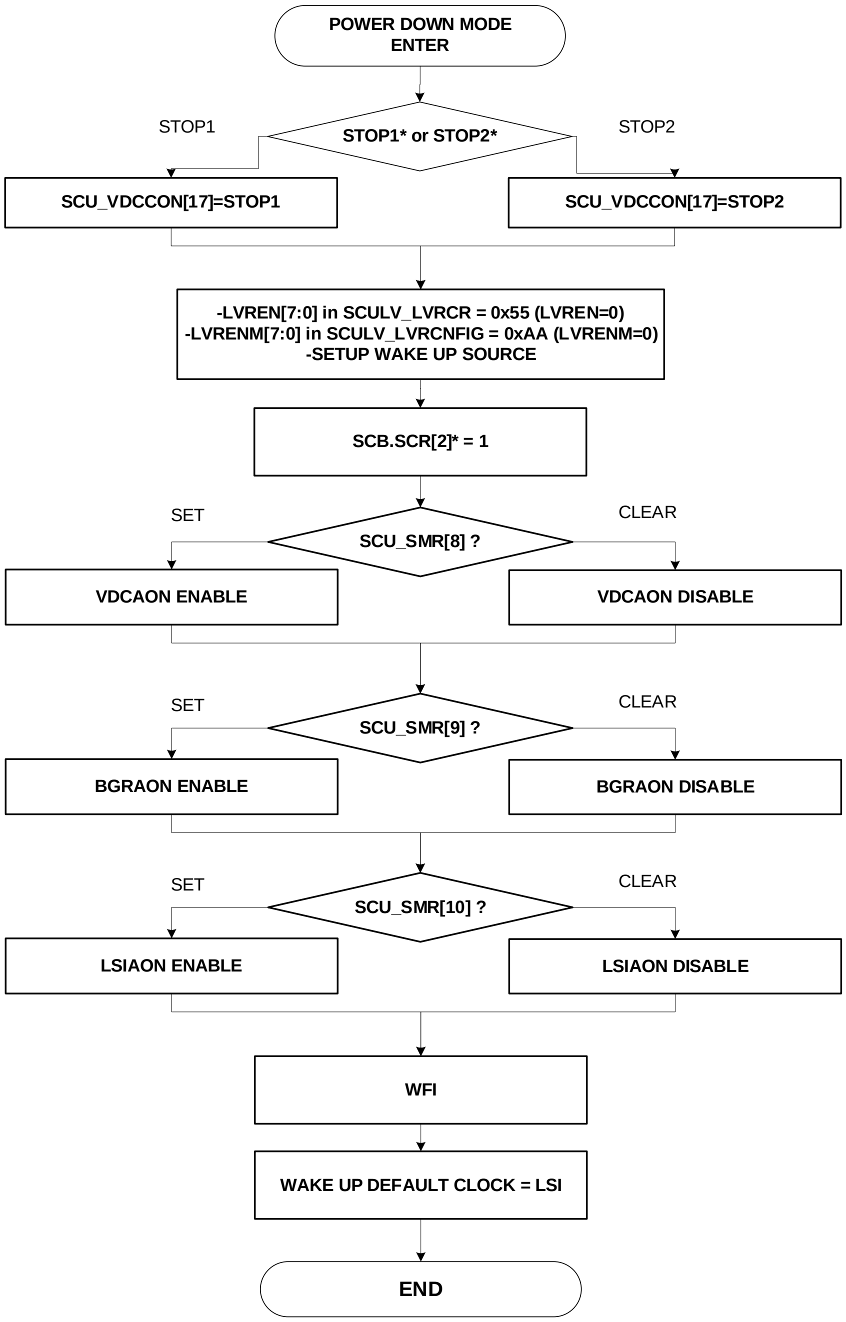
NOTE: SCB.SCR is System Control Register in System Control Block

Figure 19. SLEEP Mode Operation Sequence

4.4.3 Power-down mode

In STOP mode, all the internal circuits are entered the stop state.

Power down operation has special power off sequence as below picture.



*note 1) when STOP1, VDC current is limited 500uA (In this mode, LSI can be used as the wake-up source clock to enable LSIAON in SCU_SMR register.)
*note 2) when STOP2, VDC current is limited 10uA (In this mode, LSIAON and VDCAON in SCU_SMR register should be disabled.)
*note 3) SCB.SCR is System Control Register in System Control Block

Figure 20. Power-down Mode Sequence

4.5 Registers

Table 10 and Table 11 show base address and register map of the SCU (chip configuration).

Table 10. Base Address of SCU (Chip Configuration)

Name	Base address
SCU (Chip Configuration)	0x4000_F000

Table 11. SCU Register Map (Chip Configuration)

Name	Offset	Type	Description	Reset value	Reference
SCU_VENDORID	0x0000	RO^{NOTE}	Vendor Identification Register	0x4142_4F56	
SCU_CHIPID	0x0004	RO^{NOTE}	Chip Identification Register.	0x4D31_A0xx	
SCU_REVNR	0x0008	RO^{NOTE}	Revision Number Register	0x0000_00xx	

NOTE: 'RO' means 'Read Only'.

Table 12 and Table 13 show base address and register map of the SCU.

Table 12. Base Address of SCU

Name	Base address
SCU	0x4000_0000

Table 13. SCU Register Map

Name	Offset	Type	Description	Reset value	Reference
SCU_SMR	0x0004	RW	System Mode Register	0x0000_0000	
SCU_SCR	0x0008	RW	System Control Register	0x0000_0000	
SCU_WUER	0x0010	RW	Wake up source enable register	0x0000_0000	
SCU_WUSR	0x0014	RO	Wake up source status register	0x0000_0000	
SCU_RSER	0x0018	RW	Reset source enable register	0x0000_0069	
SCU_RSSR	0x001C	RW	Reset source status register	0x0000_00A0	
SCU_PRER1	0x0020	RW	Peripheral reset enable register 1	0x870F_3F1F	
SCU_PRER2	0x0024	RW	Peripheral reset enable register 2	0xBA10_F330	

Table 13. SCU Register Map (continued)

Name	Offset	Type	Description	Reset value	Reference
SCU_PER1	0x0028	RW	Peripheral enable register 1	0x0000_000F	
SCU_PER2	0x002C	RW	Peripheral enable register 2	0x0000_0100	
SCU_PCER1	0x0030	RW	Peripheral clock enable register 1	0x0000_000F	
SCU_PCER2	0x0034	RW	Peripheral clock enable register 2	0x0000_0100	
SCU_PPCLKSR	0x0038	RW	Peripheral clock selection register	0x0000_0000	
SCU_CSCR	0x0040	RW	Clock Source Control register	0x0000_0800	
SCU_SCCR	0x0044	RW	System Clock Control register	0x0000_0000	
SCU_CMR	0x0048	RW	Clock Monitoring register	0x0000_0090	
SCU_NMIR	0x004C	RW	NMI control register	0x0000_0000	
SCU_COR	0x0050	RW	Clock Output Control register	0x0000_000F	
SCU_PLLCON	0x0060	RW	PLL Control register	0x0000_0000	
SCU_VDCCON	0x0064	RW	VDC Control register	0x0000_007F	
SCU_TIRCCON	0x0068	RW	Touch IRC Control register	0x0000_0000	
SCU_LSICON	0x006C	RW	Internal Ring OSC Control Register	0x0000_0001	
SCU_EOSCR	0x0080	RW	External Oscillator control register	0x0000_1014	
SCU_EMODR	0x0084	RW	External mode pin read register	0x0000_0000	
SCU_RSTDBCR	0x0088	RW	Pin Reset Debounce Control Register	0x0000_0000	
SCU_MCCR1	0x0090	RW	Misc. Clock Control register 1	0x0000_0000	
SCU_MCCR2	0x0094	RW	Misc. Clock Control register 2	0x0000_0000	
SCU_MCCR3	0x0098	RW	Misc. Clock Control register 3	0x0000_0000	
SCU_MCCR4	0x009C	RW	Misc. Clock Control register 4	0x0000_0000	
SCU_MCCR5	0x00A0	RW	Misc. Clock Control register 5	0x0000_0000	
SCU_MCCR6	0x00A4	RW	Misc. Clock Control register 6	0x0000_0000	

NOTES:

1. 'RO' means 'Read Only'.
2. 'RW' means 'Read and Write'.

Table 14 and Table 15 show base address and register map of the LVI/LVR unit.

Table 14. Base Address of LVI/LVR

NAME	BASE ADDRESS
SCULV(LVI/LVR)	0x4000_5100

Table 15. LVI/LVR Register Map

Name	Offset	Type	Description	Reset value	Reference
SCULV_LVICR	0x0000	RW	Low Voltage Indicator Control Register	0x0000_0000	
SCULV_LVRCR	0x0004	RW	Low Voltage Reset Control Register	0x0000_0000	
SCULV_LVRCNFIG	0x0008	RW	Configuration for Low Voltage Reset	0x0000_000F	

NOTES:

1. 'RO' means 'Read Only' and 'RW' means 'Read and Write'.
2. 'RC' means 'Read and Write 1 Clear'.

4.5.1 SCU_VENDORID: vendor ID register

The SCU_VENDORID register shows the vendor identification information. This is a 32-bit read-only register.

SCU_VENDORID=0x4000_F000

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
VENDID			
0x4142_4F56			
RO			

31 0	VENDID	Vendor Identification bits. 0x4142_4F56

4.5.2 SCU_CHIPID: chip ID register

The SCU_CHIPID register shows chip identification information. This is a 32-bit read-only register.

SCU_CHIPID=0x4000_F004

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CHIPID			
xxxx xxxx			
RO			

31 0	CHIPID	Chip Identification bits.	
		0x4D31A01D	256k bytes flash memory for program
		0x4D31A01C	128k bytes flash memory for program

4.5.3 SCU_REVNR: revision number register

The SCU_REVNR is a 32-bit read-only register with 32/16/8-bit access.

SCU_REVNR=0x4000_F008

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved			REVNO
0x000000			xx
-			RO

7 0	REVNO	Chip Revision Number. These bits are fixed by manufacturer.

4.5.4 SCU_SMR: system mode register

Current operating mode is shown in this SCU mode register. The previous operating mode will be saved in this register after reset event. There is a VDC On/Off control bit in power down mode.

SCU_SMR=0x4000_0004

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11	10	9	8	7 6	5 4	3 2 1 0
Reserved	LSIAON	BGRAON	VDCAON	Reserved	PREVMODE	Reserved
-	0	0	0	-	00	-
-	RW	RW	RW	-	RO	-

10	LSIAON	LSI Always On select bit in power down mode	
		0	LSI is automatically off entering power down mode
		1	LSI isn't automatically off entering power down mode
		Note) It should be cleared to '0' in STOP2 (It can only be used in STOP1)	
9	BGRAON	BGR Always on select bit in power down mode	
		0	BGR is automatically off entering power down mode
		1	BGR isn't automatically off entering power down mode
8	VDCAON	VDC Always on select bit in power down mode	
		0	VDC is automatically off entering power down mode
		1	VDC isn't automatically off entering power down mode
		Note) It should be cleared to '0' in STOP2 (It can only be used in STOP1)	
5 4	PREVMODE	Previous operating mode before current reset event	
		00	Previous operating mode was RUN mode
		01	Previous operating mode was SLEEP mode
		10	Previous operating mode was Power Down mode
		11	Previous operating mode was INIT mode

4.5.5 SCU_SCR: system control register

It is possible to reset MCU as SWRST bit set. The SCU_SCR is a 32-bit register.

SCU_SCR=0x4000_0008

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
WTIDKY	Reserved	SWRST
0x0000	-	0
WO	-	RW

31 16	WTIDKY	Write Identification Key	
		On writes, write 0x9EB3 to these bits, otherwise the write is ignored.	
0	SWRST	Internal soft reset activation bit (check RSER[4] for reset)	
		0	Normal operation
		1	Internal soft reset generated and auto cleared

4.5.6 SCU_WUER: wakeup source enable register

Enable wakeup source when the chip is in the Power Down mode. Wakeup sources which will be used the source of chip wakeup should be enabled in each bit field. If the source is used as a wakeup source, the corresponding bit should be written with '1'. If the source is not used as a wakeup source, the bit should be written with '0'.

SCU_WUER=-0x4000_0010

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14	13	12	11	10	9	8	7 6 5	4	3	2	1	0
Reserved		Reserved	GPIOFWUE	GPIOEWUE	GPIODWUE	GPIOCWUE	GPIOBWUE	GPIOAWUE	Reserved	USART11WUE	USART10WUE	WTWUE	WDTWUE	LVRWUE
-		-	0	0	0	0	0	0	-	0	0	0	0	0
-		-	RW	RW	RW	RW	RW	RW	-	RW	RW	RW	RW	RW

13	GPIOFWUE	Enable wakeup source of GPIOF port pin change event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation
12	GPIOEWUE	Enable wakeup source of GPIOE port pin change event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation
11	GPIODWUE	Enable wakeup source of GPIOD port pin change event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation
10	GPIOCWUE	Enable wakeup source of GPIOC port pin change event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation
9	GPIOBWUE	Enable wakeup source of GPIOB port pin change event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation
8	GPIOAWUE	Enable wakeup source of GPIOA port pin change event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation
4	USART11WUE	Enable wakeup source of USART11 change event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation
3	USART10WUE	Enable wakeup source of USART10 change event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation
2	WTWUE	Enable wakeup source of watch timer event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation
1	WDTWUE	Enable wakeup source of watchdog timer event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation
0	LVRWUE	Enable wakeup source of LVR event	
		0	Not used for wakeup source
		1	Enable the wakeup event generation

NOTE: When WTWUE or WDTWUE is used, it can use only LSI based clock source.

4.5.7 SCU_WUSR: wakeup source status register

When the system is woken up by any wakeup source, the wakeup source is identified by reading the SCU_WUSR register. When the bit is set to 1, the corresponding wakeup source issues the wake-up signal to SCU. The bit will be cleared when the event source is cleared by the software.

SCU_WUSR=0x4000_0014

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14	13	12	11	10	9	8	7 6 5	4	3	2	1	0
Reserved		Reserved	GPIOFWU	GPIOEWU	GPIODWU	GPIOCWU	GPIOBWU	GPIOAWU	Reserved	USART11WU	USART10WU	WTWU	WDTWU	LVRWU
-		-	0	0	0	0	0	0	-	0	0	0	0	0
-		-	RO	RO	RO	RO	RO	RO	-	RO	RO	RO	RO	RO

13	GPIOFWU	Status of wakeup source of GPIOF port pin change event	
		0	No wakeup event
		1	Wakeup event was generated
12	GPIOEWU	Status of wakeup source of GPIOE port pin change event	
		0	No wakeup event
		1	Wakeup event was generated
11	GPIODWU	Status of wakeup source of GPIOD port pin change event	
		0	No wakeup event
		1	Wakeup event was generated
10	GPIOCWU	Status of wakeup source of GPIOC port pin change event	
		0	No wakeup event
		1	Wakeup event was generated
9	GPIOBWU	Status of wakeup source of GPIOB port pin change event	
		0	No wakeup event
		1	Wakeup event was generated
8	GPIOAWU	Status of wakeup source of GPIOA port pin change event	
		0	No wakeup event
		1	Wakeup event was generated
4	USART11WU	Status of wakeup source of USART11 change event	
		0	No wakeup event
		1	Wakeup event was generated
3	USART10WU	Status of wakeup source of USART10 change event	
		0	No wakeup event
		1	Wakeup event was generated
2	WTWU	Status of wakeup source of watch timer event	
		0	No wakeup event
		1	Wakeup event was generated
1	WDTWU	Status of wakeup source of watchdog timer event	
		0	No wakeup event
		1	Wakeup event was generated
0	LVRWU	Status of wakeup source of LVR event	
		0	No wakeup event
		1	Wakeup event was generated

4.5.8 SCU_RSER: reset source enable register

A reset source to CPU can be selected by the SCU_RSER register. When writing '1' in the bit field of each reset source, the reset source event will be transferred to reset generator. When writing '0' in the bit field of each reset source, the reset source event will be masked and not generate the reset event.

SCU_RSER=0x4000_0018

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Reserved				PINRST	CPURST	SWRST	WDTRST	MCKFRST	MOFRST	LVRRST
-				1	1	0	1	0	0	1
-				RW	RW	RW	RW	RW	RW	RW

6	PINRST	External pin reset enable bit	
		0	Reset from this event is masked
		1	Reset from this event is enabled
5	CPURST	CPU request reset enable bit	
		0	Reset from this event is masked
		1	Reset from this event is enabled
4	SWRST	Software reset enable bit	
		0	Reset from this event is masked
		1	Reset from this event is enabled
3	WDTRST	Watchdog Timer reset enable bit	
		0	Reset from this event is masked
		1	Reset from this event is enabled
2	MCKFRST	MCLK Clock fail reset enable bit	
		0	Reset from this event is masked
		1	Reset from this event is enabled
1	MOFRST	HSE Clock fail reset enable bit	
		0	Reset from this event is masked
		1	Reset from this event is enabled
0	LVRRST	LVR reset enable bit	
		0	Reset from this event is masked
		1	Reset from this event is enabled

4.5.9 SCU_RSSR: reset source status register

The SCU_RSSR shows reset source information when reset event is occurred. '1' means a reset event existed and '0' means no reset event exists for the corresponding reset source.

SCU_RSSR=0x4000_001C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Reserved			PORST	PINRST	CPURST	SWRST	WDTRST	MCKFRST	MOFRST	LVDRST
-			1	0	1	0	0	0	0	0
-			RW	RW	RW	RW	RW	RW	RW	RW

7	PORST	Power on reset status bit	
		0	Read: Reset from this event was not exist Write: no effect
		1	Read: Reset from this event was occurred Write: Clear the status
6	PINRST	External pin reset status bit	
		0	Read: Reset from this event was not exist Write: no effect
		1	Read: Reset from this event was occurred Write: Clear the status
5	CPURST	CPU request reset status bit	
		0	Read: Reset from this event was not exist Write: no effect
		1	Read: Reset from this event was occurred Write: Clear the status
4	SWRST	Software reset status bit	
		0	Read: Reset from this event was not exist Write: no effect
		1	Read: Reset from this event was occurred Write: Clear the status
3	WDTRST	Watchdog Timer reset status bit	
		0	Read: Reset from this event was not exist Write: no effect
		1	Read: Reset from this event was occurred Write: Clear the status
2	MCKFRST	MCLK Clock fail reset status bit	
		0	Read: Reset from this event was not exist Write: no effect
		1	Read: Reset from this event was occurred Write: Clear the status
1	MOFRST	HSE Clock fail reset status bit	
		0	Read: Reset from this event was not exist Write: no effect
		1	Read: Reset from this event was occurred Write: Clear the status
0	LVRRST	LVR reset status bit	
		0	Read: Reset from this event was not exist Write: no effect
		1	Read: Reset from this event was occurred Write: Clear the status

NOTE: When reset source is founded, write '1' into the corresponding bit to clear the reset status.

4.5.10 SCU_PRER1: peripheral reset enable register 1

The reset of each peripheral by event reset, can be masked by user setting. The SCU_PRER1/SCU_PRER2 register will control the enable of the event reset. If the corresponding bit is ‘1’, the peripheral corresponded with this bit, accepts the reset event. Otherwise, the peripheral is protected from a reset event and maintains the current operation.

SCU_PRER1=0x4000_0020

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WT	Reserved				TIMER21	TIMER20	TIMER30	Reserved				TIMER13	TIMER12	TIMER11	TIMER10	Reserved		GPIOF	GPIOE	GPIOD	GPIOC	GPIOB	GPIOA	Reserved			DMA	PCU	WDT	FMC	SCU
1	-				1	1	1	-				1	1	1	1	-		1	1	1	1	1	1	-			1	1	1	1	1
RW	-				RW	RW	RW	-				RW	RW	RW	RW	-		RW	RW	RW	RW	RW	RW	-			RW	RW	RW	RW	RW

31	WT	WT reset mask
26	TIMER21	TIMER21 reset mask
25	TIMER20	TIMER20 reset mask
24	TIMER30	TIMER30 reset mask
19	TIMER13	TIMER13 reset mask
18	TIMER12	TIMER12 reset mask
17	TIMER11	TIMER11 reset mask
16	TIMER10	TIMER10 reset mask
13	GPIOF	GPIOF reset mask
12	GPIOE	GPIOE reset mask
11	GPIOD	GPIOD reset mask
10	GPIOC	GPIOC reset mask
9	GPIOB	GPIOB reset mask
8	GPIOA	GPIOA reset mask
4	DMA	DMA reset mask
3	PCU	Port controller reset mask
2	WDT	Watchdog Timer reset mask
1	FMC	Flash memory controller reset mask
0	SCU	Power Management Unit reset mask

4.5.11 SCU_PRER2: peripheral reset enable register 2

The SCU_PRER2 is a 32-bit register.

SCU_PRER2=0x4000_0024

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC	Reserved	LED	LCD	Reserved		TOUCH	Reserved				ADC	Reserved				SPI21	SPI20	UART1	UART0	Reserved		USART11	USART10	Reserved		I2C1	I2C0	Reserved			
1	-	1	1	-		1	-				1	-				1	1	1	1	-		1	1	-		1	1	-			
RW	-	RW	RW	-		RW	-				RW	-				RW	RW	RW	RW	-		RW	RW	-		RW	RW	-			

31	CRC	CRC reset mask
29	LED	LED reset mask
28	LCD	LCD reset mask
25	TOUCH	TOUCH reset mask
20	ADC	ADC reset mask
15	SPI21	SPI21 reset mask
14	SPI20	SPI20 reset mask
13	UART1	UART1 reset mask
12	UART0	UART0 reset mask
9	USART11	USART11 reset mask
8	USART10	USART10 reset mask
5	I2C1	I2C1 reset mask
4	I2C0	I2C0 reset mask

4.5.12 SCU_PER1: peripheral enable register1

Before using a peripheral unit, it must be activated by writing '1' to a corresponding bit in the SCU_PER1/ SCU_PER2 register. Before the activation, the peripheral will stay in reset state.

All peripherals are enabled by default. To disable the peripheral unit, write '0' to the corresponding bit in the SCU_PER1/ SCU_PER2 register, and then the peripheral goes under reset state.

SCU_PER1=0x4000_0028

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WT	Reserved				TIMER21	TIMER20	TIMER30	Reserved				TIMER13	TIMER12	TIMER11	TIMER10	Reserved		GPIOF	GPIOE	GPIOD	GPIOC	GPIOB	GPIOA	Reserved			DMA	Reserved			
0	-				0	0	0	0				0	0	0	0	-		0	0	0	0	0	0	-			0	1111			
RW	-				RW	RW	RW	RW				RW	RW	RW	RW	-		RW	RW	RW	RW	RW	RW	-			RW	-			

31	WT	WT function enable
26	TIMER21	TIMER21 function enable
25	TIMER20	TIMER20 function enable
24	TIMER30	TIMER30 function enable
19	TIMER13	TIMER13 function enable
18	TIMER12	TIMER12 function enable
17	TIMER11	TIMER11 function enable
16	TIMER10	TIMER10 function enable
13	GPIOF	GPIOF function enable
12	GPIOE	GPIOE function enable
11	GPIOD	GPIOD function enable
10	GPIOC	GPIOC function enable
9	GPIOB	GPIOB function enable
8	GPIOA	GPIOA function enable
4	DMA	DMA function enable

4.5.13 SCU_PER2: peripheral enable register 2

The SCU_PER2 is a 32-bit register.

SCU_PER2=0x4000_002C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRC	Reserved	LED	LCD	Reserved		TOUCH	Reserved				ADC	Reserved				SPI21	SPI20	UART1	UART0	Reserved		USART11	USART10	Reserved		I2C1	I2C0	Reserved			
0	-	0	0	-		0	-				0	-				0	0	0	0	-		0	1	-		0	0	-			
RW	-	RW	RW	-		RW	-				RW	-				RW	RW	RW	RW	-		RW	RW	-		RW	RW	-			

31	CRC	CRC function enable
29	LED	LED function enable
28	LCD	LCD function enable
25	TOUCH	TOUCH function enable
20	ADC	ADC function enable
15	SPI21	SPI21 function enable
14	SPI20	SPI20 function enable
13	UART1	UART1 function enable
12	UART0	UART0 function enable
9	USART11	USART11 function enable
8	USART10	USART10 function enable
5	I2C1	I2C1 function enable
4	I2C0	I2C0 function enable

4.5.14 SCU_PCER1: peripheral clock enable register 1

To use peripheral unit, its clock should be activated by writing '1' to the corresponding bit in the SCU_PCER1 register. Without enabling the clock, the peripheral won't operate properly.

To stop the clock of the peripheral, write '0' to the corresponding bit in the SCU_PCER1/ SCU_PCER2 register, then the clock will be stopped.

SCU_PCER1=0x4000_0030

31	30 29 28 27	26	25	24	23 22 21 20	19	18	17	16	15 14	13	12	11	10	9	8	7 6 5	4	3 2 1 0
WT	Reserved	TIMER21	TIMER20	TIMER30	Reserved	TIMER13	TIMER12	TIMER11	TIMER10	Reserved	GPIOF	GPIOE	GPIOD	GPIOC	GPIOB	GPIOA	Reserved	DMA	Reserved
0	-	0	0	0	0	0	0	0	0	-	0	0	0	0	0	0	-	0	1111
RW	-	RW	RW	RW	RW	RW	RW	RW	RW	-	RW	RW	RW	RW	RW	RW	-	RW	-

31	WT	WT clock enable
26	TIMER21	TIMER21 clock enable
25	TIMER20	TIMER20 clock enable
24	TIMER30	TIMER30 clock enable
19	TIMER13	TIMER13 clock enable
18	TIMER12	TIMER12 clock enable
17	TIMER11	TIMER11 clock enable
16	TIMER10	TIMER10 clock enable
13	GPIOF	GPIOF clock enable
12	GPIOE	GPIOE clock enable
11	GPIOD	GPIOD clock enable
10	GPIOC	GPIOC clock enable
9	GPIOB	GPIOB clock enable
8	GPIOA	GPIOA clock enable
4	DMA	DMA clock enable

4.5.15 SCU_PCER2: peripheral clock register 2

To use peripheral unit, its clock should be activated by writing '1' to the corresponding bit in the SCU_PCER2 register.

SCU_PCER2=0x4000_0034

31	30	29	28	27 26	25	24 23 22 21	20	19 18 17 16	15	14	13	12	11 10	9	8	7 6	5	4	3 2 1 0
CRC	Reserved	LED	LCD	Reserved	TOUCH	Reserved	ADC	Reserved	SPI21	SPI20	UART1	UART0	Reserved	USART11	USART10	Reserved	I2C1	I2C0	Reserved
0	-	0	0	-	0	-	0	-	0	0	0	0	-	0	1	-	0	0	-
RW	-	RW	RW	-	RW	-	RW	-	RW	RW	RW	RW	-	RW	RW	-	RW	RW	-

31	CRC	CRC clock enable
29	LED	LED clock enable
28	LCD	LCD clock enable
25	TOUCH	TOUCH clock enable
20	ADC	ADC clock enable
15	SPI21	SPI21 clock enable
14	SPI20	SPI20 clock enable
13	UART1	UART1 clock enable
12	UART0	UART0 clock enable
9	USART11	USART11 clock enable
8	USART10	USART10 clock enable
5	I2C1	I2C1 clock enable
4	I2C0	I2C0 clock enable

4.5.16 SCU_PPCLKSR: peripheral clock selection register

The SCU_PPCLKSR is a 32-bit register with 32/16/8-bit access.

SCU_PPCLKSR=0x4000_0038

31 30 29 28 27 26 25 24 23	22	21	20	19 18	17	16 15 14 13 12 11 10 9 8	7 6	5	4 3	2 1	0
Reserved	T1xCLK	Reserved	T20CLK	Reserved	T30CLK	Reserved	LCDCLK	Reserved	WTCLK	Reserved	WDTCLK
-	0	-	0	-	0	-	00	-	00	-	0
-	RW	–	RW	-	RW	-	RW	-	RW	-	RW

22	T1xCLK	Timer 1x Clock Selection bit	
		0	SCU_MCCR1 Timer1x clock
		1	PCLK clock
20	T20CLK	Timer 20 Clock Selection bit	
		0	SCU_MCCR2 Timer20 clock
		1	PCLK clock
17	T30CLK	Timer 30 Clock Selection bit	
		0	SCU_MCCR2 Timer30 clock
		1	PCLK clock
7 6	LCDCLK	LCD Clock Selection bit	
		00	SCU_MCCR5 LCD clock
		01	LSE clock
		10	WDTRC clock
		11	Reserved
4 3	WTCLK	Watch Timer Clock Selection bit	
		00	SCU_MCCR3 WT clock
		01	LSE clock
		10	WDTRC clock
		11	Reserved
		NOTE: These bits should be changed during the WTEN bit of watch timer control register (WTCR) is "0b".	
0	WDTCLK	Watch-dog Timer Clock Selection bit	
		0	WDTRC clock
		1	SCU_MCCR3 WDT clock

NOTE:

1. WDTCLK can be reset only by LVR reset and VPWRSW POR.

2. When WTCLK or WDTCLK is used for deepsleep wakeup source, it can use only LSI based clock source. (LSI clock or WDTRC clock)

4.5.17 SCU_CSCR: clock source control register

A31T214/216 series has multiple clock sources to generate internal operating clocks. Each clock source can be controlled by the SCU_CSCR register.

SCU_CSCR=0x4000_0040

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
WTIDKY		LSECON	LSICON	HSICON	HSECON
0x0000		0000	1000	0000	0000
WO		RW	RW	RW	RW

31 16	WTIDKY	Write Identification Key	
		On writes, write 0xA507 to these bits, otherwise the write is ignored.	
15 12	LSECON	External crystal sub oscillator control	
		0XXX	Disable external sub crystal oscillator
		1000	Enable external sub crystal oscillator
		1001	Enable external sub crystal oscillator divide by 2
		1010	Enable external sub crystal oscillator divide by 4
		1100	Enable external sub crystal oscillator in Power Down mode
		1101	Enable external sub crystal oscillator divide by 2 in Power Down mode
		1110	Enable external sub crystal oscillator divide by 4 in Power Down mode
		Other	Reserved
11 8	LSICON	Low speed internal oscillator control	
		0XXX	Disable low speed internal oscillator
		1000	Enable low speed internal oscillator
		1001	Enable low speed internal oscillator divided by 2
		1010	Enable low speed internal oscillator divided by 4
		Other	Reserved
7 4	HSICON	High speed internal oscillator control	
		0XXX	Disable high speed internal oscillator
		1000	Enable high speed internal oscillator
		1001	Enable high speed internal oscillator divided by 2
		1010	Enable high speed internal oscillator divided by 4
		1011	Enable high speed internal oscillator divided by 8
		1100	Enable high speed internal oscillator divided by 16
		1101	Enable high speed internal oscillator divided by 32
		1111	Reserved
3 0	HSECON	External crystal main oscillator control	
		0XXX	Disable external main crystal oscillator
		1000	Enable external main crystal oscillator
		1001	Enable external main crystal oscillator divided by 2
		1010	Enable external main crystal oscillator divided by 4
		Other	Reserved

4.5.18 SCU_SCCR: system clock control register

Selected system clock source in the SCU_SCCR becomes MCLK. Before changing clock, clock sources have to be alive by the SCU_CSCR register.

SCU_SCCR=0x4000_0044

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3	2	1 0
WTIDKY	Reserved	PLLINCLKSEL	MCLKSEL
0x0000	-	0	00
WO	-	RW	RW

31 16	WTIDKY	Write Identification Key	
		On writes, write 0x570A to these bits, otherwise the write is ignored.	
2	PLLINCLKSEL	PLL input source select register	
		0	HSI clock is used as PLLINCLK clock
		1	HSE clock is used as PLLINCLK clock
1 0	MCLKSEL	System clock select register	
		00	Internal ring oscillator(500kHz)
		01	LSE XTAL (32kHz)
		10	PLL bypassed clock
		11	PLL output clock

NOTE: When change MCLKSEL, both clock sources should be alive. Ex) Both of HSI and HSE should be alive, otherwise the chip will malfunction.

4.5.19 SCU_CMR: clock monitoring register

A clock can be monitored by LSI for security purpose.

SCU_CMR=0x4000_0048

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14 13 12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		MCLKREC	Reserved	LSEMNT	LSEIE	LSEFAIL	LSESTS	MCLKMNT	MCLKIE	MCLKFAIL	MCLKSTS	HSEMNT	HSEIE	HSEFAIL	HSESTS
-		0	-	0	0	0	0	1	0	0	1	0	0	0	0
-		RW	-	RW	RW	RC	RO	RW	RW	RC	RO	RW	RW	RC	RO

15	MCLKREC	MCLK fail auto recovery	
		0	MCLK is changed to LSI by default when MCLKFAIL issued
		1	MCLK auto recovery is disabled
11	LSEMNT	External sub oscillator monitoring enable	
		0	External sub oscillator monitoring disabled
		1	External sub oscillator monitoring enabled
10	LSEIE	External sub oscillator fail interrupt enable	
		0	External sub oscillator fail interrupt disabled
		1	External sub oscillator fail interrupt enabled
9	LSEFAIL	External sub oscillator fail interrupt	
		0	External sub oscillator fail interrupt not occurred
		1	Read: External sub oscillator fail interrupt is pending Write: Clear pending interrupt
8	LSESTS	External sub oscillator status	
		0	Not oscillate
		1	External sub oscillator is working normally
7	MCLKMNT	MCLK monitoring enable	
		0	MCLK monitoring disabled
		1	MCLK monitoring enabled
6	MCLKIE	MCLK fail interrupt enable	
		0	MCLK fail interrupt disabled
		1	MCLK fail interrupt enabled
5	MCLKFAIL	MCLK fail interrupt	
		0	MCLK fail interrupt not occurred
		1	Read: MCLK fail interrupt is pending Write: Clear pending interrupt
4	MCLKSTS	MCLK clock status	
		0	No clock is present on MCLK
		1	Clock is present on MCLK
3	HSEMNT	External main oscillator monitoring enable	
		0	External main oscillator monitoring disabled
		1	External main oscillator monitoring enabled
2	HSEIE	External main oscillator fail interrupt enable	
		0	External main oscillator fail interrupt disabled
		1	External main oscillator fail interrupt enabled
1	HSEFAIL	External main oscillator fail interrupt	
		0	External main oscillator fail interrupt not occurred
		1	Read: External main oscillator fail interrupt is pending Write: Clear pending interrupt
0	HSESTS	External main oscillator status	
		0	Not oscillate

	1	External main oscillator is working normally

4.5.20 SCU_NMIR: NMI control register

The SCU_NMIR is a non-maskable interrupt configuration register which can be set by software. There are three types of interrupt sources for WDT and SCU.

This register makes a jump to NMI handler if a selected NMI event occurs. It must check event status.

For clearing occurred status, it should clear the interrupt flags of that peripheral occurred.

For writing access key, 0xA32C must be written to the bit field of the SCU_NMIR[31:16].

SCU_NMIR=0x4000_004C

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11	10	9	8	7 6 5 4 3	2	1	0
ACCESSCODE	Reserved	WDTINTSTS	MCLKFAILSTS	LVRSTS	Reserved	WDTINTEN	MCLKFAILEN	LVREN
-	-	0	0	0	-	0	0	0
WO	-	RO	RO	RO	-	RW	RW	RW

31 16	ACCESSCODE	This field enables writing access to this register. Writing 0xA32C is to enable writing.	
10	WDTINTSTS	WDT Interrupt condition status bit This bit can’t invoke NMI interrupt without enable bit	
		0	Not occurred
		1	Event occurred
9	MCLKFAILSTS	MCLK Fail condition status bit This bit can’t invoke NMI interrupt without enable bit	
		0	Not occurred
		1	Event occurred
8	LVRSTS	LVR condition status bit This bit can’t invoke NMI interrupt without enable bit	
		0	Not occurred
		1	Event occurred
2	WDTINTEN	WDT Interrupt condition enable for NMI interrupt	
		0	Disable
		1	Enable
1	MCLKFAILEN	MCLK Fail condition enable for NMI interrupt	
		0	Disable
		1	Enable
0	LVREN	LVR Fail condition enable for NMI interrupt	
		0	Disable
		1	Enable

4.5.21 SCU_COR: clock output register

The A31T214/216 series can drive a clock from internal MCLK clock with a dedicated post divider. To use CLKO output function, it should be set as CLKO that has output mode in Pin Mux.

The SCU_COR is an 8-bit register.

SCU_COR=0x4000_0050

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																											CLKOEN	CLKODIV			
-																											0	1111			
-																											RW	RW			

4	CLKOEN	Clock output enable	
		0	CLKO is disabled and stay "L" output
		1	CLKO Is enabled
3 0	CLKODIV	Clock output divider value CLKO = MCLK (CLKODIV = 0) $\text{CLKO} = \frac{MCLK}{2 * (\text{CLKODIV} + 1)} \quad (CLKODIV > 0)$	

4.5.22 SCU_PLLCON: PLL control register

Integrated PLL will synthesize high speed clock for extremely high performance of CPU. The PLL is controlled by setting the register. The SCU_PLLCON is a 32-bit register.

SCU_PLLCON=0x4000_0060

31	30	29 28 27 26 25 24	23	22	21	20	19	18 17 16	15 14 13 12 11 10 9 8	7 6 5 4	3 2 1 0
Reserved	PLLRDY	Reserved	PLLRSTB	PLLEN	BYPASSB	PLLMODE	Reserved	PREDIV	POSTRIV1	POSTDIV2	OUTDIV
-	0	-	0	0	0	0	-	000	00000000	0000	0000
-	RO	-	RW	RW	RW	RW	-	RW	RW	RW	RW

30	PLLRDY	PLL clock ready flag. After PLLEN is activated, this flag indicates the PLL is locked. (When the pre-divider clock is 2MHz, it is estimated about 300us delay)	
		0	PLL unlocked
		1	PLL locked
23	PLLRSTB	PLL reset	
		0	PLL reset is asserted
		1	PLL reset is negated
22	PLLEN	PLL enable	
		0	PLL is disabled
		1	PLL is enabled
21	BYPASSB	PLLINCLK bypass	
		0	FOUT is bypassed as PLLINCLK
		1	FOUT is PLL output
20	PLLMODE	PLL VCO mode (D)	
		0	VCO frequency is the same with FOUT
		1	VCO frequency is double of FOUT
18 16	PREDIV	PLLINCLK pre-divider (R)	
		0 to 7	PLLINCLK divided by (PREDIV + 1), (PLLINCLK/1 to PLLINCLK/8)
15 8	POSTDIV1	Feedback control 1 (N1)	
		0x00	N1 = 0 (N1 + 1)
		0xFF	N1 = 255 (N1 + 1)
7 4	POSTDIV2	Feedback control 1 (N2)	
		0x0	N2 = 0 (N2 + 1)
		0xF	N2 = 15 (N2 + 1)
3 0	OUTDIV	Output divider control (P)	
		0x0	P = 0 (P+1)
		0xF	P = 15 (P+1)

NOTES:

1. Bit 20 of PLLCON must be kept at 0.
2. Set PLLRSTB to '1' after at least 1us when PLLEN is set to '1'.
3. At power down mode, set PLLRSTB to '0', PLLEN to '0'
4. Output calculation formula is as followings:

$$\mathrm{F_{OUT}} = \frac{\mathrm{PLLINCLK} \times (\mathrm{N_1} + 1)}{(\mathrm{R} + 1) \times (\mathrm{N_2} + 1) \times (\mathrm{P} + 1)} * (D + 1)$$

Symbol	Description
R	Pre Divider Counter Value
N_1	Post Divider1 Counter Value
N_2	Post Divider2 Counter Value
P	Output Divider Counter Value
D	Frequency Doubler

Calculating PLL output frequency value

PLL of the A31T214/216 series can accurately set the output frequency, F_{OUT}, in 1MHz increments. The formula for the F_{IN} input to the F_{VCO} input of the PLL is as follows, and the input range of the F_{IN} frequency is between 1MHz and 3MHz. However, it is recommended to set the input frequency (FIN) to 2MHz as much as possible.

$$\mathrm{FIN} = \frac{\mathrm{PLLINCLK}}{(\mathrm{R}+1)}, \qquad \text{Where } 1\mathrm{MHz} \le \mathrm{FIN} \le 3\mathrm{MHz}\ (\text{Recommanded FIN} = 2\mathrm{MHz})$$

At this time, the range of F_{VCO} output frequency should be set to 200MHz or less, and the calculation formula is as follows.

$$\mathrm{F_{VCO}} = \mathrm{FIN} \times (\mathrm{N_1}+1), \quad \mathrm{VCO} \le 200\mathrm{MHz}$$

As a result, the final frequency of PLL, F_{OUT}, can be obtained from the formula below using the formula above.

$$\mathrm{F_{OUT}} = \frac{\mathrm{PLLINCLK} \times (\mathrm{N_1}+1)}{(\mathrm{R}+1) \times (\mathrm{N_2}+1) \times (\mathrm{P}+1)} \times (\mathrm{D}+1) = \frac{\mathrm{FIN} \times (\mathrm{N_1}+1)}{(\mathrm{N_2}+1) \times (\mathrm{P}+1)} \times (\mathrm{D}+1)$$

4.5.23 SCU_VDCCON: VDC control register

The SCU_VDCCON is the On-chip VDC control register.

Writing to the VDCWDLY is available when the VDCWDLY_WEN bit is set to '1'.

SCU_VDCCON=0x4000_0064

31 30 29 28 27 26 25 24	23 22 21 20	19 18	17	16 15 14 13 12 11 10 9	8	7 6 5 4 3 2 1 0
Reserved	VDC15 WTIDKY	Reserved	VDC15_STOP	Reserved	VDCWDLY_WEN	VDCWDLY
-	0000	-	0	-	0	0x7F
-	WO	-	RW	-	WO	RW

23 20	VDC15 WTIDKY	VDC15 Write Identification Key On writes, write 0x5 to these bits, otherwise the write is ignored.	
17	VDC15_STOP	VDC15 STOP Mode Control Signal	
		0	STOP1 Mode
		1	STOP2 Mode (LSI clock-based wake-up sources are not available.)
8	VDCWDLY_WEN	VDCWDLY value write enable. VDCWDLY value can be written with writing '1' to VDCWDLY_WEN bit simultaneously.	
7 0	VDCWDLY	VDC warm-up delay count value. When SCU is waked up from power down mode, the warm-up delay is inserted for VDC output being stabilized. The amount of delay can be defined with this register value 7F: 4msec	

NOTE: Reserved bits should never be modified.

4.5.24 SCU_TIRCCON: TOUCH IRC control register

SCU_TIRCCON=0x4000_0068

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															TIRCCON
-																															0
-																															RW

0	TIRCCON	Touch IRC Control signal	
		0	Touch IRC disable
		1	Touch IRC enable

4.5.25 SCU_EOSCR: external oscillator control register

External main crystal oscillator has two characteristics. For the noise immunity, NMOS amp type is recommended and for the low power characteristic, INV amp type is recommended.

The SCU_EOSCR is a 16-bit register.

SCU_EOSCR=0x4000_0080

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15	14	13 12	11 10 9	8	7	6	5 4	3 2	1	0
Reserved	ESEN	Reserved	ESISEL	Reserved	ESNCBYPS	EMEN	Reserved	ISEL	NCOPT	Reserved	NCSKIP
-	0		01	-	0	0	-	01	01	-	0
-	WO		RW	-	RW	WO	-	RW	RW	-	RW

15	ESEN	Write enable for External LSE	
		0	Write access disabled
		1	Write access enabled
13 12	ESISEL	Select current for External LSE	
		00	1.57uA
		01	1.79uA
		10	1.93uA
		11	2.04uA
8	ESNCBYPS	Noise Cancel Bypass enable for External LSE	
		0	Disable
		1	Enable (Noise Cancel bypassed)
7	EMEN	Write enable for External HSE	
		0	Write access disabled
		1	Write access enabled
5 4	ISE	Select current for External HSE	
		00	150uA
		01	300uA
		10	450uA
		11	600uA
3 2	NCOPT	Noise Cancel delay Option for External HSE	
		00 01 10 11	25ns (12MHz < HSE < 16MHz) 20ns (8MHz < HSE < 12MHz) 15ns (4MHz < HSE < 8MHz) 10ns (2MHz < HSE < 4MHz)
0	NCSKIP	Noise Cancel SKIP enable for External HSE	
		0	Disable
		1	Enable (Noise Cancel skipped)

4.5.26 SCU_EMODR: external mode status register

The SCU_EMODR shows external mode pin status while booting. This is an 8-bit register.

SCU_EMODR=0x4000_0084

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0
Reserved	BOOT
-	0
-	R

0	BOOT	BOOT pin level	
		0	BOOT pin is low
		1	BOOT pin is high

4.5.27 SCU_RSTDBCR: pin reset debounce control register

SCU_ RSTDBCR=0x4000_0088

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14	13 12 11 10 9 8	7 6 5 4 3 2 1	0
WTIDKY	Reserved	CLKCNT	Reserved	EN
0x0000	-	0x00	-	0
WO	-	RW	-	RW

31 16	WTIDKY	Write Identification Key	
		On writes, write 0x0514 to these bits, otherwise the write is ignored.	
13 8	CLKCNT	Noise Cancel delay Option for External LSI	
		N	N clock checking for debounce by LSI (500kHz)
0	EN	Pin reset debounce enable bit	
		0	Disable
		1	Enable

NOTE: If a user wants to operate pin reset debounce, the user must enable LSI (500kHz). Because pin reset debounce uses LSI for clock source.

4.5.28 SCU_MCCR1: miscellaneous clock control register 1

The A31T214/216 series can drive a clock from internal MCLK clock with dedicated post divider. The STCSEL and STCDIV bits of the SCU_MCCR1 are used as SYSTICK external clock source. The TEXT1CSEL and TEXT1DIV bits of the SCU_MCCR1 are used as TIMER1n external clock source.

The SCU_MCCR1 is a 32-bit register.

SCU_MCCR1=0x4000_0090

31 30 29 28 27	26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11	10 9 8	7 6 5 4 3 2 1 0
Reserved	TEXT1CSEL	TEXT1DIV	Reserved	STCSEL	SYSTICKDIV
-	0x0	0x00	-	0x0	0x00
-	RW	RW	-	RW	RW

26 24	TEXT1CSEL	TIMER1n EXT Clock source select bit	
		0xx	LSI (500kHz)
		011	LSE (32.768kHz)
		100	MCLK (bus clock)
		101	HSI (32MHz)
		110	HSE
		111	PLL Clock
23 16	TEXT1DIV	TIMER1n EXT Clock N divider	
		8'h0	disabled
		8'hN	(selected clock) / N
		To change the value, set 0x0 first without changing TEXT1CSEL	
10 8	STCSEL	SYSTIC Clock source select bit	
		0xx	LSI (500kHz)
		011	LSE (32.768kHz)
		100	MCLK (bus clock)
		101	HSI (32MHz)
		110	HSE
		111	PLL Clock
7 0	STDIV	SYSTICK Clock N divider	
		8'h0	disabled
		8'hN	(selected clock) / N
		To change the value, set 0x0 first without changing STCSEL.	

4.5.29 SCU_MCCR2: miscellaneous clock control register 2

The A31T214/216 series can drive a clock from internal MCLK clock with a dedicated post divider. The TEXT2CSEL and TEXT2DIV bits of the SCU_MCCR2 are used as a TIMER20 external clock source. The TEXT3CSEL and TEXT3DIV bits of the SCU_MCCR2 are used as a TIMER30 external clock source.

The SCU_MCCR2 is a 32-bit register.

SCU_MCCR2=0x4000_0094

31 30 29 28 27	26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11	10 9 8	7 6 5 4 3 2 1 0
Reserved	TEXT3CSEL	TEXT3DIV	Reserved	TEXT20CSEL	TEXT20DIV
-	0x0	0x00	-	0x0	0x00
-	RW	RW	-	RW	RW

26 24	TEXT3CSEL	TIMER 30 EXT Clock source select bit	
		0xx	LSI (500kHz)
		011	LSE (32.768kHz)
		100	MCLK (bus clock)
		101	HSI (32MHz)
		110	HSE
		111	PLL Clock
23 16	TEXT3DIV	TIMER 30 EXT Clock N divider	
		8’h0	disabled
		8’hN	(selected clock) / N
		To change the value, set 0x0 first without changing TEXT3DIV	
10 8	TEXT20CSEL	TIMER 20 EXT Clock source select bit	
		0xx	LSI (500kHz)
		011	LSE (32.768kHz)
		100	MCLK (bus clock)
		101	HSI (32MHz)
		110	HSE
		111	PLL Clock
7 0	TEXT20DIV	TIMER 20 EXT Clock N divider	
		8’h0	disabled
		8’hN	(selected clock) / N
		To change the value, set 0x0 first without changing TEXT20CSEL.	

4.5.30 SCU_MCCR3: miscellaneous Clock Control register 3

The A31T214/216 series can drive a clock from an internal MCLK clock with a dedicated post divider. The WDTCSEL and WDTDIV bits of the SCU_MCCR3 are used as a WDT external clock source. The WTEXTCSEL and WTEXTCDIV bits of the SCU_MCCR3 are used as a WT external clock source.

The SCU_MCCR3 is a 32-bit register.

SCU_MCCR3=0x4000_0098

31 30 29 28 27	26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11	10 9 8	7 6 5 4 3 2 1 0
Reserved	WTEXTCSEL	WTEXTCDIV	Reserved	WDTCSEL	WDTDIV
-	0x0	0x00	-	0x0	0x00
-	RW	RW	-	RW	RW

26 24	WTEXTCSEL	WT External Clock source select bit	
		0xx	LSI (500kHz)
		011	LSE (32.768kHz)
		100	MCLK (bus clock)
		101	HSI (32MHz)
		110	HSE
		111	PLL Clock
23 16	WTEXTCDIV	WT External Clock N divider	
		8’h0	disabled
		8’hN	(selected clock) / N
		To change the value, set 0x0 first without changing WTEXTCSEL	
10 8	WDTCSEL	WDT Clock source select bit	
		0xx	LSI (500kHz)
		011	LSE (32.768kHz)
		100	MCLK (bus clock)
		101	HSI (32MHz)
		110	HSE
		111	PLL Clock
7 0	WDTDIV	WDT Clock N divider	
		8’h0	disabled
		8’hN	(selected clock) / N
		To change the value, set 0x0 first without changing WDTCSEL.	

4.5.31 SCU_MCCR4: miscellaneous clock control register 4

The A31T214/216 series can drive a clock from an internal MCLK clock with a dedicated post divider. The PD0CSEL and PD0DIV bits of the SCU_MCCR4 are used as PA, PB, PC Debounce Clock source. The PD1CSEL and PD1DIV bits of the SCU_MCCR4 are used as PD, PE, PF Debounce Clock source.

The SCU_MCCR4 is a 32-bit register.

SCU_MCCR4=0x4000_009C

31 30 29 28 27	26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11	10 9 8	7 6 5 4 3 2 1 0
Reserved	PD1CSEL	PD1DIV	Reserved	PD0CSEL	PD0DIV
-	0x0	0x00	-	0x0	0x00
-	RW	RW	-	RW	RW

26 24	PD1CSEL	Debounce Clock for PORT source select bit (PD,PE,PF)	
		0xx	LSI (500kHz)
		011	LSE (32.768kHz)
		100	MCLK (bus clock)
		101	HSI (32MHz)
		110	HSE
		111	PLL Clock
23 16	PD1DIV	PORT Debounce Clock N divider (PD,PE,PF)	
		8'h0	disabled
		8'hN	(selected clock) / N
		To change the value, set 0x0 first without changing PD1CSEL.	
10 8	PD0CSEL	Debounce Clock for PORT source select bit (PA,PB,PC)	
		0xx	LSI (500kHz)
		011	LSE (32.768kHz)
		100	MCLK (bus clock)
		101	HSI (32MHz)
		110	HSE
		111	PLL Clock
7 0	PD0DIV	PORT Debounce Clock N divider (PA,PB,PC)	
		8'h0	disabled
		8'hN	(selected clock) / N
		To change the value, set 0x0 first without changing PD0CSEL.	

4.5.32 SCU_MCCR5: miscellaneous clock control register 5

The A31T214/216 series can drive a clock from an internal MCLK clock with a dedicated post divider. The LCDCSEL and LCDDIV bits of the SCU_MCCR5 are used as an LCD Clock source.

The SCU_MCCR5 is a 32-bit register.

SCU_MCCR5=0x4000_00A0

31 30 29 28 27	26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Reserved	LCDCSEL	LCDDIV	Reserved
-	000	0000_0000	-
-	RW	RW	-

26 24	LCDCSEL	LCD Clock source select bit	
		0xx	LSI (500kHz)
		011	LSE (32.768kHz)
		100	MCLK (bus clock) – not valid for LCD
		101	HSI (32MHz) – not valid for LCD
		110	HSE – not valid for LCD
		111	PLL Clock – not valid for LCD
23 16	LCDDIV	LCD Clock N divider	
		8’h0	Disabled
		8’hN	(selected clock) / N
		To change the value, set 0x0 first without changing LCDCSEL. **NOTE**: Clock is not activated during LCDDIV bit is disabled.	

4.5.33 SCULV_LVICR: low voltage indicator control register

The SCULV_LVICR is a 32-bit register with 32/16/8-bit access.

SCULV_LVICR=0x4000_5100

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Reserved			LVIEN	Reserved	LVINTEN	LVIFLAG	LVIVS			
-			0	-	0	0	0000			
-			RW	-	RW	RW	RW			

7	LVIEN	LVI Enable bit.	
		0	Disable low voltage indicator.
		1	Enable low voltage indicator.
5	LVINTEN	LVI Interrupt Enable bit.	
		0	Disable low voltage indicator interrupt.
		1	Enable low voltage indicator interrupt.
4	LVIFLAG	LVI Interrupt Flag bit.	
		0	No request occurred.
		1	Request occurred; This bit is cleared to '0' when write '1'.
3 0	LVIVS	LVI Voltage Selection bits.	
		0000	Level0
		0001	Level1
		0010	Level2
		0011	Level3
		0100	Level4
		0101	Level5
		0110	Level6
		0111	Level7
		1000	Level8
		1001	Level9
		1010	Level10
		1011	Level11
		1100	Level12
		1101	Level13
		1110	Level14
		1111	Level15

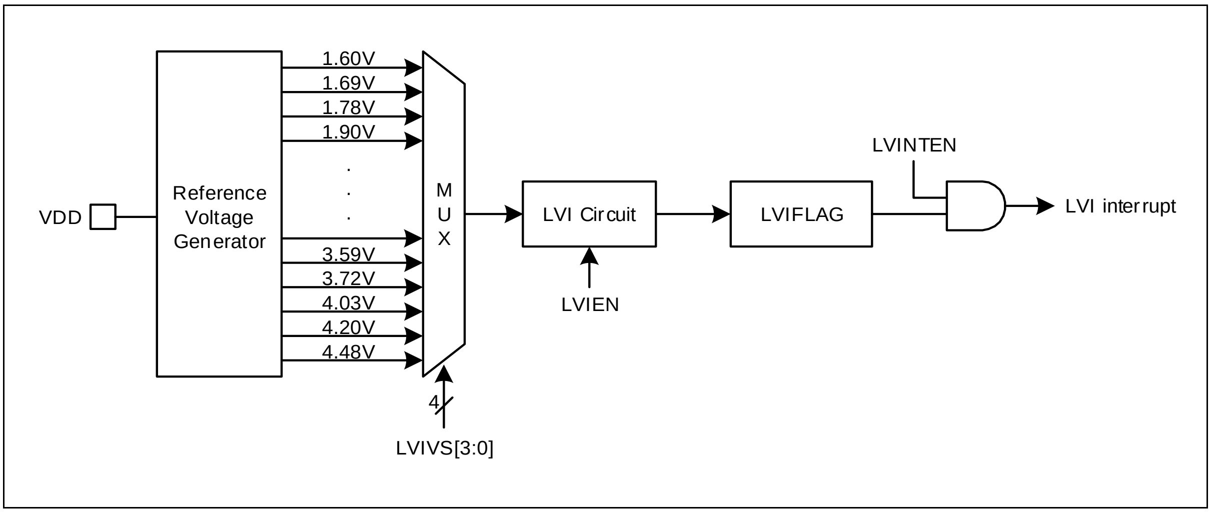


Figure 21. LVI Block Diagram

4.5.34 SCULV_LVRCR: low voltage reset control register

The SCULV_LVRCR is a 32-bit register with 32/16/8-bit access.

SCULV_LVRCR=0x4000_5104

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved			LVREN
-			0x00
-			RW

7 0	LVREN	LVR Enable bits. These bits are cleared to 0x00 by warm reset. To maintain this value when a warm reset occurs, write 0 to the SCU_PRER1.1 bit.	
		0x55	Disable low voltage reset. (LVREN=0)
		Others	Enable low voltage reset. (LVREN=1)

NOTE: When you disable the LVR, be careful not to change the LVRVS first. To use LVR or LVI function while the system is in STOP mode (DEEP SLEEP mode), set SCU_SMR<BGRAON> to '1' to enable BGR function of VDC.

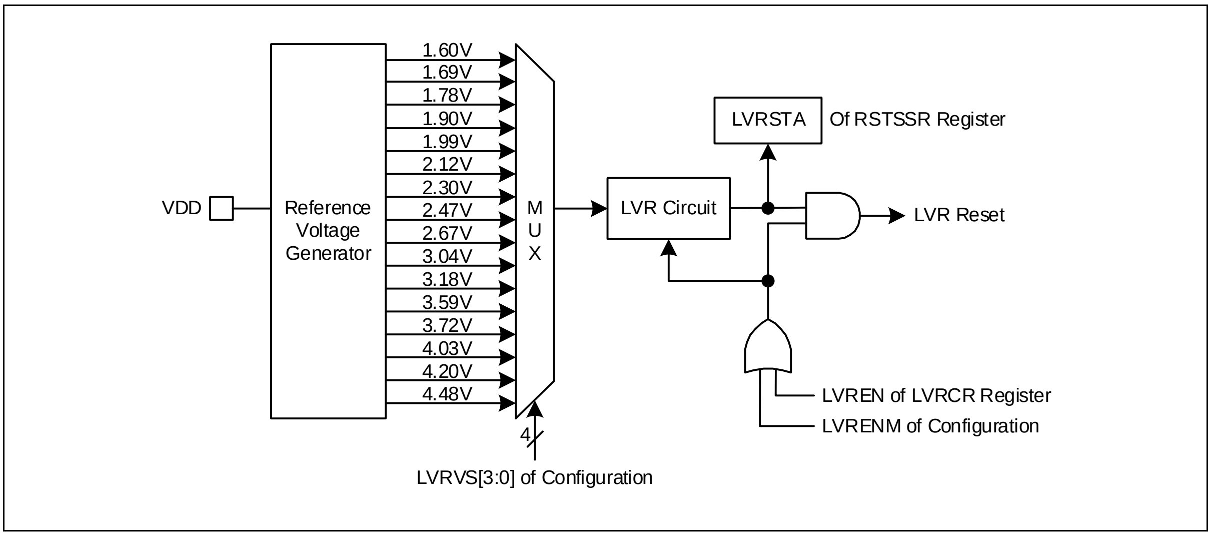


Figure 22. LVR Block Diagram

NOTE: When disabling LVR, be careful not to change LVRVS first.

4.5.35 SCULV_LVRCNFIG: configuration for low voltage reset

The SCULV_LVRCNFIG is a Low voltage indicator control register.

It is a 32-bit register with 32/16/8-bit access.

SCULV_LVRCNFIG =0x4000_5108

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4	3 2 1 0
WTIDKY		LVRENM	Reserved	LVRVS
0x0000		0x00	-	0xF
WO		RW	-	RW

31 16	WTIDKY	Write Identification Key	
		On writes, write 0x72A5 to these bits, otherwise the write is ignored.	
15 8	LVRENM	LVR Reset Operation Control Master Configuration	
		0xAA	LVR operation is decided by the LVREN of LVRCR register (LVRENM=0)
		Others	Master enable LVR operation (LVRENM=1)
3 0	LVRVS	LVR Voltage Selection bits.	
		1111	Level0
		1110	Level1
		1101	Level2
		1100	Level3
		1011	Level4
		1010	Level5
		1001	Level6
		1000	Level7
		0111	Level8
		0110	Level9
		0101	Level10
		0100	Level11
		0011	Level12
		0010	Level13
		0001	Level14
		0000	Level15

5 PCU and GPIO

Port Control Unit (PCU) configures and controls external I/Os as listed in the followings:

- External signal directions of each pins
- Interrupt trigger mode for each pins
- Internal pull-up/down register control and open drain control

General Purpose Input/Output (GPIO) is corresponding to the most pins except dedicated-function pins. GPIO ports are controlled by GPIO block as listed in the followings:

- Output signal level (H/L) select
- External interrupt interface
- Pull up/down enable or disable

Four pins in Table 16 are assigned for PCU and GPIO blocks.

Table 16. PCU and GPIO Pins

Pin name	Type	Description
PA	IO	PA0 to PA11
PB	IO	PB0 to PB11
PC	IO	PC0 to PC8
PD	IO	PD0 to PD5
PE	IO	PE0 to PE12
PF	IO	PF0 to PF7

5.1 PCU and GPIO block diagram

Figure 23 describes PCU in block diagram.

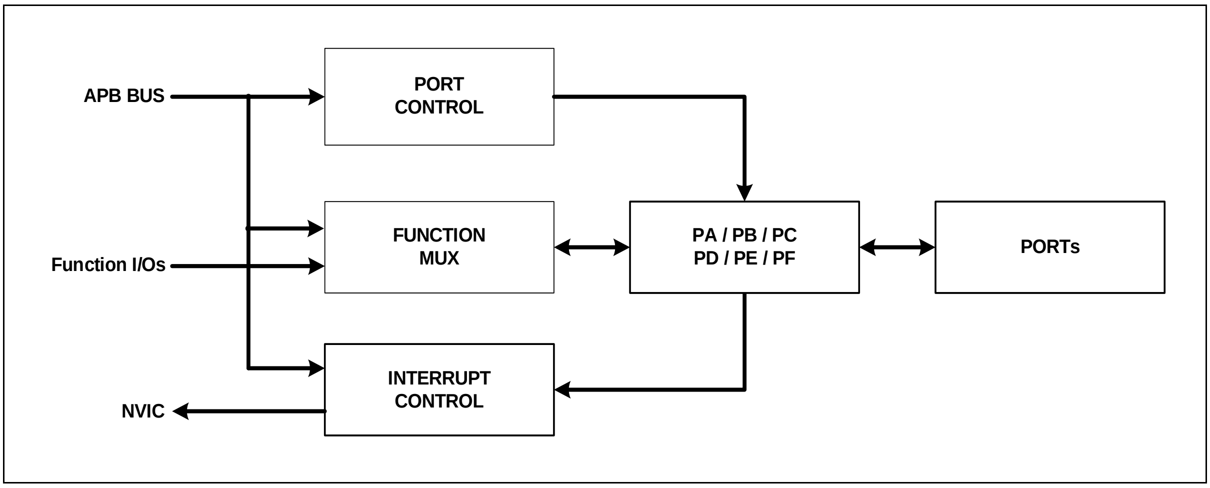


Figure 23. PCU Block Diagram

Figure 24 describes GPIO in block diagram, and Figure 25 introduces GPIO pins for external input / output.

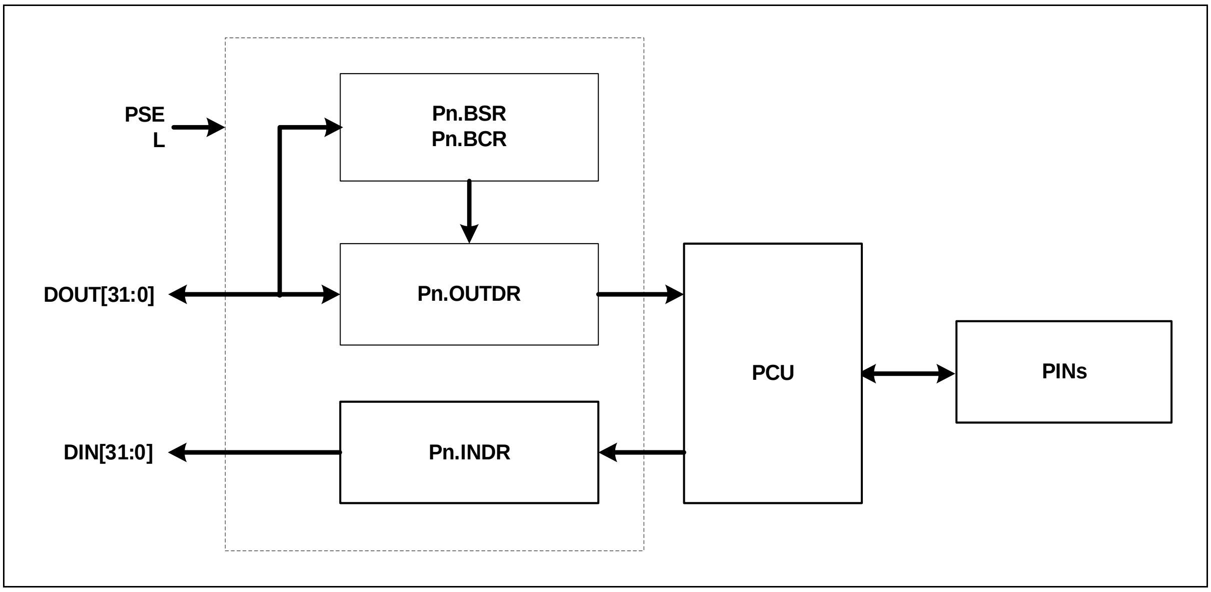


Figure 24. GPIO Block Diagram

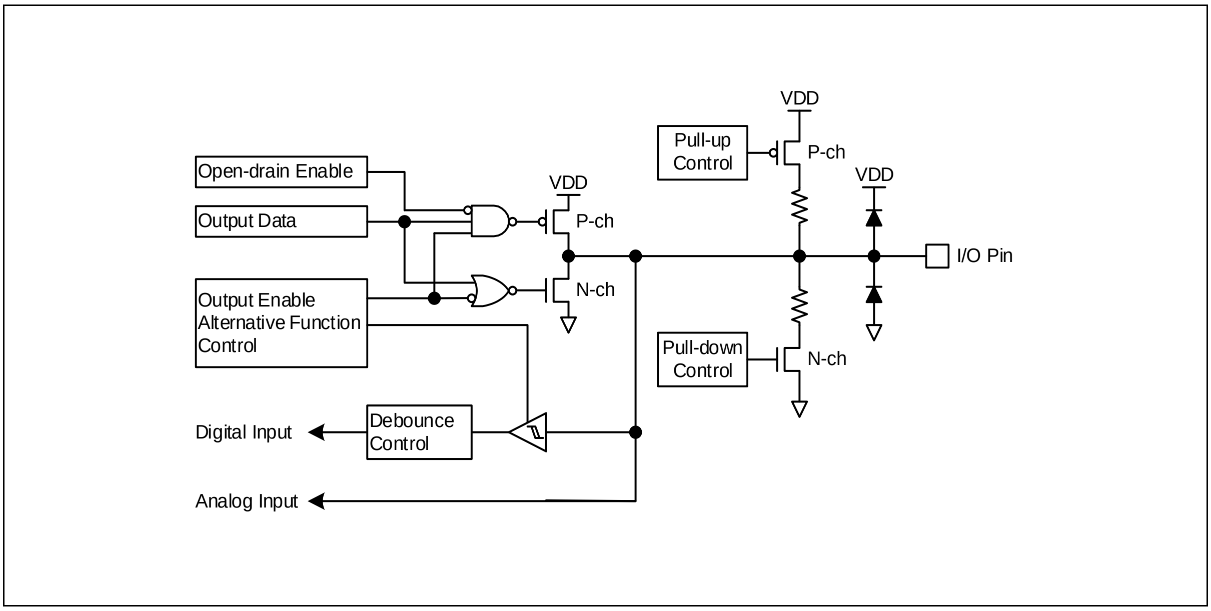


Figure 25. I/O Port Block Diagram (General I/O Pins)

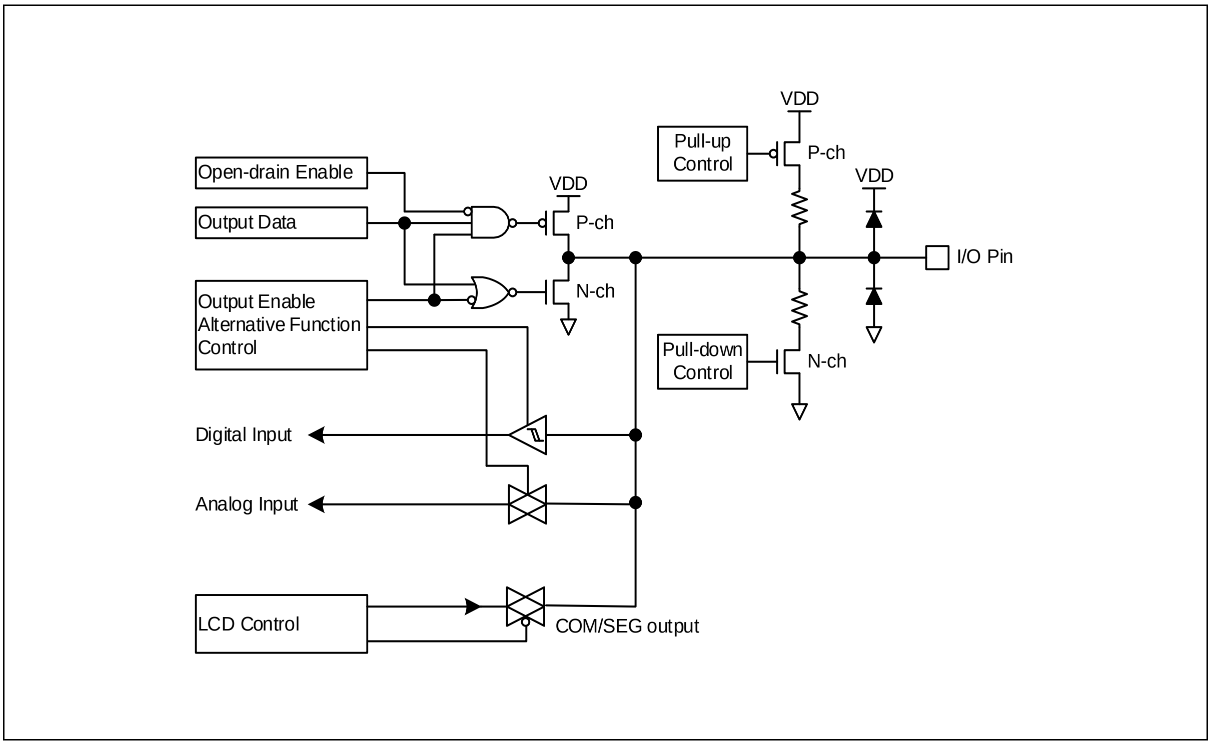


Figure 26. I/O Port Block Diagram (LCD Pins)

5.2 Pin multiplexing

GPIO pins have alternative function pins. Table 17 shows pin multiplexing information.

Table 17. GPIO Alternative Function

Pin name	Alternative function					
	AF0	**AF1**	**AF2**	**AF3**	**AF4**	**AF5**
PA0						CAPN
PA1	SEG22				AN14/AVREF	
PA2	SEG21				AN13	
PA3	SEG20				AN12	
PA4	SEG19				AN11	
PA5	SEG18	SDA1			AN10	
PA6	SEG17	SCL1			AN9	
PA7	SEG16				AN8	
PA8	SEG15				AN7	CS0
PA9	SEG14	T12O	T12C		AN6	CS1
PA10	SEG13	(T11O)	(T11C)		AN5	CS2
PA11	SEG12	T13O	T13C		AN4	CS3
PB0	SEG11	USART10_TXD	USART10_MOSI	(MOSI20)	AN3	CS4
PB1	SEG10	USART10_RXD	USART10_MISO	(MISO20)	AN2	CS5
PB2	SEG9		USART10_SCK	(SCK20)	AN1	CS6
PB3		BOOT	USART10_SS	(SS20)		
PB4	SEG8	TXD0	EC30		AN0	CS7
PB5	SEG7	RXD0	(T30C)			CS8
PB6	SEG6					
PB7	SEG5					
PB8	COM7/SEG4					
PB9	COM6/SEG3					
PB10	COM5/SEG2	TXD1	EC12			CS9
PB11	SEG1	RXD1	EC13			CS10
PC0		T20O	T20C			CS11
PC1		T21O	T21C	MOSI20		CS12
PC2			EC20	MISO20		CS13
PC3			EC21	SCK20		ISEG15/CS14
PC4		(T10O)	(T10C)	SS20		ISEG14/CS15
PC5						
PC6						
PC7						
PC8						

Table 17. GPIO Alternative Function (continued)

Pin name	Alternative function					
	AF0	AF1	AF2	AF3	AF4	AF5
PD0		SCL0	EC10	CLKO		ISEG13/CS16
PD1		SDA0	EC11			ISEG12/ICOM12/CS17
PD2		USART11_TXD	USART11_MOSI	(MOSI21)		ISEG11/ICOM11/CS18
PD3		USART11_RXD	USART11_MISO	(MISO21)		ISEG10/ICOM10/CS19
PD4		BLNK(PWM)	USART11_SCK	(SCK21)		ISEG9/ICOM9/CS20
PD5			USART11_SS	(SS21)		ISEG8/ICOM8/CS21
PE0		T11O	T11C			ISEG7/ICOM7/CS22
PE1		T10O	T10C	BLNK(PWM)		ISEG6/ICOM6/CS23
PE2		PWM30CB	(SCL0)	MOSI21		ISEG5/ICOM5
PE3	COM4/SEG0	PWM30CA	(SDA0)	MISO21		ISEG4/ICOM4
PE4	COM3/SEG31	PWM30BB		SCK21		ISEG3/ICOM3
PE5	COM2	PWM30BA		SS21		ISEG2/ICOM2
PE6	COM1	PWM30AB				ISEG1/ICOM1
PE7	COM0	PWM30AA				ISEG0/ICOM0
PE8	SEG30				VLC3	
PE9	SEG29				VLC2	
PE10	SEG28				VLC1	
PE11	SEG27				VLC0	
PE12	nRESET	nRESET	nRESET	nRESET	nRESET	nRESET
PF0	SEG26			SWDIO		
PF1	SEG25			SWCLK		
PF2	SEG24			(CLKO)		
PF3	SEG23		T30C			
PF4		(TXD1)			SXIN	
PF5		(RXD1)	(EC30)		SXOUT	
PF6		(TXD0)	(SDA1)		XIN	
PF7		(RXD0)	(SCL1)		XOUT	

NOTE: Unused pins are set to output from firmware (low output is recommended).

5.3 Registers

Table 18 and Table 19 show base address and register map of PCU.

Table 18. Base Address of PCU

Name	Base address	Description
PA	0x4000_1000	General Port A
PB	0x4000_1100	General Port B
PC	0x4000_1200	General Port C
PD	0x4000_1300	General Port D
PE	0x4000_1400	General Port E
PF	0x4000_1500	General Port F

Table 19. PCU and GPIO Register Map

Name	Offset	Type	Description	Reset value	Ref.
Pn_MOD	0x0000	RW	Port n Mode Register	0xXXXX_XXXX	5.3.1
Pn_TYP	0x0004	RW	Port n Output Type Selection Register	0x0000_0000	5.3.2
Pn_AFSR1	0x0008	RW	Port n Alternative Function Selection Register 1	0xXXXX_XXXX	5.3.3
Pn_AFSR2	0x000C	RW	Port n Alternative Function Selection Register 2	0xXXXX_XXXX	5.3.4
Pn_PUPD	0x0010	RW	Port n Pull-up/down Resistor Selection Register	0xXXXX_XXXX	5.3.5
Pn_INDR	0x0014	RO	Port n Input Data Register	0xXXXX_XXXX	5.3.6
Pn_OUTDR	0x0018	RW	Port n Output Data Register	0x0000_0000	5.3.7
Pn_BSR	0x001C	WO	Port n Output Bit Set Register	0x0000_0000	5.3.8
Pn_BCR	0x0020	WO	Port n Output Bit Clear Register	0x0000_0000	5.3.9
Pn_OUTDMSK	0x0024	RW	Port n Output Data Mask Register	0x0000_0000	5.3.10
Pn_DBCR	0x0028	RW	Port n Debounce Control Register	0x0000_0000	5.3.11
Pn_IER	0x002C	RW	Port n interrupt enable register	0x0000_0000	5.3.12
Pn_ISR	0x0030	RW	Port n interrupt status register	0x0000_0000	5.3.13
Pn_ICR	0x0034	RW	Port n interrupt control register	0x0000_0000	5.3.14
PCU_PORTEN (0x4000_1FF0)		WO	Port Access Enable	0x0000_0000	

NOTES:

1. Where n = A, B, C, D, E and F
2. For exception, the reset value of PB_MOD, PB_AFSR1, PB_PUPD register is 0x00FF_FFB3, 0x0000_1000, 0x0000_0040 respectively.
3. For exception, the reset value of PD_MOD, PD_AFSR1, PC_PUPD register is 0x0000_0FF0, 0x0000_0000, 0x0000_0005 respectively.
4. For exception, the reset value of PE_MOD, PE_AFSR2, PE_PUPD register is 0x02FF_FFFF, 0x0000_0000, 0x0100_0000 respectively.
5. For exception, the reset value of PF_MOD, PF_AFSR1, PF_PUPD register is 0x0000_FFFA, 0x0000_0033, 0x0000_0005 respectively.

5.3.1 Pn_MOD: port n mode register

Input or output control of each port pin. Each pin can be configured as an input pin, an output pin or an alternative function pin.

The Pn_MOD are 32-bit registers with 32/16/8-bit access (n = A, B, C, D, E and F).

PA_MOD=0x4000_1000, PB_MOD=0x4000_1100, PC_MOD=0x4000_1200
PD_MOD=0x4000_1300, PE_MOD=0x4000_1400, PF_MOD=0x4000_1500

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
MODE15	MODE14	MODE13	MODE12	MODE11	MODE10	MODE9	MODE8	MODE7	MODE6	MODE5	MODE4	MODE3	MODE2	MODE1	MODE0
11	11	11	11	11	11	11	11	11	11	11	11	11	11	11	11
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

2x+1 2x	MODEx	Port n Mode Selection bits, x:0 to 15	
		00	Input mode
		01	Output mode
		10	Alternative function mode
		11	Reserved

NOTE : 1) For exception, the reset value of PB_MOD, PD_MOD, PE_MOD, PF_MOD register is 0x00FF_FFB3, 0x0000_0FF0, 0x02FF_FFFF, 0x0000_FFFA respectively.
2) The Reserved state is a floating state in which the internal output path is open, and the input path is also blocked, so the port status cannot be checked.

5.3.2 Pn_TYP: port n output type selection register

The Pn_TYP select control options from a Push-pull output and Open-drain output for each port pin.

They are 32-bit registers with 32/16/8-bit access (n = A, B, C, D, E and F).

PA_TYP=0x4000_1004, PB_TYP=0x4000_1104, PC_TYP=0x4000_1204
PD_TYP=0x4000_1304, PE_TYP=0x4000_1404, PF_TYP=0x4000_1504

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	TYP15	TYP14	TYP13	TYP12	TYP11	TYP10	TYP9	TYP8	TYP7	TYP6	TYP5	TYP4	TYP3	TYP2	TYP1	TYP0
-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

x	TYPx	Port n Output Type Selection bits, x:0 to 15	
		0	Push-pull output
		1	Open-drain output

5.3.3 Pn_AFSR1: port n alternative function selection register 1

The Pn_AFSR1 must be set properly before using ports. Otherwise the ports cannot be guaranteed for their functionality.

They are 32-bit registers with 32/16/8-bit access (n = A, B, C, D, E and F).

PA_AFSR1=0x4000_1008, PB_AFSR1=0x4000_1108, PC_AFSR1=0x4000_1208
PD_AFSR1=0x4000_1308, PE_AFSR1=0x4000_1408, PF_AFSR1=0x4000_1508

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
AFSB7	AFSB6	AFSB5	AFSB4	AFSB3	AFSB2	AFSB1	AFSB0
0000	0000	0000	0000	0000	0000	0000	0000
RW	RW	RW	RW	RW	RW	RW	RW

4x+3 4x	AFSBx	Port n Alternative Function Selection bits, x:0 to 7	
		0000	Alternative Function 0 (AF0)
		0001	Alternative Function 1 (AF1)
		0010	Alternative Function 2 (AF2)
		0011	Alternative Function 3 (AF3)
		0100	Alternative Function 4 (AF4)
		0101	Alternative Function 5 (AF5)
		Others	Reserved

NOTE: 1) When HSE is used as the system clock (MCLK), the AFSBx bits must be configured as XIN/XOUT before changing the system clock and the value should not be changed.
2) When LSE is used as the system clock (MCLK) the AFSBx bits must be configured as SXIN/SXOUT before changing the system clock and the value should not be changed.
3) For exception, the reset value of PB_AFSR1, PF_AFSR1 register is 0x0000_1000, 0x0000_0033 respectively.

5.3.4 Pn_AFSR2: port n alternative function selection register 2

The Pn_AFSR2 must be set properly before using ports. Otherwise the ports cannot be guaranteed for their functionality.

They are 32-bit registers with 32/16/8-bit access (n = A, B, C, D, E and F).

PA_AFSR2=0x4000_100C, PB_AFSR2=0x4000_110C, PC_AFSR2=0x4000_120C
PD_AFSR2=0x4000_130C, PE_AFSR2=0x4000_140C, PF_AFSR2=0x4000_150C

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
AFSB15	AFSB14	AFSB13	AFSB12	AFSB11	AFSB10	AFSB9	AFSB8
0000	0000	0000	0000	0000	0000	0000	0000
RW	RW	RW	RW	RW	RW	RW	RW

4(x-8)+3 4(x-8)	AFSRx	Port n Alternative Function Selection bits, x:8 to 15	
		0000	Alternative Function 0 (AF0)
		0001	Alternative Function 1 (AF1)
		0010	Alternative Function 2 (AF2)
		0011	Alternative Function 3 (AF3)
		0100	Alternative Function 4 (AF4)
		0101	Alternative Function 5 (AF5)
		Others	Reserved

5.3.5 Pn_PUPD: port n pull-up/down resistor selection register

Each pin of the ports has on-chip pull-up/down resistor which can be configured by the Pn_PUPD registers.

They are 32-bit registers with 32/16/8-bit access (n = A, B, C, D, E and F).

PA_PUPD=0x4000_1010, PB_PUPD=0x4000_1110, PC_PUPD=0x4000_1210
PD_PUPD=0x4000_1310, PE_PUPD=0x4000_1410, PF_PUPD=0x4000_1510

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
PUPD15	PUPD14	PUPD13	PUPD12	PUPD11	PUPD10	PUPD9	PUPD8	PUPD7	PUPD6	PUPD5	PUPD4	PUPD3	PUPD2	PUPD1	PUPD0
00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

2x+1 2x	PUPDx	Port n Pull-up/down Resistor Selection bits, x:0 to 15	
		00	Disable pull-up/down resistor
		01	Enable pull-up resistor
		10	Enable pull-down resistor
		11	Analog input (ADC/OSC)

NOTE: For exception, the reset value of PB_PUPD, PD_PUPD, PE_PUPD, PF_PUPD register is 0x0000_0040, 0x0000_0005, 0x0100_0000, 0x0000_0005 respectively.

5.3.6 Pn_INDR: port n input data register

Each pin level status can be read in the Pn_INDR registers. Even if a pin is alternative mode except analog mode and output in alternative mode, the pin level can be detected in the Pn_INDR registers.

They are 32-bit registers with 32/16/8-bit access (n = A, B, C, D, E and F).

PA_INDR=0x4000_1014, PB_INDR=0x4000_1114, PC_INDR=0x4000_1214
PD_INDR=0x4000_1314, PE_INDR=0x4000_1414, PF_INDR=0x4000_1514

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		INDR15	INDR14	INDR13	INDR12	INDR11	INDR10	INDR9	INDR8	INDR7	INDR6	INDR5	INDR4	INDR3	INDR2	INDR1	INDR0
-		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
-		RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

x	INDRx	Port n Input Data bit, x:0 to 15

5.3.7 Pn_OUTDR: port n output data register

The Pn_OUTDR define output level of a pin when the pin is set as output and GPIO mode.

They are 32-bit registers with 32/16/8-bit access (n = A, B, C, D, E and F).

PA_OUTDR=0x4000_1018, PB_OUTDR=0x4000_1118, PC_OUTDR=0x4000_1218
PD_OUTDR=0x4000_1318, PE_OUTDR=0x4000_1418, PF_OUTDR=0x4000_1518

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		OUTDR15	OUTDR14	OUTDR13	OUTDR12	OUTDR11	OUTDR10	OUTDR9	OUTDR8	OUTDR7	OUTDR6	OUTDR5	OUTDR4	OUTDR3	OUTDR2	OUTDR1	OUTDR0
-		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

x	OUTDRx	Port n Output Data bit, x:0 to 15 The OUTDR bits can be individually set/cleared by writing to the Pn_BSR/Pn_BCR register

5.3.8 Pn_BSR: port n output bit set register

The Pn_BSR control each bit of Pn_OUTDR registers. Writing '1' into the specific bit field will set a corresponding bit of the Pn_OUTDR to '1'. Writing '0' has no effect.

They are 32-bit registers with 32/16/8-bit access (n = A, B, C, D, E and F).

PA_BSR=0x4000_101C, PB_BSR=0x4000_111C, PC_BSR=0x4000_121C
PD_BSR=0x4000_131C, PE_BSR=0x4000_141C, PF_BSR=0x4000_151C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		BSR15	BSR14	BSR13	BSR12	BSR11	BSR10	BSR9	BSR8	BSR7	BSR6	BSR5	BSR4	BSR3	BSR2	BSR1	BSR0
-		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-		WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO

x	BSRx	Port n Output Set bit, x: 0 to 15. These bits are always read to 0x00	
		0	No effect
		1	Set the corresponding OUTDRx bit (automatically cleared to 0)

5.3.9 Pn_BCR: port n output bit clear register

The Pn_BCR registers control each bit of the Pn_OUTDR registers. Writing '1' into the specific bit field will set a corresponding bit of the Pn_OUTDR to '0'. Writing '0' has no effect.

They are 32-bit registers with 32/16/8-bit access (n = A, B, C, D, E and F).

PA_BCR=0x4000_1020, PB_BCR=0x4000_1120, PC_BCR=0x4000_1220
PD_BCR=0x4000_1320, PE_BCR=0x4000_1420, PF_BCR=0x4000_1520

3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6																
Reserved																BCR15	BCR14	BCR13	BCR12	BCR11	BCR10	BCR9	BCR8	BCR7	BCR6	BCR5	BCR4	BCR3	BCR2	BCR1	BCR0
-																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-																WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO

x	BCRx	Port n Output Clear bit, x: 0 to 15. These bits are always read to 0x00	
		0	No effect
		1	Clear the corresponding OUTDRx bit (automatically cleared to 0)

5.3.10 Pn_OUTDMSK: port n output data mask register

The Pn_OUTDMSK registers protect each bit of the Pn_OUTDR registers. Writing '1' into the specific bit field will protect a corresponding bit of the Pn_OUTDR. Writing '0' is unmasked.

They are 32-bit registers with 32/16/8-bit access (n = A, B, C, D, E and F).

PA_OUTDMSK=0x4000_1024, PB_OUTDMSK=0x4000_1124, PC_OUTDMSK=0x4000_1224
PD_OUTDMSK=0x4000_1324, PE_OUTDMSK=0x4000_1424, PF_OUTDMSK=0x4000_1524

3	3	2	2	2	2	2	2	2	2	2	2	1	1	1	1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6																
Reserved																OUTDMSK15	OUTDMSK14	OUTDMSK13	OUTDMSK12	OUTDMSK11	OUTDMSK10	OUTDMSK9	OUTDMSK8	OUTDMSK7	OUTDMSK6	OUTDMSK5	OUTDMSK4	OUTDMSK3	OUTDMSK2	OUTDMSK1	OUTDMSK0
-																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-																RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

x	OUTDMSKx	Port n Output Data Mask bit, x: 0 to 15.	
		0	Unmask. The corresponding OUTDR bit can be changed.
		1	Mask. The corresponding OUTDRx bit is protected.

5.3.11 Pn_DBCR: port n debounce control register

The Pn_DBCR are 32-bit registers with 32/16/8-bit access (n = A, B, C, D, E and F).

PA_DBCR=0x4000_1028, PB_DBCR=0x4000_1128, PC_DBCR=0x4000_1228
PD_DBCR=0x4000_1328, PE_DBCR=0x4000_1428, PF_DBCR=0x4000_1528

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		DBEN15	DBEN14	DBEN13	DBEN12	DBEN11	DBEN10	DBEN9	DBEN8	DBEN7	DBEN6	DBEN5	DBEN4	DBEN3	DBEN2	DBEN1	DBEN0
-		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

x	DBENx	Port n Debounce Enable bit, x: 0 to 15. Port debounce length = selected debounce clock period * (4 to 5)	
		0	Disable debounce filter
		1	Enable debounce filter

NOTES:

1. If a level is not detected on an enabled pin three or more times in a row at the sampling clock, the signal is eliminated as noise.
2. The port debounce should be disabled before Power Down mode.

5.3.12 Pn_IER: port n interrupt enable register

The Pn_IER registers can configure the interrupt mode (n = A, B, C, D, E and F).

PA_IER=0x4000_102C, PB_IER=0x4000_112C, PC_IER=0x4000_122C
PD_IER=0x4000_132C, PE_IER=0x4000_142C, PF_IER=0x4000_152C

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
PIE15	PIE14	PIE13	PIE12	PIE11	PIE10	PIE9	PIE8	PIE7	PIE6	PIE5	PIE4	PIE3	PIE2	PIE1	PIE0
00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

2x+1 2x	PIEx	Port n Pin interrupt Enable Selection bits, x:0 to 15	
		00	Disable Interrupt
		01	Enable interrupt as level trigger mode
		10	Reserved
		11	Enable interrupt as edge trigger mode

5.3.13 Pn_ISR: port n interrupt status register

When an interrupt is delivered to the CPU, the interrupt status can be detected by reading the Pn_ISR registers. The Pn_ISR registers will report a source pin of the interrupt and a type of the interrupt (n = A, B, C, D, E and F).

PA_ISR=0x4000_1030, PB_ISR=0x4000_1130, PC_ISR=0x4000_1230
PD_ISR=0x4000_1330, PE_ISR=0x4000_1430, PF_ISR=0x4000_1530

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
PIS15	PIS14	PIS13	PIS12	PIS11	PIS10	PIS9	PIS8	PIS7	PIS6	PIS5	PIS4	PIS3	PIS2	PIS1	PIS0
00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

2x+1 2x	PISx	Port n Pin interrupt Status bits, x:0 to 15	
		00	No interrupt event
		01	Low level interrupt or Falling edge interrupt event is present.
		10	High level interrupt or Rising edge interrupt event is present.
		11	Both of rising and falling interrupt event is present in edge trigger interrupt mode. Not available in level trigger interrupt mode.

5.3.14 Pn_ICR: port n interrupt control register

The Pn_ICR control interrupt mode of port pins (n = A, B, C, D, E and F).

PA_ICR=0x4000_1034, PB_ICR=0x4000_1134, PC_ICR=0x4000_1234
PD_ICR=0x4000_1334, PE_ICR=0x4000_1434, PF_ICR=0x4000_1534

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
PIC15	PIC14	PIC13	PIC12	PIC11	PIC10	PIC9	PIC8	PIC7	PIC6	PIC5	PIC4	PIC3	PIC2	PIC1	PIC0
00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

2x+1 2x	PICx	Port n Pin interrupt Control bits, x:0 to 15	
		00	Prohibit external interrupt
		01	Low level interrupt or Falling edge interrupt mode
		10	High level interrupt or rising edge interrupt mode
		11	Both of rising and falling edge interrupt mode Not support for level trigger interrupt mode.

5.3.15 PCU_PORTEN: port access enable

The PCU_PORTEN enables the register writing permission of all PCU registers.

PCU_PORTEN=0x4000_1FF0

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="24">Reserved</td><td colspan="8">PORTEN</td></tr>
<tr><td colspan="24">-</td><td colspan="8">--</td></tr>
<tr><td colspan="24">-</td><td colspan="8">WO</td></tr>
</table>

7 0	PORTEN	Writing the sequence of 0x15 and 0x51 in this register enables writing to PCU registers, and writing other values protects all PCU registers from writing.

NOTE: Refer to the followings to use PORTEN:

```
PORTEN=0x15; PORTEN=0x51;      // enable PORTEN
     …                         // set Pn_MOD, Pn_TYP, Pn_AFSR1, 2,
Pn_PUPD. Pn_DBCR, Pn_IER, Pn_ICR
PORTEN=0;                      // disable PORTEN
```

5.4 Functional description

If an input function of a certain I/O port is used by Pin Control Register, an output function of the I/O port is disabled. Function of each port can be different in accordance with an Alternative Function Selection Register.

Input Data Register captures current data of the I/O pin or debounced input data at every GPIO clock cycle.

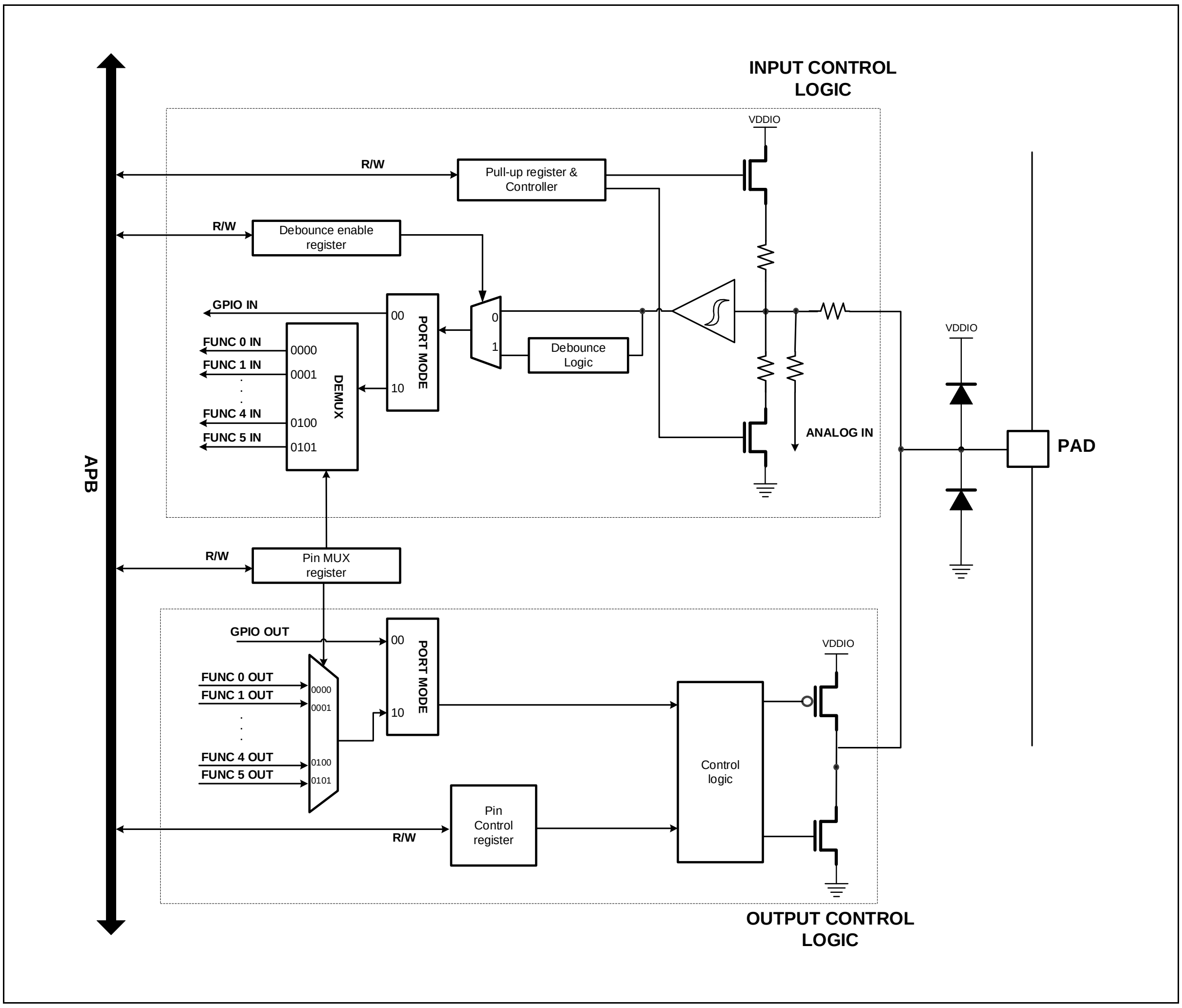


Figure 27. Port Diagram

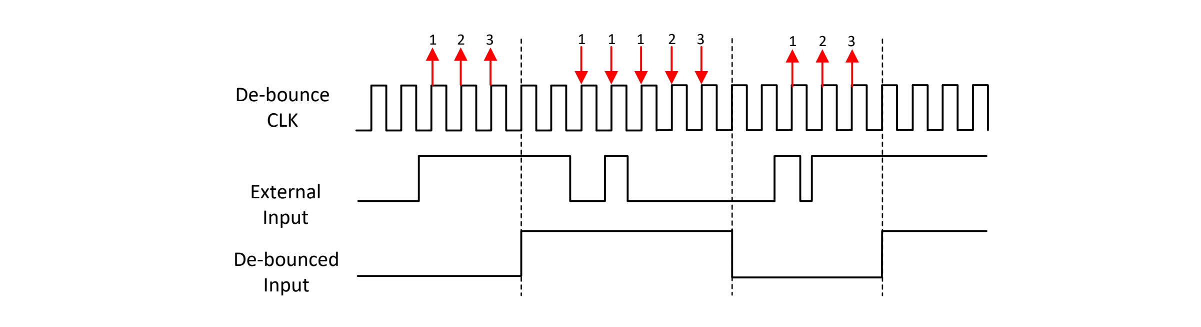


Figure 28. Debounce Function Timing Diagram of External Input

- When configured as output, the value written to the GPIO Output Data Register is output on the I/O Pin.
- When setting the Bit Set Register, GPIO Output Data Register set the high.
- When setting the Bit Clr Register, GPIO Output Data Register set the Low.
- The Input Data Register captures the data present on the I/O pin or Debounced input data at every GPIO Clock cycle.

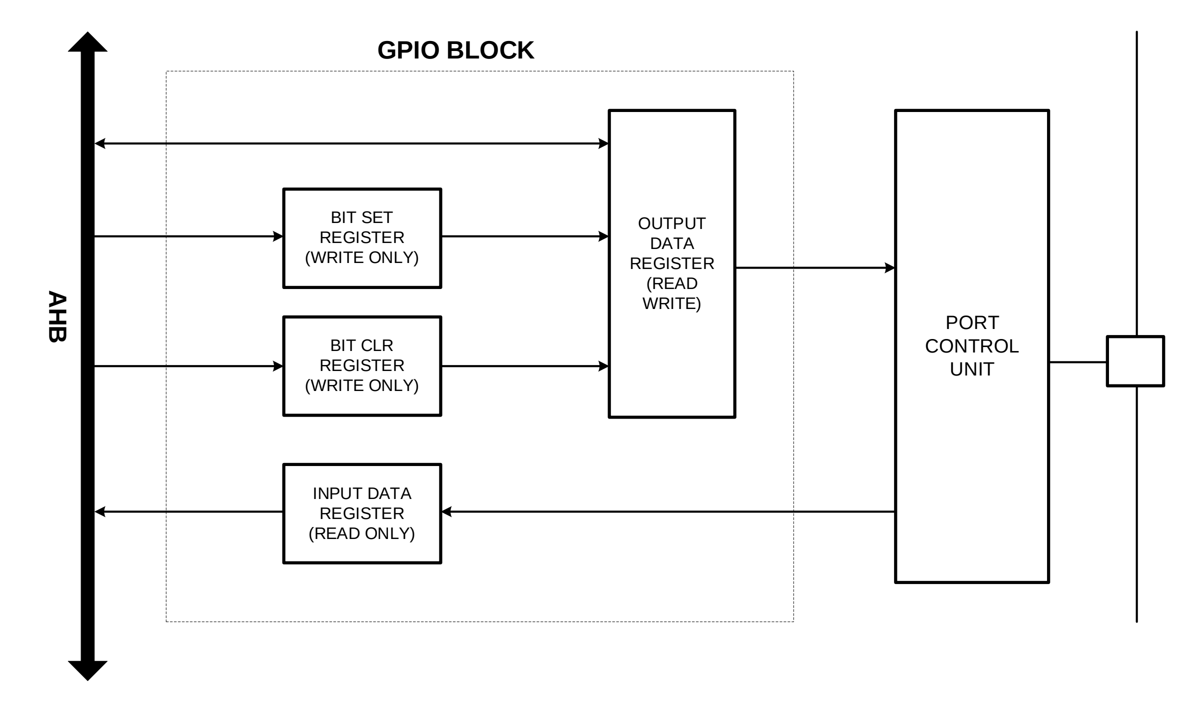

GPIO BLOCK
AHB
BIT SET REGISTER (WRITE ONLY)
BIT CLR REGISTER (WRITE ONLY)
INPUT DATA REGISTER (READ ONLY)
OUTPUT DATA REGISTER (READ WRITE)
PORT CONTROL UNIT

Figure 29. GPIO Diagram

5.4.1 External Interrupt

Each pin of the A31T214/216 can be an external interrupt source. In this case, both of edge trigger interrupt and level trigger interrupt are supported. It is recommended to enable debounce settings in the PCU block to reinforce the immunity of external input glitch noise. When Debounce is enabled, External interrupt occurs when the input signal is maintained for 4 to 5 debounce clocks. When debounce is disabled, an interrupt request occurs as soon as the input signal is received. External Interrupt trigger level is the same as VIL for falling edge or low level, and VIH for rising edge or high level.

Refer to Figure 25. I/O Port Block Diagram (General I/O Pins), Figure 28. Debounce Function Timing

Diagram of External Input, and Figure 136. Timing Diagram of External Input AC Characteristics Definitions.

Registers for External Interrupt usage :
- Pn_IER(port n interrupt enable register) : To set for External Interrupt Enable or Disable for each pin.
- Pn_ICR(port n interrupt control register) : To set for level or edge interrupt mode selection.
- Pn_DBCR(port n debounce control register) : To set for debounce filter usage.
- Pn_ISR(port n interrupt status register) : To monitor source pin or type of interrupt request.

6 Flash memory controller

Flash memory controller is an internal flash memory interface controller, and includes following features as shown below:

- 128KB and 256KB Flash code memory
- Programmable wait control (0 to 5)
- Read protection support
- Self-Program support
- User option area : 3-page (each 512 Bytes)
- Erase, Program in user mode

Table 20. Flash Memory Controller Features

Item	Description	
Size	128KB	256KB
Start address	0x0000_0000	0x0000_0000
End address	0x0002_0000	0x0004_0000
Page size	512-byte	512-byte
Total page count	256 pages	512 pages
PGM unit	32-bit (1-word)	32-bit (1-word)
Erase unit	512-byte/ 1KB/ 4KB/ bulk	512-byte/ 1KB/ 4KB/ bulk

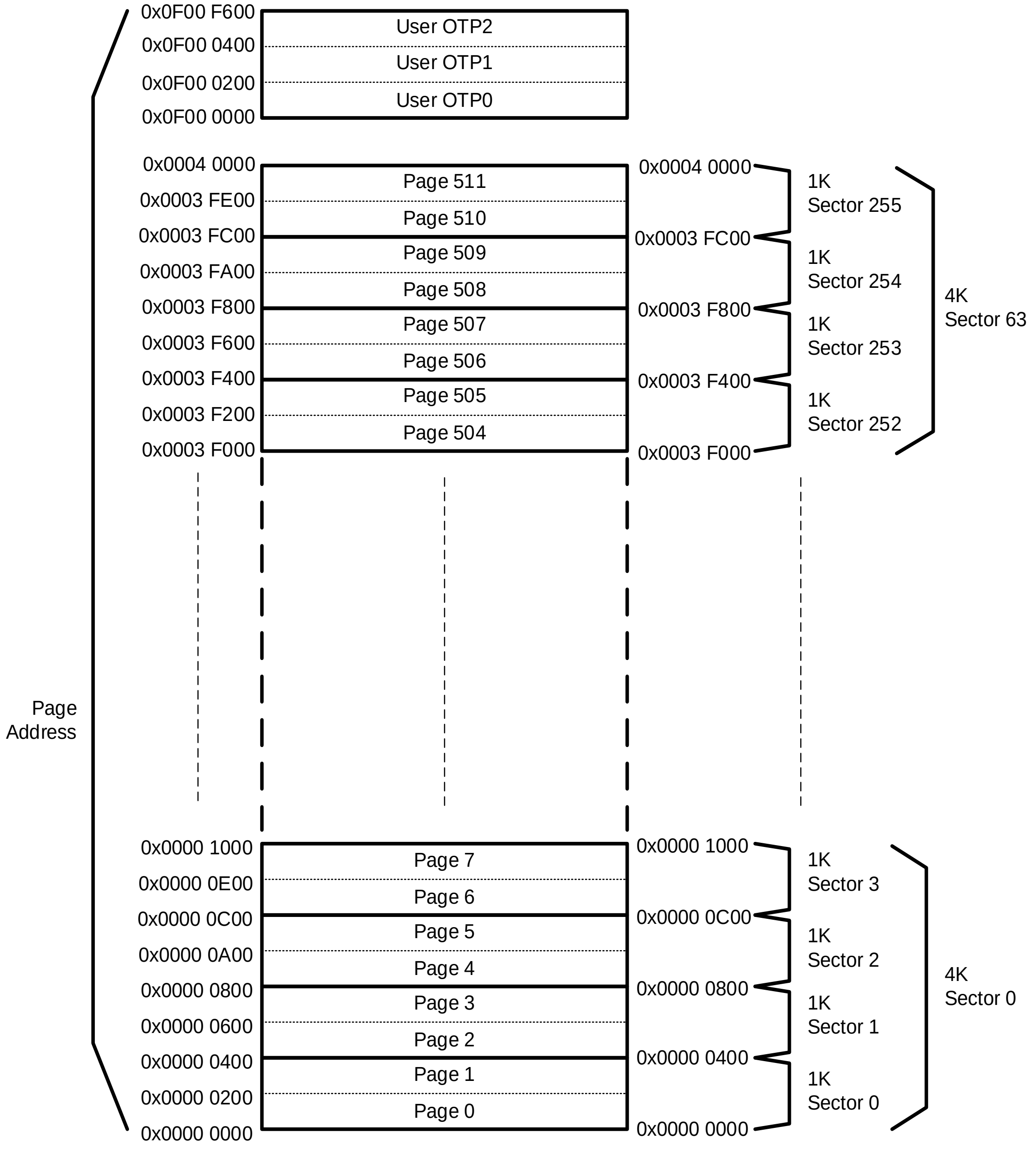


Figure 30. Flash Memory Map (256KB Code Flash)

6.1 Registers

Table 21 and Table 22 show base address and register map of flash memory controller.

Table 21. Base Address of Flash Memory Controller

Name	Base address
Flash controller	0x4000_0100

Table 22. FMC Register Map

Name	Offset	Type	Description	Reset value	Reference
FMC_MR	0x0004	R/W	Flash Memory Mode Select Register	0x0100_0000	6.1.1
FMC_CR	0x0008	R/W	Flash Memory Control Register	0x0000_0000	6.1.2
FMC_AR	0x000C	R/W	Flash Memory Address Register	0x0000_0000	6.1.3
FMC_DR	0x0010	R/W	Flash Memory Data Register	0x0000_0000	6.1.4
FMC_BUSY	0x0018	R/W	Flash Write Busy Status Register	0x0000_0000	6.1.5
FMC_CRC	0x0020	R/W	Flash CRC16 check value	0x0000_FFFF	6.1.6
FMC_CFG	0x0030	R/W	Flash Memory Configuration Register	0x0000_8200	6.1.7
FMC_WPROT	0x0034	R/W	Write Protection Register	0xFFFF_FFFF	6.1.8
FMC_LOCK	0x003C	R/W	Flash LOCK Register	0x0000_00FF	6.1.9

6.1.1 FMC_MR: flash memory mode register

The FMC_MR is an internal flash memory mode register. This is a 32-bit register.

FMC_MR=0x4000_0104

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								ACODE							
-																								0x00							
-																								RW							

7 0	ACODE	5A → A5	Flash mode entry
		A5 → 5A	Trim mode entry
		81 → 28	AMBA mode entry
		66 → 99	PROT mode entry

6.1.2 FMC_CR: flash memory control register

The FMC_CR is an internal flash memory control register.

FMC_CR=0x4000_0108

31 30 29 28 27 26 25 24	23	22 21 20 19 18 17 16 15 14 13 12 11 10 9	8	7	6	5	4	3	2	1	0
Reserved	SELFPGM	Reserved	BBLOCK	MAS	SECT4K	SECT1K	PMODE	WADCK	PGM	ERS	HVEN
-	0	-	0	0	0	0	0	0	0	0	0
-	RW	-	RW	RW	RW	RW	RW	RW	RW	RW	RW

23	SELFPGM		When this bit is set ("1"), PGM/ERS/HVEN will be cleared automatically after WRBUSY falling edge. It also enable CPU wait control when HVEN bit is set(1) (start of program or erase operation) It also affects to PMODE bit operation.
8	BBLOCK	0	Boot Block (1st 4KB) not protected from Mass(Bulk) Erase
		1	Boot Block (1st 4KB) protection enable from Mass(bulk) erase
7	MAS	0	Mass (bulk) erase disable
		1	Mass (bulk) erase enable.
6	SECT4K	0	Sector 4K erase disable
		1	Sector 4K erase enable
5	SECT1K	0	Sector 1K erase disable
		1	Sector 1K erase enable
4	PMODE	0	Normal mode
		1	PMODE enable(Flash Address path is connected with FMAR) PMODE only valid when SELFPGM bit was not set(when SELFPGM = 0)
3	WADCK	0	Program/Erase address data latch clock disable
		1	Program/Erase address data latch clock enable, this bit assert for one system clock period so user cannot read
2	PGM	0	Program mode disable
		1	Program mode enable
1	ERS	0	Erase mode disable
		1	Erase mode enable
0	HVEN	0	High Voltage cycle disable
		1	High Voltage cycle enable (start program or erase cycle) User must set and clear in PMODE. In SELFPGM mode, user must set HVEN then HVEN will be cleared automatically after WRBUSY goes low.

6.1.3 FMC_AR: flash memory address register

The FMC_AR is an internal flash memory program/ erase/ address register.

FMC_AR=0x4000_010C

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="18">Reserved</td><td colspan="14">FADDR</td></tr>
<tr><td colspan="18">-</td><td colspan="14">0x0000</td></tr>
<tr><td colspan="18">-</td><td colspan="14">RW</td></tr>
</table>

13 0	FADDR	Word (32-bit) base address Auto Incremental after WADCK trigger (after latching of target address).

6.1.4 FMC_DR: flash data input register

The FMC_DR is an internal flash memory data input register.

FMC_DR=0x4000_0110

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">FDATA</td></tr>
<tr><td colspan="32">0x00000000</td></tr>
<tr><td colspan="32">RW</td></tr>
</table>

31 0	FDATA	Word size(32-bit)

6.1.5 FMC_BUSY: flash write busy status register

The FMC_BUSY is a flash write (program/erase) busy status monitor register. This register is a 1-bit read only register.

FMC_BUSY=0x4000_0118

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="31">Reserved</td><td>WRBUSY</td></tr>
<tr><td colspan="31">-</td><td>0</td></tr>
<tr><td colspan="31">-</td><td>RO</td></tr>
</table>

0	WRBUSY	Write Busy status bit FLBUSY bit goes high after set HVEN bit (in CTRL register). FLBUSY bit goes low when WRBUSY becomes low after program (or erase) complete.

6.1.6 FMC_CRC: flash CRC check register

The FMC_CRC is an internal flash memory burst mode channel selection register.

- 16-bit read only register [15:0], which enabled by CRCEN bit of CFG register
- At least 16-word read to get a CRC value

FMC_CRC=0x4000_0120

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Reserved	CRC-CCITT
-	0xFFFF
-	RO

15 0	CRC- CCITT	CRC- CCITT check value read register polynomial: (1 + x5 + x12 + x16) data width: 32 (the first serial bit is D[31])

6.1.7 FMC_CFG: flash memory configuration register

The FMC_CFG is an internal flash memory Configuration register.

FMC_CFG=0x4000_0130

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11	10 9 8	7	6	5 4 3 2 1 0
WTIDKY	Reserved	WAIT	CRCINIT	CRCEN	Reserved
0x0000	-	010	0	0	-
WO	-	RW	RW	RW	-

31 16	WTIDKY		Write Identification Key. On writes, write 0x7858 to these bits, otherwise the write is ignored.
10 8	WAIT		This bits only be written in AMBA mode and MSB 16-bit (bit [31:16]) must be 0x7858
		000	WAIT is 000, flash access in 1 cycle (0-wait)
		001	WAIT is 001, flash access in 2 cycles (1-wait)
		010	WAIT is 010, flash access in 3 cycles (2-wait) – default
		011	WAIT is 011, flash access in 4 cycles (3-wait)
		1xx	WAIT is 1xx, flash access in 5 cycles (4-wait)
7	CRCINIT	0	When this bit is set('1'), CRC register will be initialized It should be reset again before read flash to generate CRC16 calculation (Initial value of FMC_CRC is 0xFFFF)
6	CRCEN	0	CRC-CCITT enable CRC value will be calculated at every flash read timing

6.1.8 FMC_WPROT: write protection register

The FMC_WPROT is an internal flash memory write protection register.

FMC_WPROT=0x4000_0134

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
WPROT[31:0]			
0xFFFF_FFFF			
RW			

31 s0	WPROT	Write protection Each 8 KB segments for whole memory address (needs 32 bits for 256KB flash)

NOTES:

1. Each bit individually protects the 8KB area (Bit0: 0 to 0x1FFF, Bit1: 0x2000 to 0x3FFF).
2. The FM_WPROT register can only be modified in PROT (FM_MR = 66-> 99) mode.

6.1.9 FMC_LOCK: flash lock register

The FMC_LOCK is an internal flash memory read protection register.

FMC_LOCK=0x4000_013C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved			RPROT
-			0x00FF
-			RW

7 0	RPROT	Read protection 0x0000_00FF is Default. Any other value will lock flash(enable read protection) In user mode, 0xFF cannot be written To unlock, user must erase LOCK area of Flash next to MAS(bulk) erase - 1st MAS(bulk) erase and then erase LOCK area - To unlock the flash, pin reset or power on reset required - When read protection occurs, Registers are shown as 0xAA55AA55.

NOTE: The FM_WPROT register can only be modified in PROT. (FM_MR = 66-> 99) mode.

6.2 Functional description

6.2.1 Flash erase and program examples

Basic steps of flash memory programming consist of the followings. Minimum Program or Erase unit is a Page, and 512-byte becomes a page.

- Bulk erase
- Sector(4KB) erase
- Page program
- Self page erase
- Self page program

For all of erase operations, pre-program operation is required to prevent over erase of flash memory cells. In addition, a user must enable 32MHz internal oscillator first to erase or program flash.

Bulk Erase example

1. Clear all write protection bits.

   Write 0x66 and then 0x99 into the FMC_MR register to access the FMC_WPROT register.

   Write 0x00000000 into the FMC_WPROT register, and clear the FMC_MR register to 0x00.
2. Set the FMC_CR register to access mode.

   Write 0x5A and then 0xA5 into the FMC_MR register.
3. Set the PMODE, MAS (bulk), ERS (erase) bits of the FMC_CR register.
4. Set the WADCK bit of the FMC_CR register (write 1) to latch control bits.

   Don't set the WADCK bit and the bits mentioned in step 3 (PMODE, MAS, ERS) at the same time.

   The WADCK bit will be cleared automatically, so cannot be read as "1".
5. Set the HVEN (high voltage enable) of the FMC_CR register to start Erase operation.
6. Set until the WRBUSY bit of the FWBUSY register is cleared.

   No IRQ for Flash PMODE operation, S/W must poll this bit.
7. Clear the HVEN bit.
8. Clear the MAS, PMODE, ERS bits of the FMC_CR register.
9. To exit FMC_CR access mode, write 0x00 to the FMC_MR register.

Sector (4KB) Erase example

1. Clear the write protection bit of the target address.

   Write 0x66 and then 0x99 into the FMC_MR register to access the FMC_WPROT register.

   Write 0x0 into the corresponding FMC_WPROT bit, and clear the FMC_MR register to 0x00.
2. Set the FMC_CR register to access mode.

Write 0x5A and then 0xA5 into the FMC_MR register.

3. Set the FADDR for the target address to byte address map (but least 2 bits will be ignored).

   The target address must be aligned by 4KB space.

4. Set the PMODE, SECT4K, ERS (erase) bits of the FMC_CR register.

5. Set the WADCK bit of FMC_CR register (write 1) to latch control bits.

   Don't set the WADCK bit and the bits mentioned in step 4 (PMODE, SECT4K, ERS) at the same time.

   The WADCK will be cleared automatically, so cannot be read as "1".

6. Set the HVEN (high voltage enable) of the FMC_CR register to start Erase operation.

7. Wait until the WRBUSY bit of the FWBUSY register is cleared.

   No IRQ for Flash PMODE operation, S/W must poll this bit.

8. Clear the HVEN bit.

9. Clear the SECT4K, PMODE, ERS bits of the FMC_CR register.

10. To exit FMC_CR access mode, write 0x00 to the FMC_MR register.

Program example

1. Clear the write protection bit of the target address.

   Write 0x66 and then 0x99 into the FMC_MR register to access the FMC_WPROT register.

   Write 0x0 into the corresponding FMC_WPROT bit, and clear the FMC_MR register to 0x00.
2. Set the FMC_CR register to access mode.

   Write 0x5A and then 0xA5 into the FMC_MR register.
3. Set the FADDR for the target address to byte address map (but least 2 bits will be ignored).

   The target address must be aligned by word (32-bit) address space.
4. Write a word (32-bit) Data into the FDATA register.
5. Set the PMODE, PGM (program) bits of the FMC_CR register.
6. Set the WADCK bit of the FMC_CR register (write 1) to latch control/address/data bits.

   Don't set the WADCK bit and the bits mentioned in step 5 (PMODE, PGM) at the same time.

   The WADCK will be cleared automatically, so cannot be read as "1".
7. Set the HVEN (high voltage enable) of the FMC_CR register to start Erase operation.
8. Wait until the WRBUSY bit of the FWBUSY register is cleared.

   No IRQ for Flash PMODE operation, S/W must poll this bit.
9. Clear the HVEN bit, and

   Go to step 4 to write at the next address.

   Go to step 3 to write at the new address.
10. To finish the program, clear the PMODE, PGM bits of the FMC_CR register.
11. To exit FMC_CR access mode, write 0x00 to the FMC_MR register.

Self Page Erase example

1. Clear the write protection bit of the target address.

   Write 0x66 and then 0x99 into the FMC_MR register to access the FMC_WPROT register.

   Write 0x0 into the corresponding FMC_WPROT bit, and clear the FMC_MR register to 0x00.

2. Set the FMC_CR register to access mode.

   Write 0x5A and then 0xA5 into the FMC_MR register.

3. Set the SELFPGM, ERS (erase) bits of the FMC_CR register.

4. Write 0xFFFFFFFF to the target address.

   Address must be aligned to 512 Bytes address space.

5. Flash will stop until Erase is complete.

   CPU will stop when Erase code runs in flash area.

   Erase code runs in SRAM area, flash cannot be accessed until erase is complete.

6. To Erase another page, go to step 4.

7. Clear the SELFPGM, ERS bits of the FMC_CR register.

8. To exit FMC_CR access mode, write 0x00 to the FMC_MR register.

Self Page Program example

1. Clear the write protection bit of the target address.

   Write 0x66 and then 0x99 into the FMC_MR register to access the FMC_WPROT register.

   Write 0x0 into the corresponding FMC_WPROT bit, and clear the FMC_MR register to 0x00.

2. Set the FMC_CR register to access mode.

   Write 0x5A and then 0xA5 into the FMC_MR register.

3. Set the SELFPGM, PGM(program) bits of the FMC_CR register.

4. Write 32-bit Data to the target address.

   Address must be aligned to WORD(32-bit) address space.

5. Flash will stop until Program is complete.

6. CPU will stop when Program code runs in flash area.

   Program code runs in SRAM area, flash cannot be accessed until program is complete.

   To Program another word, go to step 4.

7. Clear the SELFPGM, PGM bits of the FMC_CR register.

8. To exit FMC_CR access mode, write 0x00 to the FMC_MR register.

7 Direct Memory Access Controller (DMAC)

The direct memory access (DMA) controller is used for high-speed data transfers between peripherals and memories. DMA enables quick data transfers having memory to memory copying or moving of data within memory.

- 4 channels
- Single transfer only
- Support 8/16/32-bit data size
- Support multiple buffer with same size
- Interrupt condition is transferred through a peripheral interrupt.

7.1 Block diagram

In this section, DMAC block diagram is introduced in Figure 31.

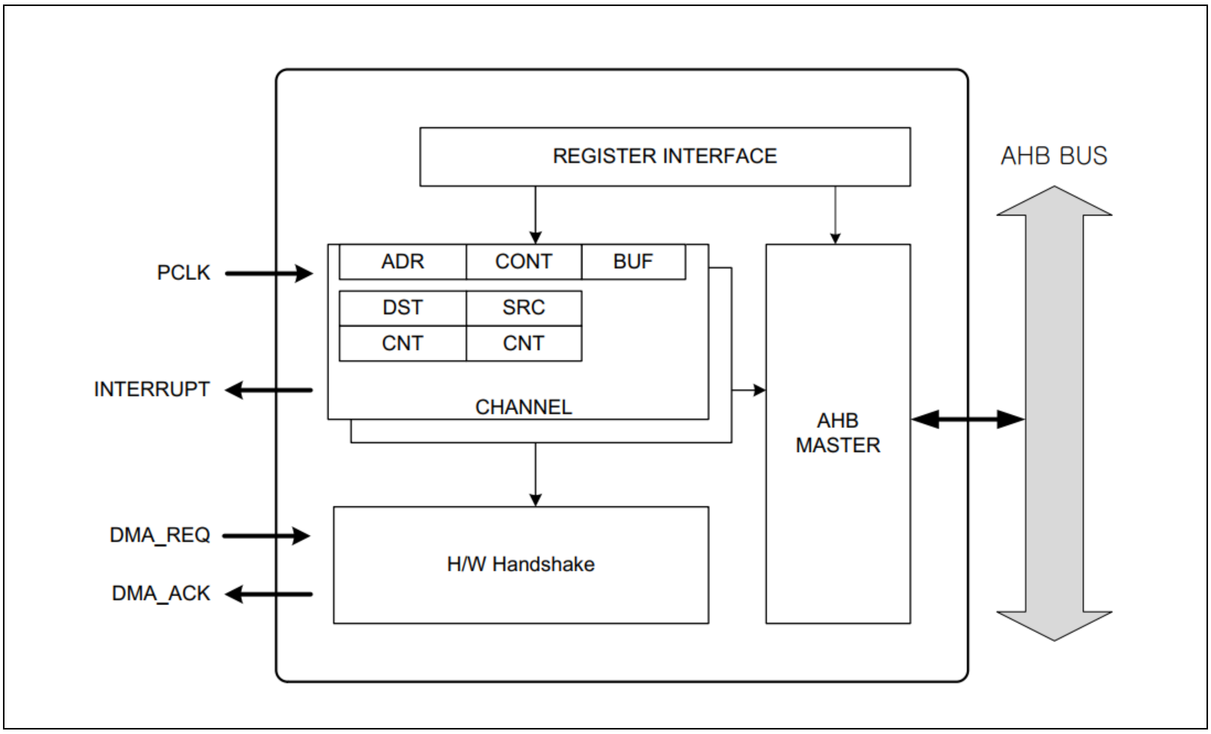


Figure 31. DMAC Block Diagram

7.2 Registers

Table 23 and Table 24 show base address and register map of DMAC.

Table 23. Base Address of DMAC

Name	Base address
DMA0	0x4000_0400
DMA1	0x4000_0410
DMA2	0x4000_0420
DMA3	0x4000_0430

Table 24. DMAC Register Map

Name	Offset	Type	Description	Reset value	Reference
DMAn_CR	0x0000	RW	DMA Channel n Control Register	0x0000_0000	7.2.1
DMAn_SR	0x0004	RW	DMA Channel n Status Register	0x0000_0080	7.2.2
DMAn_PAR	0x0008	RW	DMA Channel n Peripheral Address	0x4000_0000	7.2.3
DMAn_MAR	0x000C	RW	DMA Channel n Memory Address	0x2000_0000	7.2.4

7.2.1 DMAn_CR: DMA controller configuration register

The DMAn_CR are DMA operation control registers, and the register size is 32-bit.

DMA0_CR=0x4000_0400 , DMA1_CR=0x4000_0410
DMA2_CR=0x4000_0420 , DMA3_CR=0x4000_0430

31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2	1	0
Reserved	TRANSCNT	Reserved	PERISEL	Reserved	SIZE	DIR	Reserved
-	0x000	-	0000	-	00	0	-
-	RW	-	RW	-	RW	RW	-

Bits	Field	Value	Description
27 16	TRANSCNT		Number of DMA transfer remained Required transfer number should be written before enable DMA transfer.
		0	DMA transfer is done.
		N	N transfers are remained
11 8	PERISEL		Peripheral selection
		N	Associated peripheral selection. Refer to DMA Peripheral connection table
3 2	SIZE		Bus transfer size.
		00	DMA transfer is byte size transfer
		01	DMA transfer is half word size transfer
		10	DMA transfer is word size transfer
		11	Reserved
1	DIR		Select transfer direction.
		0	Transfer direction is from memory to peripheral. (TX)
		1	Transfer direction is from peripheral to memory (RX)

NOTE: A DMA channel will be connected with selected peripheral. Table 25 shows peripheral selection numbers. This PERISEL field should be set with proper number of peripheral which will be connected with DMA interface.

Table 25. DMAC PERISEL Selection

PERISEL[3:0]	Associate peripheral	PERISEL[3:0]	Associate peripheral
0	CHANNEL IDLE	8	USART11 TX
1	UART0 RX	9	SPI20 RX
2	UART0 TX	10	SPI20 TX
3	UART1 RX	11	SPI21 RX
4	UART1 TX	12	SPI21 TX
5	USART10 RX	13	CRC
6	USART10 TX	14	Reserved
7	USART11 RX	15	Reserved

PERISEL cannot have the same value in different channels. If the same PERISEL value is written in more than one channel, proper operation cannot be guaranteed. Unused channel should have CHANNEL IDLE value in PERISEL bit positions.

7.2.2 DMAn_SR: DMA controller status register

The DMAn_SR represent current status of DMA Controller, and enable DMA function. The register size is 8-bit.

DMA0_SR=0x4000_0404 , DMA1_SR=0x4000_0414
DMA2_SR=0x4000_0424 , DMA3_SR=0x4000_0434

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7	6 5 4 3 2 1	0
Reserved	EOT	Reserved	DMAEN
-	1	-	0
-	RO	-	RW

7	EOT	End of transfer.	
		0	Data to be transferred is existing. TRANSCNT shows non zero value
		1	All data is transferred. TRANSCNT shows now 0
0	DMAEN	DMA Enable	
		0	DMA is in stop or hold state
		1	DMA is running or enabled

7.2.3 DMAn_PAR: DMA controller peripheral address register

The DMAn_PAR represent peripheral addresses.

DMA0_PAR=0x4000_0408 , DMA1_PAR=0x4000_0418
DMA2_PAR=0x4000_0428 , DMA3_PAR=0x4000_0438

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Peripheral Base address Offset	PAR
0x4000	0x0000
RO	RW

15 0	PAR	Target Peripheral address of transmit buffer or receive buffer. User must set exact target peripheral buffer address in this field. If DIR is "0" this address is destination address of data transfer. If DIR is "1", this address is source address of data transfer.

7.2.4 DMAn.MAR: DMA controller memory address register

The DMAn.MAR represent the memory addresses.

DMA0_MAR=0x4000_040C , DMA1_MAR=0x4000_041C
DMA2_MAR=0x4000_042C , DMA3_MAR=0x4000_043C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Memory Base address Offset		MAR	
0x2000		0x0000	
RO		RW	

15 0	MAR	Target memory address of data transfer. Address is automatically incremented according to SIZE bits when each transfer is done. If DIR is “0” this address is source address of data transfer. If DIR is “1”, this address is destination address of data transfer.

7.3 Functional description

A DMA controller performs direct memory transfer by sharing the system bus with CPU core. The system bus is shared by two AHB (Advanced High-performance Bus) masters following the round-robin priority strategy. So the DMA controller can share the half of system bandwidth.

The DMA controller can be triggered only by a peripheral request. When a peripheral requests a transfer to the DMA controller, a corresponding channel is activated and the bus is accessed to transfer the requested data from memory to peripheral data buffer or vice versa.

Basic steps to trigger DMAC data transfer consist of following 10 steps:

1. Set both of peripheral address and memory address.
2. Configure DMA operation mode and transfer count.
3. Enable a DMA channel.
4. A DMA request is occurred from the peripheral.
5. DMA activates the channel which was requested.
6. DMA reads data from source address and saves in internal buffer.
7. DMA writes the buffered data to the destination address.
8. Transfer count number is decreased by '1'.
9. When the transfer count is '0', the EOT flag is set and noticed to peripheral to issue the interrupt
10. DMA does not have interrupt sources, and the interrupt related DMA status can be shown from assigned peripheral interrupt.

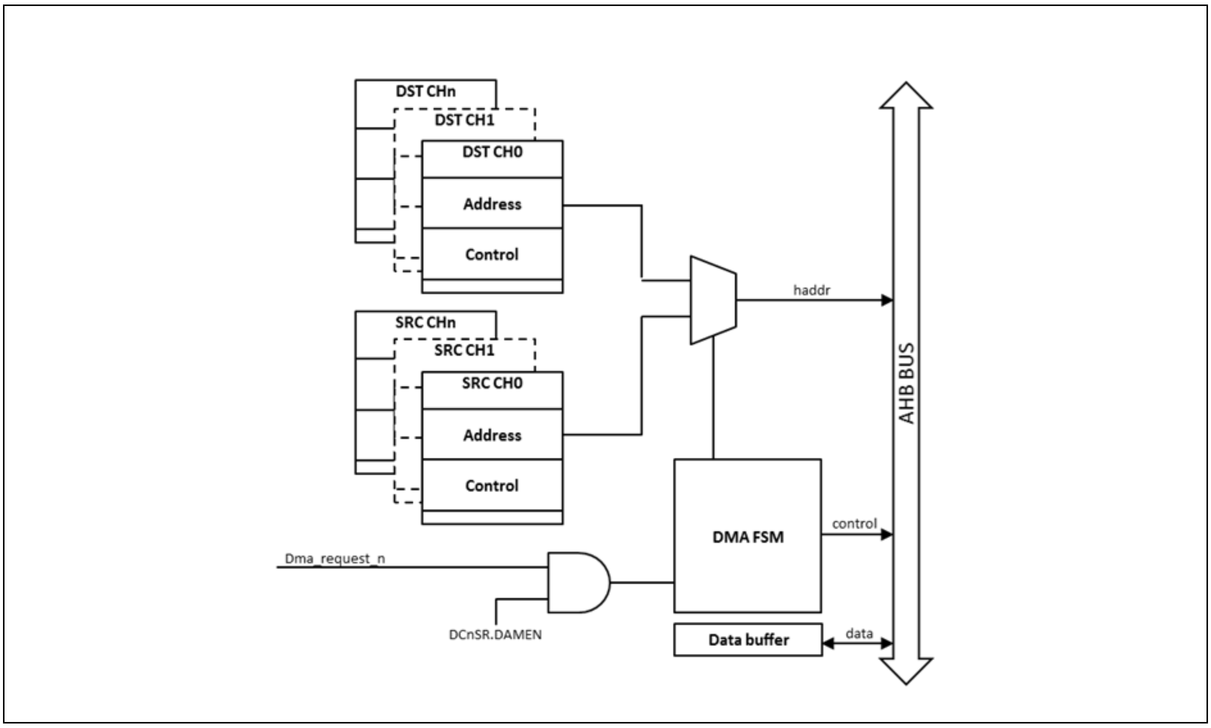


Figure 32. DMAC Functional Block Diagram

7.3.1 DMA operation

A user can start DMA operation by following the procedure introduced below:

1. Set the DMAn_CR registers of DMA.
   - [27:16]: Set a number of data to transfer to DMA.
   - [11:8]: Select a peripheral to connect with DMA.
   - [3:2]: Select a buffer size to transfer.
   - [1]: Set a transfer type between TX and RX.
2. Set the MAR register of DMA (memory address to which DMA accesses).
3. Set the PAR register of DMA (peripheral address to which DMA accesses).
4. Check the EOT flag of the DMA_SR register.
5. Check the DMA flag in the status register of each peripheral.
6. DMA stops.

A sequence of DMAC operation is described in Figure 33.

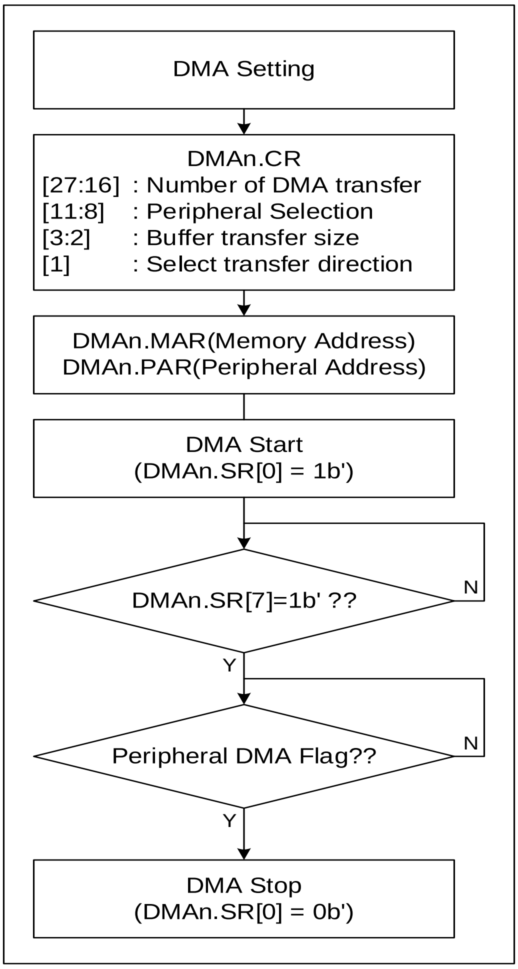

DMA Setting
DMAn.CR
[27:16] : Number of DMA transfer
[11:8] : Peripheral Selection
[3:2] : Buffer transfer size
[1] : Select transfer direction
DMAn.MAR(Memory Address)
DMAn.PAR(Peripheral Address)
DMA Start
(DMAn.SR[0] = 1b')
DMAn.SR[7]=1b' ??
N
Y
Peripheral DMA Flag??
N
Y
DMA Stop
(DMAn.SR[0] = 0b')

Figure 33. DMAC Operation Sequence

Figure 34 shows the functional timing diagram of DMAC. Transfer request from a certain peripheral is pended internally and it will invoke source data read transfer on the AHB bus. The read data from the source address is stored in the internal buffer. Then this data will be transferred to the destination address when the AHB bus is available.

Figure 34 introduces the timing diagram for a DMA transfer from peripheral to memory. There is 4-clock cycle latencies during accessing the peripheral. If the bus is occupied by different bus master, there are amount of bus waiting cycles.

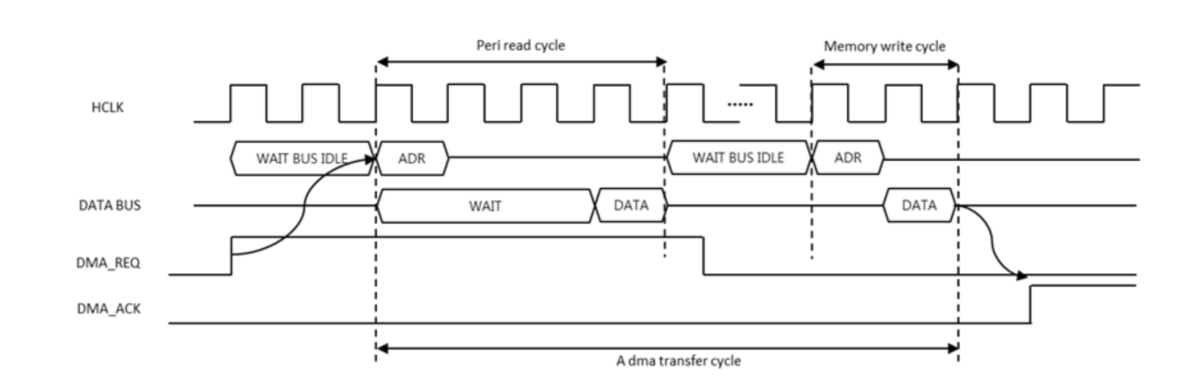


Figure 34. Timing Diagram of DMAC Transfer from Peripheral to Memory

Figure 35 introduces the timing diagram for a DMA transfer from memory to peripheral. There is 4-clock cycle latencies during accessing the peripheral. If the bus is occupied by different bus master, there are amount of bus waiting cycles.

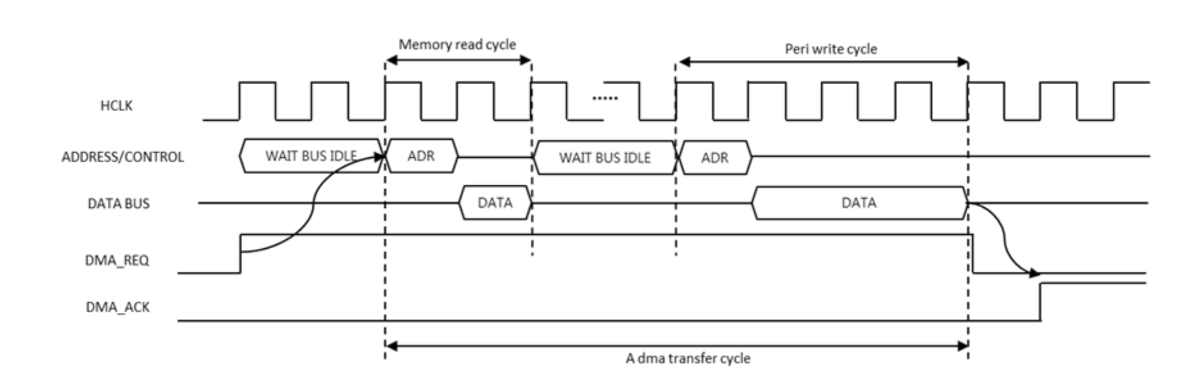


Figure 35. Timing Diagram of DMAC Transfer from Memory to Peripheral

Figure 36 introduces an example of N data transfers with DMA. The DMA transfer is started when DMAn_SR.DMAEN is set. When all the number of transfer is completed, the DMAn_SR.DMAEN register will be cleared.

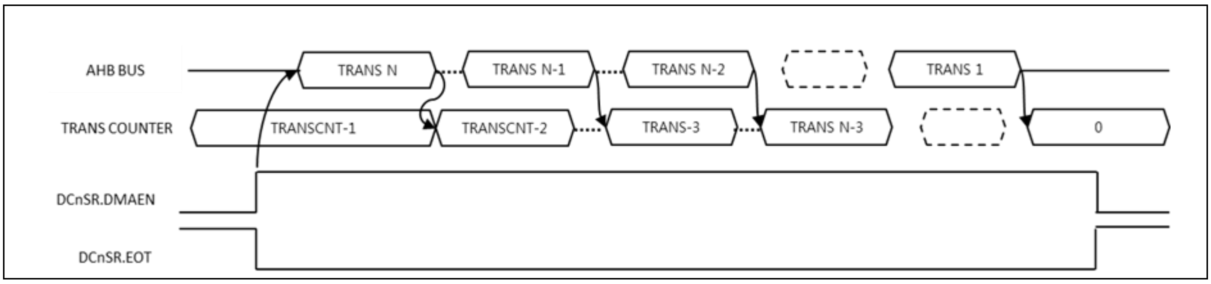


Figure 36. Timing Diagram Example of N DMAC Transfer

8 Watchdog Timer (WDT)

Watchdog Timer (WDT) rapidly detects CPU's malfunction such as endless looping caused by noise, and returns the CPU to the normal state. WDT signal for malfunction detection can be used as either a CPU reset or an interrupt request. When WDT is not being used for malfunction detection, it can be used as a timer generating an interrupt at fixed intervals.

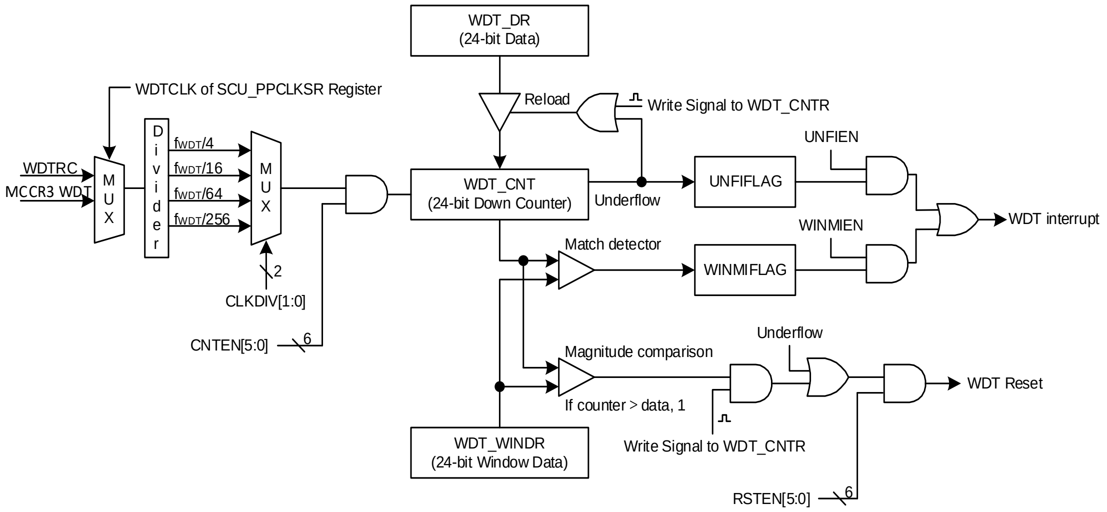
When WDT_CNT value is reached to WDT_WINDR value, a watchdog interrupt can be generated. The underflow time of WDT can be set by WDT_DR. If the underflow occurs, an internal reset is generated. WDT operates on the WDTRC embedded RC oscillator clock.

WDT of A31T214/216 series features followings:

- 24-bit down counter (WDT_CNT)
- Select reset or periodic interrupt
- Count clock selection
- Watchdog overflow output signal
- Counter window function

8.1 WDT block diagram

In this section, WDT block diagram is introduced in Figure 37.



NOTE: If a reload signal is generated, the WDT_DR value is reloaded to WDT_CNT register after 1 clock delay with the clock which is selected by the CLKDIV bits.

Figure 37. WDT Block Diagram

8.2 Registers

Initial watchdog time-out period is set to 2,000-milisecond.

Table 26 and Table 27 show base address and register map of the WDT.

Table 26. Base Address of WDT

Name	Base address
WDT	0x4000_1A00

Table 27. WDT Register Map

Name	Offset	Type	Description	Reset value	Reference
WDT_CR	0x0000	RW	Watch-dog Timer Control Register	0x0000_0000	
WDT_SR	0x0004	RW	Watch-dog Timer Status Register	0x0000_0080	
WDT_DR	0x0008	RW	Watch-dog Timer Data Register	0x0000_3D09	
WDT_CNT	0x000C	RO	Watch-dog Timer Counter Register	0x0000_0FFF	
WDT_WINDR	0x0010	RW	Watch-dog Timer Window Data Register	0x0000_FFFF	
WDT_CNTR	0x0014	WO	Watch-dog Timer Counter Reload Register	0x0000_0000	

8.2.1 WDT_CR: Watchdog Timer control register

The WDT module should be configured properly before running. The WDT module can make reset event or assert interrupt signal to system.

This is a 32-bit register.

WDT_CR=0x4000_1A00

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10	9 8 7 6 5 4	3	2	1 0
WTIDKY	RSTEN	CNTEN	WINMIEN	UNFIEN	CLKDIV
0x0000	000000	000000	0	0	00
WO	RW	RW	RW	RW	RW

31 16	WTIDKY	Write Identification Key.	
		On writes, write 0x5A69 to these bits, otherwise the write is ignored.	
15 10	RSTEN	Watch-dog Timer Reset Enable bits.	
		0x25	Disable watch-dog timer reset.
		Others	Enable watch-dog timer reset.
9 4	CNTEN	Watch-dog Timer Counter Enable bits.	
		0x1A	Disable watch-dog timer counter.
		Others	Enable watch-dog timer counter.
3	WINMIEN	Watch-dog Timer Window Match Interrupt Enable bit.	
		0	Disable window data match interrupt.
		1	Enable window data match interrupt.
2	UNFIEN	Watch-dog Timer Underflow Interrupt Enable bit.	
		0	Disable watch-dog timer underflow interrupt.
		1	Enable watch-dog timer underflow interrupt.
1 0	CLKDIV	Watch-dog Timer Clock Divider bits, The clock which is selected by SCU_PPCLKSR[0].	
		00	fWDT/4
		01	fWDT/16
		10	fWDT/64
		11	fWDT/256

8.2.2 WDT_SR: Watchdog Timer status register

The WDT_SR is a 32-bit register with 32/16/8-bit access.

WDT_SR=0x4000_1A04

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7	6 5 4 3 2	1	0
Reserved	DBGCNTEN	Reserved	WINMIFLAG	UNFIFLAG
-	1	-	0	0
-	RW	-	RW	RW

7	DBGCNTEN	Watch-dog Timer Counter Enable bit When the core is halted in the debug mode.	
		0	The watch-dog timer counter continues even if the core is halted.
		1	The watch-dog timer counter is stopped when the core is halted.
		NOTE: This bit is set to "1b" by POR reset.	
1	WINMIFLAG	Watch-dog Timer Window Match Interrupt Flag bit.	
		0	No request occurred.
		1	Request occurred, This bit is cleared to '0' when write '1'.
0	UNFIFLAG	Watch-dog Timer Underflow Interrupt Flag bit.	
		0	No request occurred.
		1	Request occurred, This bit is cleared to '0' when write '1.

NOTES:
1. Window match flag of WDT
2. Window match flag is recommended for System Clock (fx) ≥ 2 * WDT Clock (WDT)

.

8.2.3 WDT_DR: Watchdog Timer data register

The WDT_DR is used to update WDT_CNT register.

This is a 32-bit register.

WDT_DR=0x4000_1A08

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved	DATA		
-	0x003D09		
-	RW		

23 0	DATA	Watch-dog Timer Data bits. The range is 0x000000 to 0xFFFFFF.
NOTE:	Once any value is written to this data register, the register can't be changed until a system reset.	

8.2.4 WDT_CNT: Watchdog Timer counter register

The WDT_CNT represents the current count value of 32-bit down counter. When the counter value reach to 0, the interrupt or reset will be asserted.

This is a 32-bit register.

WDT_CNT=0x4000_1A0C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved	CNT		
-	0x000FFF		
-	RO		

23 0	CNT	Watch-dog Timer Counter bits.

8.2.5 WDT_WINDR: Watchdog Timer window data register

The WDT_WINDR is used to compare with the WDT_CNT for WINDOW function.

This is a 32-bit register.

WDT_WINDR=0x4000_1A10

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved	WDATA		
-	0x00FFFF		
-	RW		

23 0	WDATA	Watch-dog Timer Data bits. The range is 0x000000 to 0xFFFFFF.
NOTE:	Once any value is written to this data register, the register can't be changed until a system reset.	

8.2.6 WDT_CNTR: Watchdog Timer counter reload register

The WDT_CNTR is used to make reload signal. If reload signal is I, the WDT_DR value is reloaded to the WDT_CNT.

This is a 32-bit register.

WDT_CNTR=0x4000_1A14

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved			CNTR
-			0x00
-			WO

7 0	CNTR	Watch-dog Timer Counter Reload bits.	
		0x6A	Reload the WDTDR value to watch-dog timer counter and re-start. (Automatically cleared to "0x00" after operation)
		Others	No effect

8.3 Functional description

WDT counter can be enabled by CNTEN (WDT_CR[9:4]). Corresponding bit field of the register CNTEN is set with any value other than 0x1A. As WDT activates, a down counter will start counting from loaded value.

If RSTEN (WDT_CR[15:10]) is set with any value other than 0x25, WDT reset would be asserted when the WDT counter value reaches to '0' (underflow event) from WDT_DR value. Before WDT counter reaches to '0', software can write 0x6A to WDT_CNTR register in order to reload WDT counter when the counter value is less than or equal to the value of window data register. WDT reset may be asserted if the reload occurs when counter is greater than window data.

8.3.1 Timing diagram

In this section, WDT interrupt and reset timing diagram is introduced in Figure 38.

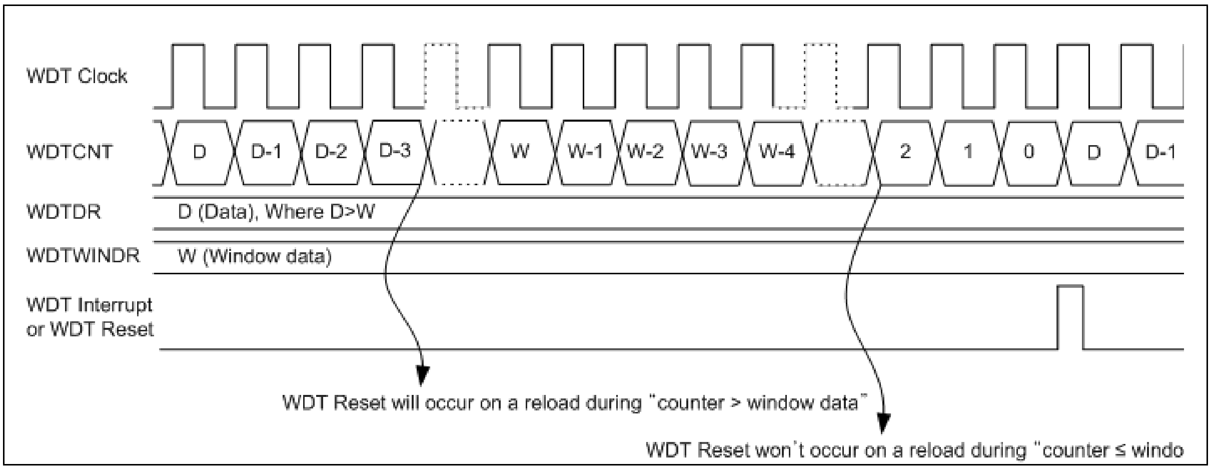

WDT Clock
WDTCNT
D
D-1
D-2
D-3
W
W-1
W-2
W-3
W-4
2
1
0
D
D-1
WDTDR
D (Data), Where D>W
WDTWINDR
W (Window data)
WDT Interrupt
or WDT Reset
WDT Reset will occur on a reload during "counter > window data"
WDT Reset won't occur on a reload during "counter ≤ windo

Figure 38. WDT Interrupt and WDT Reset Timing Diagram

8.3.2 Prescale table

WDT includes a 24-bit down counter with programmable pre-scaler to define different time-out intervals.

Clock sources of WDT can be WDT_RC or PCLK. PCLK can be selected by WDTCLK (SCU_PPCLKSR[0]) which is set to '1', then the WDTCNFIG[2] bit of configure option page 1 is cleared to logic "0b".

To configure a WDT counter as a base clock, user can control 2-bit pre-scaler CLKDIV [1:0] in the WDT_CR register, and the maximum pre-scaled value is "clock source frequency/256". The pre-scaled WDT counter clock frequency values are listed in the following table.

Selectable clock source (31.250kHz to 48MHz) and time-out interval at a single count

Time-out period = (Load Value + 1) * (1/pre-scaled WDT counter clock frequency)

***Time out period (when the Load Value reaches 0, underflow flag is set to ‘1’)**

Table 28. Pre-scaled WDT Counter Clock Frequency

Clock source	WDTCLKIN	WDTCLKIN/4	WDTCLKIN/16	WDTCLKIN/64	WDTCLKIN/256
WDTRC	31.250kHz	7.8125kHz	1.953125kHz	488.28125Hz	122.0703125Hz
MCCR3 WDT	MCCR3 WDT	MCCR3 WDT/4	MCCR3 WDT/16	MCCR3 WDT/64	MCCR3 WDT/256

9 Watch Timer (WT)

Watch Timer (WT) has functions for RTC (Real Time Clock) operation. It is generally used for RTC design. WT consists of a clock source select circuit, a timer counter circuit, an output select circuit and watch timer control registers.

Prior to operate WT, a user needs to determine an input clock source and output interval, and to set WTEN as ‘1’ in watch timer control register (WT_CR). It is able to execute simultaneously or individually. To stop or reset WT, clear the WTEN bit in WT_CR register.

Watch timer counter circuit corporates a 26-bit counter. Low 14 bits of the counter form a binary counter and high 12 bits form an auto reload counter in order to raise resolution. In WTCLR, it can control WT clear and set interval value at write time, and it can read 12-bit WT counter value at read time.

9.1 WT block diagram

As shown in Figure 39, WT of A31T214/216 series has the following blocks:

- 14-bit divider
- 12-bit up-counter
- RTC function

Figure 39 shows a block diagram of the WT.

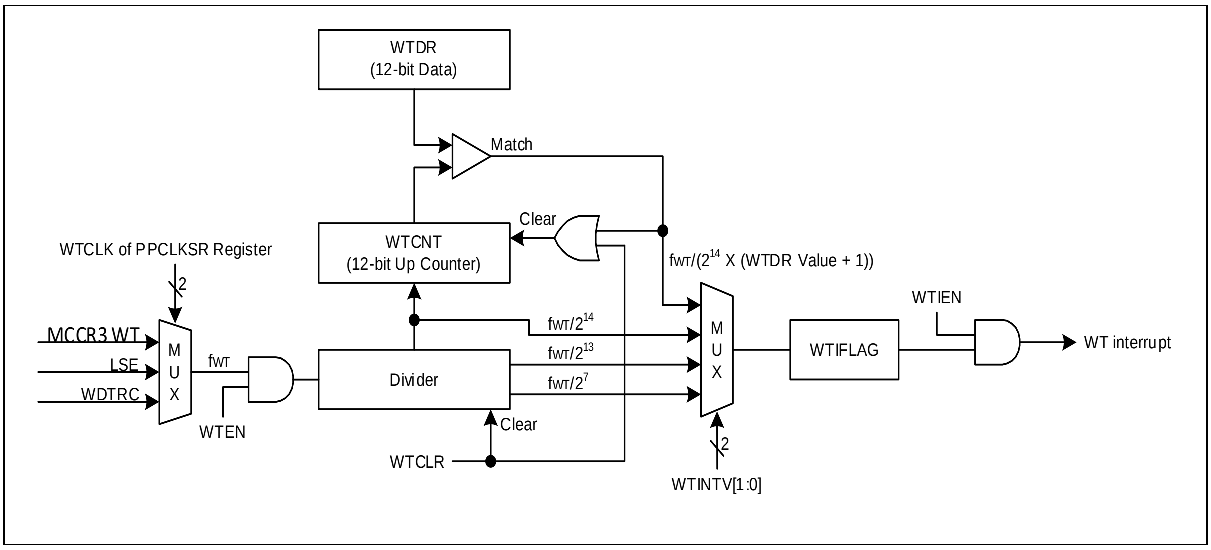


Figure 39. Watch Timer Block Diagram

9.2 Registers

Table 29 and Table 30 show base address and register map of WT.

Table 29. Base Address of WT

Name	Base address
WT	0x4000_2000

Table 30. WT Register Map

Name	Offset	Type	Description	Reset value	Reference
WT_CR	0x0000	RW	Watch Timer Control Register	0x0000_0000	
WT_DR	0x0004	RW	Watch Timer Data Register	0x0000_0FFF	
WT_CNT	0x0008	RO	Watch Timer Counter Register	0x0000_0000	

9.2.1 WT_CR: Watch Timer control register

The WT_CR is a 32-bit register with 32/16/8-bit access.

WT_CR=0x4000_2000

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Reserved			WTEN	Reserved	WTINTV		WTIEN	Reserved	WTIFLAG	WTCLR
-			0	-	00		0	-	0	0
-			RW	-	RW		RW	-	RW	RW

7	WTEN	Watch Timer Operation Enable bit.	
		0	Disable watch timer operation.
		1	Enable watch timer operation.
5 4	WTINTV	Watch Timer Interval Selection bits.	
		00	$fWT/2^7$
		01	$fWT/2^{13}$
		10	$fWT/2^{14}$
		11	$fWT/(2^{14}x(WTDR\ value + 1))$
		NOTE: These bits should be changed during WTEN bit is "0b".	
3	WTIEN	Watch Timer Interrupt Enable bit.	
		0	Disable watch timer interrupt.
		1	Enable watch timer interrupt.
1	WTIFLAG	Watch Timer Interrupt Flag bit.	
		0	No request occurred.
		1	Request occurred, This bit is cleared to '0' when write '1'.
0	WTCLR	Watch Timer Counter and Divider Clear bit.	
		0	No effect.
		1	Clear the counter and divider (Automatically cleared to "0b" after operation)

9.2.2 WT_DR: Watch Timer data register

The WT_DR is a 32-bit register.

WT_DR=0x4000_2004

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				WTDATA											
-																				0xFFF											
-																				RW											

11 0	WTDATA	Watch Timer Data bits. The range is 0x001 to 0xFFF.

9.2.3 WT_CNT: Watch Timer counter register

The WT_CNT is a 32-bit register.

WT_CNT=0x4000_2008

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				CNT											
-																				0x000											
-																				RO											

11 0	CNT	Watch Timer Counter bits.

10 16-bit timer

16-bit timer block comprises 4 channels of 16-bit general purpose timers. Each channel has an independent 16-bit counter and a dedicated prescaler that feeds a counting clock. 16-bit timer supports periodic timer, PWM pulse, one-shot and capture mode. In addition, one more optional free-run timer is provided. Main purpose of 16-bit timer is a periodical tick timer.

16-bit timer of A31T214/216 series features the followings:

- 16-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 12-bit prescaler
- Synchronous start and clear function

Table 31 introduces pins assigned for 16-bit timer.

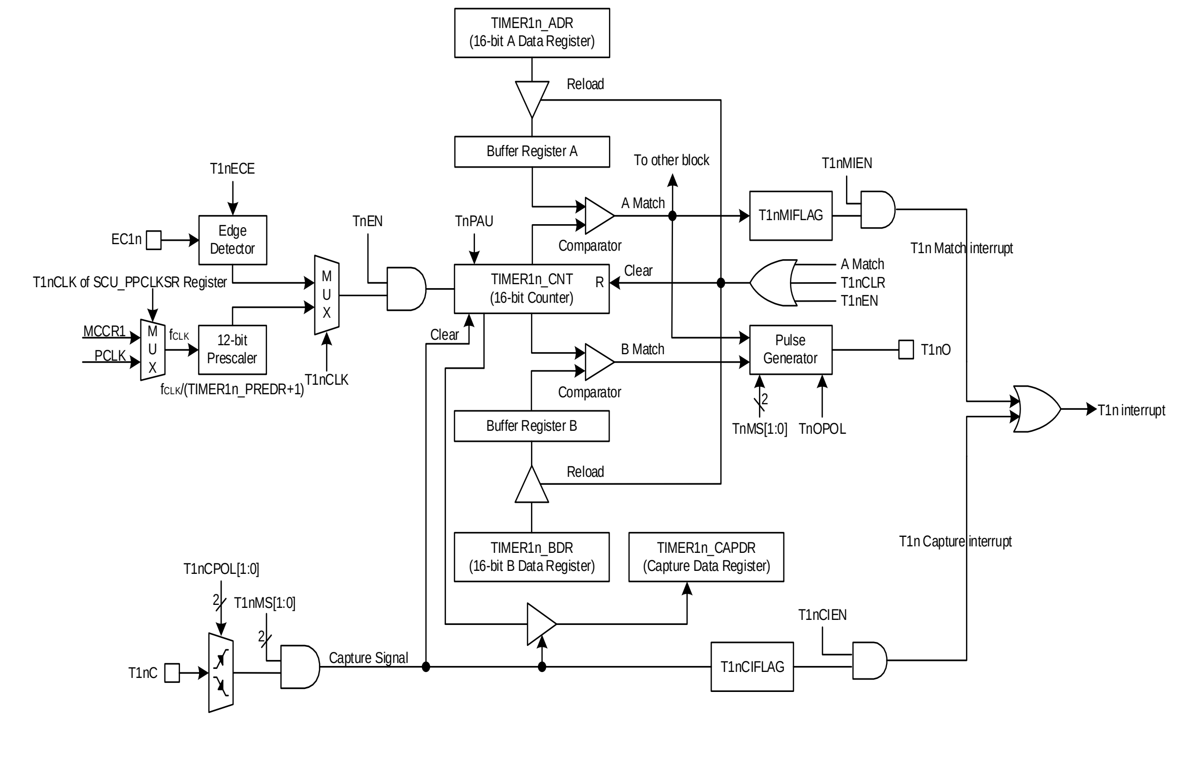
Table 31. Pin Assignment of 16-bit Timer: External Pins

Pin name	Type	Description
EC1n	I	Timer 1n External Clock input
T1nCAP	I	Timer 1n Capture input
T1nOUT	O	Timer 1n Output

NOTE: n = 0, 1, 2, and 3

10.1 16-bit timer block diagram

In this section, 16-bit timer is described in a block diagram in Figure 40.



NOTES:

1. The TnEN is automatically cleared to logic "0" after one pulse is generated at a PPG one-shot mode.
2. After the TnEN bit is set, the counting of TIMERn_CNT may be delayed 2 clocks or more.

Figure 40. 16-bit Timer Block Diagram

10.2 Registers

Table 32 and Table 33 show base address and register map of 16-bit timer.

Table 32. Base Address of 16-bit Timer

Name	Base address
TIMER10	0x4000_2100
TIMER11	0x4000_2200
TIMER12	0x4000_2300
TIMER13	0x4000_2700

Table 33. TIMER 1n Register Map

Name	Offset	Type	Description	Reset value	Reference
TIMER1n_CR	0x0000	RW	Timer/Counter 1n Control Register	0x0000_0000	
TIMER1n_ADR	0x0004	RW	Timer/Counter 1n A Data Register	0x0000_FFFF	
TIMER1n_BDR	0x0008	RW	Timer/Counter 1n B Data Register	0x0000_FFFF	
TIMER1n_CAPDR	0x000C	RO	Timer/Counter 1n Capture Data Register	0x0000_0000	
TIMER1n_PREDR	0x0010	RW	Timer/Counter 1n Prescaler Data Register	0x0000_0FFF	
TIMER1n_CNT	0x0014	RO	Timer/Counter 1n Counter Register	0x0000_0000	

NOTE: n = 0, 1, 2, and 3

10.2.1 TIMER1n_CR: timer/counter 1n control register

Timer module should be configured properly before running. When a target purpose is defined, the timer can be configured in the TIMERn_CR register. After configuring TIMER1n_CR, a user can start or stop the timer function by using TIMERn_CR.

The TIMER1n_CR are 32-bit registers with 32/16/8-bit access. (n = 0, 1, 2, and 3)

TIMER10_CR=0x4000_2100, TIMER11_CR=0x4000_2200
TIMER12_CR=0x4000_2300, TIMER13_CR=0x4000_2700

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13 12	11	10 9	8	7 6	5	4	3	2	1	0
Reserved		TnEN	TnCLK	TnMS	TnECE	Reserved	TnOPOL	TnCPOL	TnMIEN	TnCIEN	TnMIFLAG	TnCIFLAG	TnPAU	TnCLR
-		0	0	00	0	-	0	00	0	0	0	0	0	0
-		RW	RW	RW	RW	-	RW	RW	RW	RW	RW	RW	RW	RW

15	T1nEN	Timer 1n Operation Enable bit.	
		0	Disable timer 1n operation.
		1	Enable timer 1n operation. (Counter clear and start)
14	T1nCLK	Timer 1n Clock Selection bit.	
		0	Select an internal prescaler clock.
		1	Select an external clock.
		NOTE: This bit should be changed during T1nEN bit is "0b".	
13 12	T1nMS	Timer 1n Operation Mode Selection bits.	
		00	Timer/Counter mode. (T1nO: Toggle at A-match)
		01	Capture mode. (The A-match interrupt can occur)
		10	PPG one-shot mode. (T1nOUT: Programmable pulse output)
		11	PPG repeat mode. (T1nOUT: Programmable pulse output)
		NOTE: This bit should be changed during TnEN bit is "0b".	
11	T1nECE	Timer 1n External Clock Edge Selection bit.	
		0	Select falling edge of external clock.
		1	Select rising edge of external clock.
8	T1nOPOL	T1nOUT Polarity Selection bit.	
		0	Start high. (T1nOUT is low level at disable)
		1	Start low. (T1nOUT is high level at disable)
7 6	T1nCPOL	Timer 1n Capture Polarity Selection bits.	
		00	Capture on falling edge.
		01	Capture on rising edge.
		10	Capture on both of falling and rising edge.
		11	Reserved.
5	T1nMIEN	Timer 1n Match Interrupt Enable bit.	
		0	Disable timer 1n match interrupt.
		1	Enable timer 1n match interrupt.
4	T1nCIEN	Timer 1n Capture Interrupt Enable bit.	
		0	Disable timer 1n capture interrupt.
		1	Enable timer 1n capture interrupt.
3	T1nMIFLAG	Timer 1n Match Interrupt Flag bit.	
		0	No request occurred.

		1	Request occurred, This bit is cleared to ‘0’ when write ‘1’.
2	T1nCIFLAG	Timer 1n Capture Interrupt Flag bit.	
		0	No request occurred.
		1	Request occurred, This bit is cleared to ‘0’ when write ‘1’.
1	T1nPAU	Timer 1n Counter Temporary Pause Control bit.	
		0	Continue counting.
		1	Temporary pause.
0	T1nCLR	Timer 1n Counter and Prescaler Clear bit.	
		0	No effect.
		1	Clear timer 1n counter and prescaler. (Automatically cleared to “0b” after operation)

10.2.2 TIMER1n_ADR: timer/counter 1n A data register

The TIMER1n_ADR are 32-bit registers with 32/16/8-bit access. (n = 0, 1, 2, and 3)

TIMER10_ADR=0x4000_2104, TIMER11_ADR =0x4000_2204
TIMER12_ADR =0x4000_2304, TIMER13_ADR =0x4000_2704

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved		ADATA	
-		0xFFFF	
-		RW	

15 0	ADATA	Timer/Counter 1n A Data bits. The range is 0x0002 to 0xFFFF.
		NOTE: Do not write “0000H” in the TIMER1n_ADR register when PPG mode.

10.2.3 TIMER1n_BDR: timer/counter 1n B data register

The TIMER1n_BDR are 32-bit registers with 32/16/8-bit access. (n = 0, 1, 2, and 3)

TIMER10_BDR=0x4000_2108, TIMER11_BDR =0x4000_2208
TIMER12_BDR =0x4000_2308, TIMER13_BDR =0x4000_2708

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved		BDATA	
-		0xFFFF	
-		RW	

15 0	BDATA	Timer/Counter 1n B Data bits. The range is 0x0000 to 0xFFFF.

10.2.4 TIMER1n_CAPDR: timer/counter 1n capture data register

The TIMER1n_ CAPDR are 32-bit registers with 32/16/8-bit access. (n = 10, 11, 12, and 13)

TIMER10_CAPDR =0x4000_210C, TIMER11_CAPDR =0x4000_220C
TIMER12_CAPDR =0x4000_230C, TIMER13_CAPDR =0x4000_270C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved		CAPD	
-		0x0000	
-		RO	

15 0	CAPD	Timer/Counter 1n Capture Data bits.

10.2.5 TIMER1n_PREDR: timer/counter 1n prescaler data register

The TIMER1n_PREDR are 32-bit registers with 32/16/8-bit access. (n = 0, 1, 2, and 3)

TIMER10_PREDR =0x4000_2110, TIMER11_PREDR =0x4000_2210
TIMER12_PREDR =0x4000_2310, TIMER13_PREDR =0x4000_2710

<table>
<tr><td colspan="8">31 30 29 28 27 26 25 24</td><td colspan="8">23 22 21 20 19 18 17 16</td><td colspan="8">15 14 13 12 11 10 9 8</td><td colspan="8">7 6 5 4 3 2 1 0</td></tr>
<tr><td colspan="20">Reserved</td><td colspan="12">PRED</td></tr>
<tr><td colspan="20">-</td><td colspan="12">0xFFF</td></tr>
<tr><td colspan="20">-</td><td colspan="12">RW</td></tr>
</table>

11 0	PRED	Timer/Counter 1n Prescaler Data bits.

10.2.6 TIMER1n_CNT: timer/counter 1n counter register

The TIMER1n_CNT are 32-bit registers with 32/16/8-bit access. (n = 0, 1, 2, and 3)

TIMER10_CNT =0x4000_2114, TIMER11_CNT =0x4000_2214
TIMER12_CNT =0x4000_2314, TIMER13_CNT =0x4000_2714

<table>
<tr><td colspan="8">31 30 29 28 27 26 25 24</td><td colspan="8">23 22 21 20 19 18 17 16</td><td colspan="8">15 14 13 12 11 10 9 8</td><td colspan="8">7 6 5 4 3 2 1 0</td></tr>
<tr><td colspan="16">Reserved</td><td colspan="16">CNT</td></tr>
<tr><td colspan="16">-</td><td colspan="16">0x0000</td></tr>
<tr><td colspan="16">-</td><td colspan="16">RO</td></tr>
</table>

15 0	CNT	Timer/Counter 1n Counter bits.

10.3 Functional description

10.3.1 Timer counter 10/11/12/13

Timer/counter n can be clocked by an internal or an external clock source (EC1n). Its clock source is selected by a clock selection logic which is controlled by clock selection bits (T1nCLK). (n = 0, 1, 2, and 3)

- TIMER 1n clock source: {fCLK/(TIMER1n_PREDR +1), EC1n

In capture mode, by TnCAP, data is captured into input capture data register (TIMER1n_CAPDR). TIMER 1n results the comparison between a counter and the data register through T1nOUT port in timer/counter mode. In addition, TIMER 1n outputs PWM wave form through T1nOUT port in the PPG mode.

Table 34 introduces various operating modes of TIMER 1n according to the value of timer/counter register.

Table 34. TIMER 1n Operating Modes

T1nEN	Alternative mode	T1nMS[1:0]	TIMER1n_PREDR	Timer 1n
1	AF1	00	0xXXX	16-bit Timer/Counter Mode
1	AF2	01	0xXXX	16-bit Capture Mode
1	AF1	10	0xXXX	16-bit PPG Mode(one-shot mode)
1	AF1	11	0xXXX	16-bit PPG Mode(repeat mode)

10.3.2 16-bit timer/counter mode

16-bit timer/counter mode is selected by control register as shown in Figure 41. The 16-bit timer has a counter and data register. The counter register is increased by internal or external clock input. Timer n can use the clock input with 12-bit prescaler division rates (TIMER1n_PREDR) and external clock (EC1n). When each value of TIMER1n_CNT and TIMER1n_ADR are identical in timer 1n, a match signal is generated and the interrupt of Timer 1n occurs. The TIMER1n_CNT values are automatically cleared by the match signal. It can be also cleared by software (T1nCLR).

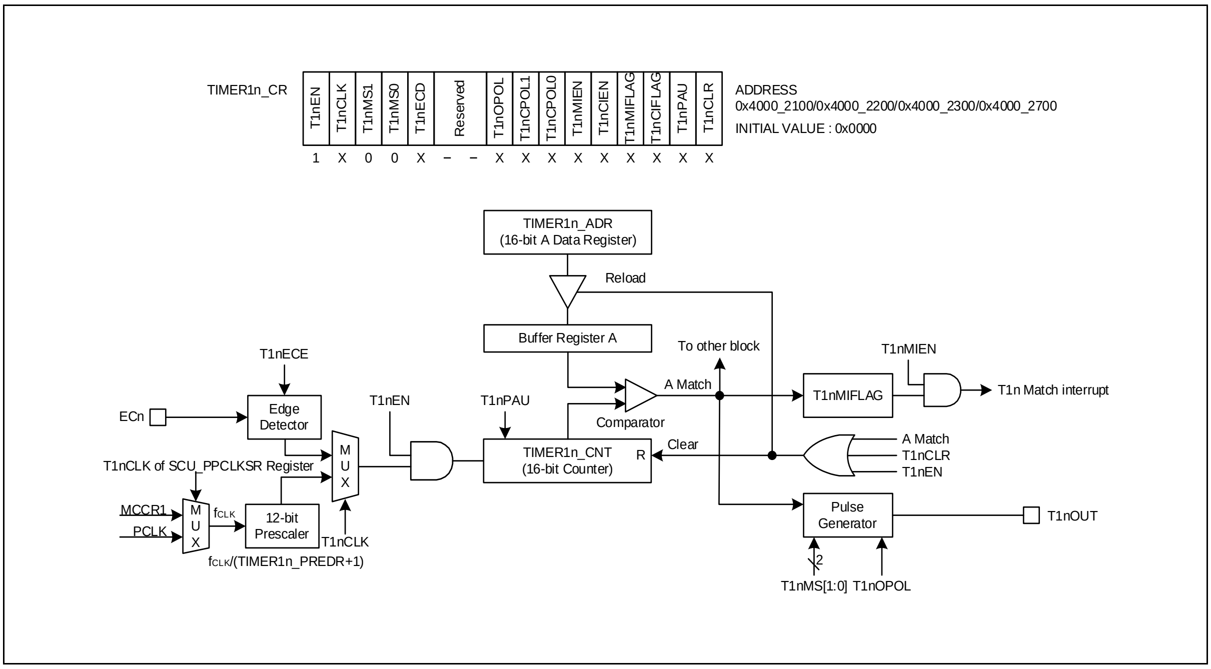


Figure 41. TIMER1n Block Diagram in Timer/Counter Mode (n = 0, 1, 2, and 3)

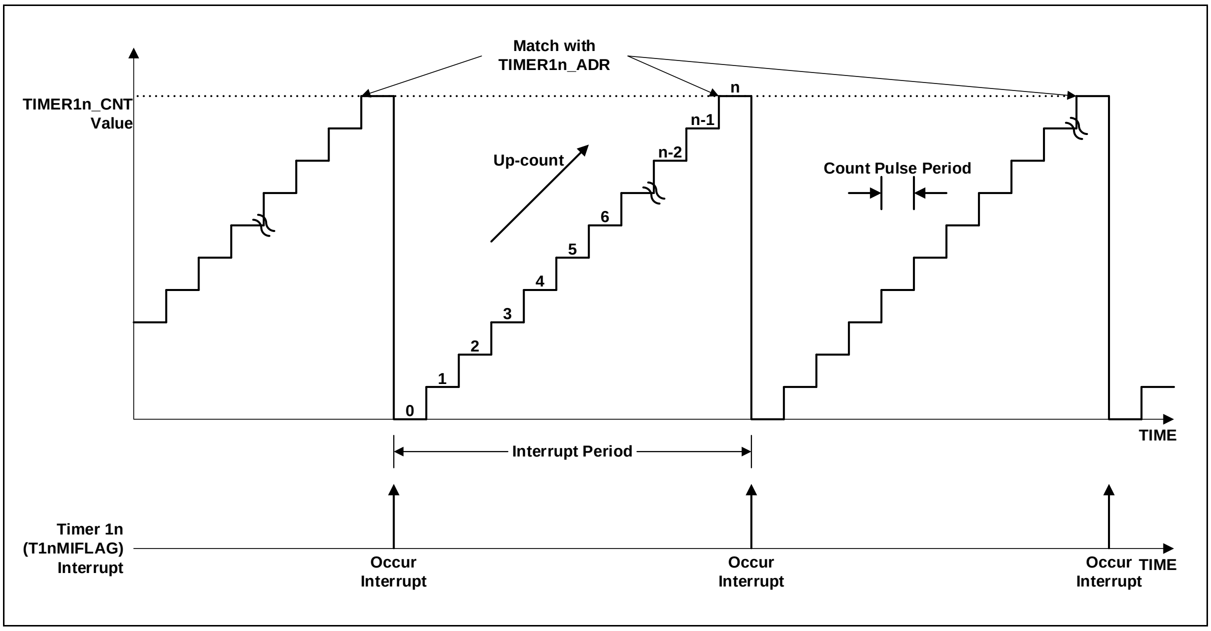


Figure 42. Timer/Counter Mode Timing Example of TIMER1n (n = 0, 1, 2, and 3)

Figure 43 shows the timer/counter mode operation of timer/counter 1n. Refer to **Figure 13. Clock Change Procedure** for internal timer clock source and section **5.2. Pin multiplexing** for Timer1n Output pin.

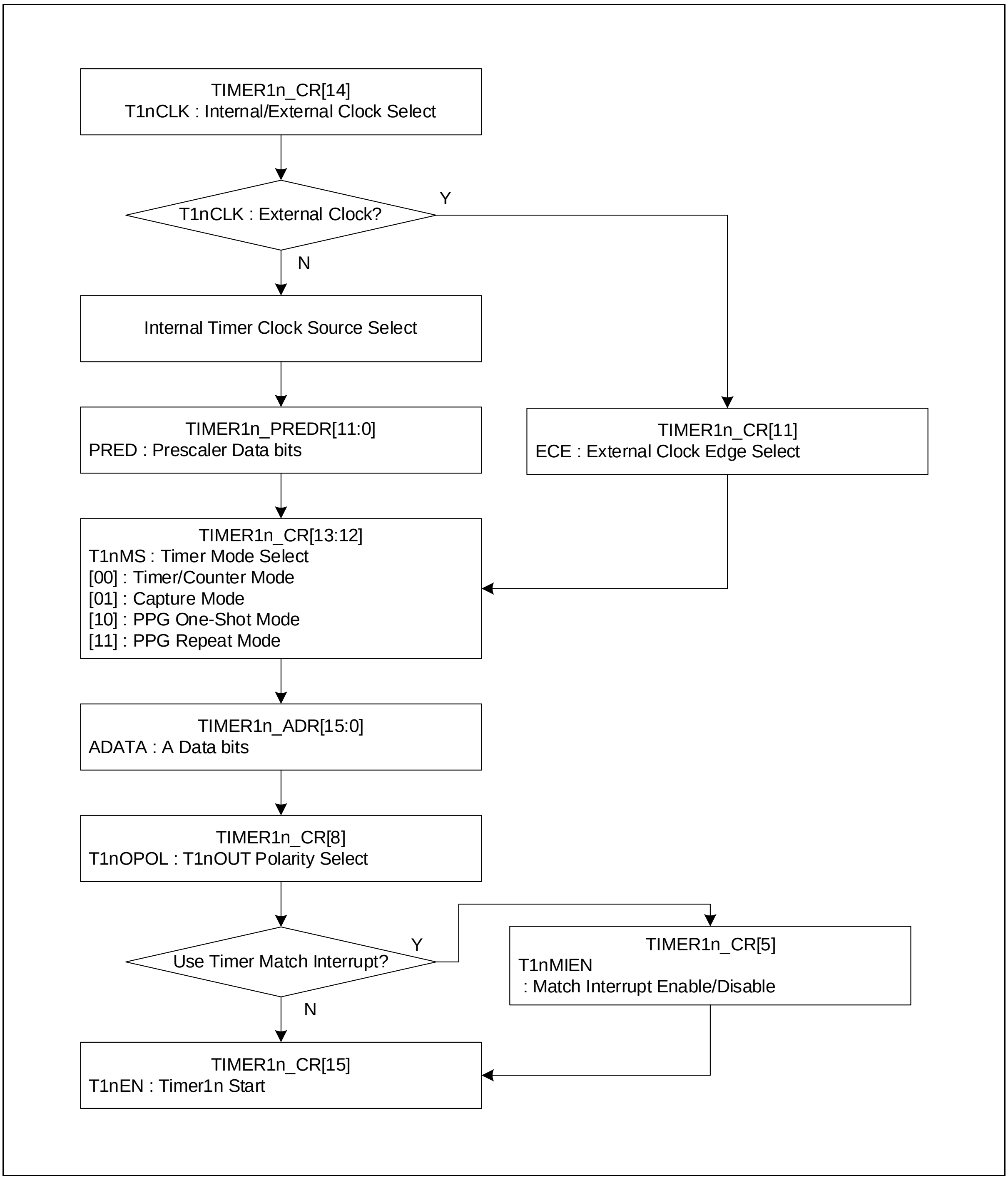

TIMER1n_CR[14]
T1nCLK : Internal/External Clock Select
T1nCLK : External Clock?
Y
N
Internal Timer Clock Source Select
TIMER1n_PREDR[11:0]
PRED : Prescaler Data bits
TIMER1n_CR[11]
ECE : External Clock Edge Select
TIMER1n_CR[13:12]
T1nMS : Timer Mode Select
[00] : Timer/Counter Mode
[01] : Capture Mode
[10] : PPG One-Shot Mode
[11] : PPG Repeat Mode
TIMER1n_ADR[15:0]
ADATA : A Data bits
TIMER1n_CR[8]
T1nOPOL : T1nOUT Polarity Select
Use Timer Match Interrupt?
Y
N
TIMER1n_CR[5]
T1nMIEN
: Match Interrupt Enable/Disable
TIMER1n_CR[15]
T1nEN : Timer1n Start

Figure 43. Timer/Counter Mode Operation Sequence of TIMER1n (n = 0, 1, 2, and 3)

10.3.3 16-bit capture mode

Timer n capture mode is evoked by setting T1nMS[1:0] as '01'. It can use an internal clock as a clock source. Basically, it has the same function as 16-bit timer/counter mode, and the interrupt occurs when TIMER1n_CNT is equal to TIMER1n_ADR. TIMER1n_CNT value can be automatically cleared by a match signal. It can be cleared by software too (TnCLR).

A timer interrupt in capture mode is very useful when pulse width of captured signal is wider than the maximum period of the timer. The capture result is loaded into TIMER1n_CAPDR. In the timer n capture mode, timer 1n output (TnO) waveform is not available.

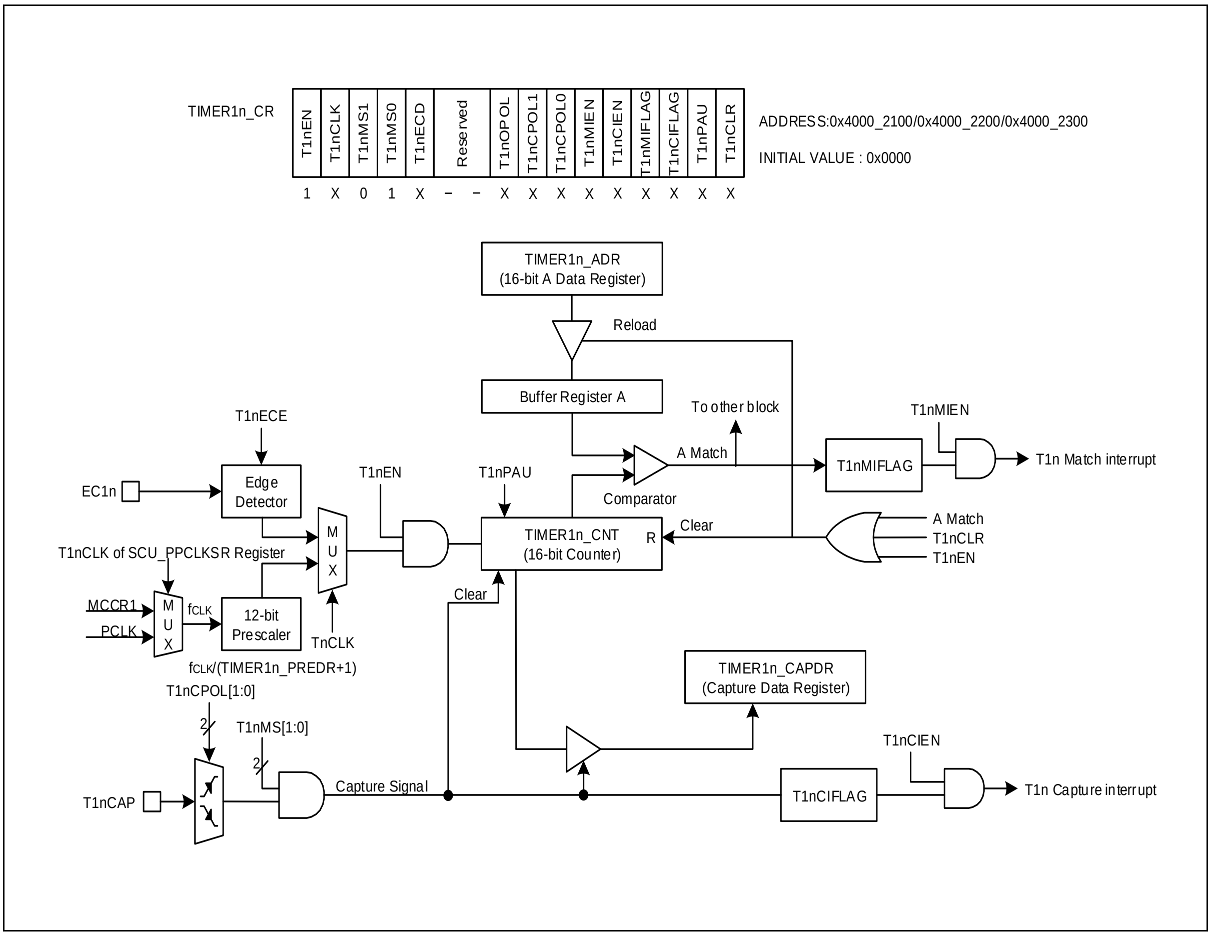


Figure 44. TIMER1n Block Diagram in Capture Mode (n = 0, 1, 2, and 3)

Capture mode of TIMER 1n can be configured by following the procedure introduced below:

1. Configure the corresponding capture pin for T1nCAP. (Refer to **5.2 Pin multiplexing**.)
2. Select a clock source for the TIMER 1n block by configuring the TIMER1n_CR<T1nCLK> bit.
3. For internal clock: Set the TIMER1n_PREDR with reference to Figure 13.
4. For external clock: Set the TIMER1n_CR<T1nECE> bit to select an edge of the external clock.
5. Set the TIMER1n_CR<T1nMS> bits to 1b' (capture mode) to enable timer capture mode.
6. Set the TIMER1n_CR<T1nCPOL> bits.

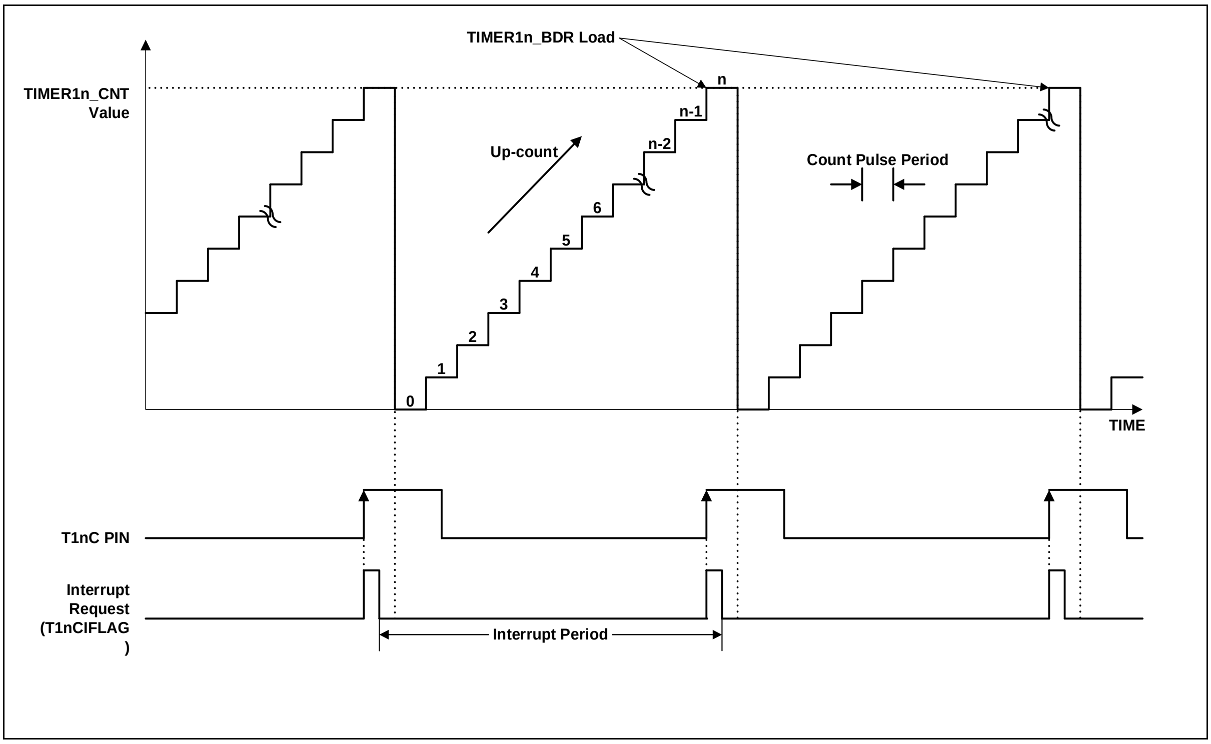


Figure 45. Capture Mode Timing Example of TIMER1n (n = 0, 1, 2, and 3)

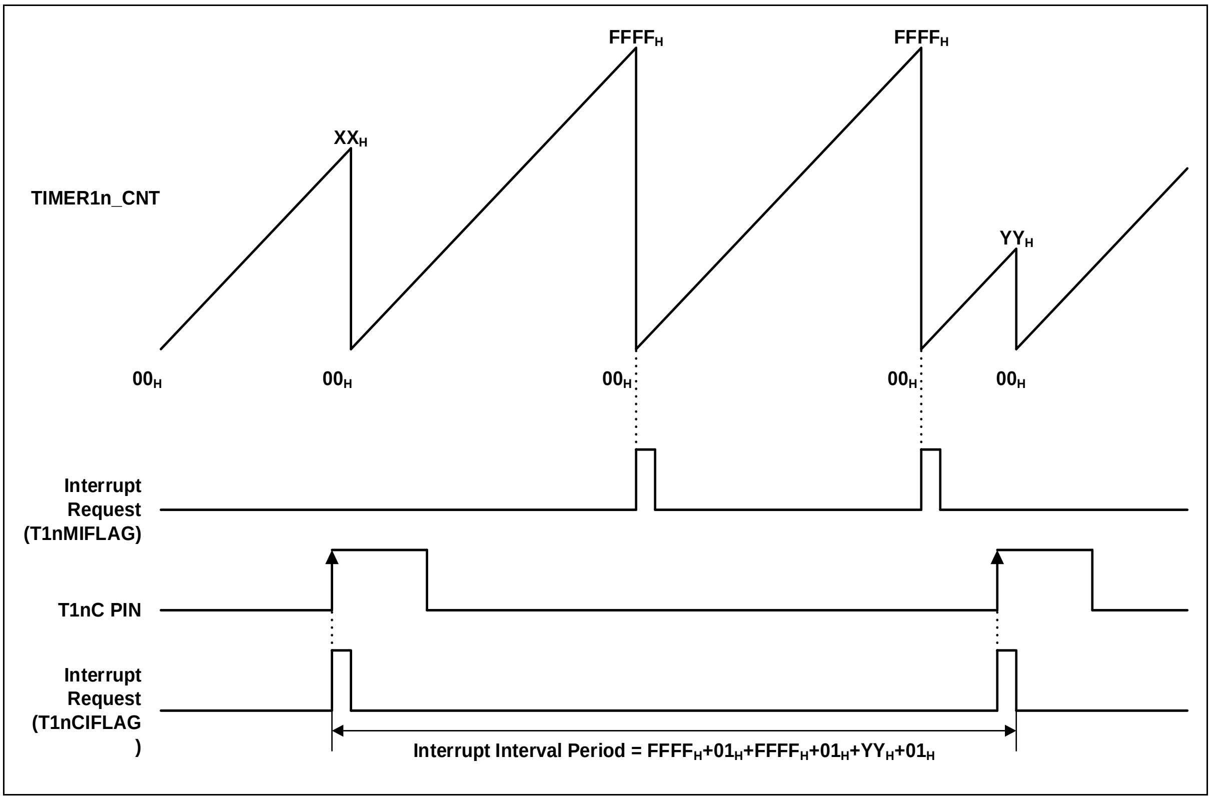

FFFF$_H$
FFFF$_H$
XX$_H$
TIMER1n_CNT
YY$_H$
00$_H$
00$_H$
00$_H$
00$_H$
00$_H$
Interrupt Request (T1nMIFLAG)
T1nC PIN
Interrupt Request (T1nCIFLAG)
Interrupt Interval Period = FFFF$_H$+01$_H$+FFFF$_H$+01$_H$+YY$_H$+01$_H$

Figure 46. Express Timer Overflow in Capture Mode of TIMER1n (n = 0, 1, 2, and 3)

Figure 47 shows the capture mode operation of timer/counter 1n. Refer to **Figure 13. Clock Change Procedure** for internal timer clock source and section **5.2. Pin multiplexing** for Timer1n Output pin.

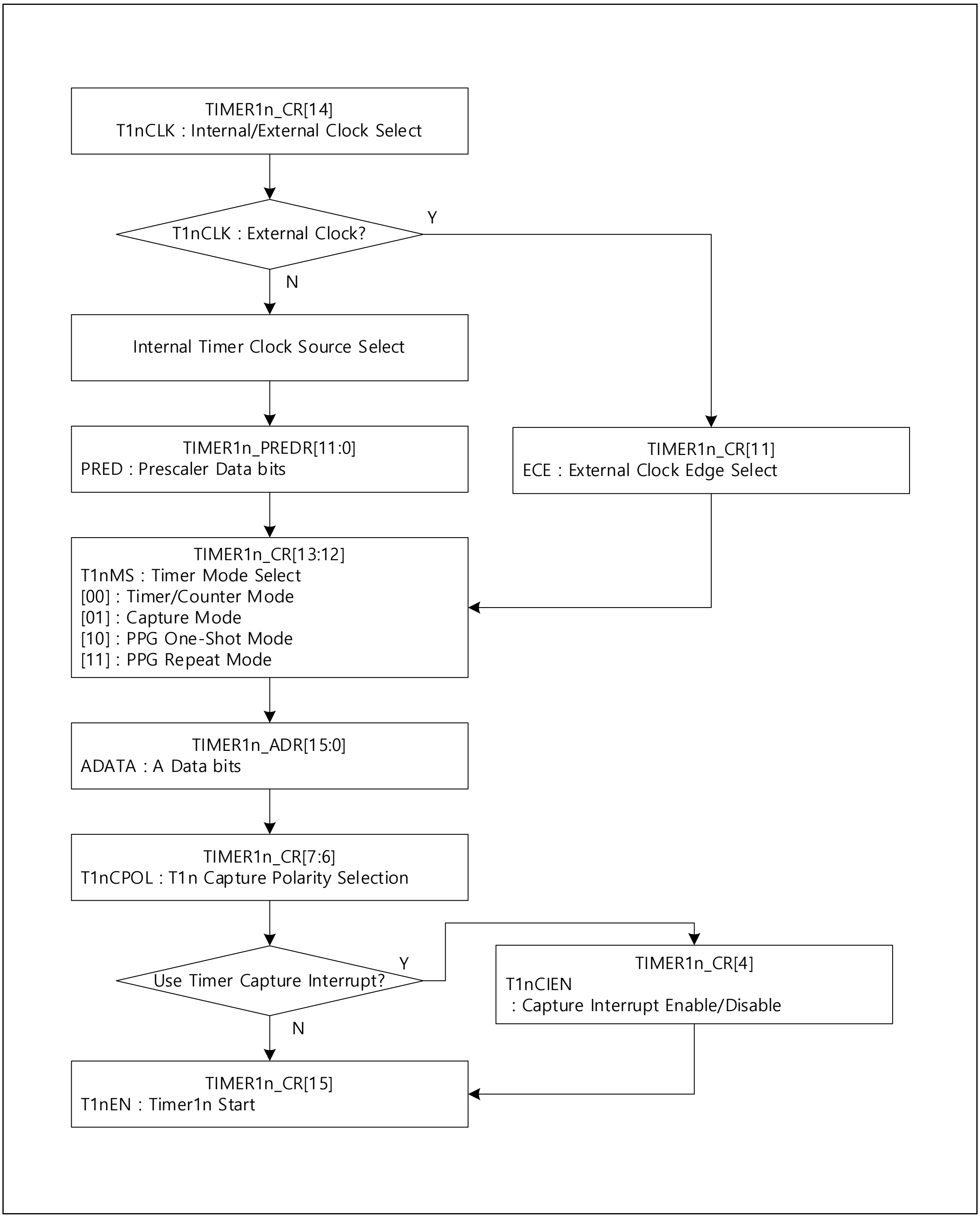
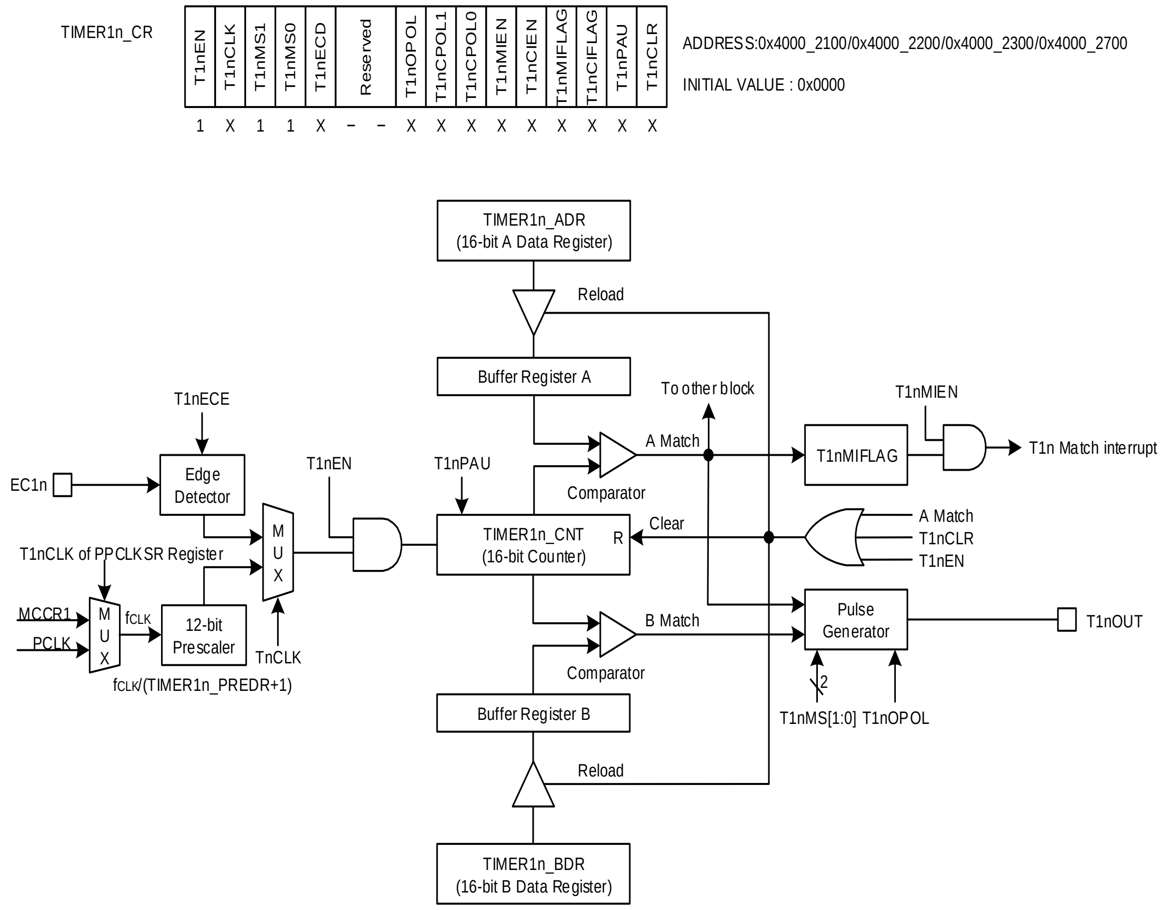

TIMER1n_CR[14]
T1nCLK : Internal/External Clock Select
T1nCLK : External Clock?
Y
N
Internal Timer Clock Source Select
TIMER1n_PREDR[11:0]
PRED : Prescaler Data bits
TIMER1n_CR[11]
ECE : External Clock Edge Select
TIMER1n_CR[13:12]
T1nMS : Timer Mode Select
[00] : Timer/Counter Mode
[01] : Capture Mode
[10] : PPG One-Shot Mode
[11] : PPG Repeat Mode
TIMER1n_ADR[15:0]
ADATA : A Data bits
TIMER1n_CR[7:6]
T1nCPOL : T1n Capture Polarity Selection
Use Timer Capture Interrupt?
Y
N
TIMER1n_CR[4]
T1nCIEN
: Capture Interrupt Enable/Disable
TIMER1n_CR[15]
T1nEN : Timer1n Start

Figure 47. Capture Mode Operation Sequence of TIMER1n (n = 0, 1, 2, and 3)

10.3.4 16-bit PPG mode

Timer1n has a PPG (Programmable Pulse Generation) function. In PPG mode, the TnO pin outputs up to 16-bit resolution PWM output. This pin should be configured as a PWM output by setting corresponding Pn_AFSRx to ‘AF1’. Period of the PWM output is determined by the TIMER1n_ADR, and duty of the PWM output is determined by the TIMER1n_BDR.



NOTE: The TnEN is automatically cleared to logic “0” after one pulse is generated at a PPG one-shot mode.

Figure 48. TIMER1n Block Diagram in PPG Mode (n = 0, 1, 2, and 3)

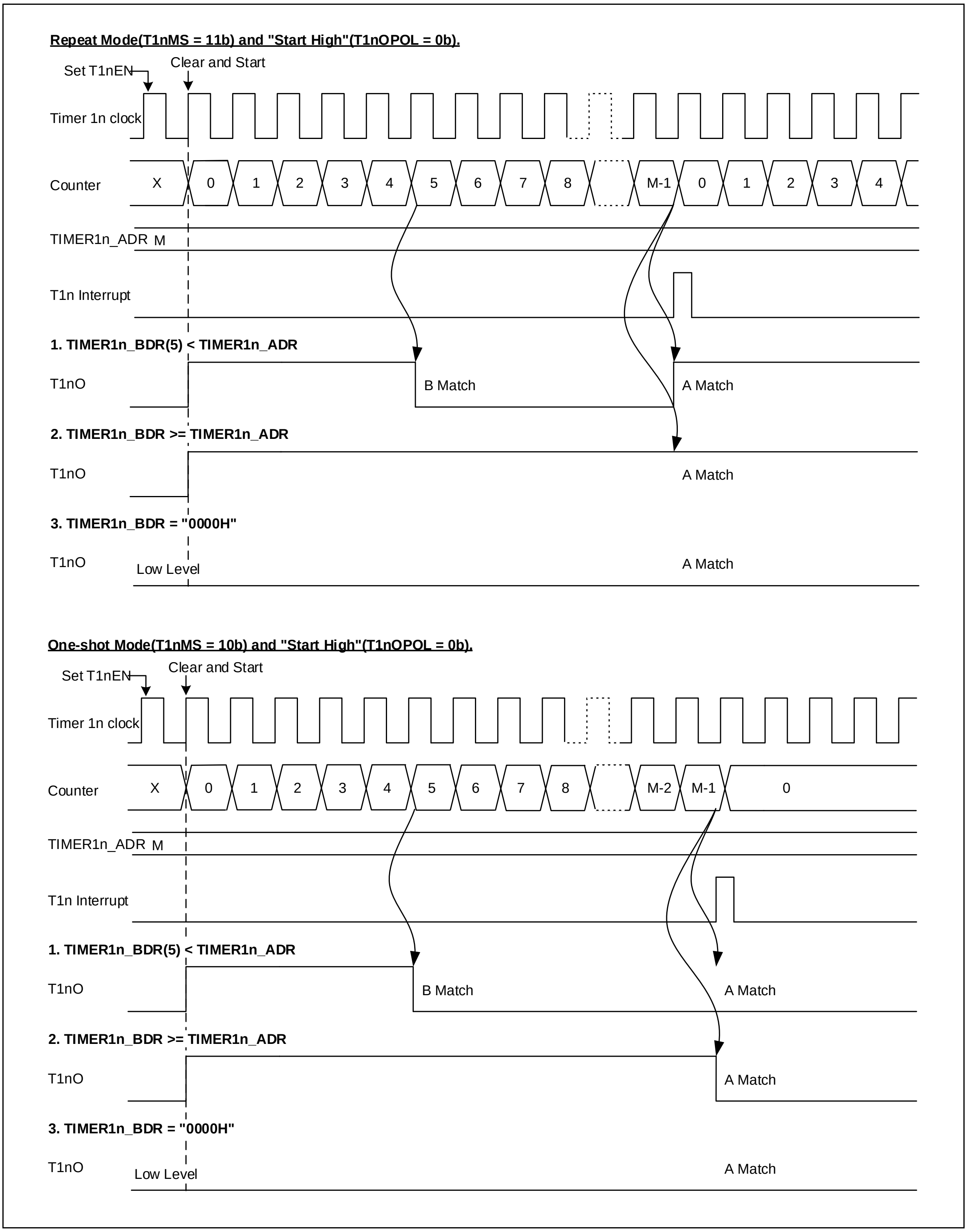


Figure 49. PPG Mode Timing Example of TIMER1n (n = 0, 1, 2, and 3)

Figure 50 shows the PPG mode operation of timer/counter 1n. Refer to **Figure 13. Clock Change Procedure** for internal timer clock source and section **5.2. Pin multiplexing** ffig13or Timer1n Output pin.

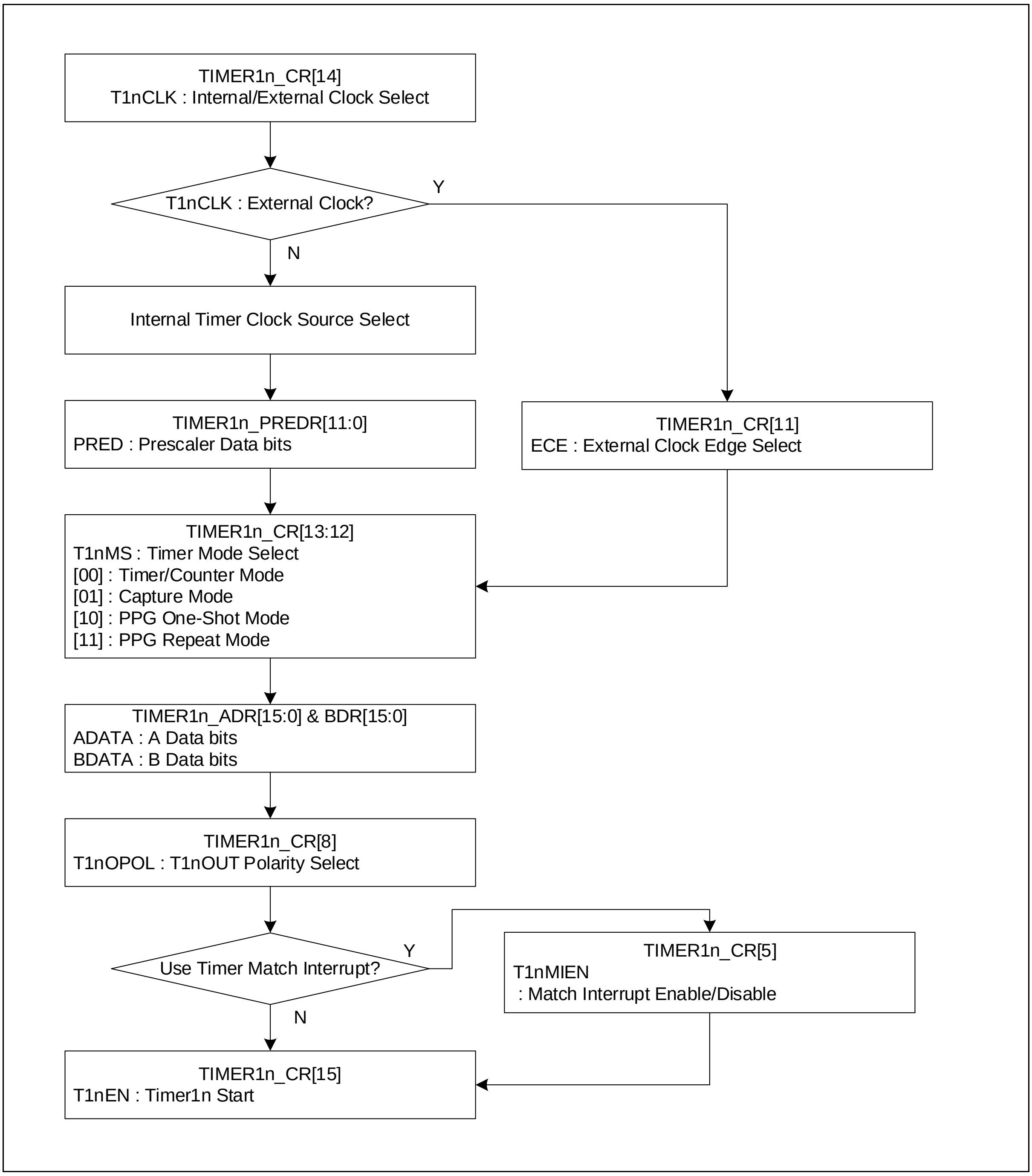

TIMER1n_CR[14]
T1nCLK : Internal/External Clock Select
T1nCLK : External Clock?
Y
N
Internal Timer Clock Source Select
TIMER1n_PREDR[11:0]
PRED : Prescaler Data bits
TIMER1n_CR[11]
ECE : External Clock Edge Select
TIMER1n_CR[13:12]
T1nMS : Timer Mode Select
[00] : Timer/Counter Mode
[01] : Capture Mode
[10] : PPG One-Shot Mode
[11] : PPG Repeat Mode
TIMER1n_ADR[15:0] & BDR[15:0]
ADATA : A Data bits
BDATA : B Data bits
TIMER1n_CR[8]
T1nOPOL : T1nOUT Polarity Select
Use Timer Match Interrupt?
Y
N
TIMER1n_CR[5]
T1nMIEN
: Match Interrupt Enable/Disable
TIMER1n_CR[15]
T1nEN : Timer1n Start

Figure 50. PPG Mode Operation Sequence of TIMER1n (n = 0, 1, 2, and 3)

11 32-bit timer

32-bit timer block comprises 2 channels of 32-bit general purpose timers. Each channel has an independent 32-bit counter and a dedicated prescaler that feeds a counting clock. 32-bit timer supports periodic timer, PWM pulse, one-shot and capture mode. In addition, one more optional free-run timer is provided. Main purpose of 32-bit timer is a periodical tick timer.

32-bit timer of A31T214/216 series features the followings:

- 32-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 12-bit prescaler
- Synchronous start and clear function

Table 35 introduces pins assigned for 32-bit timer.

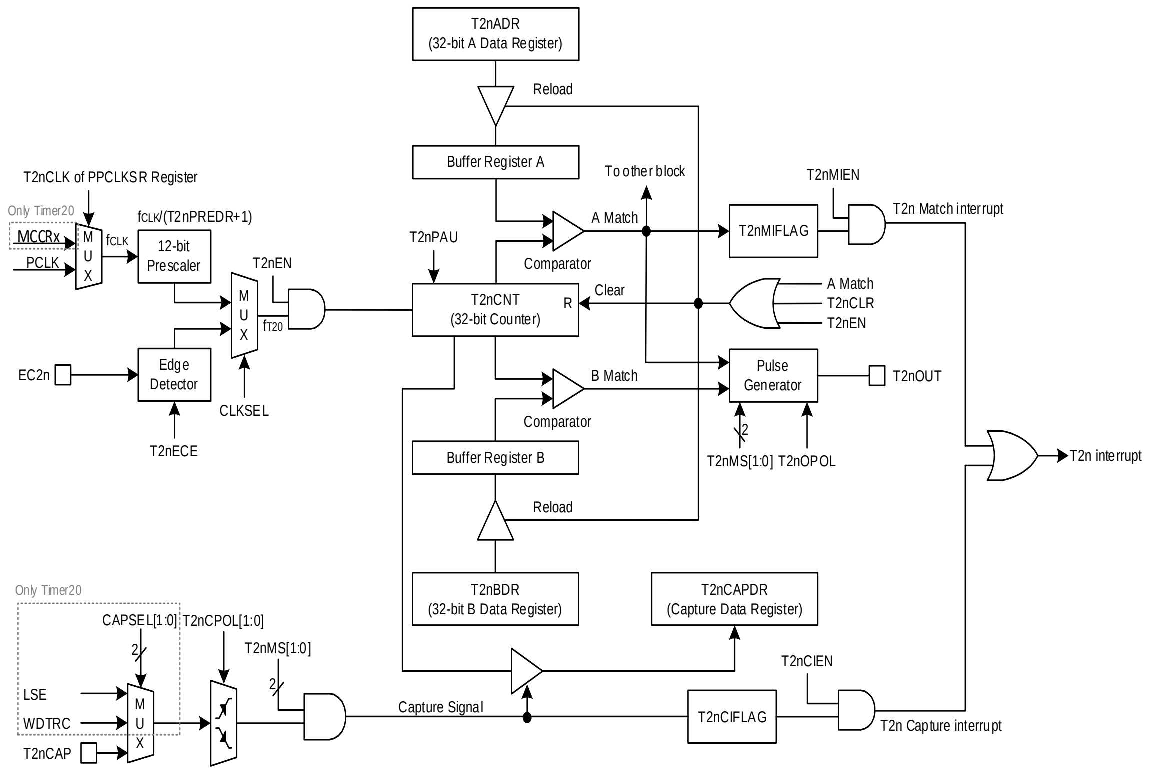
Table 35. Pin Assignment of 32-bit Timer: External Pins

Pin name	Type	Description
EC2n	I	Timer 2n external clock input
T2nCAP	I	Timer 2n capture input
T2nOUT	O	Timer/PWM/one-shot output

NOTE: n = 0 or 1

11.1 32-bit timer block diagram

In this section, 32-bit timer is described in a block diagram in Figure 51.



NOTES:

1. The T2nEN is automatically cleared to logic "0" after one pulse is generated at a PPG one-shot mode.
2. After the T2nEN bit is set, the counting of TIMER2n_CNT may be delayed 2 clocks or more.

Figure 51. 32-bit Timer Block Diagram

11.2 Registers

Table 36 and Table 37 show base address and register map of the 32-bit timer.

Table 36. Base Address of 32-bit Timer

Name	Base address
TIMER20	0x4000_2500
TIMER21	0x4000_2600

NOTE: n = 0 or 1

Table 37. TIMER 2n Register Map

Name	Offset	Type	Description	Reset value	Reference
TIMER2n_CR	0x0000	RW	Timer/Counter 2n Control Register	0x0000_0000	
TIMER2n_ADR	0x0004	RW	Timer/Counter 2n A Data Register	0xFFFF_FFFF	
TIMER2n_BDR	0x0008	RW	Timer/Counter 2n B Data Register	0xFFFF_FFFF	
TIMER2n_CAPDR	0x000C	RO	Timer/Counter 2n Capture Data Register	0x0000_0000	
TIMER2n_PREDR	0x0010	RW	Timer/Counter 2n Prescaler Data Register	0x0000_0FFF	
TIMER2n_CNT	0x0014	RO	Timer/Counter 2n Counter Register	0x0000_0000	

NOTE: n = 0 or 1

11.2.1 TIMER2n_CR: timer/counter 2n control register

Timer module should be configured properly before running. When a target purpose is defined, the timer can be configured in the TIMER2n_CR register. After configuring TIMER2n_CR, a user can start or stop the timer function by using TIMER2n_CR.

The TIMER2n_CR are 32-bit registers with 32/16/8-bit access. (n = 0 or 1)

TIMER20_CR=0x4000_2500, TIMER21_CR=0x4000_2600

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		T20EN	T20CLK	T20MS		T20ECE	CAPSEL		T20OPOL	T20CPOL		T20MIEN	T20CIEN	T20MIFLAG	T20CIFLAG	T20PAU	T20CLR
-		0	0	00		0	00		0	00		0	0	0	0	0	0
-		RW	RW	RW		RW	RW		RW	RW		RW	RW	RW	RW	RW	RW

15	T2nEN	Timer 2n Operation Enable bit.	
		0	Disable timer 2n operation.
		1	Enable timer 2n operation. (Counter clear and start)
14	T2nCLK	Timer 2n Clock Selection bit.	
		0	Select an internal prescaler clock.
		1	Select an external clock.
NOTES: 1. This bit should be changed during T2nEN bit is "0b". 2. If you select an internal prescaler clock, you should set T2nCLK bit in the SCU_PPCLKSR register first. (Only Timer20) 3. Internal prescaler clock of Timer21 is PCLK.			
13 12	T2nMS	Timer 2n Operation Mode Selection bits.	
		00	Timer/Counter mode. (T2nO: Toggle at A-match)
		01	Capture mode. (The A-match interrupt can occur)
		10	PPG one-shot mode. (T2nO: Programmable pulse output)
		11	PPG repeat mode. (T2nO: Programmable pulse output)
		NOTE: This bit should be changed during T2nEN bit is "0b".	
11	T2nECE	Timer 2n External Clock Edge Selection bit.	
		0	Select falling edge of external clock.
		1	Select rising edge of external clock.
10 9	CAPSEL	Timer 20 Capture Signal Selection bits.	
		00	Select an external capture signal.
		01	Select the LSE (External Sub Oscillator) signal
		10	Select the WDTRC (Watch-dog timer RC oscillator) signal.
		11	Not used
		NOTE: This bit should be changed during T2nEN bit is "0b". Timer21 Capture Signal is only external capture signal. (T21C)	
8	T2nOPOL	T2nO Polarity Selection bit.	
		0	Start high. (T2nO is low level at disable)
		1	Start low. (T2nO is high level at disable)
7 6	T2nCPOL	Timer 2n Capture Polarity Selection bits.	
		00	Capture on falling edge.
		01	Capture on rising edge.

		10	Capture on both of falling and rising edge.
		11	Reserved.
5	T2nMIEN	Timer 2n Match Interrupt Enable bit.	
		0	Disable timer 2n match interrupt.
		1	Enable timer 2n match interrupt.
4	T2nCIEN	Timer 2n Capture Interrupt Enable bit.	
		0	Disable timer 2n capture interrupt.
		1	Enable timer 2n capture interrupt.
3	T2nMIFLAG	Timer 2n Match Interrupt Flag bit.	
		0	No request occurred.
		1	Request occurred, This bit is cleared to ‘0’ when write ‘1’.
2	T2nCIFLAG	Timer 2n Capture Interrupt Flag bit.	
		0	No request occurred.
		1	Request occurred, This bit is cleared to ‘0’ when write ‘1’.
1	T2nPAU	Timer 2n Counter Temporary Pause Control bit.	
		0	Continue counting.
		1	Temporary pause.
0	T2nCLR	Timer 2n Counter and Prescaler Clear bit.	
		0	No effect.
		1	Clear timer 2n counter and prescaler. (Automatically cleared to “0b” after operation)

11.2.2 TIMER2n_ADR: timer/counter 2n A data register

The TIMER2n_ADR are 32-bit registers with 32/16/8-bit access. (n = 0 or 1)

TIMER20_ADR=0x4000_2504, TIMER21_ADR=0x4000_2604

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
ADATA			
0xFFFFFFFF			
RW			

31 0	ADATA	Timer/Counter 2n A Data bits. The range is 0x0002 to 0xFFFFFFFF.
NOTE: Do not write "0000H" in the TIMER20_ADR register when PPG mode.		

11.2.3 TIMER2n_BDR: timer/counter 2n B data register

The TIMER2n_BDR are 32-bit registers with 32/16/8-bit access. (n = 0 or 1)

TIMER20_BDR=0x4000_2508, TIMER21_BDR=0x4000_2608

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
BDATA			
0xFFFFFFFF			
RW			

31 0	BDATA	Timer/Counter 2n B Data bits. The range is 0x0000 to 0xFFFFFFFF.

11.2.4 TIMER2n_CAPDR: timer/counter 2n capture data register

The TIMER2n_ CAPDR are 32-bit registers with 32/16/8-bit access.

TIMER20_CAPDR=0x4000_250C, TIMER21_CAPDR=0x4000_260C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CAPD			
0x0000			
RO			

31 0	CAPD	Timer/Counter 2n Capture Data bits.

11.2.5 TIMER2n_PREDR: timer/counter 2n prescaler data register

The TIMER2n_PREDR are 32-bit registers with 32/16/8-bit access.

TIMER20_PREDR=0x4000_2510, TIMER21_PREDR=0x4000_2610

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				PRED											
0x00000																				0xFFF											
–																				RW											

11 0	PRED	Timer/Counter 2n Prescaler Data bits. f_{CLK}/(TIMER2n_PREDR +1)

11.2.6 TIMER2n_CNT: timer/counter 2n counter register

The TIMER2n_CNT are 32-bit registers with 32/16/8-bit access.

TIMER20_CNT=0x4000_2514, TIMER21_CNT=0x4000_2514

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT																															
0x00000000																															
RO																															

31 0	CNT	Timer/Counter 2n Counter bits.

11.3 Functional description

11.3.1 Timer counter 2n

Timer/counter 2n can be clocked by an internal or an external clock source (EC2n). Its clock source is selected by a clock selection logic which is controlled by clock selection bits (T2nCLK).

- TIMER 2n clock source: {fCLK/(TIMER2n_PREDR +1), EC2n

In capture mode, by T2nCAP, data is captured into input capture data register (TIMER2n_CAPDR). TIMER 2n results the comparison between a counter and the data register through T2nOUT port in timer/counter mode. In addition, TIMER 2n outputs PWM wave form through T2nOUT port in the PPG mode.

Table 38 introduces various operating modes of TIMER 2n according to the value of timer/counter register.

Table 38. TIMER 2n Operating Modes

T2nEN	Alternative mode	T2nMS[1:0]	TIMER2n_PREDR	TIMER 2n
1	AF1	00	0xXXX	32-bit Timer/Counter Mode
1	AF2	01	0xXXX	32-bit Capture Mode
1	AF1	10	0xXXX	32-bit PPG Mode(one-shot mode)
1	AF1	11	0xXXX	32-bit PPG Mode(repeat mode)

11.3.2 32-bit timer/counter mode

32-bit timer/counter mode is selected by control register as shown in Figure 52. The 32-bit timer has a counter and data register. The counter register is increased by internal or external clock input. TIMER 2n can use the clock input with 12-bit prescaler division rates (TIMER2n_PREDR) and external clock (EC2n). When each value of TIMER2n_CNT and TIMER2n_ADR are identical in TIMER2n, a match signal is generated and the interrupt of Timer 2n occurs. The TIMER2n_CNT values are automatically cleared by the match signal. It can be also cleared by software (T2nCLR).

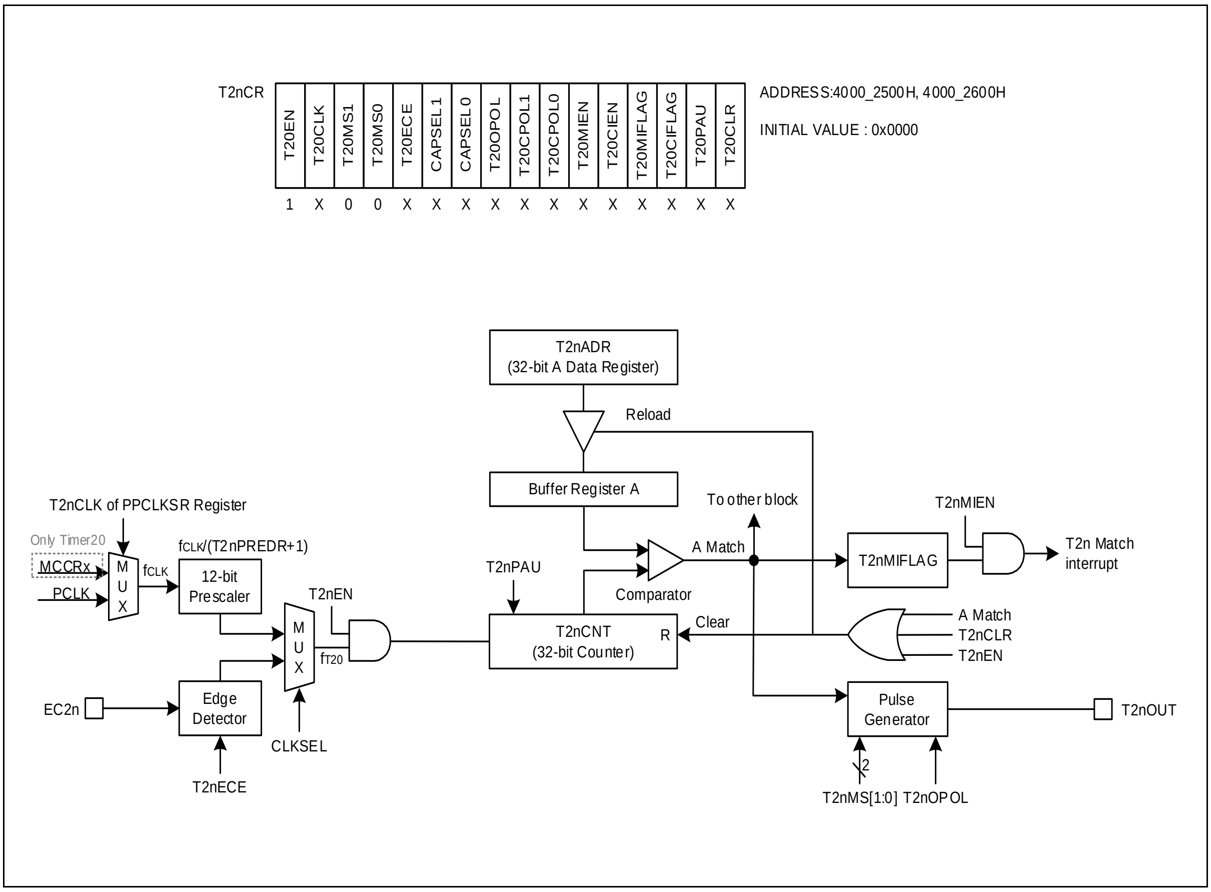


Figure 52. TIMER2n Block Diagram in Timer/Counter Mode

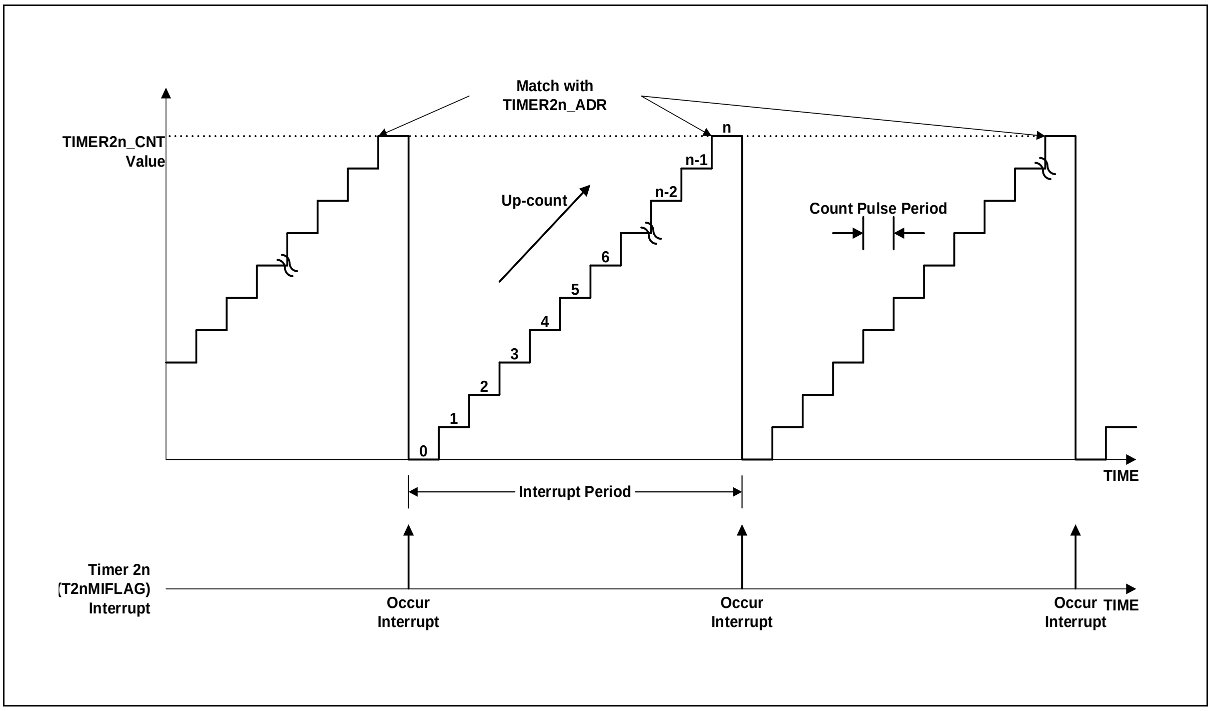


Figure 53. Timer/Counter Mode Timing Example of TIMER2n

Figure 54 shows the timer/counter mode operation of timer/counter 2n. Refer to **Figure 13. Clock Change Procedure** for internal timer clock source and section **5.2. Pin multiplexing** for Timer2n Output pin.

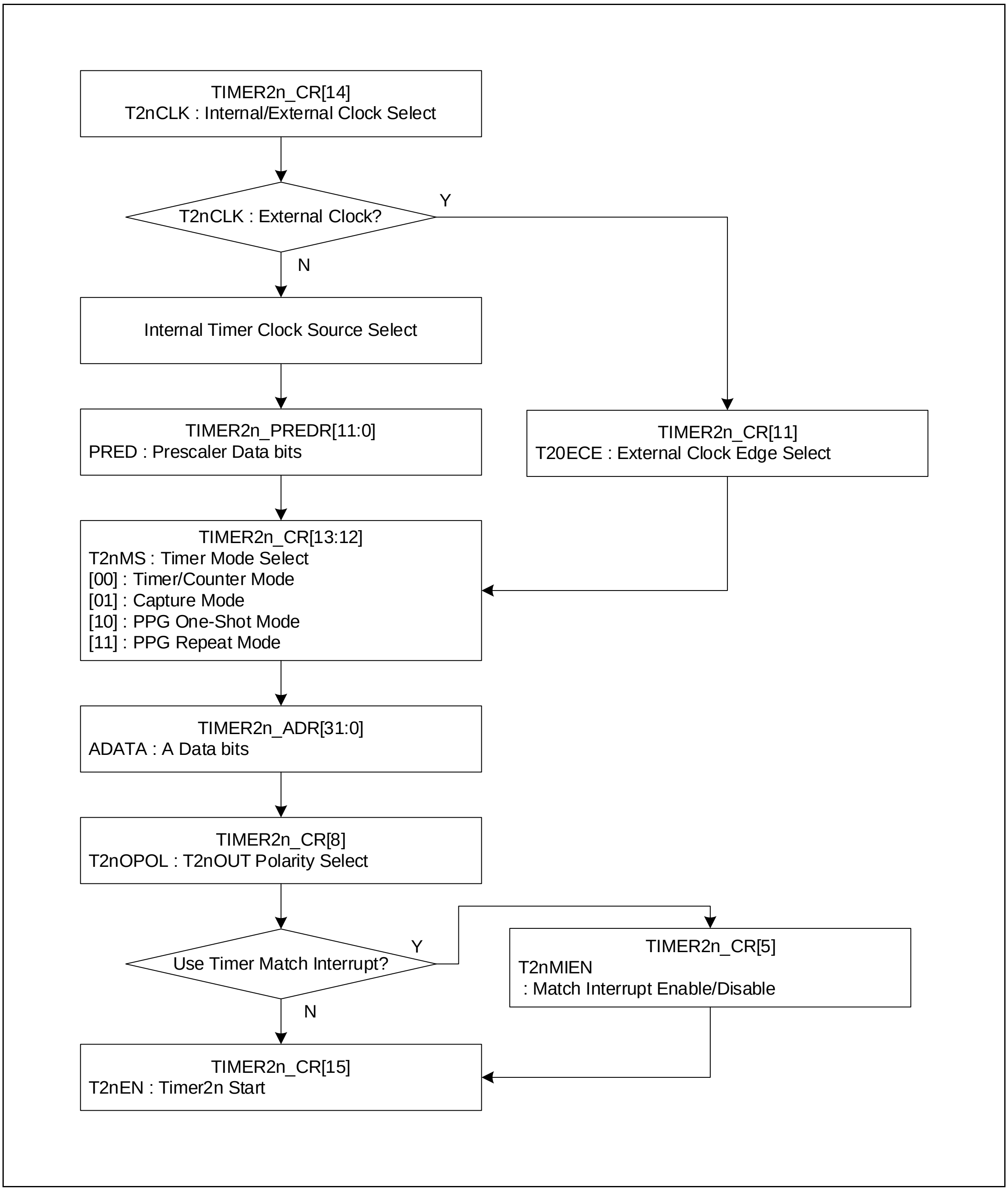
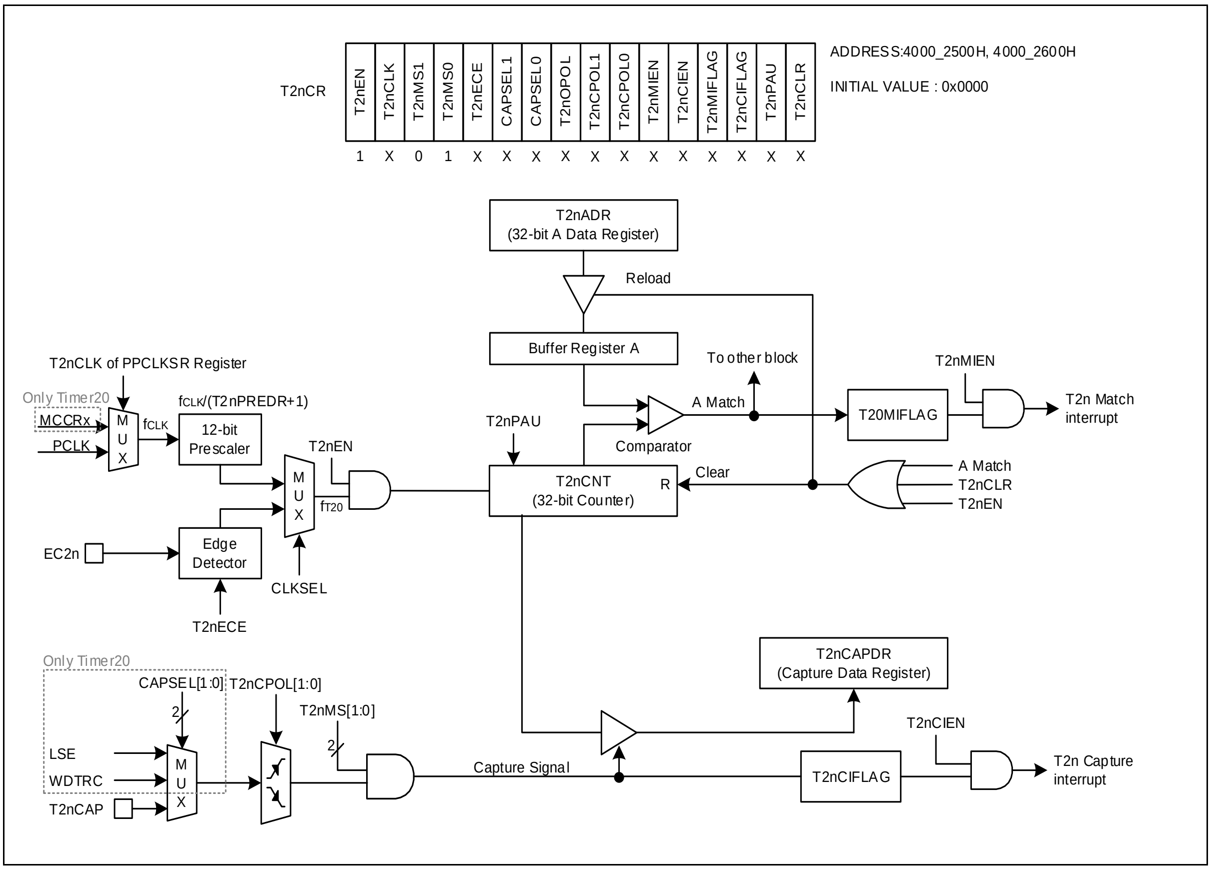

TIMER2n_CR[14]
T2nCLK : Internal/External Clock Select
T2nCLK : External Clock?
Y
N
Internal Timer Clock Source Select
TIMER2n_PREDR[11:0]
PRED : Prescaler Data bits
TIMER2n_CR[11]
T20ECE : External Clock Edge Select
TIMER2n_CR[13:12]
T2nMS : Timer Mode Select
[00] : Timer/Counter Mode
[01] : Capture Mode
[10] : PPG One-Shot Mode
[11] : PPG Repeat Mode
TIMER2n_ADR[31:0]
ADATA : A Data bits
TIMER2n_CR[8]
T2nOPOL : T2nOUT Polarity Select
Use Timer Match Interrupt?
Y
N
TIMER2n_CR[5]
T2nMIEN
: Match Interrupt Enable/Disable
TIMER2n_CR[15]
T2nEN : Timer2n Start

Figure 54. Timer/Counter Mode Operation Sequence of TIMER2n (n = 0 or 1)

11.3.3 32-bit capture mode

Timer 2n capture mode is evoked by setting T2nMS[1:0] as '01'. It can use an internal clock as a clock source. Basically, it has the same function as 32-bit timer/counter mode, and the interrupt occurs when TIMER2n_CNT is equal to TIMER2n_ADR. TIMER2n_CNT value can be cleared by software (T2nCLR).

A timer interrupt in capture mode is very useful when pulse width of captured signal is wider than the maximum period of the timer. The capture result is loaded into TIMER2n_BDR. In the TIMER2n capture mode, TIMER2n output (T2nOUT) waveform is not available. (n = 0 or 1).



T2nCR	T2nEN	T2nCLK	T2nMS1	T2nMS0	T2nECE	CAPSEL1	CAPSEL0	T2nOPOL	T2nCPOL1	T2nCPOL0	T2nMIEN	T2nCIEN	T2nMIFLAG	T2nCIFLAG	T2nPAU	T2nCLR
	1	X	0	1	X	X	X	X	X	X	X	X	X	X	X	X

ADDRESS:4000_2500H, 4000_2600H

INITIAL VALUE : 0x0000

Figure 55. TIMER2n Block Diagram in Capture Mode

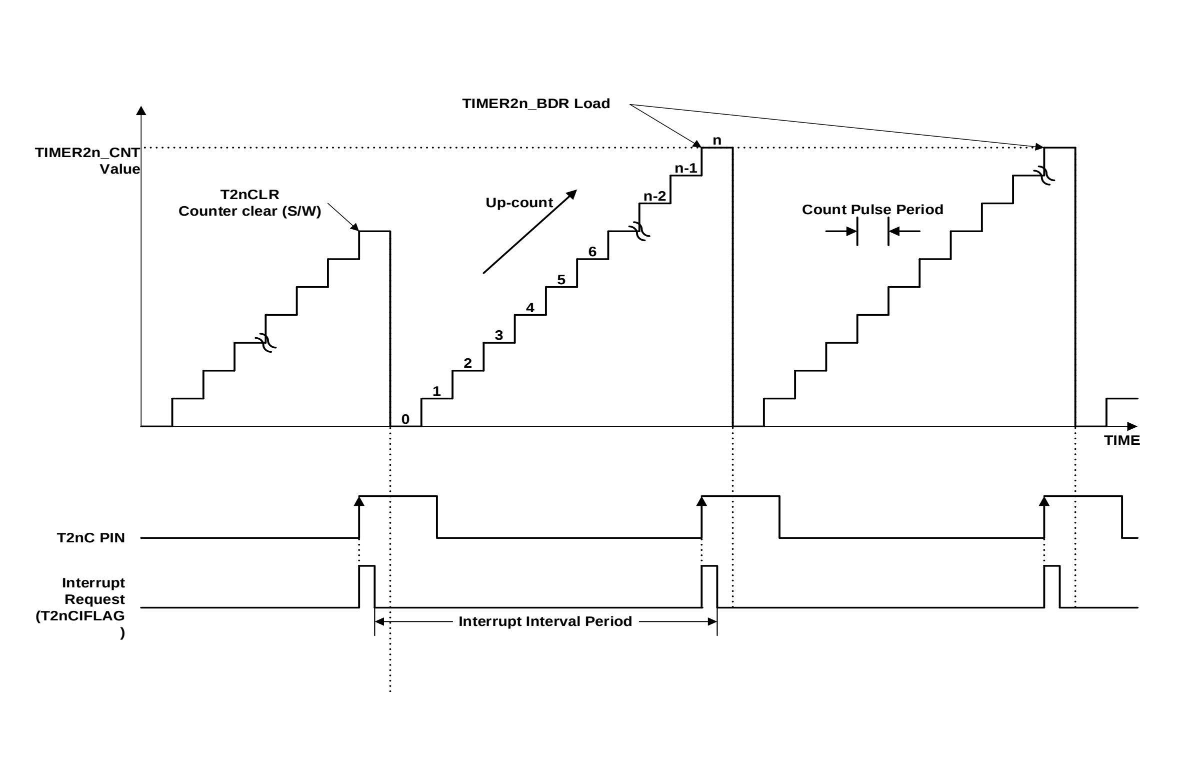


Figure 56. Capture Mode Timing Example of TIMER2n (n = 0 and 1)

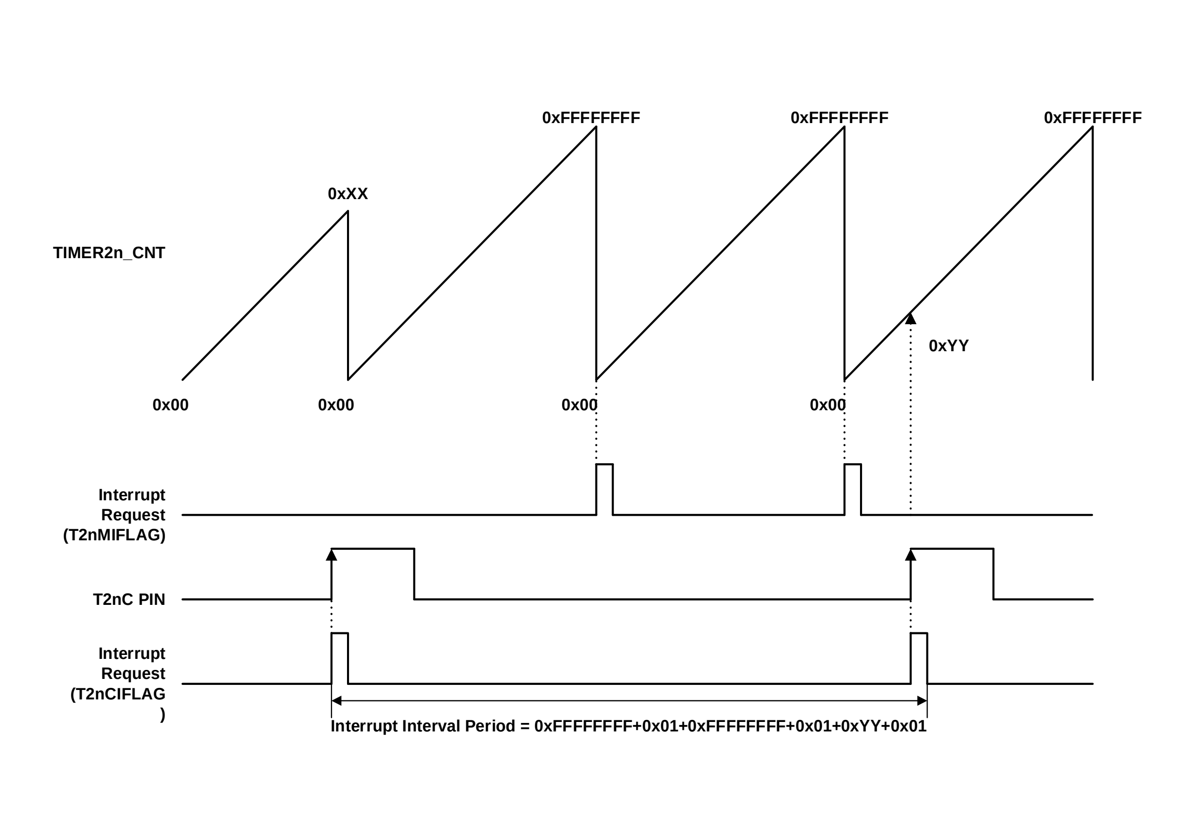

0xFFFFFFFF
0xFFFFFFFF
0xFFFFFFFF
0xXX
TIMER2n_CNT
0xYY
0x00
0x00
0x00
0x00
Interrupt Request (T2nMIFLAG)
T2nC PIN
Interrupt Request (T2nCIFLAG)
Interrupt Interval Period = 0xFFFFFFFF+0x01+0xFFFFFFFF+0x01+0xYY+0x01

Figure 57. Express Timer Overflow in Capture Mode of TIMER2n (T2nCNCLR = 1'b1)

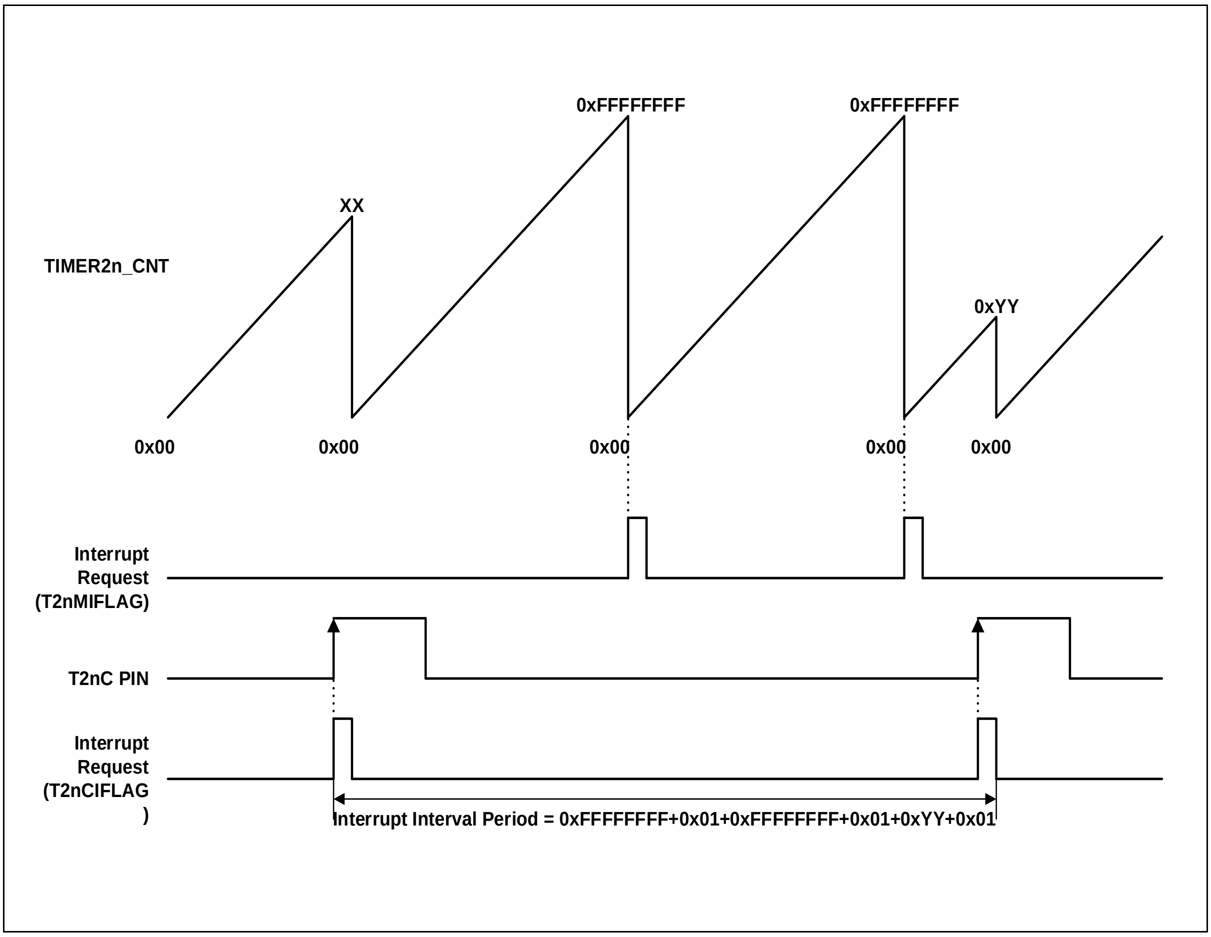

0xFFFFFFFF
0xFFFFFFFF
XX
TIMER2n_CNT
0xYY
0x00
0x00
0x00
0x00
0x00
Interrupt Request (T2nMIFLAG)
T2nC PIN
Interrupt Request (T2nCIFLAG)
Interrupt Interval Period = 0xFFFFFFFF+0x01+0xFFFFFFFF+0x01+0xYY+0x01

Figure 58. Express Timer Overflow in Capture Mode of TIMER2n (T2nCNCLR = 1’b0)

Figure 59 shows the capture mode operation of timer/counter 2n. Refer to **Figure 13. Clock Change Procedure** for internal timer clock source and section **5.2. Pin multiplexing** for Timer2n Output pin.

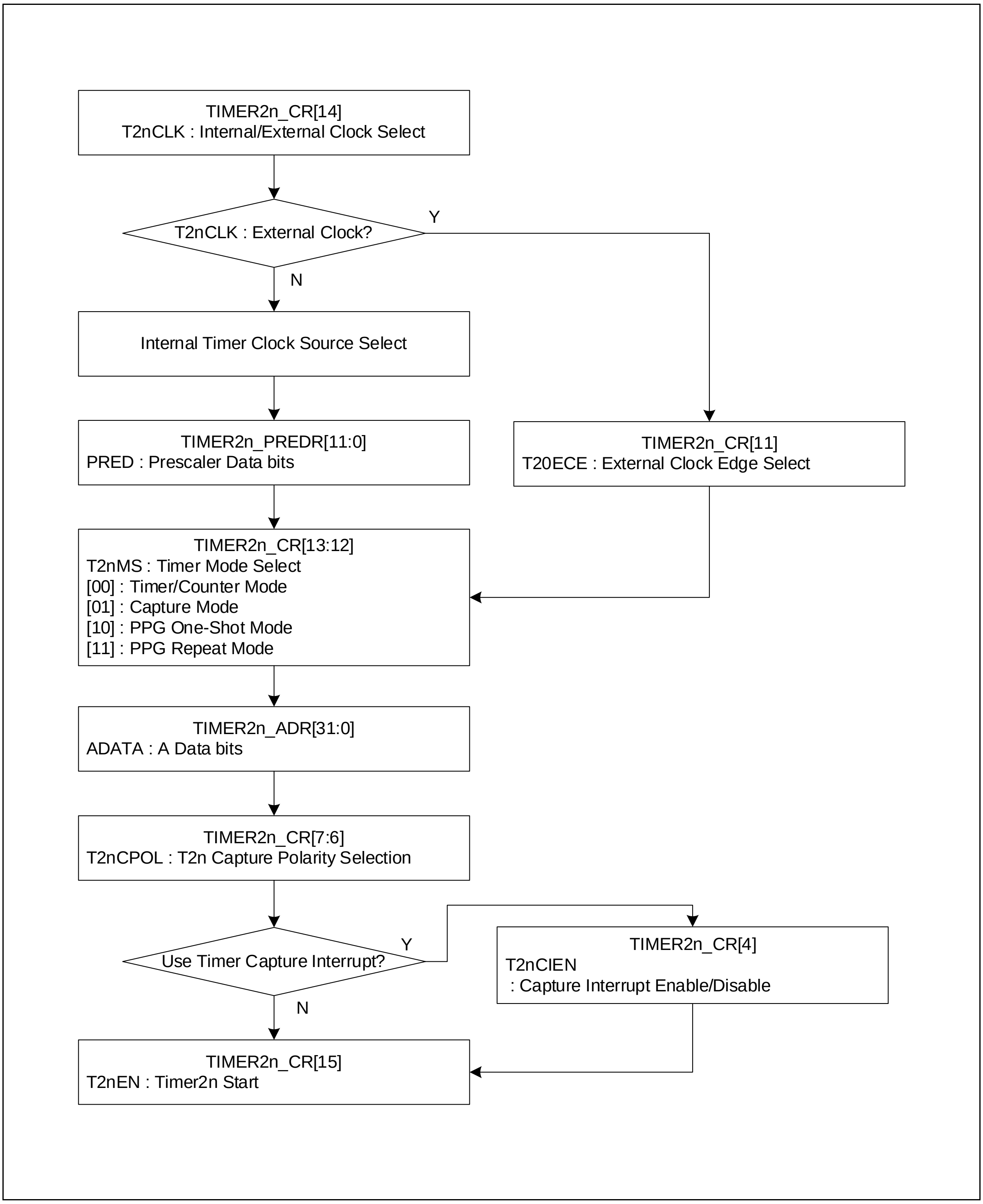
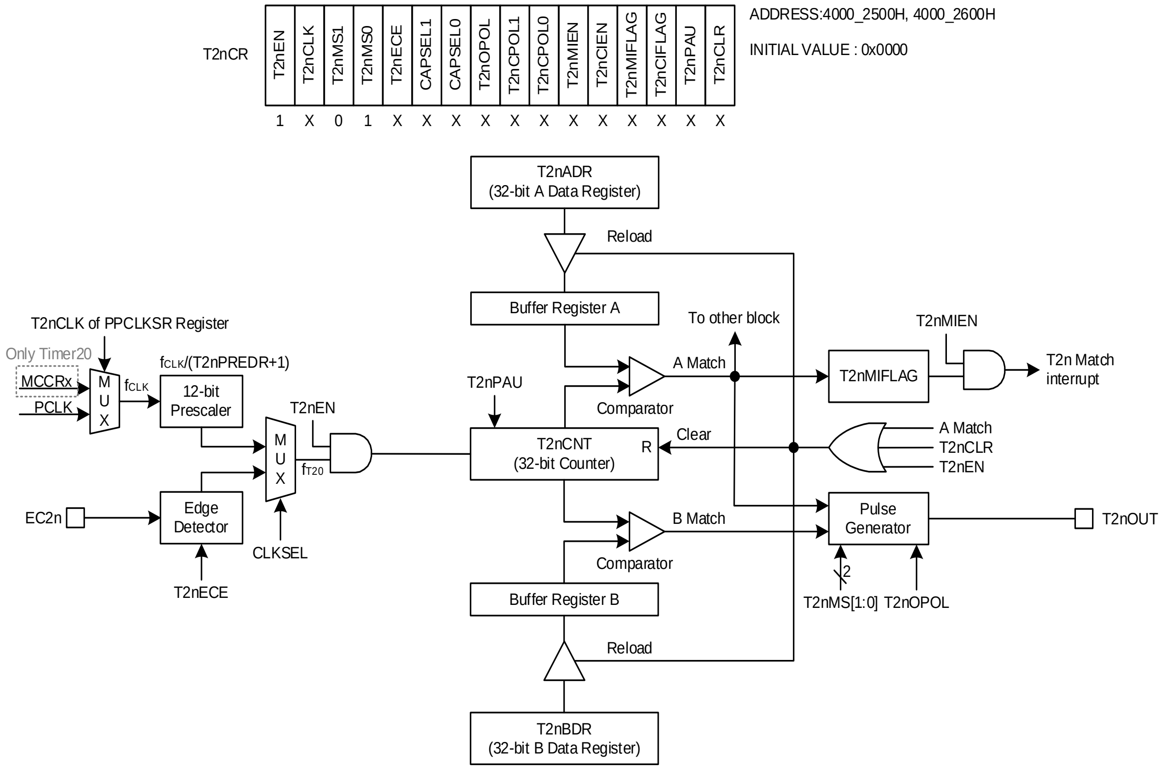

TIMER2n_CR[14]
T2nCLK : Internal/External Clock Select
T2nCLK : External Clock?
Y
N
Internal Timer Clock Source Select
TIMER2n_PREDR[11:0]
PRED : Prescaler Data bits
TIMER2n_CR[11]
T20ECE : External Clock Edge Select
TIMER2n_CR[13:12]
T2nMS : Timer Mode Select
[00] : Timer/Counter Mode
[01] : Capture Mode
[10] : PPG One-Shot Mode
[11] : PPG Repeat Mode
TIMER2n_ADR[31:0]
ADATA : A Data bits
TIMER2n_CR[7:6]
T2nCPOL : T2n Capture Polarity Selection
Use Timer Capture Interrupt?
Y
N
TIMER2n_CR[4]
T2nCIEN
: Capture Interrupt Enable/Disable
TIMER2n_CR[15]
T2nEN : Timer2n Start

Figure 59. Capture Mode Operation Sequence of TIMER2n (n = 0 or 1)

11.3.4 32-bit PPG mode

Timer 2n has a PPG (Programmable Pulse Generation) function. In PPG mode, the T2nOUT pin outputs up to 32-bit resolution PWM output. This pin should be configured as a PWM output by setting corresponding Pn_AFSRx to 'AF1'. Period of the PWM output is determined by the TIMER2n_ADR, and duty of the PWM output is determined by the TIMER2n_BDR.



NOTE: The T2nEN is automatically cleared to logic "0" after one pulse is generated at a PPG one-shot mode.

Figure 60. TIMER2n Block Diagram in PPG Mode

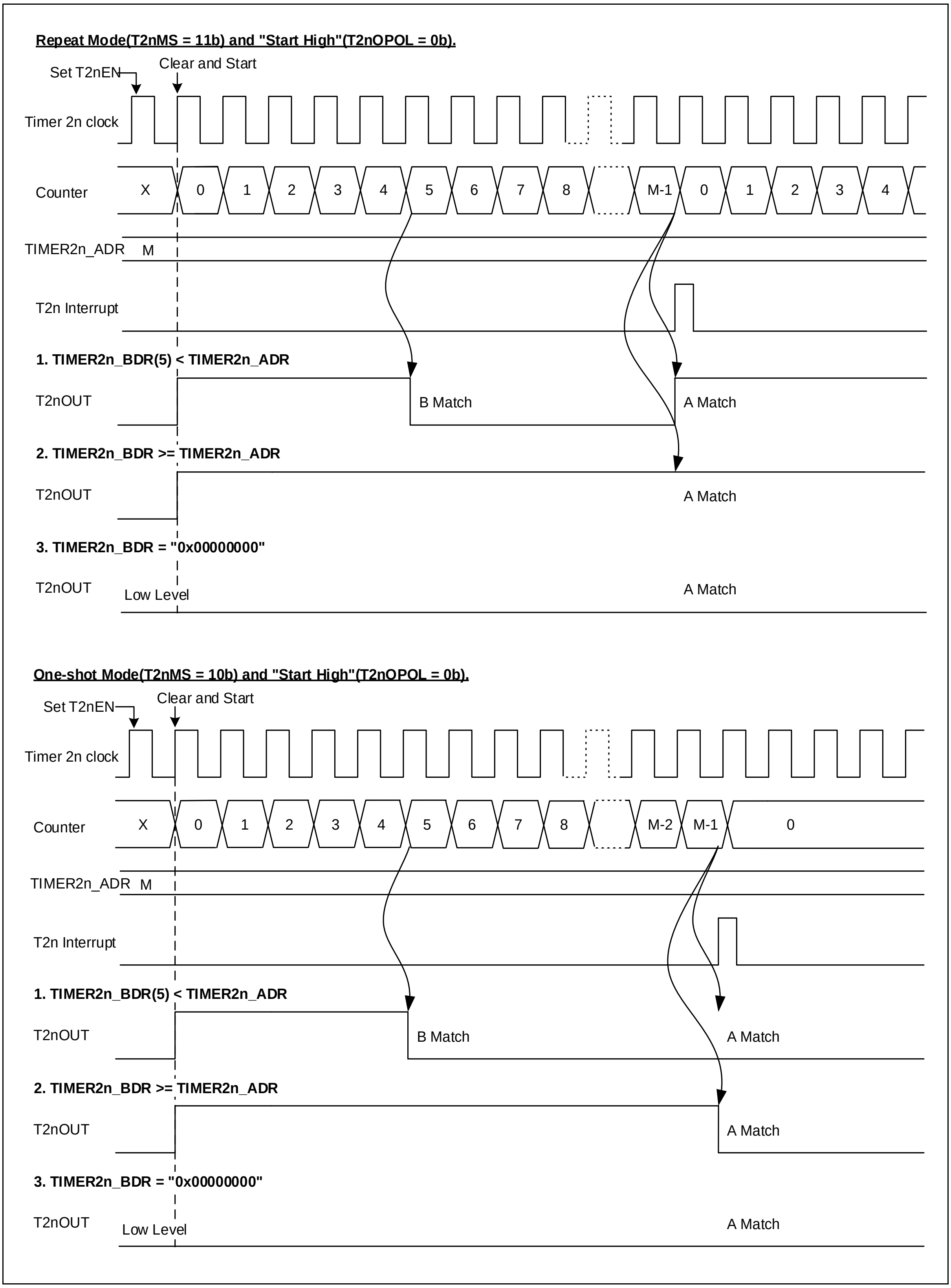

Repeat Mode(T2nMS = 11b) and "Start High"(T2nOPOL = 0b).
Set T2nEN
Clear and Start
Timer 2n clock
Counter
X
0
1
2
3
4
5
6
7
8
M-1
0
1
2
3
4
TIMER2n_ADR
M
T2n Interrupt
1. TIMER2n_BDR(5) < TIMER2n_ADR
T2nOUT
B Match
A Match
2. TIMER2n_BDR >= TIMER2n_ADR
T2nOUT
A Match
3. TIMER2n_BDR = "0x00000000"
T2nOUT
Low Level
A Match
One-shot Mode(T2nMS = 10b) and "Start High"(T2nOPOL = 0b).
Set T2nEN
Clear and Start
Timer 2n clock
Counter
X
0
1
2
3
4
5
6
7
8
M-2
M-1
0
TIMER2n_ADR
M
T2n Interrupt
1. TIMER2n_BDR(5) < TIMER2n_ADR
T2nOUT
B Match
A Match
2. TIMER2n_BDR >= TIMER2n_ADR
T2nOUT
A Match
3. TIMER2n_BDR = "0x00000000"
T2nOUT
Low Level
A Match

Figure 61. PPG Mode Timing Example of TIMER2n (n = 0 or 1)

Figure 62 shows the PPG mode operation of timer/counter 2n. Refer to **Figure 13. Clock Change Procedure** for internal timer clock source and section **5.2. Pin multiplexing** for Timer2n Output pin.

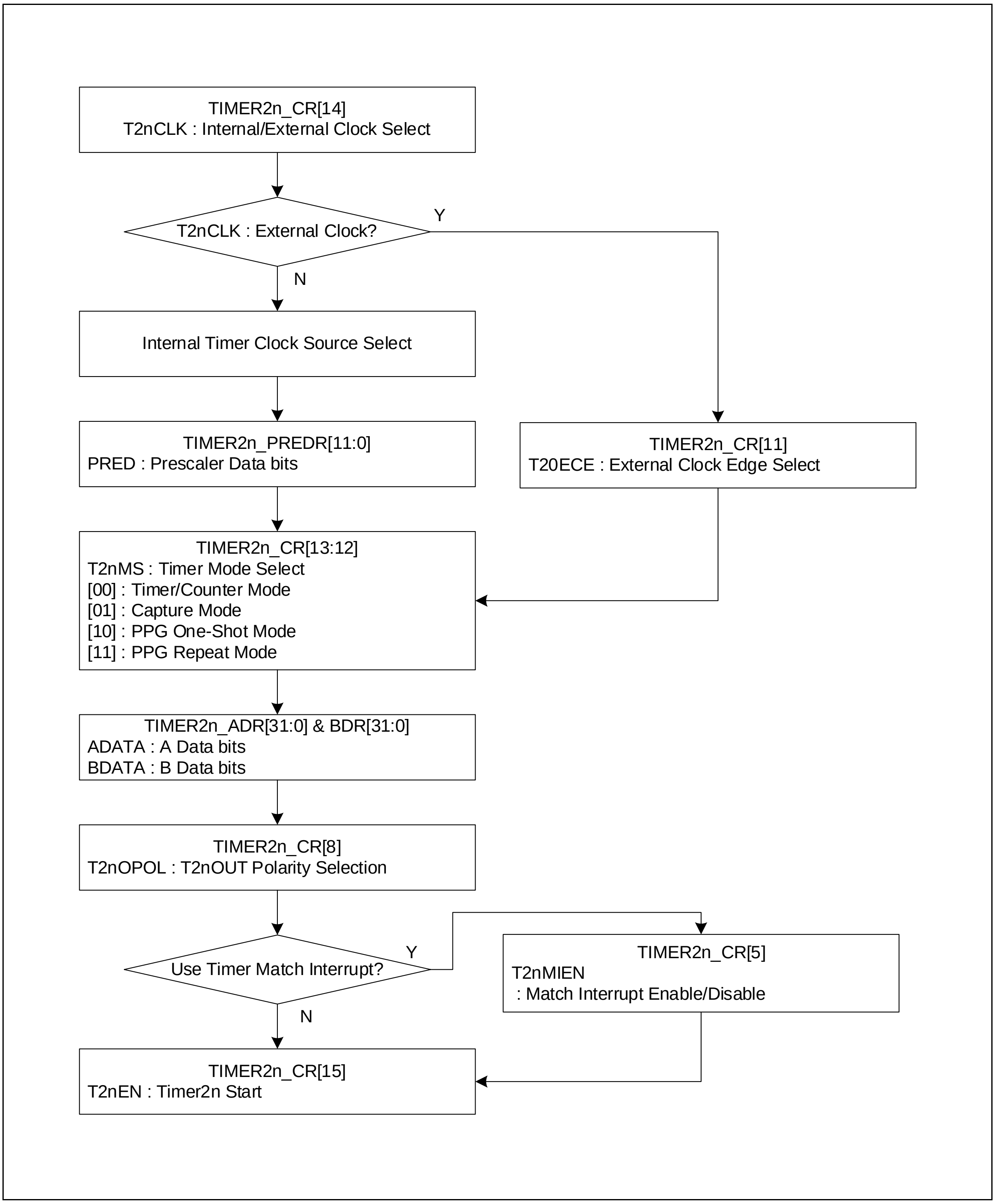

TIMER2n_CR[14]
T2nCLK : Internal/External Clock Select
T2nCLK : External Clock?
Y
N
Internal Timer Clock Source Select
TIMER2n_PREDR[11:0]
PRED : Prescaler Data bits
TIMER2n_CR[11]
T20ECE : External Clock Edge Select
TIMER2n_CR[13:12]
T2nMS : Timer Mode Select
[00] : Timer/Counter Mode
[01] : Capture Mode
[10] : PPG One-Shot Mode
[11] : PPG Repeat Mode
TIMER2n_ADR[31:0] & BDR[31:0]
ADATA : A Data bits
BDATA : B Data bits
TIMER2n_CR[8]
T2nOPOL : T2nOUT Polarity Selection
Use Timer Match Interrupt?
Y
N
TIMER2n_CR[5]
T2nMIEN
: Match Interrupt Enable/Disable
TIMER2n_CR[15]
T2nEN : Timer2n Start

Figure 62. PPG Mode Operation Sequence of TIMER2n (n = 0 or 1)

12 Timer counter 30

Timer counter 30 of A31T214/216 series consists of a multiplexer, a comparator, 16-bit sized timer data registers A/B/C, and many other registers used for its operation. Main features are listed in the followings:

- 16-bit up/down-counter
- Periodic timer mode
- Back-to-Back mode
- Capture mode
- 12-bit prescaler

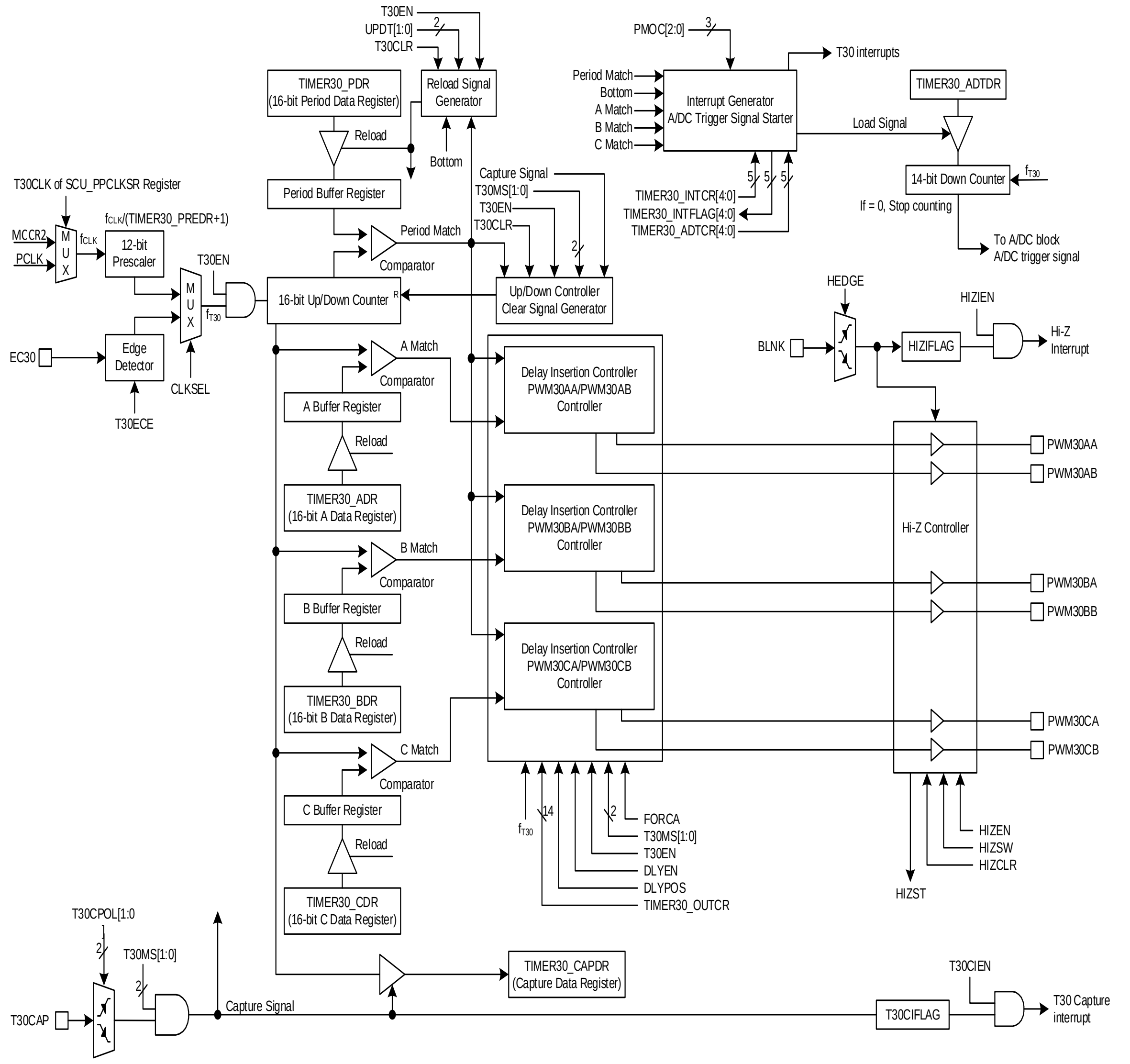
Table 39 introduces pins assigned for the timer counter 30.

Table 39. Pin Assignment of Timer Counter 30: External Pins

Pin name	Type	Description
EC30	I	External clock input
T30CAP	I	Capture input
BLNK	I	External sync signal input
PWM30AA	O	PWM output
PWM30AB	O	PWM output
PWM30BA	O	PWM output
PWM30BB	O	PWM output
PWM30CA	O	PWM output
PWM30CB	O	PWM output

12.1 Timer counter 30 block diagram

In this section, timer counter 30 is introduced in a block diagram.



NOTES:

1. The Period/A/B/C match interrupts except for Bottom can occur in the interval mode.
2. The Period match interrupt only can occur in the capture mode.
3. The 16-bit up/down counter in the capture mode is cleared to "0x0000" after the counter value is loaded to the TIMER30_CAPDR register at valid edge.
4. The HIZSW (high-impedance output software setting) bit can be used for debugging mode. That is, All T30PWM outputs can be high-impedance state with setting the HIZSW bit to '1' by the UI of debugger.
5. After the T30EN bit is set, the counting of TIMER30_CNT may be delayed 2 clocks or more.

Figure 63. Timer Counter 30 Block Diagram

12.2 Registers

Table 40 and Table 41 show base address and register map of 3-phase PWM timer 30.

Table 40. Base Address of Timer Counter 30

Name	Base address
TIMER30	0x4000_2400

Table 41. Timer Counter 30 Register Map

Name	Offset	Type	Description	Reset value	Reference
TIMER30_CR	0x0000	RW	Timer/Counter 30 Control Register	0x0000_0000	
TIMER30_PDR	0x0004	RW	Timer/Counter 30 Period Data Register	0x0000_FFFF	
TIMER30_ADR	0x0008	RW	Timer/Counter 30 A Data Register	0x0000_FFFF	
TIMER30_BDR	0x000C	RW	Timer/Counter 30 B Data Register	0x0000_FFFF	
TIMER30_CDR	0x0010	RW	Timer/Counter 30 C Data Register	0x0000_FFFF	
TIMER30_CAPDR	0x0014	RO	Timer/Counter 30 Capture Data Register	0x0000_0000	
TIMER30_PREDR	0x0018	RW	Timer/Counter 30 Prescaler Data Register	0x0000_0FFF	
TIMER30_CNT	0x001C	RO	Timer/Counter 30 Counter Register	0x0000_0000	
TIMER30_OUTCR	0x0020	RW	Timer/Counter 30 Output Control Register	0x0000_0000	
TIMER30_DLY	0x0024	RW	Timer/Counter 30 PWM Output Delay Data Register	0x0000_0000	
TIMER30_INTCR	0x0028	RW	Timer/Counter 30 Interrupt Control Register	0x0000_0000	
TIMER30_INTFLAG	0x002C	RW	Timer/Counter 30 Interrupt Flag Register	0x0000_0000	
TIMER30_HIZCR	0x0030	RW	Timer/Counter 30 High-Impedance Control Register	0x0000_0000	
TIMER30_ADTCR	0x0034	RW	Timer/Counter 30 A/DC Trigger Control Register	0x0000_0000	
TIMER30_ADTDR	0x0038	RW	Timer/Counter 30 A/DC Trigger Generator Data Register	0x0000_0000	

12.2.1 TIMER30_CR: timer/counter 30 control register

Timer module should be configured properly before running. When target purpose is defined, the timer can be configured in this register. After configuring this register, you can start or stop the timer function by TIMER30_CR register.

The TIMER30_CR is a 32-bit register with 32/16/8-bit access.

TIMER30_CR=0x4000_2400

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15	14	13 12	11	10	9	8	7 6	5 4	3 2 1	0
Reserved	T30EN	T30CLK	T30MS	T30ECE	FORCA	DLYEN	DLYPOS	T30CPOL	UPDT	PMOC	T30CLR
-	0	0	00	0	0	0	0	00	00	000	0
-	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

15	T30EN	Timer 30 Operation Enable bit.	
		0	Disable timer 30 operation.
		1	Enable timer 30 operation. (Counter clear and start)
14	T30CLK	Timer 30 Clock Selection bit.	
		0	Select an internal prescaler clock.
		1	Select an external clock.
NOTES: 1. This bit should be changed during T30EN bit is “0b”. 2. If you select an internal prescaler clock, you should set T30CLK bit in the SCU_PPCLKSR register first.			
13 12	T30MS	Timer 30 Operation Mode Selection bits.	
		00	Interval mode. (All match interrupts can occur)
		01	Capture mode. (The Period-match interrupt can occur)
		10	Back-to-back mode. (All interrupts can occur)
		11	Not used.
		NOTE: This bit should be changed during T30EN bit is “0b”.	
11	T30ECE	Timer 30 External Clock Edge Selection bit.	
		0	Select falling edge of external clock.
		1	Select rising edge of external clock.
10	FORCA	Timer 30 Output Mode Selection bit. This bit should be changed when the T30EN is “0b”.	
		0	6-Channel mode (The PWM30xA/PWM30xB pins are output according to the TIMER30_xDR registers, respectively)
		1	Force A-Channel mode (All PWM30xA/PWM30xB pins are output according to the only TIMER30_ADR registers.)
9	DLYEN	Delay Time Insertion Enable bit.	
		0	Disable to insert delay time to the PWM30xA/PWM30xB.
		1	Enable to insert delay time to the PWM30xA/PWM30xB.
8	DLYPOS	Delay Time Insertion Position.	
		0	Insert at front of PWM30xA and at back of PWM30xB pins.
		1	Insert at back of PWM30xA and at front of PWM30xB pins.
7 6	T30CPOL	Timer 30 Capture Polarity Selection bits.	
		00	Capture on falling edge.
		01	Capture on rising edge.

		10	Capture on both of falling and rising edge.
		11	Reserved
5 4	UPDT	Data Reload Time Selection bits.	
		00	Update data to buffer at the time of writing.
		01	Update data to buffer at period match.
		10	Update data to buffer at bottom.
		11	Not used.
3 1	PMOC	Period Match Interrupt Occurrence Selection.	
		000	Once every period match.
		001	Once every 2 period match.
		010	Once every 3 period match.
		011	Once every 4 period match.
		100	Once every 5 period match.
		101	Once every 6 period match.
		110	Once every 7 period match.
		111	Once every 8 period match.
NOTES: 1. A period match counter is cleared as 0x00 when the T30CLR bit is set. 2. When changing the PMOC value, must clear the period match counter with T30CLR. Otherwise, malfunction may occur.			
0	T30CLR	Timer 30 Counter and Prescaler Clear bit.	
		0	No effect.
		1	Clear timer 30 counter and prescaler (Automatically cleared to "0b" after operation)

12.2.2 TIMER30_PDR: timer/counter 30 period data register

The TIMER30_PDR is a 32-bit register with 32/16/8-bit access.

TIMER30_PDR=0x4000_2404

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved		PDATA	
-		0xFFFF	
-		RW	

15 0	PDATA	Timer/Counter 30 Period Data bits. The range is 0x0002 to 0xFFFF.
NOTE: Do not write "0x0000" in the TIMER30_PDR register when PPG mode.		

12.2.3 TIMER30_ADR: timer/counter 30 A data register

The TIMER30_ADR is a 32-bit register with 32/16/8-bit access.

TIMER30_ADR=0x4000_2408

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved		ADATA	
-		0xFFFF	
-		RW	

15 0	ADATA	Timer/Counter 30 A Data bits. The range is 0x0000 to 0xFFFF.

12.2.4 TIMER30_BDR: timer/counter 30 B data register

The TIMER30_BDR is a 32-bit register with 32/16/8-bit access.

TIMER30_BDR=0x4000_240C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved		BDATA	
-		0xFFFF	
-		RW	

15 0	BDATA	Timer/Counter 30 B Data bits. The range is 0x0000 to 0xFFFF.

12.2.5 TIMER30_CDR: timer/counter 30 C data register

The TIMER30_CDR is a 32-bit register with 32/16/8-bit access.

TIMER30_CDR=0x4000_2410

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																CDATA															
-																0xFFFF															
-																RW															

15 0	CDATA	Timer/Counter 30 C Data bits. The range is 0x0000 to 0xFFFF.

12.2.6 TIMER30_CAPDR: timer/counter 30 capture data register

The TIMER30_CAPDR is a 32-bit register with 32/16/8-bit access.

TIMER30_CAPDR=0x4000_2414

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																CAPD															
-																0x0000															
-																RO															

15 0	CAPD	Timer/Counter 30 Capture Data bits.

12.2.7 TIMER30_PREDR: timer/counter 30 prescaler data register

The TIMER30_PREDR is a 32-bit register with 32/16/8-bit access.

TIMER30_PREDR=0x4000_2418

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				PRED											
-																				0xFFF											
-																				RW											

11 0	PRED	Timer/Counter 30 Prescaler Data bits.

12.2.8 TIMER30_CNT: timer/counter 30 counter register

The TIMER30_CNT is a 32-bit register with 32/16/8-bit access.

TIMER30_CNT=0x4000_241C

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="16">Reserved</td><td colspan="16">CNT</td></tr>
<tr><td colspan="16">-</td><td colspan="16">0x0000</td></tr>
<tr><td colspan="16">-</td><td colspan="16">RO</td></tr>
</table>

15 0	CNT	Timer/Counter 30 Counter bits.

12.2.9 TIMER30_OUTCR: timer/counter 30 output control register

The TIMER30_OUTCR is a 32-bit register with 32/16/8-bit access.

TIMER30_OUTCR=0x4000_2420

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WTIDKY		POLB	POLA	PABOE	PBBOE	PCBOE	PAAOE	PBAOE	PCAOE	Reserved	LVLAB	LVLBB	LVLCB	Reserved	LVLAA	LVLBA	LVLCA
0x0000		0	0	0	0	0	0	0	0	-	0	0	0	-	0	0	0
WO		RW	RW	RW	RW	RW	RW	RW	RW	-	RW	RW	RW	-	RW	RW	RW

31 16	WTIDKY	Write Identification Key.	
		On writes, write 0xE06C to these bits, otherwise the write is ignored.	
15	POLB	PWM30xB Output Polarity Selection bit. (x: A, B and C)	
		0	Low level start. (The PWM30xB pins are started with low level after counting)
		1	High level start. (The PWM30xB pins are started with high level after counting)
14	POLA	PWM30xA Output Polarity Selection bit. (x: A, B and C)	
		0	Low level start. (The PWM30xA pins are started with low level after counting)
		1	High level start. (The PWM30xA pins are started with high level after counting)
13	PABOE	PWM30AB Output Enable bit.	
		0	Disable output.
		1	Enable output.
12	PBBOE	PWM30BB Output Enable bit.	
		0	Disable output.
		1	Enable output.
11	PCBOE	PWM30CB Output Enable bit.	
		0	Disable output.
		1	Enable output.
10	PAAOE	PWM30AA Output Enable bit.	
		0	Disable output.
		1	Enable output.
9	PBAOE	PWM30BA Output Enable bit.	
		0	Disable output.
		1	Enable output.
8	PCAOE	PWM30CA Output Enable bit.	
		0	Disable output.
		1	Enable output.
6	LVLAB	Configure PWM30AB output When Disable.	
		0	Low level
		1	High level
5	LVLBB	Configure PWM30BB output When Disable.	
		0	Low level
		1	High level
4	LVLCB	Configure PWM30CB output When Disable.	

		0	Low level
		1	High level
2	LVLAA	Configure PWM30AA output When Disable.	
		0	Low level
		1	High level
1	LVLBA	Configure PWM30BA output When Disable.	
		0	Low level
		1	High level
0	LVLCA	Configure PWM30CA output When Disable.	
		0	Low level
		1	High level

12.2.10 TIMER30_DLY: timer/counter 30 PWM output delay data register

The TIMER30_DLY is a 32-bit register with 32/16/8-bit access.

TIMER30_DLY=0x4000_2424

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																						DLY									
-																						0x000									
-																						RW									

9 0	DLY	Timer/Counter 30 PWM Delay Data bits. Delay time: (DLY[9:0]+1)÷fT30

12.2.11 TIMER30_INTCR: timer/counter 30 interrupt control register

The TIMER30_INTCR is a 32-bit register with 32/16/8-bit access.

TIMER30_INTCR=0x4000_2428

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																									HIZIEN	T30CIEN	T30BTIEN	T30PMIEN	T30AMIEN	T30BMIEN	T30CMIEN
-																									0	0	0	0	0	0	0
-																									RW	RW	RW	RW	RW	RW	RW

6	HIZIEN	Timer 30 Output High-Impedance Interrupt Enable bit.	
		0	Disable timer 30 output high-impedance interrupt.
		1	Enable timer 30 output high-impedance interrupt.
5	T30CIEN	Timer 30 Capture Interrupt Enable bit.	
		0	Disable timer 30 capture interrupt.
		1	Enable timer 30 capture interrupt.
4	T30BTIEN	Timer 30 Bottom Interrupt Enable bit.	
		0	Disable timer 30 period interrupt.
		1	Enable timer 30 period interrupt.
3	T30PMIEN	Timer 30 Period Match Interrupt Enable bit.	
		0	Disable timer 30 period interrupt.
		1	Enable timer 30 period interrupt.
2	T30AMIEN	Timer 30 A-ch Match Interrupt Enable bit.	
		0	Disable timer 30 A-ch match interrupt.
		1	Enable timer 30 A-ch match interrupt.
1	T30BMIEN	Timer 30 B-ch Match Interrupt Enable bit.	
		0	Disable timer 30 B-ch match interrupt.
		1	Enable timer 30 B-ch match interrupt.
0	T30CMIEN	Timer 30 C-ch Match Interrupt Enable bit.	
		0	Disable timer 30 C-ch match interrupt.
		1	Enable timer 30 C-ch match interrupt.

12.2.12 TIMER30_INTFLAG: timer/counter 30 interrupt flag register

The TIMER30_INTFLAG is a 32-bit register with 32/16/8-bit access.

TIMER30_INTFLAG=0x4000_242C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Reserved				HIZIFLAG	T30CIFLAG	T30BTIFLAG	T30PMIFLAG	T30AMIFLAG	T30BMIFLAG	T30CMIFLAG
-				0	0	0	0	0	0	0
-				RW	RW	RW	RW	RW	RW	RW

6	HIZIFLAG	Timer 30 Output High-Impedance Interrupt Flag bit.	
		0	No request occurred.
		1	Request occurred, This bit is cleared to '0' when write '1'.
5	T30CIFLAG	Timer 30 Capture Interrupt Flag bit.	
		0	No request occurred.
		1	Request occurred, This bit is cleared to '0' when write '1'.
4	T30BTIFLAG	Timer 30 Bottom Interrupt Flag bit.	
		0	No request occurred.
		1	Request occurred, This bit is cleared to '0' when write '1'.
3	T30PMIFLAG	Timer 30 Period Match Flag Enable bit.	
		0	No request occurred.
		1	Request occurred, This bit is cleared to '0' when write '1'.
2	T30AMIFLAG	Timer 30 A-ch Match Interrupt Flag bit.	
		0	No request occurred.
		1	Request occurred, This bit is cleared to '0' when write '1'.
1	T30BMIFLAG	Timer 30 B-ch Match Interrupt Flag bit.	
		0	No request occurred.
		1	Request occurred, This bit is cleared to '0' when write '1'.
0	T30CMIFLAG	Timer 30 C-ch Match Interrupt Flag bit.	
		0	No request occurred.
		1	Request occurred, This bit is cleared to '0' when write '1'.

12.2.13 TIMER30_HIZCR: timer/counter 30 high-impedance control register

The TIMER30_HIZCR is a 32-bit register with 32/16/8-bit access.

TIMER30_HIZCR=0x4000_2430

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Reserved			HIZEN	Reserved		HIZSW	Reserved	HEDGE	HIZSTA	HIZCLR
-			0	-		0	-	0	0	0
-			RW	-		RW	-	RW	RO	RW

7	HIZEN	PWM30xA/PWM30xB Output High-Impedance Enable bit.	
		0	Disable to control the output high-impedance.
		1	Enable to control the output high-impedance.
4	HIZSW	High-Impedance Output Software Setting.	
		0	No effect.
		1	PWM30xA/PWM30xB pins go into high impedance. (Automatically cleared to “0b” after operation)
2	HEDGE	High-Impedance Edge Selection.	
		0	Falling edge of the BLNK30 pin.
		1	Rising edge of the BLNK30 pin.
1	HIZSTA	High-Impedance Status.	
		0	Indicates that the pins are not under a Hi-Z state.
		1	Indicates that the pins are under a Hi-Z state.
0	HIZCLR	High-Impedance Output Clear bit.	
		0	No effect.
		1	Clear high-impedance output. (The PWM30xA/PWM30xB pins are back to output and this bit is automatically cleared to “0b” after operation)
NOTE: Where x = A, B, and C.			

12.2.14 TIMER30_ADTCR: timer/counter 30 A/DC trigger control register

The TIMER30_ADTCR is a 32-bit register with 32/16/8-bit access.

TIMER30_ADTCR=0x4000_2434

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5	4	3	2	1	0
Reserved				T30BTTG	T30PMTG	T30AMTG	T30BMTG	T30CMTG
-				0	0	0	0	0
-				RW	RW	RW	RW	RW

4	T30BTTG	Select Timer 30 Bottom for A/DC Trigger Signal Generator.	
		0	Disable A/DC trigger signal generator by bottom.
		1	Enable A/DC trigger signal generator by bottom.
3	T30PMTG	Select Timer 30 Period Match for A/DC Trigger Signal Generator.	
		0	Disable A/DC trigger signal generator by period match.
		1	Enable A/DC trigger signal generator by period match.
2	T30AMTG	Select Timer 30 A-ch Match for A/DC Trigger Signal Generator.	
		0	Disable A/DC trigger signal generator by A-ch match.
		1	Enable A/DC trigger signal generator by A-ch match.
1	T30BMTG	Select Timer 30 B-ch Match for A/DC Trigger Signal Generator.	
		0	Disable A/DC trigger signal generator by B-ch match.
		1	Enable A/DC trigger signal generator by B-ch match.
0	T30CMTG	Select Timer 30 C-ch Match for A/DC Trigger Signal Generator.	
		0	Disable A/DC trigger signal generator by C-ch match.
		1	Enable A/DC trigger signal generator by C-ch match.

NOTES:

1. A trigger signal generation is not related with the PMOC[2:0] bits of TIMER30_CR register.
2. If several source for trigger is selected, a signal can be lost in case of the trigger generation counter is reloaded by another signal.

12.2.15 TIMER30_ADTDR: timer/counter 30 A/DC trigger generator data register

The TIMER30_ADTDR is a 32-bit register with 32/16/8-bit access.

TIMER30_ADTDR=0x4000_2438

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14	13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved			ADTDATA	
-			0x0000	
-			RW	

13 0	CNT	Timer/Counter 30 A/DC Trigger Generation Data bits.

NOTES:

1. ADTDR of Timer30 uses the adcnt timer as tclk (timer30 clock).
2. The adcnt timer counter is a 14-bit down counter.

3. It count down from the value written in ADTDR to 0. (Delay role).

12.3 Functional description

12.3.1 Timer counter 30

The timer/counter 30 can be clocked by an internal or an external clock source (EC30). The clock source is selected by a clock selection logic which is controlled by the clock selection bits (T30CLK).

- TIMER 30 clock source: {PCLK/(TIMER30_PREDR +1), EC30

In capture mode, by T30CAP, data is captured into input capture data register (TIMER30_CAPDR).

The PWM wave form to PWM30AA, PWM30AB, PWM30BA, PWM30BB, PWM30CA, PWM3CB Port (6-channel).

Table 42. Timer 30 Operating Modes

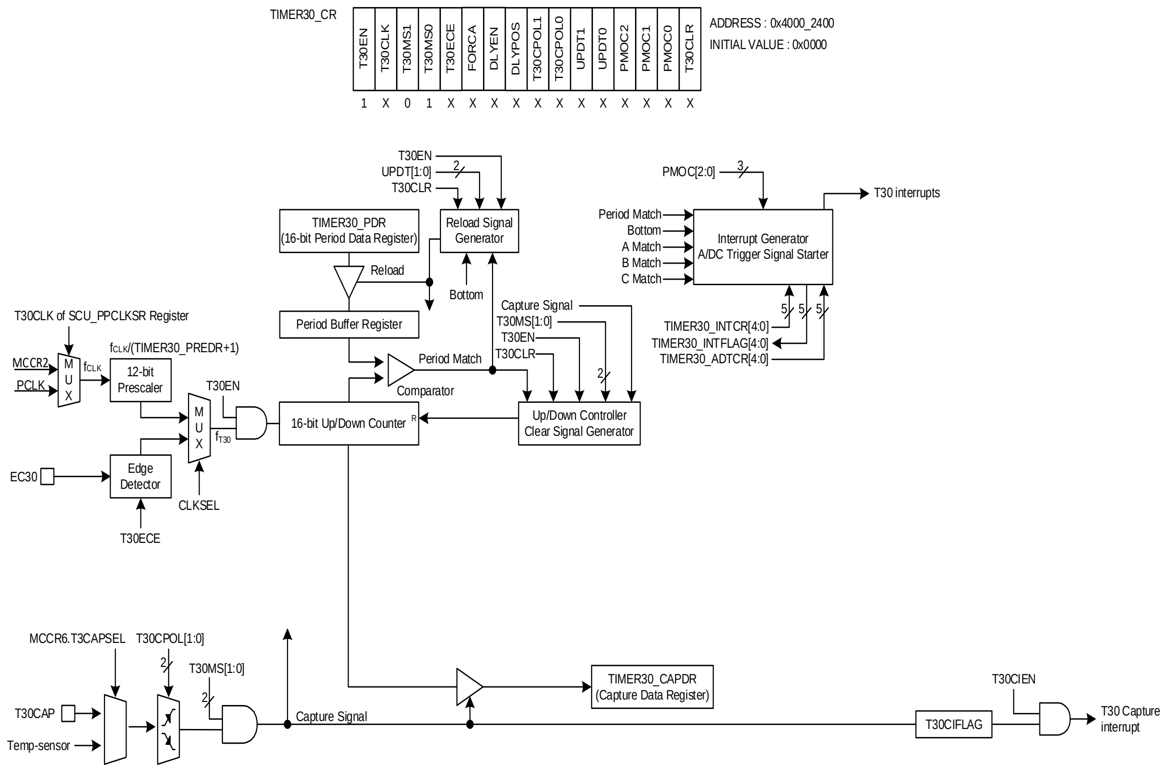
T30EN	Alternative mode	T30MS[1:0]	TIMER30_PREDR	Timer 30 mode
1	AF1	00	0xXXX	16-bit Interval Mode
1	AF1 or AF2	01	0xXXX	16-bit Capture Mode
1	AF1	10	0xXXX	16-bit back-to-back Mode

12.3.2 Timer 30 capture mode

16-bit timer 30 capture mode is set by configuring T30MS[1:0] as '01'. An internal clock input or an external clock input can be used as a clock source. Basically, the 16-bit timer 30 capture mode has the same function as the 16-bit interval mode has. Interrupts occur when value of TIMER30's 16-bit up/down counter equals to the one of TIMER30_PDR. The 16-bit up/down counter values are automatically cleared by a match signal. It can be cleared by software (T30CLR) too.

The 16-bit timer 30's interrupt in capture mode is very useful when the pulse width of captured signal is wider than the maximum period of the timer. The capture result is loaded into TIMER30_CAPDR.

Figure 64 shows 16-bit capture mode of the timer 30.



NOTES:

1. The Period match only can occur in the capture mode.
2. The 16-bit up/down counter in the capture mode is cleared to "0x0000" after the counter value is loaded to the TIMER30_CAPDR register at valid edge.

Figure 64. 16-bit Capture Mode of Timer 30

Figure 65 shows the capture mode operation of 32-bit Timer30. Refer to **Figure 13. Clock Change Procedure** for internal timer clock source and section **5.2. Pin multiplexing** for Timer 30 capture pin.

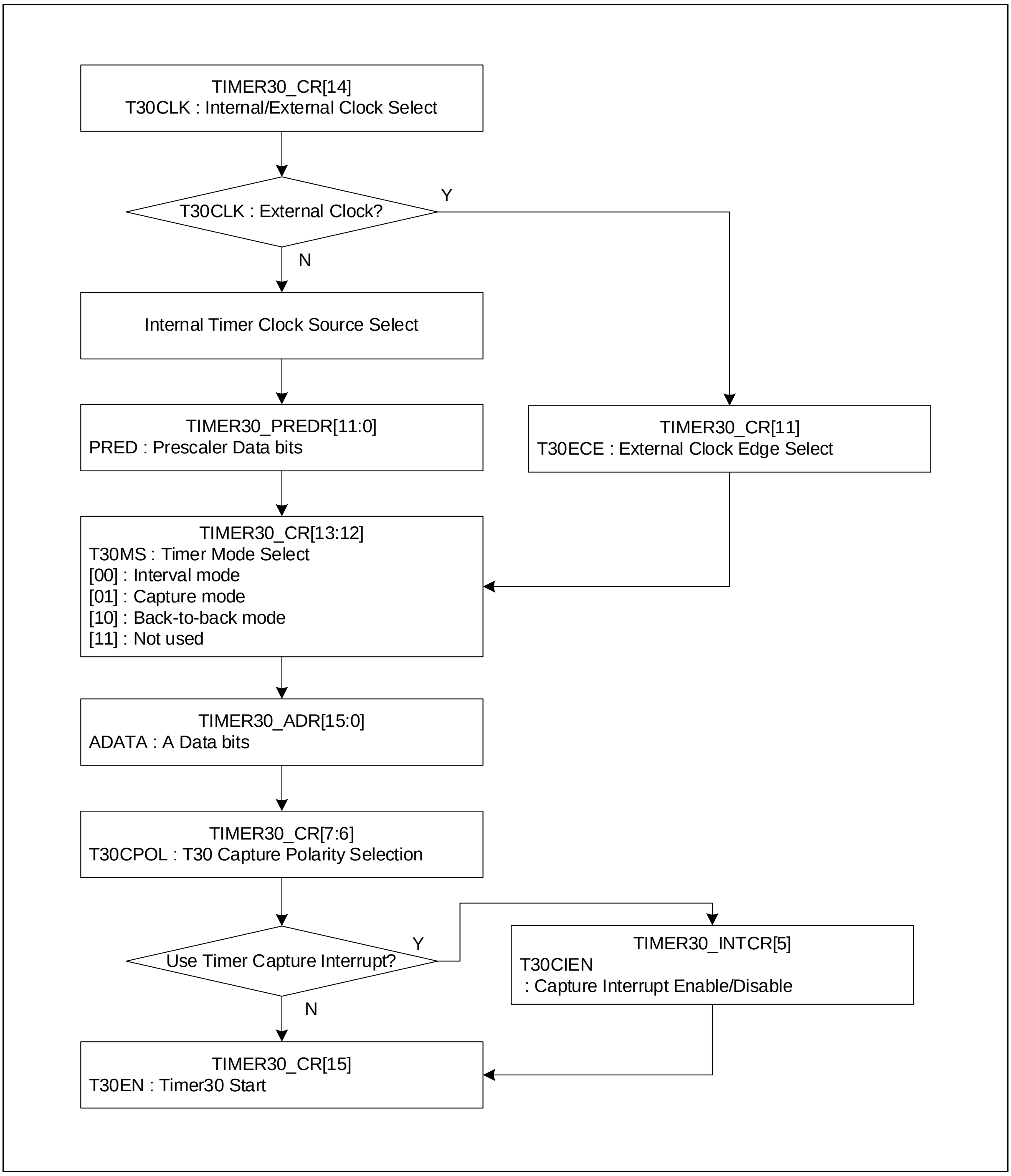


Figure 65. Capture Mode Operation Sequence of TIMER 30

12.3.3 Timer 30 interval mode

Timer 30 interval mode is determined by setting the T30MS[1:0] to '00'. The timer 30 has a counter and data registers. The 16-bit up/down counter is increased by an internal or an external clock input. The timer 30 can use the input clock with 12-bit prescaler division rates (TIMER30_PREDR[11:0]). When the value of TIMER30 16-bit up/down counter and the value of TIMER30_PDR are identical in timer 30, a match signal is generated and the period match interrupt of timer 30 is occurred. The period match interrupt can be occurred which once every 1, 2, 3, 4, 5, 6, 7, or 8 period match (PMOC[2:0]). The 16-bit up/down counter value is automatically cleared by match signal. It can be cleared by software (T30CLR) too.

The timer 30 Interval mode can be operated for BLDC motor control. It has 6-channel pins output up to 16-bit resolution PWM output. When the value of 16-bit up/down counter and TIMER30_PDR are identical in timer 30, a period match signal is generated and the period match interrupt of timer 30 is occurred.

The timer 30 A, B, and C match signals are generated and the A, B, and C match interrupts of timer 30 are occurred, when the 16-bit counter value are identical to the value of TIMER30_xDR. The period and duty of the PWM output is determined by the TIMER30_PDR (PWM period register), and T3xDR (each channel PWM duty register).

- PWM Period = [TIMER30_PDR] X Source Clock
- PWM Duty(A-ch) = [TIMER30_ADR] X Source Clock
- PWM Duty(B-ch) = [TIMER30_BDR] X Source Clock
- PWM Duty(C-ch) = [TIMER30_CDR] X Source Clock

The POLA/POLB bit of TIMER30_OUTCR register decides the polarity of PWM output. If the POLA/POLB bit is set to '1b', the PWM30xA/PWM30xB output is high level start, respectively. And if the POLA/POLB bit is cleared to '0b', the PWM30xA/PWM30xB output is low level start, respectively.

Table 43. PWM Channel Polarity

PxAOE	PxBOE	POLxA	POLxB	PWM3xA Pin put	PWM3xB Pin Output
1	1	0	0	Low level start	Low level start
		0	1	Low level start	High level start
		1	0	High level start	Low level start
		1	1	High level start	High level start

NOTE: Where x = A, B, and C.

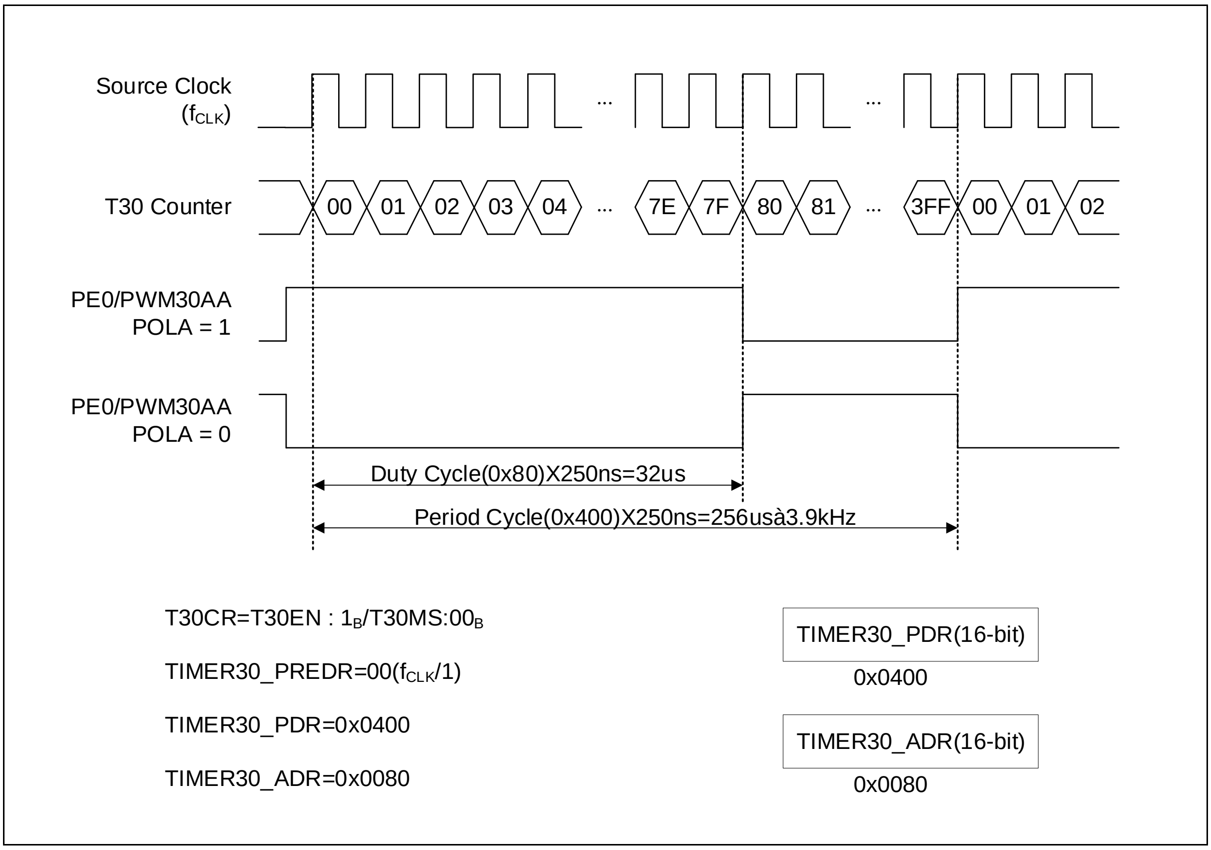
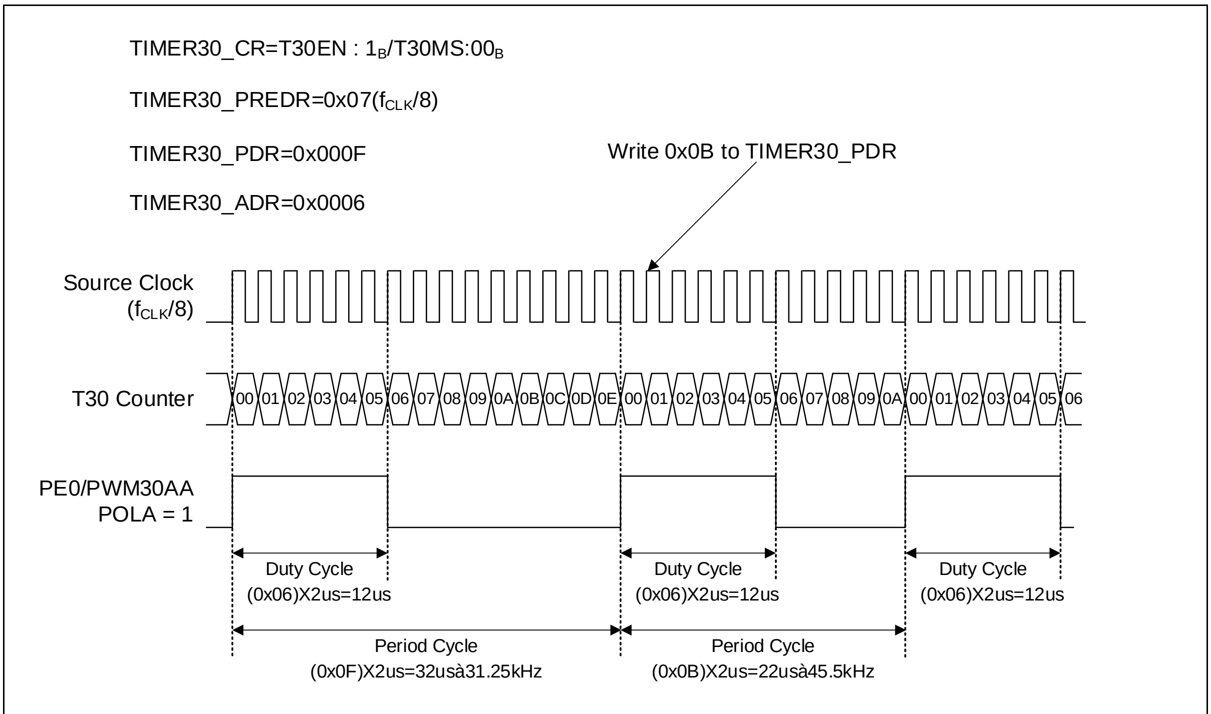

Source Clock
(f_{CLK})
T30 Counter
00 01 02 03 04 ... 7E 7F 80 81 ... 3FF 00 01 02
PE0/PWM30AA
POLA = 1
PE0/PWM30AA
POLA = 0
Duty Cycle(0x80)X250ns=32us
Period Cycle(0x400)X250ns=256usà3.9kHz
T30CR=T30EN : 1_B/T30MS:00_B
TIMER30_PREDR=00(f_{CLK}/1)
TIMER30_PDR=0x0400
TIMER30_ADR=0x0080
TIMER30_PDR(16-bit)
0x0400
TIMER30_ADR(16-bit)
0x0080

Figure 66. Example of PWM at 4MHZ



NOTE: The example shows when data reload time is chosen as the time of writing mode (UPDT[1:0] = "00b").

Figure 67. Example of Changing the Period in Absolute Duty Cycle at 4MHz

Data reload time selection

The data reload time can choose among “update data to buffer at the time of writing”, “update data to buffer at period match”, or “update data to buffer at bottom”.

PWM output delay

If using the DLYEN bit, DLYPOS bit, and TIMER30_DLY register, it can delay the PWM output. The DLYPOS setting to ‘0’, the delay inserts at front of PWM30xA and at back of PWM30xB pins. The DLYPOS setting to ‘1’, the delay inserts at back of PWM30xA and at front of PWM30xB pins. The settings of DLYEN bit, DLYPOS bit, and TIMER30_DLY register are applied equally to all PWM channels.

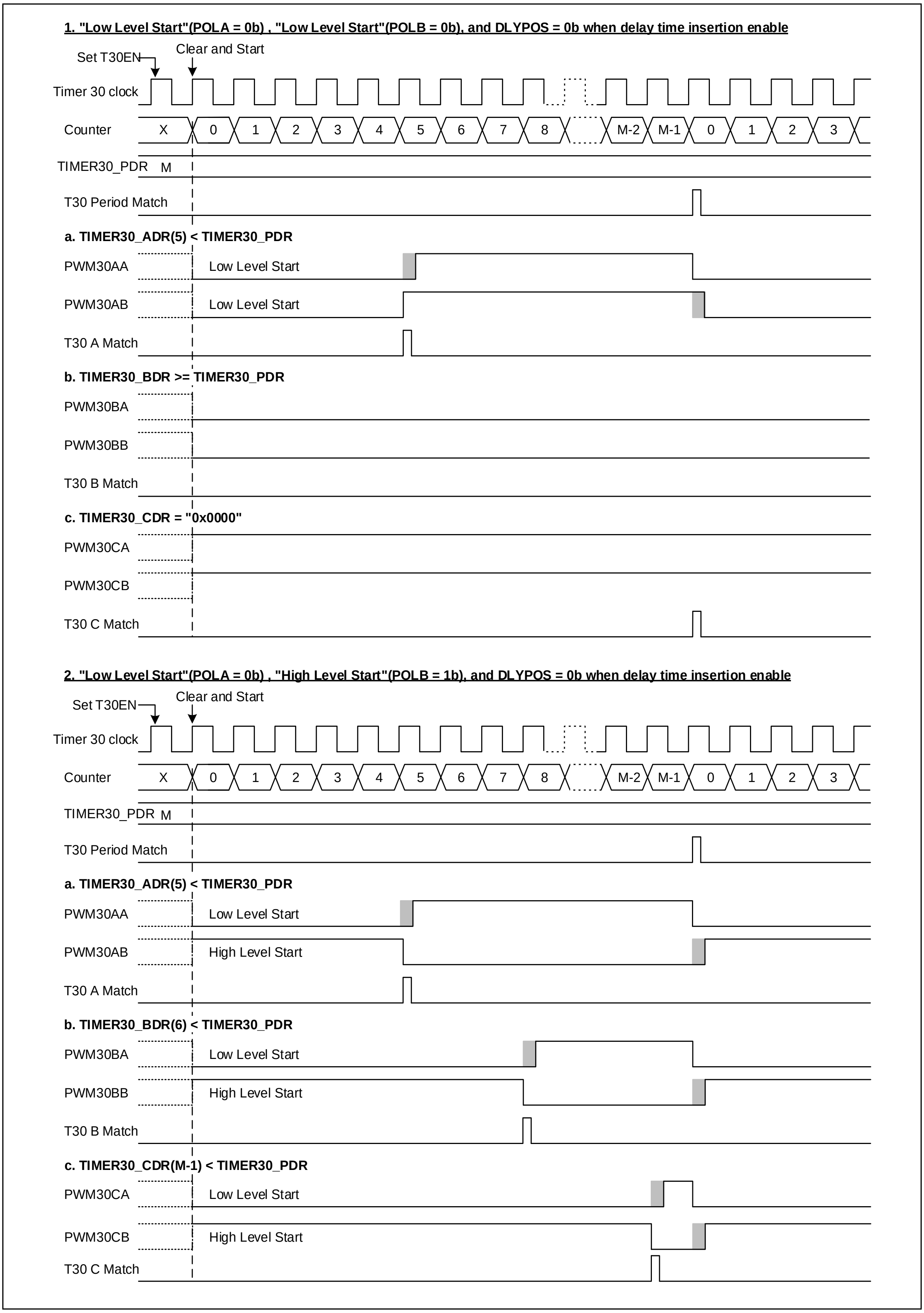


Figure 68. Interval Mode Timing Chart With "DLYPOS = 0"

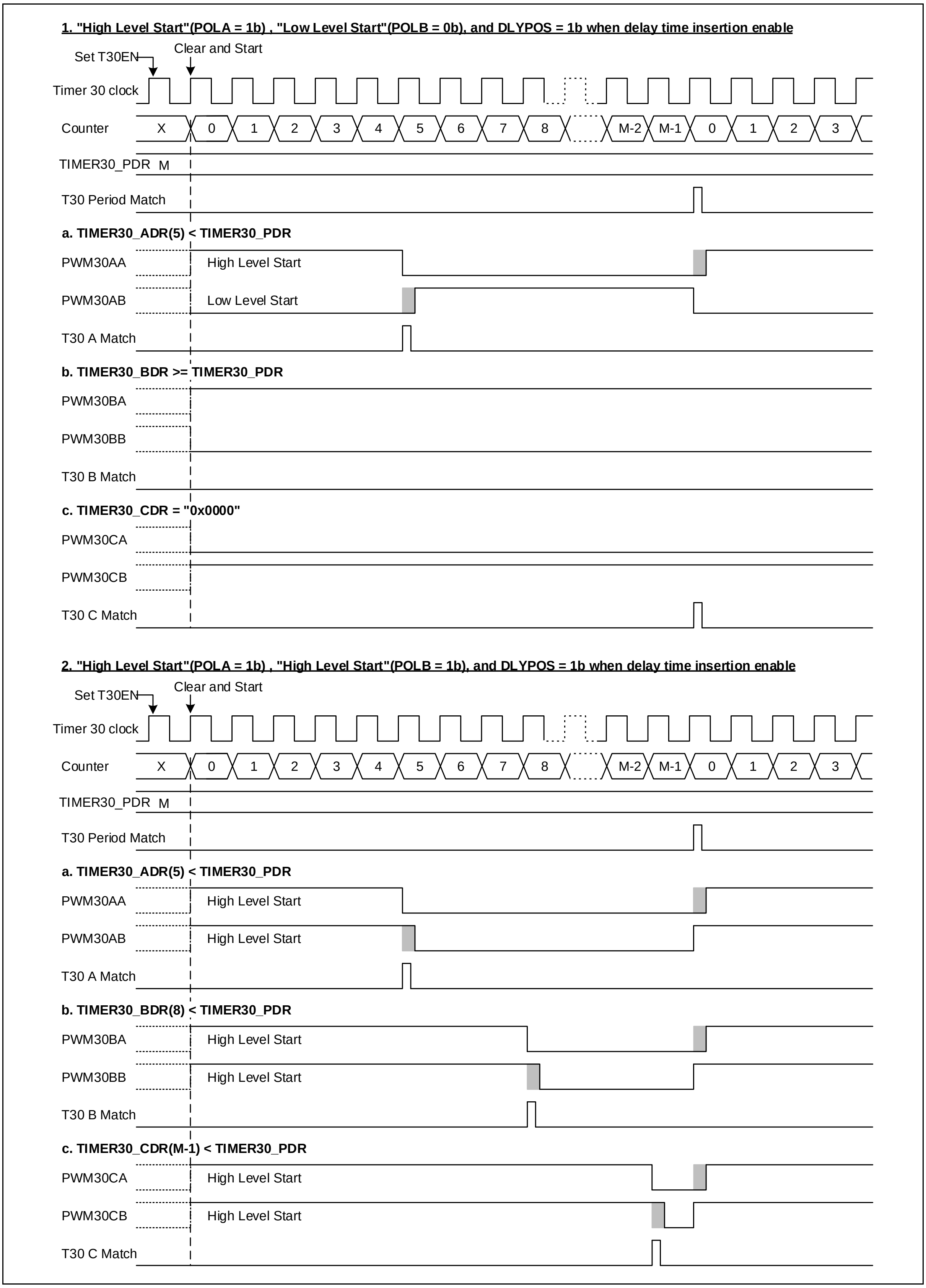


Figure 69. Interval Mode Timing Chart With "DLYPOS = 1

Back-to-back mode

The back-to-back mode is set by T30MS[1:0] as ‘10’. In the back-to-back mode, the 16-bit up/down counter repeats up/down count. In fact, the effective duty and period becomes twofold of the register set values. If the TIMER30_PDR’s data value is set to “0x3210, 16-bit up/down counter will increase until it reaches 0x3210. At this point, a period match signal is generated and the period match interrupt occurs. And then the 16-bit up/down counter will decrease until it reaches 0x0000. At this point, the bottom interrupt occurs. It is repeated in this way.

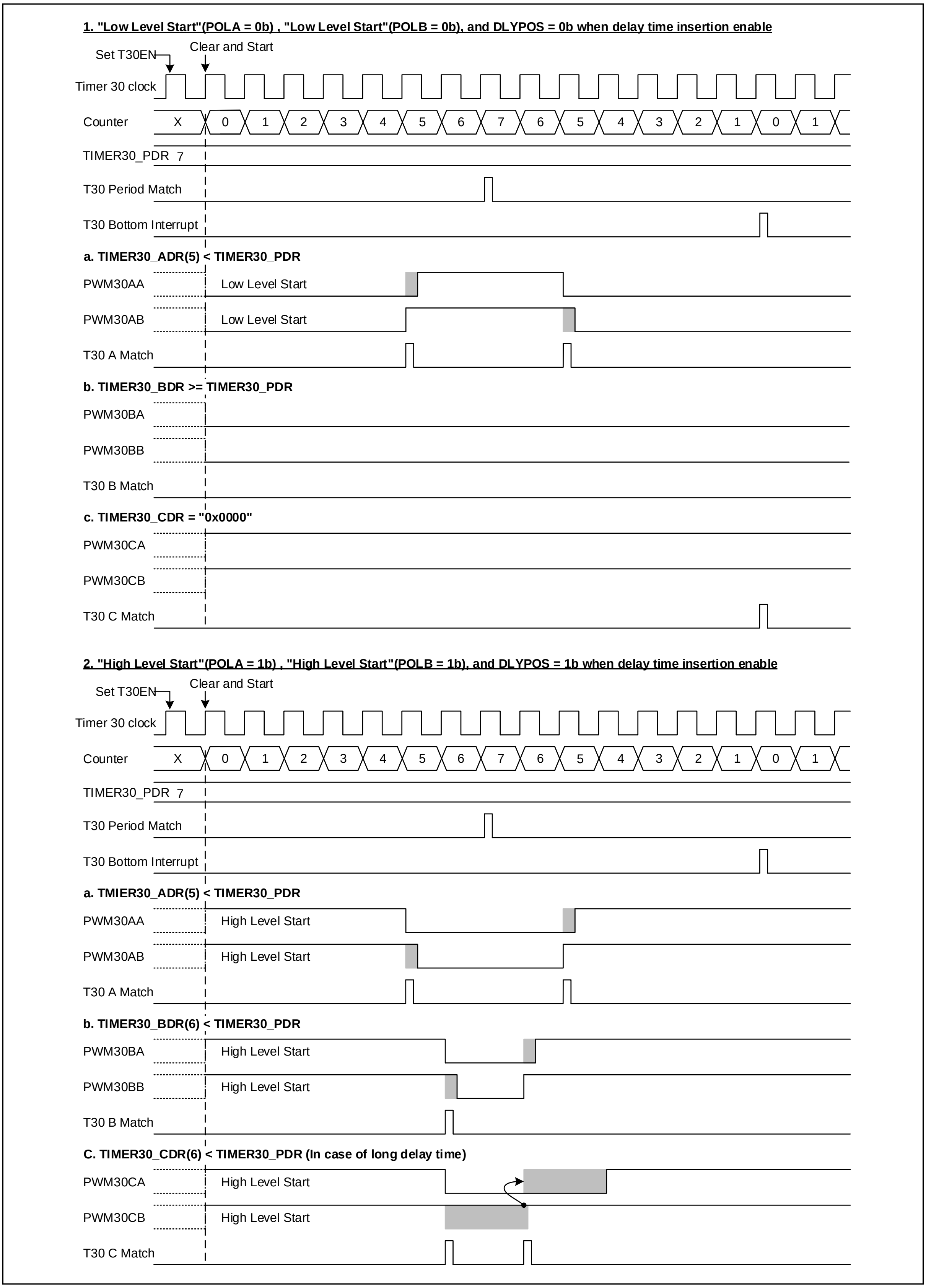


Figure 70. Back-to-Back Mode Timing Chart

Emergency protective function

This protective function is used for emergency stop, when the PWM30xA/PWM30xB output high-impedance enable bit, HIZEN is enabled. When the signal on the external BLNK input pin or internal comparator 3 output goes active (falling or rising edge triggered), the PWM30xA/PWM30xB ports are immediately disabled high-impedance against output and a high-impedance interrupt is occurred. The TIMER30_HIZCR register is used for high-impedance control. The high-impedance source is the external BLNK input pin. The high-impedance edge can be selected by HEDGE bit as falling or rising edge. If the HIZST read value is '1', it indicates that the pins are under a high-impedance state. To return from the high-impedance state, the HIZCLR bit set to '1'. If HIZSW bit is set to '1', PWM30xA/PWM30xB pins go into high impedance by software. It can be used for debugging. (x: A, B and C).

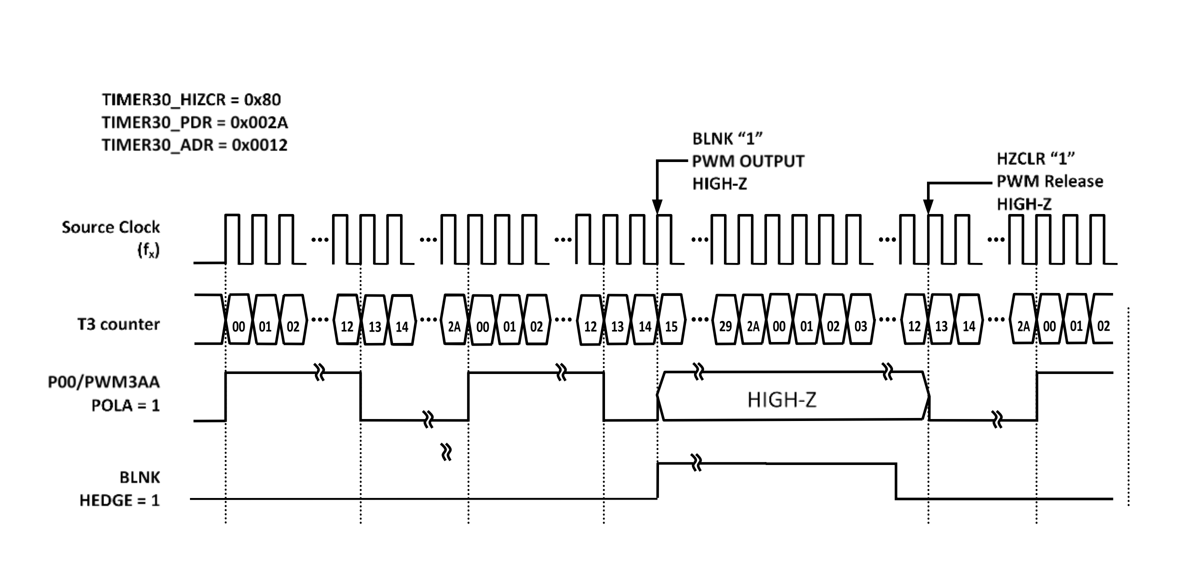


Figure 71. Example of PWM External Synchronization with BLNK Input (x: A, B and C)

Force A-channel mode

If FORCA bit is set to '1', it is possible to enable or disable all PWM output pins through PWM outputs which occur from A-ch duty counter. It is noted that the inversion outputs of A, B, C channel have the same A-ch output waveform.

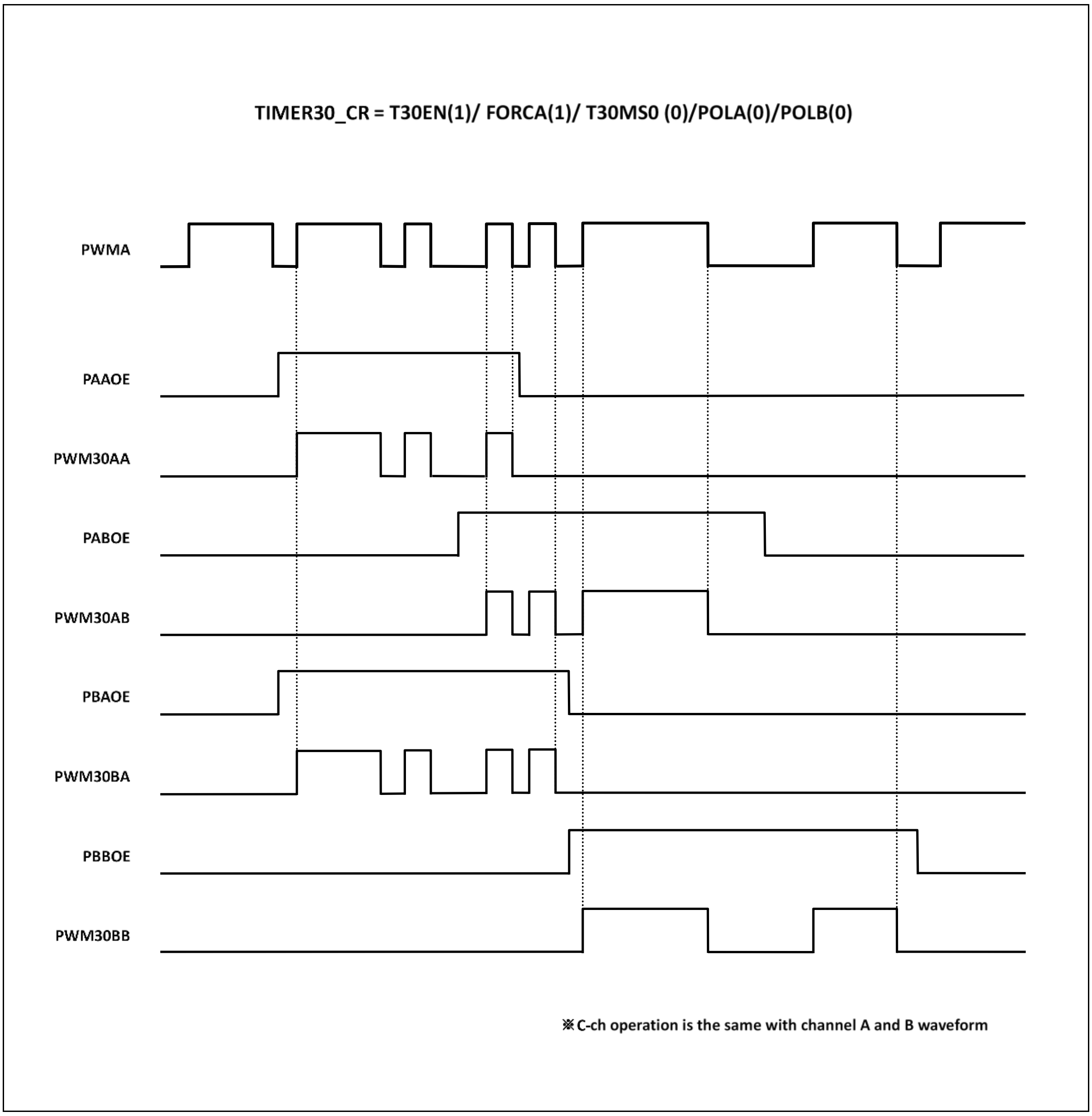

TIMER30_CR = T30EN(1)/ FORCA(1)/ T30MS0 (0)/POLA(0)/POLB(0)
PWMA
PAAOE
PWM30AA
PABOE
PWM30AB
PBAOE
PWM30BA
PBBOE
PWM30BB
※C-ch operation is the same with channel A and B waveform

Figure 72. Example of Force A-Channel Mode

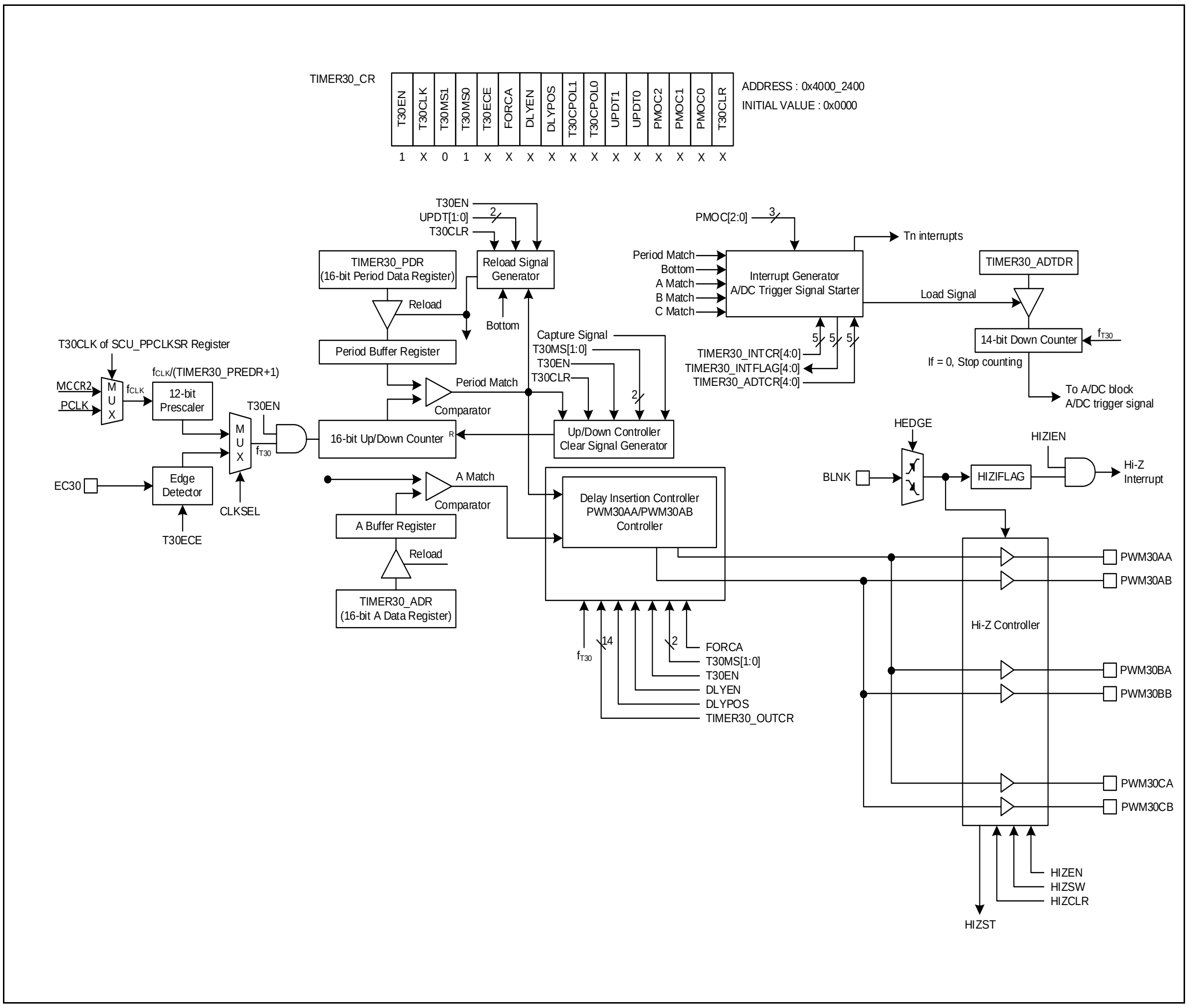


Figure 73. Force A-Channel Mode Block Diagram

6-channel mode

If FORCA bit sets to '0', it is possible to enable or disable PWM output pin and inversion output pin generated through the duty counter of each channel. The inversion output is the reverse phase of the PWM output. An AA/AB output of the A-channel duty register, a BA/BB output of the B-channel duty register, a CA/CB output of the C-channel duty register are controlled respectively.

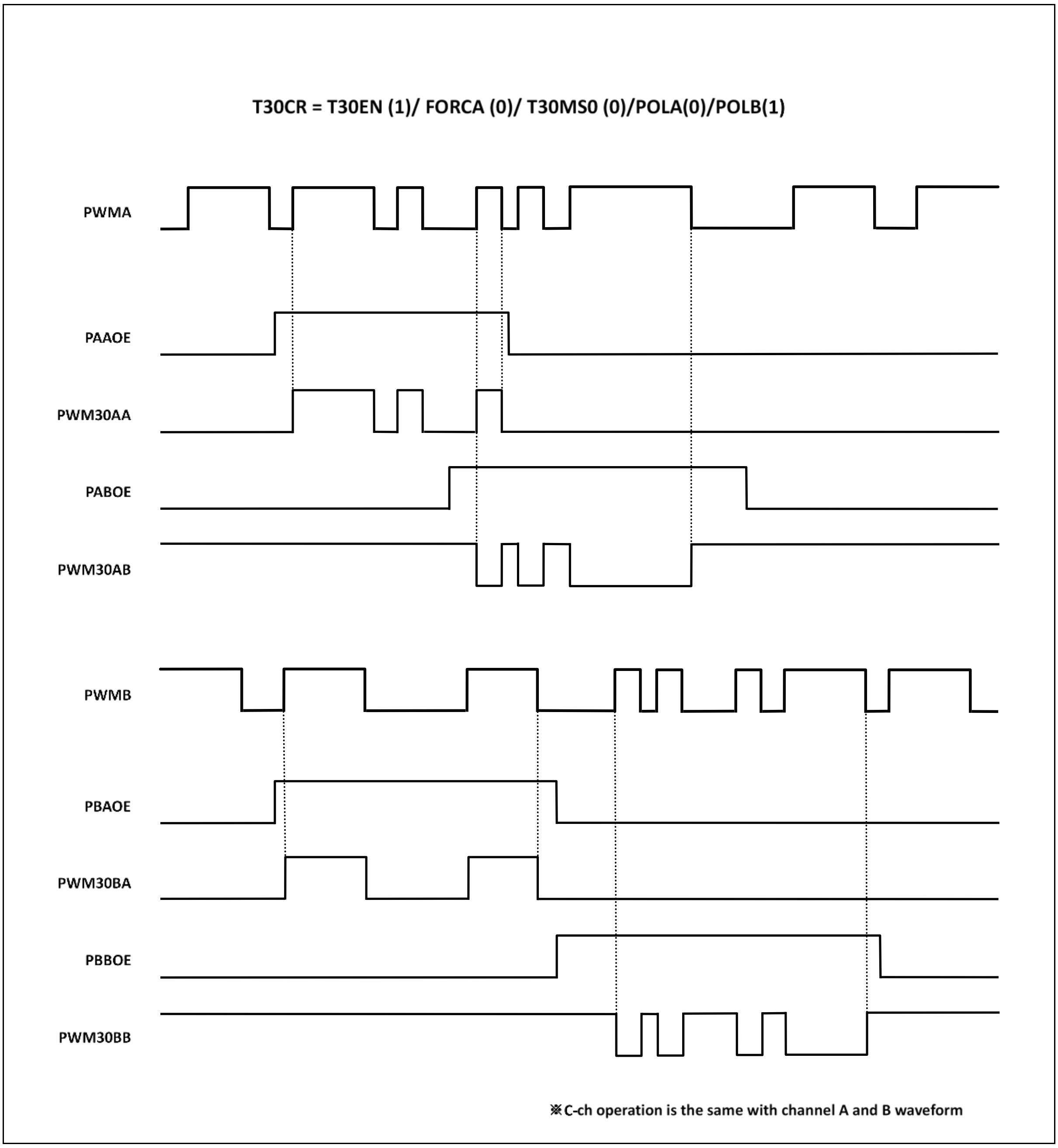

T30CR = T30EN (1)/ FORCA (0)/ T30MS0 (0)/POLA(0)/POLB(1)
PWMA
PAAOE
PWM30AA
PABOE
PWM30AB
PWMB
PBAOE
PWM30BA
PBBOE
PWM30BB
※C-ch operation is the same with channel A and B waveform

Figure 74. Example of 6-Channel Mode

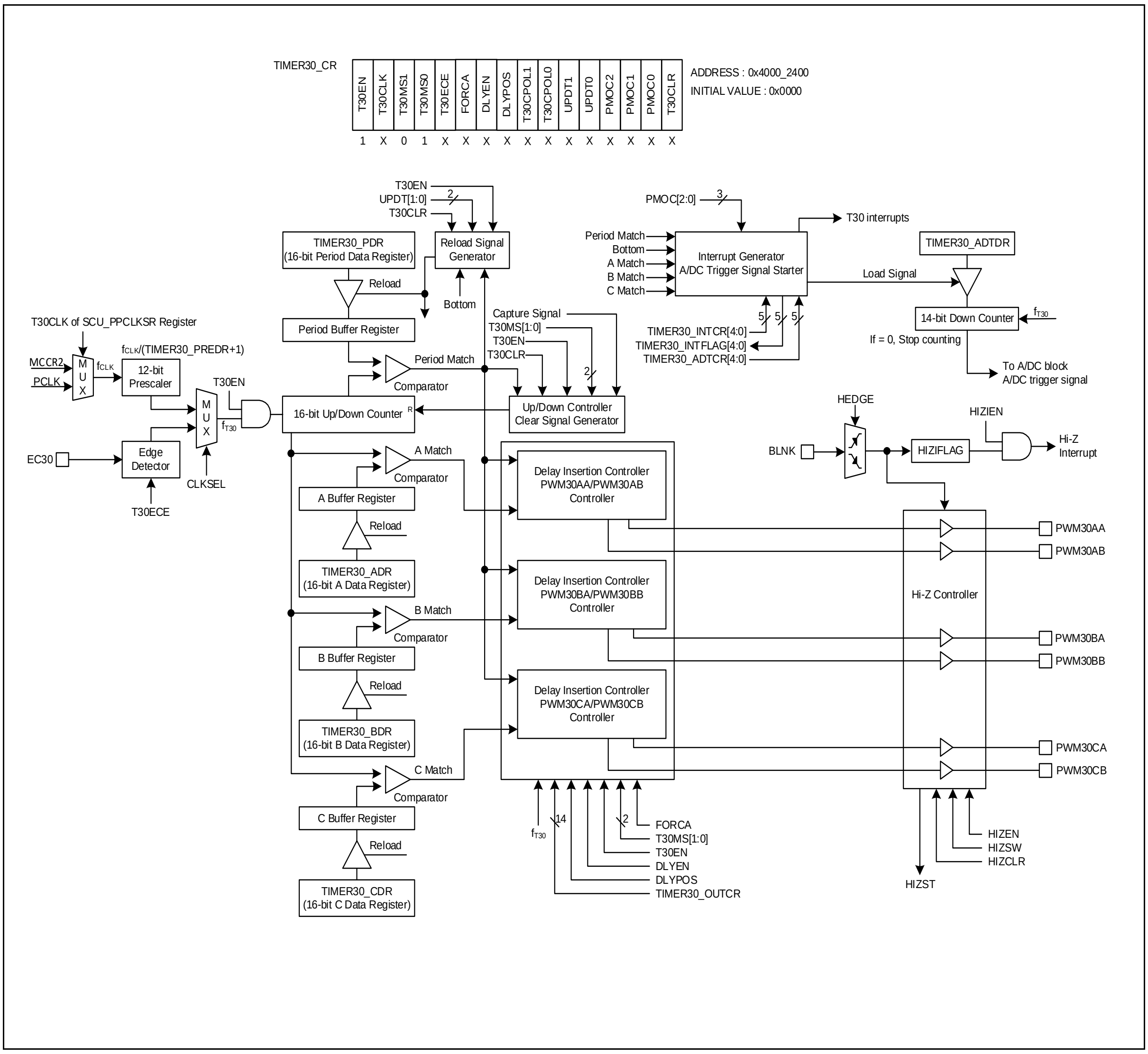


Figure 75. 6-Channel Mode Block Diagram

13 USART

Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication device. The main features are listed below:

- Full Duplex Operation. (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation.
- Baud Rate Generator.
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits.
- Odd or Even Parity Generation and Parity Check are Supported by Hardware.
- Data Over Run Detection.
- Framing Error Detection.
- Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion.
- Double Speed Asynchronous communication mode.

Additional features are:

- 0% Error Baud Rate by floating point count register.
- Supports receive time out interrupt.
- Supports direct memory access and interrupt.

Table 44 introduces pins assigned for the USART.

Table 44. Pin Assignment of USART: External Pins

Pin name	Type	Description
TXDn	O	UART Channel n transmit output
RXDn	I	UART Channel n receive input
SSn	I/O	SPIn Slave select input / output
SCKn	I/O	SPIn Serial clock input / output
MOSIn	I/O	SPIn Serial data (Master output, Slave input)
MISOn	I/O	SPIn Serial data (Master input, Slave output)

NOTE: n = 10 and 11

13.1 USART block diagram

In this section, USART and SPIN are introduced in block diagrams.

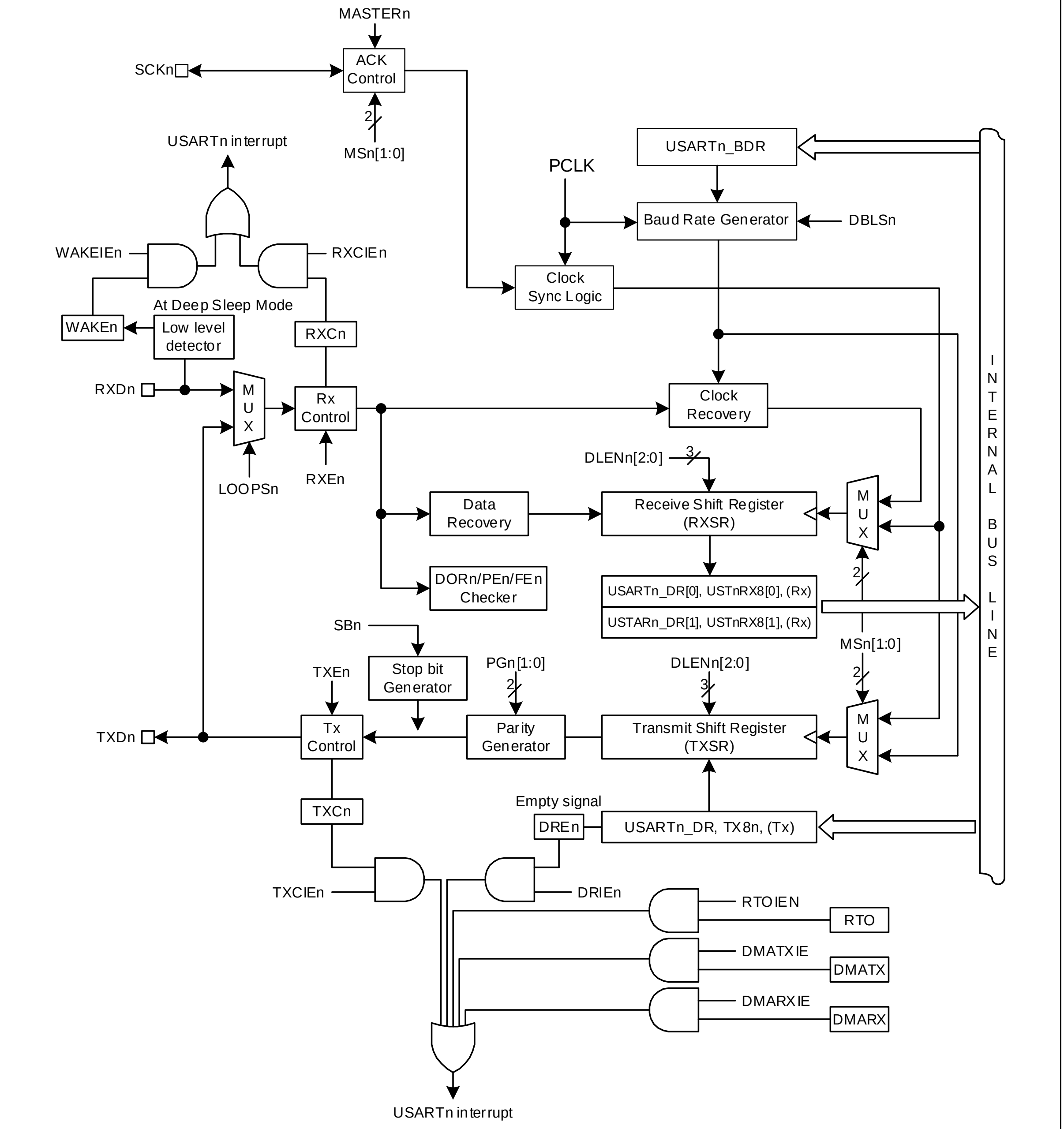


Figure 76. UART Block Diagram (n = 10 and 11)

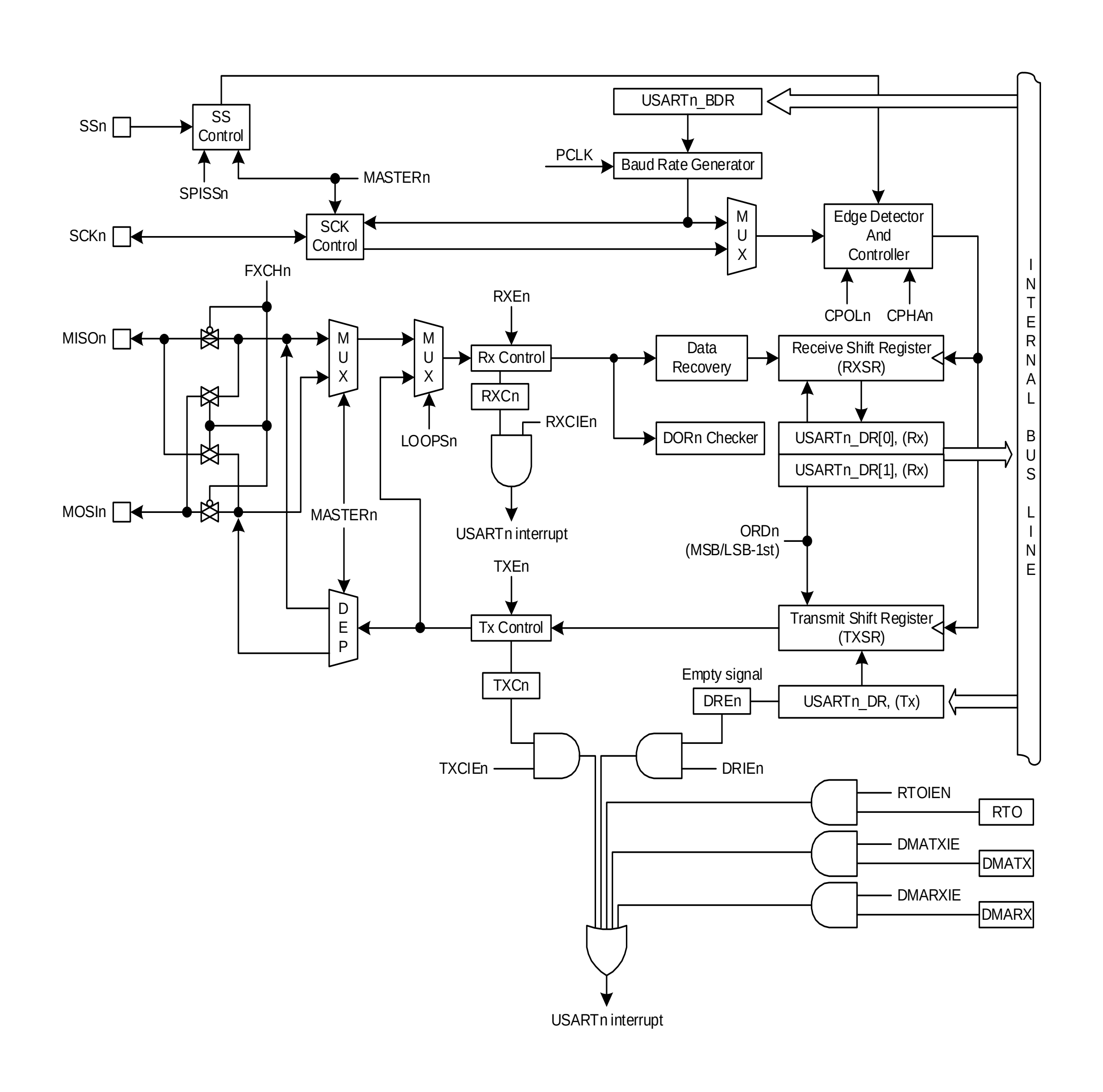


Figure 77. SPIN Block Diagram (n = 10 and 11)

13.2 Registers

Table 45 and Table 46 show base address and register map of USART.

Table 45. Base Address of USART

Name	Base address
USART 10	0x4000_3800
USART 11	0x4000_3900

Table 46. USART Register Map

Name	Offset	Type	Description	Reset value	Reference
USARTn_CR1	0x00	RW	USARTn Control Register 1	0x0000_0000	
USARTn_CR2	0x04	RW	USARTn Control Register 2	0x0000_0000	
USARTn_ST	0x0C	RW	USARTn Status Register	0x0000_0080	
USARTn_BDR	0x10	RW	USARTn Baud Rate Generation Register	0x0000_0FFF	
USARTn_DR	0x14	RW	USARTn Data Register	0x0000_0000	
USARTn_BFR	0x18	RW	USARTn Baud-Rate Fraction Counter Register	0x0000_0000	
USARTn_RTO	0x1C	RW	USARTn Receive Time Out Register	0x00FF_FFFF	

NOTE: n = 10 and 11

13.2.1 USARTn_CR1: USARTn control register 1

The USART module should be configured properly before running.

The USARTn_CR1 are 32-bit registers with 32/16/8-bit access. (n = 10 and 11)

USART10_CR1=0x4000_3800, USART11_CR1=0x4000_3900

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14	13 12	11 10 9	8	7	6	5	4	3	2	1	0
Reserved		MS	PG	DLEN	ORD	CPOL	CPHA	DRIE	TXCIE	RXCIE	WAKEIE	TXE	RXE
-		00	00	000	0	0	0	0	0	0	0	0	0
-		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

15 14	MS	USARTn Operation Mode Selection bits.			
		00	Asynchronous Mode. (UART)		
		01	Synchronous Mode.		
		10	Reserved.		
		11	SPI Mode		
13 12	PG	Selects Parity Generation and Check method. (only UART mode)			
		00	No parity.		
		01	Reserved.		
		10	Even parity.		
		11	Odd parity.		
11 9	DLEN	Selects the length of data bit in a frame when Asynchronous or Synchronous mode.			
		000	5 bit.		
		001	6 bit.		
		010	7 bit.		
		011	8 bit.		
		111	9 bit.		
		Others	Reserved.		
8	ORD	Selects the first data bit to be transmitted. (only SPI mode)			
		0	LSB-first.		
		1	MSB-first.		
7	CPOL	Selects the clock polarity of ACK in synchronous or SPI mode.			
		0	TXD Change @Rising Edge, RXD Change @Falling Edge.		
		1	TXD Change @Falling Edge, RXD Change @Rising Edge.		
6	CPHA	The CPOLn and this bit determine if data are sampled on the leading or trailing edge of SCK. (only SPI mode)			
		CPOLn	CPHAn	Leading edge	Trailing edge
		0	0	Sample (Rising)	Setup (Falling)
		0	1	Setup (Rising)	Sample (Falling)
		1	0	Sample (Falling)	Setup (Rising)
		1	1	Setup (Falling)	Sample (Rising)
5	DRIE	Transmit Data Register Empty Interrupt Enable bit.			
		0	Disable the transmit data empty interrupt.		
		1	Enable the transmit data empty interrupt.		
4	TXCIE	Transmit Complete Interrupt Enable bit.			
		0	Disable transmit complete interrupt.		

		1	Enable transmit complete interrupt.
3	RXCIE	Receive Complete Interrupt Enable bit.	
		0	Disable receive complete interrupt.
		1	Enable receive complete interrupt.
2	WAKEIE	Asynchronous Wake-up Interrupt Enable bit in Deep Sleep Mode. When device is in DEEP SLEEP mode, if RXDn goes to low level, an interrupt can be requested to wake-up system. (only UART mode) Must be set “1b” in Stop mode, set to “0b” if wake up from STOP mode.	
		0	Disable asynchronous wake-up interrupt.
		1	Enable asynchronous wake-up interrupt.
1	TXE	Enables the Transmitter unit.	
		0	Transmitter is disabled.
		1	Transmitter is enabled.
0	RXE	Enables the Receiver unit.	
		0	Receiver is disabled.
		1	Receiver is enabled.
NOTE: The CPOLn and CPHAn bits should be changed during the TXEn and RXEn bits are “0b”			

13.2.2 USARTn_CR2: USARTn control register 2

The USART module should be configured properly before running.

The USARTn_CR2 are 32-bit registers with 32/16/8-bit access. (n = 10 and 11)

USART10_CR2=0x4000_3804, USART11_CR2=0x4000_3904

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			DMATXIE	DMARXIE	RTOIE	RTOEN	BFREN	EN	DBLS	MASTER	LOOPS	DISSCK	SSEN	FXCH	SB	TX8	RX8
-			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Bits	Name	Function
14	DMATXIE	DMA TX Interrupt bit
		0 Disable DMS TX Interrupt
		1 Enable DMA TX Interrupt
13	DMARXIE	DMA RX Interrupt bit
		0 Disable DMA RX Interrupt
		1 Enable DMA RX Interrupt
12	RTOIE	RTO Interrupt bit
		0 Disable RTO Interrupt
		1 Enable RTO Interrupt
11	RTOEN	Activate RTO Block by supplying
		0 Disable RTO
		1 Enable RTO
10	BFREN	Activate Baud Rate Fraction Counter Register
		0 Disable Fraction Counter Register
		1 Enable Fraction Counter Register
9	EN	Activate USARTn Block by supplying.
		0 Disable USARTn block.
		1 Enable USARTn block.
8	DBLS	Selects receiver sampling rate. (only UART mode)
		0 Normal asynchronous operation.
		1 Double speed asynchronous operation.
7	MASTER	Selects master or slave in SPIn or synchronous mode and controls the direction of SCKn pin.
		0 Slave operation. (External clock for SCKn)
		1 Master operation. (Internal clock for SCKn)
6	LOOPS	Control the Loop Back mode of USARTn for test mode.
		0 Normal operation.
		1 Loop Back mode.
5	DISSCK	In synchronous mode operation, selects the waveform of SCKn output.
		0 SCKn is free-running while USARTn is enabled in synchronous master mode.
		1 SCKn is active while any frame is on transferring.
4	SSEN	This bit controls the SSn pin operation. (only SPI mode)
		0 Disable.

		1	Enable.
3	FXCH	SPIn port function exchange control bit. (only SPI mode)	
		0	No effect.
		1	Exchange MOSIn and MISOn function.
2	SB	Selects the length of stop bit in asynchronous or synchronous mode.	
		0	1 Stop bit.
		1	2 Stop bit.
1	TX8	The ninth bit of data frame in asynchronous or synchronous mode of operation. Write this bit first before loading the USTnDR register.	
		0	MSB (9th bit) to be transmitter is ‘0’.
		1	MSB (9th bit) to be transmitter is ‘1’.
0	RX8	The ninth bit of data frame in asynchronous or synchronous mode of operation. Read this bit first before reading the receive buffer (only UART mode)	
		0	MSB (9th bit) to be received is ‘0’.
		1	MSB (9th bit) to be received is ‘1’.

13.2.3 USARTn_ST: USARTn status register

The USARTn_ST are 32-bit registers with 32/16/8-bit access. (n = 10 and 11)

USART10_ST =0x4000_380C, USART11_ST =0x4000_390C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10	9	8	7	6	5	4	3	2	1	0
Reserved			DMATXF	DMARXF	DRE	TXC	RXC	WAKE	RTOF	DOR	FE	PE
-			0	0	1	0	0	0	0	0	0	0
-			RW	RW	RW	RW	RO	RO	RW	RO	RW	RW

Bits	Name	Function	
9	DMATXF	DMA Transmit Operation Complete flag (DMA to USART)	
		0	DMA Transmit Operation is working or is disabled
		1	DMA Transmit Operation is done
8	DMARXF	DMA Receive Operation Complete flag (USART to DMA)	
		0	DMA Receive Operation is working or is disabled
		1	DMA Transmit Operation is done
7	DRE	Transmit Data Register Empty Interrupt Flag. The DRE flag indicates if the transmit data register (USARTn_DR) is ready to receive new data. If DRE is '1', the data register is empty and ready to be written.	
		0	Transmit buffer is not empty.
		1	Transmit buffer is empty. This bit is cleared to '0' when write '1'.
6	TXC	Transmit Complete Interrupt Flag. This flag is set when the entire frame in the transmit shift register has been shifted out and there is no new data currently present in the transmit buffer.	
		0	No request occurred.
		1	Transmit buffer is empty and the data in transmit shift register are shifted out completely. This bit is cleared to '0' when write '1'.
5	RXC	Receive Complete Interrupt Flag. This flag is set when there are unread data in the receive buffer and cleared when all the data in the receive buffer are read.	
		0	There is no data unread in the receive buffer.
		1	There are more than 1 data in the receive buffer.
4	WAKE	Asynchronous Wake-up Interrupt Flag. This flag is set when the RXD pin is detected low while the CPU is in DEEP SLEEP mode. (only UART mode)	
		0	No request occurred.
		1	Request occurred, This bit is cleared to '0' when write '1'.
3	RTOF	Receive Time Out Interrupt flag. This bit is cleared to '0' when write '1'.	
		0	Receive time out is not generated
		1	Receive time out is generated.
2	DOR	This bit is set if data Over Run occurs. While this bit is set, the incoming data frame is ignored. This flag is valid until the receive buffer is read.	
		0	No Data Over Run.
		1	Data Over Run detected.
1	FE	This bit is set if the first stop bit of next character in the receive buffer is detected as '0'. This bit is valid until the receive buffer is read. (only UART mode)	
		0	No Frame Error.

		1	Frame Error detected.
0	PE	This bit is set if the next character in the receive buffer has a Parity Error while parity is checked. This bit is valid until the receive buffer is read. (only UART mode)	
		0	No Parity Error.
		1	Parity Error detected.

13.2.4 USARTn_BDR: USARTn baud rate generation register

The USARTn_BDR are 32-bit registers with 32/16/8-bit access. (n = 10 and 11)

USART10_BDR =0x4000_3810, USART11_BDR =0x4000_3910

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				BDATA											
-																				0xFFF											
-																				RW											

11 0	BDATA	The value in this register is used to generate internal baud rate in UART mode or to generate SCK clock in SPI mode. To prevent malfunction, do not write '0' in UART mode and do not write '0' or '1' in synchronous or SPI mode.

13.2.5 USARTn_DR: USARTn data register

The USARTn_DR are 32-bit registers with 32/16/8-bit access. (n = 10 and 11)

USART10_DR =0x4000_3814, USART11_DR =0x4000_3914

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																								DATA							
-																								0x00							
-																								RW							

7 0	DATA	The USART Transmit buffer and Receive buffer share the same I/O address with this DATA register. The Transmit Data Buffer is the destination for data written to the USARTn_DR register. Reading the USTnDR register returns the contents of the Receive Buffer. Write to this register only when the DRE flag is set. In SPI master mode, the SCK clock is generated when data are written to this register.

NOTE: This byte won't be written when the block is disabled or both of TXEn and RXEn bits are "0b".

13.2.6 USARTn_BFR: USARTn-baud-rate fraction count register

The USARTn_BFR are 32-bit registers with 32/16/8-bit access. (n = 10 and 11)

USART10_FPCR =0x4000_3818, USART11_FPCR =0x4000_3918

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved			BFC
-			0xFFF
-			RW

Bits	Name	Function
7 0	BFC	USARTn baud rate fraction counter 8-bit floating point counter

13.2.7 USARTn_RTO: USARTn-RTO register

The USARTn_RTO are 32-bit registers with 32/16/8-bit access. (n = 10 and 11)

USART10_RTO =0x4000_381C, USART11_RTO =0x4000_391C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved	RTO		
-	0xFFFFFF		
-	RW		

Bits	Name	Function
23 0	RTO	USART receive time out register

13.3 Functional description

The USART includes a clock generator, transmitter and receiver.

The clock generation logic consists of a synchronization logic for external clock input used by synchronizing or SPI slave operation, and the baud rate generator for asynchronous or master (synchronous or SPI) operation.

The transmitter consists of a single write buffer, a serial shift register, parity generator and control logic for handling different serial frame formats. The write buffer allows continuous transfer of data without any delay between frames.

The receiver is the most complex part of the UART module due to its clock and data recovery units. The recovery unit is used for asynchronous data reception. In addition to the recovery unit, the receiver includes a parity checker, a shift register, a two-level receive FIFO (USARTn_DR) and control logic. The receiver supports the same frame formats as the transmitter and can detect frame error, data overrun and parity errors (n = 10 and 11).

13.3.1 USART clock generation

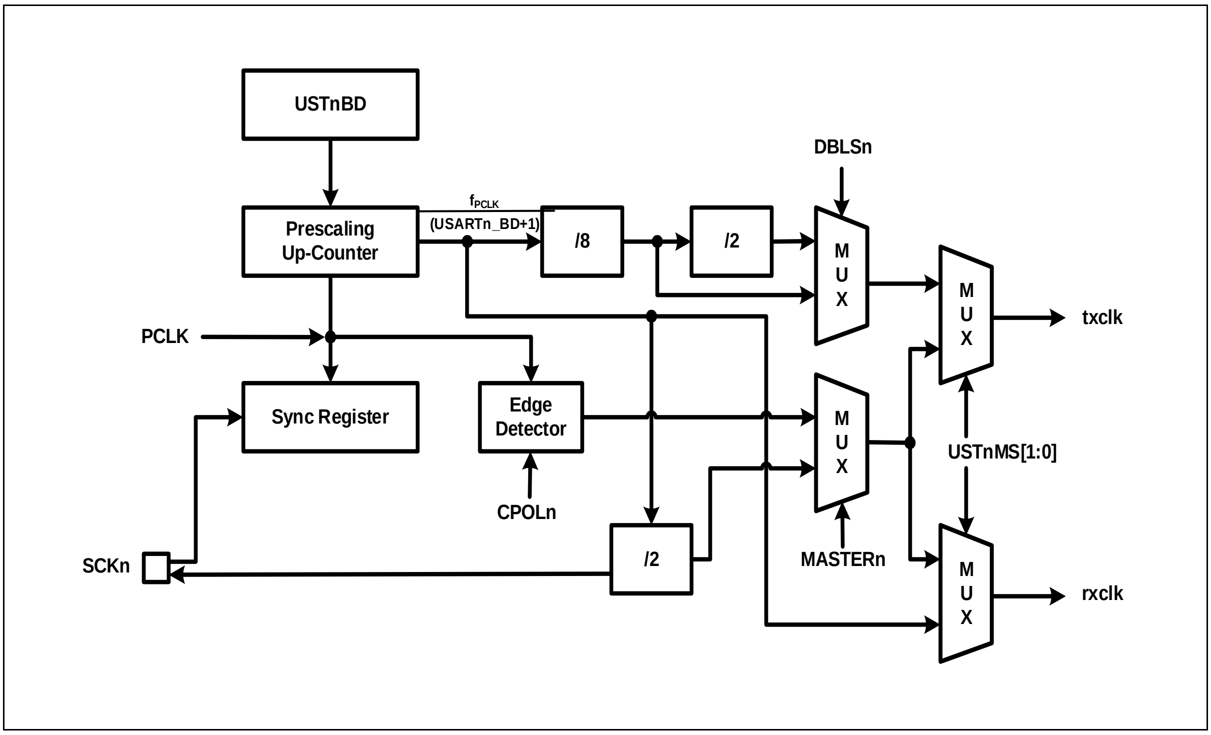


Figure 78. Clock Generation Block Diagram (USARTn, n = 10 and 11)

The clock generation logic generates the base clock for the transmitter and receiver. The USART supports four modes of clock operation and those are normal asynchronous, double speed asynchronous, master synchronous and slave synchronous modes.

The clock generation scheme for master SPI and slave SPI mode is the same as master synchronous and slave synchronous operation mode.

MS[1:0] bits in USARTn_CR1 register selects asynchronous or synchronous operation. Asynchronous double speed mode is controlled by the DBLS[8] bit in the USARTn_CR2 register.

MASTER[7] bit in USARTn_CR2 register controls whether the clock source is internal (master mode, output pin) or external (slave mode, input pin). The SCKn pin is active only when the USART operates in synchronous or SPI mode.

Table 47 shows the equations for calculating baud rate (in bps).

Table 47. Equations for Calculating USART Baud Rate Register Settings

Operating Mode	Equation for Calculating Baud Rate
Asynchronous Normal Mode (DBLSn=0)	Baud Rate = PCLK/(16(USARTn_BDR+1))
Asynchronous Double Speed Mode (DBLSn=1)	Baud Rate = PCLK/(8(USARTn_BDR+1))
Synchronous or SPI Master Mode	Baud Rate = PCLK/(2(USARTn_BDR+1))

NOTE: n = 10 and 11

13.3.2 External clock (SCKn)

External clocking is used in the synchronous or SPI slave mode of operation.

External clock input from the SCKn pin is sampled by a synchronization logic to remove meta-stability. Output from the synchronization logic must be passed through an edge detector before it is used by the transmitter and receiver. This process introduces two CPU clock period delay. The maximum frequency of the external SCKn pin is limited by 1MHz.

13.3.3 Synchronous mode operation

External clocking is used in the synchronous or SPI slave mode of operation.

When synchronous or SPI mode is used, the SCKn pin will be used as either clock input (slave) or clock output (master). Data sampling and transmitter are issued on the different edge of SCKn clock respectively. For example, if data input on RXDn (MISOn in SPI mode) pin is sampled on the rising edge of SCKn clock, data output on TXDn (MOSIn in SPI mode) pin is altered on the falling edge.

CPOL[7] bit in USARTn_CR1 register selects which SCKn clock edge is used for data sampling and which is used for data change. As shown in Figure 79, when CPOL[7] is zero, the data will be changed at rising edge of SCKn and sampled at falling edge of SCKn.

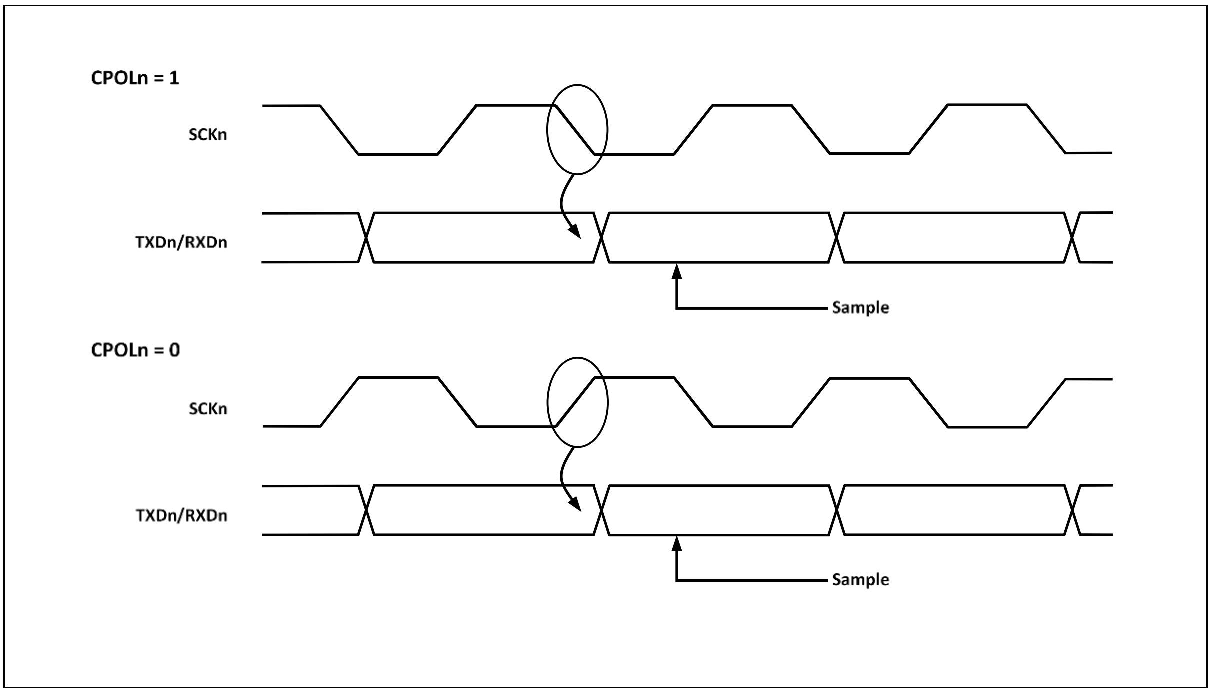


Figure 79. Synchronous Mode SCKn Timing (USARTn, n = 10 and 11)

13.3.4 UART data format

A serial frame is defined to be one character of data bits with synchronization bits (start and stop bits), and optionally a parity bit for error detection. USART supports all 30 combinations of the following as valid frame formats.

- 1 start bit
- 5, 6, 7, 8 or 9 data bits
- No, even or odd parity bit.
- 1 or 2 stop bits.

A frame starts with a start bit followed by the least significant data bit (LSB). Next data bits, up to nine, are succeeding, ending with the most significant bit (MSB). If parity function is enabled, the parity bit is inserted between the last data bit and the stop bit.

A high-to-low transition on data pin is considered as start bit. When a complete frame is transmitted, it can be directly followed by a new frame, or the communication line can be set to an idle state. The idle means high state of data pin.

Figure 80 shows possible combinations of the frame formats. Bits inside brackets are optional.

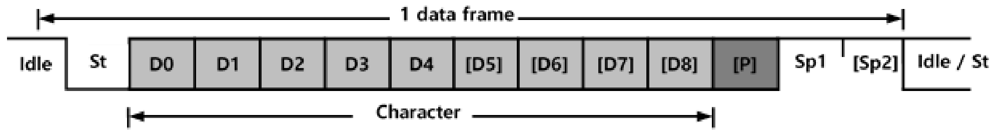


Figure 80. Frame Format (USART)

Single data frame consists of the following bits:

- Idle: No communication on communication line (TXDn/RXDn)
- St: Start bit (Low)
- Dm: Data bits (0 to 8)
- Parity bit ------------ Even parity, Odd parity, No parity
- Stop bit(s) ---------- 1 bit or 2 bits

Frame format of UART is set by configuring DLEN[11:9], PE[13:12] bits in USARTn_CR1 register and SB[2] bit in USARTn_CR2 register. Transmitter and receiver use the same figures (n = 10 and 11).

13.3.5 UART parity bit

Parity bit is calculated by doing an exclusive-OR of all data bits. If odd parity is used, the result of the exclusive-OR is inverted. Parity bit is located between the MSB and first stop bit of a serial frame.

- Peven = Dm-1 ^ … ^ D3 ^ D2 ^ D1 ^ D0 ^ 0
- Podd = Dm-1 ^ … ^ D3 ^ D2 ^ D1 ^ D0 ^ 1
- Peven: Parity bit using even parity
- Podd: Parity bit using odd parity
- Dm: Data bit n of the character

13.3.6 UART transmitter

UART transmitter is enabled by configuring TXE[1] bit in USARTn_CR1 register. When the transmitter is enabled, TXDn pin should be set to TXDn function for the serial output pin of UART by the PB_AFSR1/PD_AFSR1 and PB_MOD/PD_MOD. Baud rate, operation mode and frame format must be set up once before starting any transmission.

In synchronous operation mode, SCKn pin is used as a transmission clock, so it should be selected to function SCKn by PB_AFSR1/PD_AFSR1 and PB_MOD/PD_MOD (n = 10 and 11).

UART sending TX data

A data transmission is initiated by loading the transmit buffer (USARTn_DR register I/O location) with the data to be transmitted. The data be written in transmit buffer is moved to the shift register when the shift register is ready to send a new frame. The shift register is loaded with the new data if it is in idle state or immediately after the last stop bit of the previous frame is transmitted. When the shift register is loaded with new data, it will transfer one complete frame according to the settings of control registers. If the 9-bit characters are used in asynchronous or synchronous operation mode, the ninth bit must be written to the TX8[1] bit in USARTn_CR2 register before it is loaded to the transmit buffer USARTn_DR register (n = 10 and 11).

UART transmitter flag and interrupt

The USART transmitter has two flags which indicate its state. One is USART data register empty flag (DRE[7]) and the other is transmit completion flag (TXC[6]). Both flags can be interrupt sources.

DRE[7] flag indicates whether the transmit buffer is ready to receive new data. This bit is set when the transmit buffer is empty and cleared when the transmit buffer contains data to be transmitted but has not yet been moved into the shift register. And also this flag can be cleared by writing '0' to this bit position. Writing '1' to this bit position is prevented.

When the data register empty interrupt enable (DRIE[5]) bit in USARTn_CR1 register is set and the global interrupt is enabled, USARTn_ST status register empty interrupt is generated while DRE[7] flag is set.

The transmit complete (TXC[6]) flag bit is set when the entire frame in the transmit shift register has been shifted out and there is no more data in the transmit buffer. The TXC[6] flag is automatically cleared when the transmit complete interrupt serve routine is executed, or it can be cleared by writing '0' to TXC[6] bit in USARTn_ST register.

When the transmit complete interrupt enable (TXCIE[4]) bit in USARTn_CR1 register is set and the global interrupt is enabled, UART transmit complete interrupt is generated while TXC[6] flag in USARTn_ST register is set (n = 10 and 11).

UART parity generator

The parity generator calculates the parity bit for the serial frame data to be sent. When parity bit is enabled by setting PG[13:12] bit value to 10b (even parity) or 11b (odd parity) in USARTn_CR1 register, the transmitter control logic inserts the parity bit between the MSB and the first stop bit of the frame to be sent.

UART disabling transmitter

Disabling the transmitter by clearing the TXE[1] bit in USARTn_CR1 will not become effective until ongoing transmission is completed. When the transmitter is disabled, the TXDn pin can be used as a normal general purpose I/O (n = 10 and 11).

13.3.7 UART receiver

USART receiver is enabled by setting the RXE[0] bit in the USARTn_CR1 register. When the receiver is enabled, the RXDn pin should be set to RXDn function for the serial input pin of UART by PB_AFSR1/PD_AFSR1 and PB_MOD/PD_MOD. The baud-rate, mode of operation and frame format must be set before serial reception. In synchronous or SPI operation mode the SCKn pin is used as transfer clock input, so it should be selected to do SCKn function by PB_AFSR1/PD_AFSR1 and PB_MOD/PD_MOD. In SPI operation mode the SSn input pin in slave mode can be configured as SSn output pin in master mode. This can be done by setting SSEN[4] bit in USARTn_CR2 register (n = 10 and 11).

UART receiving RX data

When UART is in synchronous or asynchronous operation mode, the receiver starts data reception when it detects a valid start bit (LOW) on RXDn pin. Each bit after start bit is sampled at pre-defined baud-rate (asynchronous) or sampling edge of SCKn (synchronous), and shifted into the receive shift register until the first stop bit of a frame is received. Even if there's the second stop bit in the frame, the second stop bit is ignored by the receiver. That is, receiving the first stop bit means that a complete serial frame is presented in the receiver shift register and contents of the shift register are to be moved into the receive buffer. The receive buffer is read by reading the USARTn_DR register.

If 9-bit characters are used (DLEN[2:0] = "111"), the ninth bit is stored in the RX8[0] bit position in the USARTn_CR2 register. The ninth bit must be read from the RX8[0] bit before reading the low 8 bits from the USARTn_TDR register. Likewise, the error flags Fen, DOR[2], PE[0] bit must be read before reading the data from USARTn_DR register. It's because the error flags are stored in the same FIFO position of the receive buffer (n = 10 and 11).

UART receiver flag and interrupt

The UART receiver has one flag that indicates the receiver state.

A receive complete (RXC[5]) flag indicates whether there are unread data in the receive buffer. This flag is set when there is unread data in the receive buffer and cleared when the receive buffer is empty. If the receiver is disabled (RXE[0] = 0), the receiver buffer is flushed and the RXC[5] flag is cleared.

When a receive complete interrupt enable (RXCIE[3]) bit in the USARTn_CR1 register is set and global interrupt is enabled, the UART receiver complete interrupt is generated while RXC[5] flag is set.

The UART receiver has three error flags which are frame error (FE[2]), data overrun (DOR[2]) and parity error (PE[0]). These error flags can be read from the USARTn_ST register. As received data is stored in the 2-level receive buffer, these error flags are also stored in the same position of receive buffer. So, before reading received data from USARTn_DR register, read the USARTn_ST register first which contains error flags.

The frame error (FE[1]) flag indicates the state of the first stop bit. The Fen flag is "0" when the stop bit was correctly detected as "1", and the Fen flag is "1" when the stop bit was incorrect, i.e. detected as "0". This flag can be used for detecting out-of-sync conditions between data frames.

The data overrun (DOR[2]) flag indicates data loss due to a receive buffer full condition. DOR[2] occurs when the receive buffer is full, and another new data is presented in the receive shift register which are to be stored into the receive buffer. After the DOR[2] flag is set, all the incoming data are lost. To avoid data loss or clear this flag, read the receive buffer.

The parity error (PE[0]) flag indicates that the frame in the receive buffer had a parity error when received. If parity check function is not enabled (PG[13:12] = 0 in USARTn_CR1 register), the PE[0] bit in USARTn_ST register is always read "0" (n = 10 and 11).

UART parity checker

If parity bit is enabled (PG[13:12]=1 in USARTn_CR1 register), the Parity Checker calculates the parity of the data bits in incoming frame and compares the result with the parity bit from the received serial frame (n = 10 and 11).

UART disabling receiver

In contrast to transmitter, disabling the Receiver by clearing RXE[0] bit makes the Receiver inactive immediately.

When the receiver is disabled, the receiver flushes the receive buffer, the remaining data in the buffer is all reset, and the RXDn pin can be used as a normal general purpose I/O (n = 10 and 11).

Asynchronous data reception

To receive asynchronous data frame, the USART includes a clock and data recovery unit. The clock recovery logic is used for synchronizing the internally generated baud-rate clock to the incoming asynchronous serial frame on the RXDn pin.

The data recovery logic does sampling and low pass filtering the incoming bits, and removing the noise of RXDn pin.

The next figure illustrates the sampling process of the start bit of an incoming frame. The sampling rate is 16 times of the baud-rate in normal mode and 8 times the baud-rate for double speed mode (DBLS[8] = 1 in USARTn_CR2 register). The horizontal arrows show the synchronization variation due to the asynchronous sampling process. Note that larger time variation is shown when using the double speed mode (n = 10 and 11).

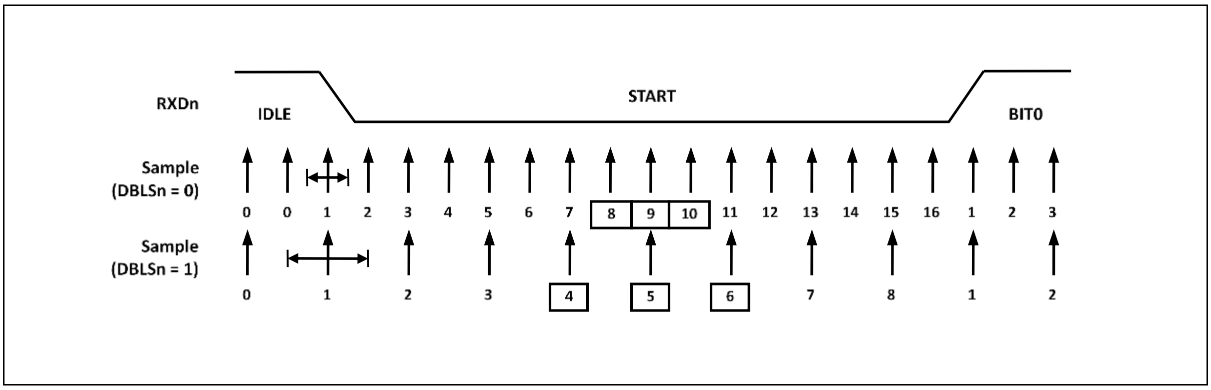


Figure 81. Asynchronous Start Bit Sampling (n = 10 and 11)

When the receiver is enabled (RXE[0] = 1), the clock recovery logic tries to find a high-to-low transition on the RXDn line, the start bit condition. After detecting high to low transition on RXDn line, the clock recovery logic uses samples 8, 9 and 10 for normal mode to decide if a valid start bit is received. If more than 2 samples have logical low level, it is considered that a valid start bit is detected and the internally generated clock is synchronized to the incoming data frame. And the data recovery can begin. The synchronization process is repeated for each start bit.

As described above, when the receiver clock is synchronized to the start bit, the data recovery can begin. Data recovery process is almost same to the clock recovery process. The data recovery logic samples 16 times for each incoming bits for normal mode and 8 times for double speed mode, and uses sample 8, 9 and 10 to decide data value. If more than 2 samples have low levels, the received bit is considered to a logic '0' and if more than 2 samples have high levels, the received bit is considered to a logic '1'.

The data recovery process is then repeated until a complete frame is received including the first stop bit. The decided bit value is stored in the receive shift register in order. Note that the Receiver only uses the first stop bit of a frame. Internally, after receiving the first stop bit, the Receiver is in idle state and waiting to find start bit.

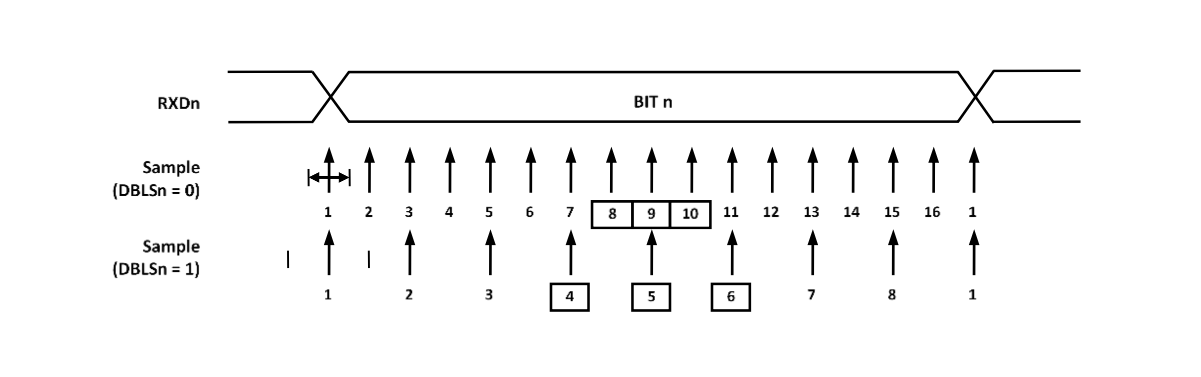


Figure 82. Asynchronous Data and Parity Bit Sampling (n = 10 and 11)

The process for detecting stop bit is same as clock and data recovery process. That is, if 2 or more samples of 3 center values have high level, correct stop bit is detected, else a frame error (FE[1]) flag is set. After deciding whether the first stop bit is valid or not, the Receiver goes to idle state and monitors the RXDn line to check a valid high to low transition is detected (start bit detection). (n = 10 and 11).

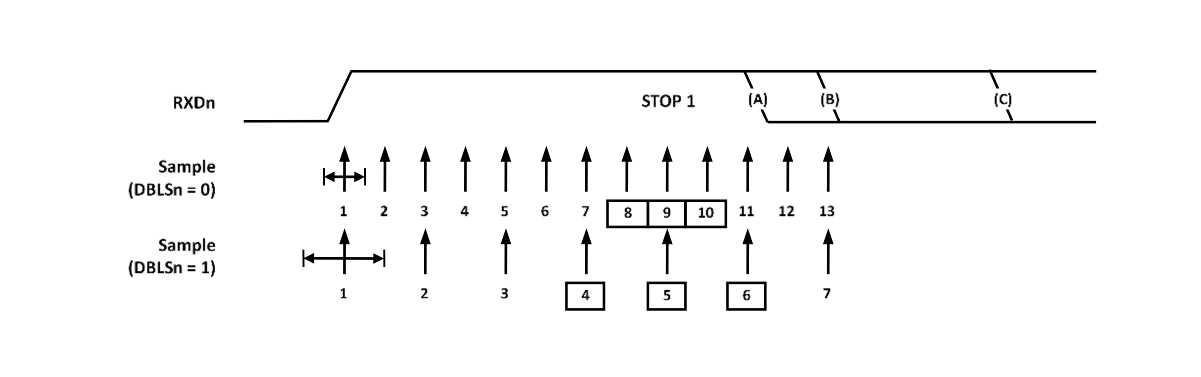


Figure 83. Stop Bit Sampling and Next Start Bit Sampling (n = 10 and 11)

13.3.8 SPI mode

The USART can be set to operate in industrial standard SPI compliant mode.

The SPI mode features the followings:

- Full Duplex, Three-wire synchronous data transfer.
- Mater and Slave Operation.
- Supports all four SPI modes of operation (mode 0, and 1).
- Selectable LSB first or MSB first data transfer.
- Double buffered transmit and receive.
- Programmable transmit bit rate.

When the SPI mode is enabled by configuring MS[15:14] as ”11”, the slave select (SSn) pin becomes active LOW input in slave mode operation, or can be output in master mode operation if USARTn_CR2<SSEN[4]> bit is set to ‘0’.

Note that during SPI mode of operation, the pin RXDn is renamed as MISOn, and TXDn is renamed as MOSIn for compatibility to other SPI devices (n = 10 and 11).

13.3.9 SPI clock formats and timing

To accommodate a wide variety if synchronous serial peripherals from different manufacturers, the USART has a clock polarity bit (CPOL[7]) and a clock phase control bit (CPHA[6]) to select one of four clock formats for data transfers. CPOL[7] selectively insert an inverter in series with the clock. CPHA[6] chooses between two different clock phase relationships between the clock and data. Note that CPHA[6] and CPOL[7] bits in USARTn_CR1 register have different meanings according to the USARTn_CR1<MS[15:14]> bits which decides the operating mode of USART(MS[15:14] = 01b).

Table 48 shows four combinations of CPOL and CPHA for SPI modes 0, 1, 2 and 3 (n = 10 and 11).

Table 48. CPOL Functionality

SPIn mode	CPOLn	CPHAn	Leading edge	Trailing edge
0	0	0	Sample (Rising)	Setup (Falling)
1	0	1	Setup (Rising)	Sample (Falling)
2	1	0	Sample (Falling)	Setup (Rising)
3	1	1	Setup (Falling)	Sample (Rising)

NOTE: n = 10 and 11

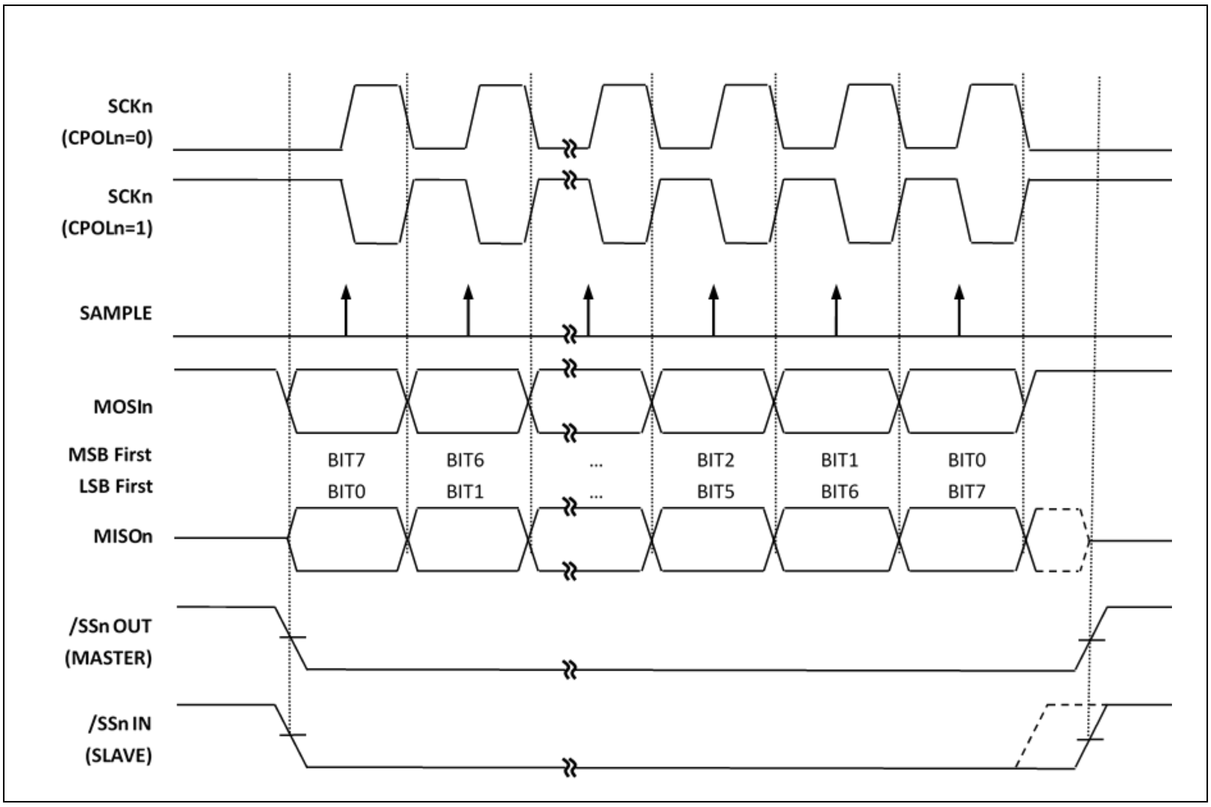


Figure 84. USART SPIn Clock Formats when CPHAn = 0 (n = 10 and 11)

When CPHA[6]=0, the slave begins to drive its MISOn output with the first data bit value when SSn goes to active low. The first SCKn edge causes both the master and the slave to sample the data bit value on their MISOn and MOSIn inputs, respectively.

At the second SCKn edge, the USART shifts the second data bit value out to the MOSIn and MISOn outputs of the master and slave, respectively. Unlike the case of CPHA[6] = 1, when CPHA[6] = 0, the slave's SSn input must go to its inactive high level between transfers. This is because the slave can prepare the first data bit when it detects falling edge of SSn input (n = 10 and 11).

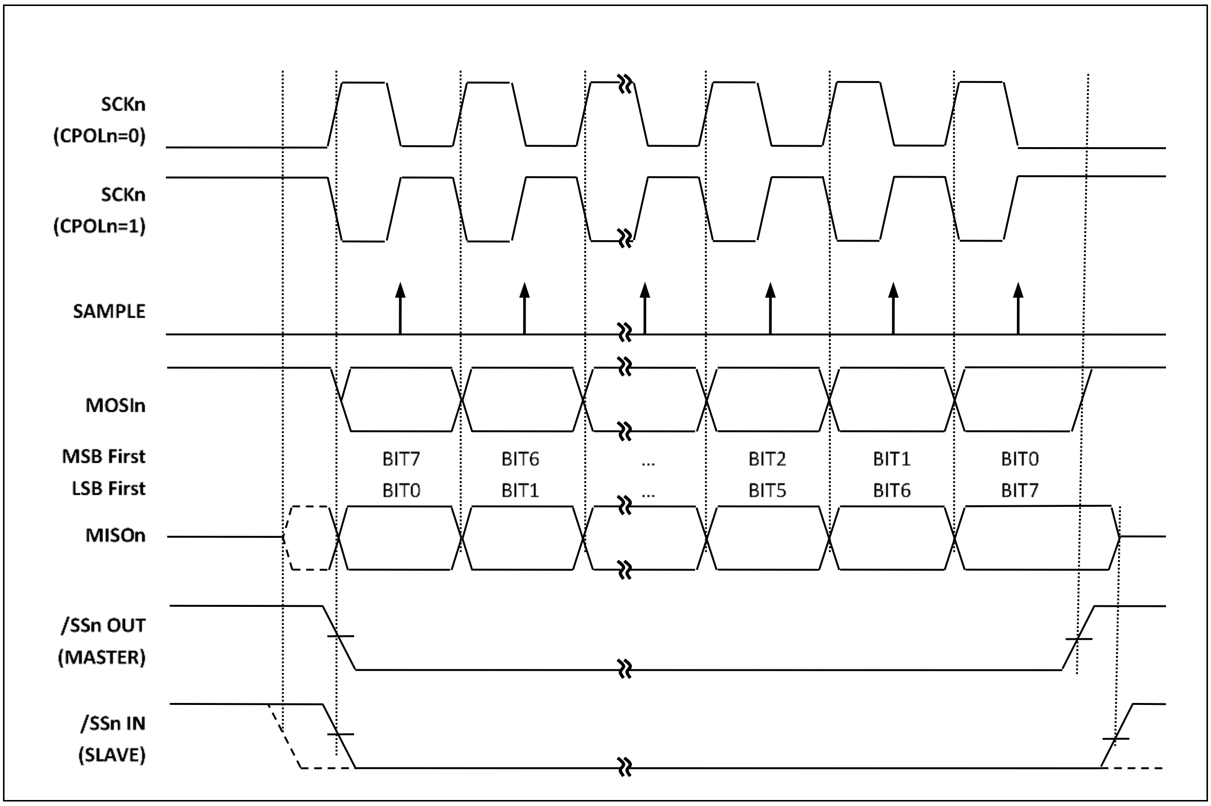


Figure 85. USART SPIn Clock Formats when CPHAn=1 (n = 10 and 11)

When CPHA[6] = 1, the slave begins to drive its MISOn output when SSn goes active low, but the data is not defined until the first SCKn edge. The first SCKn edge shifts the first bit of data from the shifter onto the MOSIn output of the master and the MISOn output of the slave.

The next SCKn edge causes both the master and slave to sample the data bit value on their MISOn and MOSIn inputs, respectively. At the third SCKn edge, the USART shifts the second data bit value out to the MOSIn and MISOn output of the master and slave respectively. When CPHA[6] = 1, the slave's SSn input is not required to go to its inactive high level between transfers.

Because the SPIn logic reuses the USART resources, SPIn mode of operation is similar to that of synchronous or asynchronous operation. SPIn transfer is initiated by checking for the USART Data Register Empty flag (DRE[7] = 1) in USARTn_ST register and then writing a byte of data to the USARTn_DR register. In master mode of operation, even if transmission is not enabled (TXE[0] = 0), writing data to the USARTn_DR register is necessary because the clock SCKn is generated from transmitter block.

13.3.10 Baud rate settings (example)

Table 49. Baud Rate Settings Example

Baud Rate	fOSC=1.00MHz				fOSC=1.8432MHz				fOSC=2.00MHz			
	DBLSn=0		DBLSn=1		DBLSn=0		DBLSn=1		DBLSn=0		DBLSn=1	
	UBAUD	ERROR	UBAUD	ERROR	UBAUD	ERROR	UBAUD	ERROR	UBAUD	ERROR	UBAUD	ERROR
2400	25	0.2%	51	0.2%	47	0.0%	95	0.0%	51	0.2%	103	0.2%
4800	12	0.2%	25	0.2%	23	0.0%	47	0.0%	25	0.2%	51	0.2%
9600	6	-7.0%	12	0.2%	11	0.0%	23	0.0%	12	0.2%	25	0.2%
14.4K	3	8.5%	8	-3.5%	7	0.0%	15	0.0%	8	-3.5%	16	2.1%
19.2K	2	8.5%	6	-7.0%	5	0.0%	11	0.0%	6	-7.0%	12	0.2%
28.8K	1	8.5%	3	8.5%	3	0.0%	7	0.0%	3	8.5%	8	-3.5%
38.4K	1	-18.6%	2	8.5%	2	0.0%	5	0.0%	2	8.5%	6	-7.0%
57.6K	-	-	1	8.5%	1	-25.0%	3	0.0%	1	8.5%	3	8.5%
76.8K	-	-	1	-18.6%	1	0.0%	2	0.0%	1	-18.6%	2	8.5%
115.2K	-	-	-	-	-	-	1	0.0%	-	-	1	8.5%
230.4K	-	-	-	-	-	-	-	-	-	-	-	-

Baud Rate	fOSC=3.6864MHz				fOSC=4.00MHz				fOSC=7.3728MHz			
	DBLSn=0		DBLSn=1		DBLSn=0		DBLSn=1		DBLSn=0		DBLSn=1	
	UBAUD	ERROR	UBAUD	ERROR	UBAUD	ERROR	UBAUD	ERROR	UBAUD	ERROR	UBAUD	ERROR
2400	95	0.0%	191	0.0%	103	0.2%	207	0.2%	191	0.0%	-	-
4800	47	0.0%	95	0.0%	51	0.2%	103	0.2%	95	0.0%	191	0.0%
9600	23	0.0%	47	0.0%	25	0.2%	51	0.2%	47	0.0%	95	0.0%
14.4K	15	0.0%	31	0.0%	16	2.1%	34	-0.8%	31	0.0%	63	0.0%
19.2K	11	0.0%	23	0.0%	12	0.2%	25	0.2%	23	0.0%	47	0.0%
28.8K	7	0.0%	15	0.0%	8	-3.5%	16	2.1%	15	0.0%	31	0.0%
38.4K	5	0.0%	11	0.0%	6	-7.0%	12	0.2%	11	0.0%	23	0.0%
57.6K	3	0.0%	7	0.0%	3	8.5%	8	-3.5%	7	0.0%	15	0.0%
76.8K	2	0.0%	5	0.0%	2	8.5%	6	-7.0%	5	0.0%	11	0.0%
115.2K	1	0.0%	3	0.0%	1	8.5%	3	8.5%	3	0.0%	7	0.0%
230.4K	-	-	1	0.0%	-	-	1	8.5%	1	0.0%	3	0.0%
250K	-	-	1	-7.8%	-	-	1	0.0%	1	-7.8%	3	-7.8%
0.5M	-	-	-	-	-	-	-	-	-	-	1	-7.8%

Baud Rate	fOSC=8.00MHz				fOSC=11.0592MHz				fOSC=14.7456MHz			
	DBLSn=0		DBLSn=1		DBLSn=0		DBLSn=1		DBLSn=0		DBLSn=1	
	UBAUD	ERROR	UBAUD	ERROR	UBAUD	ERROR	UBAUD	ERROR	UBAUD	ERROR	UBAUD	ERROR
2400	207	0.2%	-	-	-	-	-	-	-	-	-	-
4800	103	0.2%	207	0.2%	143	0.0%	-	-	191	0.0%	-	-
9600	51	0.2%	103	0.2%	71	0.0%	143	0.0%	95	0.0%	191	0.0%
14.4K	34	-0.8%	68	0.6%	47	0.0%	95	0.0%	63	0.0%	127	0.0%
19.2K	25	0.2%	51	0.2%	35	0.0%	71	0.0%	47	0.0%	95	0.0%
28.8K	16	2.1%	34	-0.8%	23	0.0%	47	0.0%	31	0.0%	63	0.0%
38.4K	12	0.2%	25	0.2%	17	0.0%	35	0.0%	23	0.0%	47	0.0%
57.6K	8	-3.5%	16	2.1%	11	0.0%	23	0.0%	15	0.0%	31	0.0%
76.8K	6	-7.0%	12	0.2%	8	0.0%	17	0.0%	11	0.0%	23	0.0%
115.2K	3	8.5%	8	-3.5%	5	0.0%	11	0.0%	7	0.0%	15	0.0%
230.4K	1	8.5%	3	8.5%	2	0.0%	5	0.0%	3	0.0%	7	0.0%
250K	1	0.0%	3	0.0%	2	-7.8%	5	-7.8%	3	-7.8%	6	5.3%
0.5M	-	-	1	0.0%	-	-	2	-7.8%	1	-7.8%	3	-7.8%
1M	-	-	-	-	-	-	-	-	-	-	1	-7.8%

13.3.11 0% error baud rate

This USART system supports the fraction counter logic for the 0% error of baud rate. By using the 8 bits floating point counter logic, the cumulative error to below the decimal point can be removed.

The fraction counter value is defined by baud rate error. In the baud rate formula, USARTn_BDR is presented the integer count value. For example, If you want to use the 57600 baud rate (f_{XIN} = 16MHz), a calculated integer count value must be 17.36 value (USARTn_BDR+1 = 16000000/(16×57600) = 17.36).

Here, USARTn_BDR which can be set is the nearest big integer number 17. To realize 0% error of baud rate, fraction counter value must be 92 ((0.36) x 256 ≒ 92). Namely you have to write 92 (decimal number) to USARTn_BFR and 17 (decimal number) to USART_BDR register.

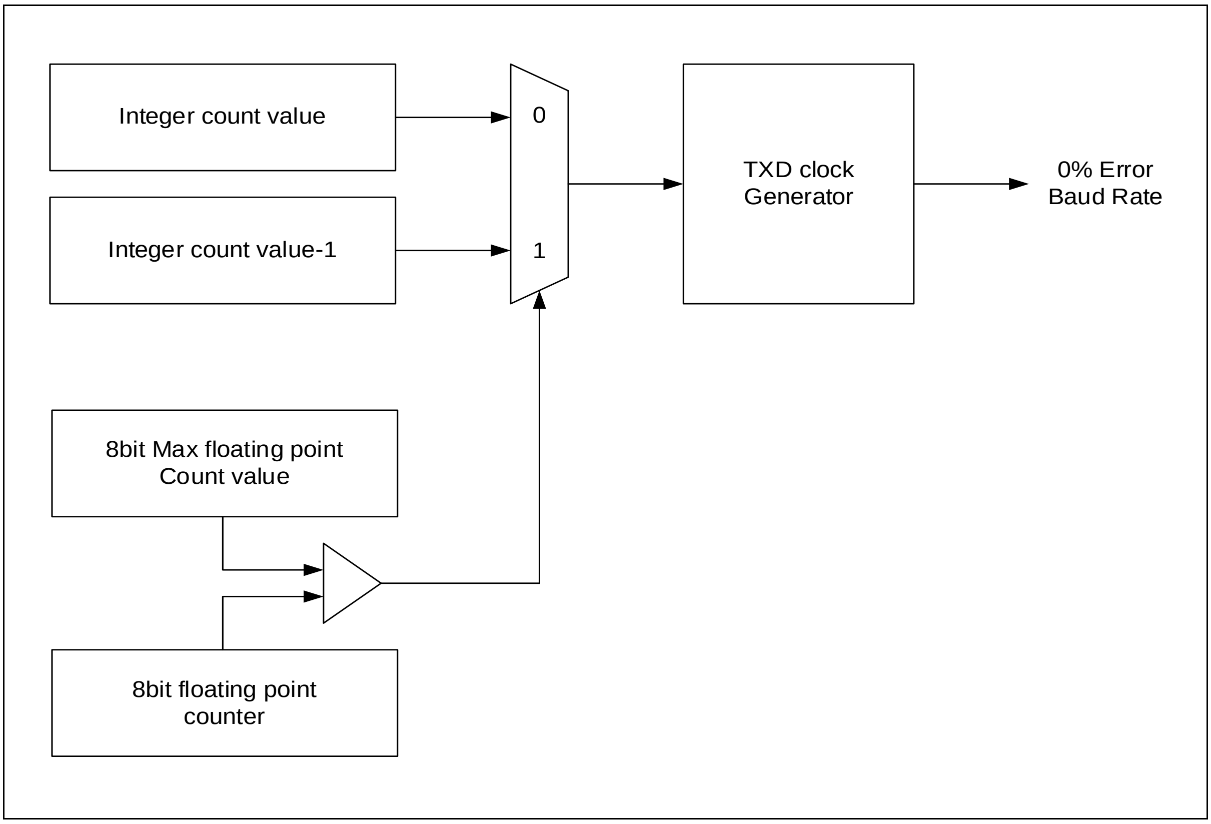


Figure 86. 0% Error Baud Rate Diagram

13.3.12 Receive Time Out (RTO)

This USART system supports the receive time out (RTO) interrupt. The RTO counter uses the system clock and continues counting while the RXD input is not present. If the RTO counter matches USARTn_RTO, RTOF becomes 1. RTOEN is set to 1 to enable this operation, and RTOEN is automatically set to 0 when an RTO match occurs. You can use RTO interrupts with RTOIE.

14 UART

Universal Asynchronous serial Receiver and Transmitter (UART) is a highly flexible serial communication device. UART operation status including error status can be read from status register. The prescaler which generates proper baud rate, is exist for each UART channel. The prescaler can divide the UART clock source that is PCLK, from 1 to 65535. And baud rate generation is by clock which internally divided by 16 of the prescaled clock and 8-bit precision clock tuning function. Programmable interrupt generation function will help to control the communication via UART channel

The main features are listed below:

- Compatible with 16450
- Standard asynchronous control bit (start, stop, and parity) configurable B
- Programmable 16-bit fractional baud generator
- Programmable serial communication
- 5-, 6-, 7- or 8- bit data transfer
- Even, odd, or no-parity bit insertion and detection
- 1-, 1.5- or 2-stop bit-insertion and detection
- 16-bit baud rate generation with 8-bit fraction control
- Hardware inter-frame delay function
- Stop bit error detection
- Detail status register

Table 50 introduces pins assigned for the UART.

Table 50. Pin Assignment of UART: External Pins

Pin name	Type	Description
TXD0	O	UART Channel 0 transmit output
RXD0	I	UART Channel 0 receive input
TXD1	O	UART Channel 1 transmit output
RXD1	I	UART Channel 1 receive input

NOTE: n = 0 and 1

14.1 UART block diagram

In this section, the UART interface block is described in a block diagram.

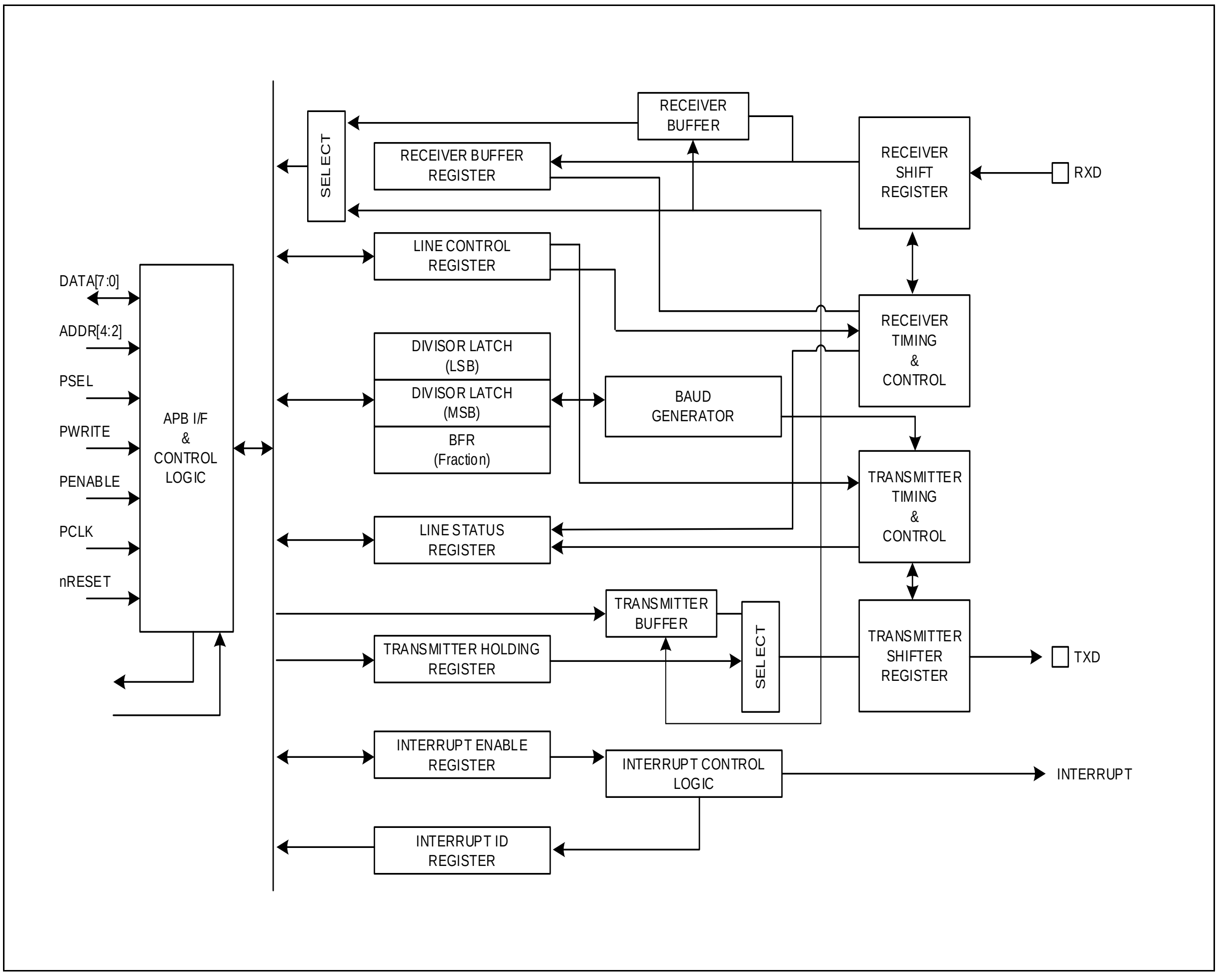


Figure 87. UART Block Diagram

14.2 Registers

Table 51 and Table 52 show base address and register map of the UART.

Table 51. Base Address of UART Interface

Name	Base address
UART0	0x4000_4000
UART1	0x4000_4100

Table 52. UART Register Map

Name	Offset	Type	Description	Reset value	Reference
UARTn_RBR	0x00	RO	Receive data buffer register	0x0000_0000	16.2.1
UARTn_THR	0x00	WO	Transmit data hold register	0x0000_0000	16.2.2
UARTn_IER	0x04	RW	Interrupt enable register	0x0000_0000	16.2.3
UARTn_IIR	0x08	RO	Interrupt ID register	0x0000_0001	16.2.4
UARTn_LCR	0x0C	RW	Line control register	0x0000_0000	16.2.5
UARTn_DCR	0x10	RW	Data control register	0x0000_0000	16.2.6
UARTn_LSR	0x14	RO	Line status register	0x0000_0060	16.2.7
UARTn_BDR	0x20	RW	Baud rate divisor latch register	0x0000_0000	16.2.8
UARTn_BFR	0x24	RW	Baud rate fractional counter value	0x0000_0000	16.2.9
UARTn_IDTR	0x30	RW	Inter-frame delay time register	0x0000_0000	16.2.10

NOTE: n = 0 and 1

14.2.1 UARTn_RBR: UARTn receive data buffer register

The UARTn_RBR are 32-bit registers with 32/16/8-bit access. (UART, n = 0, 1)

Received data will be read out from these registers. Maximum length of data is 8 bits. Last data received will be maintained in these registers until a new byte is received.

UART0_RBR=0x4000_4000, UART1_RBR=0x4000_4100

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved			RBR
-			0x00
-			RO

7 0	RBR	UARTn Receive Data Buffer bits

14.2.2 UARTn_THR: UARTn transmit data hold register

The UARTn_THR are 32-bit registers with 32/16/8-bit access. (UART, n = 0, 1)

UART0_THR=0x4000_4000, UART1_THR=0x4000_4100

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved			THR
-			0x00
-			WO

7 0	THR	UARTn Transmit Data Hold bits

14.2.3 UARTn_IER: UARTn interrupt enable register

The UARTn_IER are 32-bit registers with 32/16/8-bit access. (UART, n = 0, 1)

UART0_IER=0x4000_4004, UART1_IER=0x4000_4104

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																										DTXIEN	DRXIEN	TXEIE	RLSIE	THREIE	DRIE
-																										0	0	0	0	0	0
-																										RW	RW	RW	RW	RW	RW

5	DTXIEN	DMA transmit done interrupt enable	
		0	Receive line status interrupt is disabled
		1	Receive line status interrupt is enabled
4	DRXIEN	DMA receive done interrupt enable	
		0	DMA receive done interrupt is disabled
		1	DMA receive done interrupt is enabled
3	TXEIE	Transmit Register Empty Interrupt Enable.	
		0	Disable transmit register empty interrupt.
		1	Enable transmit register empty interrupt.
2	RLSIE	Receiver Line Status Interrupt Enable bit.	
		0	Disable receiver line status interrupt.
		1	Enable receiver line status interrupt.
1	THREIE	Transmit Holding Register Empty Interrupt Enable bit.	
		0	Disable transmit holding register empty interrupt.
		1	Enable transmit holding register empty interrupt.
0	DRIE	Data Receive Interrupt Enable bit.	
		0	Disable data receive interrupt.
		1	Enable data receive interrupt.

14.2.4 UARTn_IIR: UARTn interrupt ID register

The UARTn_IIR are 32-bit registers with 32/16/8-bit access. (UART, n = 0, 1)

UART0_IIR=0x4000_4008, UART1_IIR=0x4000_4108

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5	4	3	2 1	0
Reserved	TXE	Reserved	IID	IPEN
-	0	-	00	1
-	RO	-	RO	RO

4	TXE	Transmit Complete Interrupt Source ID bit.	
2 1	IID	UARTn Interrupt ID bits. **NOTE**:The UARTn supports 3-priority interrupt generation and the interrupt source ID register shows one interrupt source which has highest priority among pending interrupts. The priority is defined as below. - Receive line status interrupt. - Receive data ready interrupt and Character timeout interrupt. - Transmit hold register empty interrupt.	
0	IPEN	Interrupt Pending bit.	
		0	Interrupt is pending.
		1	No interrupt is pending.

Table 53. Interrupt ID and Control

Priority	TXE	IID		IPEN	Interrupt sources		
	Bit 4	Bit 2	Bit 1	Bit 0	Interrupt	Interrupt condition	Interrupt clear
-	0	0	0	1	None	-	-
1	0	1	1	0	Receiver Line Status	Overrun, Parity, Framing or Break Error	Read LSR register
2	0	1	0	0	Receiver Data Available	Receive data is available.	Read receive register or read IIR register
3	0	0	1	0	Transmitter Holding Register Empty	Transmit buffer empty	Write transmit hold register or read IIR register
4	1	X	X	X	Transmitter Register Empty	Transmit register empty	Write transmit hold register or read IIR register

NOTE: After check the above bits, Read data buffer to avoid losing interrupt source.

14.2.5 UARTn_LCR: UARTn line control register

The UARTn_LCR are 32-bit registers with 32/16/8-bit access. (UART, n = 0, 1)

UART0_LCR=0x4000_400C, UART1_LCR=0x4000_410C

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="25">Reserved</td><td>BREAK</td><td>STICKP</td><td>PARITY</td><td>PEN</td><td>STOPBIT</td><td colspan="2">DLEN</td></tr>
<tr><td colspan="25">-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">00</td></tr>
<tr><td colspan="25">-</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td><td colspan="2">RW</td></tr>
</table>

6	BREAK	Transfer Break Control bit. The TXDn pin will be driven at low state in order to notice the alert to the receiver.	
		0	Normal transfer mode.
		1	Break transmit mode.
5	STICKP	Force Parity bit. This bit is effective when the PEN bit is set to "1b".	
		0	Disable parity stuck.
		1	Enable parity stuck. A parity is always the value of the PARITY bit.
4	PARITY	Parity Mode and Parity Stuck Selection bit.	
		0	Odd parity mode.
		1	Even parity mode.
3	PEN	Parity Bit Transfer Enable bit.	
		0	Disable parity transfer.
		1	Enable parity transfer.
2	STOPBIT	Stop Bit Length Selection bit.	
		0	1 stop bit.
		1	1.5 or 2 stop bit. 1.5 stop bit in case of 5-bit data length and 2 stop bit in case of 6/7/8-bit data length.
1 0	DLEN	Data Length Selection bits.	
		00	5-bit data length
		01	6-bit data length
		10	7-bit data length
		11	8-bit data length

Parity bit will be generated according to bit 3,4,5 of UARTn_LCR register. The table shows the variation of parity bit generation.

Table 54. Interrupt ID and Control

STICKP	PARITY	PEN	Parity
X	X	0	No Parity
0	0	1	Odd Parity
0	1	1	Even Parity
1	0	1	Force parity as "1"
1	1	1	Force parity as "0"

14.2.6 UARTn_DCR: UARTn data control register

The UARTn_DCR are 32-bit registers with 32/16/8-bit access. (UART, n = 0, 1)

UART0_DCR=0x4000_4010, UART1_DCR=0x4000_4110

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5	4	3	2	1 0
Reserved				LBON	RXINV	TXINV	Reserved
-				0	0	0	-
-				RW	RW	RW	-

4	LBON	Local Loopback Test Mode Enable bit.	
		0	Normal mode.
		1	Local loopback mode. TXDn connected to RXDn internally.
3	RXINV	Receive Data Inversion Selection bit.	
		0	Normal receive data input.
		1	Inverted receive data input.
2	TXINV	Transmit Data Inversion Selection bit.	
		0	Normal transmit output.
		1	Inverted transmit output.

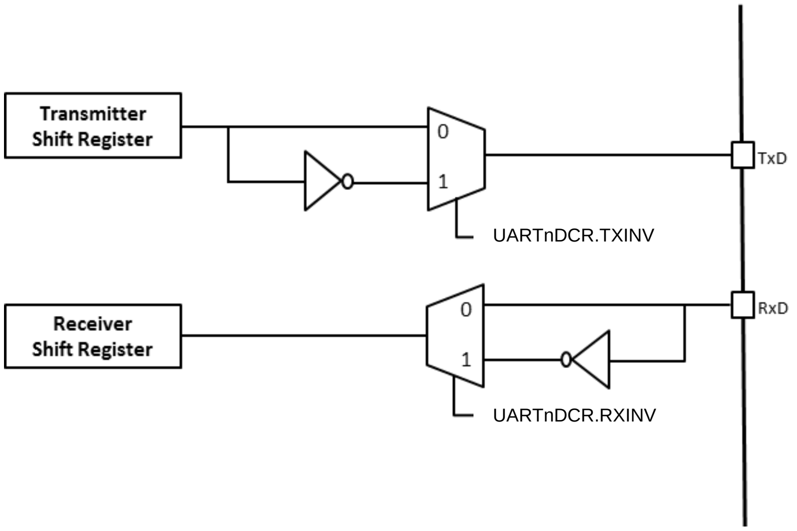


Figure 88. Data Inversion Control Diagram

14.2.7 UARTn_LSR: UARTn line status register

The UARTn_LSR are 32-bit registers with 32/16/8-bit access. (UART, n = 0, 1)

UART0_LSR=0x4000_4014, UART1_LSR=0x4000_4114

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																									TEMT	THRE	BI	FE	PE	OE	DR
-																									1	1	0	0	0	0	0
-																									RO	RO	RO	RO	RO	RO	RO

6	TEMT	Transmit Empty bit.	
		0	Transmit register has data or is transferring.
		1	Transmit register is empty.
5	THRE	Transmit Holding Empty bit.	
		0	Transmit holding register is not empty.
		1	Transmit holding register is empty
		NOTE: This bit will be set to "1b" when it starts transmit.	
4	BI	Break Condition Indication bit.	
		0	Normal status.
		1	Break condition is detected.
3	FE	Frame Error Indicator bit.	
		0	No frame error.
		1	Frame error occurs. The receive character did not have a valid stop bit.
2	PE	Parity Error Indicator bit.	
		0	No parity error.
		1	Parity error occurs. The receive character have not correct parity information.
1	OE	Overrun Error Indicator bit.	
		0	No overrun error.
		1	Overrun error occurs. Additional data arrive while the RHR is full.
0	DR	Data Receive Indicator bit.	
		0	No data in receive holding register.
		1	Data has been received and is saved in the receive holding register.

This register provides the status of data transfers between transmitter and receiver. User can get the line status information from this register and can handle the next process. Bit 1,2,3,4 will arise the line status interrupt when RLSIE bit in UARTnIEN register is set. Other bits can generate its interrupt when its interrupt enable bit in UARTnIEN register is set.

14.2.8 UARTn_BDR: UARTn baud rate divisor latch register

The UARTn_BDR are 32-bit registers with 32/16/8-bit access. (UART, n = 0, 1)

UART0_BDR=0x4000_4020, UART1_BDR=0x4000_4120

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved		BDR	
-		0x0000	
-		RW	

15 0	BDR	Baud Rate Divider Latch Value Baud rate = fUARTnCLK/(16 x BDR[15:0] x 2). **NOTE**: The UART block won't work if the BDR[15:0] ≤ 0x0003.

To establish the communication with UART channel, the baud rate should be set properly. The programmable baud rate generation is provided to give from 1 to 65535 divider number. The 16-bits divider register (UARTn_BDR) should be written for expected baud rate. UARTclock is PCLK.

Baud rate calculation formula is as below.

In case of 40 MHz UARTclock speed, the divider value and error rate is described in table

Table 55. Example of Baud Rate Calculation (without BFR)

UARTclock=48 MHz		
Baud rate	**Divider**	**Error (%)**
1200	1250	0.0%
2400	625	0.0%
4800	312	0.16%
9600	156	0.16%
19200	78	0.16%
38400	39	0.16%
57600	26	0.16%
115200	13	0.16%

14.2.9 UARTn_BFR: UARTn baud rate fraction counter register

The UARTn_BFR are 32-bit registers with 32/16/8-bit access. (UART, n = 0, 1)

UART0_BFR=0x4000_4024, UART1_BFR=0x4000_4124

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved			BFR
-			0x00
-			RW

7 0	BFR	Fraction Counter value.	
		0	Disable fraction counter.
		N	Fraction compensation mode is operating. Fraction counter is incremented by FCNT.
		NOTE:	8-bit fractional counter will count up by FCNT value every (baud rate)/16 period and whenever fractional counter overflow is happen, the divisor value will increment by 1. So this period will be compensated. Then next period, the divisor value will return to original set value.

Table 56. Example of Baud Rate Calculation

UARTclock =48 MHz			
Baud rate	**Divider**	**FCNT**	**Error (%)**
1200	1250	0	0.00%
2400	625	0	0.00%
4800	312	128	0.00%
9600	156	64	0.00%
19200	78	32	0.00%
38400	39	16	0.00%
57600	26	10	0.01%
115200	13	5	0.01%

FCNT value can be calculated above equation. For example, if the target baud rate is 4800 bps and UARTclock is 48MHz case, the BDR value is 312.5. The integer number 312 should be the BDR value and the FCNT value can be calculated by the floating number 0.5 as below.

FCNT = 0.5 * 256 = 128, so the FCNT value is 128.

8-bit fractional counter will be counted up by FCNT value every (baud rate)/16 periods and whenever fractional counter overflow is happened, the divider value will be incremented by 1. So this period will be compensated. Then in next period, the divider value will return to original set value.

14.2.10 UARTn_IDTR: UARTn inter-frame delay time register

The UARTn_IDTR are 32-bit registers with 32/16/8-bit access. (UART, n = 0, 1)

UART0_IDTR=0x4000_4030, UART1_IDTR=0x4000_4130

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="24">Reserved</td><td>SMS</td><td>DMS</td><td colspan="3">Reserved</td><td colspan="3">WAITVAL</td></tr>
<tr><td colspan="24">-</td><td>0</td><td>0</td><td colspan="3">-</td><td colspan="3">000</td></tr>
<tr><td colspan="24">-</td><td>RW</td><td>RW</td><td colspan="3">-</td><td colspan="3">RW</td></tr>
</table>

7	SMS	Start Bit Multi Sampling Enable bit.	
		0	Multi sampling is disable for start bit, Single sample will be done at 8/16 baud rate for the start bit.
		1	Multi sampling is enabled for start bit. Sampling is done 3 times at 7/16, 8/16 and 9/16 baud rate. Dominant value of 3 samples will be selected for the start bit.
6	DMS	Data Bit Multi sampling enable.	
		0	Multi sampling is disable for data bit, Single sample will be done at 8/16 baud rate for the data bit.
		1	Multi sampling is enabled for data bit. Sampling is done 3 times at 7/16, 8/16 and 9/16 baud rate. Dominant value of 3 samples will be selected for the data bit.
2 0	WAITVAL	Wait Time Value. Dummy delay can be inserted between 2 Continuous Transmits.	
		Wait Time = WAITVAL[2:0]/(Baud Rate)	

14.3 Functional description

The UART module of the A31T214/216 is compatible with 16450 UART. Additionally, fractional baud rate compensation logic is provided. It does not have an internal FIFO block.

14.3.1 Receiver sampling timing

The UART module operates according to the sampling timing shown in Figure 89.

If the falling edge on the receive line, UART judges as the start bit. From the start timing, UART oversamples 16 times of 1-bit and detect the bit value at the 8th sample of 16 samples.

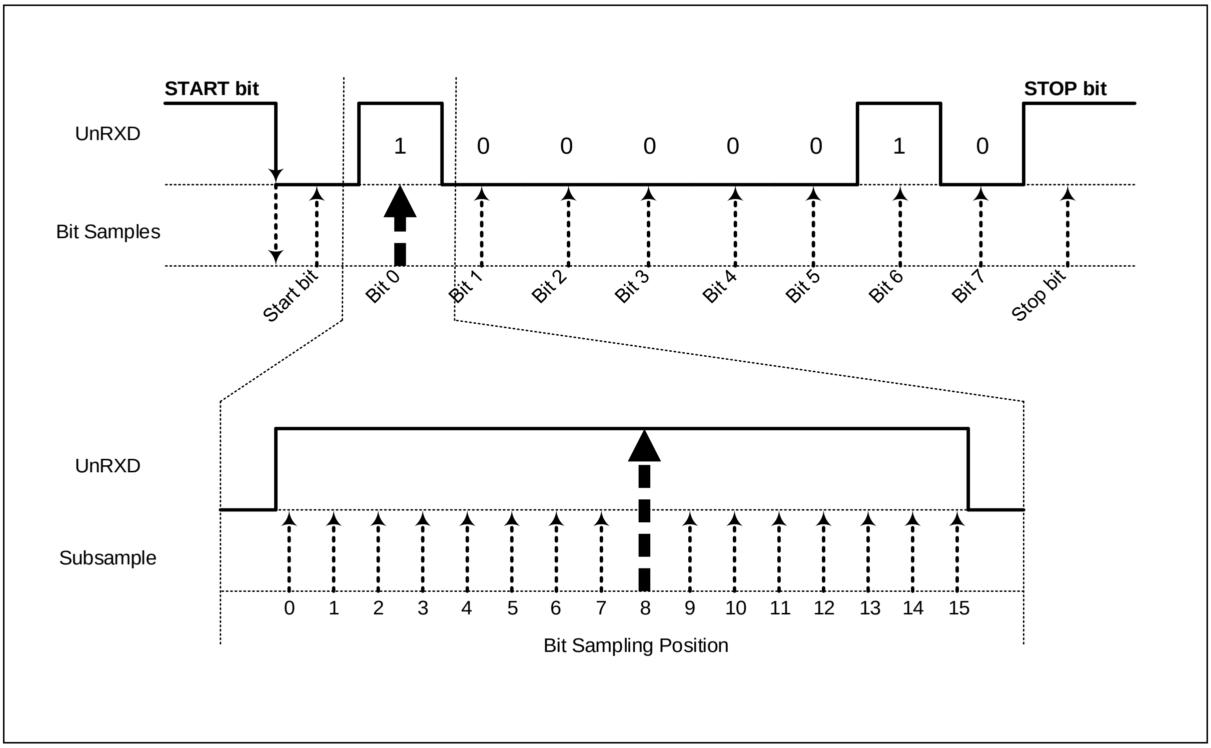


Figure 89. The Sampling Timing of UART Receiver

It is recommended to enable debounce settings in the PCU block to reinforce the immunity of external input glitch noise.

14.3.2 Transmitter

The transmitter has a data transmission function. The start bit, data bits, optional parity bit, and stop bit shift in series, shifting the least significant bit first.

The number of data bit is selected in the UARTn_LCR<DLEN> bits.

The parity bit is set according to the PARITY and PEN bit filed in UARTn_LCR register. If the parity type is even, the parity bit depends on one-bit sum of all data bits. For odd parity, the parity bit is an inverted sum of all data bits.

The number of stop bits is selected in the UARTn_LCR<STOPBIT> bit.

Figure 90 shows an example of transmission data format.

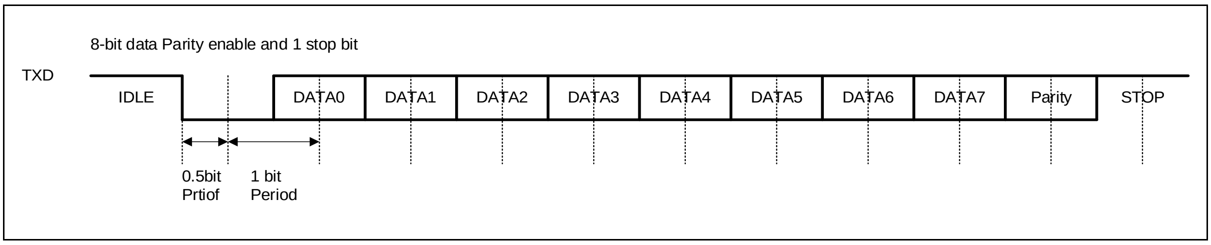


Figure 90. Example of Transmit Data Format

14.3.3 Inter-frame delay transmission

The inter-frame delay function allows the transmitter to insert an idle state on the TXD line between 2 characters. The width of the idle state is defined in WAITVAL field of the UARTn_IDTR register. When this field is set as 0, no time-delay is generated. Otherwise, the transmitter holds a high level on TXD after each transmitted character during the number of bit periods defined in WATIVAL field.

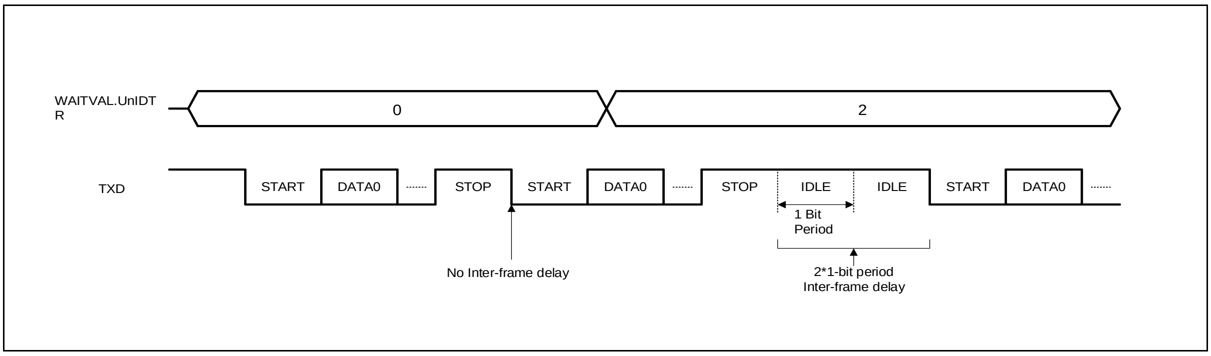


Figure 91. Inter-frame Delay Timing Diagram

14.3.4 Transmit interrupt

The transmit operation makes some kind of interrupt flags. When transmitter holding register is empty, the THRE interrupt flag will be set. When transmitter shifter register is empty, the TXE interrupt flag will be set. User can select which interrupt timing is best for the application.

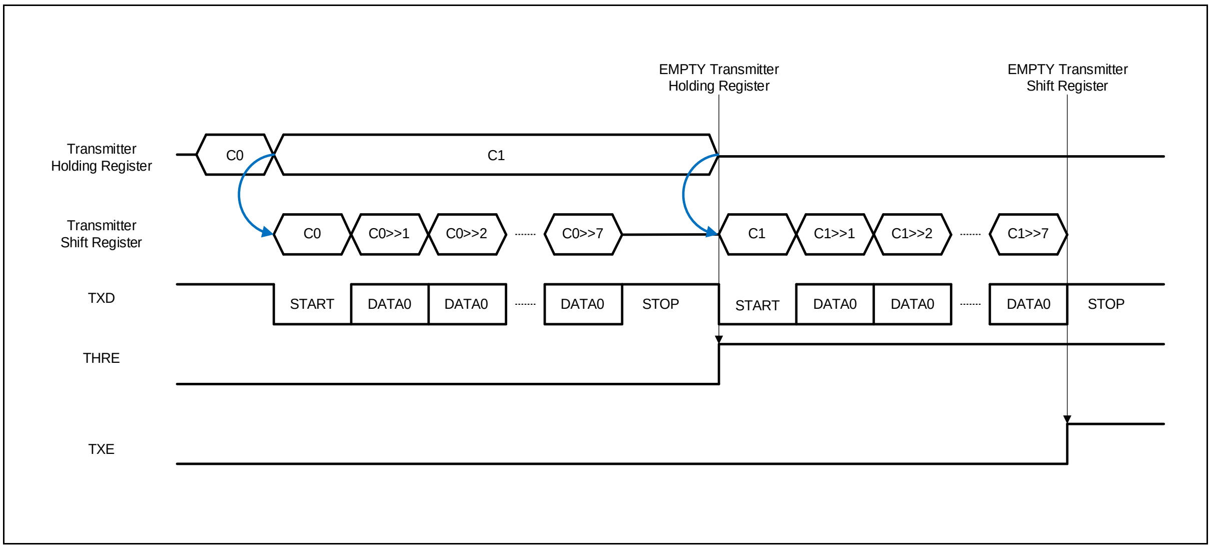


Figure 92. Transmit Interrupt Timing Diagram

15 I2C interface

I2C is one of industrial standard serial communication protocols, and which uses 2 bus lines such as Serial Data Line (SDAn) and Serial Clock Line (SCLn) to exchange data. Because both SDAn and SCLn lines are open-drain output, each line needs pull-up resistor respectively.

I2C features the followings (n = 0 and 1):

- Compatible with I2C bus standard.
- Multi-master operation.
- Up to 1MHz data transfer read speed.
- 7-bit address.
- Support two slave address.
- Both master and slave operation.
- Bus busy detection

Table 57 introduces pins assigned for I2C interface.

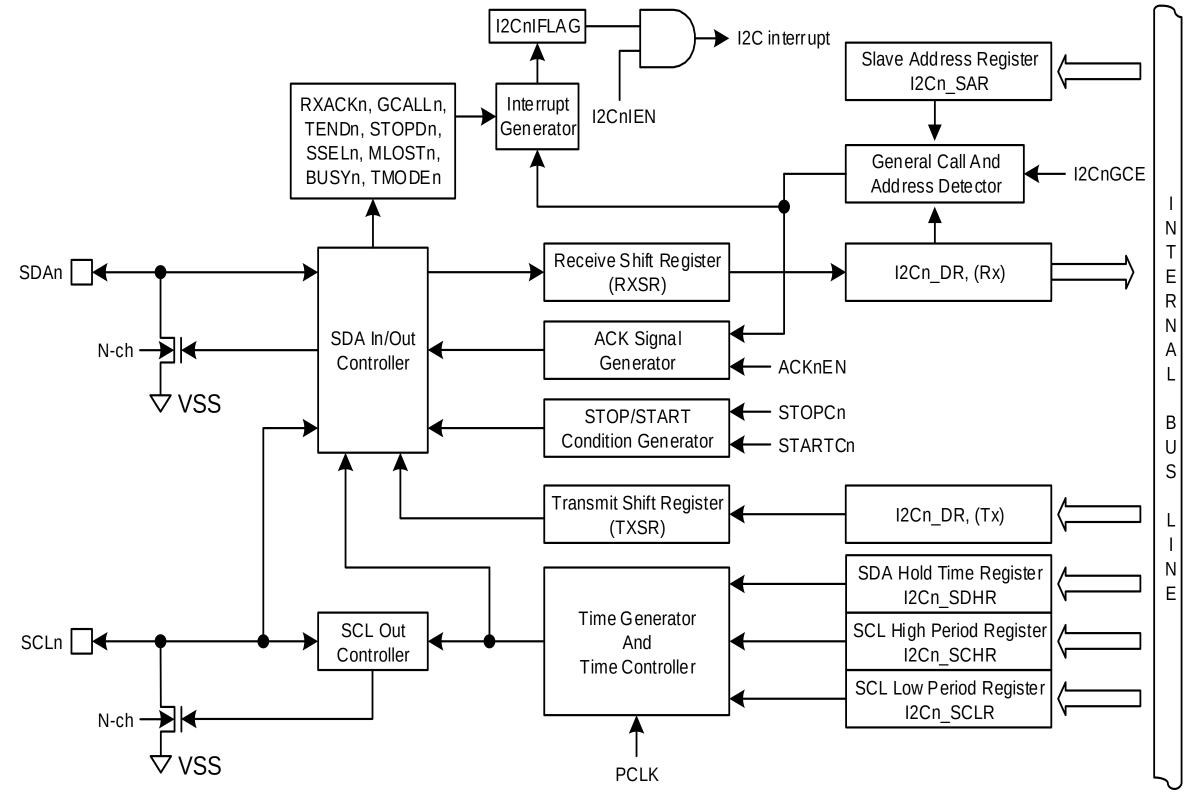
Table 57. Pin Assignment of I2C: External Pins

Pin name	Type	Description
SCL0	I/O	I2C channel 0 Serial clock bus line (open-drain)
SDA0	I/O	I2C channel 0 Serial data bus line (open-drain)
SCL1	I/O	I2C channel 1 Serial clock bus line (open-drain)
SDA1	I/O	I2C channel 1 Serial data bus line (open-drain)

NOTE: n = 0 and 1

15.1 I2C block diagram

In this section, I2C interface block is described in a block diagram.



NOTE: When the corresponding port of I2C is a sub-function for SCL/SDA pin, the SCL/SDA pins are automatically set to the N-channel open-drain outputs and the input latch is read in the case of reading the pins. The corresponding pull-up resistor is determined by the control register.

Figure 93. I2C Block Diagram

15.2 Registers

Table 58 and Table 59 show base address and register map of I2C.

Table 58. Base Address of I2C Interface

Name	Base address
I2C0	0x4000_4800
I2C1	0x4000_4900

Table 59. I2C Register Map

Name	Offset	Type	Description	Reset value	Reference
I2Cn_CR	0x00	RW	I2Cn Control Register	0x0000_0000	16.2.1
I2Cn_ST	0x04	RW	I2Cn Status Register	0x0000_0000	16.2.2
I2Cn_SAR1	0x08	RW	I2Cn Slave Address Register 1	0x0000_0000	16.2.3
I2Cn_SAR2	0x0C	RW	I2Cn Slave Address Register 2	0x0000_0000	16.2.4
I2Cn_DR	0x10	RW	I2Cn Data Register	0x0000_0000	16.2.5
I2Cn_SDHR	0x14	RW	I2Cn SDA Hold Time Register	0x0000_0001	16.2.6
I2Cn_SCLR	0x18	RW	I2Cn SCL Low Period Register	0x0000_003F	16.2.7
I2Cn_SCHR	0x1C	RW	I2Cn SCL High Period Register	0x0000_003F	16.2.8
I2Cn_SLTCR	0x20	RW	I2Cn SCL low timeout control Register	0x0000_0000	16.2.9
I2Cn_SLTPDR	0x24	RW	I2Cn SCL Low Timeout Period Data Register	0x00FF_FFFF	
I2C_MBCR	0x28	RW	I2Cn Manual Bus Control Register	0x0000_030C	

NOTE: n = 0 and 1

15.2.1 I2Cn_CR: I2Cn control register

The I2Cn_CR can be set to configure I2C operation mode and simultaneously allowed for I2C transactions to be kicked off.

The I2Cn_CR are 32-bit registers with 32/16/8-bit access.

I2C0_CR=0x4000_4800, I2C1_CR=0x4000_4900

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Reserved			EN	TXDLYENB	IEN	IFLAG	ACKEN	IMASTER	STOPC	STARTC
-			0	0	0	0	0	0	0	0
-			RW	RW	RW	RO	RW	RO	RW	RW

7	EN	Activate I2Cn Block by supplying	
		0	Disable I2Cn block
		1	Enable I2Cn block
6	TXDLYENB	I2Cn_SDHR Register Control bit.	
		0	Enable I2Cn_SDHR register.
		1	Disable I2Cn_SDHR register.
5	IEN	I2Cn Interrupt Enable bit.	
		0	Disable I2Cn interrupt.
		1	Enable I2Cn interrupt.
4	IFLAG	I2Cn Interrupt Flag bit. This bit is cleared when all interrupt source bits in the I2Cn_ST register are cleared to "0b".	
		0	No request occurred.
		1	Request occurred.
3	ACKEN	Controls ACK signal generation at ninth SCL period.	
		0	No ACK signal is generated. (SDA = 1)
		1	ACK signal is generated. (SDA = 0)
NOTE: ACK signal is output (SDA = 0) for the following 3 cases. Where x = 0 and 1. 1. When received address packet equals to SLAx[6:0] bits in I2Cn_SARx register. 2. When received address packet equals to value 0x00 with GCALLn enabled. 3. When I2Cn operates as a receiver (master or slave)			
2	IMASTER	Represent Operation Mode of I2Cn. This bit is cleared to "0b" on STOP condition.	
		0	I2Cn is in slave mode.
		1	I2Cn is in master mode.
1	STOPC	STOP Condition Generation When I2Cn is master.	
		0	No effect.
		1	STOP condition is to be generated.
0	STARTC	START Condition Generation When I2Cn is master.	
		0	No effect.
		1	START or Repeated START condition is to be generated.

15.2.2 I2Cn_ST: I2Cn status register

The I2Cn_ST are 32-bit registers with 32/16/8-bit access.

I2C0_ST=0x4000_4804, I2C1_ST=0x4000_4904

31	30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
SLT	Reserved			GCALLn	TENDn	STOPDn	SSELn	MLOSTn	BUSYn	TMODEn	RXACKn
0	-			0	0	0	0	0	0	0	0
RW	-			RW	RW	RW	RW	RW	RW	RO	RW

31	SLT	This bit shows SCL low timeout status	
		0	SCL low timeout has not occurred.
		1	SCL low timeout has occurred.
7	GCALLn	This bit has different meaning depending on whether I2C is master or slave. When I2C is a master, this bit represents whether it received AACK (address ACK) from slave.	
		0	No AACK is received. (Master mode)
		1	AACK is received (Master mode). It may be set to "1b" after address transmission.
		When I2C is a slave, this bit is used to indicate general call.	
		0	General call address is not detected. (Slave mode)
		1	General call address is detected. (Slave mode)
6	TENDn	This bit is set when 1-byte of data is transferred completely.	
		0	1 byte of data is not completely transferred.
		1	1 byte of data is completely transferred.
5	STOPDn	This bit is set when a STOP condition is detected.	
		0	A STOP condition is not detected.
		1	A STOP condition is detected.
4	SSELn	This bit is set when I2C is addressed by other master.	
		0	I2C is not selected as a slave.
		1	I2C is addressed by other master and acts as a slave.
3	MLOSTn	This bit represents the result of bus arbitration in master mode.	
		0	I2C maintains bus mastership.
		1	I2C has lost bus mastership during arbitration process.
2	BUSYn	This bit reflects bus status.	
		0	I2C bus is idle, so a master can issue a START condition.
		1	I2C bus is busy.
1	TMODEn	This bit is used to indicate whether I2C is transmitter or receiver.	
		0	I2C is a receiver.
		1	I2C is a transmitter.
0	RXACKn	This bit shows the state of ACK signal.	
		0	No ACK is received.
		1	ACK is received at ninth SCL period.

NOTES:

1. The SLT, GCALLn, TENDn, STOPDn, SSELn, and MLOSTn bits can be source of interrupt.
2. When an I2C interrupt occurs except for DEEP SLEEP mode, the SCL line is held low.
3. To release SCL, Clear to "0b" all interrupt source bits in I2Cn_ST register.
4. The GCALLn, TENDn, STOPDn, SSELn, MLOSTn, and RXACKn bits are cleared when "1b" is written to the corresponding bit.

15.2.3 I2Cn_SAR1: I2Cn slave address register 1

The I2Cn_SAR1 are 32-bit registers with 32/16/8-bit access.

I2C0_SAR1=0x4000_4808, I2C1_SAR1=0x4000_4908

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1	0
Reserved			SLAn	GCALLnEN
–			0000000	0
–			RW	RW

7 1	SLAn	These bits configure the slave address 0 in slave mode.	
0	GCALLnEN	This bit decides whether I2Cn allows general call address 0 or not in I2Cn slave mode.	
		0	Ignore general call address 0.
		1	Allow general call address 0.

15.2.4 I2Cn_SAR2: I2Cn slave address register 2

The I2Cn_SAR2 are 32-bit registers with 32/16/8-bit access.

I2C0_SAR2=0x4000_480C, I2C1_SAR2=0x4000_490C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1	0
Reserved			SLAn	GCALLnEN
0x000000			0000000	0
–			RW	RW

7 1	SLAn	These bits configure the slave address 1 in slave mode.	
0	GCALLnEN	This bit decides whether I2Cn allows general call address 1 or not in I2Cn slave mode.	
		0	Ignore general call address 1.
		1	Allow general call address 1.

15.2.5 I2Cn_DR: I2Cn data register

The I2Cn_DR are 32-bit registers with 32/16/8-bit access.

I2C0_DR=0x4000_4810, I2C1_DR=0x4000_4910

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved			DATA
			0x00
			RW

7 0	DATA	The I2Cn_DR Transmit buffer and Receive buffer share the same I/O address with this DATA register. The Transmit Data Buffer is the destination for data written to the I2Cn_DR register. Reading the I2Cn_DR register returns the contents of the Receive Buffer.

15.2.6 I2Cn_SDAHR: I2Cn SDA hold time register

The I2Cn_ SDAHR are 32-bit registers with 32/16/8-bit access.

I2C0_SDHR=0x4000_4814, I2C1_SDHR=0x4000_4914

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4 3 2 1 0
Reserved			HLDT	
-			0x001	
-			RW	

11 0	HLDT	This register is used to control SDA output timing from the falling edge of SCL. Note that SDA is changed after tPCLK X (I2Cn_SDHR+2). In master mode, load half the value of I2Cn_SCLR to this register to make SDA change in the middle of SCL. In slave mode, configure this register regarding the frequency of SCL from master. The SDA is changed after tPCLK X (I2Cn_SDHR+2) in master mode. So, to ensure operation in slave mode, the value tPCLK X (I2Cn_SDHR + 2) must be smaller than the period of SCL.

15.2.7 I2Cn_SCLLR: I2Cn SCL low period register

The I2Cn_ SCLLR are 32-bit registers with 32/16/8-bit access.

I2C0_SCLR=0x4000_4818, I2C1_SCLR=0x4000_4918

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				SCLL											
-																				0x03F											
-																				RW											

11 0	SCLL	This register defines the low period of SCL in master mode. The base clock is PCLK and the period is calculated by the formula: tPCLK X (4 X I2Cn_SCLR + 2) where tPCLK is the period of PCLK.

15.2.8 I2Cn_SCLHR: I2Cn SCL high period register

The I2Cn_ SCLHR are 32-bit registers with 32/16/8-bit access.

I2C0_SCHR=0x4000_481C, I2C1_SCHR=0x4000_491C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				SCLH											
-																				0x03F											
-																				RW											

11 0	SCLH	This register defines the high period of SCL in master mode. The base clock is PCLK and the period is calculated by the formula: tPCLK X (4 X I2Cn_SCHR + 2) where tPCLK is the period of PCLK.

15.2.9 I2Cn_SLTCR: I2Cn SCL low timeout control register

The I2Cn_SLTCR are 32-bit registers. These registers support to configure SCL low timeout and interrupt function. (n=0 and 1)

I2C0_SLTCR=0x4000_4820, I2C1_SLTCR=0x4000_4920

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="30">Reserved</td><td>SLTINT</td><td>SLTEN</td></tr>
<tr><td colspan="30">-</td><td>0</td><td>0</td></tr>
<tr><td colspan="30">-</td><td>RW</td><td>RW</td></tr>
</table>

1	SLTINT	Selection of SCL Low Timeout Interrupt	
		0	Disable interrupt
		1	Enable interrupt
0	SLTEN	SCL Low Timeout Enable bit.	
		0	Disable timeout function
		1	Enable timeout function

15.2.10 I2Cn_SLTPDR: I2Cn SCL low timeout period data register

The I2Cn_SLTPDR are 32-bit registers. When the SCL low timeout function is activated, they run from the time the SCL signal goes low to the duration set by users. (n=0 and 1)

I2C0_SLTPDR=0x4000_4824, I2C1_SLTPDR=0x4000_4924

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">Reserved</td><td colspan="24">PDATA</td></tr>
<tr><td colspan="8">-</td><td colspan="24">0xFFFFFF</td></tr>
<tr><td colspan="8">-</td><td colspan="24">RW</td></tr>
</table>

23 0	PDATA	This register defines the period of SCL low timeout. The base clock is PCLK and the period is calculated by the formula : t_pclk X 4 X (PDATA+1) where t_pclk is the period of PCLK.

15.2.11 I2Cn_MBCR: I2Cn manual bus control register

The I2Cn_MBCR are 32-bit registers. They support manual control of SCL and SDA signals on I2Cn channel. (n=0 and 1)

I2C0_MBCR=0x4000_4828, I2C1_MBCR=0x4000_4928

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10	9	8	7 6 5 4	3	2	1	0
Reserved	SCLS	SDAS	Reserved	SCLO	SDAO	SCLMCE	SDAMCE
-	1	1	-	1	1	0	0
-	RO	RO	-	RW	RW	RW	RW

9	SCLS	SCL status bit.	
		0	Low
		1	High
8	SDAS	SDA status bit.	
		0	Low
		1	High
3	SCLO	SCL output data bit. (This value is valid when SCLMCE = 1)	
		0	Low
		1	High (Open-drain)
2	SDAO	SDA output data bit. (This value is valid when SDAMCE = 1)	
		0	Low
		1	High (Open-drain)
1	SCLMCE	SCL manual control enable bit.	
		0	Disable manual control
		1	Enable manual control
0	SDAMCE	SDA manual control enable bit.	
		0	Disable manual control
		1	Enable manual control

15.3 Functional description

15.3.1 I2C bit transfer

Data on the SDAn line must be stable during HIGH period of the clock, SCLn. HIGH or LOW state of the data line can only change when the clock signal on the SCLn line is LOW. The exceptions are START(S), repeated START(Sr) and STOP(P) condition where data line changes when clock line is high.

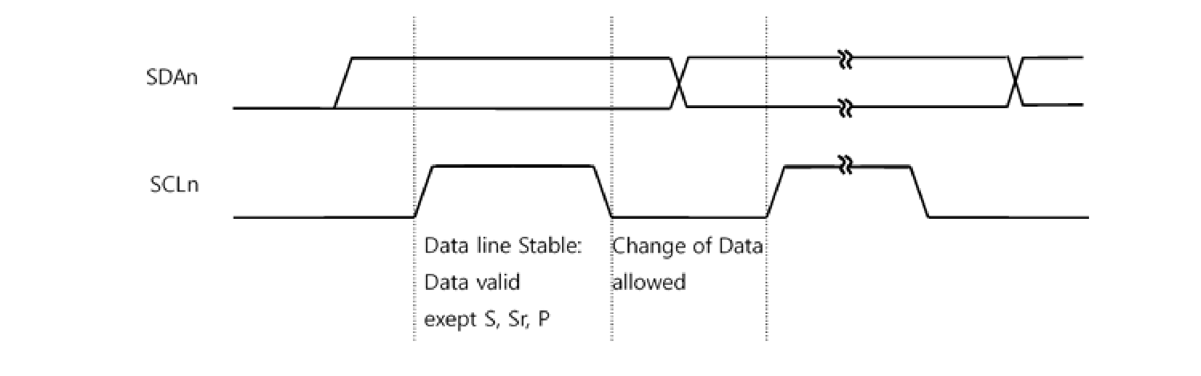


Figure 94. I2C Bus Bit Transfer (n = 0 and 1)

15.3.2 START/repeated START/STOP

One master can issue a START (S) condition to notice other devices connected to the SCLn, SDAn lines that it will use the bus. A STOP (P) condition is generated by the master to release the bus lines so that other devices can use it.

- A high to low transition on the SDAn line while SCLn is high defines a START (S) condition.
- A low to high transition on the SDAn line while SCLn is high defines a STOP (P) condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after START condition. The bus is considered to be free again after STOP condition, i.e., the bus is busy between START and STOP condition. If a repeated START condition (Sr) is generated instead of STOP condition, the bus stays busy. So, the START and repeated START conditions are functionally identical.

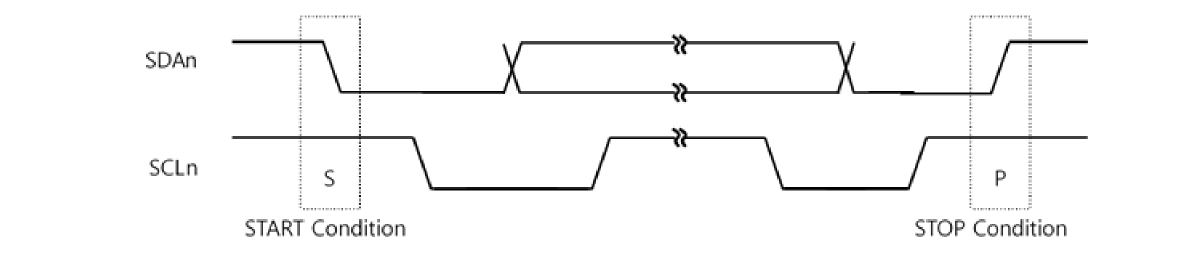


Figure 95. START and STOP Condition (n = 0 and 1)

15.3.3 Data transfer

Every byte put on the SDAn line must be 8-bits long. The number of bytes that can be transmitted per transfer is unlimited. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.

If a slave can't receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCLn LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCLn.

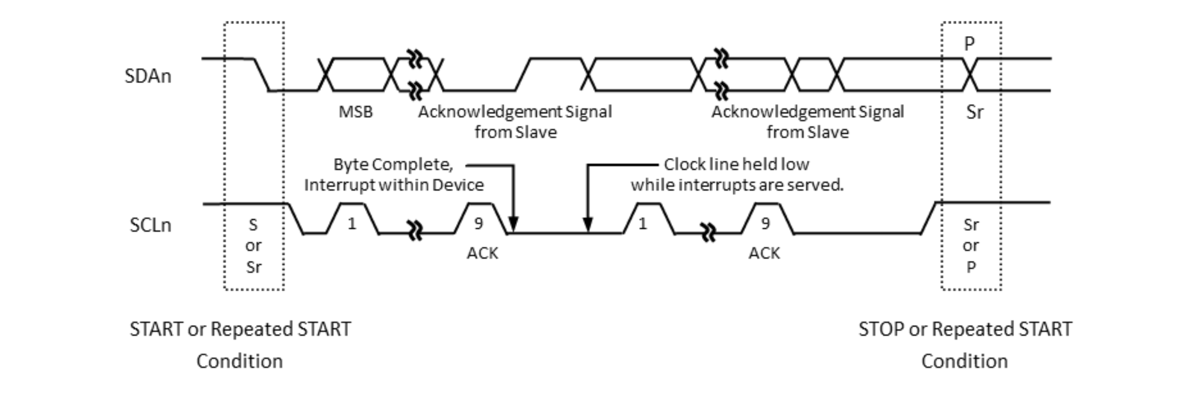

SDAn
P
MSB
Acknowledgement Signal from Slave
Acknowledgement Signal from Slave
Sr
Byte Complete, Interrupt within Device
Clock line held low while interrupts are served.
SCLn
S or Sr
1
9
ACK
1
9
ACK
Sr or P
START or Repeated START Condition
STOP or Repeated START Condition

Figure 96. I2C Bus Data Transfer (n = 0 and 1)

15.3.4 Acknowledge

The acknowledge related clock pulse is generated by the master. The transmitter releases the SDAn line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDAn line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse. When a slave is addressed by a master (Address Packet), and if it is unable to receive or transmit because it's performing some real time function, the data line must be left HIGH by the slave.

And also, when a slave addressed by a master is unable to receive more data bits, the slave receiver must release the SDAn line (Data Packet). The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

If a master receiver is involved in a transfer, it must signal the end of data to the slave transmitter by not generating any acknowledge on the last byte that was clocked out of the slave. The slave transmitter must release the data line to allow the master to generate a STOP or repeated START condition.

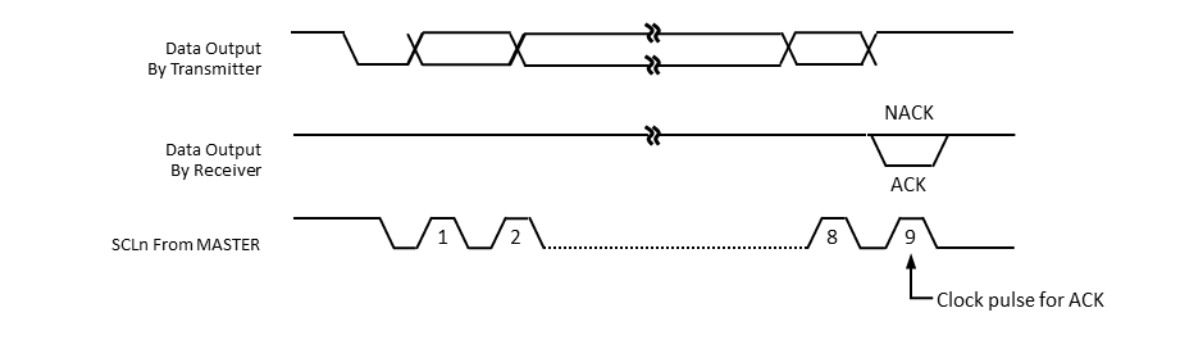


Figure 97. I2C Bus Acknowledge (n = 0 and 1)

15.3.5 Synchronization/arbitration

Clock synchronization is performed using the wired-AND connection of I2C interfaces to the SCLn line. This means that a HIGH to LOW transition on the SCLn line will cause the devices concerned to start counting off their LOW period and it will hold the SCLn line in that state until the clock HIGH state is reached. However the LOW to HIGH transition of this clock may not change the state of the SCLn line if another clock is still within its LOW period. In this way, a synchronized SCLn clock is generated with its LOW period determined by the device with the longest clock LOW period, and its HIGH period determined by the one with the shortest clock HIGH period.

A master may start a transfer only if the bus is free. Two or more masters may generate a START condition. Arbitration takes place on the SDAn line, while the SCLn line is at the HIGH level, in such a way that the master which transmits a HIGH level, while another master is transmitting a LOW level will switch off its DATA output state because the level on the bus doesn't correspond to its own level. Arbitration continues for many bits until a winning master gets the ownership of I2C bus. Its first stage is comparison of the address bits.

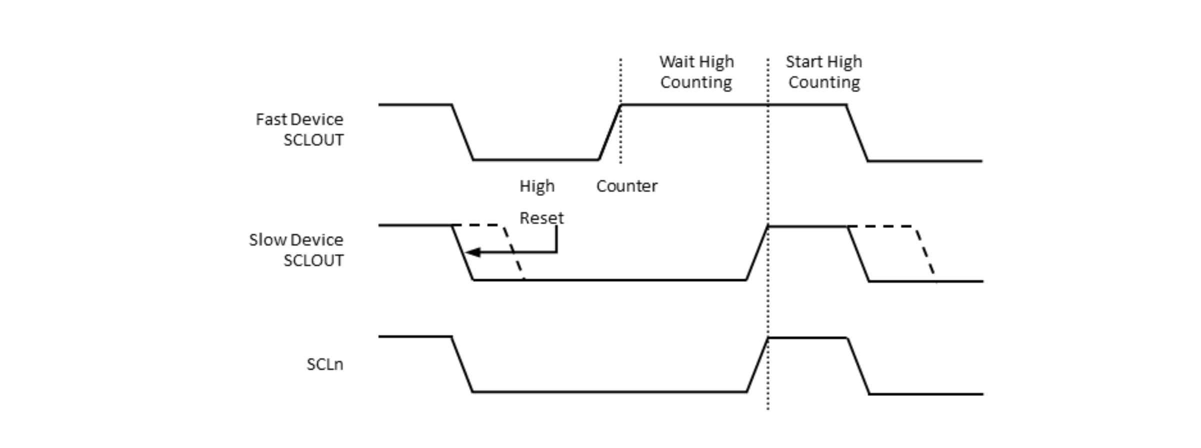


Figure 98. Clock Synchronization during the Arbitration Procedure (n = 0 and 1)

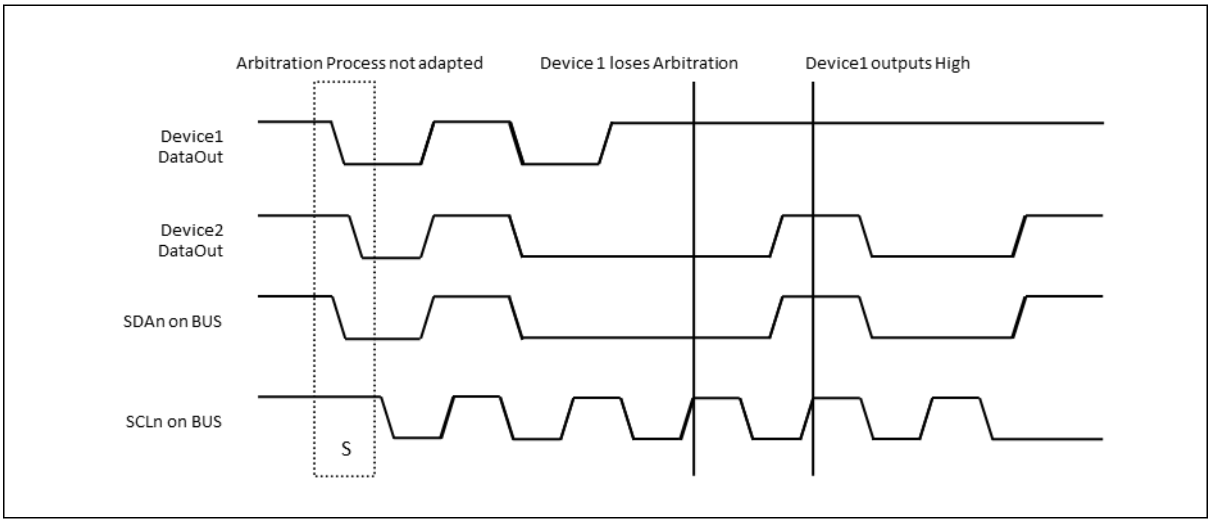


Figure 99. Arbitration Procedure between Two Masters (n = 0 and 1)

15.3.6 I2C operation

The I2C is byte-oriented and interrupt based. Interrupts are issued after all bus events except for a transmission of a START condition. Because the I2C is interrupt based, the application software is free to carry on other operations during an I2C byte transfer.

Note that when an I2C interrupt is generated, I2CnIFLAG flag in I2CnIEN register is set, it is cleared when all interrupt source bits in the I2Cn_ST register are cleared to "0b". When I2C interrupt occurs, the SCLn line is hold LOW until clearing "0b" all interrupt source bits in I2Cn_ST register. When the I2CnIFLAG flag is set, the I2Cn_ST contains a value indicating the current state of the I2C bus. According to the value in I2Cn_ST, software can decide what to do next.

I2C can operate in 4 modes by configuring master/slave, transmitter/receiver. The operating mode is configured by a winning master. A more detailed explanation follows below. (n = 0 and 1)

Master transmitter

To operate I2C in master transmitter, follow the recommended steps below:

1. Enable I2C by setting I2CnEN bit in I2Cn_CR. This provides main clock to the peripheral.
2. Load SLA+W into the I2Cn_DR where SLA is address of slave device and W is transfer direction from the viewpoint of the master. For master transmitter, W is ‘0’. Note that I2Cn_DR is used for both address and data.
3. Configure baud rate by writing desired value to both I2Cn_SCLR and I2Cn_SCHR for the Low and High period of SCLn line.
4. Configure the I2Cn_SDHR to decide when SDAn changes value from falling edge of SCLn. If SDA should change in the middle of SCLn LOW period, load half the value of I2Cn_SCLR to the I2Cn_SDHR.
5. Set the STARTCn bit in I2Cn_CR. This transmits a START condition. And also configure how to handle interrupt and ACK signal. When the STARTCn bit is set, 8-bit data in I2Cn_DR is transmitted out according to the baud-rate.
6. This is ACK signal processing stage for address packet transmitted by master. When 7-bit address and 1-bit transfer direction is transmitted to target slave device, the master can know whether the slave acknowledged or not in the 9th high period of SCLn. If the master gains bus mastership, I2C generates GCALL interrupt regardless of the reception of ACK from the slave device. When I2C loses bus mastership during arbitration process, the MLOSTn bit in I2Cn_ST is set, and I2C waits in idle state or can be operate as an addressed slave. To operate as a slave when the MLOSTn bit in I2Cn_ST is set, the ACKnEN bit in I2Cn_CR must be set and the received 7-bit address must equal to the SLAn bits in I2Cn_SAR1/2.
   In this case I2C operates as a slave transmitter or a slave receiver (go to appropriate section).
   In this stage, I2C holds the SCLn LOW. This is because to decide whether I2C continues serial transfer or stops communication. The following steps continue assuming that I2C does not lose mastership during first data transfer.

   I2C (master) can choose one of the following cases regardless of the reception of ACK signal from slave.

   Case 1. Master receives ACK signal from slave, so continues data transfer because slave can receive more data from master. In this case, load data to transmit to I2Cn_DR.

   Case 2. Master stops data transfer even if it receives ACK signal from slave. In this case, set the STOPC bit in I2Cn_CR.

Case 3. Master transmits repeated START condition with not checking ACK signal. In this case, load SLA+R/W into the I2Cn_DR and set STARTCn bit in I2Cn_CR.

After doing one of the actions above, clear all interrupt source bits in I2Cn_ST to "0b" to release SCLn line.

For the Case 1, move to step 7. For the Case 2, move to step 9 to handle STOP interrupt. For the Case 3, move back to step 6 after transmitting the data in I2Cn_DR and if transfer direction bit is '1' go to master receiver section.

7. 1-Byte of data is being transmitted. During data transfer, bus arbitration continues.

8. This is ACK signal processing stage for data packet transmitted by master. I2C holds the SCLn LOW. When I2C loses bus mastership while transmitting data arbitrating other masters, the MLOSTn bit in I2Cn_ST is set. If then, I2C waits in idle state. When the data in I2Cn_DR is transmitted completely, I2C generates TENDn interrupt.

   I2C can choose one of the following cases regardless of the reception of ACK signal from slave.

   Case A. Master receives ACK signal from slave, so continues data transfer because slave can receive more data from master. In this case, load data to transmit to I2Cn_DR.

   Case B. Master stops data transfer even if it receives ACK signal from slave. In this case, set the STOPCn bit in I2CnCR.

   Case C. Master transmits repeated START condition with not checking ACK signal. In this case, load SLA+R/W into the I2Cn_DR and set the STARTCn bit in I2Cn_CR.

   After doing one of the actions above, clear all interrupt source bits in I2Cn_ST to "0b" to release SCL line. For the Case A, move back to step 7. For the Case B, move to step 9 to handle STOP interrupt. For the Case C, move back to step 6 after transmitting the data in I2C_DR, and if transfer direction bit is '1' go to master receiver section.

9. This is the final step for master transmitter function of I2C, handling STOP interrupt. The STOP bit indicates that data transfer between master and slave is over. To clear I2Cn_ST, write "0" to I2CnST. After this, I2C enters in idle state.

Master receiver

To operate I2C in master receiver, follow the recommended steps below:

1. Enable I2C by setting I2CnEN bit in I2Cn_CR. This provides main clock to the peripheral.
2. Load SLA+R into the I2Cn_DR where SLA is address of slave device and R is transfer direction from the viewpoint of the master. For master receiver, R is ‘1’. Note that I2Cn_DR is used for both address and data.
3. Configure baud rate by writing desired value to both I2Cn_SCLR and I2Cn_SCHR for the Low and High period of SCLn line.
4. Configure the I2CnSDHR to decide when SDAn changes value from falling edge of SCLn. If SDAn should change in the middle of SCLn LOW period, load half the value of I2Cn_SCLR to the I2Cn_SDHR.
5. Set the STARTCn bit in I2Cn_CR. This transmits a START condition. And also configure how to handle interrupt and ACK signal. When the STARTCn bit is set, 8-bit data in I2Cn_DR is transmitted out according to the baud-rate.
6. This is ACK signal processing stage for address packet transmitted by master. When 7-bit address and 1-bit transfer direction is transmitted to target slave device, the master can know whether the slave acknowledged or not in the 9th high period of SCLn. If the master gains bus mastership, I2C generates GCALL interrupt regardless of the reception of ACK from the slave device. When I2C loses bus mastership during arbitration process, the MLOSTn bit in I2Cn_ST is set, and I2C waits in idle state or can be operate as an addressed slave. To operate as a slave when the MLOSTn bit in I2Cn_ST is set, the ACKnEN bit in I2Cn_CR must be set and the received 7-bit address must equal to the SLAn bits in I2Cn_SAR1/2. In this case I2C operates as a slave transmitter or a slave receiver (go to appropriate section). In this stage, I2C holds the SCLn LOW. This is because to decide whether I2C continues serial transfer or stops communication. The following steps continue assuming that I2C does not lose mastership during first data transfer.

   I2C (master) can choose one of the following cases according to the reception of ACK signal from slave.

   Case 1. Master receives ACK signal from slave, so continues data transfer because slave can prepare and transmit more data to master. Configure ACKnEN bit in I2Cn_CR to decide whether I2C Acknowledges the next data to be received or not.

   Case 2. Master stops data transfer because it receives no ACK signal from slave. In this case, set the STOPCn bit in I2Cn_CR.

Case 3. Master transmits repeated START condition due to no ACK signal from slave. In this case, load SLA+R/W into the I2Cn_DR and set STARTCn bit in I2Cn_CR.

After doing one of the actions above, clear all interrupt source bits in I2Cn_ST to “0b” to release SCLn line. For the Case 1, move to step 7. For the Case 2, move to step 9 to handle STOP interrupt. For the Case 3, move to step 6 after transmitting the data in I2Cn_DR and if transfer direction bit is ‘0’ go to master transmitter section.

7. 1-Byte of data is being received.

8. This is ACK signal processing stage for data packet transmitted by slave. I2C holds the SCLn LOW. When 1-Byte of data is received completely, I2C generates TENDn interrupt.

   I2C can choose one of the following cases according to the RXACKn flag in I2Cn_ST.

   Case A. Master continues to receive data from slave. To do this, set ACKnEN bit in I2Cn_CR to acknowledge the next data to be received.

   Case B. Master wants to terminate data transfer when it receives next data by not generating ACK signal. This can be done by clearing ACKnEN bit in I2Cn_CR.

   Case C. Because no ACK signal is detected, master terminates data transfer. In this case, set the STOPCn bit in I2Cn_CR.

   Case D. No ACK signal is detected, and master transmits repeated START condition. In this case, load SLA+R/W into the I2CnDR and set the STARTCn bit in I2Cn_CR.

   After doing one of the actions above, clear all interrupt source bits in I2Cn_ST to “0b” to release SCLn line. For the Case A and B, move to step 7. For the Case C, move to step 9 to handle STOP interrupt. For the Case D, move to step 6 after transmitting the data in I2Cn_DR, and if transfer direction bit is ‘0’ go to master transmitter section.

9. This is the final step for master receiver function of I2C, handling STOP interrupt. The STOP bit indicates that data transfer between master and slave is over. To clear I2Cn_ST, write “0” value to I2Cn_ST. After this, I2C enters idle state.

Slave transmitter

To operate I2C in slave transmitter, follow the recommended steps below:

1. If the main operating clock (SCLK) of the system is slower than that of SCLn, load value 0x00 into I2Cn_SDHR to make SDAn change within one system clock period from the falling edge of SCLn. Note that the hold time of SDAn is calculated by SDAH x period of SCLK where SDAH is multiple of number of SCLK coming from I2CnSDHR. When the hold time of SDAn is longer than the period of SCLK, I2C (slave) cannot transmit serial data properly.

2. Enable I2C by setting I2CnIEN bit and I2CnEN bit in I2Cn_CR. This provides main clock to the peripheral.

3. When a START condition is detected, I2C receives one byte of data and compares it with SLAn bits in I2Cn_SAR1/2. If the GCALLnEN bit in I2Cn_SAR1/2 is enabled, I2C compares the received data with value 0x00, the general call address.

4. If the received address does not equal to SLAn bits in I2Cn_SAR, I2C enters idle state i.e., waits for another START condition. Else if the address equals to SLAn bits and the ACKnEN bit is enabled, I2C generates SSELn interrupt and the SCLn line is held LOW. Note that even if the address equals to SLAn bits, when the ACKnEN bit is disabled, I2C enters idle state. When SSELn interrupt occurs, load transmit data to I2Cn_DR and clear to "0b" all interrupt source bits in I2Cn_ST to release SCLn line.

5. 1-Byte of data is being transmitted.

6. In this step, I2C generates TENDn interrupt and holds the SCLn line LOW regardless of the reception of ACK signal from master. Slave can select one of the following cases:

   Case 1. No ACK signal is detected and I2C waits STOP or repeated START condition.

   Case 2. ACK signal from master is detected. Load data to transmit into I2Cn_DR.

   After doing one of the actions above, clear all interrupt source bits in I2Cn_ST to "0b" to release SCLn line. For the Case 1, move to step 7 to terminate communication. For the Case 2, move back to step 5. In either case, a repeated START condition can be detected. For that case, move back to step 4.

7. This is the final step for slave transmitter function of I2C, handling STOP interrupt. The STOPCn bit indicates that data transfer between master and slave is over. To clear I2Cn_ST, write "0" to I2Cn_ST. After this, I2C enters idle state.

Slave receiver

To operate I2C in slave receiver, follow the recommended steps below:

1. If the main operating clock (SCLK) of the system is slower than that of SCLn, load value 0x00 into I2Cn_SDHR to make SDAn change within one system clock period from the falling edge of SCLn. Note that the hold time of SDAn is calculated by SDAH x period of SCLK where SDAH is multiple of number of SCLK coming from I2Cn_SDHR. When the hold time of SDAn is longer than the period of SCLK, I2C (slave) cannot transmit serial data properly.
2. Enable I2C by setting I2CnIEN bit in I2CnCR. This provides main clock to the peripheral.
3. When a START condition is detected, I2C receives one byte of data and compares it with SLA bits in I2C_SAR. If the GCALLnEN bit in I2Cn_SAR1/2 is enabled, I2C compares the received data with value 0x00, the general call address.
4. If the received address does not equal to SLAn bits in I2Cn_SAR1/2, I2C enters idle state i.e., waits for another START condition. Else if the address equals to SLAn bits and the ACKnEN bit is enabled, I2C generates SSELn interrupt and the SCLn line is held LOW. Note that even if the address equals to SLA bits, when the ACKnEN bit is disabled, I2C enters idle state. When SSELn interrupt occurs and I2C is ready to receive data, clear to “0b” all interrupt source bits in I2Cn_ST to release SCLn line.
5. 1-Byte of data is being received.
6. In this step, I2C generates TENDn interrupt and holds the SCLn line LOW regardless of the reception of ACK signal from master. Slave can select one of the following cases:

   Case 1. No ACK signal is detected (ACKnEN=0) and I2C waits STOP or repeated START condition.

   Case 2. ACK signal is detected (ACKnEN=1) and I2C can continue to receive data from master.

   After doing one of the actions above, clear all interrupt source bits in I2CnST to “0b” to release SCLn line. For the Case 1, move to step 7 to terminate communication. For the Case 2, move back to step 5. In either case, a repeated START condition can be detected. For that case, move back to step 4.
7. This is the final step for slave receiver function of I2C, handling STOP interrupt. The STOPCn bit indicates that data transfer between master and slave is over. To clear I2CnST, write “0” to I2CnST. After this, I2C enters idle state.

16 Serial Peripheral Interface (SPI)

A channel serial interface is provided for synchronous serial communications with external peripherals. SPI block support both of master and slave mode. Four signals will be used for SPI communication such as SS, SCK, MOSI, and MISO.

SPI of A31T214/216 series features the followings:

- Master or Slave operation.
- Programmable clock polarity and phase.
- 8, 9, 16, 17-bit wide transmit/receive register.
- 8, 9, 16, 17-bit wide data frame.
- Loop-back mode.
- Programmable start, burst, and stop delay time.
- DMA transfer operation.

Table 60 introduces pins assigned for SPI.

Table 60. Pin Assignment of SPI: External Pins

Pin name	Type	Description
SSn	I/O	SPIn Slave select input / output
SCKn	I/O	SPIn Serial clock input / output
MOSIn	I/O	SPIn Serial data (Master output, Slave input)
MISOn	I/O	SPIn Serial data (Master input, Slave output)

NOTE: n = 20 and 21

16.1 SPI block diagram

In this section, SPI is described in a block diagram in Figure 100.

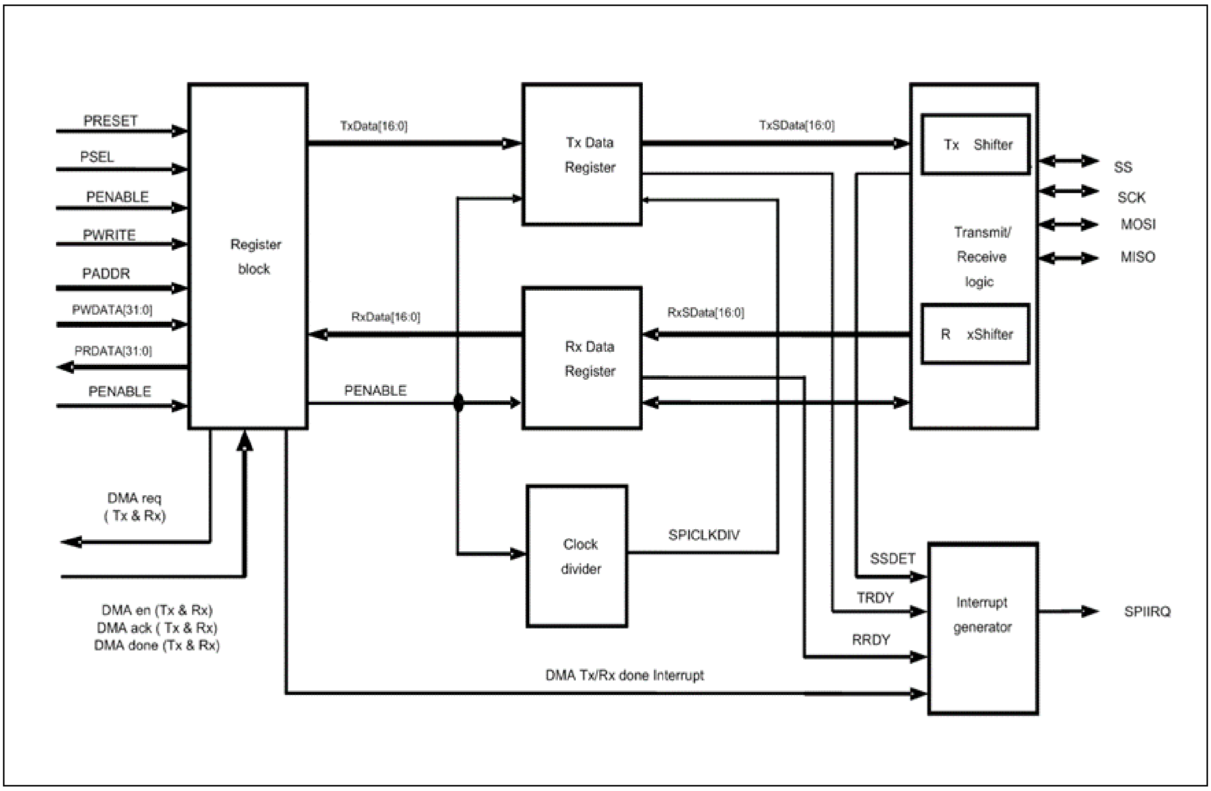


Figure 100. SPI Block Diagram

16.2 Registers

Table 61 and Table 62 show base address and register map of SPI.

Table 61. Base Address of SPI

Name	Base address
SPI20	0x4000_4C00
SPI21	0x4000_4D00

Table 62. SPI Register Map

Name	Offset	Type	Description	Reset value	Reference
SPIn.TDR	0x00	WO	SPIn Transmit Data Register	0x000000	17.2.1
SPIn.RDR	0x00	RO	SPIn Receive Data Register	0x000000	17.2.2
SPIn.CR	0x04	RW	SPIn Control Register	0x001020	17.2.3
SPIn.SR	0x08	RW	SPIn Status Register	0x000006	17.2.4
SPIn.BR	0x0C	RW	SPIn Baud rate Register	0x00FFFF	17.2.5
SPIn.EN	0x10	RW	SPIn Enable register	0x000000	17.2.6
SPIn.LR	0x14	RW	SPIn delay Length Register	0x010101	17.2.7

16.2.1 SPIn_TDR: SPI transmit data register

The SPIn_TDR are 17-bit sized read/write registers. They contain serial transmit data.

SPI20_TDR=0x4000_4C00, SPI21_TDR=0x4000_4D00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															TDR																
-															0x00000																
-															WO																

16 0	TDR	Transmit Data Register

16.2.2 SPIn_RDR: SPI receive data register

The SPIn_RDR are 17-bit sized read/write registers. They contain serial receive data.

SPI20_RDR=0x4000_4C00, SPI21_RDR=0x4000_4D00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															RDR																
-															0x00000																
-															RO																

16 0	RDR	Receive Data Register

16.2.3 SPIn_CR: SPI control register

The SPIn_CR are 20-bit sized read/write registers. They can be set to configure SPI operation mode.

SPI20_CR=0x4000_4C04, SPI21_CR=0x4000_4D04

31 30 29 28 27 26 25 24	23 22 21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 6	5	4	3	2	1 0
Reserved		TXBC	RXBC	DTXIE	DRXIE	SSCIE	TXIE	RXIE	SSMOD	SSOUT	LBE	SSMARK	SS0MO	SS0POL	Reserved	MS	MSBF	CPHA	CPOL	BITSZ
0		0	0	0	0	0	0	0	0	1	0	0	0	0	-	1	0	0	0	00
-		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	-	RW	RW	RW	RW	RW

20	TXBC	Tx buffer clear bit.	
		0	No action
		1	Clear Tx buffer
19	RXBC	Rx buffer clear bit	
		0	No action
		1	Clear Rx buffer
18	TXDIE	DMA Tx Done Interrupt Enable bit.	
		0	DMA Tx Done Interrupt is disabled.
		1	DMA Tx Done Interrupt is enabled.
17	RXDIE	DMA Rx Done Interrupt Enable bit.	
		0	DMA Rx Done Interrupt is disabled.
		1	DMA Rx Done Interrupt is enabled.
16	SSCIE	SS Edge Change Interrupt Enable bit.	
		0	nSS interrupt is disabled.
		1	nSS interrupt is enabled for both edges (L→H, H→L)
15	TXIE	Transmit Interrupt Enable bit.	
		0	Transmit Interrupt is disabled.
		1	Transmit Interrupt is enabled.
14	RXIE	Receive Interrupt Enable bit.	
		0	Receive Interrupt is disabled.
		1	Receive Interrupt is enabled.
13	SSMOD	SS Auto/Manual output select bit.	
		0	SS output is not set by SSOUT (SPInCR[12]). SS signal is in normal operation mode.
		1	SS output signal is set by SSOUT.
12	SSOUT	SS output signal select bit.	
		0	SS output is 'L.'
		1	SS output is 'H'.
11	LBE	Loop-back mode select bit in master mode.	
		0	Loop-back mode is disabled.
		1	Loop-back mode is enabled.
10	SSMASK	SS signal masking bit in slave mode.	
		0	SS signal masking is disabled. Receive data when SS signal is active.
		1	SS signal masking is enabled. Receive data at SCLK edges. SS signal is ignored.

9	SSMO	SS output signal select bit.	
		0	SS output signal is disabled.
		1	SS output signal is enabled.
8	SSPOL	SS signal Polarity select bit.	
		0	SS signal is Active-Low.
		1	SS signal is Active-High.
5	MS	Master/Slave select bit.	
		0	SPI is in Slave mode.
		1	SPI is in Master mode.
4	MSBF	MSB/LSB Transmit select bit.	
		0	LSB is transferred first.
		1	MSB is transferred first.
3	CPHA	SPI Clock Phase bit.	
		0	Sampling of data occurs at odd edges (1, 3, 5,…, 15).
		1	Sampling of data occurs at even edges (2, 4, 6,…, 16).
2	CPOL	SPI Clock Polarity bit.	
		0	Active-high clocks selected.
		1	Active-low clocks selected.
1 0	BITSZ	Transmit/Receive Data Bits select bit.	
		00	8 bits
		01	9 bits
		10	16 bits
		11	17 bits

NOTES:

1. CPOL=0, CPHA=0: data sampling at rising edge, data changing at falling edge
2. CPOL=0, CPHA=1: data sampling at falling edge, data changing at rising edge
3. CPOL=1, CPHA=0: data sampling at falling edge, data changing at rising edge
4. CPOL=1, CPHA=1: data sampling at rising edge, data changing at falling edge

16.2.4 SPIn_SR: SPI status register

The SPIn_SR are 10-bit sized read/write registers. They contain the status of SPI interface.

SPI20_SR=0x4000_4C08, SPI21_SR=0x4000_4D08

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10	9	8	7	6	5	4	3	2	1	0
Reserved	TXDMAF	RXDMAF	SBUSY	SSDET	SSON	OVRF	UDRF	TXIDLE	TRDY	RRDY
-	0	0	0	0	0	0	0	1	1	0
-	RC	RC	RO	RC	RC	RC	RC	RO	RO	RO

9	TXDMAF	DMA Transmit Operation Complete flag. (DMA to SPI)	
		0	DMA Transmit Operation is working or is disabled.
		1	DMA Transmit Operation is done.
8	RXDMAF	DMA Receive Operation Complete flag. (SPI to DMA)	
		0	DMA Receive Operation is working or is disabled.
		1	DMA Transmit Operation is done.
7	SBUSY	Transmit or receive flag	
		0	Idle state
		1	A transmission or reception is in progress.
6	SSDET	The rising or falling edge of SS signal Detect flag.	
		0	SS edge is not detected.
		1	SS edge is detected. The bit is cleared when it is written as “0”.
5	SSON	SS signal Status flag.	
		0	SS signal is inactive.
		1	SS signal is active.
4	OVRF	Receive Overrun Error flag.	
		0	Receive Overrun error is not detected.
		1	Receive Overrun error is detected. This bit is cleared by writing or reading SPInRDR.
3	UDRF	Transmit Underrun Error flag.	
		0	Transmit Underrun is not occurred.
		1	Transmit Underrun is occurred. This bit is cleared by writing or reading SPInTDR.
2	TXIDLE	Transmit/Receive Operation flag.	
		0	SPI is transmitting data
		1	SPI is in IDLE state.
1	TRDY	Transmit buffer Empty flag.	
		0	Transmit buffer is busy.
		1	Transmit buffer is ready. This bit is cleared by writing data to SPInTDR.
0	RRDY	Receive buffer Ready flag.	
		0	Receive buffer has no data.
		1	Receive buffer has data. This bit is cleared by writing data to SPInRDR.

16.2.5 SPIn_BR: SPI baud rate register

The SPIn_BR are 16-bit sized read/write registers. Baud rate can be set by writing to these registers.

SPI20.BR=0x4000_4C0C, SPI21.BR=0x4000_4D0C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																BR															
-																0xFFFF															
-																RW															

15 0	BR	Baud rate setting bits Baud Rate = PCLK / (BR + 1)

NOTES:
1. BR[15:0] must be greater than or equal to "2" (BR[15:0] >= 2)
2. For SPI speed, it is recommended to set the BR value to 2 or higher so that the SPI input clock is divided by at least 3.
e.g., PCLK = 24 MHz, BR = 2, SPI Freq. = 24MHz / (2 + 1) = 8 MHz

16.2.6 SPIn_EN: SPI enable register

The SPIn_EN are 1bit sized read/write registers. They contain the SPI enable bit.

SPI20_EN=0x4000_4C10, SPI21_EN=0x4000_4D10

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															ENABLE
-																															0
-																															RW

0	ENABLE	SPI Enable bit
		SPI is disabled. SPInSR is initialized by writing "0" to this bit but other registers aren't initialized.
		SPI is enabled. When this bit is written as "1", the dummy data of transmit buffer will be shifted. To prevent this, write data to SPTDR before this bit is active.

16.2.7 SPIn_LR: SPI delay length register

The SPIn_LR are 24-bit sized read/write registers. They contain start, burst, and stop length values.

SPI20_LR=0x4000_4C14, SPI21_LR=0x4000_4D14

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved	SPL	BTL	STL
-	0x01	0x01	0x01
-	RW	RW	RW

23 16	SPL	StoPLength value 0x01 to 0xFF: 1 to 255 SCLKs. (SPL ≥ 1)
15 8	BTL	BursTLength value 0x01 to 0xFF: 1 to 255 SCLKs. (BTL ≥ 1)
7 0	STL	STartLength value 0x01 to 0xFF: 1 to 255 SCLKs. (STL ≥ 1)

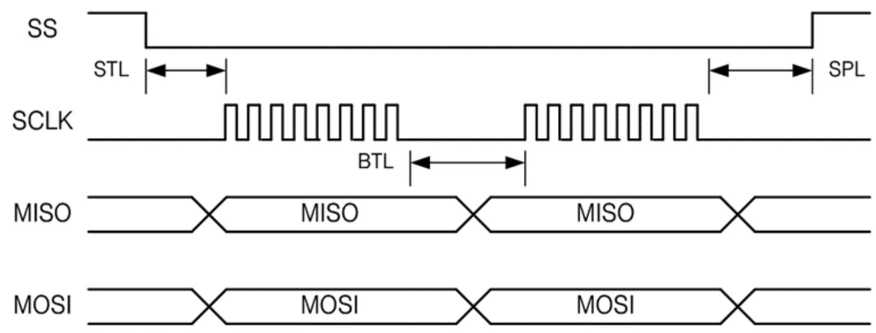


Figure 101. SPI Wave Form (STL, BTL and SPL)

16.3 Functional description

SPI's Transmit block and Receive block share a Clock Gen block, but they operate independently each other. The Transmit block and the Receive block have double buffers and SPI is available for back to back transfer operation.

16.3.1 SPI timing

SPI has four modes of operation. These modes essentially control the way data is clocked in or out of an SPI device. The configuration is done by two bits in the SPI control register (SPInCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock. The clock phase (CPHA) control bit selects one of the two fundamentally different transfer formats.

To ensure a proper communication between master and slave both devices have to run in the same mode. This can require a reconfiguration of the master to match the requirements of different peripheral slaves.

The clock polarity has no significant effect on the transfer format. Switching this bit causes the clock signal to be inverted (active high becomes active low and idle low becomes idle high). The settings of the clock phase, however, selects one of the two different transfer timings, which are described closer in the next two chapters. Since the MOSI and MISO lines of the master and the slave are directly connected to each other, the diagrams show the timing of both device, master and slave.

The nSS line is the slave select input of the slave. The nSS pin of the master is not shown in the diagrams. It has to be inactive by a high level on this pin (if configured as input pin) or by configuring it as an output pin.

The timing of a SPI transfer where CPHA is zero is shown in Figure 102 and Figure 103. Two wave forms are shown for the SCK signal -one for CPOL equals zero and another for CPOL equals one.

When the SPI is configured as a slave, the transmission starts with the falling edge of the /SS line. This activates the SPI of the slave and the MSB of the byte stored in its data register (SPInTDR) is output on the MISO line. The actual transfer is started by a software write to the SPInTDR of the master. This causes the clock signal to be generated. In cases where the CPHA equals zero, the SCLK signal remains zero for the first half of the first SCLK cycle. This ensures that the data is stable on the input lines of both the master and the slave.

The data on the input lines is read with the edge of the SCLK line from its inactive to its active. The edge of the SCLK line from its active to its inactive state (falling edge if CPOL equals zero and rising edge if CPOL equals one) causes the data to be shifted one bit further so that the next bit is output on the MOSI and MISO lines.

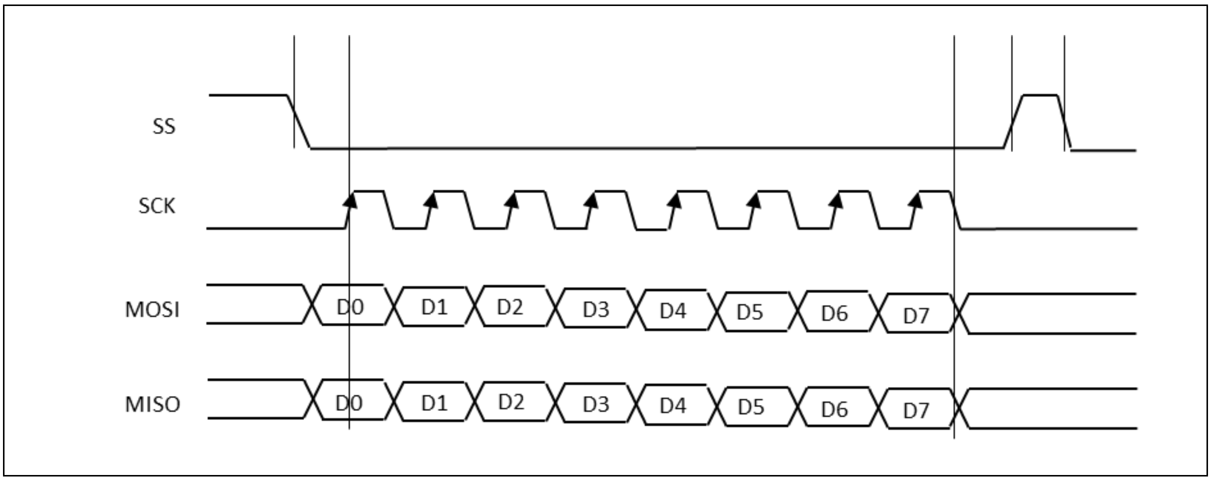


Figure 102. SPI Transfer Timing 1/4 (CPHA=0, CPOL=0, MSBF=0)

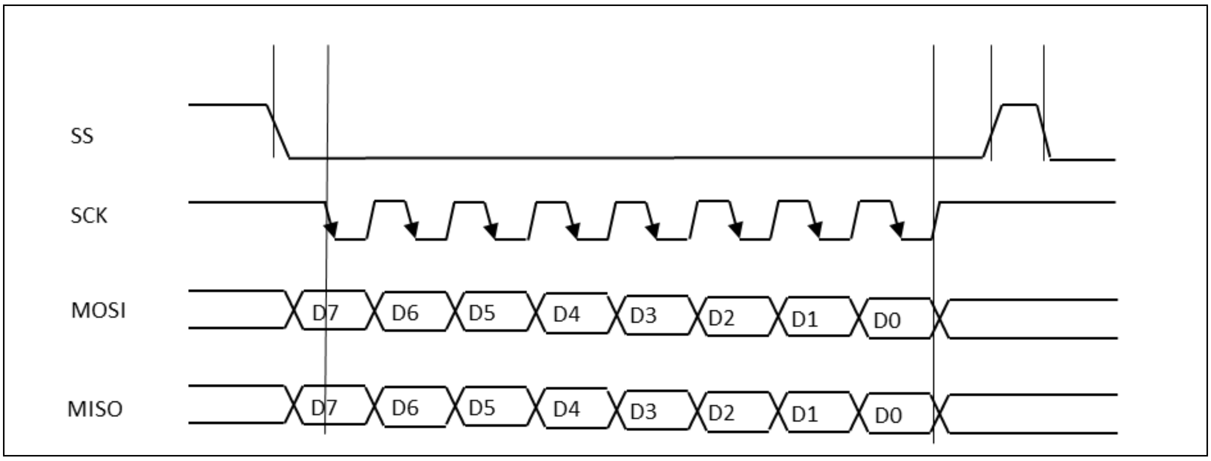


Figure 103. SPI Transfer Timing 2/4 (CPHA=0, CPOL=1, MSBF=1)

The timing of a SPI transfer where CPHA is one is shown in Figure 104 and Figure 105. Two wave forms are shown for the SCLK signal -one for CPOL equals zero and another for CPOL equals one.

Like in the previous cases the falling edge of the nSS lines selects and activates the slave. Compared to the previous cases, where CPHA equals zero, the transmission is not started and the MSB is not output by the slave at this stage. The actual transfer is started by a software write to the SPInTDR of the master what causes the clock signal to be generated. The first edge of the SCLK signal from its inactive to its active state (rising edge if CPOL equals zero and falling edge if CPOL equals one) causes both the master and the slave to output the MSB of the byte in the SPInTDR.

As shown in Figure 104 and Figure 105, there is no delay of half a SCLK-cycle. The SCLK line changes its level immediately at the beginning of the first SCLK-cycle. The data on the input lines is read with the edge of the SCLK line from its active to its inactive state (falling edge if CPOL equals zero and rising edge if CPOL equals one). After eight clock pulses the transmission is completed.

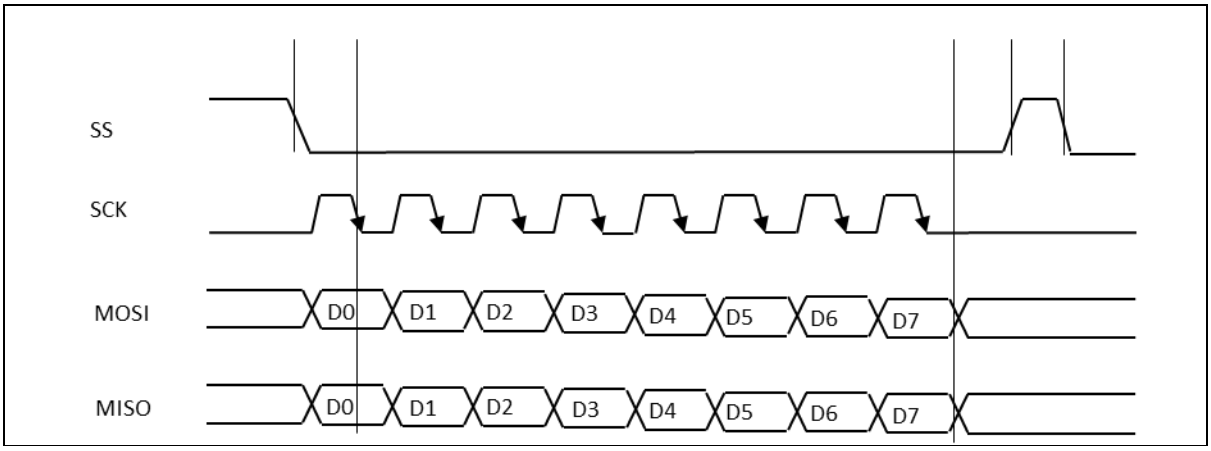


Figure 104. SPI Transfer Timing 3/4 (CPHA=1, CPOL=0, MSBF=0)

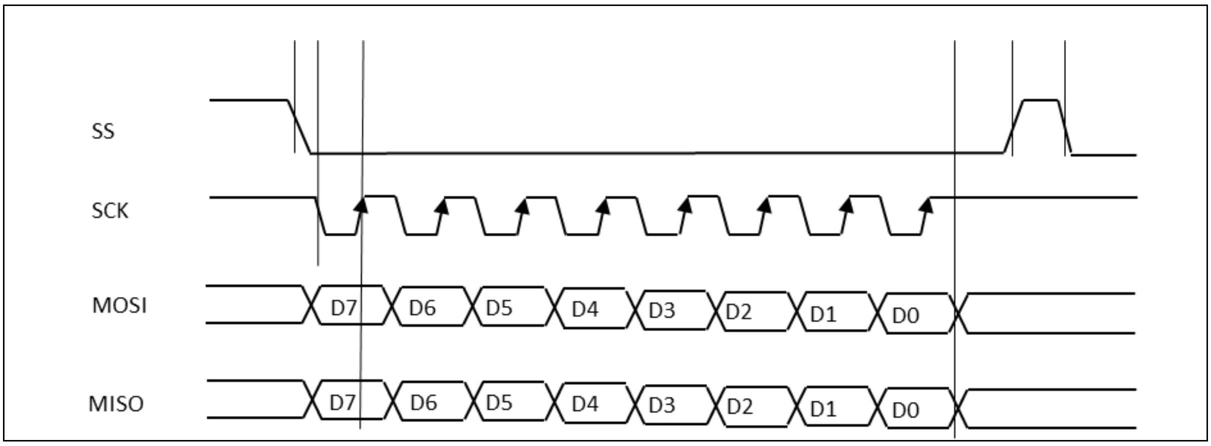


Figure 105. SPI Transfer Timing 4/4 (CPHA=1, CPOL=1, MSBF=1)

16.3.2 DMA handshake

The SPI supports DMA handshaking operation. In order to operate DMA handshake, DMA registers should be set first (see chapter 7. DMAC). As Transmitter and Receiver are independent each other, SPI can operate the two channels at the same time.

After DMA channel for receiver is enabled and receive buffer is filled, SPI sends Rx request to DMA to empty the buffer and waits ACK signal from DMA. If Receive buffer is filled again after ACK signal, SPI sends Rx request. If DMA Rx DONE becomes high, RXDMAF (SPInSR[8]) goes "1" and an interrupt is serviced when RXDIE (SPInCR[17]) is set.

Likewise, if transmit buffer is empty after DMA channel for transmitter is enabled, SPI sends Tx request to DMA to fill the buffer and waits ACK signal from DMA. If transmit buffer is empty again after ACK signal, SPI sends Tx request. If DMA Tx DONE becomes high, TXDMAF (SPInSR[9]) goes "1" and an interrupt is serviced when TXDIE (SPInCR[18]) is set.

Slave transmitter sends dummy data at the first transfer (8 to 17 SCLKs) in DMA handshake mode.

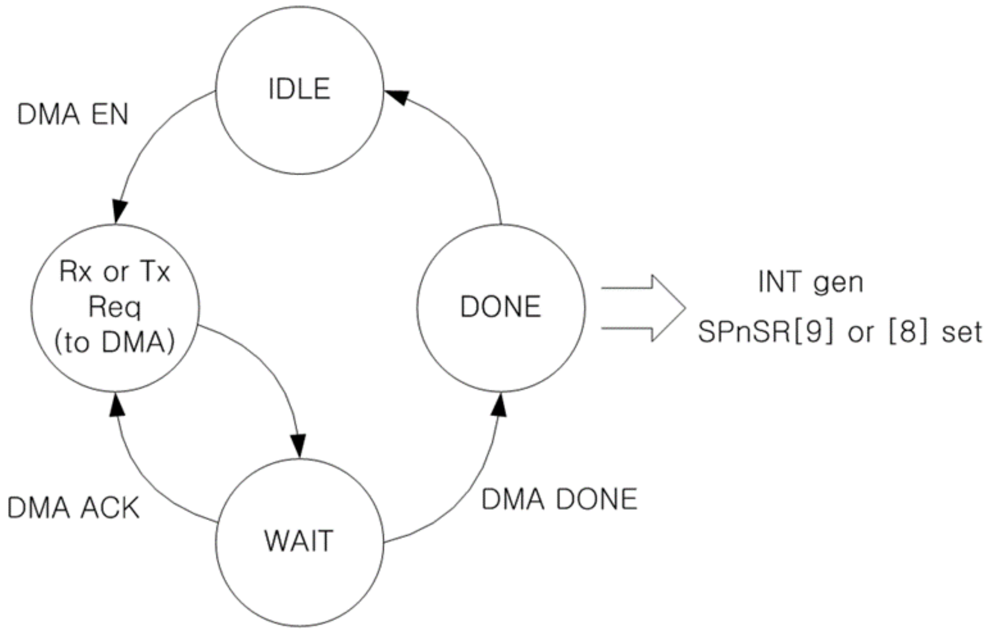


Figure 106. DMA Handshake Flow Chart

17 12-bit ADC

Analog to Digital Converter (A/D Converter) allows conversion of an analog input signal to corresponding 12-bit digital value. The A/D module has 15 analog inputs. The output of the multiplexer is the input into the converter which generates the result through successive approximation. The A/D module has three registers which are the A/D converter control register (ADC_CR), A/D converter data register (ADC_DR) and A/D converter prescaler data register (ADC_PREDR). The channels to be converted are selected by setting ADSEL[3:0]. The register ADC_DR contains the results of the A/D conversion. When the conversion is completed, the result is loaded into the ADC_DR, the A/D conversion status bit AFLAG is set to '1', and the A/D interrupt is set. During A/D conversion, AFLAG bit is read as '0'.

ADC block of A31T214/216 series consists of an independent ADC unit featuring the followings:

- 14 channels of analog inputs
- S/W (ADST) and Timer trigger: TIMER10/11/12 A match and ADC trigger signal from TIMER30 support
- Maximum 4.5MHz conversion rate (Max. 150Ksps)
- Conversion time: 30 clock
- 6-bit Prescaler

Table 63 introduces pins assigned for ADC.

Table 63. Pin Assignment of ADC: External Signal

Pin name	Type	Description
AVREF	P	Analog Reference Voltage
AN0	A	ADC Input 0
AN1	A	ADC Input 1
AN2	A	ADC Input 2
AN3	A	ADC Input 3
AN4	A	ADC Input 4
AN5	A	ADC Input 5
AN6	A	ADC Input 6
AN7	A	ADC Input 7
AN8	A	ADC Input 8
AN9	A	ADC Input 9
AN10	A	ADC Input 10
AN11	A	ADC Input 11
AN12	A	ADC Input 12
AN13	A	ADC Input 13
AN14	A	ADC Input 14

17.1 12-bit ADC block diagram

In this section, 12-bit ADC is described in a block diagram in Figure 107.

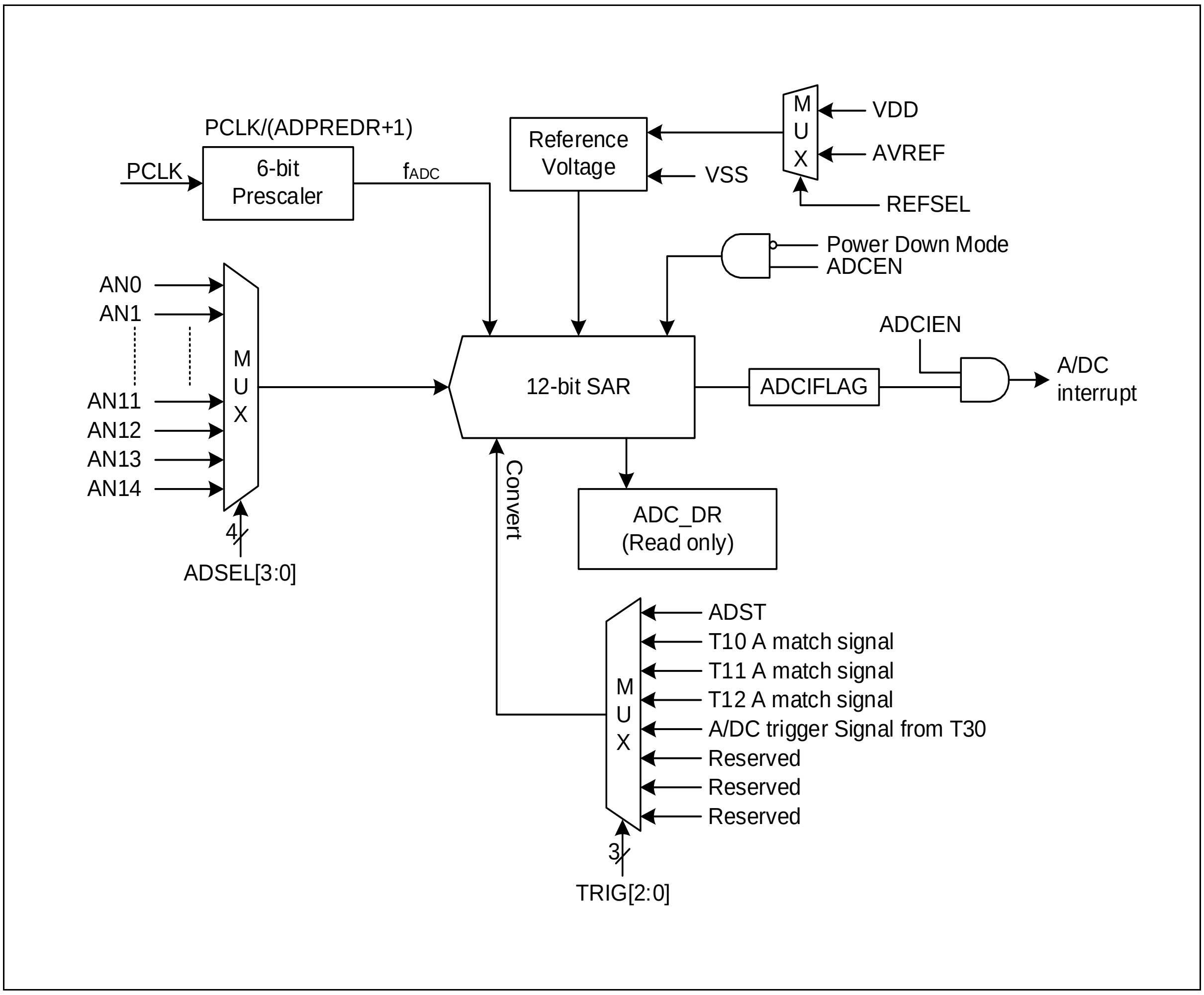


Figure 107. 12-bit ADC Block Diagram

17.2 Registers

Table 64 and Table 65 show base address and register map of the ADC unit.

Table 64. Base Address of 12-bit ADC

Name	Base address
ADC	0x4000_3000

Table 65. 12-bit ADC Register Map

Name	Offset	Type	Description	Reset value	Reference
ADC_CR	0x0000	RW	A/D Converter Control Register	0x0000_0000	18.2.1
ADC_DR	0x0004	RO	A/D Converter Data Register	0x0000_XXXX	18.2.2
ADC_PREDR	0x0008	RW	A/D Converter Prescaler Data Register	0x0000_000F	18.2.3

17.2.1 ADC_CR: A/D converter control register

The A/D Converter module should be configured properly before running.

The ADC_CR is a 32-bit register with 32/16/8-bit access.

ADC_CR=0x4000_3000

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13 12 11	10	9	8	7 6	5	4	3 2 1 0
Reserved		ADCEN	Reserved	TRIG	REFSEL	Reserved	ADST	Reserved	ADCIEN	ADCIFLAG	ADSEL
-		0	-	000	0	-	0	-	0	0	0000
-		RW	-	RW	RW	-	RW	-	RW	RW	RW

15	ADCEN	ADC Module Enable bit. (The ADC is automatically disabled at power down mode)	
		0	Disable ADC module operation.
		1	Enable ADC module operation.
13 11	TRIG	ADC Trigger Signal Selection bits.	
		000	ADST.
		001	Timer 10 A-match signal.
		010	Timer 11 A-match signal.
		011	Timer 12 A-match signal.
		100	ADC trigger signal from timer 30
		Others	Reserved
10	REFSEL	ADC Reference Selection bit.	
		0	Select analog power. (VDD)
		1	Select external reference. (AVREF)
8	ADST	ADC Conversion Start bit. This bit is automatically cleared to “0b” after operation.	
		0	No effect.
		1	Trigger signal generation for conversion start.
5	ADCIEN	ADC Interrupt Enable bit	
		0	Disable ADC interrupt
		1	Enable ADC interrupt
4	ADCIFLAG	ADC Interrupt Flag bit	
		0	No request occurred.
		1	Request occurred. This bit is cleared to ‘0’ when write ‘1’.
3 0	ADSEL	ADC Channel Selection bits.	
		0000	AN0
		0001	AN1
		0010	AN2
		0011	AN3
		0100	AN4
		0101	AN5
		0110	AN6
		0111	AN7
		1000	AN8
		1001	AN9

	1010	AN10
	1011	AN11
	1100	AN12
	1101	AN13
	1111	AN14
	Others	Reserved

17.2.2 ADC_DR: A/D converter data register

The ADC_DR is a 32-bit register with 32/16/8-bit access.

ADC_DR=0x4000_3004

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="20">Reserved</td><td colspan="12">ADDATA</td></tr>
<tr><td colspan="20">-</td><td colspan="12">0xXXX</td></tr>
<tr><td colspan="20">-</td><td colspan="12">RO</td></tr>
</table>

11 0	ADDATA	A/D Converter Result Data bits.

17.2.3 ADC_PREDR: A/D converter prescaler data register

The ADC_PREDR is a 32-bit register with 32/16/8-bit access.

ADC_PREDR=0x4000_3008

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="26">Reserved</td><td colspan="6">PRED</td></tr>
<tr><td colspan="26">-</td><td colspan="6">0x0F</td></tr>
<tr><td colspan="26">-</td><td colspan="6">RW</td></tr>
</table>

5 0	PRED	A/D Converter Prescaler Data bits.

17.3 Functional description

17.3.1 ADC conversion timing diagram

The A/D conversion process requires 2 steps to convert each bit and 30 clocks

The conversion rate is calculated as follows:

4 clocks sample time + 26 clocks conversion time = 30 clock

Conversion Time : MCLK * 30 clock = 4.5MHz * 30 = 6.67us

(Maximum 4.5MHz conversion rate)

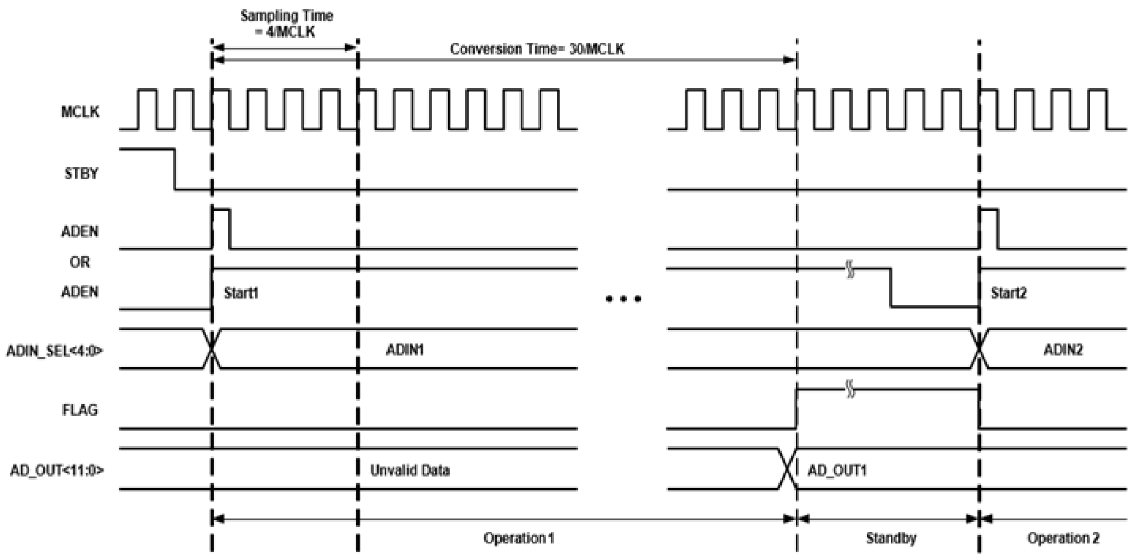


Figure 108. ADC Converter Timing Chart

18 TOUCH

Capacitive touch sensor systems are typical Human Machine Interfaces (HMI) which operate by detecting changes in electrostatic capacitance produced by the touch of a finger or other conductor.

The use of capacitive touch technology can easily improve reliability in product design, and enhance the end-user experience. It also enables manufacturing costs to be lowered in a wide range of fields such as household appliances (white goods), healthcare devices, and other electric and electronic equipment.

TOUCH of A31T214/216 series features the followings:

- 10V Conducted Susceptibility (CS) Immunity
- Self-capacitive Touch Key Sensor.
- Total 24-channel Touch Key Support.
- 16-bits Sensing Resolutions.
- Fast Initial Self Calibration.
- Key Detection Mode: Single/Multi-Mode.
- Clock Frequency during Sensing Operation: 16MHz.
- The Improvement of the SNR by Bias-Calibration in Analog Sensing Block.
- VDD Operating Voltage: 2.7V to 5.5V.
- Current Consumption: T.B.D.
- Current Consumption @STOPmode: < 1uA.
- Operation Temperature: -40℃ to +85℃.

Table 66 introduces pins assigned for TOUCH.

Table 66. Pin Assignment of TOUCH: External Signal

Pin name	Type	Description
CS0 to CS23	IA	Capacitive Touch switch input

18.1 TOUCH block diagram

Figure 109 shows a block diagram of TOUCH.

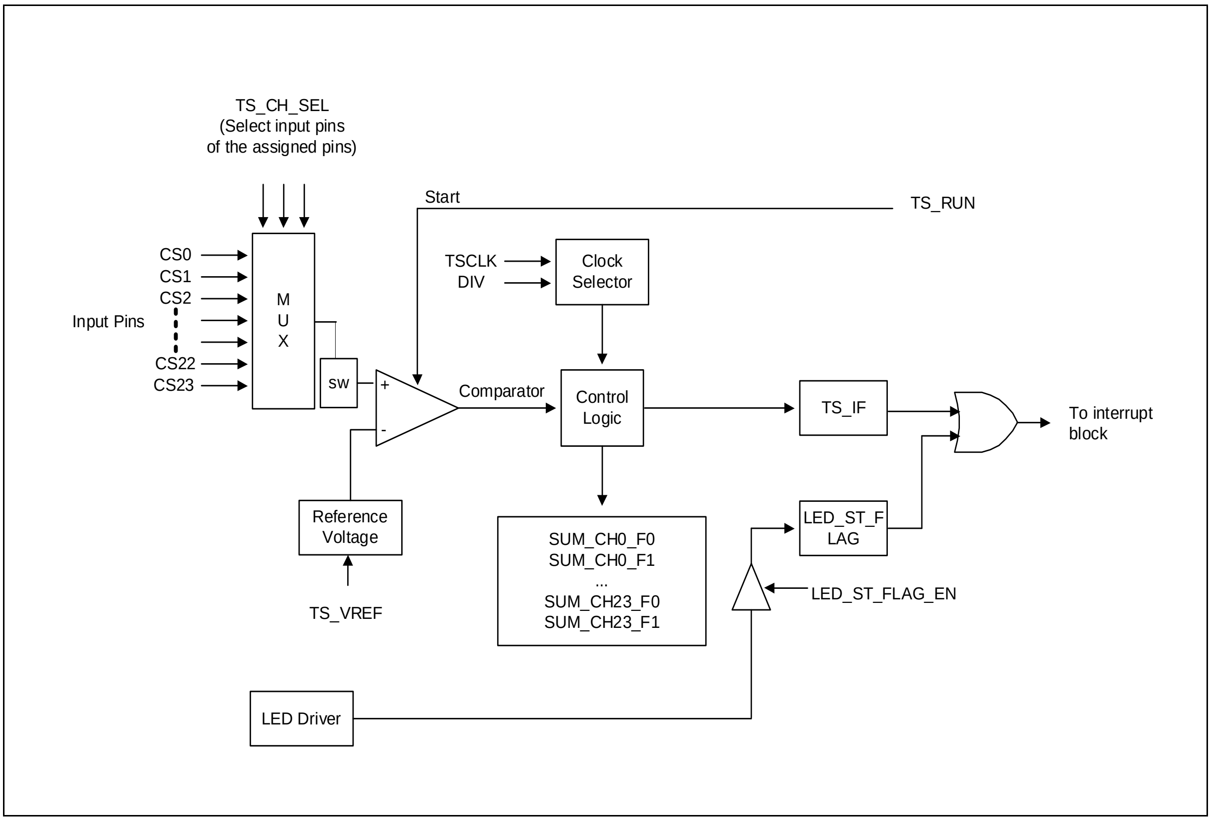


Figure 109. TOUCH Block Diagram

18.2 Registers

Table 67 and Table 68 show base address and register map of TOUCH unit.

Table 67. Base Address of TOUCH

Name	Base address
TS	0x4000_3600

Table 68. TOUCH Register Map

Name	Offset	Type	Description	Reset value	Ref.
TS_SUM_CH00_F0	0x0000	RO	Touch Sensor Channel 0 Freq0 Sum Register	0x0000_0000	
TS_SUM_CH00_F1	0x0004	RO	Touch Sensor Channel 0 Freq1 Sum Register	0x0000_0000	
TS_SUM_CH01_F0	0x0008	RO	Touch Sensor Channel 1 Freq0 Sum Register	0x0000_0000	
TS_SUM_CH01_F1	0x000C	RO	Touch Sensor Channel 1 Freq1 Sum Register	0x0000_0000	
……….					
TS_SUM_CH22_F0	0x00B0	RO	Touch Sensor Channel 22 Freq0 Sum Register	0x0000_0000	
TS_SUM_CH22_F1	0x00B4	RO	Touch Sensor Channel 22 Freq1 Sum Register	0x0000_0000	
TS_SUM_CH23_F0	0x00B8	RO	Touch Sensor Channel 23 Freq0 Sum Register	0x0000_0000	
TS_SUM_CH23_F1	0x00BC	RO	Touch Sensor Channel 23 Freq1 Sum Register	0x0000_0000	
TS_SCOn	0x00C0 to 0x011C	RW	Touch Sensor Offset Capacitor Selection Register for Channel n (0 to 23)	0x0000_0000	
TS_CON	0x0120	RW	Touch Sensor Control Register	0x0000_0000	
TS_MODE	0x0124	RW	Touch Sensor Mode Register	0x0000_0020	
TS_SUM_CNT	0x0128	RW	Touch Sensor Sum Repeat Count Register	0x0000_0001	
TS_CH_SEL	0x012C	RW	Touch Sensor Channel Selection Register	0x0000_0000	
TS_S1_WIDTH	0x0130	RW	S1 Minimum Time Register	0x0000_0015	
TS_SLP_CON	0x0134	RW	Touch Sensor Low Pass Filter Control Register	0x0000_0074	
TS_TRIM	0x0138	RW	Touch Sensor Trimming Register	0x0000_0007	

Table 68. TOUCH Register Map (continued)

Name	Offset	Type	Description	Reset value	Ref.
TS_CLK_CFG	0x013C	RW	Touch Sensor Clock Configuration Register	0x0000_0002	
TS_TRIM_OSC	0x0140	RW	Touch Sensor RING Oscillator Trimming Selection Register	0x0000_0020	
TS_DELTA_OSC	0x0144	RW	Touch Sensor RING Oscillator Delta Register	0x0000_0001	
TS_TLED	0x0148	RW	LED stable time Register	0x0000_0030	
TS_VHS	0x014C	RW	Touch Sensor High Sense Voltage Register	0x0000_0280	
TS_VREF	0x0150	RW	Touch Sensor COMP Reference Voltage Register	0x0000_0210	
SHLD_CON	0x0160	RW	Touch Shield Control Register	0x0000_0000	

18.2.1 TS_SUM_CHn_Fm: touch sensor channel n frequency m sum register

The TS_SUM_CHn_Fm is the Touch Sensor Channel n Sum Register.

TS_SUM_CH00_F0=0x4000_3600, TS_SUM_CH00_F1=0x4000_3604
TS_SUM_CH01_F0=0x4000_3608, TS_SUM_CH01_F1=0x4000_360C
TS_SUM_CH02_F0=0x4000_3610, TS_SUM_CH02_F1=0x4000_3614
TS_SUM_CH03_F0=0x4000_3618, TS_SUM_CH03_F1=0x4000_361C
TS_SUM_CH04_F0=0x4000_3620, TS_SUM_CH04_F1=0x4000_3624
TS_SUM_CH05_F0=0x4000_3628, TS_SUM_CH05_F1=0x4000_362C
TS_SUM_CH06_F0=0x4000_3630, TS_SUM_CH06_F1=0x4000_3634
TS_SUM_CH07_F0=0x4000_3638, TS_SUM_CH07_F1=0x4000_363C
TS_SUM_CH08_F0=0x4000_3640, TS_SUM_CH08_F1=0x4000_3644
TS_SUM_CH09_F0=0x4000_3648, TS_SUM_CH09_F1=0x4000_364C
TS_SUM_CH10_F0=0x4000_3650, TS_SUM_CH10_F1=0x4000_3654
TS_SUM_CH11_F0=0x4000_3658, TS_SUM_CH11_F1=0x4000_365C
TS_SUM_CH12_F0=0x4000_3660, TS_SUM_CH12_F1=0x4000_3664
TS_SUM_CH13_F0=0x4000_3668, TS_SUM_CH13_F1=0x4000_366C
TS_SUM_CH14_F0=0x4000_3670, TS_SUM_CH14_F1=0x4000_3674
TS_SUM_CH15_F0=0x4000_3678, TS_SUM_CH15_F1=0x4000_367C
TS_SUM_CH16_F0=0x4000_3680, TS_SUM_CH16_F1=0x4000_3684
TS_SUM_CH17_F0=0x4000_3688, TS_SUM_CH17_F1=0x4000_368C
TS_SUM_CH18_F0=0x4000_3690, TS_SUM_CH18_F1=0x4000_3694
TS_SUM_CH19_F0=0x4000_3698, TS_SUM_CH19_F1=0x4000_369C
TS_SUM_CH20_F0=0x4000_36A0, TS_SUM_CH20_F1=0x4000_36A4
TS_SUM_CH21_F0=0x4000_36A8, TS_SUM_CH21_F1=0x4000_36AC
TS_SUM_CH22_F0=0x4000_36B0, TS_SUM_CH22_F1=0x4000_36B4
TS_SUM_CH23_F0=0x4000_36B8, TS_SUM_CH23_F1=0x4000_36BC

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved		TS_SUM_CHn_Fm	
-		0x0000	
-		RO	

15 0	SUM_CH_DATA	Touch Sensor Channel n Frequency x Sum Register (n = 0 to 23, m = 0, 1)

Note) Frequency hopping can be used to reduce the effect of the touch sensing value due to noise. Touch sensing at two frequencies (F0, F1) instead of a single frequency, providing a sensing frequency far away from the system's noise frequencies.

18.2.2 TS_SCOn: touch sensor offset capacitor selection register for CHn

The TS_SCOn is the Touch Sensor Offset Capacitor Selection Register for CHn.

TS_SCO00=0x4000_36C0, TS_SCO01=0x4000_36C4
TS_SCO02=0x4000_36C8, TS_SCO03=0x4000_36CC
TS_SCO04=0x4000_36D0, TS_SCO05=0x4000_36D4
TS_SCO06=0x4000_36D8, TS_SCO07=0x4000_36DC
TS_SCO08=0x4000_36E0, TS_SCO09=0x4000_36E4
TS_SCO10=0x4000_36E8, TS_SCO11=0x4000_36EC
TS_SCO12=0x4000_36F0, TS_SCO13=0x4000_36F4
TS_SCO14=0x4000_36F8, TS_SCO15=0x4000_36FC
TS_SCO16=0x4000_3700, TS_SCO17=0x4000_3704
TS_SCO18=0x4000_3708, TS_SCO19=0x4000_370C
TS_SCO20=0x4000_3710, TS_SCO21=0x4000_3714
TS_SCO22=0x4000_3718, TS_SCO23=0x4000_371C

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved	SCO
-	0000_0000
-	RW

13 0	SCO	Touch Sensor Offset Capacitor Selection (n = 0 to 23)

18.2.3 TS_CON: touch sensor control register

The TS_CON is the Touch Sensor Control Register. This is an 8-bit register.

TS_CON=0x4000_3720

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4	3	2	1	0
Reserved				LED_FLAG	TS_IF	Reserved	TS_RUN
-				0	0	-	0
-				RW	RW	-	RW

3	LED_ST_FLAG	During the Touch operation, if the LED start signal occurs, the LED_ST_FLAG is set to '1'. It is available when the TS_MODE<LED_ST_FLAG_EN> bit is '1'. If this bit is '1', the Touch sensing operation may not have worked correctly due to the LED.	
		0	The LED start signal not occurs
		1	During the Touch operation, the LED start signal occurs.
2	TS_IF	Touch Sensor Interrupt Flag. To start the new sensing, this bit must be cleared after reading the SUM registers. If this bit is changed from 1 to 0, the SUM registers will be reset to 0s.	
		0	No new sensing results
		1	In normal mode, this flag indicates that the new sensing results are generated.
0	TS_RUN	Touch Sensor Enable	
		0	Touch Sensor Disable (Default)
		1	Touch Sensor Enable
NOTE:	When the LED_ST_FLAG or TS_IF is cleared, the TS_RUN is cleared 1-clock after, automatically.		

18.2.4 TS_MODE: touch sensor mode register

The TS_MODE is the Touch Sensor Mode Register. This is an 8-bit register.

TS_MODE=0x4000_3724

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15	14 13 12 11 10 9	8	7	6	5	4 3 2	1	0
Reserved	SADJ_OPT	Reserved	LED_ST_FLAG_EN	PORT_OPT	SC_GAIN	S1_SWEEP_FIX	MODE[2:0]	PORT1	PORT0
-	0	-	0	0	0	1	0	0	0
-	RW	-	RW	RW	RW	RW	RW	RW	RW

15	SADJ_OPT	Channel-Adjust path enable	
		0	Disable
		1	Enable
8	LED_ST_FLAG_EN	LED ST FLAG enable bit	
		0	LED FLAG disable
		1	LED FLAG enable
7	PORT_OPT	Determine the channel and timing to apply PORT[1:0]. If only one channel is selected, PORT[1:0] is applied to the unselected channel. When using multiple channels, it must be set to 0.	
		0	PORT[1:0] is applied to the inactive channel only during sensing.
		1	PORT[1:0] is applied to the unselected channel.
6	SC_GAIN	Gain Calibration Capacitor Enable	
		0	Gain Calibration Capacitor Disable (Default)
		1	Gain Calibration Capacitor Enable
5	S1_SWEEP_FIX	S1 width sweep fix	
		0	S1 width = TS_S1_WIDTH + random value
		1	S1 width = TS_S1_WIDTH
4 2	MODE[2:0]	Touch Sensor Mode	
		000	Normal sensing mode
		001	High sensing mode
		010	Channel Adjust sensing mode
		011	Offset Calibration sensing mode
		100	Simultaneous sensing for all selected channels to reduce the sensing time
		NOTE:	The Touch will not operate if the MODE bits are set to a value other than the above.
1 0	PORT[1:0]	Port Configuration During Inactive Status	
		00	Input Floating
		01	Output Low
		10	Output High

18.2.5 TS_SUM_CNT: touch sensor sum repeat count register

The TS_SUM_CNT is the Touch Sensor Sum Repeat Count Register. This is an 8-bit register.

TS_SUM_CNT=0x4000_3728

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved			TS_SUM_CNT
-			0000_0001
-			RW

7 0	TS_SUM_CNT	Touch Sensor Sum Repeat Count

18.2.6 TS_CH_SEL: touch sensor channel selection register

The TS_CH_SEL is the Touch Sensor Channel Selection Register.

TS_CH_SEL=0x4000_372C

31 30 29 28 27 26 25 24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	CH23_SEL	CH22_SEL	CH21_SEL	CH20_SEL	CH19_SEL	CH18_SEL	CH17_SEL	CH16_SEL	CH15_SEL	CH14_SEL	CH13_SEL	CH12_SEL	CH11_SEL	CH10_SEL	CH09_SEL	CH08_SEL	CH07_SEL	CH06_SEL	CH05_SEL	CH04_SEL	CH03_SEL	CH02_SEL	CH01_SEL	CH00_SEL
-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

	CH[23:0]_SEL	Touch Sensor Channel Selection Register	
		0	Disable (Default)
		1	Enable Touch Key

18.2.7 TS_S1_WIDTH: touch sensor S1 width register

TS_S1_WIDTH=0x4000_3730

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved			TS_S1_WIDTH
-			0x20
-			RW

7 0	TS_S1_WIDTH	Touch sensor S1 width register

18.2.8 TS_TRIM: touch sensor trimming register

TS_TRIM=0x4000_3738

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="27">Reserved</td><td>HC</td><td colspan="4">IB_TRIM[3:0]</td></tr>
<tr><td colspan="27">-</td><td>0</td><td colspan="4">0x7</td></tr>
<tr><td colspan="27">-</td><td>R
W</td><td colspan="4">RW</td></tr>
</table>

4	HC	High Current Enable	
		0	Disable
		1	Enable
3 0	IB_TRIM	Current Bias Trimming Value	
		0000	1.0uA(N)
		0001	1.5uA(N)
		0010	2.0uA(N)
		0011	2.5uA(N)
		0100	3.0uA(N)
		0101	3.5uA(N)
		0110	4.0uA(N)
		0111	4.5uA(N) (Default)
		1000	5.0uA(N)
		1001	5.5uA(N)
		1010	6.0uA(N)
		1011	6.5uA(N)
		1100	7.0uA(N)
		1101	7.5uA(N)
		1110	8.0uA(N)
		1111	8.5uA(N)

18.2.9 TS_CLK_CFG: touch sensor clock configuration register

The TS_CLK_CFG is the Touch Sensor Clock Configuration Register. This is an 8-bit register.

TS_CLK_CFG=0x4000_373C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Reserved			SCLK_EN	Reserved	CLKSEL1	CLKSEL0	Reserved	TSCLKDIV2	TSCLKDIV1	TSCLKDIV0
-			0	-	1	1	-	0	1	0
-			RW	-	RW	RW	-	RW	RW	RW

7	SCLK_EN	Select Touch Sensor Clock Source	
		0	Touch-only RING Oscillator (OSCts)
		1	MCLK
5 4	CLKSEL[1:0]	Select Touch Sensor Clock (Note2)	
		00	Touch Sensor clock 0 and Touch Sensor clock 1 are used. (F0, F1)
		01	Touch Sensor clock 0 (F0) is used only
		1x	Touch Sensor clock 1 (F1) is used only
2 0	TSCLKDIV[2:0]	Touch Sensor Clock Divider	
		000	fOSCts / 1 (16MHz)
		001	fOSCts / 2
		010	fOSCts / 4
		011	fOSCts / 8
		100	fOSCts / 16
		101	fOSCts / 32
		110	fOSCts / 64
		111	fOSCts / 128

Note) 1. After TS_RUN is cleared, please change the clock divide.

2. The touch sensing clock frequency calculation formula is as follows.

- Frequency of Touch Sensor Clock 0 (F0) =

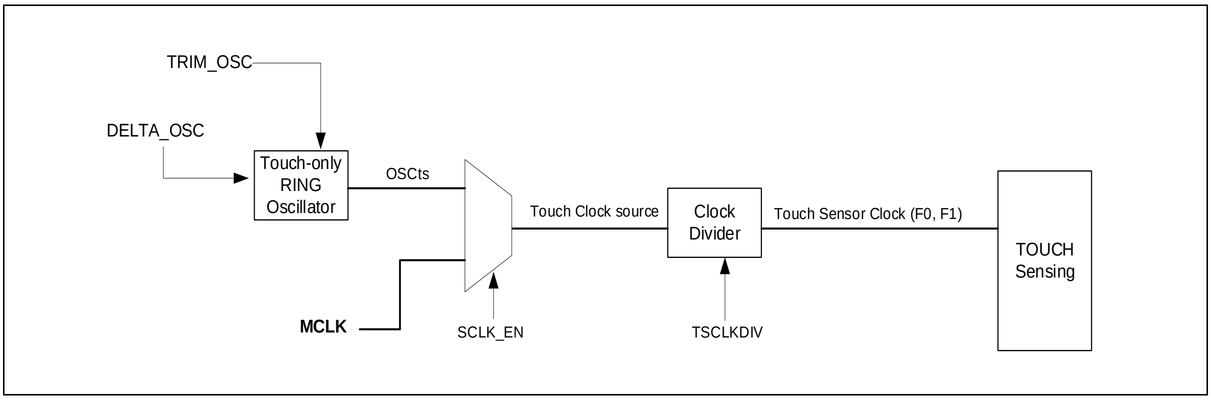
16MHz *(1+(TRIM_OSC+DELTA_OSC-20H)*0.7%) / (2^TSCLKDIV), (when TRIM_OSC + DELTA_OSC < 40H)

16MHz *(1+(TRIM_OSC+DELTA_OSC-60H)*0.7%) / (2^TSCLKDIV), (when TRIM_OSC + DELTA_OSC >= 40H)

- Frequency of Touch Sensor Clock 1 (F1) =

16 MHz*(1+(TRIM_OSC-20H)*0.7%) / (2^TSCLKDIV)

3. Touch-only RING Oscillator operates when TS_RUN=1 or TIRCCON[0]=1. If TS_RUN=1 with TIRCCON[0]=0, the Touch sensor starts to operate after 30us. (based on system clock=32MHz)



18.2.10 TS_TRIM_OSC: touch sensor RING oscillator trimming selection register

The TS_TRIM_OSC is the Touch Sensor RING Oscillator Trimming Selection Register. This is an 8-bit register.

TS_TRIM_OSC=0x4000_3740

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6	5 4 3 2 1 0
Reserved				TRIM_OSC
-				0x20
-				RW

5 0	TRIM_OSC	Touch-only RING Oscillator(OSCts) Trimming selection (Determine the F1 frequency) * bit6, bit7 must be 0	
		3FH	+21.7% (19.47MHz)
		3EH	+21%
		……	
		21H	+0.7%
		20H	16MHz (default)
		1FH	-0.7%
		……	
		01H	-21.7%
		00H	-22.4% (12.42MHz)

18.2.11 TS_DELTA_OSC: touch sensor RING oscillator delta register

TS_DELTA_OSC=0x4000_3744

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6	5 4 3 2 1 0
Reserved				DELTA_OSC
-				0x01
-				RW

5 0	DELTA_OSC	Touch-only RING Oscillator (OSCts) Trimming selection (Determine the F0 frequency with TRIM_OSC) Refer to the description of the TS_CLK_CFG register for the F0 frequency calculation formula. * bit6, bit7 must be 0

18.2.12 TS_TLED: LED stable time register

The TS_TLED is the LED stable Time Register. This is an 8-bit register.

TS_TLED=0x4000_3748

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Reserved	TLED
-	0x30
-	RW

11	TLED	LED stable Time
0		To run the Touch sensing again after LED working, the stable time in the range of 25us to 30us is required. This counter works based on the system clock.

18.2.13 TS_VHS: touch sensor high sense voltage register

TS_VHS=0x4000_374C

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
Reserved	TS_VHS
-	0x280
-	RW

9	TS_VHS	Touch Sensor High Sense Voltage register
0		

Note) When operating in High Sense Mode, total 1024 steps of voltage of <VHS9:0> is generated. The actual use area should only be used for an area larger than VDD/2.

TS_VHS	VHS @ VDD=5.12V	TS_VHS	VHS @ VDD=5.12V
00000000	VREF=0	100000000	VREF=2.56V
00000001	VREF=5mV	100000001	VREF=2.565V
00000010	VREF=10mV	100000010	VREF=2.570V
00000011	VREF=15mV	……	……
……	……	11111100	VREF=5.100V
01111110	VREF=2.550V	11111101	VREF=5.105V
01111111	VREF=2.555V	11111110	VREF=5.110V
		11111111	VREF=5.115V

18.2.14 TS_VREF: touch sensor COMP reference voltage register

TS_VREF=0x4000_3750

<table>
<tr><td colspan="8">31 30 29 28 27 26 25 24</td><td colspan="8">23 22 21 20 19 18 17 16</td><td colspan="8">15 14 13 12 11 10 9 8</td><td colspan="8">7 6 5 4 3 2 1 0</td></tr>
<tr><td colspan="22">Reserved</td><td colspan="10">TS_VREF</td></tr>
<tr><td colspan="22">-</td><td colspan="10">0x210</td></tr>
<tr><td colspan="22">-</td><td colspan="10">RW</td></tr>
</table>

9 0	TD	Touch Sensor COMP Reference voltage register

Note) Comparator reference voltage value varies according to HC(High current option). When operating low current(HC=0), total 1024 steps of voltage is generated. During high current(HC=1) operation, only one bit of TS_VREF[9:0] should be valid.

HC **(Low current** **mode)**	**TS_VREF**	**VREF** **@ VDD=5.12V**	**HC** **(High current** **mode)**	**TS_VREF**	**VREF**
0	0000000000	VREF=0	1	0000000000	Floating
0	0000000001	VREF=5mV	1	0000000001	0.50VDD
0	0000000010	VREF=10mV	1	0000000010	0.52VDD
0	0000000011	VREF=15mV	1	0000000100	0.54VDD
0	…	…	1	0000001000	0.56VDD
0	0111111110	VREF=2.550V	1	0000010000	0.58VDD
0	0111111111	VREF=2.555V	1	0000100000	0.60VDD
0	1000000000	VREF=2.56V	1	0001000000	0.62VDD
0	1000000001	VREF=2.565V	1	0010000000	0.64VDD
0	1000000010	VREF=2.570V	1	0100000000	0.66VDD
0	…	…	1	1000000000	0.68VDD
0	1111111100	VREF=5.100V			
0	1111111101	VREF=5.105V			
0	1111111110	VREF=5.110V			
0	1111111111	VREF=5.115V			

18.2.15 SHLD_CON: touch sensor shield channel control register

SHLD_CON=0x4000_3760

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MESH	MESH_ADD	MODE	RESERVED				SHLD_EN	SHLD_CH23	SHLD_CH22	SHLD_CH21	SHLD_CH20	SHLD_CH19	SHLD_CH18	SHLD_CH17	SHLD_CH16	SHLD_CH15	SHLD_CH14	SHLD_CH13	SHLD_CH12	SHLD_CH11	SHLD_CH10	SHLD_CH09	SHLD_CH08	SHLD_CH07	SHLD_CH06	SHLD_CH05	SHLD_CH04	SHLD_CH03	SHLD_CH02	SHLD_CH01	SHLD_CH00
0	0	0	-				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RW	RW	RW	-				RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

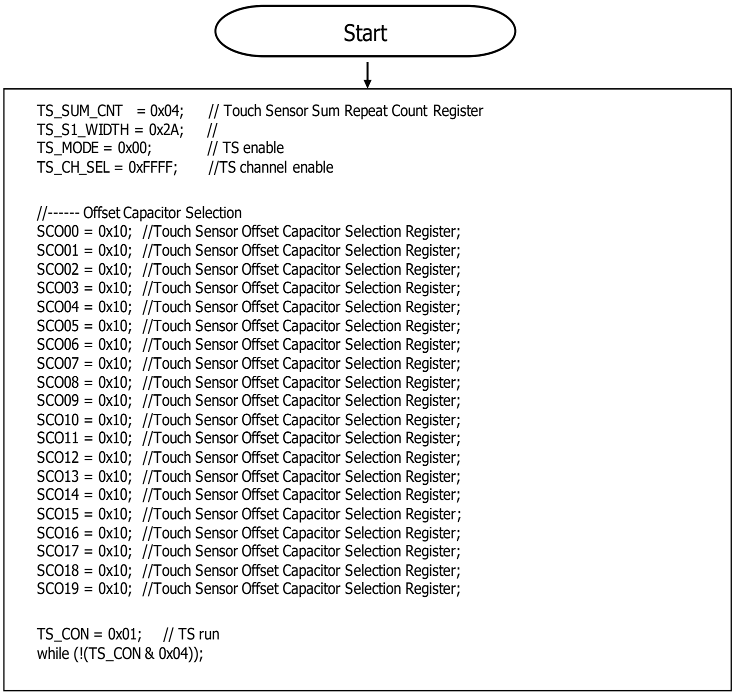
31	MESH	Shield mesh enable bit	
		0	Ch.23 Shield mesh disable
		1	Ch.23 Shield mesh enable
30	MESH_ADD	Additional shield mesh enable bit	
		0	Additional shield mesh disable
		1	Additional shield mesh enable
29	MODE	Shield mode bit	
		0 (Default)	BFAMP Input: CAPN (Low drive: switch)
		1 (Option)	BFAMP Input: TOG_N (Low drive: AMP)
24	SHLD_EN	Shield enable bit	
		0	Shield channel & mesh Disable
		1	Shield channel & mesh Enable
23 0	SHLD_CHx	Shield channel selection bits	
		0	Disable Ch.x as shield channel
		1	Enable Ch.x as shield channel

NOTES :

1. The SHLD_CHx is not available while the SCH is being used. (All channels without sensing can be turned on.)
2. If the MESH and SHLD_CH23 are used simultaneously, the capability for the shielding is enhanced.
3. If the MESH is enabled, the CH23 cannot be used for the Touch sensing.

18.3 Functional description

18.3.1 User programming procedure



```
TS_SUM_CNT   = 0x04;     // Touch Sensor Sum Repeat Count Register
TS_S1_WIDTH = 0x2A;     //
TS_MODE = 0x00;          // TS enable
TS_CH_SEL = 0xFFFF;      //TS channel enable

//------ Offset Capacitor Selection
SCO00 = 0x10;  //Touch Sensor Offset Capacitor Selection Register;
SCO01 = 0x10;  //Touch Sensor Offset Capacitor Selection Register;
SCO02 = 0x10;  //Touch Sensor Offset Capacitor Selection Register;
SCO03 = 0x10;  //Touch Sensor Offset Capacitor Selection Register;
SCO04 = 0x10;  //Touch Sensor Offset Capacitor Selection Register;
SCO05 = 0x10;  //Touch Sensor Offset Capacitor Selection Register;
SCO06 = 0x10;  //Touch Sensor Offset Capacitor Selection Register;
SCO07 = 0x10;  //Touch Sensor Offset Capacitor Selection Register;
SCO08 = 0x10;  //Touch Sensor Offset Capacitor Selection Register;
SCO09 = 0x10;  //Touch Sensor Offset Capacitor Selection Register;
SCO10 = 0x10;  //Touch Sensor Offset Capacitor Selection Register;
SCO11 = 0x10;  //Touch Sensor Offset Capacitor Selection Register;
SCO12 = 0x10;  //Touch Sensor Offset Capacitor Selection Register;
SCO13 = 0x10;  //Touch Sensor Offset Capacitor Selection Register;
SCO14 = 0x10;  //Touch Sensor Offset Capacitor Selection Register;
SCO15 = 0x10;  //Touch Sensor Offset Capacitor Selection Register;
SCO16 = 0x10;  //Touch Sensor Offset Capacitor Selection Register;
SCO17 = 0x10;  //Touch Sensor Offset Capacitor Selection Register;
SCO18 = 0x10;  //Touch Sensor Offset Capacitor Selection Register;
SCO19 = 0x10;  //Touch Sensor Offset Capacitor Selection Register;

TS_CON = 0x01;     // TS run
while (!(TS_CON & 0x04));
```

Figure 110. User Programming Procedure

18.3.2 CAPN port

Connect the negative terminal of the reference capacitor Cs to CAPN port, and the positive terminal of the Cs capacitor to VDD. The Cs capacitors must use 5% precision polyester plug-in capacitors and 10% high precision NPO or X7R chip capacitors. C0G type or Mylar Capacitor is recommended for applications with severe temperature changes.

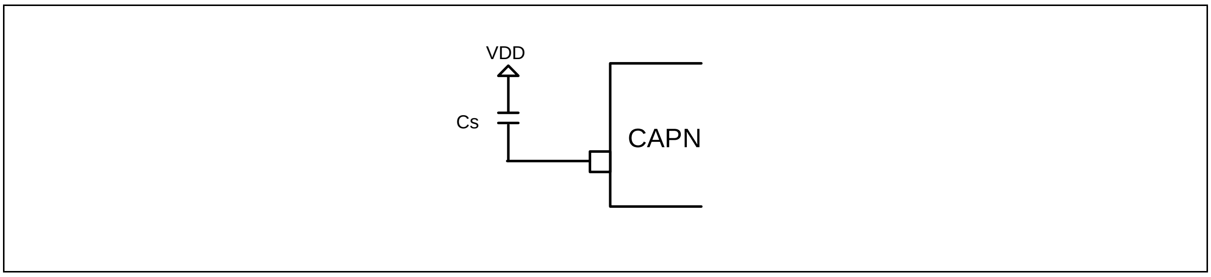


Figure 111. CAPN Pin with Cs Capacitor

18.3.3 TOUCH and LED port control

Before using a port for Touch/LED mode, users must set the Pn_AFSRx register to '0x5' (ALT5 mode).

The COM/SEG drive operates for output in LED mode, only when ALT5 mode is set. Similarly, the TOUCH Sensing operation is valid only when ALT5 mode is set.

By configuring the LED_PORTCTRL and Pn_OUTDR registers, the LED port can operate as a GPIO while LED does not work (while the LEDST = 0).

The TOUCH port, which is an inactive channel port, can also work as a GPIO or Shield while other channels are performing the sensing operation.

The Shield function has higher priority than the GPIO. A port used both for TOUCH and LED operates as Shield for TOUCH. If the Shield function is not used, the port operates as a GPIO for LED. TOUCH's GPIO is ignored.

19 LCD Driver

LCD Driver is controlled by the LCD control register (LCD_CR) and the LCD Driver bias and contrast control register (LCD_BCCR).

The LCD_CR<LCLK> bits determine the frequency of COM signal scanning of each segment output. A RESET clears the LCD control registers LCD_CR and LCD_BCCR values to logic '0'.

The LCD display can continue operating during IDLE and STOP modes.

The clock and duty for LCD Driver are automatically initialized by hardware, whenever the LCD_CR register data value is re-written. Therefore, it is not recommended that users re-write the LCD_CR frequently.

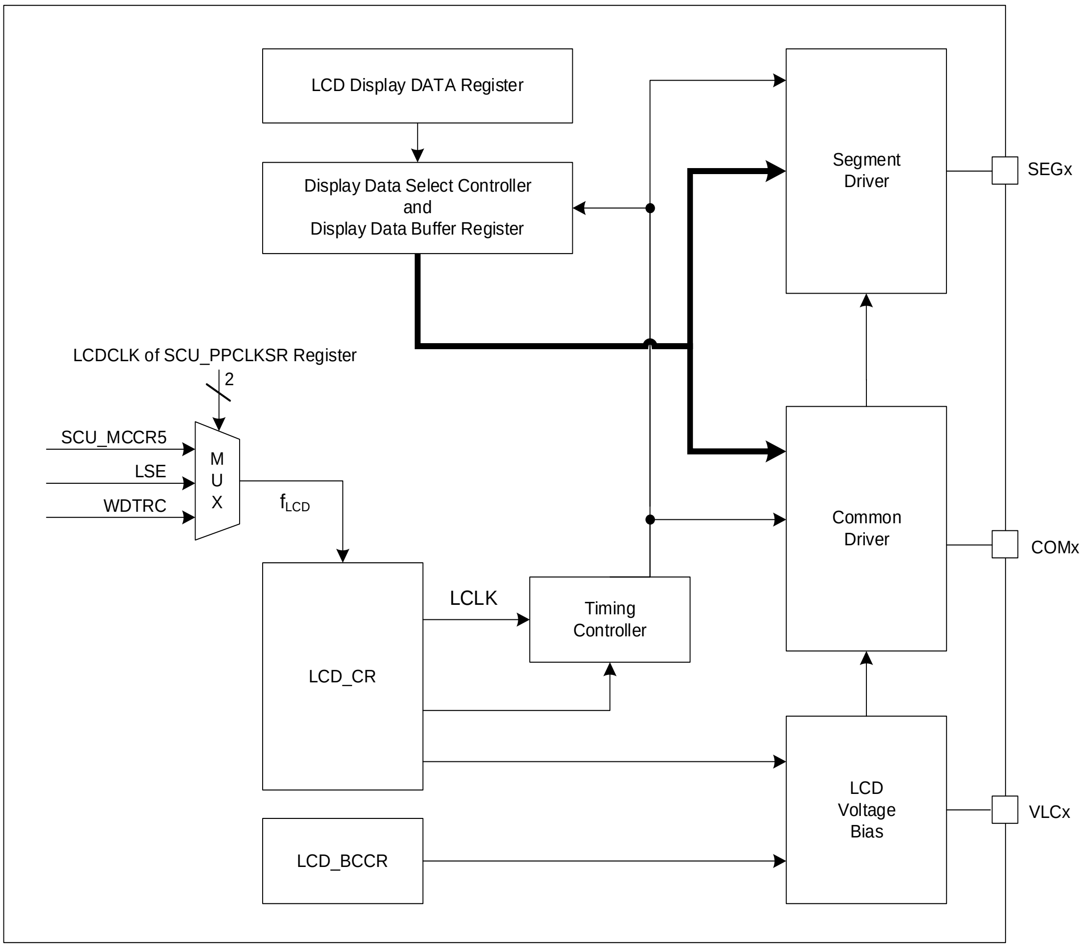
Table 69 introduces pins assigned for LCD Driver.

Table 69. Pin Assignment of LCD Driver: External Signal

Pin name	Type	Description
VLC0 to 3	A	LCD External Bias voltage input
COM0 to 7	O	LCD Common signal outputs
SEG0 to SEG31	O	LCD Segment signal outputs

19.1 LCD driver block diagram

Figure 112 shows a block diagram of LCD Driver.



NOTE: The pull-up resistors for PF0 (SEG26) and PF1 (SEG25) are initially enabled.

Figure 112. LCD Driver Block Diagram

19.2 Registers

Table 70 and Table 71 show base address and register map of the LCD Driver unit.

Table 70. Base Address of LCD Driver

Name	Base address
LCD	0x4000_5000

Table 71. LCD Driver Register Map

Name	Offset	Type	Description	Reset value	Ref.
LCD_CR	0x00	RW	LCD Driver Control Register	0x0000_0000	
LCD_BCCR	0x04	RW	LCD Automatic Bias and Contrast Control Register	0x0000_0000	
LCD_DRn (n=0 to 7)	0x10 to 0x2C	RW	LCD Display Data Registers (0 to 7)	Unknown	

19.2.1 LCD_CR: LCD driver control register

The LCD_CR is the LCD Driver control register. This is a 32-bit register with 32/16/8-bit access.

LCD_CR=0x4000_5000

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6	5 4 3	2 1	0
Reserved	IRSEL	DBS	LCLK	DISP
-	00	000	00	0
-	RW	RW	RW	RW

7 6	IRSEL	Internal LCD Bias Dividing Resistor Selection bits.	
		00	RLCD3: 105/105/80[kΩ] @(1/2)/(1/3)/(1/4) bias.
		01	RLCD1: 10/10/10[kΩ] @(1/2)/(1/3)/(1/4) bias.
		10	RLCD2: 66/66/50[kΩ] @(1/2)/(1/3)/(1/4) bias.
		11	RLCD4: 320/320/240[kΩ] @(1/2)/(1/3)/(1/4) bias.
5 3	DBS	LCD Duty and Bias Selection bits.	
		000	1/8 duty, 1/4 bias.
		001	1/6 duty, 1/4 bias.
		010	1/5 duty, 1/3 bias.
		011	1/4 duty, 1/3 bias.
		100	1/3 duty, 1/3 bias.
		101	1/3 duty, 1/2 bias
		Others	Reserved.
2 1	LCLK	LCD clock divider selection bits. fLCD(LCD clock source) is selected by SCU_PPCLKSR	
		00	fLCD / 256 (128Hz @ fLCD = 32.768kHz)
		01	fLCD / 128 (256Hz @ fLCD = 32.768kHz)
		10	fLCD / 64 (512Hz @ fLCD = 32.768kHz)
		11	fLCD / 32 (1024Hz @ fLCD = 32.768kHz)
0	DISP	LCD Display Control bit.	
		0	Display off.
		1	Normal display on.

19.2.2 LCD_BCCR: LCD automatic bias and contrast control register

The LCD_BCCR is the LCD automatic bias and contrast control register. This is a 32-bit register with 32/16/8-bit access.

LCD_BCCR=0x4000_5004

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13	12	11	10 9 8	7 6	5	4	3 2 1 0
Reserved	LCDABC	Reserved	BMSEL	Reserved	LCTEN	Reserved	VLCD
-	0	-	000	-	0	-	0000
-	RW	-	RW	-	RW	-	RW

12	LCDABC	LCD Automatic Bias Control bit.	
		0	LCD automatic bias is off.
		1	LCD automatic bias is on.
10 8	BMSEL	"Bias Mode A" Time Selection bits. Refer to Figure 119. LCD Automatic Bias Control Timing Diagram.	
		000	"Bias Mode A" for 1-clock of fLCD.
		001	"Bias Mode A" for 2-clock of fLCD.
		010	"Bias Mode A" for 3-clock of fLCD.
		011	"Bias Mode A" for 4-clock of fLCD.
		100	"Bias Mode A" for 5-clock of fLCD.
		101	"Bias Mode A" for 6-clock of fLCD.
		110	"Bias Mode A" for 7-clock of fLCD.
		111	"Bias Mode A" for 8-clock of fLCD.
5	LCTEN	LCD Driver Contrast Control bit.	
		0	Disable LCD driver contrast.
		1	Enable LCD driver contrast.
3 0	VLCD	VLC0 Voltage Control when the contrast is enabled.	
		0000	LVC0 = VDD x 16/31 step
		0001	LVC0 = VDD x 16/30 step
		0010	LVC0 = VDD x 16/29 step
		0011	LVC0 = VDD x 16/28 step
		0100	LVC0 = VDD x 16/27 step
		0101	LVC0 = VDD x 16/26 step
		0110	LVC0 = VDD x 16/25 step
		0111	LVC0 = VDD x 16/24 step
		1000	LVC0 = VDD x 16/23 step
		1001	LVC0 = VDD x 16/22 step
		1010	LVC0 = VDD x 16/21 step
		1011	LVC0 = VDD x 16/20 step
		1100	LVC0 = VDD x 16/19 step
		1101	LVC0 = VDD x 16/18 step
		1110	LVC0 = VDD x 16/17 step
		1111	LVC0 = VDD x 16/16 step

NOTE: The above LCD contrast step is based on 1/3 bias with 66kΩ RLCD and on 1/4 bias with 50kΩ RLCD.

19.2.3 LCD_BSSR: LCD source selection register

The LCD_BSSR is the LCD Driver control register. This is a 32-bit register with 32/16/8-bit access.

LCD_CR=0x4000_5000

31	30	29	15	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				VLE_EN	Reserved	LCDDR	PVLC_OPEN	VLC_PE3	VLC_PE2	VLC_PE1	VLC_PE0	Reserved			
-																				0	-	0	0	0	0	0	0	-			
-																				RW	-	RW	RW	RW	RW	RW	RW	-			

11	VLE_EN	External bias test register.	
		0	Test mode is on and external bias cannot be used
		1	External bias can be used normally with test mode off
9	LCDDR	LCD external bias path enable bit	
		0	Internal LCD driving resistors for bias
		1	External LCD driving resistors for bias
8	PVLC_OPEN	LCD external bias path enable bit	
		0	Disable
		1	enable
7	VLC_PE3	External bias VLC3 enable bit	
		0	Disable VLC3
		1	Enable VLC3
6	VLC_PE2	External bias VLC2 enable bit	
		0	Disable VLC2
		1	Enable VLC2
5	VLC_PE1	External bias VLC1 enable bit	
		0	Disable VLC1
		1	Enable VLC1
4	VLC_PE0	External bias VLC0 enable bit	
		0	Disable VLC0
		1	Enable VLC0

NOTES:

1. LCD_BSSR[3:0] must be fixed to 0.
2. Register settings for the use of external bias are as follows
   - VLE_EN=1
   - LCDDR=1
   - PVLC_OPEN=1
   - VLC_PEx=1

19.2.4 LCD_DRn: LCD display data register x

The LCD_DRn are the LCD display data registers. They are 32-bit registers with 32/16/8-bit access. (n = 0 to 7)

LCD_DRx=0x4000_5010 to 0x4000_502C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
LCDDR(4xn+3)	LCDDR(4xn+2)	LCDDR(4xn+1)	LCDDR(4xn+0)
0x00	0x00	0x00	0x00
RW	RW	RW	RW

31 24	LCDDR(4xn+3)	LCD Display Data bits.
23 16	LCDDR(4xn+2)	LCD Display Data bits.
15 8	LCDDR(4xn+1)	LCD Display Data bits.
7 0	LCDDR(4xn+0)	LCD Display Data bits.

NOTE: The pull-up resistors for PF0 (SEG26) and PF1 (SEG25) are initially enabled.

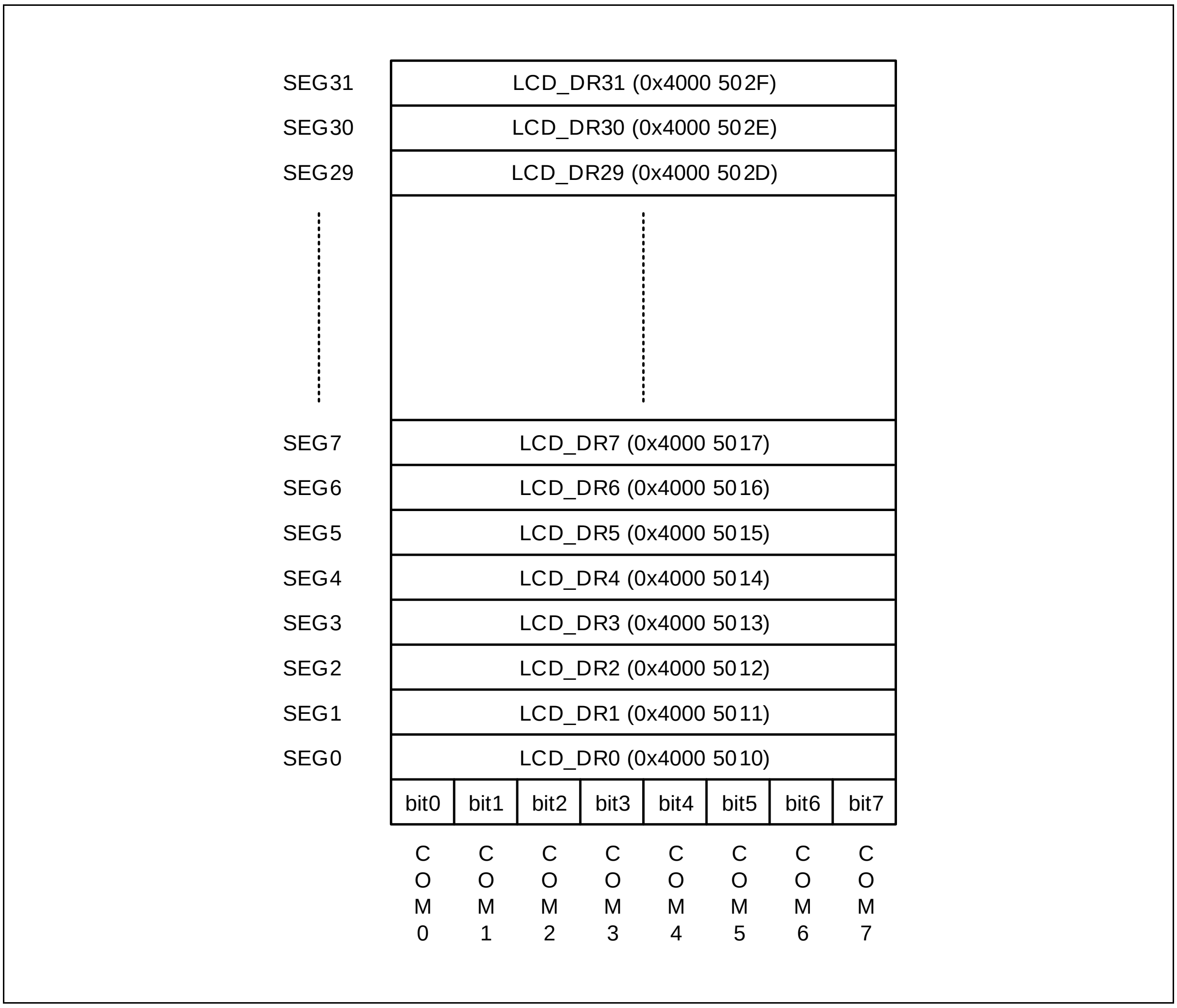
19.3 Functional description

19.3.1 LCD display RAM organization

Display data is stored in the display data area of external data memory.

The display data in the display external data area (address 0x4000_5010 to 0x4000_502F) are read automatically and sent to the LCD driver by the hardware. The LCD driver generates the segment signals and common signals in accordance with the display data and drive method. Therefore, display patterns can be changed only by overwriting the contents of the display external data area with an application.

Figure 113 shows the correspondence between the display external data area and the COM/SEG pins. The LCD turns on when the display data is ‘1’, and turns off when it is ‘0’.



SEG31	LCD_DR31 (0x4000 502F)
SEG30	LCD_DR30 (0x4000 502E)
SEG29	LCD_DR29 (0x4000 502D)
SEG7	LCD_DR7 (0x4000 5017)
SEG6	LCD_DR6 (0x4000 5016)
SEG5	LCD_DR5 (0x4000 5015)
SEG4	LCD_DR4 (0x4000 5014)
SEG3	LCD_DR3 (0x4000 5013)
SEG2	LCD_DR2 (0x4000 5012)
SEG1	LCD_DR1 (0x4000 5011)
SEG0	LCD_DR0 (0x4000 5010)

bit0	bit1	bit2	bit3	bit4	bit5	bit6	bit7
COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7

Figure 113. LCD Display RAM

19.3.2 LCD signal waveform

Figure 114, Figure 115, and Figure 116 show LCD signal waveforms with different duties and biases, respectively.

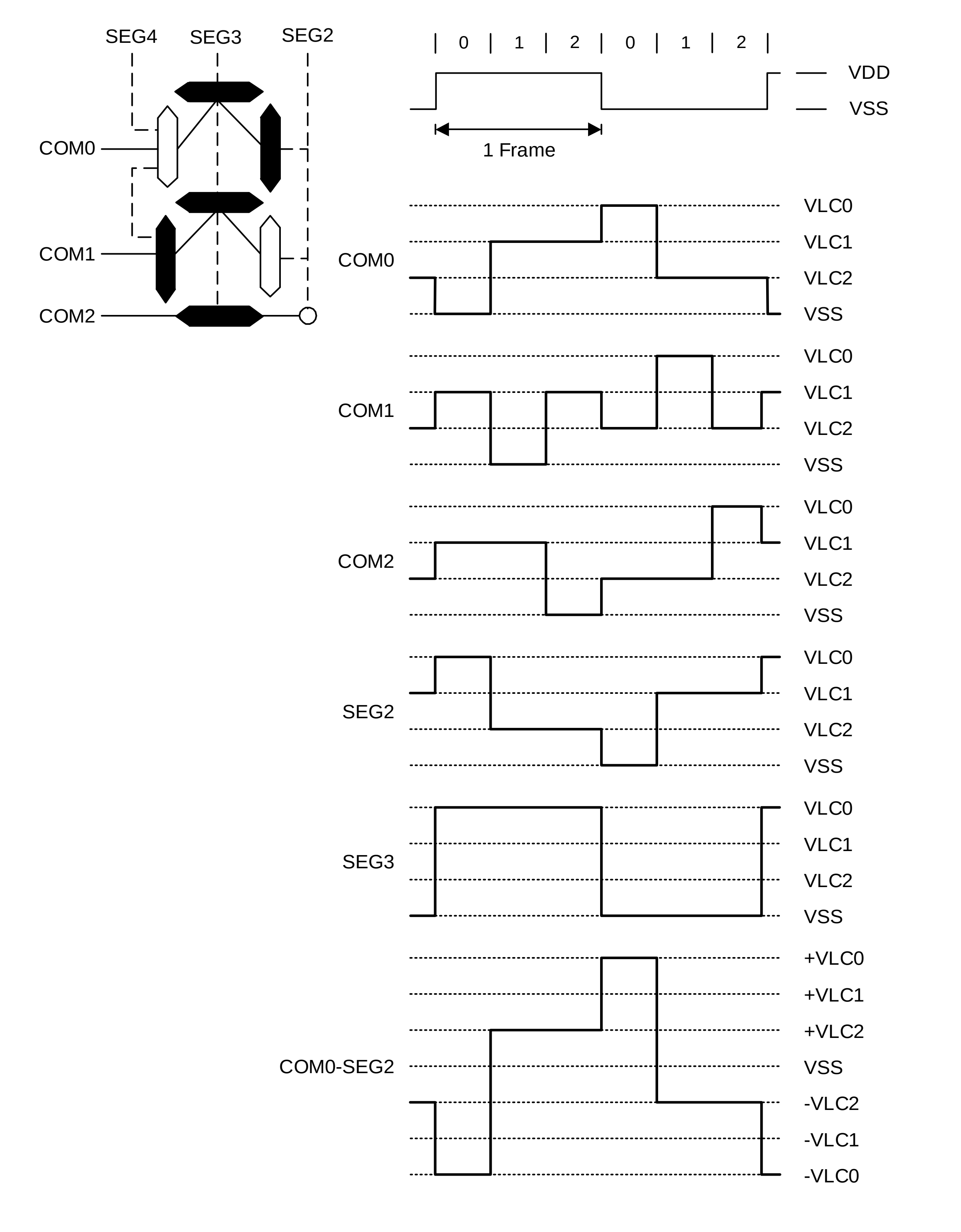


Figure 114. LCD Signal Waveforms (1/3 Duty, 1/3 Bias)

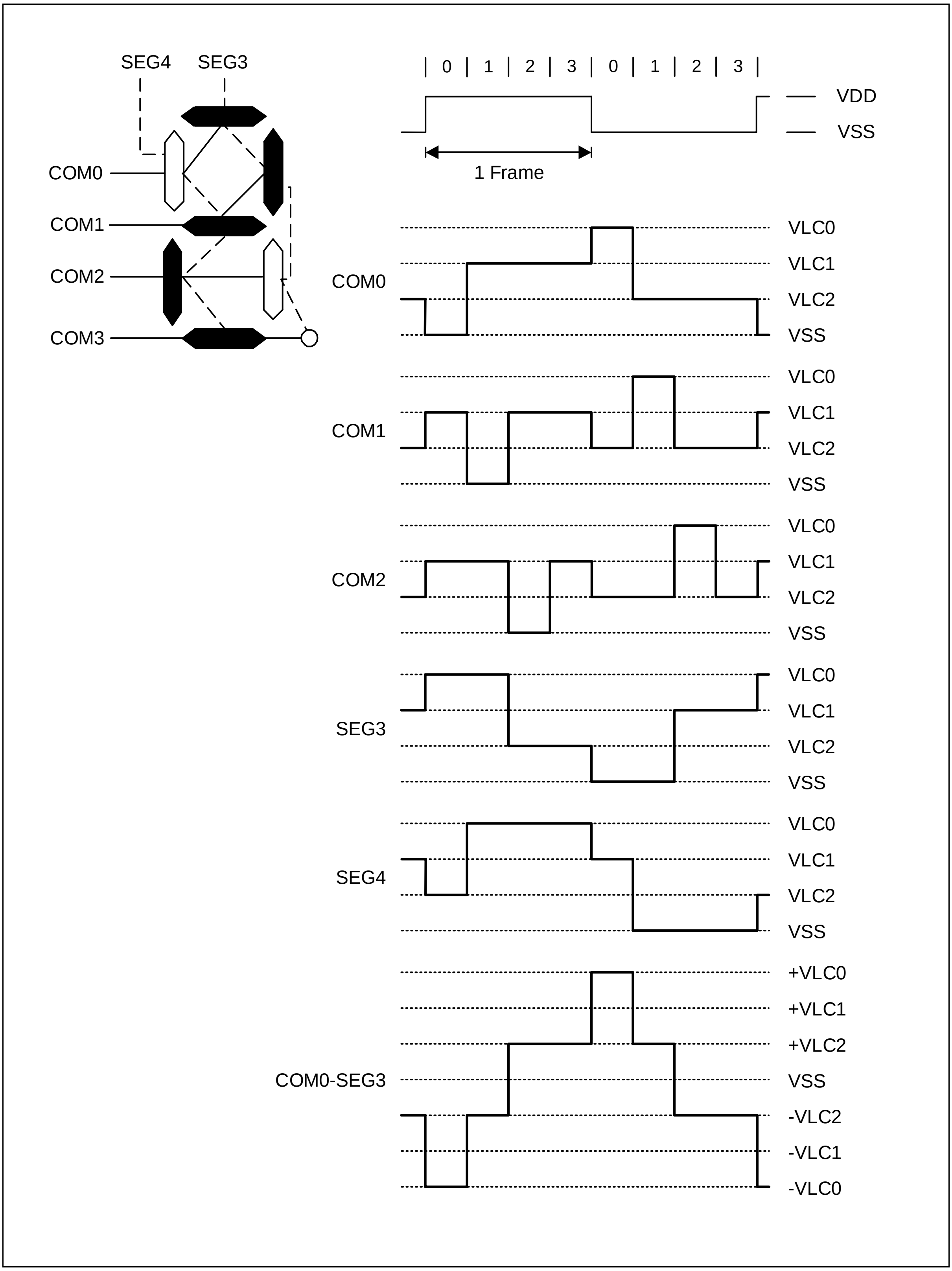


Figure 115. LCD Signal Waveforms (1/4 Duty, 1/3 Bias)

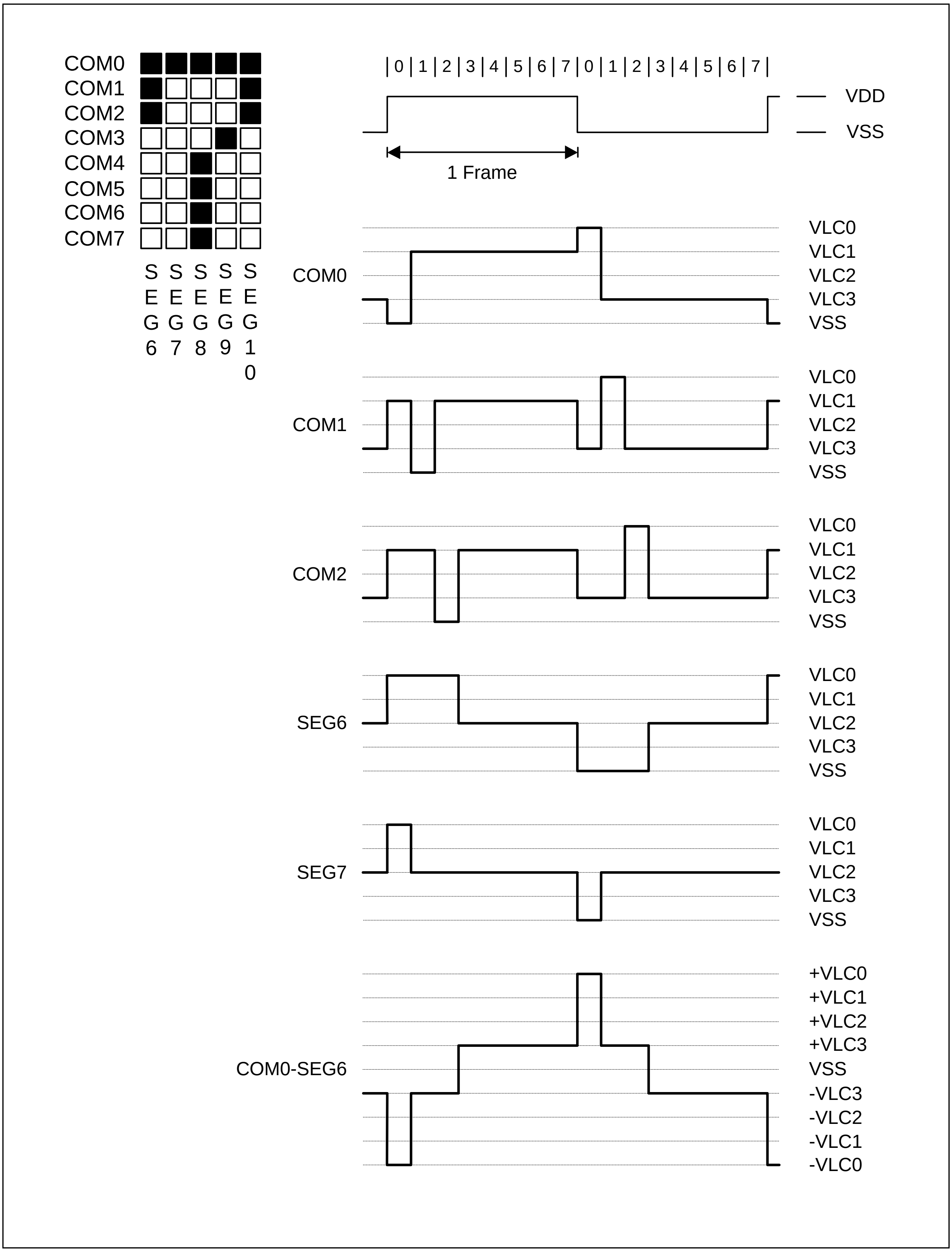
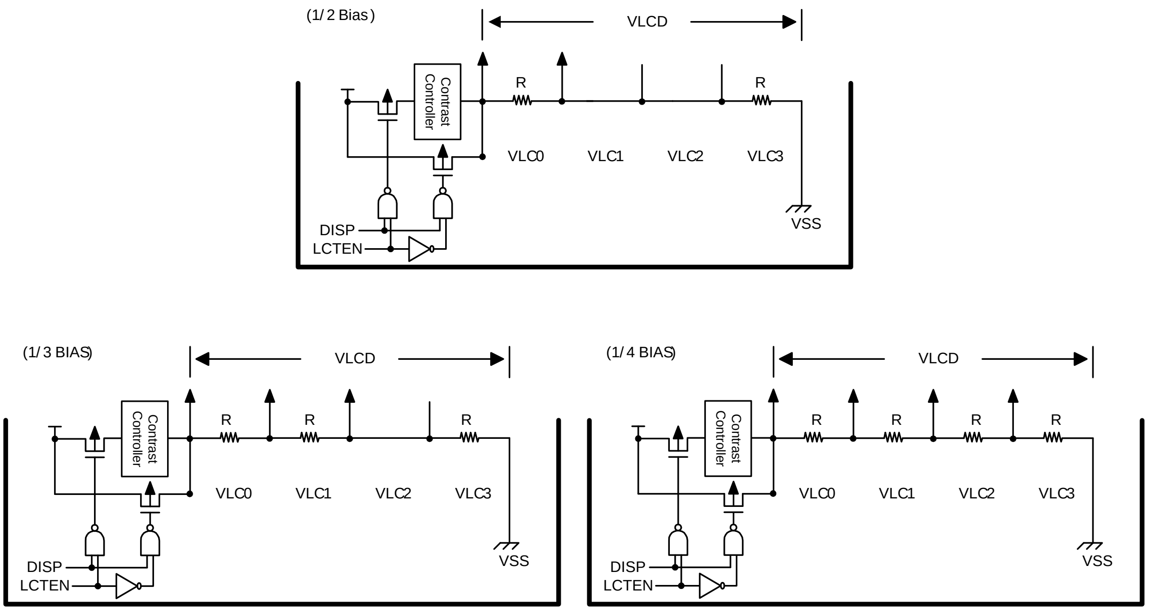


Figure 116. LCD Signal Waveforms (1/8 Duty, 1/4 Bias)

19.3.3 Internal resistor bias connection

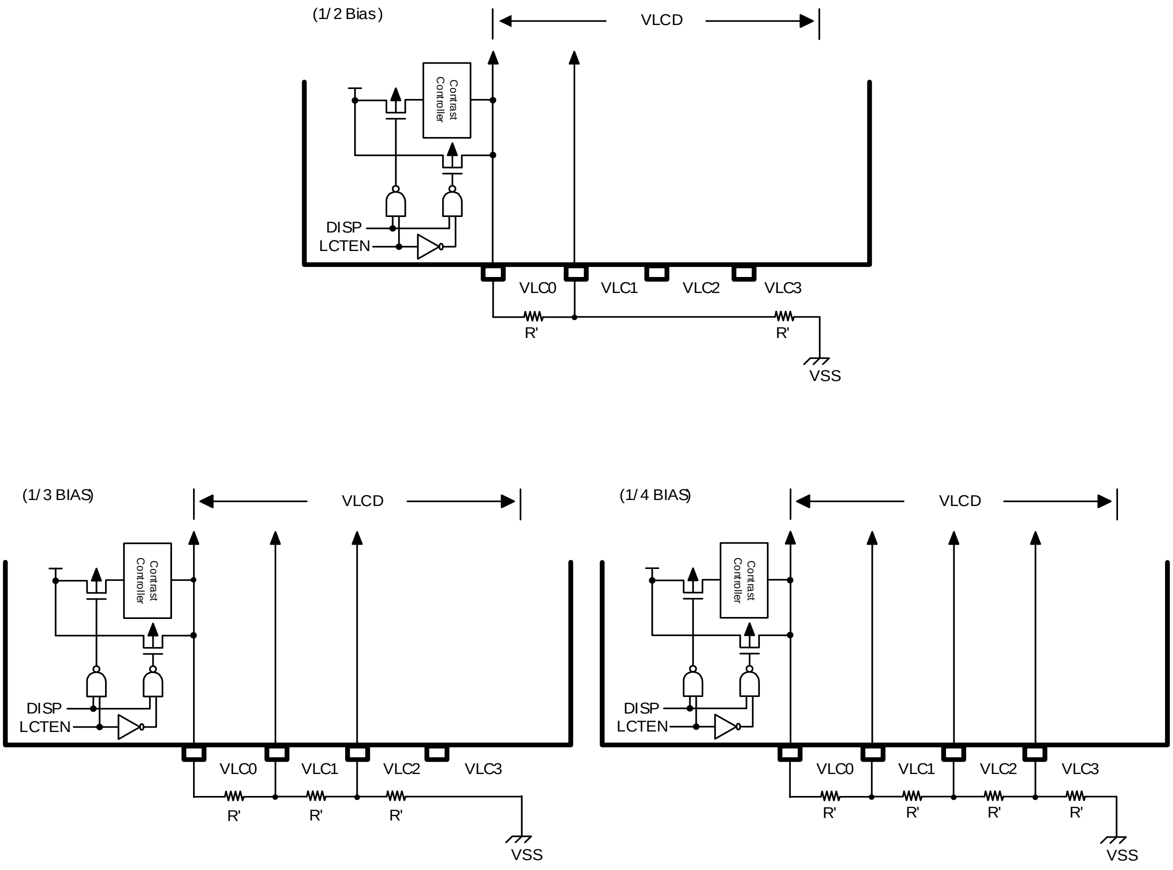


NOTES:

1. When 1/2 bias are selected, the VLC1, VLC2 and VLC3 are internally connected.
2. When 1/3 bias are selected, the VLC2 and VLC3 are internally connected.
3. When the internal resistors are selected, all the PE8/VLC0, PE9/VLC1, PE10/VLC2 and PE11/VLC3 pins can be used for normal I/O.
4. In the LCD resistor bias mode, there is a possibility that the signal of LCD could generate glitch signal at scanning COM port switching. But there is no abnormal display operation due to glitch.

Figure 117. Internal Resistor Bias Connection

19.3.4 External resistor bias connection

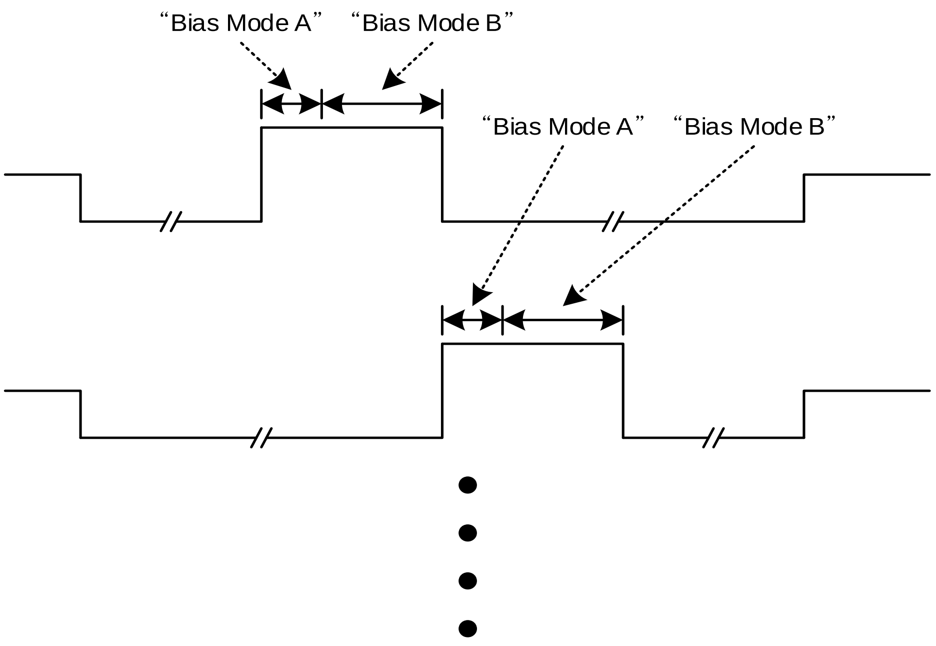


NOTES:

1. When the external resistor bias is selected, the internal resistors for bias are disconnected.
2. When the external resistor bias is selected, the dividing resistors should be connected like the above figure and the needed bias pins should be selected as the LCD bias function pins (VLC0, VLC1, VLC2 and VLC3) by PE_MOD & PE_ASFR2 register.

Figure 118. External Resistor Bias Connection

19.3.5 LCD automatic bias control timing



NOTE: When the LCD automatic bias is on,

- “Bias Mode A”: Always RLCD1 (10kΩ).
- “Bias Mode B”: An LCD bias dividing resistor which is selected by the IRSEL[1:0] bits

Figure 119. LCD Automatic Bias Control Timing Diagram

20 LED Driver

LED Driver has 13 ICOM / 16 ISEG output pins that are shared with Touch sensing pins. By configuring the LED control register 1 (LED_CON1), users can decide whether to share pins with Touch sensing function.

The LED Driver consists of display data RAM memory, and the ICOM and ISEG generator with the following features:

- ICOM0, ICOM1, …, ICOM12 are shared with ISEG0, ISEG1, …, ISEG12. It is selected by configuring the LED_COMER register.
- ISEG13, ISEG14, and ISEG15 are dedicated only for the ISEG function in LED function.
- ICOM and ISEG pins can be used as I/O pins.
- The LED_COMOE and LED_SEGOE registers are used to enable or disable each of ISEG0, ISEG1, …, ISEG15 and ICOM0, ICOM1, …, ICOM12.
- During the power-on reset, the reset pin, BOD reset or watchdog reset, and LED are turned off.
- The fPCLK is the PERI clock.

Table 72 introduces pins assigned for LED Driver.

Table 72. Pin Assignment of LED Driver: External Signal

Pin name	Type	Description
ICOM0 to ICOM12	O	LED Common signal outputs
ISEG0 to ISEG15	O	LED Segment signal outputs

20.1 LED Driver block diagram

Figure 120 shows a block diagram of LED Driver.

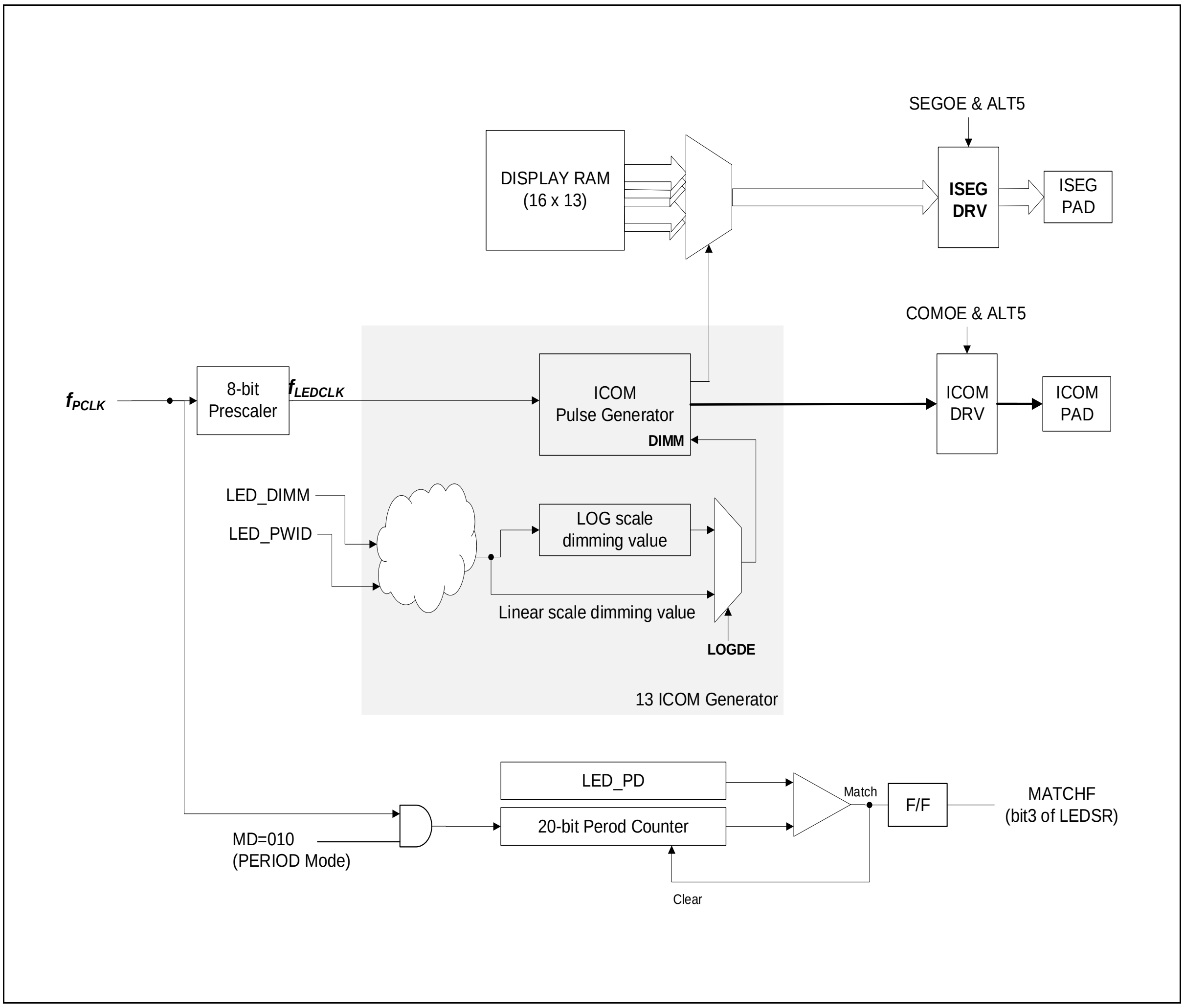


Figure 120. LED Driver Block Diagram

20.2 Registers

Table 73 and Table 74 show base address and register map of the LED Driver unit.

It is strongly recommended that users set the LED_CON1<LEDEN> bit before setting other registers and set the LED_CON1<LEDST> bit at the end of setting other registers.

Table 73. Base Address of LED Driver

Name	Base address
LED	0x4000_6000

Table 74. LED Driver Register Map

Name	Offset	Type	Description	Reset value	Ref.
LED_COMOE	0x00	RW	LED IICOM Output Enable Register	0x0000_0000	
LED_SEGOE	0x04	RW	LED ISEG Output Enable Register	0x0000_0000	
LED_PRESD	0x08	RW	LED Pre-scaler Register	0x0000_0000	
LED_COMER	0x0C	RW	LED ICOM Enable Register	0x0000_0000	
LED_COMPWID	0x10	RW	LED ICOM Pulse Width Control Register	0x0000_0000	
LED_COMDIMM0 to 3	0x14 to 0x20	RW	LED ICOM Dimming Control 0 to 3 Register	0x0000_0000	
LED_PD	0x24	RW	LED Period Data Register	0x0000_0000	
LED_SR	0x28	RW	LED Status Register	0x0000_0001	
LED_CON3	0x2C	RW	LED Control 3 Register	0x0000_0000	
LED_CON2	0x30	RW	LED Control 2 Register	0x0000_0000	
LED_CON1	0x34	RW	LED Control 1 Register	0x0000_0000	
LED_CIOL_TST	0x38	RW	LED CIOL Test Register	0x0000_0000	
LED_DISPRAM0 to 12	0x40 to 0x70	RW	LED Display RAM 0 to 12	0x0000_0000	
LED_CCSTRIM	0x74	RW	Constant Current Level Select Register	0x0000_0001	
LED_LOGDE	0x80	RW	LED Log-scale Dimming Enable Register	0x0000_0000	
LED_COMDRIVE	0x84	RW	LED ICOM Current Drive Enable Register	0x0000_0000	
LED_PORTCTRL	0x88	RW	LED Port Control Register	0x0000_0000	
LED_DLYCNT	0x8C	RW	LED run signal Delay Count Register	0x0000_0000	

20.2.1 LED_COMOE: ICOM output enable register

The LED_COMOE is the ICOM output enable register. This is a 13-bit register with 32/16/8-bit access.

LED_COMOE=0x4000_6000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			ICOMOE12	ICOMOE11	ICOMOE10	ICOMOE9	ICOMOE8	ICOMOE7	ICOMOE6	ICOMOE5	ICOMOE4	ICOMOE3	ICOMOE2	ICOMOE1	ICOMOE0
-																			0	0	0	0	0	0	0	0	0	0	0	0	0
-																			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

12	ICOMOE12	ICOM12 output enable bit	
		0	ICOM12 output disable
		1	ICOM12 output enable
11	ICOMOE11	ICOM11 output enable bit	
		0	ICOM11 output disable
		1	ICOM11 output enable
10	ICOMOE10	ICOM10 output enable bit	
		0	ICOM10 output disable
		1	ICOM10 output enable
9	ICOMOE9	ICOM9 output enable bit	
		0	ICOM9 output disable
		1	ICOM9 output enable
8	ICOMOE8	ICOM8 output enable bit	
		0	ICOM8 output disable
		1	ICOM8 output enable
7	ICOMOE7	ICOM7 output enable bit	
		0	ICOM7 output disable
		1	ICOM7 output enable
6	ICOMOE6	ICOM6 output enable bit	
		0	ICOM6 output disable
		1	ICOM6 output enable
5	ICOMOE5	ICOM5 output enable bit	
		0	ICOM5 output disable
		1	ICOM5 output enable
4	ICOMOE4	ICOM4 output enable bit	
		0	ICOM4 output disable
		1	ICOM4 output enable
3	ICOMOE3	ICOM3 output enable bit	
		0	ICOM3 output disable
		1	ICOM3 output enable
2	ICOMOE2	ICOM2 output enable bit	
		0	ICOM2 output disable
		1	ICOM2 output enable
1	ICOMOE1	ICOM1 output enable bit	
		0	ICOM1 output disable
		1	ICOM1 output enable
0	ICOMOE0	ICOM0 output enable bit	
		0	ICOM0 output disable
		1	ICOM0 output enable

20.2.2 LED_SEGOE: ISEG output enable register

The LED_SEGOE is the ISEG output enable register. This is a 16-bit register with 32/16/8-bit access.

LED_SEGOE=0x4000_6004

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		ISEGOE15	ISEGOE14	ISEGOE13	ISEGOE12	ISEGOE11	ISEGOE10	ISEGOE9	ISEGOE8	ISEGOE7	ISEGOE6	ISEGOE5	ISEGOE4	ISEGOE3	ISEGOE2	ISEGOE1	ISEGOE0
-		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

15	ISEGOE15	ISEG15 output enable bit	
		0	ISEG15 output disable
		1	ISEG15 output enable
14	ISEGOE14	ISEG14 output enable bit	
		0	ISEG14 output disable
		1	ISEG14 output enable
13	ISEGOE13	ISEG13 output enable bit	
		0	ISEG13 output disable
		1	ISEG13 output enable
12	ISEGOE12	ISEG12 output enable bit	
		0	ISEG12 output disable
		1	ISEG12 output enable
11	ISEGOE11	ISEG11 output enable bit	
		0	ISEG11 output disable
		1	ISEG11 output enable
10	ISEGOE10	ISEG10 output enable bit	
		0	ISEG10 output disable
		1	ISEG10 output enable
9	ISEGOE9	ISEG9 output enable bit	
		0	ISEG9 output disable
		1	ISEG9 output enable
8	ISEGOE8	ISEG8 output enable bit	
		0	ISEG8 output disable
		1	ISEG8 output enable
7	ISEGOE7	ISEG7 output enable bit	
		0	ISEG7 output disable
		1	ISEG7 output enable
6	ISEGOE6	ISEG6 output enable bit	
		0	ISEG6 output disable
		1	ISEG6 output enable
5	ISEGOE5	ISEG5 output enable bit	
		0	ISEG5 output disable
		1	ISEG5 output enable
4	ISEGOE4	ISEG4 output enable bit	
		0	ISEG4 output disable
		1	ISEG4 output enable
3	ISEGOE3	ISEG3 output enable bit	
		0	ISEG3 output disable
		1	ISEG3 output enable
2	ISEGOE2	ISEG2 output enable bit	
		0	ISEG2 output disable
		1	ISEG2 output enable
1	ISEGOE1	ISEG1 output enable bit	
		0	ISEG1 output disable
		1	ISEG1 output enable
0	ISEGOE0	ISEG0 output enable bit	
		0	ISEG0 output disable
		1	ISEG0 output enable

20.2.3 LED_PRESD: LED prescaler data register

The LED_PRESD is the LED prescaler data register. This is an 8-bit register with 32/16/8-bit access.

LED_PRESD =0x4000_6008

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED			PRESD
-			0000_0000
-			RW

7 0	PRESD	LED Pre-scale CLK Control bits fLEDCLK = fPCLK / (PRESD + 1)

NOTE: The PRESD value must be greater than '1'.

20.2.4 LED_COMER: ICOM enable register

The LED_COMER is the ICOM enable register. This is a 13-bit register with 32/16/8-bit access.

LED_COMER=0x4000_600C

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	ICOM12	ICOM11	ICOM10	ICOM9	ICOM8	ICOM7	ICOM6	ICOM5	ICOM4	ICOM3	ICOM2	ICOM1	ICOM0
-	0	0	0	0	0	0	0	0	0	0	0	0	0
-	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

12	ICOMER12	ICOM12 / ISEG12 operation selection bit	
		0	ISEG12 only operation
		1	ISEG12 / ICOM12 combined operation
11	ICOMER11	ICOM11 / ISEG11 operation selection bit	
		0	ISEG11 only operation
		1	ISEG11 / ICOM11 combined operation
10	ICOMER10	ICOM10 / ISEG10 operation selection bit	
		0	ISEG10 only operation
		1	ISEG10 / ICOM10 combined operation
9	ICOMER9	ICOM9 / ISEG9 operation selection bit	
		0	ISEG9 only operation
		1	ISEG9/ ICOM9 combined operation
8	ICOMER8	ICOM8 / ISEG8 operation selection bit	
		0	ISEG8 only operation
		1	ISEG8 / ICOM8 combined operation
7	ICOMER7	ICOM7 / ISEG7 operation selection bit	
		0	ISEG7 only operation
		1	ISEG7 / ICOM7 combined operation
6	ICOMER6	ICOM6 / ISEG6 operation selection bit	
		0	ISEG6 only operation
		1	ISEG6 / ICOM6 combined operation
5	ICOMER5	ICOM5 / ISEG5 operation selection bit	
		0	ISEG5 only operation
		1	ISEG5 / ICOM5 combined operation
4	ICOMER4	ICOM4 / ISEG4 operation selection bit	
		0	ISEG4 only operation
		1	ISEG4 / ICOM4 combined operation
3	ICOMER3	ICOM3 / ISEG3 operation selection bit	
		0	ISEG3 only operation
		1	ISEG3 / ICOM3 combined operation
2	ICOMER2	ICOM2 / ISEG2 operation selection bit	
		0	ISEG2 only operation
		1	ISEG2 / ICOM2 combined operation
1	ICOMER1	ICOM1 / ISEG1 operation selection bit	
		0	ISEG1 only operation
		1	ISEG1 / ICOM1 combined operation
0	ICOMER0	ICOM0 / ISEG0 operation selection bit	
		0	ISEG0 only operation
		1	ISEG0 / ICOM0 combined operation

NOTES:

1. If ICOMERx (x = 0, 1, …, 12) is set to 1, both ISEGx and ICOMx is outputted.
2. If not, only ISEGx is outputted. In this case, LED ON time is determined by the number of enable ICOM (LED ON time = ICOM width * # of Enabled ICOM)
3. Refer to Table 75 LED Display RAM.
4. ICOM output has a higher priority than ISEG output. Therefore, when ICOM is outputted, ISEG output is ignored regardless of display RAM setting.

20.2.5 LED_COMPWID: ICOM pulse width control register

The LED_COMPWID is the ICOM pulse width control register. This is an 8-bit register with 32/16/8-bit access.

LED_COMPWID=0x4000_6010

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved			ICOMPWID
-			0000_0000
-			RW

7	ICOMPWID	ICOM Pulse Width Control bits
0		ICOM Width= (COMPWID + 1) / fLEDCLK

20.2.6 LED_DIMM0: ICOM dimming control register0

The LED_DIMM0 is the DIMM0 dimming control register. This is a 32-bit register with 32/16/8-bit access.

LED_DIMM0=0x4000_6014

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
ICOM3_DIMM	ICOM2_DIMM	ICOM1_DIMM	ICOM0_DIMM
0000_0000	0000_0000	0000_0000	0000_0000
RW	RW	RW	RW

31 24	ICOM3_DIMM	ICOM3 Dimming Control bits	
		00 to FF	Dimmed ICOM Width = ICOM Width – *Overlaptime – (ICOM3_DIMM / fLEDCLK)
23 16	ICOM2_DIMM	ICOM2 Dimming Control bits	
		00 to FF	Dimmed ICOM Width = ICOM Width – *Overlaptime – (ICOM2_DIMM / fLEDCLK)
15 8	ICOM1_DIMM	ICOM1 Dimming Control bits	
		00 to FF	Dimmed ICOM Width = ICOM Width – *Overlaptime – (ICOM1_DIMM / fLEDCLK)
7 0	ICOM0_DIMM	ICOM0 Dimming Control bits	
		00 to FF	Dimmed ICOM Width = ICOM Width – *Overlaptime – (ICOM0_DIMM / fLEDCLK)

NOTES:

1. All ICOMDIMM should be less than (ICOM Width – Overlaptime). If not, ICOM is not displayed!!!
2. The overlap time can be set in the LED_CON2[2:0].

20.2.7 LED_DIMM1: ICOM dimming control register1

The LED_DIMM1 is the DIMM1 dimming control register. This is a 32-bit register with 32/16/8-bit access.

LED_DIMM1=0x4000_6018

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
ICOMDIMM7	ICOMDIMM6	ICOMDIMM5	ICOMDIMM4
0000_0000	0000_0000	0000_0000	0000_0000
RW	RW	RW	RW

31 24	ICOMDIMM7	ICOM7 Dimming Control bits	
		00 to FF	Dimmed ICOM Width = ICOM Width – *Overlaptime – (ICOM7_DIMM / fLEDCLK)
23 16	ICOMDIMM6	COM6 Dimming Control bits	
		00 to FF	Dimmed ICOM Width = ICOM Width – *Overlaptime – (ICOM6_DIMM / fLEDCLK)
15 8	ICOMDIMM5	ICOM5 Dimming Control bits	
		00 to FF	Dimmed ICOM Width = ICOM Width – *Overlaptime – (ICOM5_DIMM / fLEDCLK)
7 0	ICOMDIMM4	COM4 Dimming Control bits	
		00 to FF	Dimmed ICOM Width = ICOM Width – *Overlaptime – (ICOM4_DIMM / fLEDCLK)

NOTES:

1. All ICOMDIMM should be less than (ICOM Width – Overlaptime). If not, COM is not displayed!!!
2. The overlap time can be set in the LED_CON2[2:0].

20.2.8 LED_DIMM2: ICOM dimming control register2

The LED_DIMM2 is the DIMM2 dimming control register. This is a 32-bit register with 32/16/8-bit access.

LED_DIMM2=0x4000_601C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
ICOMDIMM11	ICOMDIMM10	ICOMDIMM9	ICOMDIMM8
0000_0000	0000_0000	0000_0000	0000_0000
RW	RW	RW	RW

31 24	ICOMDIMM11	ICOM11 Dimming Control bits	
		00 to FF	Dimmed ICOM Width = ICOM Width – *Overlaptime – (ICOM11_DIMM / fLEDCLK)
23 16	ICOMDIMM10	COM10 Dimming Control bits	
		00 to FF	Dimmed ICOM Width = ICOM Width – *Overlaptime – (ICOM10_DIMM / fLEDCLK)
15 8	ICOMDIMM9	COM9 Dimming Control bits	
		00 to FF	Dimmed ICOM Width = ICOM Width – *Overlaptime – (ICOM9_DIMM / fLEDCLK)
7 0	ICOMDIMM8	COM8 Dimming Control bits	
		00 to FF	Dimmed ICOM Width = ICOM Width – *Overlaptime – (ICOM8_DIMM / fLEDCLK)

NOTES:

1. All ICOMDIMM should be less than (ICOM Width – Overlaptime). If not, ICOM is not displayed!!!
2. The overlap time can be set in the LED_CON2[2:0].

20.2.9 LED_DIMM3: ICOM dimming control register3

The LED_DIMM3 is the DIMM3 dimming control register. This is a 32-bit register with 32/16/8-bit access.

LED_DIMM3=0x4000_6020

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="24">RESERVED</td><td colspan="8">ICOMDIMM12</td></tr>
<tr><td colspan="24">-</td><td colspan="8">0000_0000</td></tr>
<tr><td colspan="24">-</td><td colspan="8">RW</td></tr>
</table>

7	ICOMDIMM12	ICOM12 Dimming Control bits	
0		00 to FF	Dimmed ICOM Width = ICOM Width – *Overlaptime – (ICOM12_DIMM / fLEDCLK)

NOTES:

1. All ICOMDIMM should be less than (ICOM Width – Overlaptime). If not, ICOM is not displayed!!!
2. The overlap time can be set in the LED_CON2[2:0].

20.2.10 LED_PD: LED period data register

The LED_PD is the LED period data register. This is a 20-bit register.

LED_STPD=0x4000_6024

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												LEDPD																			
-												0x00000																			
-												RW																			

19 0	LEDPD	LED Period Data Register (LED period time) This register operates only in LED Period Mode.

NOTES:

1. LED Period = (LEDPD + 1) / fPCLK
2. LED Operation time is determined by the ICOM width and COMER value.
3. The COM width must not be set to longer than the PD register value.

20.2.11 LED_SR: LED status register

The LED_SR is the LED status register. This is a 4-bit register with 32/16/8-bit access.

LED_SR=0x4000_6028

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="28">Reserved</td><td>MATCHF</td><td>LED_INT</td><td>LED_INTE</td><td>LED_ENDF</td></tr>
<tr><td colspan="28">-</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td colspan="28">-</td><td>RW</td><td>RW</td><td>RW</td><td>RW</td></tr>
</table>

3	MATCHF	Flag to occur when LEDPD reg match with counter	
		0	Not Matched
		1	Matched
2	LED_INT	LED Interrupt Flag (in LED_INTE=1)	
		0	LED Interrupt not Generated
		1	LED Interrupt Generated
1	LED_INTE	LED Interrupt Enable	
		0	Disable
		1	Enable
0	LED_ENDF	LED Operation End Flag	
		1	Under LED no Operation
		0	Under LED Operation

NOTES:

1. ‘0’ is written to the MATCHF after matching, or the bit is cleared when the LED operation is ending.
2. The LED_INT bit is not cleared unless ‘0’ is written after the interrupt occurs.
3. Under the following conditions, the LED_ENDF bit is set to ‘1’.
   — After the reset release
   — When the LED_ENDF bit is written with ‘1’
   — When LED operation is terminated since LED starts
   — When ‘0’ is written to the LED_CON1<LEDEN> bit or LED_CON1<LEDST> bit
4. Under the following conditions, the LED_ENDF bit is set to ‘0’.
   — When ‘0’ is written to the LED_ENDF bit
   — When LED is operating since LED starts

20.2.12 LED_CON3: LED control register3

The LED_CON3 is the LED control register3. This is an 8-bit register with 32/16/8-bit access.

LED_CON3=0x4000_602C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
RESERVED			SET TIME 3	SET TIME 2	SET TIME 1	SET TIME 0	CLR TIME 3	CLR TIME 2	CLR TIME 1	CLR TIME 0
-			0	0	0	0	0	0	0	0
-			RW	RW	RW	RW	RW	RW	RW	RW

7 4	SET TIME	ISEG-GND function start timing control bits	
		These function bits are valid only when SRTEN(LED_CON2[3]) is “1” When, fPCLK = 16MHz	
		0000	1µs
		0001	2µs
		0010	4µs
		0011	6µs
		0100	8µs
		0101	10µs
		0110	12µs
		0111	14µs
		1000	16µs
		1001	18µs
		1010	20µs
		1011	22µs
		1100	24µs
		1101	26µs
		1110	28µs
		1111	32µs
3 0	CLR TIME	ISEG-GND function end timing control bits	
		These function bits are valid only when SRTEN(LED_CON2[3]) is “1” When, fPCLK = 16MHz	
		0000	Overlap time – 1µs
		0001	Overlap time – 2µs
		0010	Overlap time – 4µs
		0011	Overlap time – 6µs
		0100	Overlap time – 8µs
		0101	Overlap time – 10µs
		0110	Overlap time – 12µs
		0111	Overlap time – 14µs
		1000	Overlap time – 16µs
		1001	Overlap time – 18µs
		1010	Overlap time – 20µs
		1011	Overlap time – 22µs
		1100	Overlap time – 24µs
		1101	Overlap time – 26µs
		1110	Overlap time – 28µs
		1111	Overlap time – 32µs

NOTE: ISEG GND time must be less than Overlap time. If ISEG GND time exceeding, the Overlap time has no effect.

20.2.13 LED_CON2: LED control register2

The LED_CON2 is the LED control register2. This is a 6-bit register with 32/16/8-bit access.

LED_CON2=0x4000_6030

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5	4	3	2 1 0
Reserved				SRTEN	OVERLAP	OVERTS
-				0	0	0
-				RW	RW	RW

4	SRTEN	ISEG-GND function selection	
		0	ISEG-GND function disable
		1	ISEG-GND function enable
3	OVERLAP	Overlap time source selection	
		0	Overlap time is determined by OVERTS
		1	Overlap time = 2/fPCLK
2 0	OVERTS	Overlap time selection. These bits are valid only when OVERLAP is LOW. When fPCLK = 16MHz,	
		000	64µs
		001	32µs
		010	24µs
		011	21µs
		100	12µs
		101	9µs
		110	6µs
		111	3µs
NOTE: The Overlap time is recommended to be within the range of 5us to 60us.			

20.2.14 LED_CON1: LED control register1

The LED_CON1 is the LED control register1. This is a 4-bit register with 32/16/8-bit access.

LED_CON1=0x4000_6034

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="27">RESERVED</td><td colspan="3">MD</td><td>LEDEN</td><td>LEDST</td></tr>
<tr><td colspan="27">-</td><td colspan="3">0</td><td>0</td><td></td></tr>
<tr><td colspan="27">-</td><td colspan="3">RW</td><td>RW</td><td>RW</td></tr>
</table>

4 2	MD[2:0]	Mode Select	
		000	LED Auto Mode
		001	Reserved
		010	LED Period Mode(since LED Start)
		011	Reserved
		1XX	LED Alone Mode
1	LEDEN	LED Enable	
		0	LED Disable
		1	LED Enable
0	LEDST	LED START, STOP Operation	
		0	Stop LED Operation
		1	Start LED Operation

NOTES:

1. LED operation is possible only after the LED_CON1<LEDEN> bit is set to '1'.
2. Under the following conditions, the LEDST bit is set to '1'.
   — When '1' is written to the LED_CON1<LEDST> bit
   — When the LED_PD register is matched with the counter value in LED Period Mode
3. Under the following conditions, the LEDST bit is cleared to '0'.
   — When '0' is written to the LEDEN bit
   — When '0' is written to the LEDST bit
   — When LED operation is terminated
4. MD is changed to '00' only when '0' is written to the LEDEN. Otherwise, MD is holding previously written value.

20.2.15 LED_DISPRAMx: display RAMx

The LED_DISPRAMx are the display RAM registers.

DISPRAMx=0x4000_6040 – 0x4000_6070

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved		DISPRAM	
-		0x0000_0000	
-		RW	

15 0	DISPRAM	Display RAM Register	
		0	LED turns off
		1	LED turns on

NOTE: For more detail information, Refer to 20.3.1 LED Display RAM Organization section.

20.2.16 LED_LOGDE: LED log-scale dimming enable register

The LED_LOGDE is the LED log-scale dimming enable register with 32/16/8-bit access.

LED_LOGDE=0x4000_6080

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			LOGD EN 12	LOGD EN 11	LOGD EN 10	LOGD EN 9	LOGD EN 8	LOGD EN 7	LOGD EN 6	LOGD EN 5	LOGD EN 4	LOGD EN 3	LOGD EN 2	LOGD EN 1	LOGD EN 0
-																			0	0	0	0	0	0	0	0	0	0	0	0	0
-																			R W	R W	R W	R W	R W	R W	R W	R W	R W	R W	R W	R W	R W

12	LOGD EN 12	ICOM12 Log-scale dimming enable bit	
		0	ICOM12 Log-scale dimming disable
		1	ICOM12 Log-scale dimming enable
11	LOGD EN 11	ICOM11 Log-scale dimming enable bit	
		0	ICOM11 Log-scale dimming disable
		1	ICOM11 Log-scale dimming enable
10	LOGD EN 10	ICOM10 Log-scale dimming enable bit	
		0	ICOM10 Log-scale dimming disable
		1	ICOM10 Log-scale dimming enable
9	LOGD EN 9	ICOM9 Log-scale dimming enable bit	
		0	ICOM9 Log-scale dimming disable
		1	ICOM9 Log-scale dimming enable
8	LOGD EN 8	ICOM8 Log-scale dimming enable bit	
		0	ICOM8 Log-scale dimming disable
		1	ICOM8 Log-scale dimming enable
7	LOGD EN 7	ICOM7 Log-scale dimming enable bit	
		0	ICOM7 Log-scale dimming disable
		1	ICOM7 Log-scale dimming enable
6	LOGD EN 6	ICOM6 Log-scale dimming enable bit	
		0	ICOM6 Log-scale dimming disable
		1	ICOM6 Log-scale dimming enable
5	LOGD EN 5	ICOM5 Log-scale dimming enable bit	
		0	ICOM5 Log-scale dimming disable
		1	ICOM5 Log-scale dimming enable
4	LOGD EN 4	ICOM4 Log-scale dimming enable bit	
		0	ICOM4 Log-scale dimming disable
		1	ICOM4 Log-scale dimming enable
3	LOGD EN 3	ICOM3 Log-scale dimming enable bit	
		0	ICOM3 Log-scale dimming disable
		1	ICOM3 Log-scale dimming enable
2	LOGD EN 2	ICOM2 Log-scale dimming enable bit	
		0	ICOM2 Log-scale dimming disable
		1	ICOM2 Log-scale dimming enable
1	LOGD EN 1	ICOM1 Log-scale dimming enable bit	
		0	ICOM1 Log-scale dimming disable
		1	ICOM1 Log-scale dimming enable
0	LOGD EN 0	ICOM0 Log-scale dimming enable bit	
		0	ICOM0 Log-scale dimming disable
		1	ICOM0 Log-scale dimming enable

20.2.17 LED_CCSTRIM: LED CCS trim control register

The LED_CCSTRIM is the register for ccs trim control.

LED_CCSTRIM=0x4000_6074

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="30">RESERVED</td><td colspan="2">CCSTRIM</td></tr>
<tr><td colspan="30">-</td><td colspan="2">01</td></tr>
<tr><td colspan="30">-</td><td colspan="2">RW</td></tr>
</table>

1 0	CCSTRIM	CCSTRIM Control bits	
		00	IREF 338µA
		01	(Default) IREF 579µA
		10	IREF 1094µA
		11	IREF 1413µA

NOTE: IREF value is referenced from M13EU5CCS_V00.

20.2.18 LED_PORTCTRL: LED port control register

The LED_PORTCTRL is the LED port control register with 32/16/8-bit access.

PORTCTRL = 0x4000_6088

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PORT15 DIR	PORT14 DIR	PORT13 DIR	PORT12 DIR	PORT11 DIR	PORT10 DIR	PORT9 DIR	PORT8 DIR	PORT7 DIR	PORT6 DIR	PORT5 DIR	PORT4 DIR	PORT3 DIR	PORT2 DIR	PORT1 DIR	PORT0 DIR
-		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

PORTx DIR	Selects the PORT status after LED operation (LEDST = low).	
	0	Floating
	1	Output

NOTES:

1. If the LED_DLYCNT value is not '0', the PORTCTRL value is applied after the delay time calculated using the LED_CLYCNT register, not immediately after the LED operation is terminated.
2. Port Output Data complies with the settings of the Pn_ODR.
   - — PORT0 to PORT12: ISEG/ICOM Port
   - — PORT13 to PORT15: ISEG Port
3. When both ISEG and Touch are used on a Port, the Port must be set to Output High, not Floating, to enhances Touch SNR. If the Port is set to Output Low, Ground Path is formed and Touch operation fails.

20.2.19 LED_DLYCNT: LED run signal delay count register

The LED_DLYCNT is the LED run signal delay count register with 32/16/8-bit access.

DLYCNT = 0x4000_608C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED			DLYCNT
-			0
-			RW

7 0	DLYCNT	This value determines the delay time after the LEDST operation (LEDST = 0) until the LED_PORTCTRL value is applied.	
		0	Disable
		else	Delay time = tPCLK * DLYCNT + tPCLK

20.3 Functional description

20.3.1 LED display RAM organization

Display data is stored in the display data area of the external data memory.

The display data which is stored in the display external data area (address 0x4000_6040 - 0x4000_6070) are read automatically and sent to the LED Driver by the hardware. The LED Driver generates the segment signals and com signals in accordance with the display data and drive method. Therefore, display patterns can be changed by only overwriting the contents of the display external data area with an application.

Figure 121 shows the correspondence between the display external data area and the ICOM/ISEG pins. The LED turns on when the display data is '1', and turns off when it is '0'. Bits 31 to 16 are not implemented.

While ICOMx is driving, ISEGx output is ignored since ICOMx and ISEGx share an output pad.

Table 75. LED Display RAM

Name	**Address**	**Bit**						
		31	**…**	**15**	**…**	**2**	**1**	**0**
DISPRAM0	0x4000_6040	---	…	ISEG15	…	ISEG2	ISEG1	---
DISPRAM1	0x4000_6044	---	…	ISEG15	…	ISEG2	---	ISEG0
DISPRAM2	0x4000_6048	---	…	ISEG15	…	---	ISEG1	ISEG0
DISPRAM3	0x4000_604C	---	…	ISEG15	…	ISEG2	ISEG1	ISEG0
DISPRAM4	0x4000_6050	---	…	ISEG15	…	ISEG2	ISEG1	ISEG0
DISPRAM5	0x4000_6054	---	…	ISEG15	…	ISEG2	ISEG1	ISEG0
DISPRAM6	0x4000_6058	---	…	ISEG15	…	ISEG2	ISEG1	ISEG0
DISPRAM7	0x4000_605C	---	…	ISEG15	…	ISEG2	ISEG1	ISEG0
DISPRAM8	0x4000_6060	---	…	ISEG15	…	ISEG2	ISEG1	ISEG0
DISPRAM9	0x4000_6064	---	…	ISEG15	…	ISEG2	ISEG1	ISEG0
DISPRAM10	0x4000_6068	---	…	ISEG15	…	ISEG2	ISEG1	ISEG0
DISPRAM11	0x4000_606C	---	…	ISEG15	…	ISEG2	ISEG1	ISEG0
DISPRAM12	0x4000_6070	---	…	ISEG15	…	ISEG2	ISEG1	ISEG0

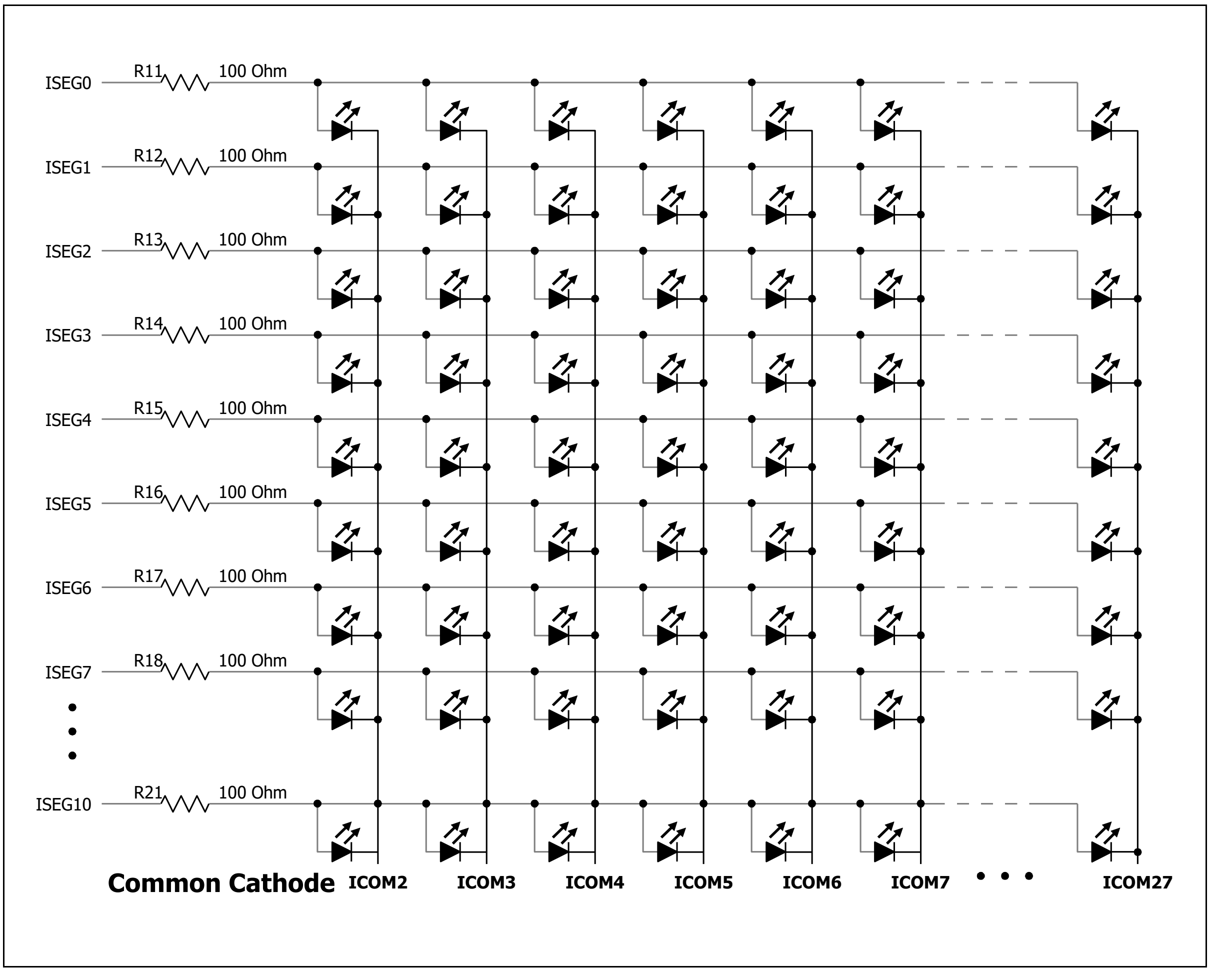


Figure 121. Example LED Schematic

20.3.2 MODE function

There are three modes as introduced below, depending on the set value of the LED_CON1<MD> bits:

1. First mode is LED auto mode that is irrelevant to touch sensing function. It starts by writing '1' to the LEDST using a program.

All modes introduced below are only possible after the LED_CON1<LEDEN> bit is set to '1'.

Figure 122 shows an example timing diagram of LED auto mode with COMER = 0100_0001. (k) in Figure 122 shows the overlap time that exists between different ICOM signals that are controllable by the program. The larger the ICOMx_DIMM value, the smaller the ICOM width in the arrow direction as shown in (j).

When enabling the LED by writing '1' to the LEDST bit as shown in (A), LED can operate continually. An interrupt occurs at point (B) where the LED 1 frame operation is terminated when the LED_INTE is set.

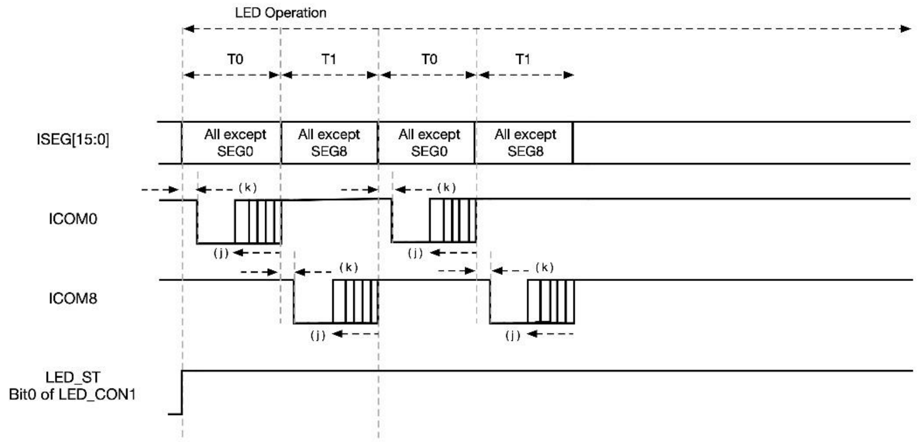


Figure 122. Example Timing Diagram of LED Auto Mode

2. The second mode is LED alone mode that is irrelevant to touch function. It can re-start by writing '1' to the LEDST bit using a program.

All modes introduced below are only possible after the LED_CON1<LEDEN> bit is set to '1'.

Figure 123 shows an example timing diagram of LED alone mode with LED_COMER reg = 000_0000_0000_0000_0000_0100_0001. (k) in Figure 123 shows the overlap time that exists between different ICOM signals that are controllable by the program. The larger the COMDIMM value, the smaller the ICOM width in the arrow direction as shown in (j).

An interrupt occurs at point (A) where the LED operation is terminated when the LED_INTE bit is set. When enabling the LED by re-writing '1' to the LEDST bit as shown in (B), LED can start again.

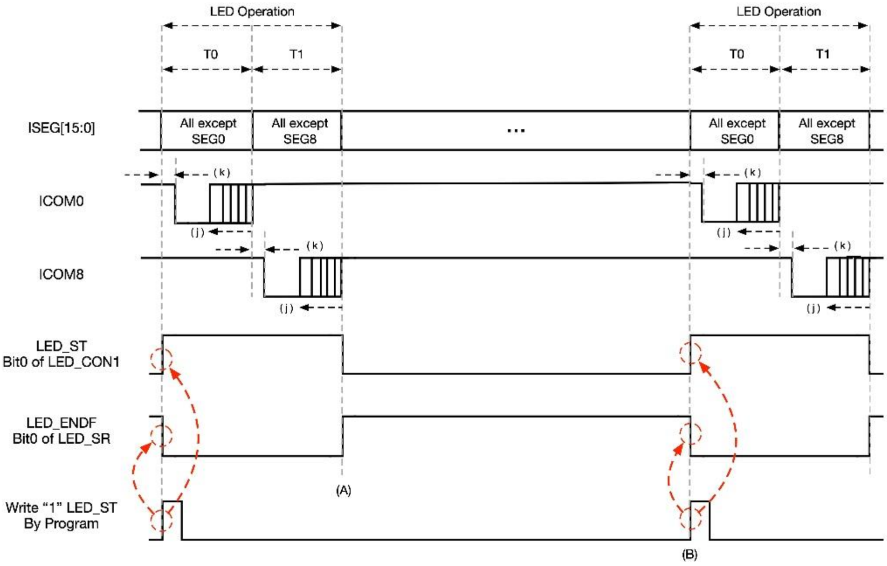


Figure 123. Example Timing Diagram of LED Alone Mode

3. The third mode is LED period mode. In this mode, the start of the next LED operation is determined by the LED period register value after the previous LED operation ends.

It is necessary to determine the period of frame in which the LED can operate without flicker.

Figure 124 shows an example timing diagram of LED period mode with LED_COMER reg = 0_0000_0000_0001.

At (A) when the LED is enabled by writing '1' to the LEDST bit, the 20-bit counter starts counting.

At (B) when LED operation is terminated, the LED operation is completed to set the LED_ENDF bit to '1', and the interrupt is generated. The 20-bit counter continues to operate without stopping.

At (C) when the Period match occurs, the LED_SR<MATCHF> flag is generated, the LED_ENDF bit is cleared to '0', and the 20-bit counter is initialized. After this, the LEDST bit is set to '1' automatically, and the LED operation and the 20-bit counter are re-started (B).

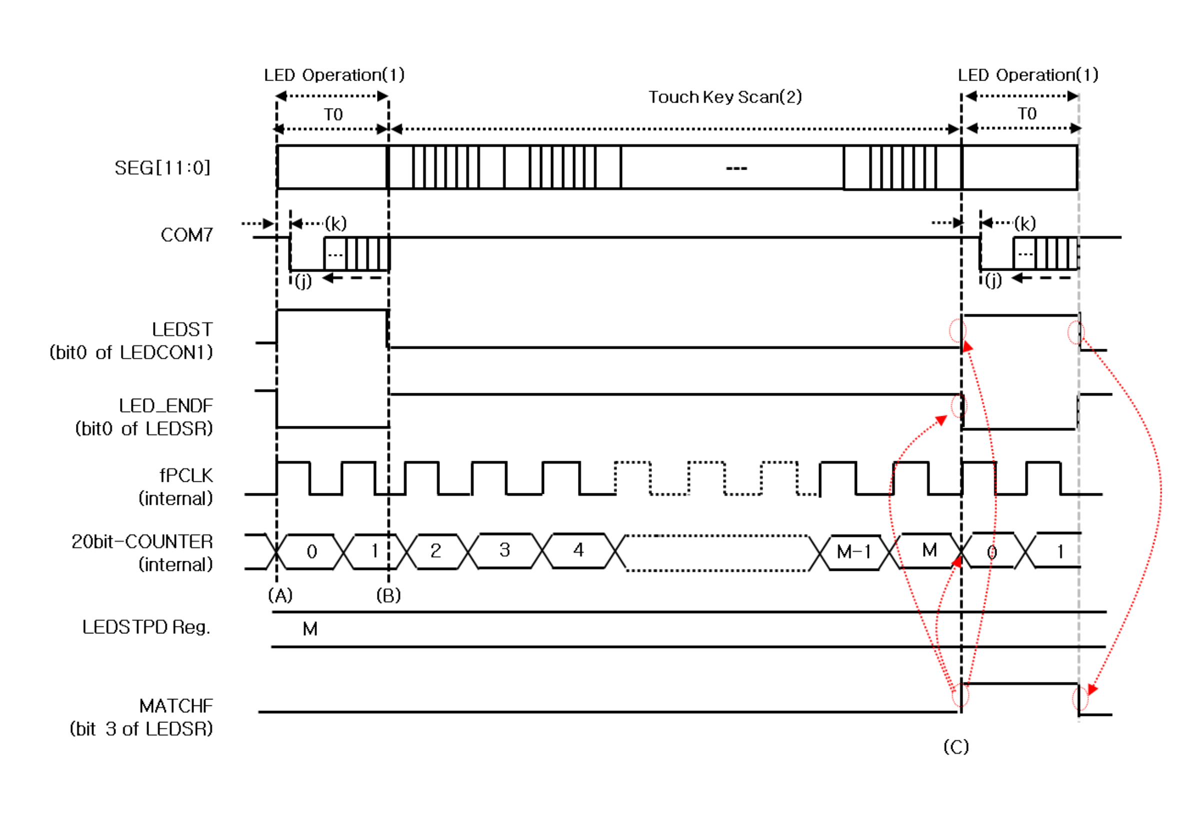


Figure 124. Example Timing Diagram of LED Period Mode

20.3.3 SEG-GND function

The ISEG-GND function removes the remaining charge on the pad by grounding the ISEG PAD during the overlap time that is required to prevent different ICOMs from being driven simultaneously.

Users can determine how long the ISEG PAD is grounded during the overlap time by configuring the LED_CON3<SET TIME n> bit and LED_CON3<CLR TIME n> bit. (n = 0, 1, 2, and 3)

Figure 125 shows a timing diagram of the ISEG-GND function, where PAD control signal is generated during the overlap time between ICOM0 and ICOM1. In the figure, (A) represents the ICOM0 end point, (B) the ISEC-GND active point, (C) the ISEG_GND inactive point, and (D) the ICOM1 start point, respectively.

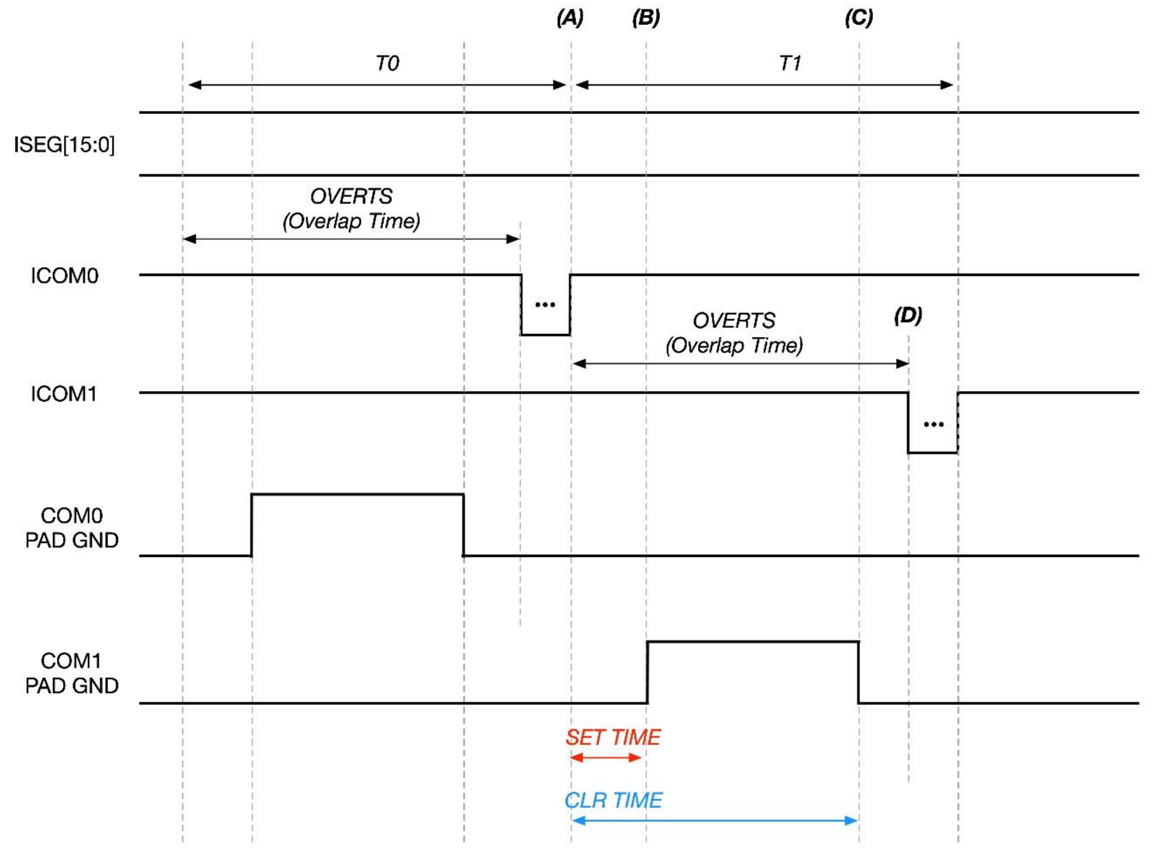


Figure 125. Timing Diagram of ISEG-GND Function

20.3.4 Log-scale dimming

The log-scale functionality of a ICOM can be enabled by setting the LED_LOGDE<LOGD EN n> bit. (n = 0, 1, 2, …, 12)

When the log-scale is enabled, users feel that LED brightness changes naturally due to the human brightness perception characteristics.

Figure 126 shows that the human eye feels a small change of the brightness as a big change at an interval with low measured light. Therefore, the log-scale dimming function is required to correct for this interval.

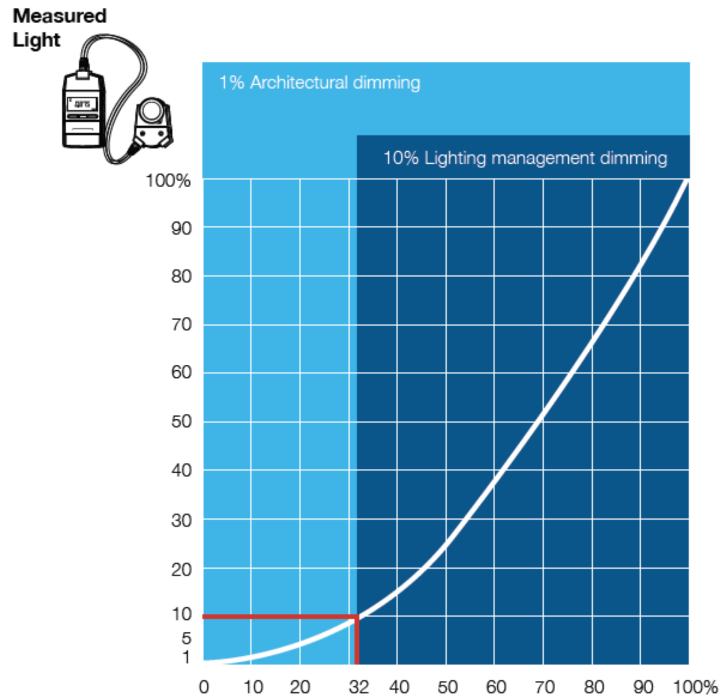


Figure 126. Perceived vs. Measured Light

Figure 127 shows the relative brightness^{NOTE} of log-scale dimming that is disabled or enabled according to the set value of the COM_DIMM register.

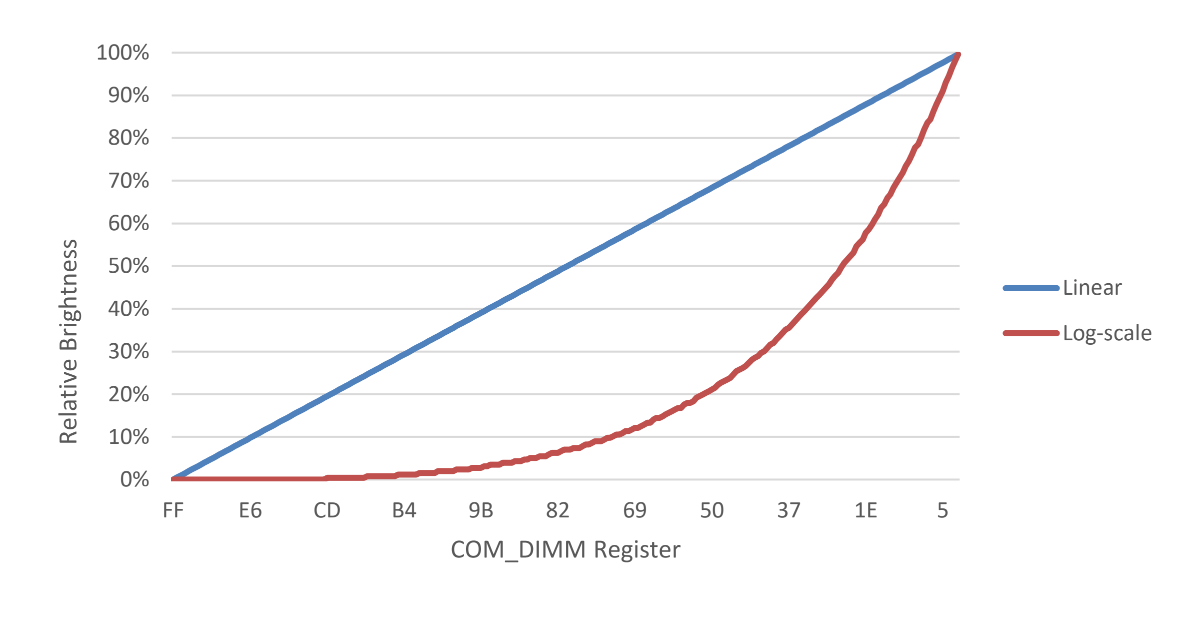


Figure 127. Relative Brightness of Linear Dimming and Log-scale Dimming by COM_DIMM

NOTE: Assuming that the ICOM width is brightness 100% when the COMDIMM is set to '0', Relative Brightness refers to the brightness converted based on the ICOM width, regardless of the COMPWID value.

Figure 128 shows that the internal log-scale dimmer's compensation characteristic changes with the relative brightness, according to the settings of the COMPWID register and overlap time. As shown in this figure, it is recommended that the COMPWID is set to FF and overlap time is set to f_{LEDCLK} / 2, when the LOG EN bit is enabled.

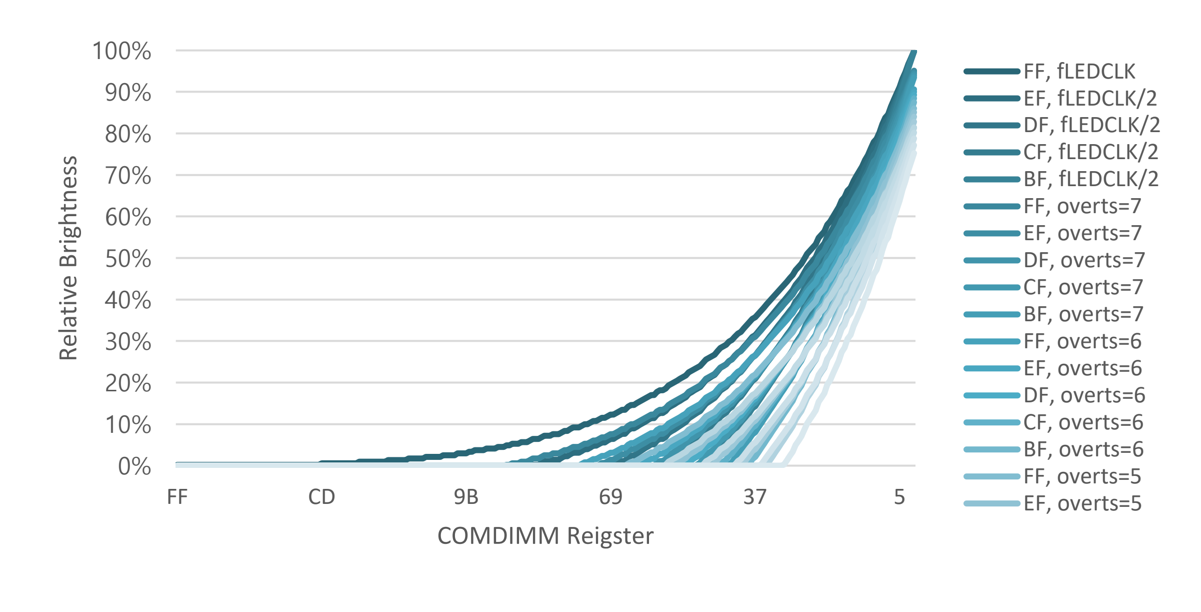


Figure 128. Brightness Characteristic Curve

21 Cyclic Redundancy Check (CRC) and checksum

Cyclic redundancy check (CRC) generator is used to get a 16-bit CRC code from Flash ROM and a generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the functional safety standards, they offer a means of verifying the Flash memory integrity. CRC generator helps compute a signature of the software during runtime, to be compared with a reference signature.

CRC generator of A31T21x series features the followings:

- Auto CRC (DMA) and User CRC Mode.
- Polynomial:
  - — CRC-CCITT ($G_1(x) = x^{16} + x^{12} + x^5 + 1$)
  - — CRC-16 ($G_2(x) = x^{16} + x^{15} + x^2 + 1$)
- CRC Mode and Checksum Mode.

21.1 CRC and checksum block diagram

Figure 129 describes the CRC and checksum in a block diagram.

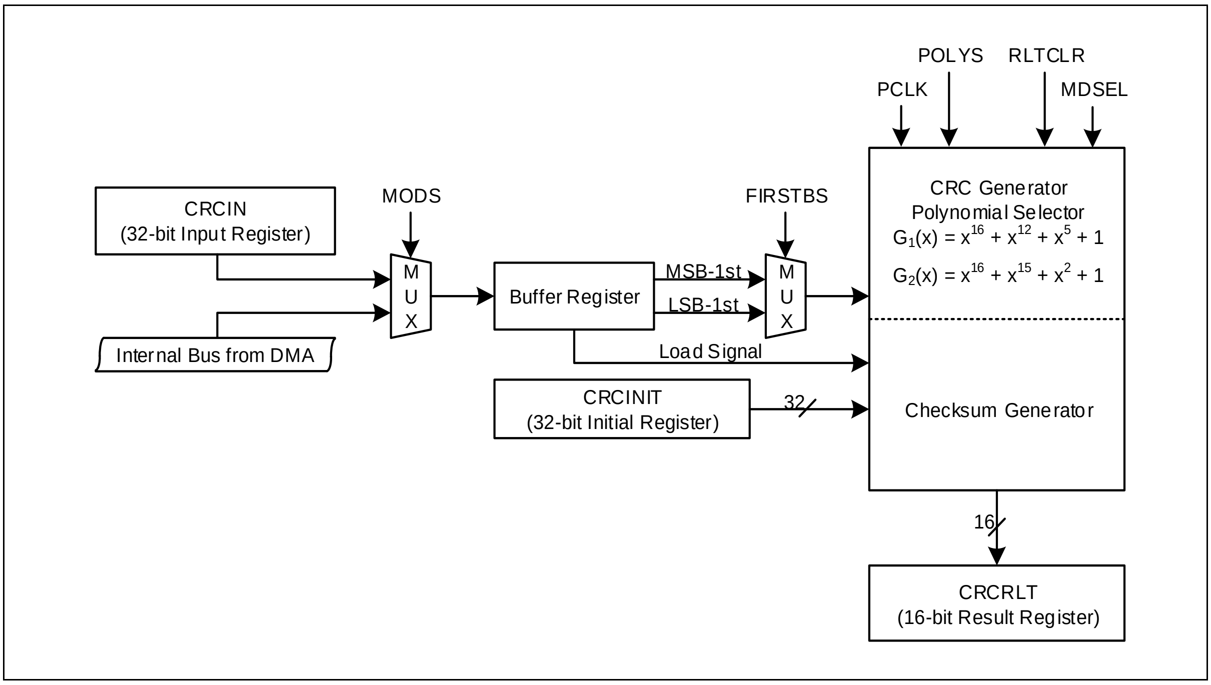


Figure 129. CRC and Checksum Block Diagram

21.2 Registers

Table 76 and Table 77 show base address and register map of the CRC and checksum block.

Table 76. Base Address of CRC

Name	Base address
CRC	0x4000_0300

Table 77. CRC Register Map

Name	Offset	Type	Description	Reset value	Reference
CRC_CR	0x0000	RW	CRC/Checksum Control Register	0x0000_0000	21.2.1
CRC_IN	0x0004	RW	CRC/Checksum Input Data Register	0x0000_0000	21.2.2
CRC_RLT	0x0008	RO	CRC/Checksum Result Data Register	0x0000_FFFF	21.2.3
CRC_INIT	0x000C	RW	CRC/Checksum Initial Data Register	0x0000_0000	21.2.4

21.2.1 CRC_CR: CRC control register

The CRC_CR is a 32-bit register with 32/16/8-bit access.

CRC_CR=0x4000_0300

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																						CRCINTEN	CRCINTF	MODS	RLTCLR	MDSEL	POLYS	Reserved		FIRSTBS	CRCRUN
-																						0	0	0	0	0	0	-		0	0
-																						RW	RW	RW	RW	RW	RW	-		RW	RW

9	CRCINTEN	CRC DMA interrupt enable bit	
		0	Disable
		1	Enable
8	CRCINTF	CRC DMA done interrupt flag bit	
		0	No request occurred
		1	Request occurred, This bit is cleared to '0' when write '1'.
7	MODS	User/DMA Mode Selection bit.	
		0	User mode. (Calculation every writing data to the CRC_IN register)
		1	Auto mode. (Calculation till CRCSADR == CRCEADR)
6	RLTCLR	CRC/Checksum Result Data Register (CRC_RLT) Initialization bit.	
		0	No effect.
		1	Initialize the CRC_RLT register with the value of CRC_INIT (This bit is automatically cleared to "0b" after operation)
NOTE: The checksum is calculated by byte unit. Ex) On 0x34A7E991, CRCRLT = 0x34 + 0xA7 + 0xE9 + 0x91.			
5	MDSEL	CRC/Checksum Selection bit.	
		0	Select CRC.
		1	Select checksum.
		Note) The checksum is calculated by byte unit. Ex) On 0x34A7E991, CRCRLT = 0x34 + 0xA7 + 0xE9 + 0x91.	
4	POLYS	Polynomial Selection bit. (CRC only)	
		0	Select CRC-CCITT ($G_1(x) = x^{16} + x^{12} + x^5 + 1$)
		1	Select CRC-16 ($G_2(x) = x^{16} + x^{15} + x^2 + 1$)
1	FIRSTBS	First Shifted-in Selection bit. (CRC only)	
		0	MSB-1st.
		1	LSB-1st.
0	CRCRUN	CRC/Checksum enable control. In DMA mode, this bit is a busy bit.	
		0	Not busy. The CRC operation can be finished by writing "0b" to this bit on running.
		1	Start CRC operation.

NOTES:

1. The CRC_RLT register and the CRC/Checksum block should be initialized by writing "1b" to the RLTCLR bit before a new CRC/Checksum calculation.
2. The CRCRUN bit should be set to "1b" last time after setting appropriate values to the registers.
3. On the user mode, it will be calculated every writing data to the CRC_IN register during CRCRUN=1.
4. The 4 "NOP instruction" should follow immediately after this bit is set.
5. It will be calculated every writing data to the CRC_IN register during CRCRUN=1.
6. It is prohibited writing any data to the CRC_IN register during CRCRUN=0 or running in DMA mode.

21.2.2 CRC_IN: CRC input data register

The CRC_IN is a 32-bit register.

CRC_IN=0x4000_0304

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
INDATA			
0x00000000			
RW			

31 0	INDATA	CRC Input Data bits.
NOTE: The CRC_IN register should be written by 1-word (32-bits).		

21.2.3 CRC_RLT: CRC result data register

The CRC_RLT is a 32-bit register with 32/16/8-bit access.

CRC_RLT=0x4000_0308

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved		RLTDATA	
-		0xFFFF	
-		RO	

15 0	RLTDATA	CRC Result Data bits.

21.2.4 CRC_INIT: CRC initial data register

The CRC_INIT is a 32-bit register with 32/16/8-bit access.

CRC_INIT=0x4000_030C

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
Reserved		INIDATA	
-		0x0000	
-		RW	

15 0	INIDATA	CRC Initial Data bits.

21.3 Functional description

21.3.1 CRC polynomial structure

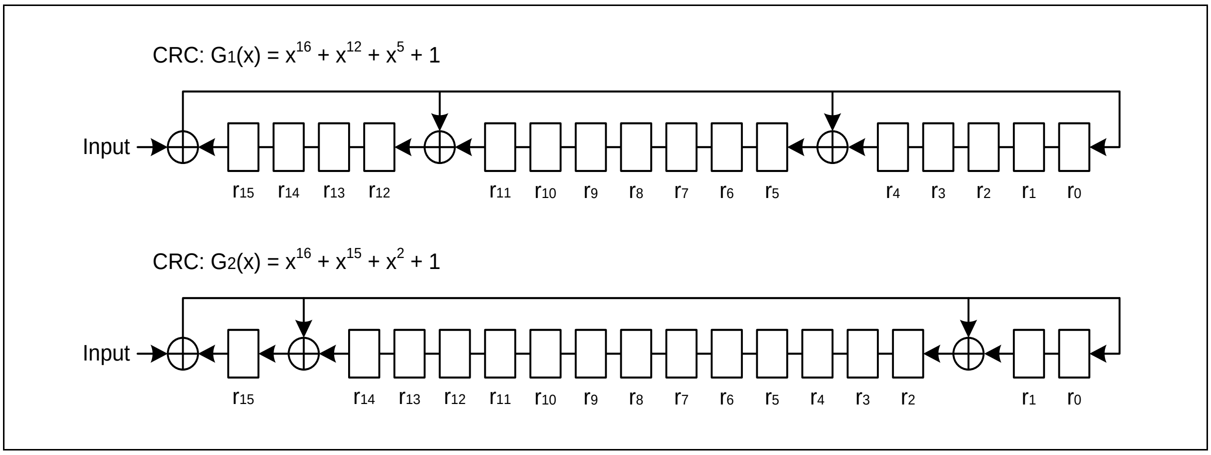

CRC: G1(x) = x16 + x12 + x5 + 1
Input
r15 r14 r13 r12 r11 r10 r9 r8 r7 r6 r5 r4 r3 r2 r1 r0
CRC: G2(x) = x16 + x15 + x2 + 1
Input
r15 r14 r13 r12 r11 r10 r9 r8 r7 r6 r5 r4 r3 r2 r1 r0

Figure 130. CRC Polynomial Structure

21.3.2 CRC operation procedure in auto CRC/checksum (DMA) mode

1. CRC/Checksum Enable and Clock Enable. (SCU_PCER, SCU_PER)
2. Set CRC initial data register. (CRC_INIT)
3. Global interrupt disable.
4. Select Auto CRC/Checksum mode and CRC.
5. CRC operation starts. (CRCRUN = 1)
6. DMA configuration & operation
7. Read the CRC result.
8. Global interrupt enable.

21.3.3 CRC operation procedure in user CRC/checksum mode

1. CRC/Checksum Enable and Clock Enable (SCU_PCER, SCU_PER)
2. Set CRC initial data register. (CRC_INIT)
3. Select User CRC/Checksum Mode and CRC.
4. CRC operation enable. (CRCRUN = 1)
5. Input CRC Data at CRC_IN.
6. CRC stops and reads CRC result.

22 Electrical characteristics

22.1 Absolute maximum ratings

Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions.

Table 78. Absolute Maximum Rating

Parameter	Symbol	Ratings	Unit	Remark
Supply voltage	V_{DD}	-0.3 – +6.5	V	—
Normal pin	V_I	-0.3 – VDD+0.3	V	Voltage on any pin with respect to V_{SS}
	V_O	-0.3 – VDD+0.3	V	
	I_{OH}	-20	mA	Maximum output current sourced by per I/O pin
	ΣI_{OH}	-100	mA	Total output current sourced by sum of all I/Os
	I_{OL1}	25	mA	Maximum output current sunk by per I/O pin
	ΣI_{OL1}	210	mA	Total output current sunk by sum of all I/Os
LED ICOM pin	I_{OL2}	250	mA	Maximum output current sunk by per LED ICOM pin
	ΣI_{OL2}	250	mA	Total output current sunk by sum of all LED ICOM
Total power dissipation	T_P	300	mW	—
Storage temperature	T_{STG}	-55 – +125	℃	—

22.2 Recommended operating conditions

Table 79. Recommended Operating Condition

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	Core and Peripherals	1.8	—	5.5	V
		ADC	2.4	—	5.5	V
		LED/LCD/TOUCH	2.7	—	5.5	V
		HSE	1.8	—	5.5	V
		LSE	2.7	—	5.5	V
Operating frequency	f_{OP}	PLL	1	—	48	MHz
		HSE	1	—	16	MHz
		LSE	—	32.768	—	kHz
		HSI	31.52	32.00	32.48	MHz
		LSI	400	500	600	kHz
Operating temperature	T_{OP}	Top	-40	+25	+105	℃
		TOUCH	-40	+25	+85	℃

22.3 POR (Power on Reset) characteristics

Table 80. Operating Condition of POR

Parameter	Symbol	Min	Typ.	Max	Units
Analog supply voltage	V_{DD}	VSS	5.0	5.5	V
Operating Temperature	T_A	-40	25	105	℃

Table 81. POR Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
Operating current	I_{DD}	–	-	0.5	4	uA
POR set level	V_{SET}	–	1.20	1.40	1.60	V
POR reset level	V_{RESET}	–	1.00	1.20	1.40	V
Supply rising rate	T_{rVDD}		0.05	-	50	ms/V
Supply falling rate	T_{fVDD}		-	-	2.5	ms/V

NOTE: The specifications of the parameters are guaranteed by design.

22.4 LVI (Low Voltage Indicator) LVR (Low Voltage Reset) characteristics

Table 82. Operating Condition of Low Voltage Reset

Parameter	Symbol	Min	Typ.	Max	Units
Operating temperature	T_A	-40	25	105	℃

Table 83. Low Voltage Indicator Characteristics

Parameter	Symbol		Conditions	Min	Typ.	Max	Units
Operating voltage	VDD			0.8	5.0	5.5	V
Detection level	V_{LVI}	Level0	Rising voltage	1.49	1.60	1.71	V
			Falling voltage	1.45	1.56	1.67	
		Level1	Rising voltage	1.62	1.74	1.86	
			Falling voltage	1.58	1.70	1.82	
		Level2	Rising voltage	1.70	1.83	1.96	
			Falling voltage	1.66	1.79	1.92	
		Level3	Rising voltage	1.83	1.96	2.09	
			Falling voltage	1.78	1.91	2.04	
		Level4	Rising voltage	1.92	2.06	2.20	
			Falling voltage	1.86	2.00	2.14	
		Level5	Rising voltage	2.04	2.19	2.34	
			Falling voltage	1.98	2.13	2.28	
		Level6	Rising voltage	2.21	2.37	2.53	
			Falling voltage	2.15	2.31	2.47	
		Level7	Rising voltage	2.37	2.54	2.71	
			Falling voltage	2.31	2.48	2.65	
		Level8	Rising voltage	2.56	2.75	2.94	
			Falling voltage	2.49	2.68	2.87	
		Level9	Rising voltage	2.91	3.13	3.35	
			Falling voltage	2.83	3.05	3.27	
		Level10	Rising voltage	3.05	3.28	3.51	
			Falling voltage	2.97	3.19	3.41	
		Level11	Rising voltage	3.45	3.70	3.95	
			Falling voltage	3.35	3.60	3.85	
		Level12	Rising voltage	3.58	3.84	4.10	
			Falling voltage	3.48	3.74	4.00	
		Level13	Rising voltage	3.86	4.15	4.44	
			Falling voltage	3.76	4.04	4.32	
		Level14	Rising voltage	4.03	4.33	4.63	
			Falling voltage	3.92	4.22	4.52	
		Level15	Rising voltage	4.30	4.62	4.94	
			Falling voltage	4.18	4.50	4.82	

Table 84. Low Voltage Reset Characteristics

Parameter	Symbol		Conditions	Min	Typ.	Max	Units
Operating voltage	VDD			0.8	5.0	5.5	V
Detection level	V_{LVR}	Level0	Rising voltage	1.49	1.60	1.71	V
			Falling voltage	1.45	1.56	1.67	
		Level1	Falling voltage	1.58	1.70	1.82	
		Level2	Falling voltage	1.66	1.79	1.92	

		Level3	Falling voltage	1.78	1.91	2.04	
		Level4	Falling voltage	1.86	2.00	2.14	
		Level5	Falling voltage	1.98	2.13	2.28	
		Level6	Falling voltage	2.15	2.31	2.47	
		Level7	Falling voltage	2.31	2.48	2.65	
		Level8	Falling voltage	2.49	2.68	2.87	
		Level9	Falling voltage	2.83	3.05	3.27	
		Level10	Falling voltage	2.97	3.19	3.41	
		Level11	Falling voltage	3.35	3.60	3.85	
		Level12	Falling voltage	3.48	3.74	4.00	
		Level13	Falling voltage	3.76	4.04	4.32	
		Level14	Falling voltage	3.92	4.22	4.52	
		Level15	Falling voltage	4.18	4.50	4.82	

Table 85. Low Voltage Reset Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
Noise cancelling time	—		—	2	-	us
Operation current	I_{DD}		—	3.5	5	uA
Operation current(STOP)	$I_{DD, STOP}$		—	2.5	3	nA

NOTES:

1. The specifications of the parameters are guaranteed by design.
2. To use LVR or LVI function while the system is in STOP mode (DEEP SLEEP mode), set SCU_SMR <BGRAON> to '1' to enable BGR function of VDC.

22.5 HSI (High Frequency Internal) RC oscillator characteristics

Table 85. Operating Condition of HSI

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	VDD	1.8	5.0	5.5	V
Operating temperature	T_A	-40	25	105	℃

Table 86. High Frequency Internal RC Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{HSI}	V_{DD} = 1.8V to 5.5V T_A = – 20 °C to + 85 °C	31.68	32.0	32.32	MHz
Frequency	f_{HSI}	V_{DD} = 1.8V to 5.5V T_A = – 40 °C to + 105 °C	31.52	32.0	32.48	MHz
Tolerance	–	T_A = – 20 °C to + 85 °C	-1.0	–	1.0	%
		T_A = – 40 °C to + 105 °C	-1.5	–	1.5	%
Clock duty ratio	T_{OD}	–	–	50	–	%
Stabilization time	t_{HFS}	–	100	–	–	us
IRC current	I_{HSI}	Enable	–	300	350–	uA
		Disable	–	1	–	uA

NOTE: The specifications of the parameters are guaranteed by design.

22.6 LSI (Low Frequency Internal) RC oscillator characteristics

Table 87. Operating Condition of LSI

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	VDD	1.8	5.0	5.5	V
Operating temperature	T_A	-40	25	105	℃

Table 88. Low Frequency (500KHz) Internal RC Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating current	I_{LIRC}	Enable	—	3.2	4.3	uA
		Disable	—	1	20	nA
Frequency	f_{LSI}	V_{DD} = 1.8V to 5.5V T_A = – 40 °C to + 105 °C	400	500	600	kHz
Tolerance	–	V_{DD} = 1.8V to 5.5V T_A = – 40 °C to + 105 °C	-20	–	20	%

NOTE: The specifications of the parameters are guaranteed by design.

22.7 HSE (main oscillator) characteristics

Table 89. Operating Condition of HSE

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	VDD	1.8	5.0	5.5	V
Operating temperature	T_A	-40	25	105	℃

Table 90. Main Oscillator Characteristics

Oscillator	Parameter	Conditions	Min	Typ.	Max	Units
Operating current	I_{DD}	—	—	—	2.5	mA
Power down current	I_{STOP}	—	—	0.2	30	nA
Output frequency	XOUT input frequency	VDDEXT ≥ 1.8V SCU_EOSCR < ISEL[1:0] >= 2'b11 SCU_EOSCR < NCOPT[1:0] >= 2'b00	1.0	—	4.0	MHz
		VDDEXT ≥ 2.0V SCU_EOSCR < ISEL[1:0] >= 2'b10 SCU_EOSCR < NCOPT[1:0] >= 2'b01	1.0	—	8.0	MHz
		VDDEXT ≥ 2.2V SCU_EOSCR < ISEL[1:0] >= 2'b01 SCU_EOSCR < NCOPT[1:0] >= 2'b10	1.0	—	12.0	MHz
		VDDEXT ≥ 2.4V SCU_EOSCR < ISEL[1:0] >= 2'b00 SCU_EOSCR < NCOPT[1:0] >= 2'b11	1.0	—	16	MHz
Start-up time	T_{start}	—	—	2	—	ms
Crystal input (low)	V_{IL}	—	—	—	0.2VDD	V
Crystal input (high)	V_{IH}	—	0.8VDD	—	—	V
Crystal out (low)	V_{OL}	—	—	—	0.2VDD	V
Crystal out (high)	V_{OH}	—	0.8VDD	—	—	V
External load cap	C_L	1M < f_{OUT} < 4M	18	30	35	pf
		4M < f_{OUT} < 12M	10	22	30	pf
		12M < f_{OUT} < 16M	7	18	22	pf
Feedback resistance	R_{FB}	VDDEXT = 5V	0.7	1.0	1.3	MΩ

NOTE: The specifications of the parameters are guaranteed by design.

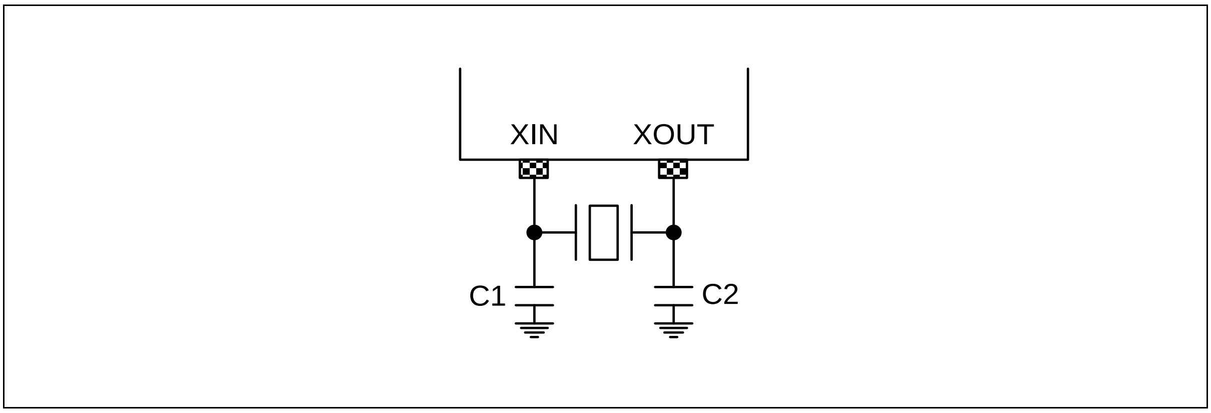


Figure 131. Crystal/Ceramic Oscillator

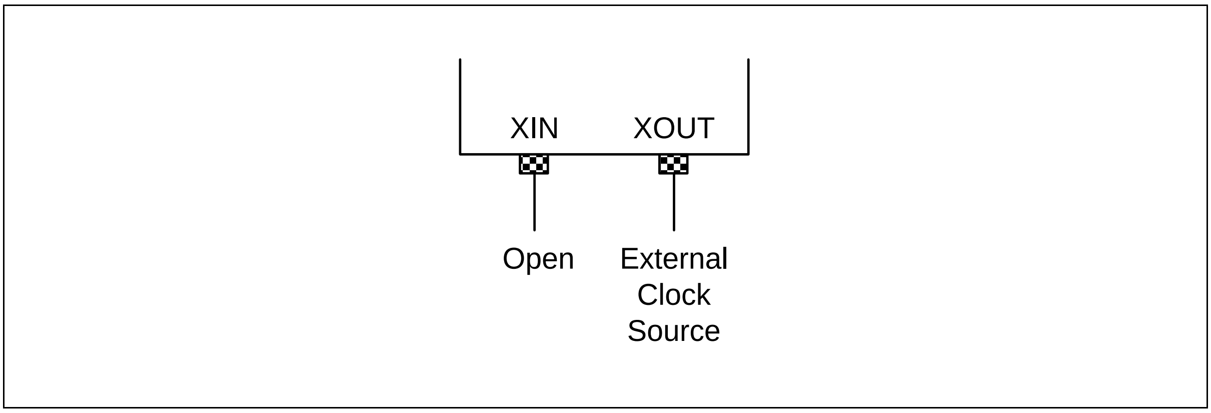


Figure 132. External Clock

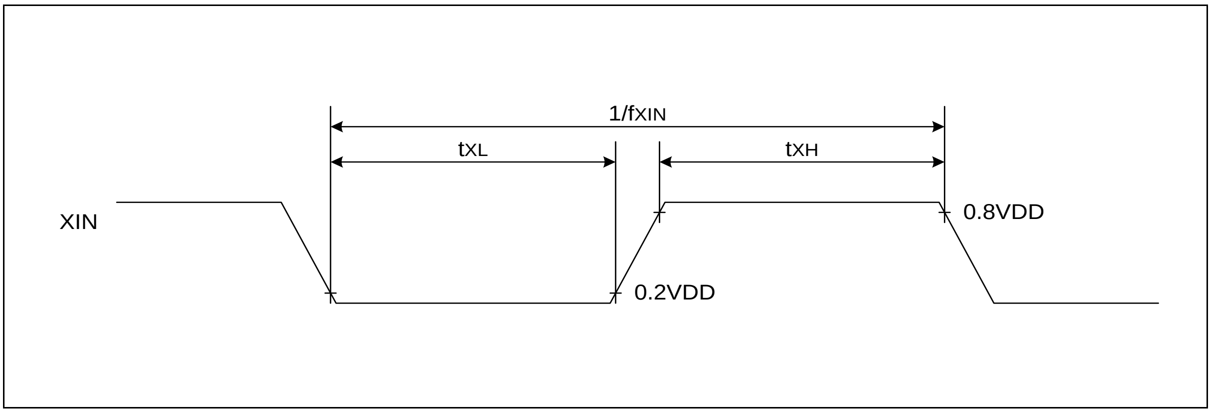


Figure 133. Clock Timing Measurement at XIN

22.8 LSE (sub oscillator) characteristics

Table 91. Operating Condition of LSE

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V_{DD}	2.7	5.0	5.5	V
Operating temperature	T_A	-40	25	105	℃

Table 92. Sub Oscillator Characteristics

Oscillator	Parameter	Conditions	Min	Typ	Max	Units
Operating current	I_{DD}			-	5.0	uA
Power down current	I_{STOP}	—	—	0.2	15.0	nA
Output frequency	f_{SUB}	—	—	32.768	—	KHz
Start-up time	T_{start}	—	—	2	—	s
Crystal input (low)	V_{IL}	—	—	—	0.2VDD	V
Crystal input (High)	V_{IH}	—	0.8VDD	—	—	V
Crystal out (low)	V_{OL}	—	—	—	0.2VDD	V
Crystal out (high)	V_{OH}	—	0.8VDD	—	—	V
External load cap	R_{FB}	—	5	15	35	pF
Feedback resistance	C_L	—	7	12	24	MΩ

NOTE: The specifications of the parameters are guaranteed by design.

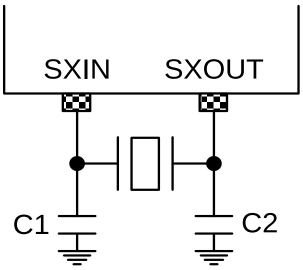


Figure 134. Crystal Oscillator

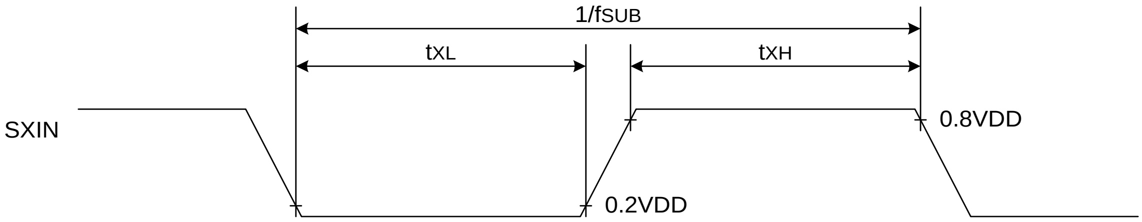


Figure 135. Clock Timing Measurement at SXIN

22.9 PLL electrical characteristics

Table 93. Operating Condition of PLL

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V_{DD}	1.8	5.0	5.5	V
Operating temperature	T_A	-40	25	105	℃

Table 94. PLL Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating current	I_{DD}	Enable	—	—	1	mA
		Disable	—	5	500	nA
Output frequency	f_{OUT}	—	1	—	48	MHz
Duty	f_{DUTY}		40	—	60	%
VCO Frequency	f_{VCO}		10	—	240	MHz
Frequency Peak-to-Peak Jitter	$f_{JITTER(P-P)}$				500	ps
VCO Linear Range	f_{VCO_LIN}		50	—	150	MHz
Input Frequency[NOTE3]	$f_{PLLINCLK}$		4	8	16	MHz
Locking Time[NOTE2]	t_{LOCK}		—	60	100	us
Input Bandwidth	f_{IN}		—	2	—	MHz

NOTES:

1. The specifications of the parameters are guaranteed by design.
2. The tolerance of PLL output frequency is reflected based on PLL input clock source selected by PLLINCLKSEL in the SCU_SCCR[2] register.
3. It is recommended to use 8MHz for input frequency.

22.10 Supply current characteristics

Table 95. Operating Condition of Supply Current

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V_{DD}	1.8	5.0	5.5	V
Operating temperature	T_A	-40	25	105	℃

Table 96. Supply Current Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply current	I_{DD1} (Run)	f_{PLL} = 48MHz	VDD=5V±10% T_A =25℃ All peripherals off	-	9.0	12.0	mA
		f_{HSI} = 32MHz		-	6.0	8.0	
		f_{XIN} = 8MHz		-	3.0	4.0	
		f_{LSI} = 500KHz		-	200	600	uA
		f_{LSE} = 32.768KHz		-	140	300	
	I_{DD2} (Sleep)	f_{PLL} = 48MHz	VDD=5V±10% T_A =25℃ All peripherals off	-	6.0	10.0	mA
		f_{HSI} = 32MHz		-	4.0	7.0	
		f_{XIN} = 8MHz		-	2	6	
		f_{LSI} = 500KHz		-	180	500	uA
		f_{LSE} = 32.768KHz		-	130	400	
	I_{DD3} (Deep-Sleep) (STOP1)	WDTRC = ON, (LSIAON=ENABLE) [NOTE4], LVD=ON	VDD=5V±10% T_A =25℃	-	50	-	uA
	I_{DD4} (Deep-Sleep) (STOP1)	WDTRC = ON, (LSIAON=ENABLE) [NOTE4], LVD=OFF[NOTE5]	VDD=5V±10% T_A =25℃	-	30	-	uA
	I_{DD5} (Deep-Sleep) (STOP2)	WDTRC = OFF, LVD=ON	VDD=5V±10% T_A =25℃	-	15	-	uA
	I_{DD6} (Deep-Sleep) (STOP2)	WDTRC = OFF, LVD=OFF [NOTE5]	VDD=5V±10% T_A =25℃	-	2	-	uA

NOTES:

1. The specifications of the parameters are guaranteed by design.
2. All supply current items do not include the current of a low frequency internal RC oscillator and a peripheral block.
3. All supply current items include the current of the power-on reset (POR) block.
4. SCU_SMR<LSIAON> bit must be enabled in order to use the WDT as a wake up source in deep-sleep mode(STOP1).
5. 'LVD = OFF' indicates that LVR reset function , LVR block and LVI block are disabled.
   — LVRRST in SCU_RSER = 0
   — LVREN[7:0] in SCULV_LVRCR = 0x55 (LVREN=0)
   — LVRENM[7:0] in SCULV_LVRCNFIG = 0xAA (LVRENM=0)
   — LVIEN in SCULV_LVICR = 0

22.11 I/O port characteristics

Table 97. Operating Condition of I/O Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V_{DD}	1.8	5.0	5.5	V
Operating temperature	T_A	-40	25	105	℃

22.11.1 General I/O characteristics

Parameters given in Table 98 for I/O static characteristics are derived from tests performed under the ambient temperature, and VDD supply voltage conditions summarized in Table 97.

Table 98. I/O Static Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output high voltage	V_{OH1}	V_{DD}=5V, I_{OH}=-2.68mA All output ports NOTE2	0.8VDD	-	VDD	V
	V_{OH2}	V_{DD}=5V, I_{OH}=-3.80mA All output ports NOTE3				
	V_{OH3}	V_{DD}=5V, I_{OH}=-2.54mA All output ports NOTE4				
Output low voltage	V_{OL1}	V_{DD}=5V, I_{OL}=3.68mA All output ports NOTE2	0	-	0.2VDD	V
	V_{OL2}	V_{DD}=5V, I_{OL}=3.74mA All output ports NOTE3				
	V_{OL3}	V_{DD}=5V, I_{OL}=3.74mA All output ports NOTE4				
ISEG output high voltage NOTE5	V_{OHSEG0}	V_{DD}=5V, I_{OH}=-8.66mA, TA=25°C	-	V_{DD}-0.5	-	V
	V_{OHSEG1}	V_{DD}=5V, I_{OH}=-13.22mA, TA=25°C	-	V_{DD}-0.5	-	V
	V_{OHSEG2}	V_{DD}=5V, I_{OH}=-19.49mA, TA=25°C	-	V_{DD}-0.5	-	V
	V_{OHSEG3}	V_{DD}=5V, I_{OH}=-22.06mA, TA=25°C	-	V_{DD}-0.5	-	V
ISEG current matching NOTE1	ITOSEG	V_{DD}=5V, V_{OH}=4.5V, TA=25°C, V_{OHSEG1}	-5	-	5	%
ICOM output low voltage	V_{OLCOM}	V_{DD}=5V, I_{OL}=250mA, TA=25°C LED ICOM High sink current output	-	1.5	-	V
Input high voltage	V_{IH1}	All Input ports	0.8*V_{DD}	—	V_{DD}	V
Input low voltage	V_{IL1}	All Input ports	V_{GND}	—	0.2*V_{DD}	V
Input high leakage current	I_{IHLKG}	All Input ports	—	—	1	uA
Input low leakage	I_{ILLKG}	All Input ports	-1	—	—	uA

current						
Pull-up resistor	R_{PU}	All Input pins	25	50	100	KΩ
Pull-down resistor	R_{PD}	All Input pins	25	50	100	KΩ
I/O pin capacitance	C_{IO}	—	—	TBD	—	pF

NOTES:

1. The specifications of the parameters are guaranteed by design.
2. PA[0], PB[3], PC[8:5, 2:0], PE[12], PF[7:4]
3. PA[11:1], PB[11:4, 2:0], PE[11:8], PF[3:0]
4. PC[4:3], PD[5:0], PE[7:0]
5. The items are classified according to the CCSTRIM[1:0] in LED_CCSTRIM register.
6. In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in **22.1 Absolute maximum ratings**.
   - The sum of the currents sourced by all the I/Os on VDD, plus the maximum run consumption of the MCU sourced on VDD, cannot exceed the absolute maximum rating ΣIOH.
   - The sum of the currents sunk by all the I/Os on VSS plus the maximum run consumption of the MCU sunk on VSS cannot exceed the absolute maximum rating ΣIOL.
7. SEG Current Matching represents (ISEGx - ISEGAVR) / ISEGAVR)
   - ISEGx: Output high current on each SEG pin (x = 0 to 15)
   - ISEGAVR: Sum of ISEG0 to ISEG15

22.11.2 I/O AC characteristics

The definition and values of external input AC characteristics are given in Table 99 and Figure 136.

Table 99. External Input AC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Interrupt input high low width	t_{IWH}, t_{IWL}	All external interrupts 1.8 V≤V_{DD}≤ 5.5 V -40 °C≤T_A ≤105 °C	0.2	—	—	ns
External counter input high low pulse width	t_{ECWH}, t_{ECWL}	ECn, All external counter input 1.8 V≤V_{DD}≤ 5.5 V -40 °C≤T_A ≤105 °C	100	—	—	
External counter transition time	t_{REC}, t_{FEC}	ECn, All external counter input 1.8 V≤V_{DD}≤ 5.5 V -40 °C≤T_A ≤105 °C	—	—	20	

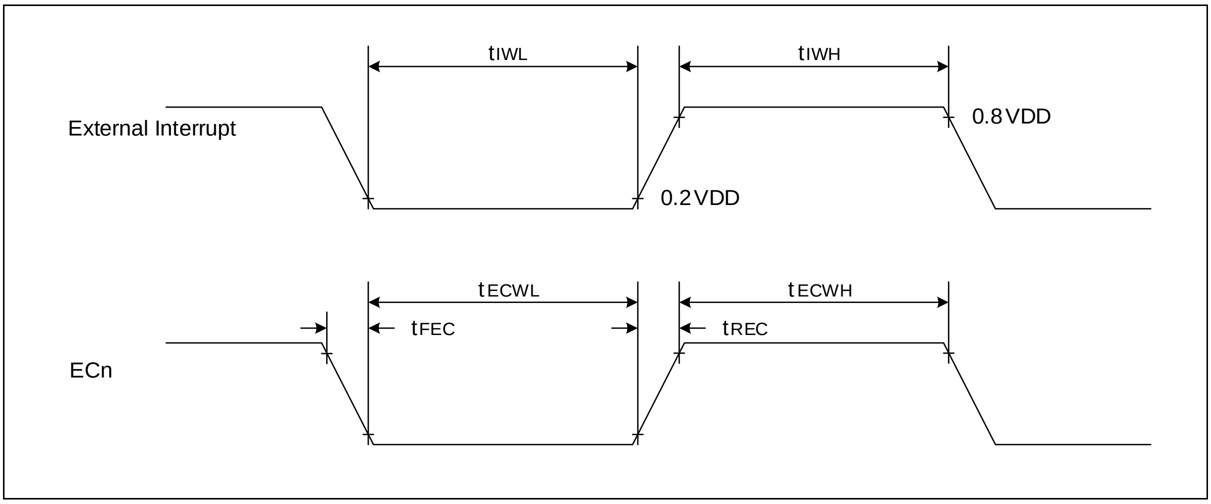


Figure 136. Timing Diagram of External Input AC Characteristics Definitions

22.12 UART characteristics

Table 100. Operating Condition of UART

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V_{DD}	1.8	5.0	5.5	V
Operating temperature	T_A	-40	25	105	℃

22.13 SPI characteristics

Parameters given in for SPI are derived from tests performed under the ambient temperature, and fPCLK frequency and VDD supply voltage conditions summarized in .

Table 101. Operating Condition of SPIn (n = 20, 21)

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V_{DD}	1.8	5.0	5.5	V
Operating temperature	T_A	-40	25	105	℃

Table 102. SPIn Characteristics (n = 20, 21)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
SPI clock frequency	f_{SCK1}	SPI20, SPI21 $V_{DD} \leq 1.8$ V	—	—	5	MHz
	f_{SCK2}	SPI20, SPI21 $V_{DD} \leq 3.3$ V	—	—	8	MHz
	f_{SCK3}	SPI20, SPI21 $V_{DD} \leq 5.5$ V	—	—	10	MHz
Duty cycle of SPI frequency (SCK)	Duty	Slave mode	30	50	70	%
Capacitance load	C_{CL}	—	—	—	TBD	pF

NOTE: The specifications of the parameters are guaranteed by design.

22.14 USART SPI characteristics

Table 103. Operating Condition of USART SPI

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V_{DD}	1.8	5.0	5.5	V
Operating temperature	T_A	-40	25	105	℃

Table 104. USART SPI Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output clock pulse period	tSCK	Internal SCK source	400	—	—	ns
Input clock pulse period		External SCK source	400	—	—	
Output clock high, low pulse width	tSCKH, tSCKL	Internal SCK source	180	—	—	
Input clock high, low pulse width		External SCK source	180	—	—	
First output clock delay time	tFOD	Internal/external SCK source	200	—	—	
Output clock delay time	tDS	—	—	—	100	
Input setup time	tDIS	—	180	—	—	
Input hold time	tDIH	—	180	—	—	

NOTE: The specifications of the parameters are guaranteed by design.

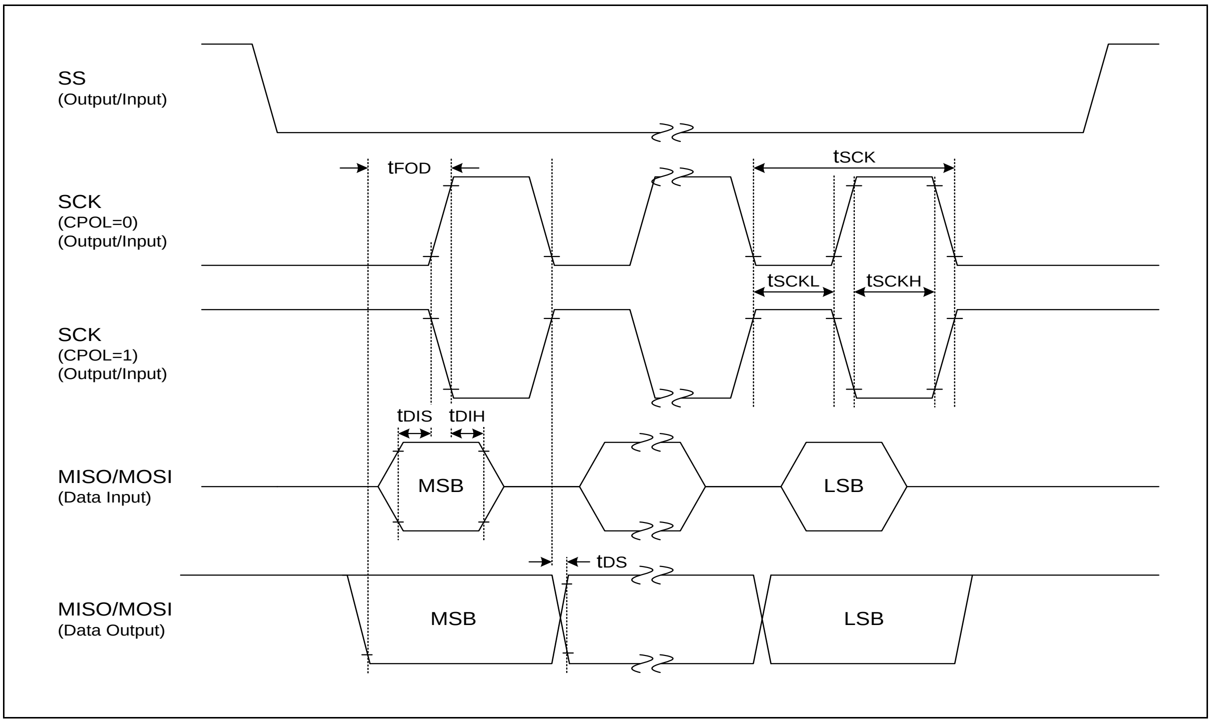


Figure 137. SPI (USART) Timing Diagram

22.15 USART UART timing characteristics

Table 105. Operating Condition of USART UART

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V_{DD}	1.8	5.0	5.5	V
Operating temperature	T_A	-40	25	105	℃

Table 106. USART UART Timing Characteristics

Parameter	Symbol	Typ	Units
Serial port clock cycle time	tSCK	tCPU x 16	us

NOTE: The specifications of the parameters are guaranteed by design.

tCPU : BDR * 2 * (1/PCLK)

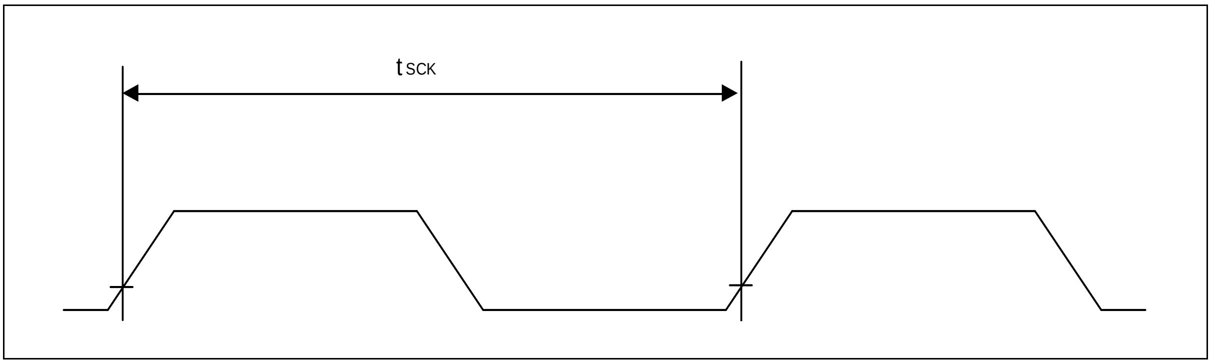


Figure 138. Timing Diagram of UART Timing Characteristics

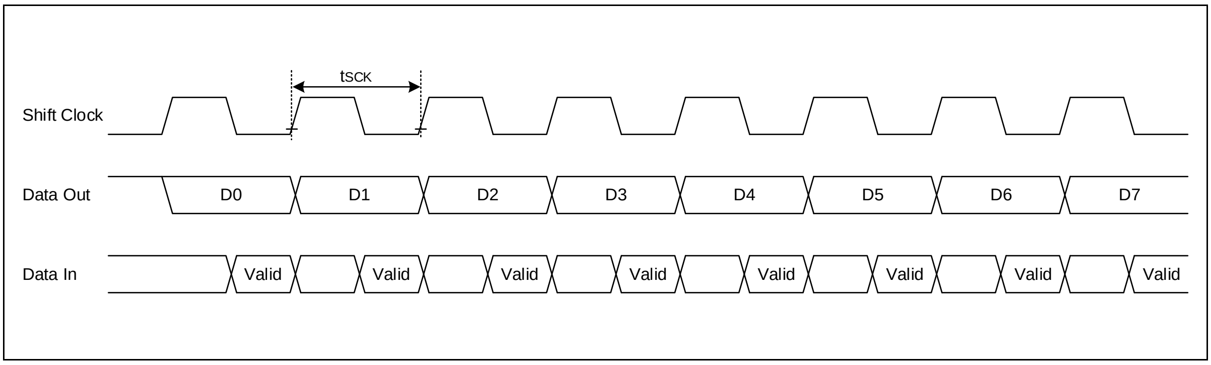


Figure 139. Timing Diagram of UART Module

NOTES:

1. tSCK : Board Rate

22.16 I2C characteristics

Table 107. Operating Condition of I2C

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V_{DD}	1.8	5.0	5.5	V
Operating temperature	T_A	-40	25	105	℃

Table 108. I2C Characteristics

Parameter	Symbol	Standard		Fast		Units
		Min	Max	Min	Max	
Clock frequency	tSCL	0	100	0	400	kHz
Clock high pulse width	tSCLH	4.0	—	0.6	—	us
clock low pulse width	tSCLL	4.7	—	1.3	—	
Bus free time	tBF	4.7	—	1.3	—	
Start condition setup time	tSTSU	4.7	—	0.6	—	
Start condition hold time	tSTHD	4.0	—	0.6	—	
Stop condition setup time	tSPSU	4.0	—	0.6	—	
Stop condition hold time	tSPHD	4.0	—	0.6	—	
Output valid from clock	tVD	0	—	0	—	
Data input hold time	tDIH	0	—	0	1.0	
Data input setup time	tDIS	250	—	100	—	ns

NOTE: The specifications of the parameters are guaranteed by design.

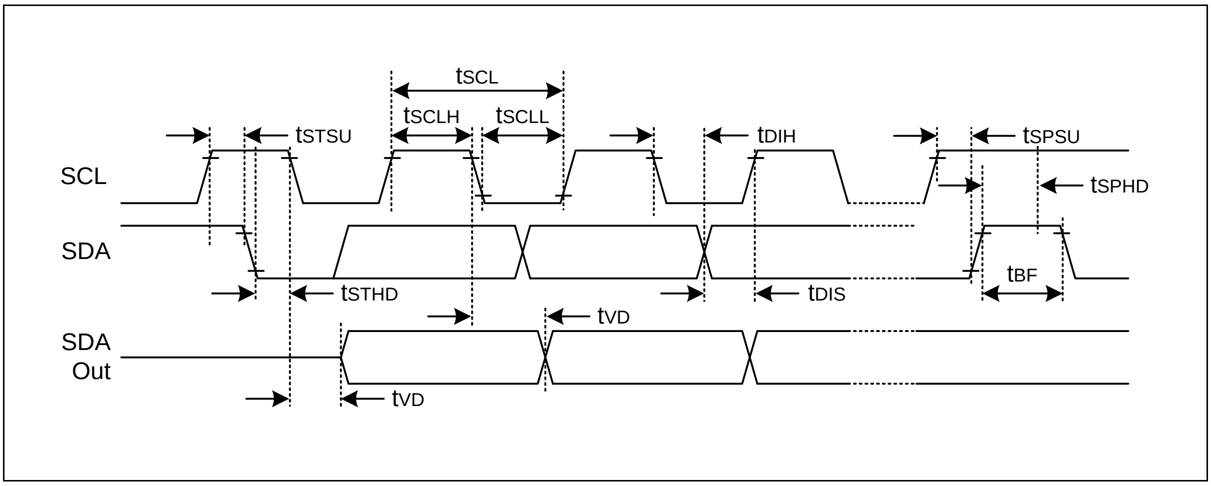


Figure 140. Timing Diagram of I2CTiming Characteristics

22.17 Internal code flash characteristics

Table 109. Operating Condition of Internal Code Flash

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V_{DD}	1.8	5.0	5.5	V
Operating temperature	T_A	-40	25	105	℃

Table 110. Internal Code Flash Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Max. available clock frequency	-	0-wait	—	—	32	MHz
Reset Cycle Time	fRSTBUSY	—	5.6	8	10.4	us
Fuse Program Cycle Time	fFRDBUSY	—	4.2	6	7.8	us
Normal Program Cycle Time	tPGMBUSY	—	21	30	42	us
Normal Page Erase Cycle Time	tPERSBUSY	—	2.8	4	5.2	ms
Sector Erase Cycle Time	tSERSBUSY	—	2.8	4	5.2	ms
Chip Erase Cycle Time	tMERSBUSY	—	5.6	8	10.4	ms
Endurance of write/erase	NFWE	TA=25 °C, Page unit	10,000	—	—	Times
Retention time	tFRT	—	10	—	—	Years

NOTE: The specifications of the parameters are guaranteed by design.

22.18 ADC characteristics

Table 111. Operating Condition of ADC

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V_{DD}	2.4	5.0	5.5	V
Operating temperature	T_A	-40	25	105	℃

NOTE: If 12-bit ADC uses voltage of less than 2.4V, measurement error may be big. To avoid this, it is recommended to use voltage ranging from 2.4V to 5.5V for the ADC which is used for precision sensing of analog voltage.

Table 112. ADC Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Resolution	—	—	—	—	12	Bit
Number of channel	—	—	—	15	—	CH
Analog input range	V_{IN}	$V_{AVREF}=V_{DD}$ $V_{SS}=V_{GND}$	VSS	—	AVREF	V
Operating current	I_{DD}	VDD = 5V	—	1	2—	mA
Standby current	I_{ST}	—	—	20	1500	nA
Differential nonlinearity	DNL	—	—	±1	±4	LSB
Integral nonlinearity	INL	T_A = 25 °C	—	±4	±10	LSB
Top offset error (FSE)	TOE	—	—	±6	±12	LSB
Zero offset error	ZOE	—	—	±4	±8	LSB
Operating frequency	ACLK	—	—	—	4.5	MHz
Conversion frequency	f_{CONV}		—	—	150	Ksps

NOTE: The specifications of the parameters are guaranteed by design.

22.19 LCD Driver characteristics

Table 113. Operating Condition of LCD Driver

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V_{DD}	2.7	5.0	5.5	V
Operating temperature	T_A	-40	25	105	℃

Table 114. Comparator Characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
LCD voltage	VLC0	LCD contrast = DISABLED, 1/4 bias	—	—	—	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 00H	Typ.x0.94	V_{DD}x16/31	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 01H	Typ.x0.94	V_{DD}x16/30	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 02H	Typ.x0.94	V_{DD}x16/29	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 03H	Typ.x0.94	V_{DD}x16/28	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 04H	Typ.x0.94	V_{DD}x16/27	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 05H	Typ.x0.94	V_{DD}x16/26	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 06H	Typ.x0.94	V_{DD}x16/25	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 07H	Typ.x0.94	V_{DD}x16/24	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 08H	Typ.x0.94	V_{DD}x16/23	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 09H	Typ.x0.94	V_{DD}x16/22	Typ.x1.06	V

Table 115. Comparator Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
LCD voltage	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0AH	Typ.x0.94	V_{DD}x16/21	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0BH	Typ.x0.94	V_{DD}x16/20	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0CH	Typ.x0.94	V_{DD}x16/19	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0DH	Typ.x0.94	V_{DD}x16/18	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0EH	Typ.x0.94	V_{DD}x16/17	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0FH	Typ.x0.94	V_{DD}x16/16	Typ.x1.06	V
LCD mid bias voltage^{NOTE 2}	VLC1	V_{DD} = 2.7V to 5.5V, LCD clock = 0Hz, 1/4 bias, No panel load	Typ-0.2	3/4xVLC0	Typ+0.2	V
	VLC2		Typ-0.2	2/4xVLC0	Typ+0.2	
	VLC3		Typ-0.2	1/4xVLC0	Typ+0.2	
LCD Driver output impedance	RLO	VLCD=3.0V	–	5	10	kΩ
LCD bias dividing resistor	RLCD1	1/4 bias, T_A = 25°C	7.5	10	12.5	kΩ
	RLCD2		38	50	62	
	RLCD3		60	80	100	
	RLCD4		180	240	300	

NOTES:

1. The specifications of the parameters are guaranteed by design.
2. It is middle output voltage when the VDD and the VLC0 node are connected.

22.20 Touch sensing characteristics

Table 115. Operating Condition of Touch Sensing

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V_{DD}	2.7	5.0	5.5	V
Operating temperature	T_A	-40	25	85	℃
VDD RIPPLE NOTE	V_{R_5V}	-	-	±100	mV
	$V_{R\_3.3V}$	-	-	±100	mV

NOTE: The above values are experimental data and depend on the test conditions. (sensitivity, cover, board...)
- Test with A31T216 Start Kit Shield board. (9pi Touch stick Sensitivity on 2T Acrylic Cover)

Table 116. Touch Sensing Characteristics

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
Load capacitance	Cload	-	—	50	100	pF
Operating frequency	Fop	Cload=50pF(@typ.) Cload=100pF(@min.)	2	4	4	MHz
High-sense voltage	V_{HS}	VDD=5V	2.6	3.5	5	V
COMP reference voltage	V_{COM}	VDD=5V	2.6	3	3.5	V

NOTE: The specifications of the parameters are guaranteed by design.

22.21 Operating voltage range

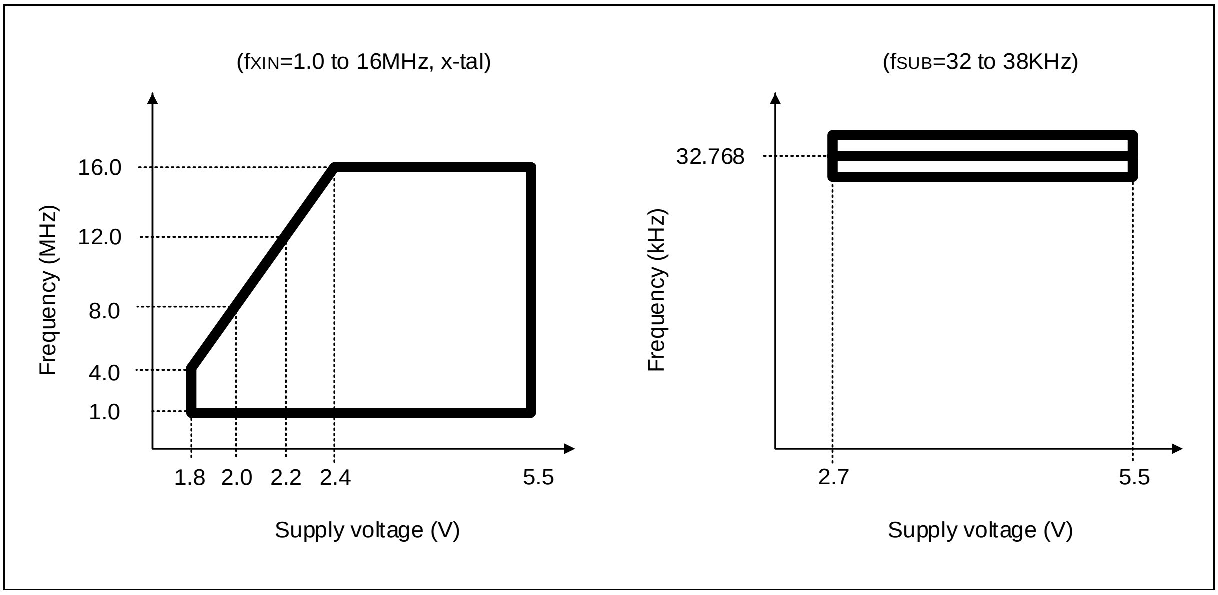
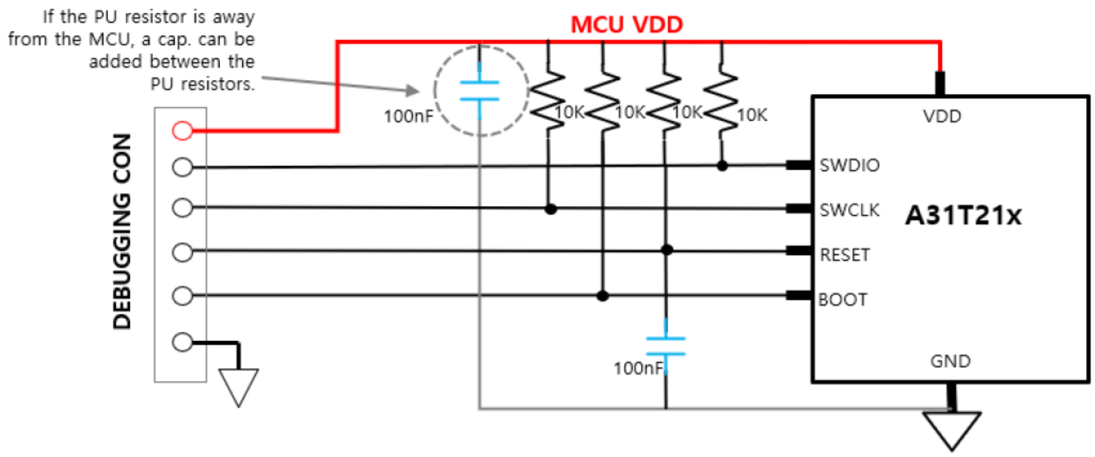


Figure 141. Operating Voltage Range

22.22 Circuit design guide

Figure 142 shows a recommended circuit design.



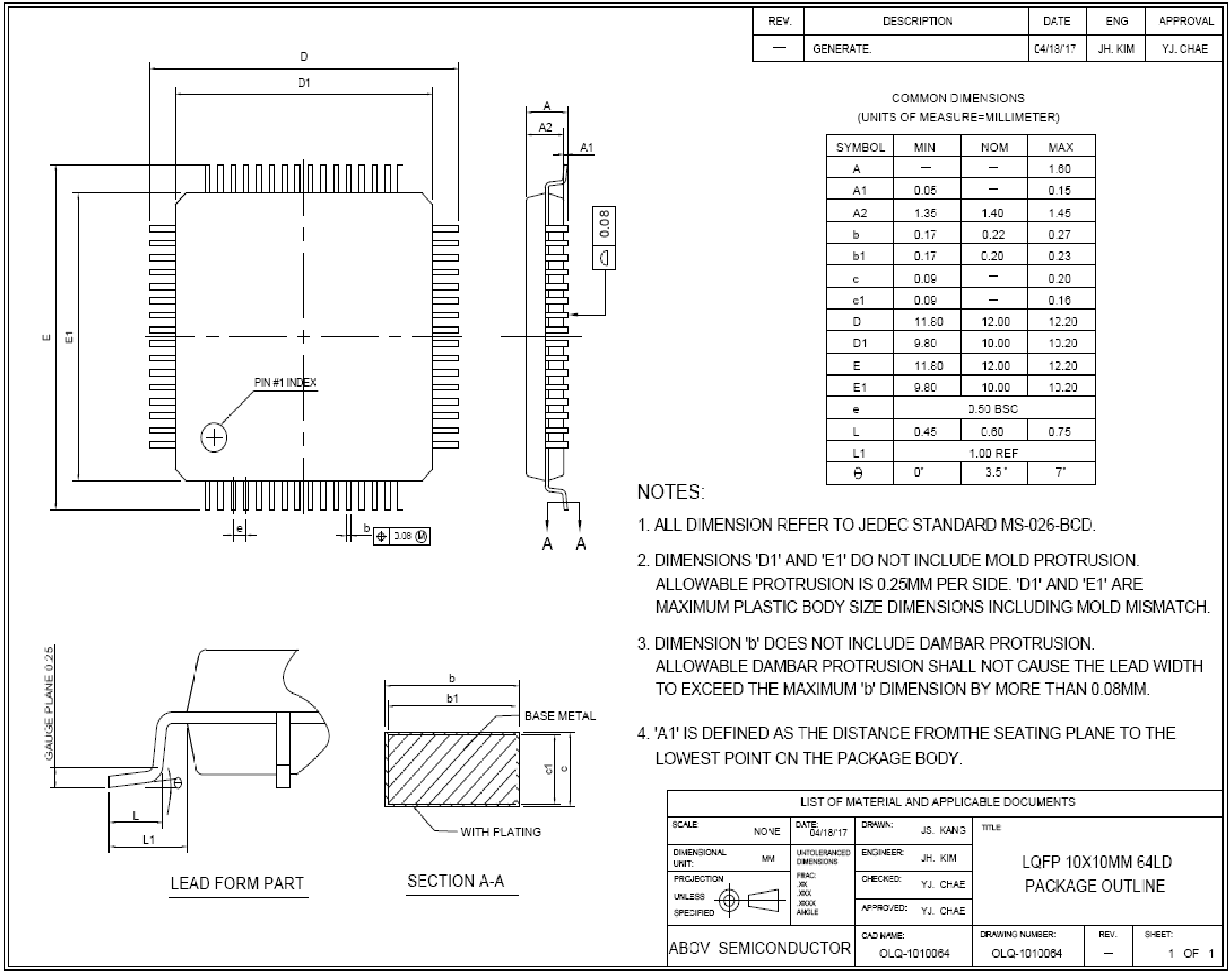
If the PU resistor is away from the MCU, a cap. can be added between the PU resistors.

Figure 142. Circuit Design Guide for On-Board Programming

23 Package information

This chapter provides A31T214/216 series package information.

23.1 64 LQFP package information



REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/18/17	JH. KIM	YJ. CHAE

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16
D	11.80	12.00	12.20
D1	9.80	10.00	10.20
E	11.80	12.00	12.20
E1	9.80	10.00	10.20
e		0.50 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

NOTES:

1. ALL DIMENSION REFER TO JEDEC STANDARD MS-026-BCD.
2. DIMENSIONS 'D1' AND 'E1' DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. 'D1' AND 'E1' ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 'b' DIMENSION BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROMTHE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

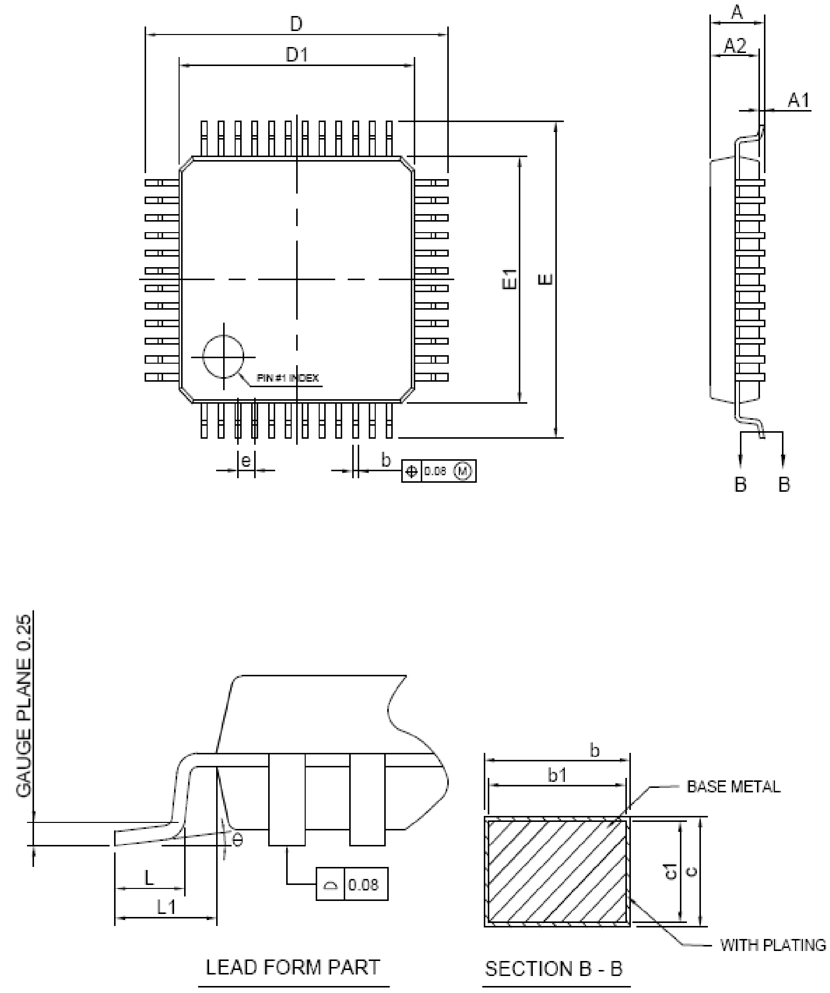
LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE: 04/18/17	DRAWN: JS. KANG	TITLE LQFP 10X10MM 64LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS	ENGINEER: JH. KIM	
PROJECTION UNLESS SPECIFIED	FRAC: .XX .XXX .XXXX ANGLE	CHECKED: YJ. CHAE	
		APPROVED: YJ. CHAE	
ABOV SEMICONDUCTOR	CAD NAME: OLQ-1010064	DRAWING NUMBER: OLQ-1010064	REV. — SHEET: 1 OF 1

Figure 143. 64 LQFP Package Dimension

23.2 48 LQFP package information

REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/18/'17	JH. KIM	YJ. CHAE



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026-BBC.
2. DIMENSION 'D1' AND 'E1' DO NOT INCLDUE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. 'D1' AND 'E1' ARE MAXIMUM PLASTIC BODY DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMABR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 'b' DIMENSION BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

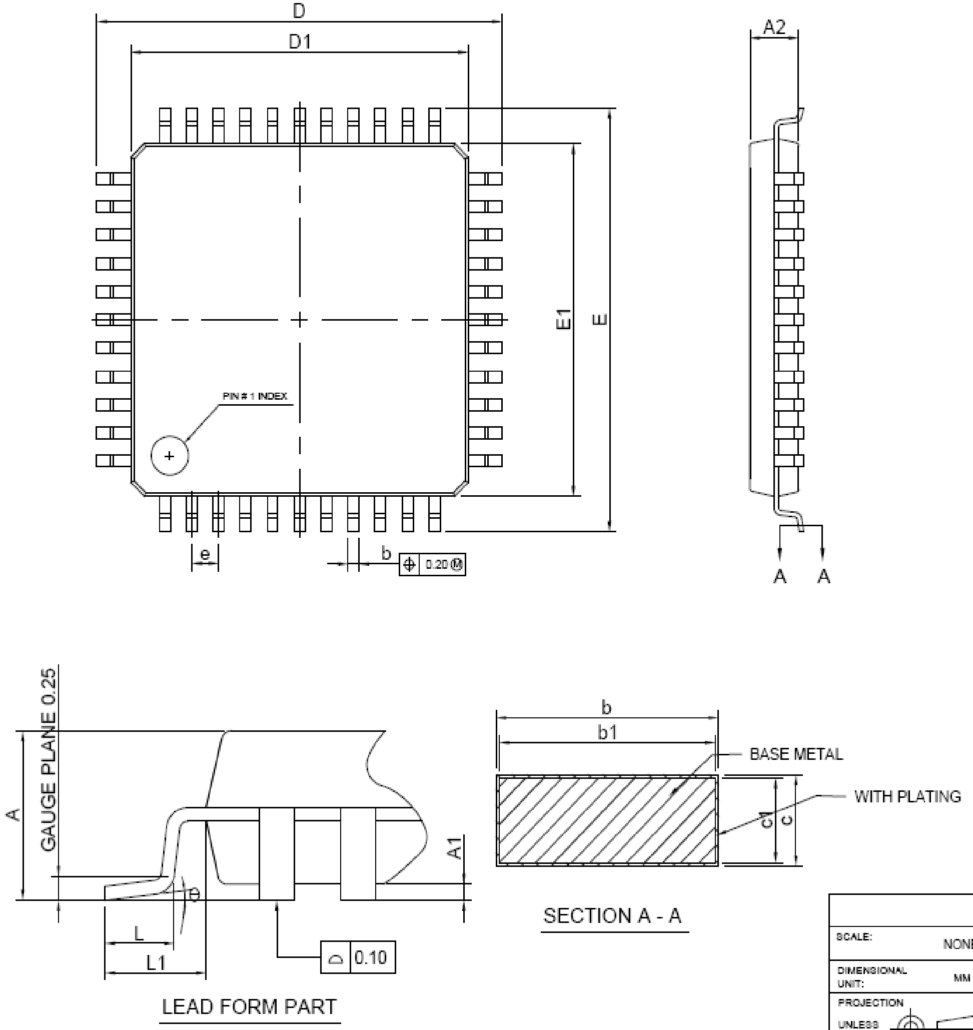
LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE:	DRAWN: JS. KANG	TITLE: LQFP 7X7MM 48LD PACKAGE OUTLINE	
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS FRAC: .XX .XXX .XXXX ANGLE	ENGINEER: YJ. CHAE		
PROJECTION UNLESS SPECIFIED		CHECKED: YJ. CHAE		
		APPROVED: JH. KIM		
ABOV SEMICONDUCTOR		CAD NAME: OLQ-0707048	DRAWING NUMBER: OLQ-0707048	REV.: — SHEET: 1 OF 1

Figure 144. 48 LQFP Package Dimension

23.3 44 LQFP package information

REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/18/'17	JH. KIM	YJ. CHAE



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.22	0.37	0.45
b1	0.22	0.35	0.40
c	0.09	—	0.20
c1	0.09	—	0.16
D	11.80	12.00	12.20
D1	9.80	10.00	10.20
E	11.80	12.00	12.20
E1	9.80	10.00	10.20
e	0.80 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	8°

NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026-BCB.
2. DIMENSIONS 'D1' AND 'E1' DON NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. 'D1' AND 'E1' ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 'b' DIMENSION BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PAKCAGE BODY.

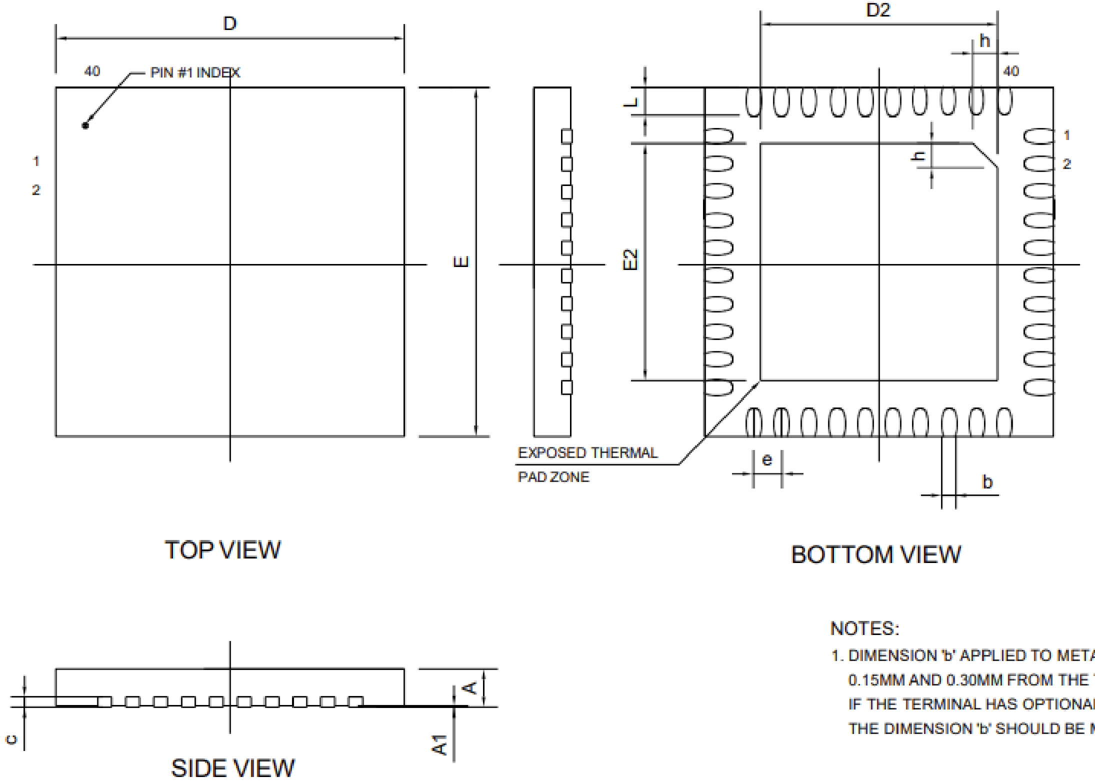
LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE: 04/18/'17	DRAWN: JS. KANG	TITLE: LQFP 10X10MM 44LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS	ENGINEER: JH. KIM	
PROJECTION UNLESS SPECIFIED	FRAC: .XX .XXX .XXXX ANGLE	CHECKED: YJ. CHAE	
		APPROVED: YJ. CHAE	
ABOV SEMICONDUCTOR	CAD NAME: OLQ-1010044	DRAWING NUMBER: OLQ-1010044	REV.: — SHEET: 1 OF 1

Figure 145. 44 LQFP Package Dimension

23.4 40 QFN package information

REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	10/20/'22	MK. PARK	SB. PARK



COMMON DIMENSIONS
(UNITS OF MEASURE=MM)

SYMBOL	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	–	0.02	0.05
b	0.18	0.25	0.30
c	0.150 REF		
D	5.90	6.00	6.10
D2	4.50	4.60	4.70
e	0.50 BSC		
E	5.90	6.00	6.10
E2	4.50	4.60	4.70
L	0.30	0.40	0.50
h	0.30	0.35	0.40

NOTES:

1. DIMENSION 'b' APPLIED TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TEMINAL, THE DIMENSION 'b' SHOULD BE MEASURED IN THAT RADIUS AREA.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE: 10/20/'21	DRAWN: MK. PARK	TITLE: QFN 6X6MM 40LD 0.6T PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS FRAC: .XX .XXX .XXXX ANGLE	ENGINEER: MK. PARK	
PROJECTION UNLESS SPECIFIED		CHECKED: SB. PARK	
		APPROVED: SB. PARK	
ABOV SEMICONDUCTOR		CAD NAME: OQN-06060406	DRAWING NUMBER: OQN-06060406 · REV. — · SHEET: 1 OF 1

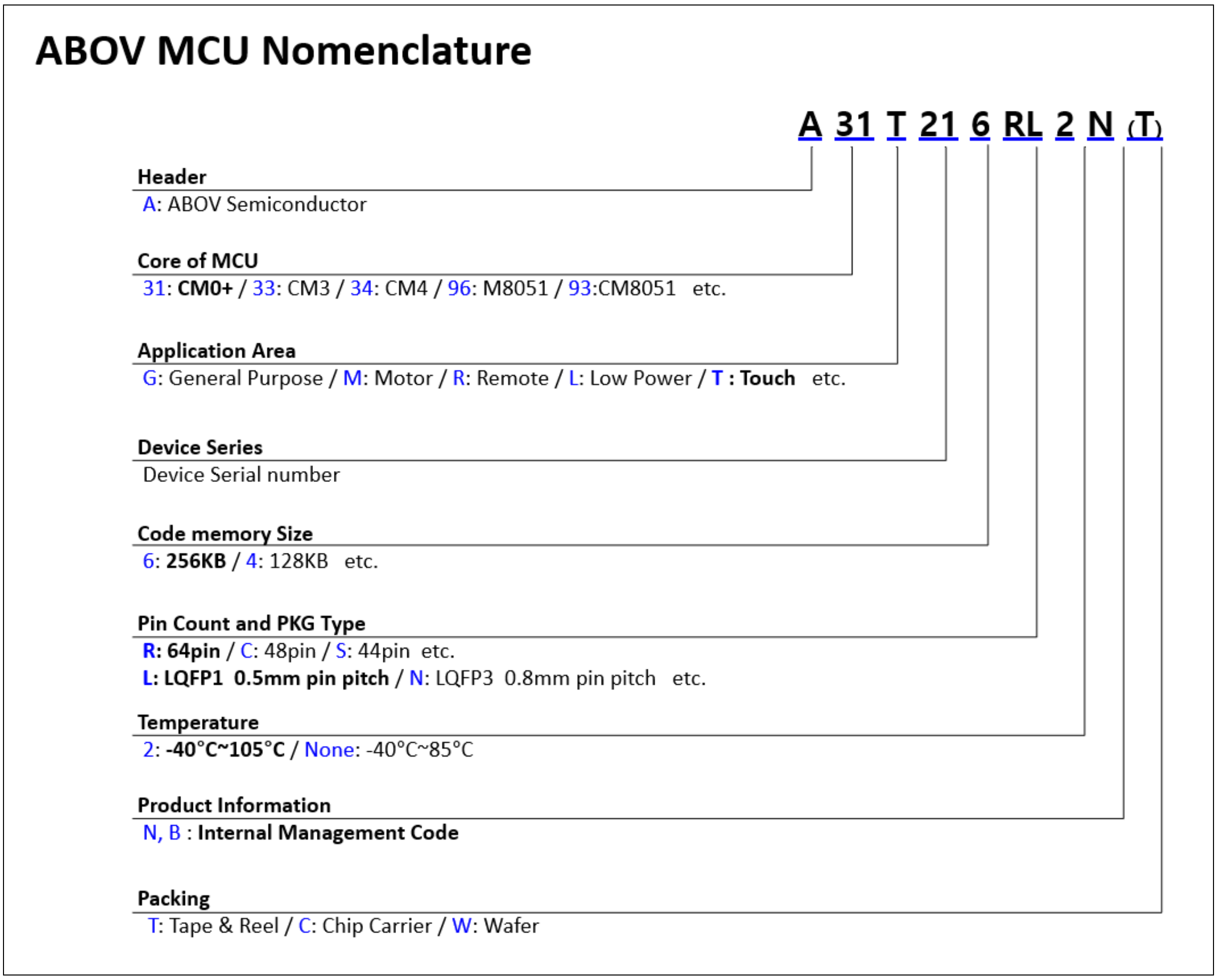
Figure 146. 40 QFN Package Dimension

24 Ordering information

Table 117. A31T214/216 Device Ordering Information

Device name	Flash	SRAM	SPI	USART	I2C	Timer	PWM	ADC	I/O ports	Op. Temp.[℃]	Package
A31T216RLN	256KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	15-ch	60	-40~85	64-LQFP
A31T216CLN	256KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	11-ch	44	-40~85	48-LQFP
A31T216SNN	256KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	9-ch	40	-40~85	44-LQFP
A31T214RLN	128KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	15-ch	60	-40~85	64-LQFP
A31T214CLN	128KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	11-ch	44	-40~85	48-LQFP
A31T214SNN	128KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	9-ch	40	-40~85	44-LQFP
A31T214IUN	128KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	9-ch	38	-40~85	40-QFN
A31T216RL2N*	256KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	15-ch	60	-40~105	64-LQFP
A31T216CL2N*	256KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	11-ch	44	-40~105	48-LQFP
A31T216SN2N*	256KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	9-ch	40	-40~105	44-LQFP
A31T214RL2N*	128KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	15-ch	60	-40~105	64-LQFP
A31T214CL2N*	128KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	11-ch	44	-40~105	48-LQFP
A31T214SN2N*	128KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	9-ch	40	-40~105	44-LQFP
A31T214IU2N	128KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	9-ch	38	-40~105	40-QFN

* For available options or further information on the devices with "*" marks, please contact the ABOV sales offices.



ABOV MCU Nomenclature

A 31 T 21 6 RL 2 N (T)

Header
A: ABOV Semiconductor

Core of MCU
31: **CM0+** / 33: CM3 / 34: CM4 / 96: M8051 / 93:CM8051 etc.

Application Area
G: General Purpose / M: Motor / R: Remote / L: Low Power / **T : Touch** etc.

Device Series
Device Serial number

Code memory Size
6: **256KB** / 4: 128KB etc.

Pin Count and PKG Type
R: 64pin / C: 48pin / S: 44pin etc.
L: LQFP1 0.5mm pin pitch / N: LQFP3 0.8mm pin pitch etc.

Temperature
2: **-40°C~105°C** / None: -40°C~85°C

Product Information
N, B : **Internal Management Code**

Packing
T: Tape & Reel / C: Chip Carrier / W: Wafer

Figure 147. A31T214/216 Device Numbering Nomenclature

25 Development tools

This chapter introduces wide range of development tools for A31T214/216. ABOV offers software tools, debuggers, and programmers to help a user in generating right results to match target applications. ABOV supports entire development ecosystem of the customers.

25.1 Compiler

ABOV semiconductor does not provide any compiler for A31T214/216. However, since A31T214/216 have ARM's high-speed 32-bit Cortex-M0+ Cores for their CPU, you can use all kinds of third party's standard compiler such as Keil C Compiler. These compilers' output debug information can be integrated with our A-Link and A-Link Pro. Please visit our website www.abovsemi.com for more information regarding the A-Link and A-Link Pro.

25.2 Debugger

The A-Link and A-Link Pro support ABOV Semiconductor's A31T214/216 MCU emulation in SWD Interface. The A-Link and A-Link Pro use two wires interfacing between PC and MCU, which is attached to user's system. The A-Link and A-Link Pro can read or change the value of MCU's internal memory and I/O peripherals. In addition, the A-Link and A-Link Pro control MCU's internal debugging logic. This means A-Link and A-Link Pro control emulation, step run, monitoring and many more functions regarding debugging.

The A-Link and A-Link Pro run underneath MS operating system such as MS-Windows NT/ 2000/ XP/ Vista/ 7/ 8/ 8.1/ 10 (32-bit, 64-bit).

Programming information using the A-Link and A-Link Pro are provided in Figure 148. More detailed information about the A-Link and A-Link Pro, please visit our website www.abovsemi.com and download the debugger S/W and documents.

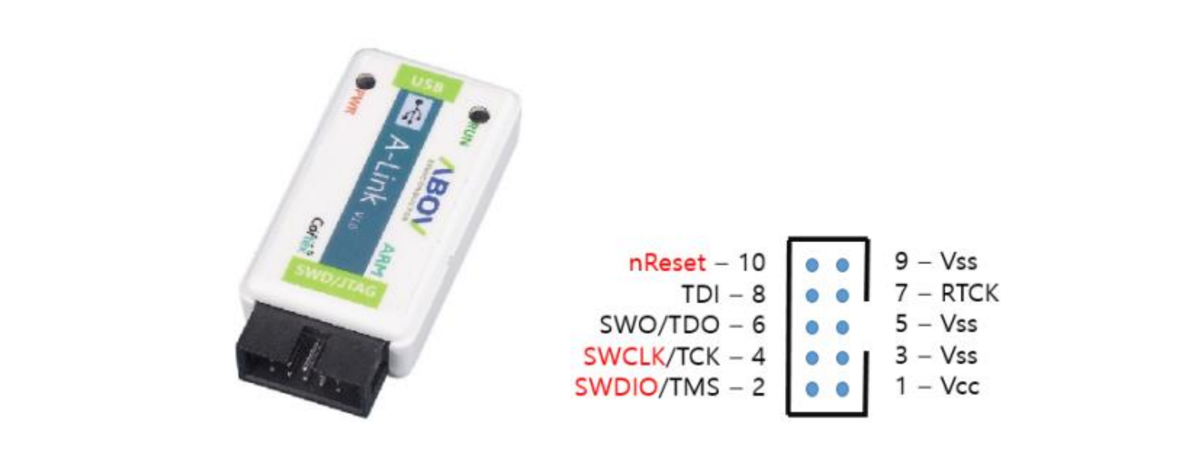


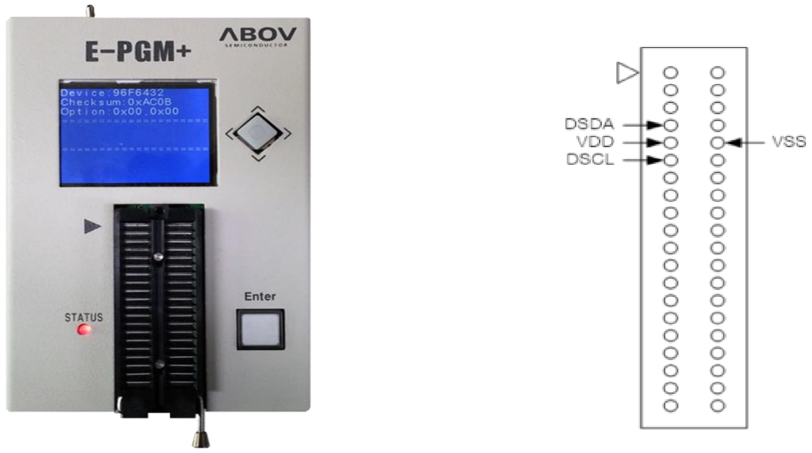
Figure 148. A-Link and Pin Descriptions

25.3 Programmer

25.3.1 E-PGM+

E-PGM+ is a single programmer, and allows a user to program on the device directly.

- Support ABOV devices
- 2 to 5 times faster than S-PGM+
- Main controller: 32-bit MCU @ 72MHz
- Buffer memory: 1MB



DSDA : SWDIO, DSCL: SWCLK

Figure 149. E-PGM+ (Single Writer) and Pin Descriptions

25.3.2 Gang programmer

E-Gang4 and E-Gang6 allows a user to program on multiple devices at a time. They run not only in PC controlled mode but also in standalone mode without PC control. USB interface is available and it is easy to connect to the handler.

Figure 150. E-Gang4 and E-Gang6 (for Mass Production)

Revision history

Revision	Date	Notes
1.00	2021-10-28	Document Created
1.01	2021-11-25	1. Add note about deepsleep wakeup clock source of WT and WDT. (SCU_WUER, SCU_PPCLKSR) 2. Modify LCD block diagram and LCD_CR register description.
1.02	2022-01-24	1. Modified The start-up time of HSE Characteristics from Typ. 200 ms to Typ. 2 ms. 2. Modified Stabilization time of HSI characteristics from Max. 100 us to Min. 100 us. 3. Added the notifications to Figure 112 and 19.2.4 4. Updated the notifications of 18.2.15
1.03	2022-05-30	Modified incorrect device name.
1.04	2022-06-28	Added note in Figure 117. Internal Resistor Bias Connection in LCD. Modified t_{IWH}, t_{IWL} specs in Figure 136. Timing Diagram of External Input AC Characteristics Definitions. Added subtitle 5.4.1 External Interrupt.
1.05	2022-07-15	Updated Table <Operating Condition of Touch Sensing>.
1.06	2022-12-12	Updated font style of this document Changed LED COM / SEG notation. (Change to ICOM/ISEG) Added 40-QFN Package information. Changed LCD COM / SEG notation.
1.07	2023-01-17	Contents 5.3.14 Pn_ICR: port n interrupt control register The falling edge is displayed incorrectly and the rising edge is changed.
1.08	2023-02-15	Contents 22.15 USART UART timing characteristics Remove unnecessary content and information in the USART/UART part Add Bookmarks
1.09	2023-03-15	Contents 23.4 40 QFN package information Incorrect content has been corrected in the Package Description section.
1.10	2023-05-12	Contents 5.3.1 Pn_MOD: port n mode register Added Reserved status description because there is no content for Port Setup Status Reserved

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