
**16 MHz 8-bit MCU, 16 KB Flash Memory,
12-bit ADC, 3 Timers, USART, I2C, High Current Port**

Datasheet Version 1.18

Features**Core**

- 8-bit CISC M8051 core

16 Kbytes On-Chip FLASH

- Endurance : 30,000 times
- In-System Programming (ISP)

256 bytes IRAM / 512 bytes XRAM**General Purpose I/O (GPIO)**

- Normal I/O: max 30 ports
- High sink current port: max 8 ports

Timer/counter

- Basic Interval Timer (BIT)
- Watch Timer (WT)
- Window Watch Dog Timer (WDT)
- 8-bit × 1-ch (T0)
- 16-bit × 2-ch (T1/T2)

Programmable pulse generation

- Pulse generation (by T0/T1/T2)
- 16-bit complement PWM (dead time control)

I2C

- 8-bit x 1-ch

USART0/1 (UART + SPI)

- 8-bit USART × 2-ch or 8-bit SPI × 2-ch
- Receiver Time Out(RTO)
- 0% Error Baud Rate

12-bit A/D Converter

- 15 External Input channels
- 1-Channel for internal reference voltage

Power-on Reset

- Reset release level (1.32V)

Low Voltage Reset

- 16 levels detect

Low Voltage Indicator

- 13 levels detect

Interrupt Sources

- EINT0 to 4, EINT5, EINT6, EINT7 to A, EINT10, EINT11, EINT12 (7)
- Timer (0/1/2) (3)
- WDT (1)
- BIT (1)
- WT (1)

- USART RX/TX (4)

- I2C (1)
- ADC (1)
- CRC (1)
- LVI (1)

Internal RC Oscillator

- HSI 32MHz ±1.5% (TA= 0~ +50°C)
- HSI 32MHz ±2.0% (TA= -10~ +70°C)
- HSI 32MHz ±2.5% (TA= -40~ +85°C)
- HSI 32MHz ±5.0% (TA= -40~ +105°C)
- LSI 128kHz ±20% (TA= -40~ +85°C)
- LSI 128kHz ±30% (TA= -40~ +105°C)

Power down mode

- STOP, IDLE mode

Operating voltage and frequency

- 1.8V to 5.5V (@32.768kHz crystal)
- 2.2V to 5.5V (@4MHz to 10MHz with crystal)
- 2.4V to 5.5V (@4MHz to 12MHz with crystal)
- 1.8V to 5.5V (@0.5MHz to 16MHz with internal RC)

Minimum Instruction Execution Time

- 125ns (@16MHz main clock)
- 61us (@32.768kHz sub clock)

Operating temperature

- -40°C to +85°C, -40°C to +105°C

Packages

- 32 LQFP
- 28 TSSOP/SOP
- 24 QFN
- 20 TSSOP/SOP
- 16 SOPN
- Pb-free package

16 MHz 8-bit MCU, 16 KB Flash Memory,
12-bit ADC, 3 Timers, USART, I2C, High Current Port

Datasheet Version 1.18

Product selection table

Table 1. Device Summary

| Part number | FLASH | XRAM | IRAM | Timer (PWM) | Communication function | | ADC 12-bit (Channel) | GPIO | High current port | Package | Temperature Range |
|-------------|-------|-----------|----------|-------------|------------------------|----------|----------------------|------|-------------------|-----------|-------------------|
| | | | | | USART | I2C | | | | | |
| A96G166KN | 16KB | 512 bytes | 256bytes | 3 | 2 | 1 | 15 inputs | 30 | 8 | 32 LQFP | -40°C~+85°C |
| A96G166GD | | | | 3 | 2 | 1 | 12 inputs | 26 | 8 | 28 SOP | |
| A96G166GR | | | | 3 | 2 | 1 | 12 inputs | 26 | 8 | 28 TSSOP | |
| A96G166LU* | | | | 3 | 2 | 1 | 11 inputs | 22 | 4 | 24 QFN | |
| A96G166FD | | | | 3 | 1 | 1 | 8 inputs | 18 | 4 | 20 SOP | |
| A96A166FD | | | | 3 | 2 | 1 | 10 inputs | 18 | 2 | 20 SOP | |
| A96G166FR | | | | 3 | 1 | 1 | 8 inputs | 18 | 4 | 20 TSSOP | |
| A96S166FR* | | | | 3 | 1 | 1 | 8 inputs | 18 | 4 | 20 TSSOP | |
| A96G166AE* | | | | 3 | 2 | 1 | 7 inputs | 14 | 3 | 16 SOPN | |
| A96G166KN2 | | | | 16KB | 512 bytes | 256bytes | 3 | 2 | 1 | 15 inputs | |
| A96G166GD2 | 3 | 2 | 1 | | | | 12 inputs | 26 | 8 | 28 SOP | |
| A96G166GR2 | 3 | 2 | 1 | | | | 12 inputs | 26 | 8 | 28 TSSOP | |
| A96G166LU2* | 3 | 2 | 1 | | | | 11 inputs | 22 | 4 | 24 QFN | |
| A96G166FD2 | 3 | 1 | 1 | | | | 8 inputs | 18 | 4 | 20 SOP | |
| A96A166FD2 | 3 | 2 | 1 | | | | 10 inputs | 18 | 2 | 20 SOP | |
| A96G166FR2 | 3 | 1 | 1 | | | | 8 inputs | 18 | 4 | 20 TSSOP | |
| A96S166FR2* | 3 | 1 | 1 | | | | 8 inputs | 18 | 4 | 20 TSSOP | |
| A96G166AE* | 3 | 2 | 1 | | | | 7 inputs | 14 | 3 | 16 SOPN | |

* For available options or further information on the devices with "*" marks, please contact [the ABOV sales offices](#).

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1 Description

A96G166/A96A166/A96S166 is an advanced CMOS 8-bit microcontroller with 16Kbytes of FLASH. This is a powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications.

1.1 Device overview

In this section, features of A96G166/A96A166/A96S166 and peripheral counts are introduced.

Table 2. A96G166/A96A166/A96S166 Device Features and Peripheral Counts

| Peripherals | | Description |
|------------------------------------|----------------------|---|
| Core | CPU | 8-bit CISC core (M8051, 2 clocks per cycle) |
| | Interrupt | Up to 21 peripheral interrupts supported. <ul style="list-style-type: none"> EINT0 to 4, EINT5, EINT6, EINT7 to A, EINT10, EINT11, EINT12 (7) Timer (0/1/2) (3) WDT (1) BIT (1) WT (1) USART *Rx/Tx (4) I2C (1) ADC (1) CRC (1) LVI (1) |
| Memory | ROM (FLASH) capacity | <ul style="list-style-type: none"> 16 Kbytes FLASH with self-read and write capability In-system programming (ISP) Endurance: 30,000times |
| | IRAM | 256Bytes |
| | XRAM | 512Bytes |
| Programmable pulse generation | | <ul style="list-style-type: none"> Pulse generation (by T0/T1/T2) 16-bit Complement PWM (Dead time control) |
| Buzzer | | 8-bit × 1-ch |
| Minimum instruction execution time | | <ul style="list-style-type: none"> 125ns (@ 16MHz main clock) 61us (@ 32.768kHz sub clock) |
| Power down mode | | <ul style="list-style-type: none"> STOP mode IDLE mode |

Table 2. A96G166/A96A166/A96S166 Device Features and Peripheral Counts (continued)

| Peripherals | | Description |
|---------------------------------|-------------------|--|
| General Purpose I/O (GPIO) | | <ul style="list-style-type: none"> Normal I/O: Max 30 ports High sink current port: LED 8 x COM |
| Reset | Power on reset | Reset release level: 1.32V |
| | Low voltage reset | <ul style="list-style-type: none"> 16 levels detect 1.61/1.68/1.77/1.88/2.00/2.13/2.28/2.46/2.68/2.81/3.06/3.21/3.56/3.73/3.91/4.25V |
| Low voltage indicator | | <ul style="list-style-type: none"> 13 levels detect 1.88/2.00/2.13/2.28/2.46/2.68/2.81/3.06/3.21/3.56/3.73/3.91/4.25V |
| Watch Timer (WT) | | 3.91ms/0.25s/0.5s/1s/1min interval at 32.768kHz |
| Timer/counter | | <ul style="list-style-type: none"> Basic interval timer (BIT) 8-bit x 1-ch. Watchdog timer (WDT) 8-bit x 1-ch. 8-bit x 1-ch (T0), 16-bit x 2-ch (T1/T2) |
| Communication function | USART (UART+SPI) | <ul style="list-style-type: none"> 8-bit USART x 2-ch or 8-bit SPI x 2-ch Receiver timer out (RTO) 0% error baud rate |
| | I2C | <ul style="list-style-type: none"> 8-bit I2C x 1-ch |
| 12-bit A/D converter | | 15 input channels |
| Oscillator type | | <ul style="list-style-type: none"> 4MHz to 12MHz crystal or ceramic for main clock 32.768kHz Crystal for sub clock |
| Internal RC oscillator | | <ul style="list-style-type: none"> HSI 32MHz $\pm 3.0\%$ ($T_A = -40$ to $+85^\circ\text{C}$) HSI 32MHz $\pm 5.0\%$ ($T_A = -40$ to $+105^\circ\text{C}$) LSI 128kHz $\pm 20\%$ ($T_A = -40$ to $+85^\circ\text{C}$) LSI 128kHz $\pm 30\%$ ($T_A = -40$ to $+105^\circ\text{C}$) |
| Operating voltage and frequency | | <ul style="list-style-type: none"> 1.8V to 5.5V @ 32.768kHz with crystal 2.2V to 5.5V @ 4MHz to 10MHz with crystal 2.4V to 5.5V @ 4MHz to 12MHz with crystal 1.8V to 5.5V @ 0.5MHz to 16.0MHz with internal RC |
| Operating temperature | | -40°C to +85°C, -40°C to +105°C |
| Package | | <ul style="list-style-type: none"> Pb-free packages 32 LQFP 28 TSSOP / SOP 24 QFN 20 TSSOP / SOP |

1.2 A96G166/A96A166/A96S166 block diagram

In this section, A96G166/A96A166/A96S166 device with peripherals are described in a block diagram.

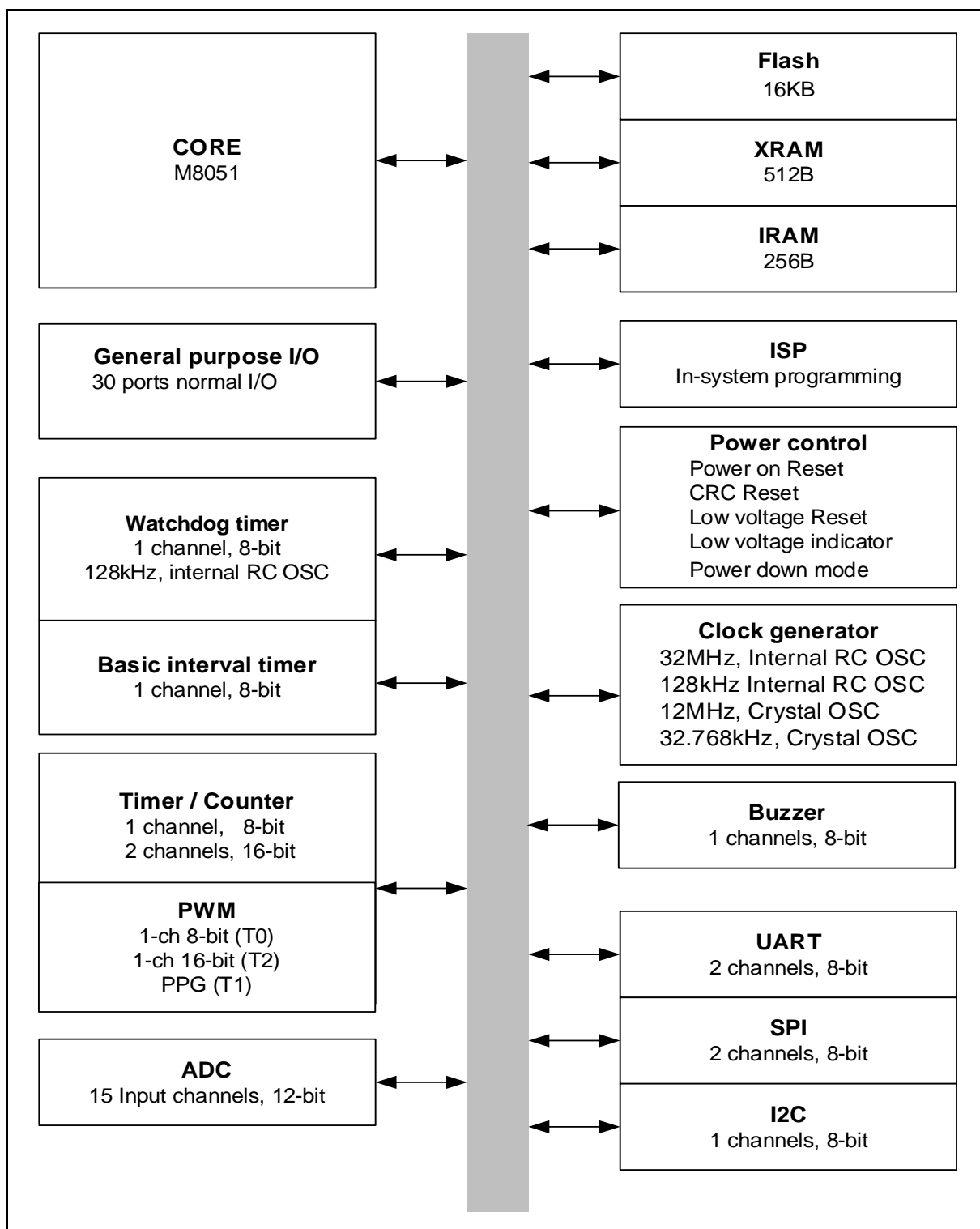


Figure 1. A96G166/A96A166/A96S166 Block Diagram

2 Pinouts and pin description

In this chapter, A96G166/A96A166/A96S166 device pinouts and pin descriptions are introduced.

2.1 Pinouts

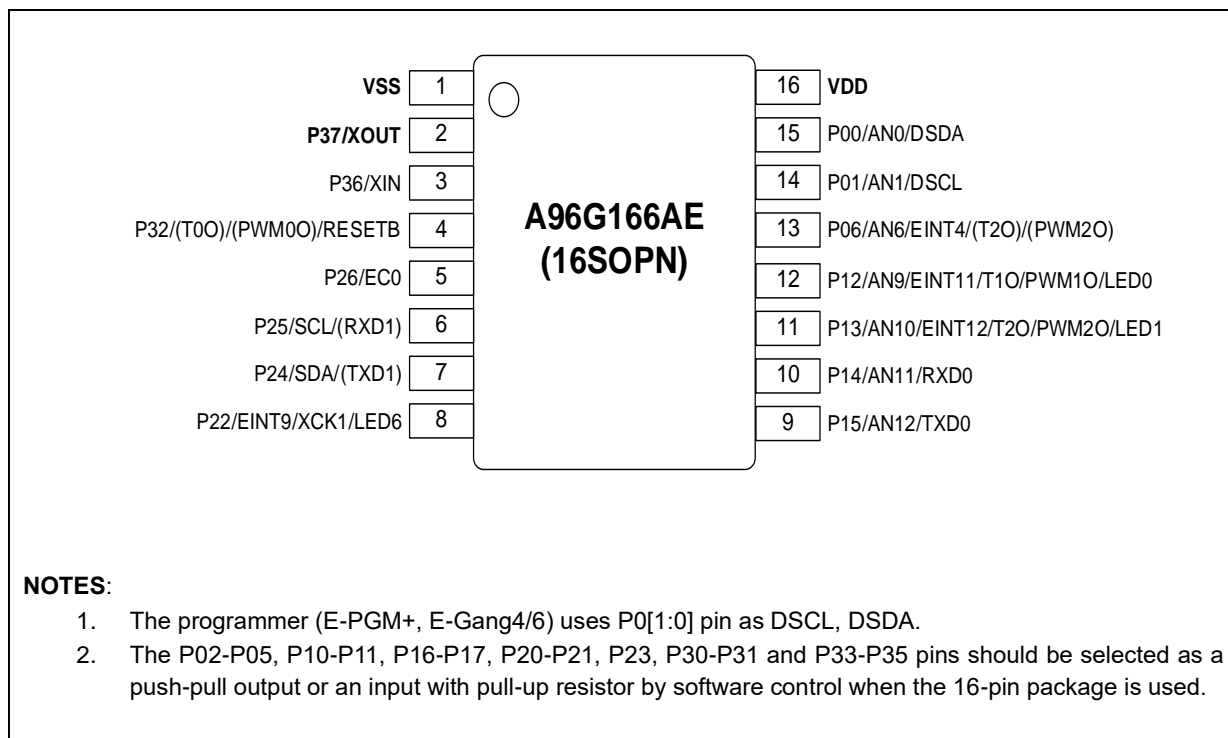


Figure 2 A96G166 16SOPN Pin Assignment

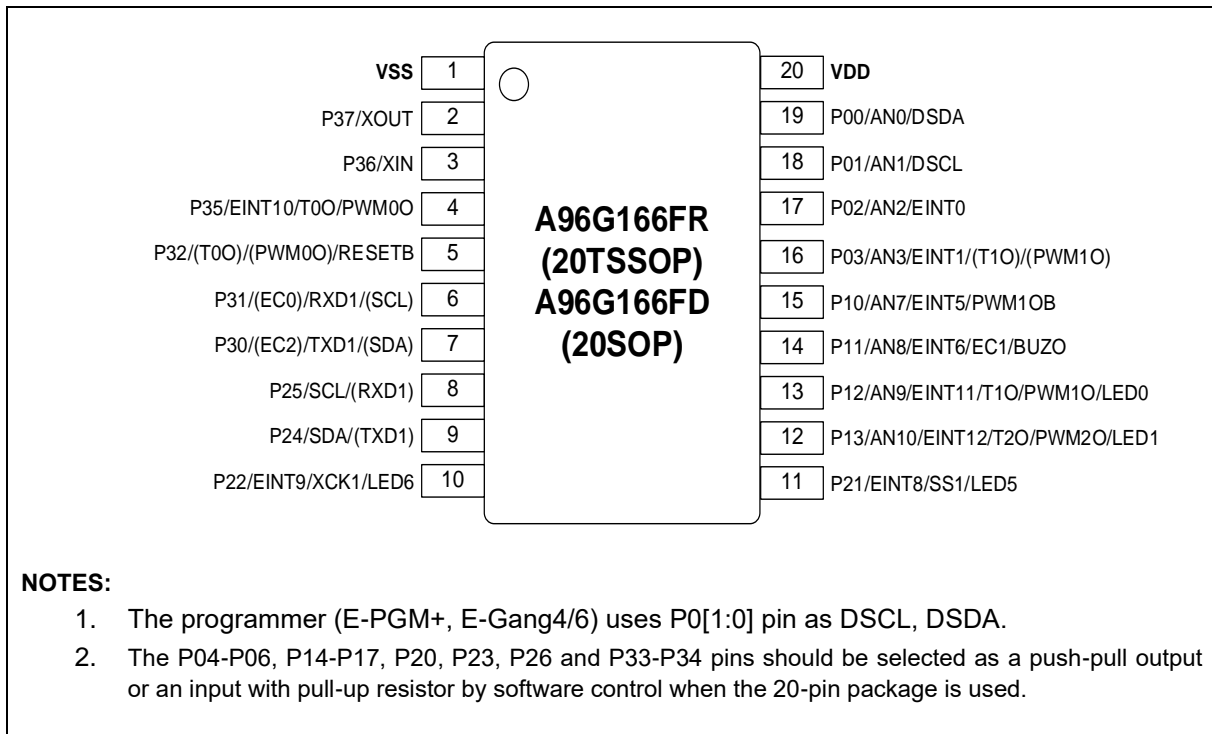


Figure 3. A96G166 20TSSOP/20SOP Pin Assignment

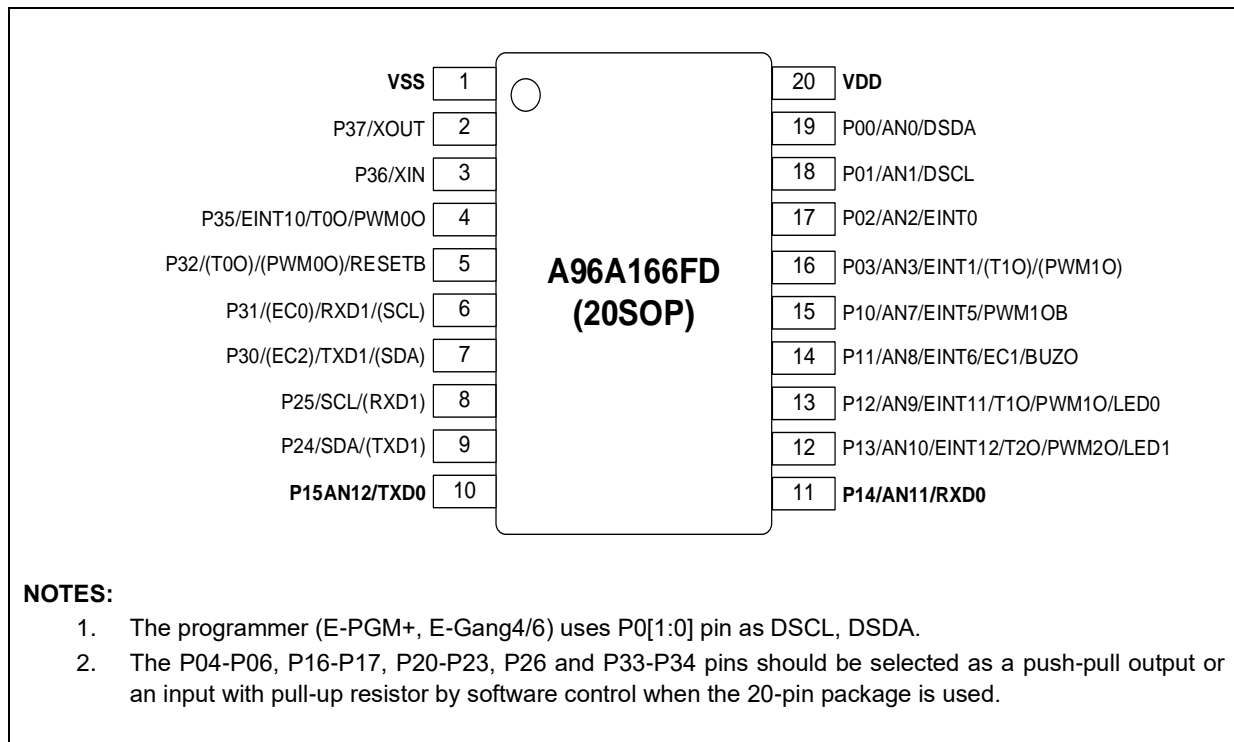


Figure 4 A96A166 20SOP Pin Assignment

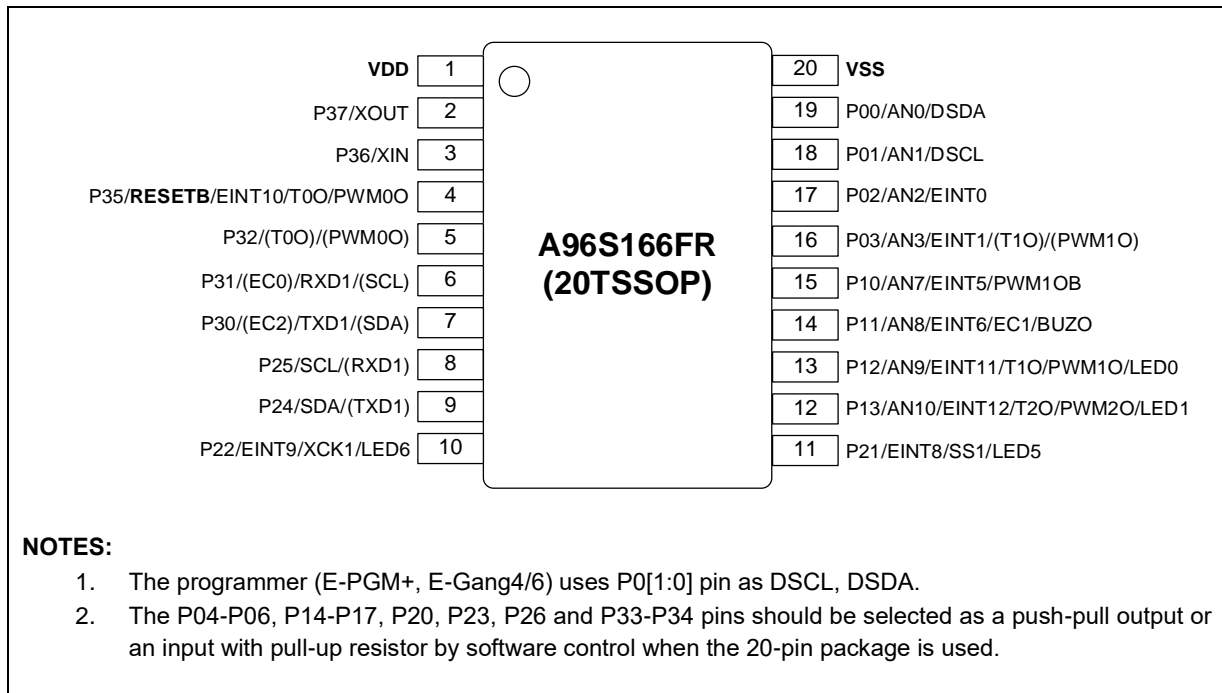


Figure 5. A96S166 20TSSOP Pin Assignment

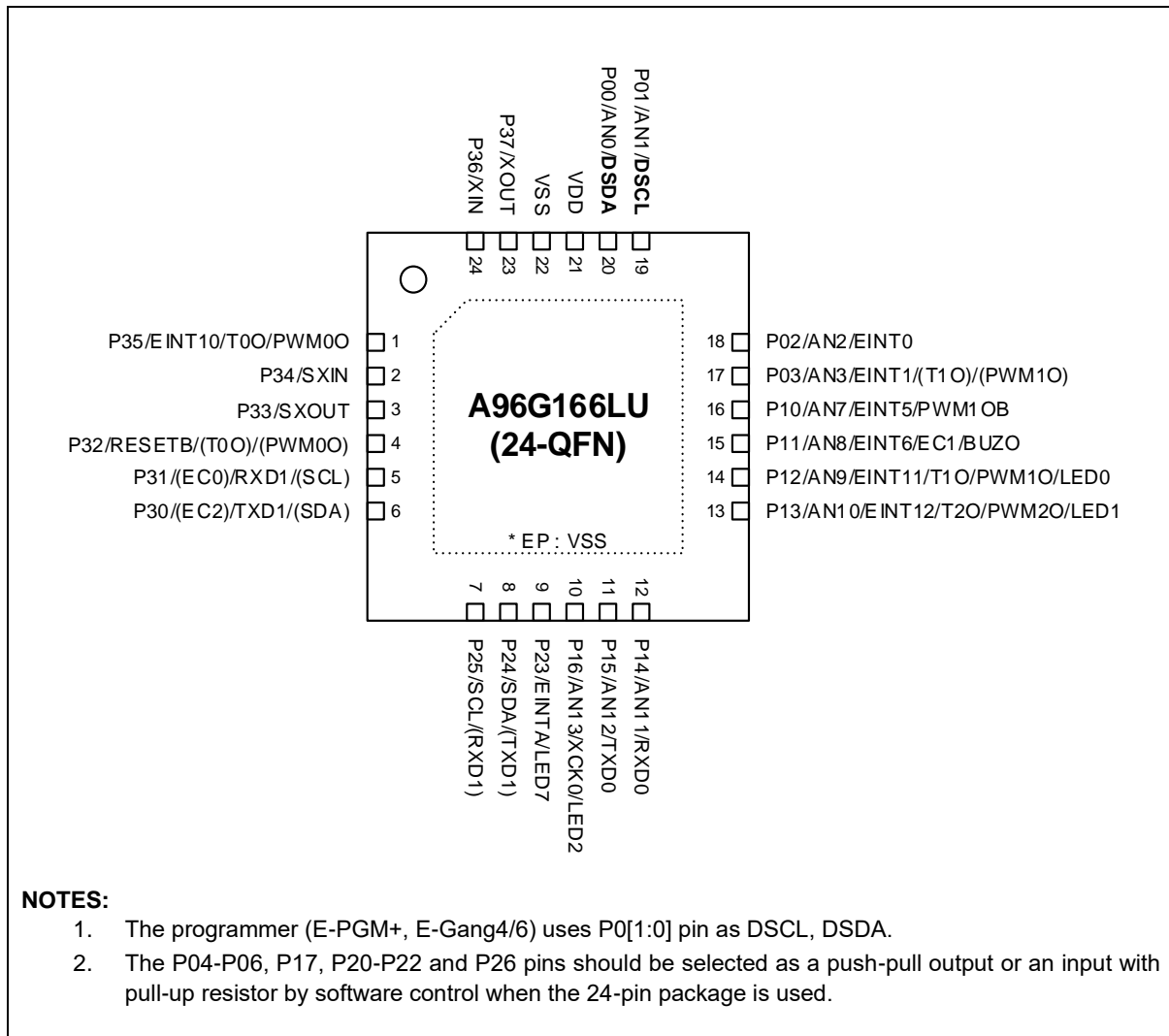


Figure 6. A96G166 24 QFN Pin Assignment

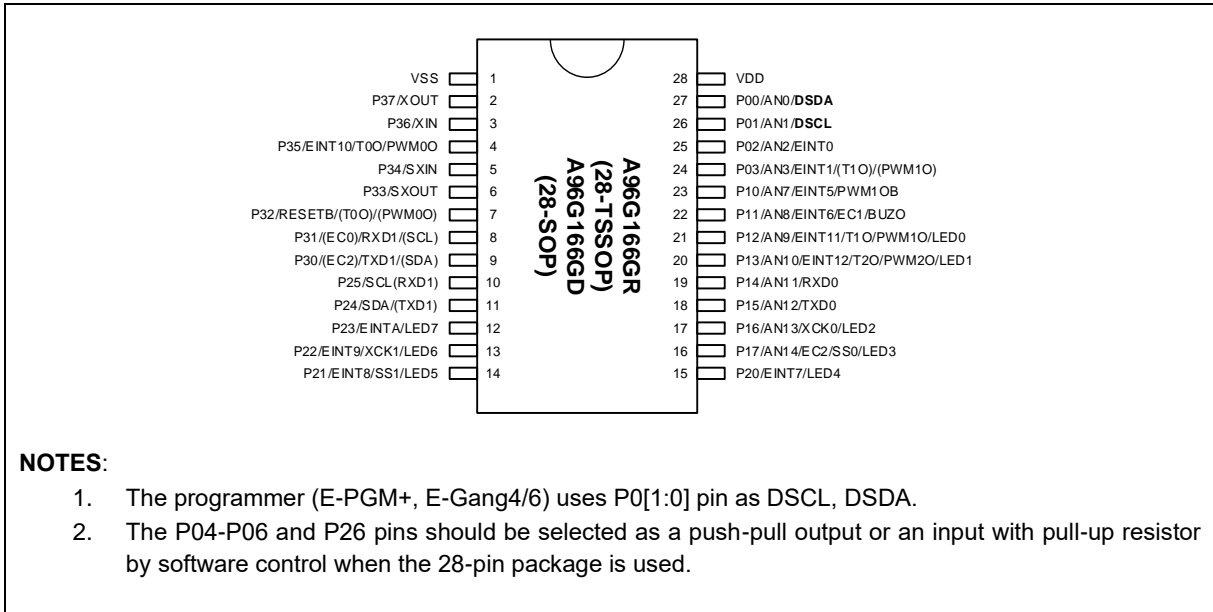


Figure 7. A96G166 28TSSOP / 28SOP Pin Assignment

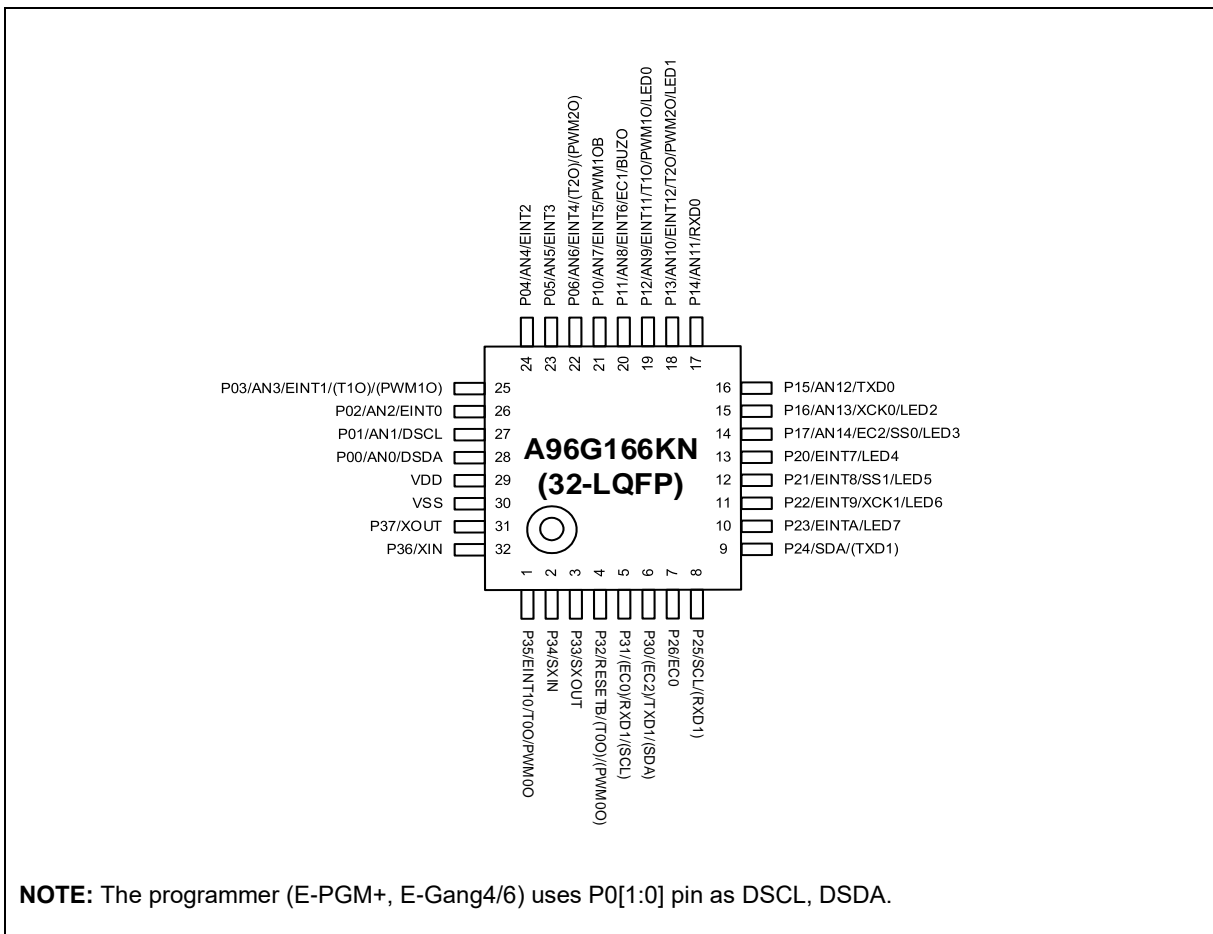


Figure 8. A96G166 32 LQFP Pin Assignment

2.2 Pin description

Table 3. Normal Pin Description

| Pin no. | | | | | | PIN name | I/O ⁽¹⁾ | Description | Remark |
|------------|--------------------|-----------|--------------------|-----------|------------|----------|--------------------|----------------------------------|---------|
| 32 LQFP | 28 SOP TSSOP | 24 QFN | 20 TSSOP | 20 SOP | 16 SOPN | | | | |
| 28 | 27 | 20 | 19 ⁽¹⁹⁾ | 19 | 15 | P00* | IOUS | Port 0 bit 0 Input/output | |
| | | | | | | AN0 | IA | ADC input ch-0 | |
| | | | | | | DSDA | IOU | OCD debugger data input/output | Pull-up |
| 27 | 26 | 19 | 18 ⁽¹⁸⁾ | 18 | 14 | P01* | IOUS | Port 0 bit 1 Input/output | |
| | | | | | | AN1 | IA | ADC input ch-1 | |
| | | | | | | DSCL | IOU | OCD debugger clock | Pull-up |
| 26 | 25 | 18 | 17 ⁽¹⁷⁾ | 17 | - | P02* | IOUS | Port 0 bit 2 Input/output | |
| | | | | | | AN2 | IA | ADC input ch-2 | |
| | | | | | | EINT0 | I | External interrupt input ch-0 | |
| 25 | 24 | 17 | 16 ⁽¹⁶⁾ | 16 | - | P03* | IOUS | Port 0 bit 3 Input/output | |
| | | | | | | AN3 | IA | ADC input ch-3 | |
| | | | | | | EINT1 | I | External interrupt input ch-1 | |
| | | | | | | T1O | O | Timer 1 interval output | |
| | | | | | | PWM1O | O | Timer 1 PWM output | |
| 24 | - | - | - | - | - | P04* | IOUS | Port 0 bit 4 Input/output | |
| | | | | | | AN4 | IA | ADC input ch-4 | |
| | | | | | | EINT2 | I | External interrupt input ch-2 | |
| 23 | - | - | - | - | - | P05* | IOUS | Port 0 bit 5 Input/output | |
| | | | | | | AN5 | IA | ADC input ch-5 | |
| | | | | | | EINT3 | I | External interrupt input ch-3 | |
| 22 | - | - | - | - | 13 | P06* | IOUS | Port 0 bit 6 Input/output | |
| | | | | | | AN6 | IA | ADC input ch-6 | |
| | | | | | | EINT4 | I | External interrupt input ch-4 | |
| | | | | | | T2O | O | Timer 2 interval output | |
| | | | | | | PWM2O | O | Timer 2 PWM output | |
| 21 | 23 | 16 | 15 ⁽¹⁵⁾ | 15 | - | P10* | IOUS | Port 1 bit 0 Input/output | |
| | | | | | | AN7 | IA | ADC input ch-7 | |
| | | | | | | EINT5 | I | External interrupt input ch-5 | |
| | | | | | | PWM1OB | IO | Timer 1 PWM complementary output | |
| 20 | 22 | 15 | 14 ⁽¹⁴⁾ | 14 | - | P11* | IOUS | Port 1 bit 1 Input/output | |
| | | | | | | AN8 | IA | ADC input ch-8 | |
| | | | | | | EINT6 | I | External interrupt input ch-6 | |
| | | | | | | EC1 | I | Timer 1(Event Capture) input | |
| | | | | | | BUZO | O | Buzzer output | |

Table 3. Normal Pin Description (continued)

| Pin no. | | | | | | PIN name | I/O ⁽¹⁾ | Description | Remark |
|---------|--------------|--------|--------------------|--------|---------|----------|--------------------|--------------------------------|--------|
| 32 LQFP | 28 SOP TSSOP | 24 QFN | 20 TSSOP | 20 SOP | 16 SOPN | | | | |
| 19 | 21 | 14 | 13 ⁽¹³⁾ | 13 | 12 | P12* | IOUS | Port 1 bit 2 Input/output | |
| | | | | | | AN9 | IA | ADC input ch-9 | |
| | | | | | | EINT11 | I | External interrupt input ch-11 | |
| | | | | | | T1O | O | Timer 1 interval output | |
| | | | | | | PWM1O | O | Timer 1 PWM output | |
| 18 | 20 | 13 | 12 ⁽¹²⁾ | 12 | 11 | LED0 | O | High sink current ports | |
| | | | | | | P13* | IOUS | Port 1 bit 3 Input/output | |
| | | | | | | AN10 | IA | ADC input ch-10 | |
| | | | | | | EINT12 | I | External interrupt input ch-12 | |
| | | | | | | T2O | O | Timer 2 interval output | |
| 17 | 19 | 12 | - | - | 10 | PWM2O | O | Timer 2 PWM output | |
| | | | | | | LED1 | O | High sink current ports | |
| | | | | | | P14* | IOUS | Port 1 bit 4 Input/output | |
| | | | | | | AN11 | IA | ADC input ch-11 | |
| | | | | | | RXD0 | I | USART0 data receive | |
| 16 | 18 | 11 | - | - | 9 | P15* | IOUS | Port 1 bit 5 Input/output | |
| | | | | | | AN12 | IA | ADC input ch-12 | |
| | | | | | | TXD0 | O | USART0 data transmit | |
| 15 | 17 | 10 | - | - | - | P16* | IOUS | Port 1 bit 6 Input/output | |
| | | | | | | AN13 | IA | ADC input ch-13 | |
| | | | | | | LED2 | O | High sink current ports | |
| | | | | | | XCK0 | IO | USART0 clock signal | |
| 14 | 16 | - | - | - | - | P17* | IOUS | Port 1 bit 7 Input/output | |
| | | | | | | AN14 | IA | ADC input ch-14 | |
| | | | | | | EC2 | I | Timer 2(Event Capture) input | |
| | | | | | | SS0 | IO | USART0 slave select signal | |
| | | | | | | LED3 | O | High sink current ports | |
| 13 | 15 | - | - | - | - | P20* | IOUS | Port 2 bit 0 Input/output | |
| | | | | | | EINT7 | I | External interrupt input ch-7 | |
| | | | | | | LED4 | O | High sink current ports | |
| 12 | 14 | - | 11 ⁽¹¹⁾ | 11 | - | P21* | IOUS | Port 2 bit 1 Input/output | |
| | | | | | | EINT8 | I | External interrupt input ch-8 | |
| | | | | | | SS1 | IO | USART1 slave select signal | |
| | | | | | | LED5 | O | High sink current ports | |
| 11 | 13 | - | 10 ⁽¹⁰⁾ | 10 | 8 | P22* | IOUS | Port 2 bit 2 Input/output | |
| | | | | | | EINT9 | I | External interrupt input ch-9 | |
| | | | | | | XCK1 | IO | USART1 clock signal | |
| | | | | | | LED6 | O | High sink current ports | |
| 10 | 12 | 9 | - | - | - | P23* | IOU | Port 2 bit 3 Input/output | |
| | | | | | | EINTA | I | External interrupt input ch-A | |
| | | | | | | LED7 | O | High sink current ports | |

Table 3. Normal Pin Description (continued)

| Pin no. | | | | | | PIN name | I/O ⁽¹⁾ | Description | Remark |
|---------|--------------|--------|-------------------|--------|---------|----------|--------------------|--------------------------------|---------|
| 32 LQFP | 28 SOP TSSOP | 24 QFN | 20 TSSOP | 20 SOP | 16 SOPN | | | | |
| 9 | 11 | 8 | 9 ⁽⁹⁾ | 9 | 7 | P24* | IOU | Port 2 bit 4 Input /output | |
| | | | | | | SDA | IO | I2C data signal | |
| | | | | | | TXD1 | O | USART1 data transmit | |
| 8 | 10 | 7 | 8 ⁽⁸⁾ | 8 | 6 | P25* | IOU | Port 2 bit 5 Input /output | |
| | | | | | | SCL | IO | I2C clock signal | |
| | | | | | | RXD1 | I | USART1 data receive | |
| 7 | - | - | - | - | 5 | P26* | IOU | Port 2 bit 6 Input /output | |
| | | | | | | EC0 | I | Timer 0(Event Capture) input | |
| 6 | 9 | 6 | 7 ⁽⁷⁾ | 7 | - | P30* | IOUS | Port 3 bit 0 Input /output | |
| | | | | | | TXD1 | O | USART1 data transmit | |
| | | | | | | EC2 | I | Timer 2(Event Capture) input | |
| | | | | | | SDA | IO | I2C data signal | |
| 5 | 8 | 5 | 6 ⁽⁶⁾ | 6 | - | P31* | IOUS | Port 3 bit 1 Input /output | |
| | | | | | | RXD1 | I | USART1 data receive | |
| | | | | | | EC0 | I | Timer 0(Event Capture) input | |
| | | | | | | SCL | IO | I2C clock signal | |
| 4 | 7 | 4 | 5 ⁽⁵⁾ | 5 | 4 | P32* | IOUS | Port 3 bit 2 Input /output | |
| | | | | | | RESETB | IU | A96G166 only, Reset pin | Pull-up |
| | | | | | | T0O | O | Timer 0 interval output | |
| | | | | | | PWM0O | O | Timer 0 PWM output | |
| 3 | 6 | 3 | - | - | - | P33* | IOUS | Port 3 bit 3 Input /output | |
| | | | | | | SXOUT | O | Sub Oscillator Output | |
| 2 | 5 | 2 | - | - | - | P34* | IOUS | Port 3 bit 4 Input /output | |
| | | | | | | SXIN | I | Sub Oscillator Input | |
| 1 | 4 | 1 | 4 ⁽⁴⁾ | 4 | - | P35* | IOUS | Port 3 bit 5 Input /output | |
| | | | | | | EINT10 | I | External interrupt input ch-10 | |
| | | | | | | T0O | O | Timer 0 interval output | |
| | | | | | | PWM0O | O | Timer 0 PWM output | |
| | | | | | | RESETB | IU | A96S166 only, Reset pin | Pull-up |
| 32 | 3 | 24 | 3 ⁽³⁾ | 3 | 3 | P36* | IOUS | Port 3 bit 6 Input/output | |
| | | | | | | XIN | I | Main Oscillator Input | |
| 31 | 2 | 23 | 2 ⁽²⁾ | 2 | 2 | P37* | IOUS | Port 3 bit 7 Input/output | |
| | | | | | | XOUT | I | Main Oscillator Output | |
| 29 | 28 | 21 | 20 ⁽¹⁾ | 20 | 16 | VDD | P | VDD | |
| 30 | 1 | 22 | 1 ⁽²⁰⁾ | 1 | 1 | VSS | P | VSS | |

NOTES:

- The ^(*) is applied to 20 TSSOP of A96S166
- The P04–P06 and P26 are not in the 28-pin package.
- The P04–P06, P17, P20–P22 and P26 are not in the 24-pin package.
- The P04–P06, P14–P17, P20, P23, P26 and P33–P34 are not in the 20-pin package.
- The P02–P05, P10–P11, P16–P17, P20–P21, P23, P30–P31 and P33–P35 are not in the 16-pin package.
- The P32/RESETB (A96G166) pin is configured as one of the P32 and RESETB pin by the "CONFIGURE OPTION." (P35/RESETB : A96S166)
- If the P00/AN0/DSDA and P01/AN1/DSCL pins are connected to the programmer during power-on reset, the pins are automatically configured as In-system programming pins.
- The P00/AN0/DSDA and P01/AN1/DSCL pins are configured as inputs with internal pull-up resistor only during the reset or power-on reset.
- The P36/XIN, P37/XOUT, P33/SXOUT, and P34/SXIN pins are configured as a function pin by software control.
- (1) I=Input, O=Output, U=Pull-up, D=Pull-down, S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
- The * means 'Selected pin function after reset condition

3 Port structures

In this chapter, two port structures are introduced. Figure 9 and Figure 10 show general purpose I/O port and external interrupt I/O port respectively.

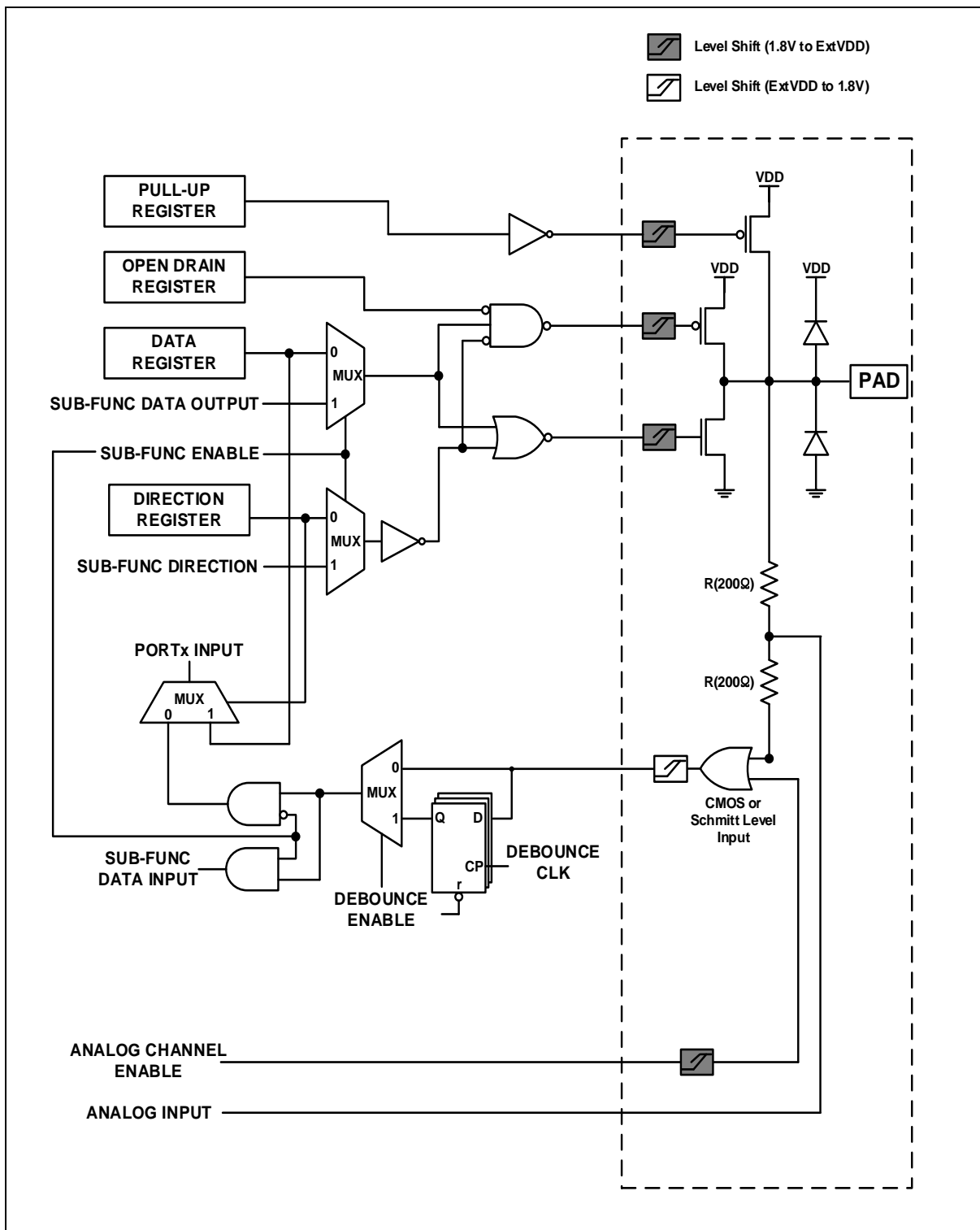


Figure 9. General Purpose I/O Port

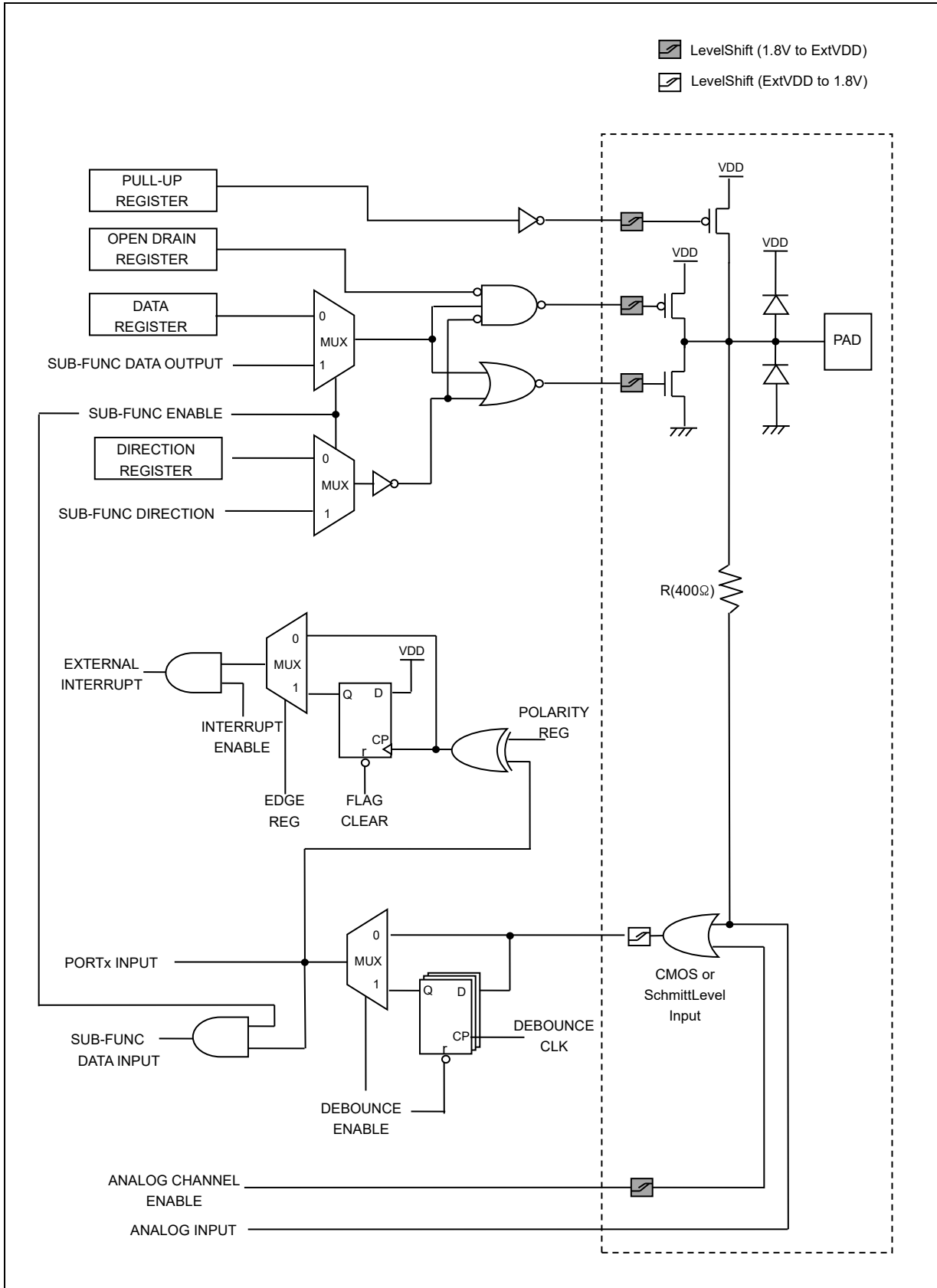


Figure 10. External Interrupt I/O Port

4 Central processing unit (CPU)

Central Processing Unit (CPU) of A96G140 is based on Mentor Graphics M8051EW core, which offers improved code efficiency and performance.

4.1 Architecture and registers

Figure 11 shows a block diagram of the M8051EW architecture. As shown in the figure, the M8051EW supports both Program Memory and External Data Memory. In addition, it features a Debug Mode in which it can be driven through a dedicated debug interface.

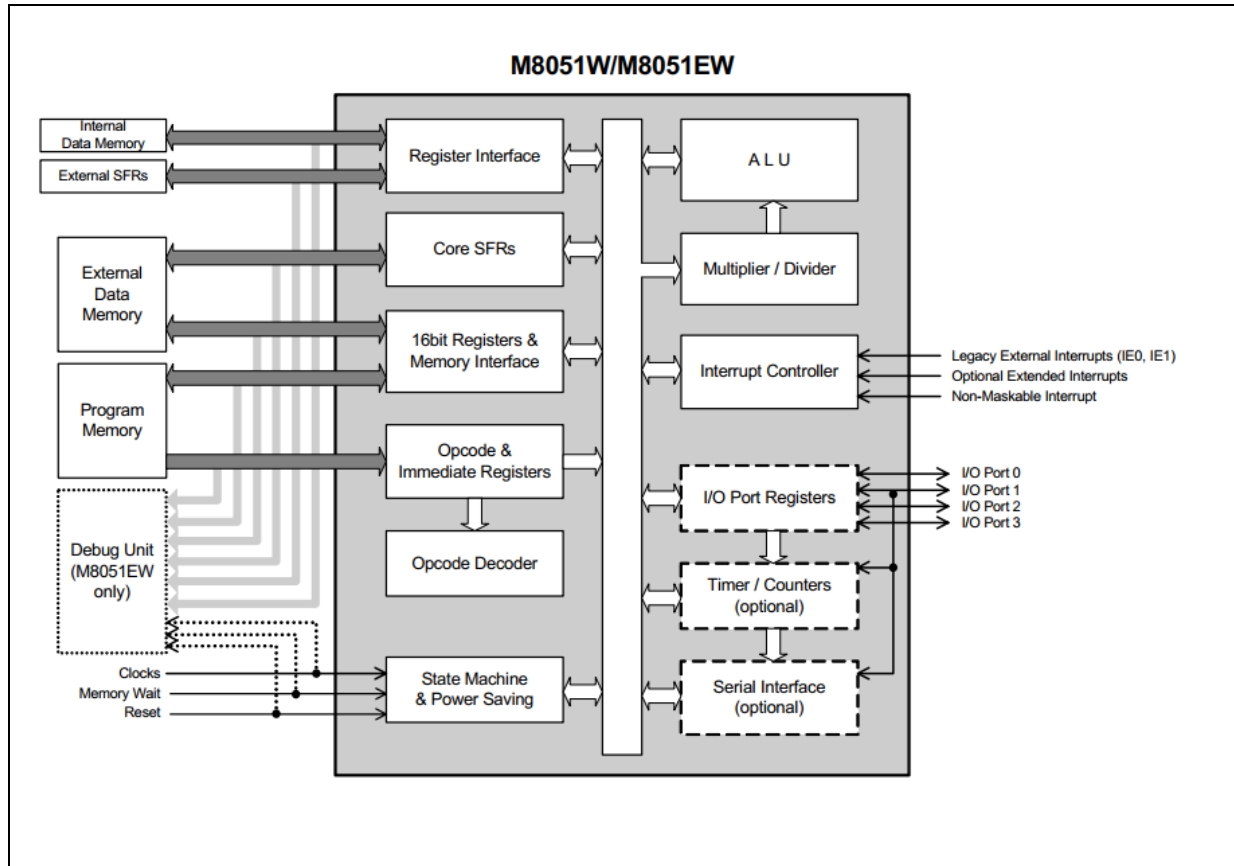


Figure 11 M8051EW Architecture

Main features of the M8051EW are listed below:

- Two clocks per machine cycle architecture:
- Debug support (OCD and OCD II):
- Separate program and external data memory interfaces or a single multiplexed interface
- Support for synchronous and asynchronous Program, External Data and Internal Data Memory
- Wait states support for slow Program and External Data Memory
- 16-bit Data Memory address is generated through the Data Point register (DPTR register).
- 16-bit program counter is capable of addressing up to Flash size in Each device
- A single data pointer, two memory-mapped data pointers, or 2 banked data pointers

- Support 2 or 4 level of priority scheme – Up to 24 maskable Interrupt sources
- External Special Function Register(SFR) are memory mapped into Direct Memory at the address between 80 hex and FF hex.

4.2 Addressing

The M8051EW supports six types of addressing modes as listed below:

1. Direct addressing mode: In this mode, the operand is specified by the 8-bit address field. Only internal data and SFRs can be accessed using this mode.
2. Indirect addressing mode: In this mode, the operand is specified by addresses contained in a register. Two registers (R0 and R1) from the current bank or the Data Pointer may be used for addressing in this mode. Both internal and external Data Memory may be indirectly addressed.
3. Register addressing mode: In this mode, the operand is specified by the top 3 bits of the opcode, which selects one of the current bank of registers. Four banks of registers are available. The current bank is selected by the 3rd and 4th bits of the PSW.
4. Register specific addressing mode: In this mode, some instructions only operate on specific registers. This is defined by the opcode. In particular many accumulator operations and some stack pointer operations are defined in this manner.
5. Immediate DATA mode: In this mode, Instructions which use Immediate Data are 2 or more bytes long and the Immediate operand is stored in Program Memory as part of the instruction.

Example) MOV A, #100

It loads the Accumulator with the decimal number 100. The same number could be specified in hex digits as 64H.

6. Indexed addressing mode: In this mode, only Program Memory can be addressed. It is intended for simple implementation of look-up tables. A 16-bit base register (either the PC or the DPTR) is combined with an offset stored in the accumulator to access data in Program Memory.

4.3 Instruction set

An instruction is a single operation of a processor that is defined by the instruction set. The M8051EW uses the instruction set of 8051 that is broadly classified into five functional categories:

1. Arithmetic instructions
2. Logical instructions
3. Data transfer instructions
4. Boolean instructions
5. Branching instructions

Major features of the instruction set are listed below. If you need detailed information about the instruction table, please refer to **Appendix** or **Instruction table**:

- Instructions are either 1, 2 or 3 bytes long as listed in the 'Bytes'.
- Each instruction takes either 1, 2 or 4 machine cycles to execute. 1 machine cycle comprises 2 CCLK clock cycles.
- An M8051EW-specific instruction "MOVC @ (DPTR++), A" is provided to enable software to be downloaded into Program Memory where it is implemented as RAM. This instruction can also be used subsequently to modify contents of the Program Memory RAM.
- Arithmetic Instruction
- Logical Instruction
- Internal data memory
- External data memory
- Unconditional Jumps
- Subroutine calls and returns
- Conditional Jumps
- Boolean Instructions
- Flag

5 Memory organization

A96G166/A96A166/A96S166 addresses two separate address memory spaces:

- Program memory
- Data memory

By means of this logical separation of the memory, 8-bit CPU address can access the Data Memory more rapidly. 16-bit Data Memory address is generated through the DPTR register.

A96G166/A96A166/A96S166 provides on-chip 16Kbytes of the ISP type flash program memory, which readable and writable. Internal data memory (IRAM) is 256bytes and it includes the stack area. External data memory (XRAM) is 512bytes.

5.1 Program memory

A 16-bit program counter is capable of addressing up to 64Kbytes, and A96G166/A96A166/A96S166 has just 16Kbytes program memory space.

Figure 12 shows a map of the lower part of the program memory.

After reset, CPU begins execution from location 0000H. Each interrupt is assigned a fixed location in the program memory. An interrupt causes the CPU to jump to the corresponding location, where it commences execution of the service routine.

An external interrupt 11, for example, is assigned to location 000BH. If the external interrupt 11 is going to be used, its service routine must begin at location 000BH. If the interrupt is not going to be used, its service location is available as general purpose program memory. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within an interval of 8-bytes.

Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.

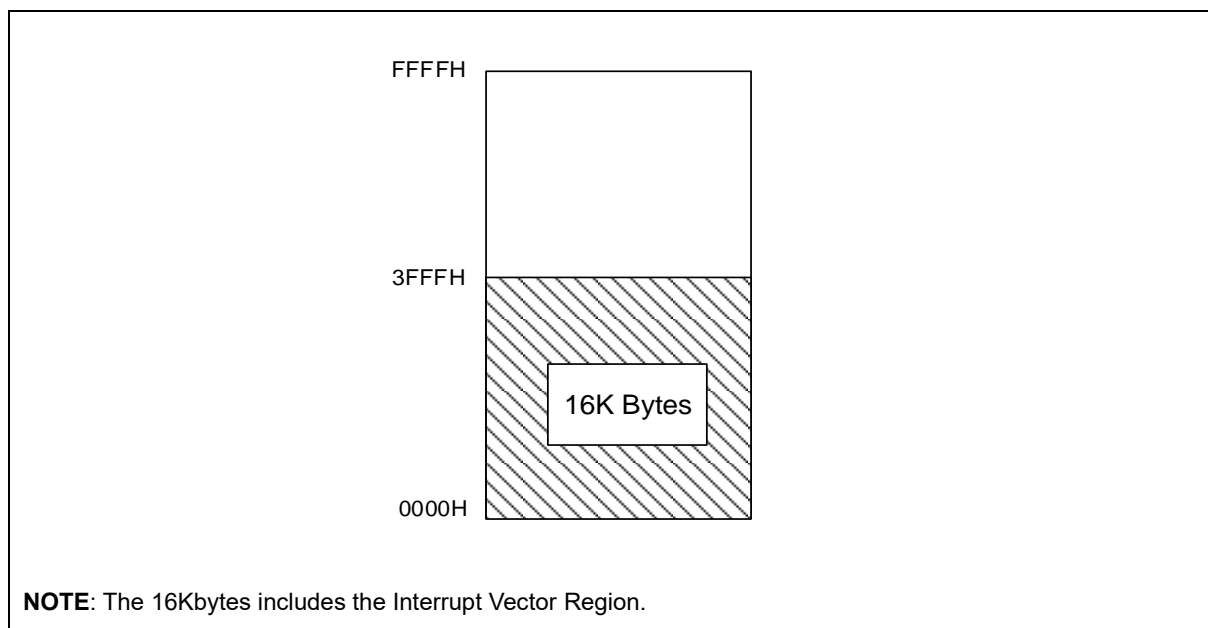


Figure 12. Program Memory Map

5.2 Data memory

Internal data memory space is divided into three blocks, which are generally referred to as lower 128bytes, upper 128bytes, and SFR space. Internal data memory addresses are always one byte wide, which implies an address space of 256bytes. In fact, the addressing modes for the internal data memory can accommodate up to 384bytes by using a simple trick. Direct addresses higher than 7FH access one memory space, while indirect addresses higher than 7FH access a different memory space. Thus as shown in Figure 13, the upper 128bytes and SFR space occupy the same block of addresses, 80H through FFH, although they are physically separate entities.

The lower 128bytes of RAM are present in all 8051 devices as mapped in Figure 14. The lowest 32bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16bytes above the register banks form a block of bit-addressable memory space. The 8051 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All of the bytes in the lower 128bytes can be accessed by either direct or indirect addressing. The upper 128bytes of RAM can only be accessed by indirect addressing. These spaces are used for data RAM and stack.

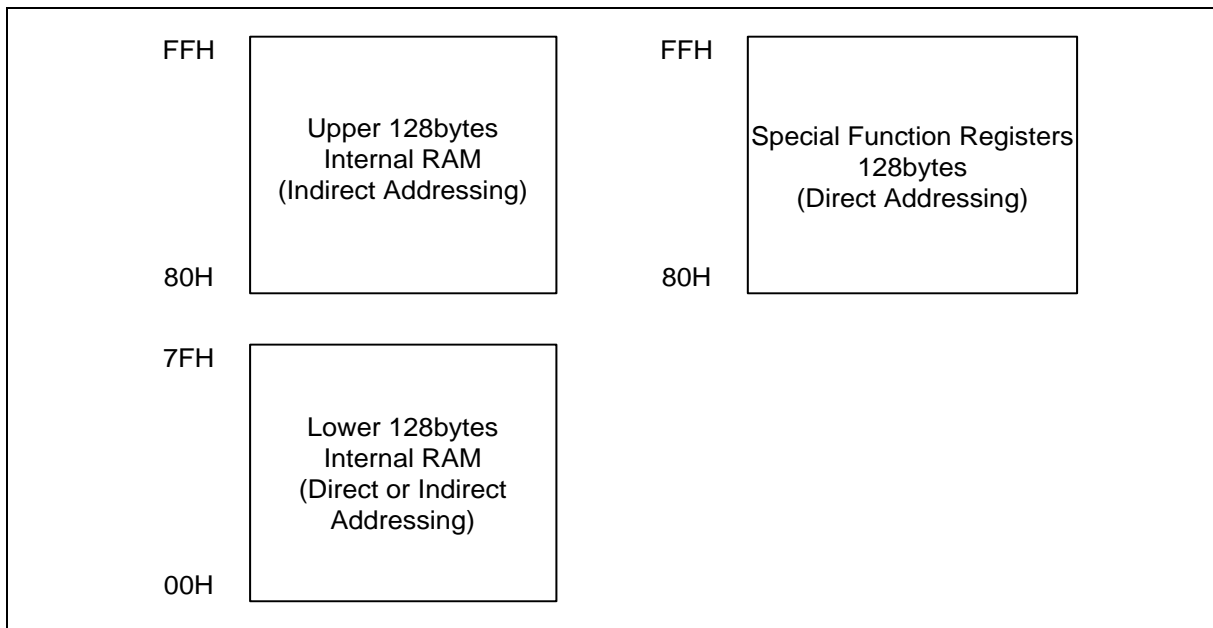


Figure 13. Data Memory Map

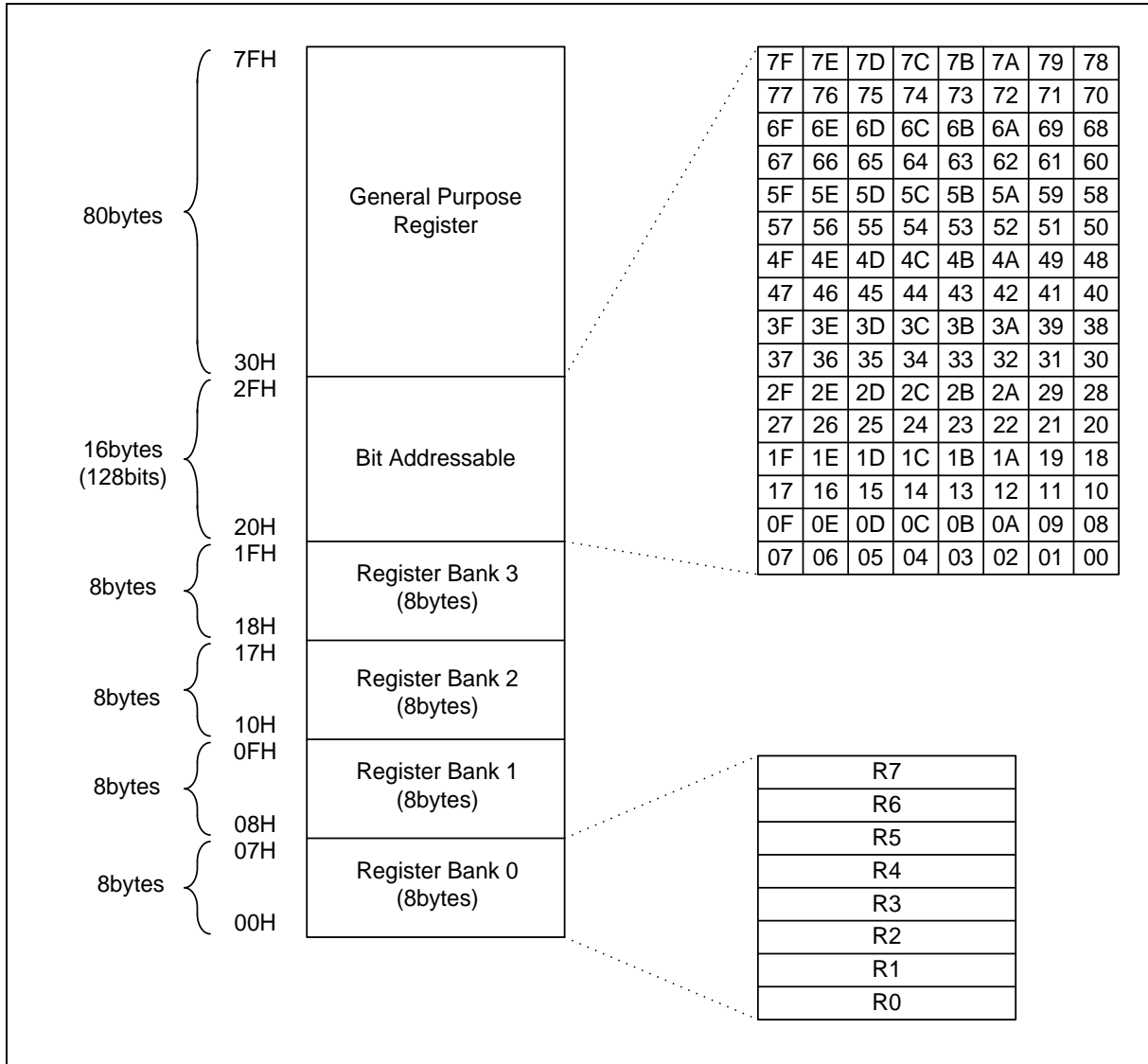


Figure 14. Lower 128bytes of RAM

5.3 External data memory

A96G166/A96A166/A96S166 has 512bytes of XRAM and XSFR. This area has no relation with RAM/FLASH. It can be read and written to through SFR with 8-bit unit.

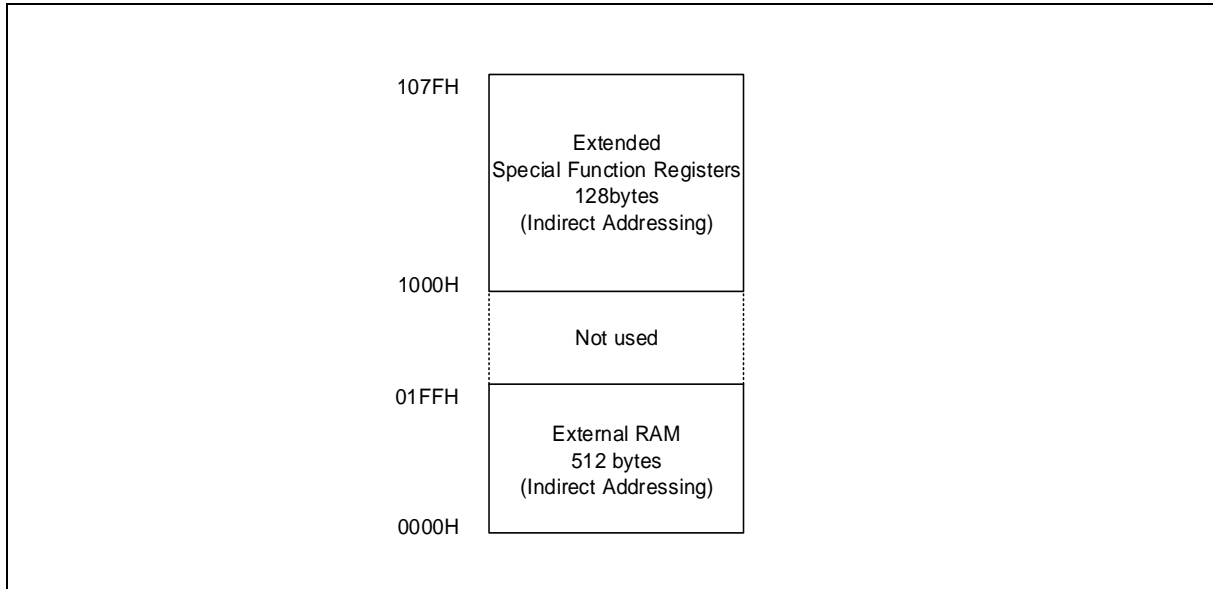


Figure 15. XDATA Memory Area

5.4 SFR map

5.4.1 SFR map summary

Table 4. SFR Map Summary

| | 00H/8H ⁽¹⁾ | 01H/9H | 02H/0AH | 03H/0BH | 04H/0CH | 05H/0DH | 06H/0EH | 07H/0FH |
|------|-----------------------|------------------|---------|----------|----------------|----------|---------|---------|
| | – | Reserved | | | | | | |
| | | M8051 compatible | | | | | | |
| 0F8H | IP1 | – | – | – | U0BAUD | U0DATA | – | – |
| 0F0H | B | U1CTRL1 | U1CTRL2 | U1CTRL3 | – | U1BAUD | U1DATA | U1STAT |
| 0E8H | RSTFR | I2CSAR | I2CSAR1 | – | – | – | – | – |
| 0E0H | ACC | I2CMR | I2CSR | I2CSCLLR | I2CSCLHR | I2CSDAHR | I2CDR | – |
| 0D8H | LVRRCR | T1CDRL | T1CDRH | T1DDRL | T1DDRH | – | P0DB | P12DB |
| 0D0H | PSW | – | P0FSRL | P0FSRH | P1FSRL | P1FSRH | P2FSRL | P2FSRH |
| 0C8H | OSCCR | – | – | U0CTRL1 | U0CTRL2 | U0CTRL3 | – | U0STAT |
| 0C0H | EIFLAG0 | – | T2CRL | T2CRH | T2ADRL | T2ADRH | T2BDRL | T2BDRH |
| 0B8H | IP | P2IO | T1CRL | T1CRH | T1ADRL | T1ADRH | T1BDRL | T1BDRH |
| 0B0H | – | P1IO | T0CR | T0CNT | T0DR/ T0CDR | | | |
| 0A8H | IE | IE1 | IE2 | IE3 | P0PU | P1PU | P2PU | P3PU |
| 0A0H | – | P0IO | EO | EIPOL2 | EIPOL0L | EIPOL0H | EIFLAG1 | EIPOL1 |
| 98H | P3 | P3IO | P3FSRL | P3FSRH | ADCCR2 | ADCCRH | ADC2DRL | ADC2DRH |
| 90H | P2 | P0OD | P1OD | P2OD | P3OD | – | WTCR | BUZCR |
| 88H | P1 | WTDR/ WTCNT | SCCR | BITCR | BITCNT | WDTCR | WDTIDR | BUZDR |
| 80H | P0 | SP | DPL | DPH | DPL1 | DPH1 | LVICR | PCON |

NOTE: 00H/8H, these registers are bit-addressable.

Table 5. XSFR Map Summary

| | 00H/8H ⁽¹⁾ | 01H/9H | 02H/0AH | 03H/0BH | 04H/0CH | 05H/0DH | 06H/0EH | 07H/0FH |
|-------|-----------------------|------------------|------------------|------------------|----------------|----------------|----------------|---------|
| 1078H | – | CRC_ADDR_START_H | CRC_ADDR_START_M | CRC_ADDR_START_L | CRC_ADDR_END_H | CRC_ADDR_END_M | CRC_ADDR_END_L | – |
| 1070H | CRC_CON | – | CRC_H | CRC_L | CRC_MNT_H | CRC_MNT_L | – | – |
| 1068H | – | – | – | – | – | – | – | – |
| 1060H | – | – | – | – | – | – | – | – |
| 1058H | – | – | – | – | – | – | – | – |
| 1050H | – | – | – | – | – | – | – | – |
| 1048H | – | – | – | – | – | – | – | – |
| 1040H | – | – | – | – | – | – | – | – |
| 1038H | XTFLSR | – | – | – | – | – | – | – |
| 1030H | – | – | – | – | – | – | – | – |
| 1028H | FEARH | FEARM | FEARL | FEDR | FETR | – | – | – |
| 1020H | FEMR | FECR | FESR | FETCR | FEARM1 | FEARL1 | – | – |
| 1018H | U0CTRL4 | U1CTRL4 | FPCR0 | RTOCH0 | RTOCL0 | FPCR1 | RTOCH1 | RTOCL1 |
| 1010H | WDC | WDTSR | WDCNTH | WDCNTL | – | – | – | – |
| 1008H | – | – | – | – | – | – | – | – |
| 1000H | – | – | – | – | – | – | – | – |

NOTE: 00H/8H, these registers are bit-addressable.

5.4.2 SFR map

Table 6. SFR Map

| Address | Function | Symbol | R/W | @Reset | | | | | | | | |
|---------|---|--------|-----|--------|---|---|---|---|---|---|---|---|
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 80H | P0 Data Register | P0 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 81H | Stack Pointer | SP | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 82H | Data Pointer Register Low | DPL | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 83H | Data Pointer Register High | DPH | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 84H | Data Pointer Register Low 1 | DPL1 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 85H | Data Pointer Register High 1 | DPH1 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 86H | Low Voltage Indicator Control Register | LVICR | R/W | – | – | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 87H | Power Control Register | PCON | R/W | 0 | – | – | – | 0 | 0 | 0 | 0 | 0 |
| 88H | P1 Data Register | P1 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 89H | Watch Timer Data Register | WTDR | W | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Watch Timer Counter Register | WTCNT | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 8AH | System and Clock Control Register | SCCR | R/W | – | – | – | – | – | – | 0 | 0 | 0 |
| 8BH | Basic Interval Timer Control Register | BITCR | R/W | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 8CH | Basic Interval Timer Counter Register | BITCNT | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 8DH | Watch Dog Timer Control Register | WDTCR | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 8EH | Watch Dog Timer Identification Register | WDTIDR | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 8FH | Buzzer Data Register | BUZDR | R/W | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 90H | P2 Data Register | P2 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 91H | P0 Open-drain Selection Register | P0OD | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 92H | P1 Open-drain Selection Register | P1OD | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 93H | P2 Open-drain Selection Register | P2OD | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 94H | P3 Open-drain Selection Register | P3OD | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 96H | Watch Timer Control Register | WTCR | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 97H | Buzzer Control Register | BUZCR | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 98H | P3 Data Register | P3 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 99H | P3 Direction Register | P3IO | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 9AH | P3 Function Selection Low Register | P3FSRL | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 9BH | P3 Function Selection High Register | P3FSRH | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 9CH | A/D Converter Control Low Register | ADCCRL | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 9DH | A/D Converter Control High Register | ADCCRH | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 9EH | A/D Converter Data Low Register | ADCRL | R | x | x | x | x | x | x | x | x | x |
| 9FH | A/D Converter Data High Register | ADCRH | R | x | x | x | x | x | x | x | x | x |

Table 6. SFR Map (continued)

| Address | Function | Symbol | R/W | @Reset | | | | | | | | |
|---------|---|---------|-----|--------|---|---|---|---|---|---|---|---|
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| A1H | P0 Direction Register | P0IO | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| A2H | Extended Operation Register | EO | R/W | – | – | – | 0 | – | 0 | 0 | 0 | 0 |
| A3H | External Interrupt Polarity 2 Register | EIPOL2 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| A4H | External Interrupt Polarity 0 Low Register | EIPOL0L | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| A5H | External Interrupt Polarity 0 High Register | EIPOL0H | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| A6H | External Interrupt Flag 1 Register | EIFLAG1 | R/W | 0 | 0 | – | – | 0 | 0 | 0 | 0 | 0 |
| A7H | External Interrupt Polarity 1 Register | EIPOL1 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| A8H | Interrupt Enable Register | IE | R/W | 0 | – | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| A9H | Interrupt Enable Register 1 | IE1 | R/W | – | – | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| AAH | Interrupt Enable Register 2 | IE2 | R/W | – | – | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ABH | Interrupt Enable Register 3 | IE3 | R/W | – | – | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ACH | P0 Pull-up Resistor Selection Register | P0PU | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| ADH | P1 Pull-up Resistor Selection Register | P1PU | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| AEH | P2 Pull-up Resistor Selection Register | P2PU | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| AFH | P3 Pull-up Resistor Selection Register | P3PU | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| B1H | P1 Direction Register | P1IO | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| B2H | Timer 0 Control Register | T0CR | R/W | 0 | – | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| B3H | Timer 0 Counter Register | T0CNT | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| B4H | Timer 0 Data Register | T0DR | R/W | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Timer 0 Capture Data Register | T0CDR | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| B8H | Interrupt Priority Register | IP | R/W | – | – | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| B9H | P2 Direction Register | P2IO | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BAH | Timer 1 Control Low Register | T1CRL | R/W | 0 | 0 | 0 | 0 | – | 0 | 0 | 0 | 0 |
| BBH | Timer 1 Counter High Register | T1CRH | R/W | 0 | – | 0 | 0 | – | – | – | – | 0 |
| BCH | Timer 1 A Data Low Register | T1ADRL | R/W | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| BDH | Timer 1 A Data High Register | T1ADRH | R/W | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| BEH | Timer 1 B Data Low Register | T1BDRL | R/W | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| BFH | Timer 1 B Data High Register | T1BDRH | R/W | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| D9H | Timer 1 C Data Low Register | T1CDRL | R/W | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| DAH | Timer 1 C Data High Register | T1CDRH | R/W | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| DBH | Timer 1 D Data Low Register | T1DDRL | R/W | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| DCH | Timer 1 D Data High Register | T1DDRH | R/W | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Table 6. SFR Map (continued)

| Address | Function | Symbol | R/W | @Reset | | | | | | | | |
|---------|--------------------------------------|----------|-----|--------|---|---|---|---|---|---|---|---|
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| C0H | External Interrupt Flag 0 Register | EIFLAG0 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| C2H | Timer 2 Control Low Register | T2CRL | R/W | 0 | 0 | 0 | 0 | – | 0 | – | 0 | 0 |
| C3H | Timer 2 Control High Register | T2CRH | R/W | 0 | – | 0 | 0 | – | – | – | 0 | 0 |
| C4H | Timer 2 A Data Low Register | T2ADRL | R/W | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| C5H | Timer 2 A Data High Register | T2ADRH | R/W | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| C6H | Timer 2 B Data Low Register | T2BDRL | R/W | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| C7H | Timer 2 B Data High Register | T2BDRH | R/W | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| C8H | Oscillator Control Register | OSCCR | R/W | – | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| CBH | USART0 Control Register 1 | U0CTRL1 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CCH | USART0 Control Register 2 | U0CTRL2 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| CDH | USART0 Control Register 3 | U0CTRL3 | R/W | 0 | 0 | 0 | 0 | – | 0 | 0 | 0 | 0 |
| CFH | USART0 Status Register | U0STAT | R/W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| FCH | USART0 Baud Rate Generation Register | UBAUD | R/W | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| FDH | USART0 Data Register | UDATA | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0H | Program Status Word Register | PSW | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D2H | P0 Function Selection Low Register | P0FSRL | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D3H | P0 Function Selection High Register | P0FSRH | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D4H | P1 Function Selection Low Register | P1FSRL | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D5H | P1 Function Selection High Register | P1FSRH | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D6H | P2 Function Selection Low Register | P2FSRL | R/W | – | – | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D7H | P2 Function Selection High Register | P2FSRH | R/W | – | – | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D8H | Low Voltage Reset Control Register | LVRCR | R/W | – | – | – | 0 | 0 | 0 | 0 | 0 | 0 |
| DEH | P0 De-bounce Enable Register | P0DB | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DFH | P1 De-bounce Enable Register | P1DB | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| E0H | Accumulator Register | ACC | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| E1H | I2C Mode Control Register | I2CMR | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| E2H | I2C Status Register | I2CSR | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| E3H | SCL Low Period Register | I2CSCLLR | R/W | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| E4H | SCL High Period Register | I2CSCLHR | R/W | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| E5H | SDA Hold Time Register | I2CSDAHR | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| E6H | I2C Data Register | I2CDR | R/W | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| E8H | Reset Flag Register | RSTFR | R/W | 1 | x | 0 | 0 | x | – | – | – | – |
| E9H | I2C Slave Address Register | I2CSAR | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| EAH | I2C Slave Address Register 1 | I2CSAR1 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| F0H | B Register | B | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| F1H | USART1 Control Register 1 | U1CTRL1 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| F2H | USART1 Control Register 2 | U1CTRL2 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| F3H | USART1 Control Register 3 | U1CTRL3 | R/W | 0 | 0 | 0 | 0 | – | 0 | 0 | 0 | 0 |
| F5H | USART1 Baud Rate Generation Register | U1BAUD | R/W | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| F6H | USART1 Data Register | U1DATA | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| F7H | USART1 Status Register | U1STAT | R/W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| F1H | USART1 Control Register 1 | U1CTRL1 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| F8H | Interrupt Priority Register 1 | IP1 | R/W | – | – | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 7. XSFR Map

| Address | Function | Symbol | R/W | @Reset | | | | | | | | |
|---------|--|----------------------|-----|--------|---|---|---|---|---|---|---|---|
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 1010H | Watch Dog Timer Clear Register | WDTC | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1011H | Watch Dog Timer Status Register | WDTSR | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1012H | Watch Dog Timer Count H Register | WDTCNTH | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1013H | Watch Dog Timer Count L Register | WDTCNTL | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1018H | USART0 Control Register 4 | U0CTRL4 | R/W | – | – | – | 0 | 0 | 0 | 0 | 0 | 0 |
| 1019H | USART1 Control Register 4 | U1CTRL4 | R/W | – | – | – | 0 | 0 | 0 | 0 | 0 | 0 |
| 101AH | USART0 Floating Point Counter | FPCR0 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 101BH | USART0 Receiver Time Out Counter High Register | RTOCH0 | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 101CH | USART0 Receiver Time Out Counter Low Register | RTOCL0 | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 101DH | USART1 Floating Point Counter | FPCR1 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 101EH | USART1 Receiver Time Out Counter High Register | RTOCH1 | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 101FH | USART1 Receiver Time Out Counter Low Register | RTOCL1 | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1020H | Flash Mode Register | FEMR | R/W | 0 | – | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1021H | Flash Control Register | FECR | R/W | 0 | – | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1022H | Flash Status Register | FESR | R/W | 1 | – | – | – | 0 | 0 | 0 | 0 | 0 |
| 1023H | Flash Time Control Register | FETCR | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1024H | Flash Address Middle Register 1 | FEARM1 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1025H | Flash Address Low Register 1 | FEARL1 | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1028H | Flash Address High Register | FEARH | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1029H | Flash Address Middle Register | FEARM | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 102AH | Flash Address Low Register | FEARL | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1038H | Main Crystal OSC Filter Selection Register | XTFLSR | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1070H | CRC Control Register | CRC_CON | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1072H | CRC High Register | CRC_H | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1073H | CRC Low Register | CRC_L | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1074H | CRC Monitor High Register | CRC_MNT_H | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1075H | CRC Monitor Low Register | CRC_MNT_L | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1079H | CRC Start Address High Register | CRC_ADDR_S TART_H | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 107AH | CRC Start Address Middle Register | CRC_ADDR_S TART_M | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 107BH | CRC Start Address Low Register | CRC_ADDR_S TART_L | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 107CH | CRC End Address High Register | CRC_ADDR_E ND_H | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 107DH | CRC End Address Middle Register | CRC_ADDR_E ND_M | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 107EH | CRC End Address Low Register | CRC_ADDR_E ND_L | R/W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

6 I/O ports

A96G166/A96A166/A96S166 has ten groups of I/O ports (P0 to P2). Each port can be easily configured by software as an I/O pin, an internal pull up or an open-drain pin to meet various system configurations and design requirements. P0 includes a function that can generate interrupt signals according to state of a pin.

6.1 P0 port

6.1.1 P0 port description

P0 is an 8-bit I/O port. P0 control registers consist of P0 data register (P0), P0 direction register (P0IO), debounce enable register (P0DB), P0 pull-up resistor selection register (P0PU), and P0 open-drain selection register (P0OD). Refer to the port function selection registers for the P0 function selection.

6.2 P1 port

6.2.1 P1 port description

P1 is an 8-bit I/O port. P1 control registers consist of P1 data register (P1), P1 direction register (P1IO), debounce enable register (P1DB), P1 pull-up resistor selection register (P1PU), and P1 open-drain selection register (P1OD). Refer to the port function selection registers for the P1 function selection.

6.3 P2 port

6.3.1 P2 port description

P2 is an 8-bit I/O port. P2 control registers consist of P2 data register (P2), P2 direction register (P2IO), P2 pull-up resistor selection register (P2PU) and P2 open-drain selection register (P2OD). Refer to the port function selection registers for the P2 function selection.

6.4 P3 port

6.4.1 P3 port description

P3 is an 8-bit I/O port. P3 control registers consist of P3 data register (P3), P3 direction register (P3IO) and P3 pull-up resistor selection register (P3PU). Refer to the port function selection registers for the P3 function selection.

7 Interrupt controller

A96G166/A96A166/A96S166 supports up to 21 interrupt sources. The interrupts have separate enable register bits associated with them, allowing software control. In addition, they have four levels of priority assigned to themselves.

A non-maskable interrupt source is always enabled with a higher priority than any other interrupt sources, and is not controllable by software.

Interrupt controller of A96G166/A96A166/A96S166 has following features:

- Request receive from the 21 interrupt sources
- 6 groups of priority
- 4 levels of priority
- Multi Interrupt possibility
- A request of higher priority level is served first, when multiple requests of different priority levels are received simultaneously.
- Each interrupt source can be controlled by EA bit and each IEx bit
- Interrupt latency of 3 to 9 machine cycles in single interrupt system

A non-maskable interrupt is always enabled, while maskable interrupts are enabled through four pairs of interrupt enable registers (IE, IE1, IE2, and IE3). Each bit of IE, IE1, IE2, IE3 register individually enables/disables the corresponding interrupt source. Overall control is provided by bit 7 of IE (EA). When EA is set to '0', all interrupts are disabled: when EA is set to '1', interrupts are individually enabled or disabled through the other bits of the interrupt enable registers. The EA bit is always cleared to '0' jumping to an interrupt service vector and set to '1' executing the [RETI] instruction. The A96G166/A96A166/A96S166 supports a four-level priority scheme. Each maskable interrupt is individually assigned to one of four priority levels according to IP and IP1.

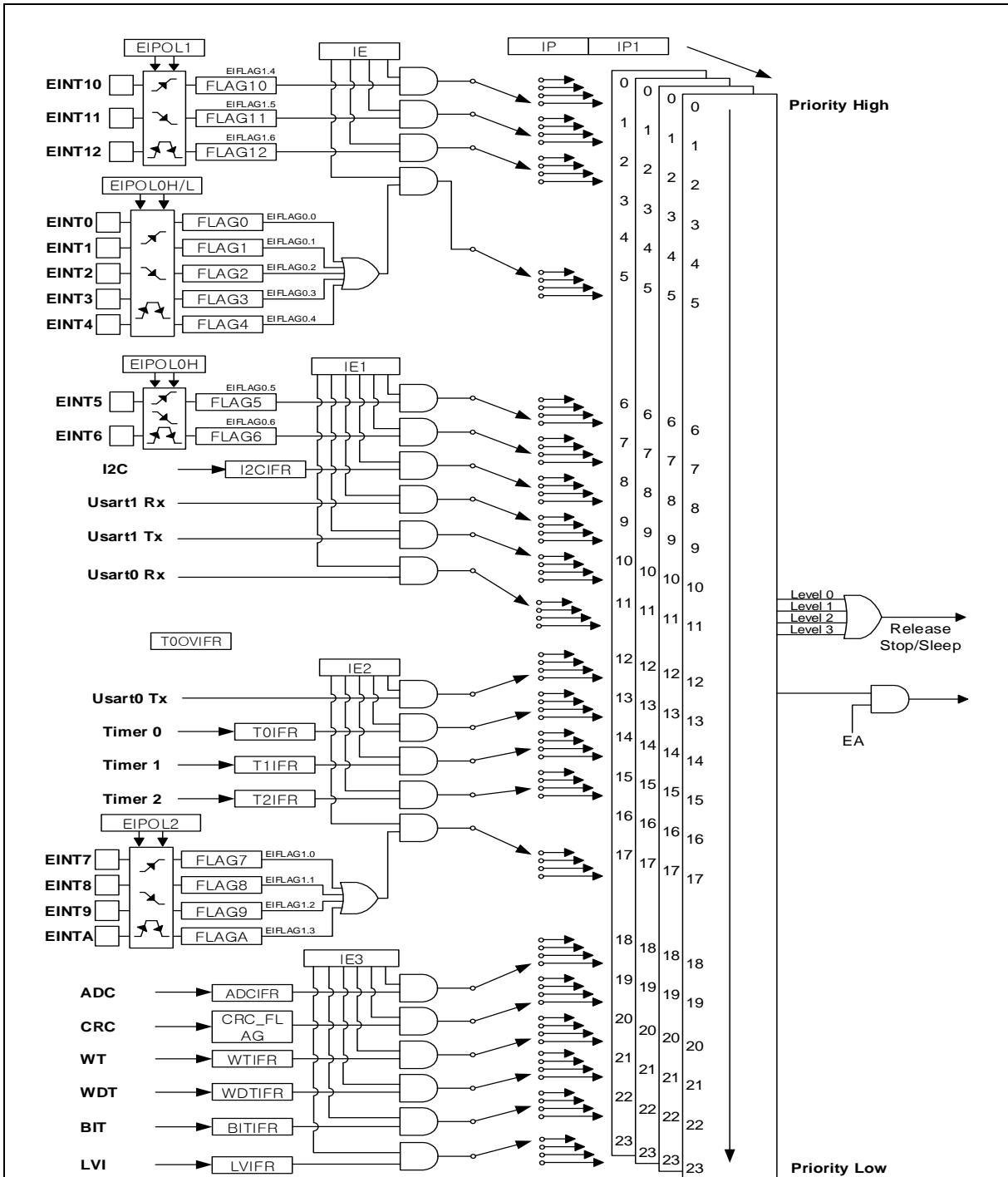
Default interrupt mode is level-trigger mode basically, but if needed, it is possible to change to edge-trigger mode. Figure 16 shows the Interrupt Group Priority Level that is available for sharing interrupt priority. Priority of a group is set by two bits of interrupt priority registers (one bit from IP, another one from IP1). Interrupt service routine serves higher priority interrupt first. If two requests of different priority levels are received simultaneously, the request of higher priority level is served prior to the lower one.

| Interrupt Group | Highest Lowest | | | |
|-----------------|---|--------------|--------------|--------------|
| | → | | | |
| 0 (Bit0) | Interrupt 0 | Interrupt 6 | Interrupt 12 | Interrupt 18 |
| 1 (Bit1) | Interrupt 1 | Interrupt 7 | Interrupt 13 | Interrupt 19 |
| 2 (Bit2) | Interrupt 2 | Interrupt 8 | Interrupt 14 | Interrupt 20 |
| 3 (Bit3) | Interrupt 3 | Interrupt 9 | Interrupt 15 | Interrupt 21 |
| 4 (Bit4) | Interrupt 4 | Interrupt 10 | Interrupt 16 | Interrupt 22 |
| 5 (Bit5) | Interrupt 5 | Interrupt 11 | Interrupt 17 | Interrupt 23 |

Highest
↓
Lowest

Figure 16. Interrupt Group Priority Level

7.1 Block diagram



NOTES:

1. The release signal for stop/idle mode may be generated by all interrupt sources which are enabled without reference to the priority level.
2. An interrupt request is delayed while data are written to IE, IE1, IE2, IE3, IP, IP1, and PCON register.

Figure 17. Interrupt Controller Block Diagram

7.2 Interrupt vector table

Interrupt controller of A96G166/A96A166/A96S166 supports 21 interrupt sources as shown in Table 8. When interrupt is served, long call instruction (LCALL) is executed and program counter jumps to the vector address. All interrupt requests have their own priority order.

Table 8. Interrupt Vector Address Table

| Interrupt source | Symbol | Interrupt Enable Bit | Priority | Mask | Vector address |
|------------------------|--------|----------------------|----------|--------------|----------------|
| Hardware Reset | RESETB | — | 0 | Non-Maskable | 0000H |
| External Interrupt 10 | INT0 | IE.0 | 1 | Maskable | 0003H |
| External Interrupt 11 | INT1 | IE.1 | 2 | Maskable | 000BH |
| External Interrupt 12 | INT2 | IE.2 | 3 | Maskable | 0013H |
| - | INT3 | IE.3 | 4 | Maskable | 001BH |
| - | INT4 | IE.4 | 5 | Maskable | 0023H |
| External Interrupt 0-4 | INT5 | IE.5 | 6 | Maskable | 002BH |
| External Interrupt 5 | INT6 | IE1.0 | 7 | Maskable | 0033H |
| External Interrupt 6 | INT7 | IE1.1 | 8 | Maskable | 003BH |
| I2C Interrupt | INT8 | IE1.2 | 9 | Maskable | 0043H |
| USART1 RX Interrupt | INT9 | IE1.3 | 10 | Maskable | 004BH |
| USART1 TX Interrupt | INT10 | IE1.4 | 11 | Maskable | 0053H |
| USART0 RX Interrupt | INT11 | IE1.5 | 12 | Maskable | 005BH |
| USART0 TX Interrupt | INT12 | IE2.0 | 13 | Maskable | 0063H |
| T0 Match Interrupt | INT13 | IE2.1 | 14 | Maskable | 006BH |
| T1 Match Interrupt | INT14 | IE2.2 | 15 | Maskable | 0073H |
| T2 Match Interrupt | INT15 | IE2.3 | 16 | Maskable | 007BH |
| - | INT16 | IE2.4 | 17 | Maskable | 0083H |
| External Interrupt 7-A | INT17 | IE2.5 | 18 | Maskable | 008BH |
| ADC Interrupt | INT18 | IE3.0 | 19 | Maskable | 0093H |
| CRC Interrupt | INT19 | IE3.1 | 20 | Maskable | 009BH |
| WT Interrupt | INT20 | IE3.2 | 21 | Maskable | 00A3H |
| WDT Interrupt | INT21 | IE3.3 | 22 | Maskable | 00ABH |
| BIT Interrupt | INT22 | IE3.4 | 23 | Maskable | 00B3H |
| LVI Interrupt | INT23 | IE3.5 | 24 | Maskable | 00BBH |

For maskable interrupt execution, the EA bit must be set to '1' and a specific interrupt must be enabled by writing '1' to associated bit in the IEx. If an interrupt request is received, the specific interrupt request flag is set to '1'. And it remains '1' until CPU accepts the interrupt. If the interrupt is served, the interrupt request flag will be cleared automatically.

8 Clock generator

As shown in Figure 18, a clock generator produces basic clock pulses which provide a system clock for CPU and peripheral hardware.

It contains main/sub-frequency clock oscillator. The main/sub clock can operate easily by attaching a crystal between the XIN/SXIN and XOUT/SXOUT pin, respectively. The main/sub clock can be also obtained from the external oscillator. For this, it is necessary to place external clock signal into the XIN/SXIN pin and open XOUT/SXOUT pin.

Default system clock is 16MHz INT-RC Oscillator. To stabilize the system internally, 128kHz LOW INT-RC oscillator on POR is recommended.

Oscillators in the clock generator are introduced in the followings:

- Calibrated high internal RC oscillator (32MHz)
 - HSI OSC/2 (16MHz, default system clock)
 - HSI OSC/4 (8MHz)
 - HSI OSC/8 (4MHz)
 - HSI OSC/16 (2MHz)
 - HSI OSC/32 (1MHz)
 - HSI OSC/64 (0.5MHz)
- Main crystal oscillator (0.4~12MHz)
- Sub-crystal Oscillator (32.768kHz)
- Internal LSI oscillator (128kHz)

8.1 Clock generator block diagram

In this section, a clock generator of A96G166/A96A166/A96S166 is described in a block diagram.

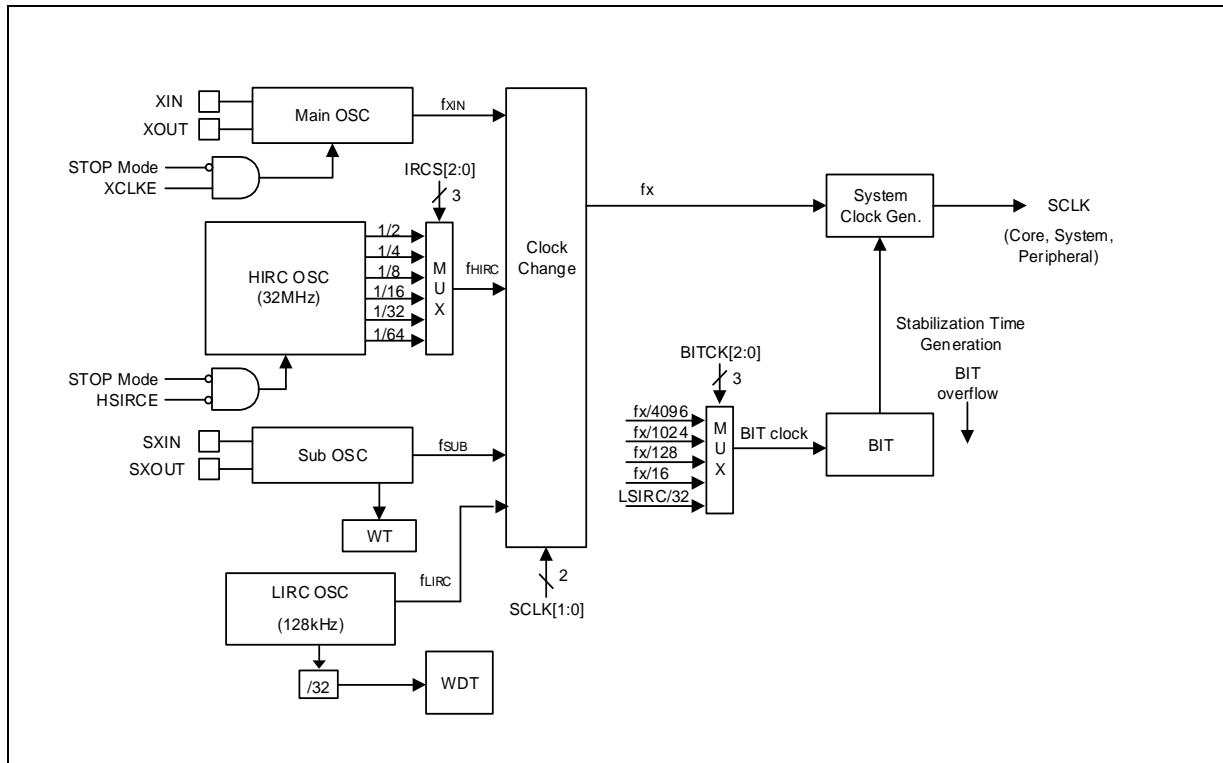


Figure 18. Clock Generator Block Diagram

9 Basic interval timer

A96G166/A96A166/A96S166 has a free running 8-bit Basic Interval Timer (BIT). BIT generates the time base for watchdog timer counting, and provides a basic interval timer interrupt (BITIFR).

BIT of A96G166/A96A166/A96S166 features the followings:

- During Power On, BIT gives a stable clock generation time
- On exiting Stop mode, BIT gives a stable clock generation time
- As a timer, BIT generates a timer interrupt.

9.1 BIT block diagram

In this section, basic interval timer of A96G166/A96A166/A96S166 is described in a block diagram.

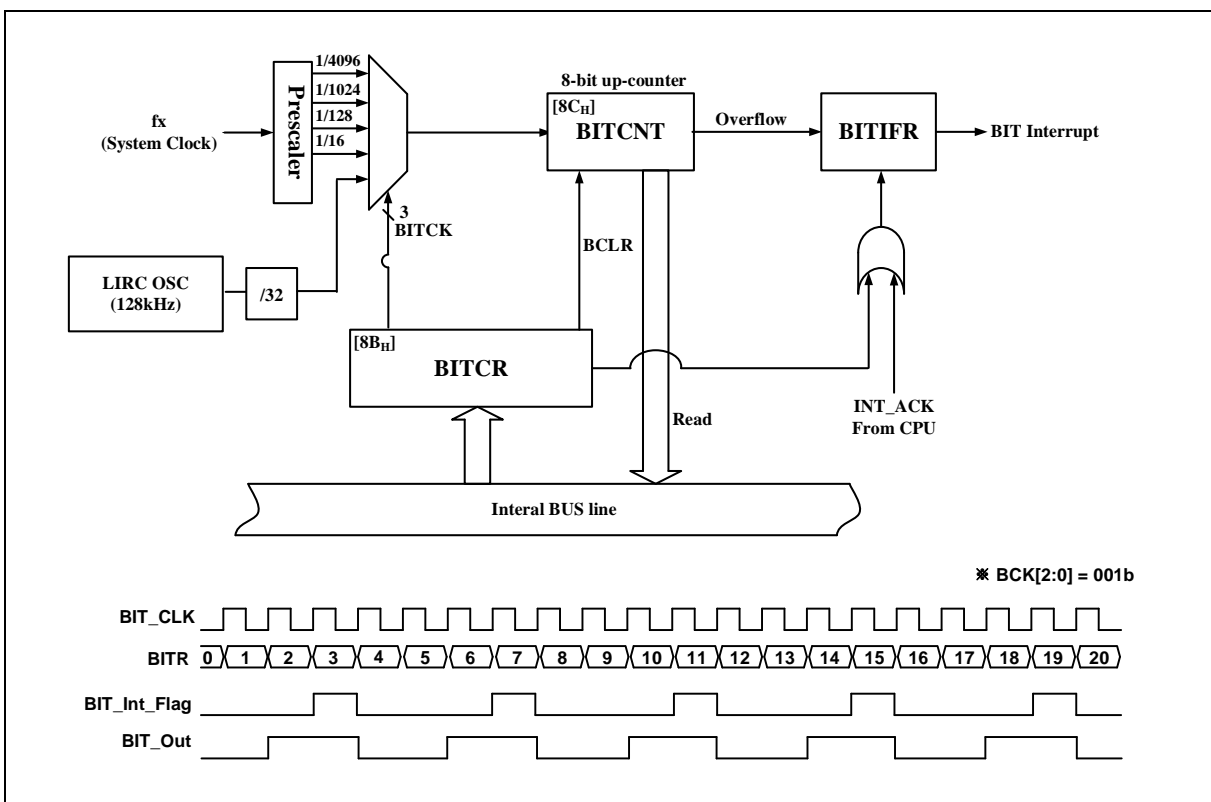


Figure 19. Basic Interval Timer Block Diagram

10 Watchdog timer

The watchdog timer rapidly detects the CPU malfunction such as endless looping caused by noise or something like that, and resumes the CPU to the normal state. The watchdog timer signal for malfunction detection can be used as either a CPU reset or an interrupt request.

When the watchdog timer is not being used for malfunction detection, it can be used as a timer to generate an interrupt at fixed intervals. When 75% of the overflow time is reached, a watchdog interrupt can be generated.

The overflow time of the watchdog timer can select by WDTOVF[2:0] of WDTCR. If an overflow occurs, an internal reset is generated. The WDTRC operation in the STOP/IDLE mode differs as follows depending on the setting value of WDTPDON.

If WDTPDON = 0, the WDTRC operation stop in the STOP/IDLE mode and if WDTPDON = 1, the WDTRC operation in the STOP/IDLE mode. The Watchdog timer operate on the 4kHz, based on clock 128kHz Ring oscillator clock.

Watchdog reset is occurred in the following cases:

- When the watchdog timer counter overflows
- When the data except "96H" is written to the WDTC register
- When the data "96H" is written to the WDTC register during a window close period

10.1 WDT block diagram

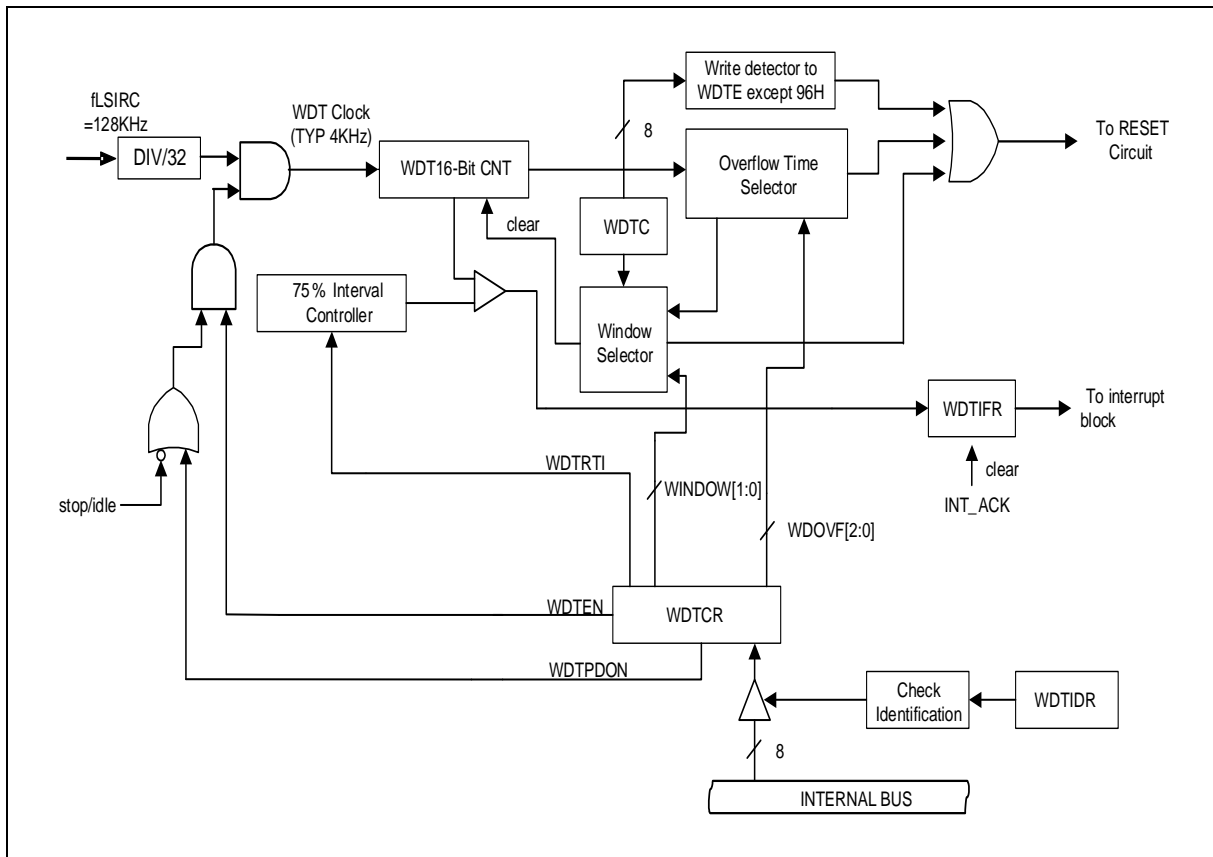


Figure 20. Watch Dog Timer Block Diagram

11 Watch timer

Watch timer (WT) has functions for RTC (Real Time Clock) operation. It is generally used for RTC design. WT consists of a clock source select circuit, a timer counter circuit, an output select circuit and watch timer control registers.

Prior to operate WT, a user needs to determine an input clock source and output interval, and to set WTEN to '1' in watch timer control register (WTCR). It is able to execute simultaneously or individually. To stop or reset WT, clear the WTEN bit in WTCR register.

Although CPU is in STOP mode, a sub clock can be alive so that WT continues its operation. Watch timer counter circuits may be composed of 21-bit counter which contains low 14-bit with binary counter and high 7-bit counter in order to increase resolution. In WTDR, it can control WT clear and set interval value at write time, and it can read 7-bit WT counter value at read time.

11.1 WT block diagram

In this section, watch timer of A96G166/A96A166/A96S166 is described in a block diagram.

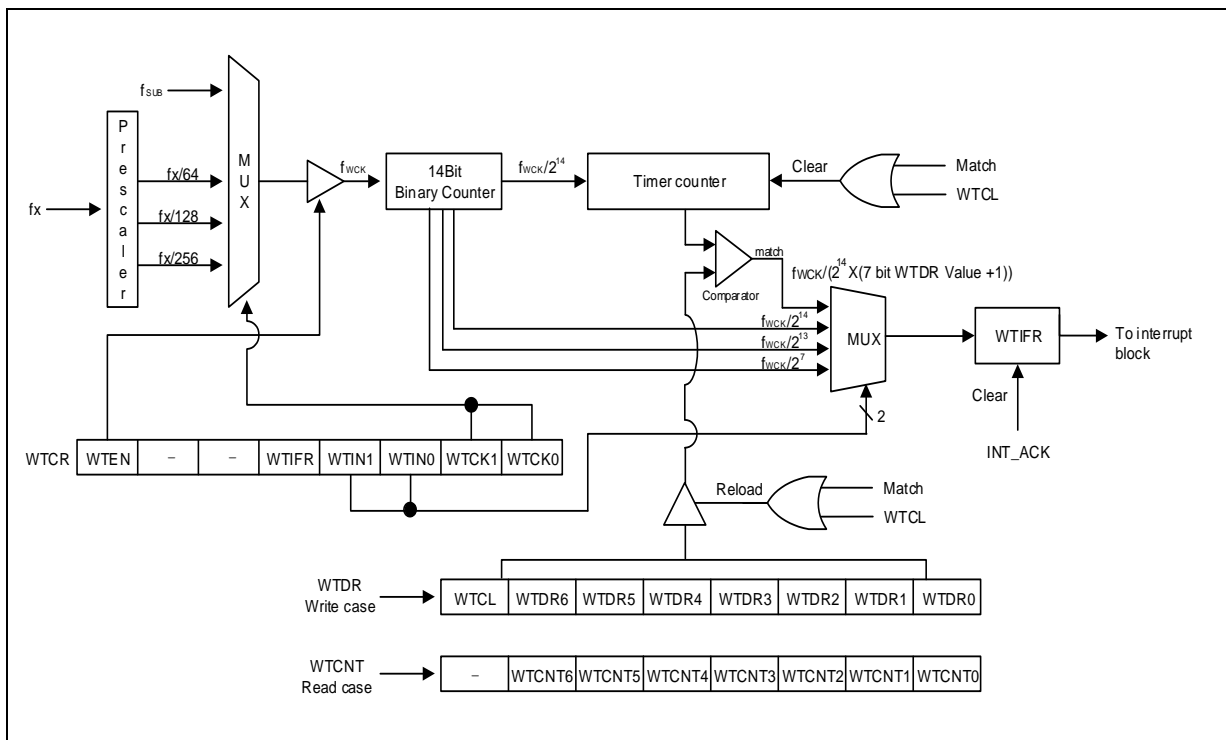


Figure 21. Watch Timer Block Diagram

12 Timer 0/1/2

12.1 Timer 0

An 8-bit timer 0 consists of a multiplexer, a timer 0 counter register, a timer 0 data register, a timer 0 capture data register and a timer 0 control register (T0CNT, T0DR, T0CDR, T0CR).

Timer 0 operates in one of three modes introduced in the followings:

- 8-bit timer/counter mode
- 8-bit PWM output mode
- 8-bit capture mode

Timer/counter 0 can be clocked by an internal or an external clock source (EC0). The clock source is selected by clock selection logic which is controlled by clock selection bits T0CK[2:0].

- TIMER0 clock source: $f_x/2$, $f_x/4$, $f_x/8$, $f_x/32$, $f_x/128$, $f_x/512$, $f_x/2048$ and EC0

In capture mode, data is captured into input capture data register (T0CDR) by EINT10. In timer/counter mode, whenever counter value is equal to T0DR, T0O port toggles. In addition, timer 0 outputs PWM waveform through PWM0O port in the PWM mode.

Table 9. Timer 0 Operating Mode

| T0EN | T0MS[1:0] | T0CK[2:0] | Timer 0 |
|------|-----------|-----------|--------------------------|
| 1 | 00 | XXX | 8-bit Timer/Counter Mode |
| 1 | 01 | XXX | 8-bit PWM Mode |
| 1 | 1X | XXX | 8-bit Capture Mode |

12.1.1 Timer 0 block diagram

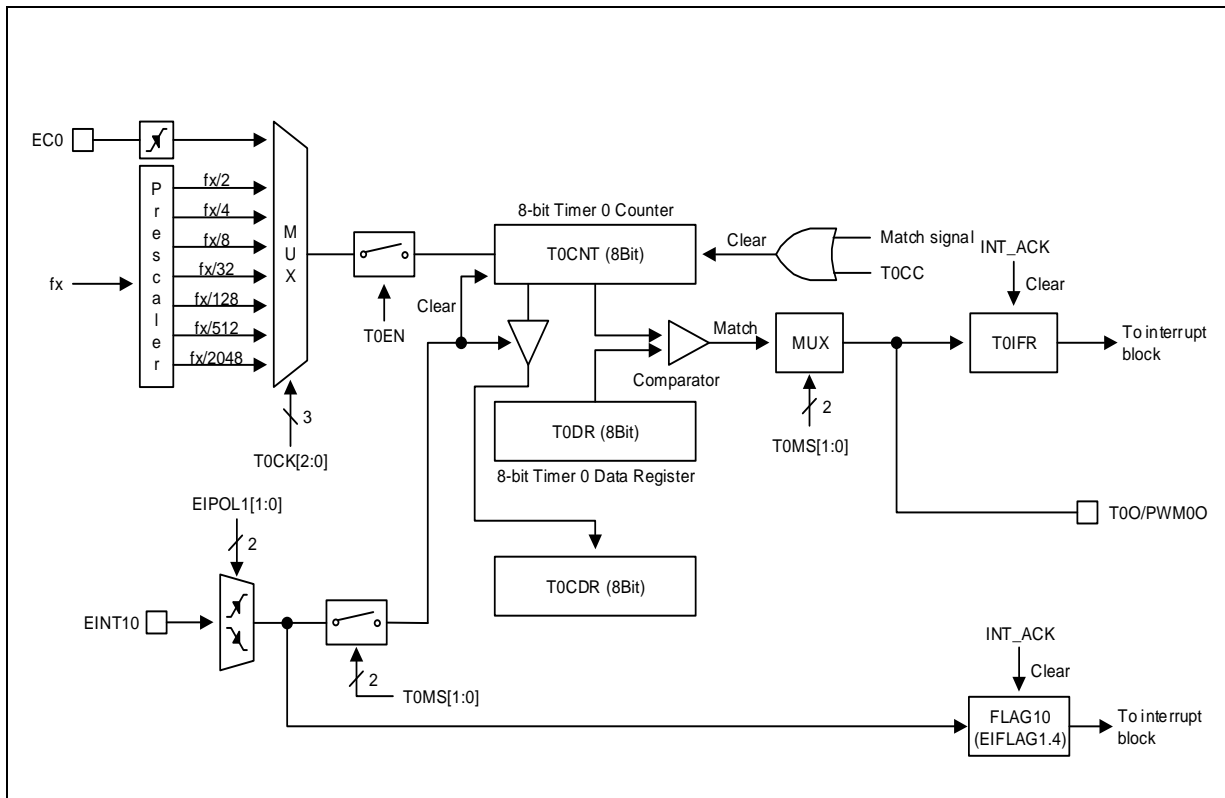


Figure 22. 8-bit Timer 0 Block Diagram

12.2 Timer 1

A 16-bit timer 1 consists of multiplexer, timer 1 A data register high/low, timer 1 B data register high/low and timer 1 control register high/low (T1ADRH, T1ADRL, T1BDRH, T1BDRL, T1CRH, T1CRL).

Timer 1 operates in one of the following modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 1 uses an internal clock or an external clock (EC1) as an input clock source. The clock sources are introduced below, and one is selected by clock selection logic which is controlled by clock selection bits (T1CK[2:0]).

- TIMER 1 clock source: $f_x/1$, $f_x/2$, $f_x/4$, $f_x/8$, $f_x/64$, $f_x/2048$, HSI and EC1

In capture mode, the data is captured into input capture data register (T1BDRH/T1BDRL) by EINT11. Timer 1 results in the comparison between counter and data register through T1O port in timer/counter mode. In addition, Timer 1 outputs PWM waveform through PWM1O port in the PPG mode.

Table 10. TIMER 1 Operating Modes

| T1EN | P1FSRL[5:4] | T1MS[1:0] | T1CK[2:0] | Timer 1 |
|------|-------------|-----------|-----------|--------------------------------|
| 1 | 01 | 00 | XXX | 16 Bit Timer/Counter Mode |
| 1 | 00 | 01 | XXX | 16 Bit Capture Mode |
| 1 | 01 | 10 | XXX | 16 Bit PPG Mode(one-shot mode) |
| 1 | 01 | 11 | XXX | 16 Bit PPG Mode(repeat mode) |

12.2.1 16-bit timer 1 block diagram

In this section, a 16-bit timer 1 is described in a block diagram.

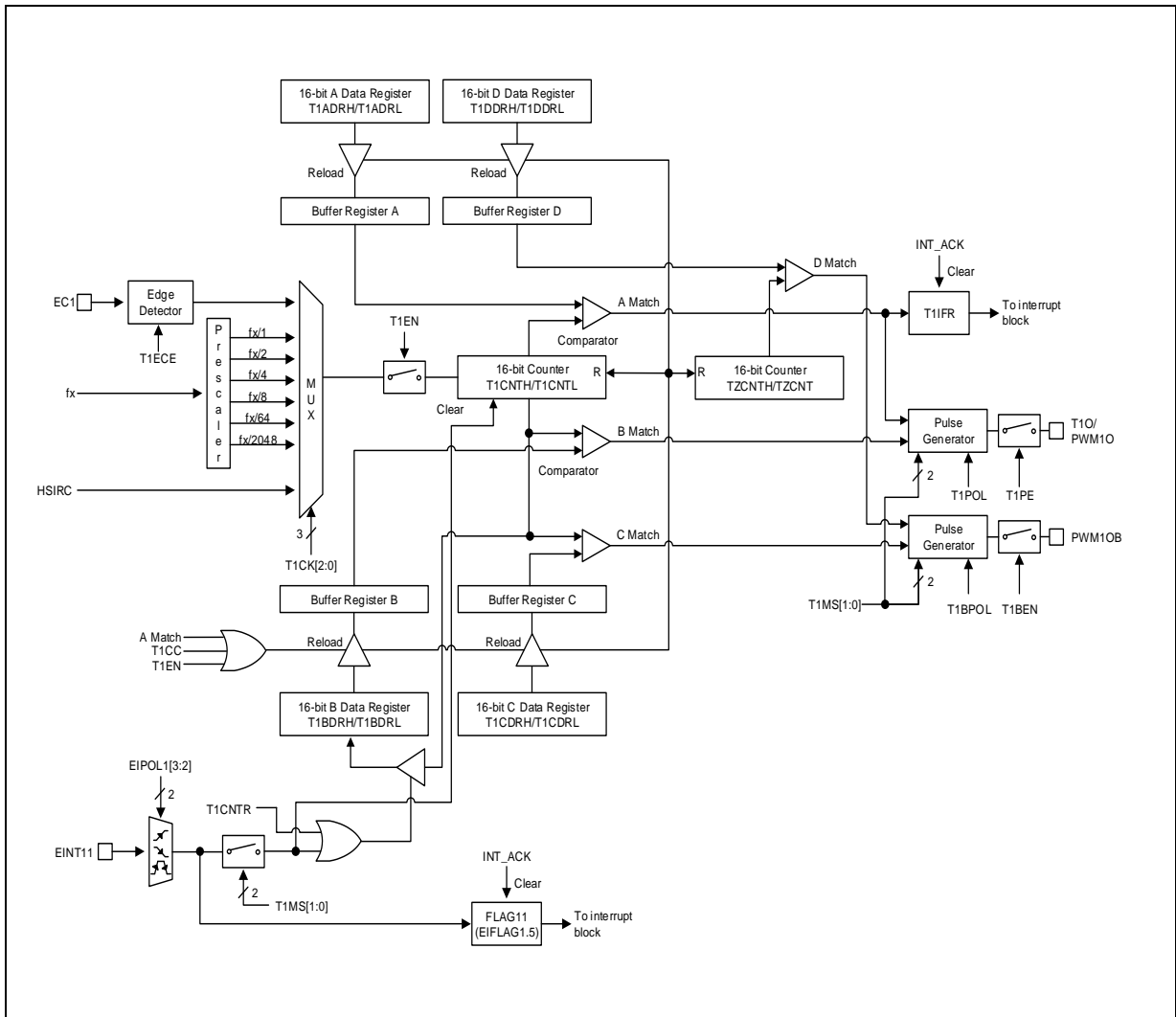


Figure 23. 16-bit Timer 1 Block Diagram

12.3 Timer 2

A 16-bit timer 2 consists of a multiplexer, timer 2 A data high/low register, timer 2 B data high/low register and timer 2 control high/low register (T2ADRH, T2ADRL, T2BDRH, T2BDRL, T2CRH, and T2CRL).

Timer 2 operates in one of the following modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 2 can be a divided clock of a system clock which is selected from prescaler output, external clock(EC2) and T1 A Match (timer 1 A match signal). The clock source is selected by a clock selection logic, controlled by clock selection bits (T2CK[2:0]).

- TIMER 2 clock source: $f_x/1$, $f_x/2$, $f_x/4$, $f_x/8$, $f_x/128$, $f_x/512$, EC2 and T1 A Match

In capture mode, data is captured into input capture data registers (T2BDRH/T2BDRL) by EINT12. In timer/counter mode, whenever counter value is equal to T2ADRH/L, T2O port toggles. In addition, the timer 2 outputs PWM waveform to PWM2O port in the PPG mode.

Table 11. TIMER 2 Operating Modes

| T2EN | P1FSRL[7:6] | T2MS[1:0] | T2CK[2:0] | Timer 2 |
|------|-------------|-----------|-----------|--------------------------------|
| 1 | 01 | 00 | XXX | 16 Bit Timer/Counter Mode |
| 1 | 00 | 01 | XXX | 16 Bit Capture Mode |
| 1 | 01 | 10 | XXX | 16 Bit PPG Mode(one-shot mode) |
| 1 | 01 | 11 | XXX | 16 Bit PPG Mode(repeat mode) |

12.3.1 16-bit timer 2 block diagram

In this section, a 16-bit timer 2 is described in a block diagram.

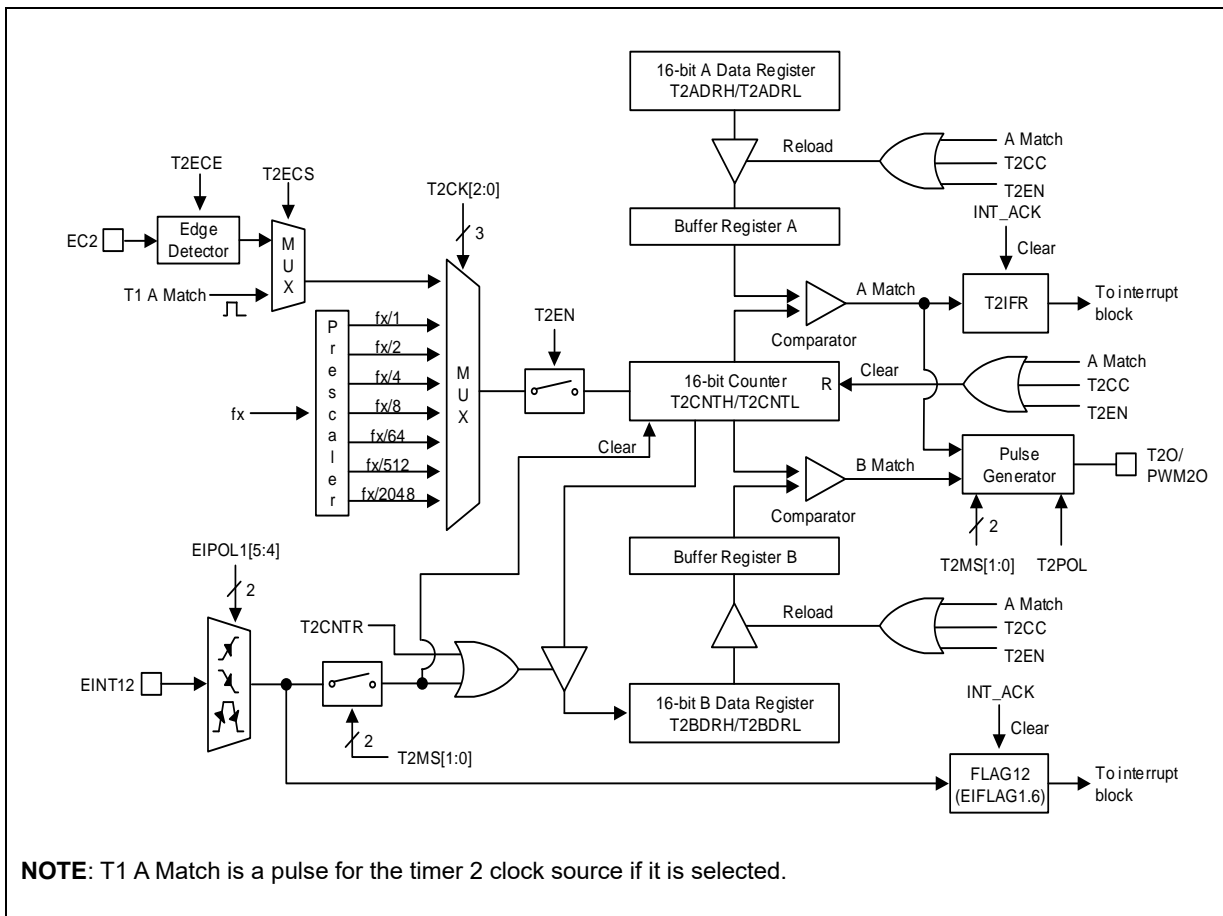


Figure 24. 16-bit Timer 2 Block Diagram

13 Buzzer driver

A buzzer of A96G166/A96A166/A96S166 consists of 8-bit counter, a buzzer data register (BUZDR), and a buzzer control register (BUZCR). It outputs square wave (61.035Hz to 125.0kHz @ 8MHz) through P11/AN8/EINT6/EC1/BUZO pin, and its buzzer data register (BUZDR) controls the buzzer frequency (refer to the following expression). In a buzzer control register (BUZCR), BUCK[2:0] bits select a source clock divided by prescaler.

Table 12. Buzzer Frequency at 8MHz

$$f_{BUZ} \text{ (Hz)} = \frac{\text{Oscillator Frequency}}{2 \times \text{Prescaler Ratio} \times (\text{BUZDR} + 1)}$$

| BUZDR[7:0] | Buzzer Frequency (kHz) | | | |
|------------|------------------------|----------------|----------------|----------------|
| | BUZCR[3:1]=000 | BUZCR[3:1]=001 | BUZCR[3:1]=010 | BUZCR[3:1]=011 |
| 0000_0000 | 125kHz | 62.5kHz | 31.25kHz | 15.625kHz |
| 0000_0001 | 62.5kHz | 31.25kHz | 15.625kHz | 7.812kHz |
| ... | ... | ... | ... | ... |
| 1111_1101 | 492.126Hz | 246.063Hz | 123.031Hz | 61.515Hz |
| 1111_1110 | 490.196Hz | 245.098Hz | 122.549Hz | 61.274Hz |
| 1111_1111 | 488.281Hz | 244.141Hz | 122.07Hz | 61.035Hz |

13.1 Buzzer driver block diagram

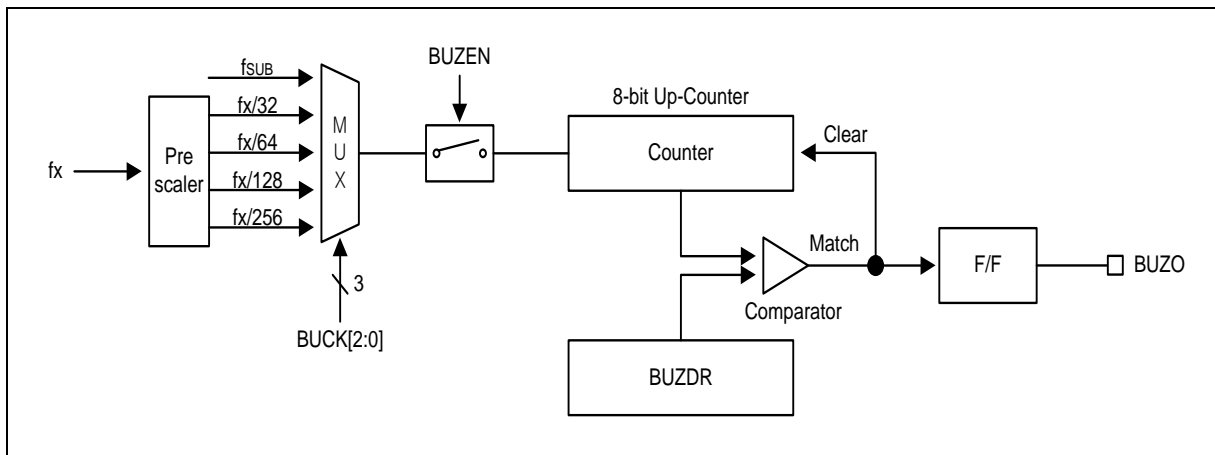


Figure 25. Buzzer Driver Block Diagram

14 12-bit ADC

Analog-to-digital converter (ADC) of A96G166/A96A166/A96S166 allows conversion of an analog input signal to corresponding 12-bit digital value. This A/D module has eight analog inputs. Output of the multiplexer becomes input into the converter which generates the result through successive approximation.

The A/D module has four registers which are the A/D converter control high register (ADCCRH), A/D converter control low register (ADCCRL), A/D converter data high register (ADCDRH), and A/D converter data low register (ADCDRL).

ADSEL[3:0] bits are used to select channels to be converted. To execute A/D conversion, TRIG[2:0] bits should be set to 'xxx'. Registers ADCDRH and ADCDRL contain the result of A/D conversion. When the conversion is completed, the result is loaded into ADCDRH and ADCDRL, A/D conversion status bit AFLAG is set to '1', and A/D interrupt is set. During the A/D conversion, AFLAG bit is read as '0'.

14.1 Block diagram

In this section, the 12-bit ADC is described in a block diagram, and an analog input pin and a power pin with capacitors respectively are introduced.

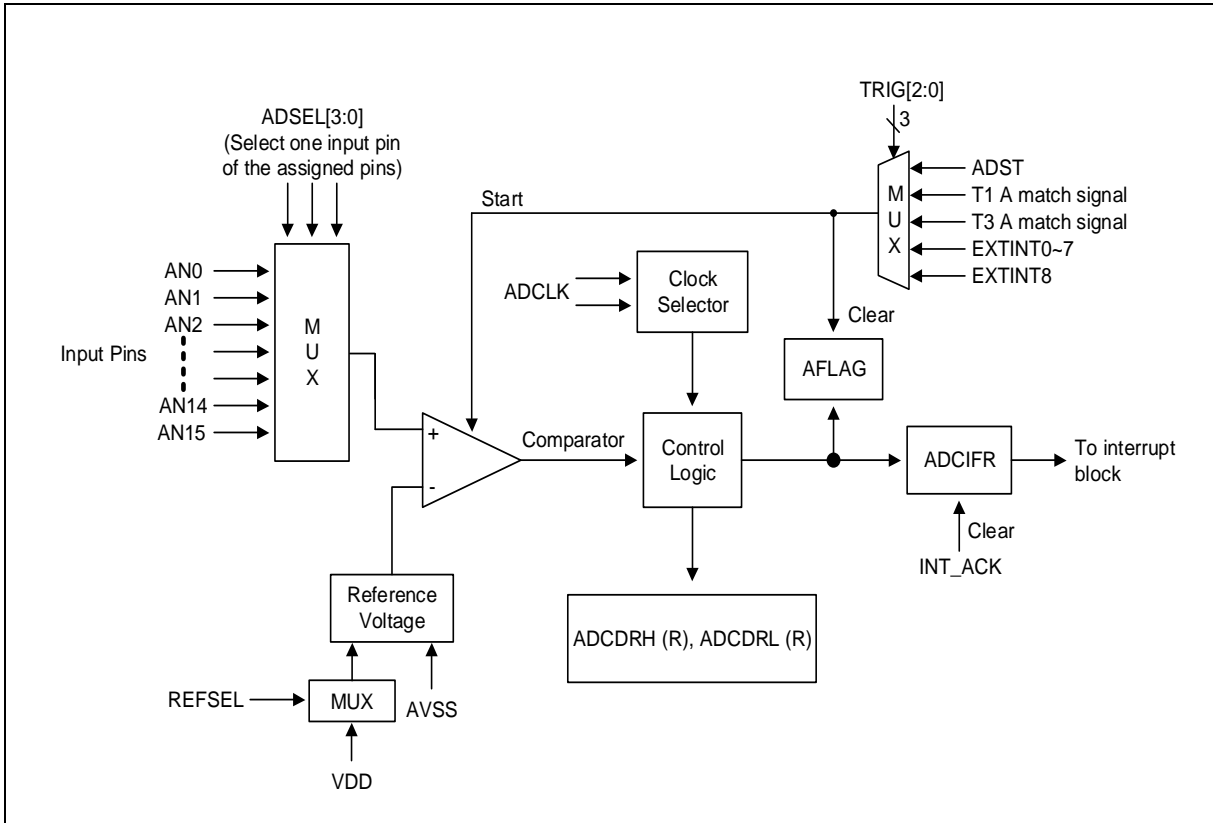


Figure 26. 12-bit ADC Block Diagram

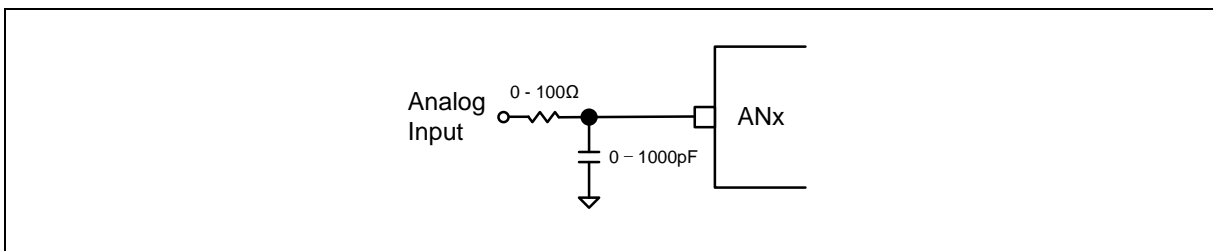


Figure 27. A/D Analog Input Pin with a Capacitor

15 I2C

The I²C is one of industrial standard serial communication protocols, and which uses 2 bus lines Serial Data Line (SDA) and Serial Clock Line (SCL) to exchange data. Because both SDA and SCL lines are open-drain output, each line needs pull-up resistor. The features are as shown below.

- Compatible with I2C bus standard
- Multi-master operation
- Up to 400 kHz data transfer speed
- 7 bit address
- Support 2 slave addresses
- Both master and slave operation
- Bus busy detection

15.1 Block diagram

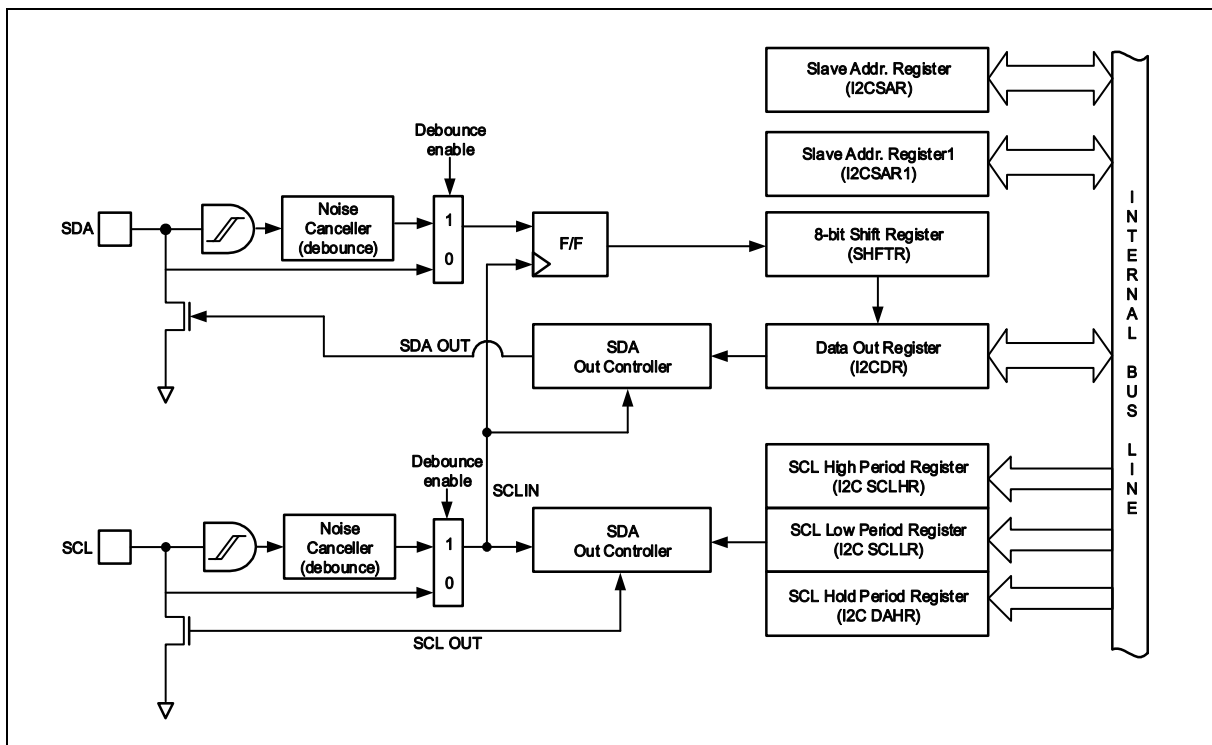


Figure 28. I²C Block Diagram

16 USART 0/1

Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication device. A96G166/A96A166/A96S166 has two USART function blocks, USART0 and USART1, which have the same functionality. The main features are listed below.

- Full duplex operation (Independent Serial Receive and Transmit Registers)
- Asynchronous or synchronous operation
- Master or slave clocked synchronous and SPI operation
- Supports all four SPI modes of operation (mode 0, 1, 2, 3)
- LSB first or MSB first data transfer @SPI mode
- High resolution baud rate generator
- Supports serial frames with 5,6,7,8, or 9 data bits and 1 or 2 stop bits
- Odd or even parity generation and parity check supported by hardware
- Data OverRun detection
- Framing Error detection
- Digital low pass filter
- Three separate interrupts on TX complete, TX data register empty and RX complete
- Double speed asynchronous communication mode

USART has three main parts such as a clock generator, a transmitter and a receiver.

The clock generation logic consists of a synchronization logic for external clock input used by synchronous or SPI slave operation, and a baud rate generator for asynchronous or master (synchronous or SPI) operation.

The transmitter consists of a single write buffer, a serial shift register, parity generator and control logic for handling different serial frame formats. Write buffer allows a continuous transfer of data without any delay between frames.

The receiver is the most complex part of the USART module due to its clock and data recovery units. Recovery unit is used for asynchronous data reception. In addition to the recovery unit, the receiver includes a parity checker, a shift register, a two level receive FIFO (UDATA) and control logic. The receiver supports the same frame formats as the transmitter and can detect Frame Error, Data OverRun and Parity Errors.

16.1 Block diagram

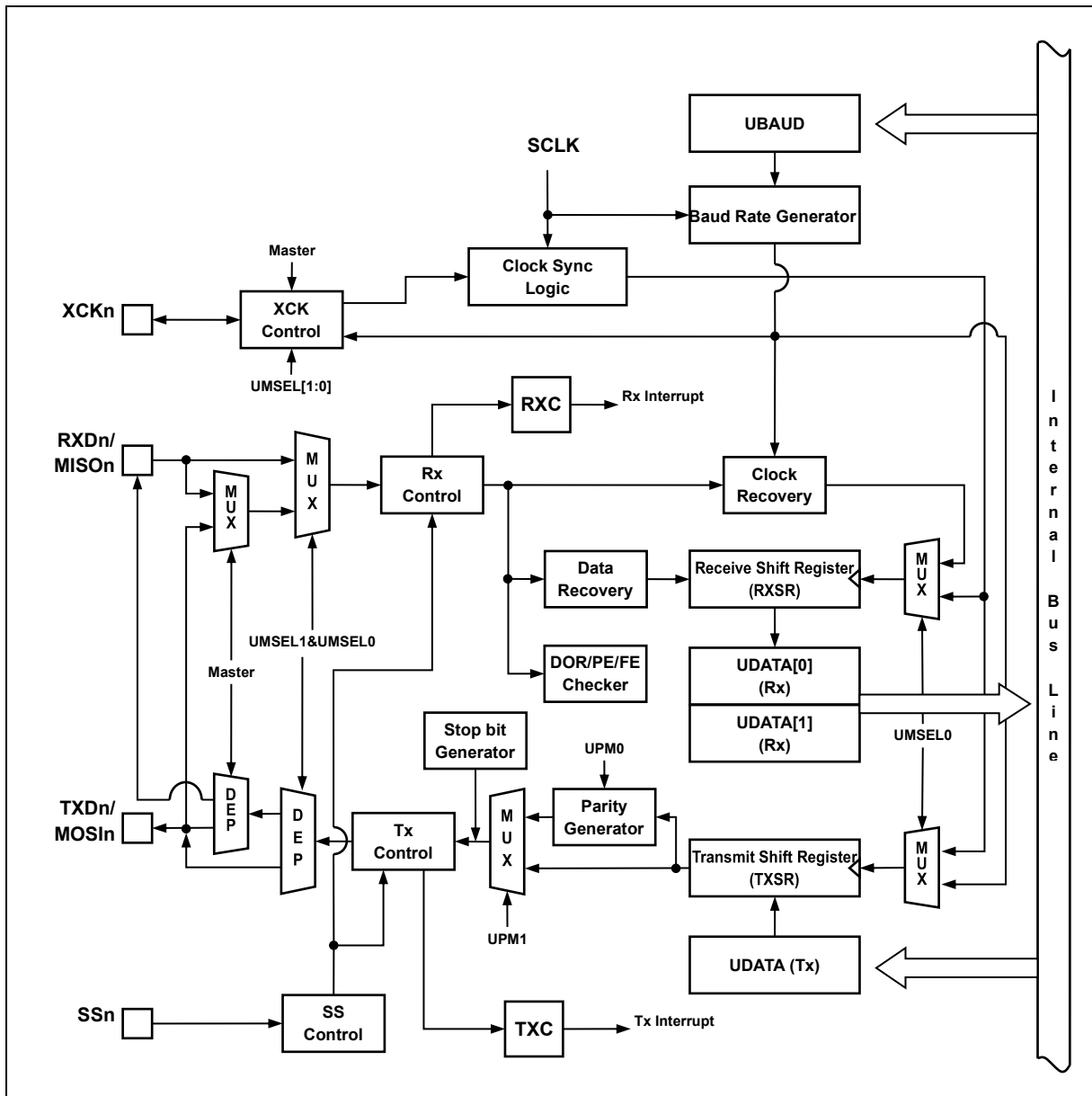


Figure 29. USARTn Block Diagram (n=0, 1)

| | | | | | | | | | |
|----------------|--------|--------|--------|--------|----------|--------|---------|-------|---|
| UnCTRL1 | UMSEL1 | UMSEL0 | UPM1 | UPM0 | USIZE2 | USIZE1 | USIZE0 | UCPOL | ADDRESS: CB _H / F1 _H INITIAL VALUE: 0000_0000 _B |
| UnCTRL2 | UDRIE | TXCIE | RXCIE | WAKEIE | TXE | RXE | USARTEN | U2X | ADDRESS: CC _H / F2 _H INITIAL VALUE: 0000_0000 _B |
| UnCTRL3 | MASTER | LOOPS | DISXCK | SPISS | - | USBS | TX8 | RX8 | ADDRESS: CD _H / F3 _H INITIAL VALUE: 0000_0000 _B |
| UnSTAT | UDRE | TXC | RXC | WAKE | SOFTSRST | DOR | FE | PE | ADDRESS: CF _H / F7 _H INITIAL VALUE: 1000_0000 _B |

17 CRC

Using the CRC, memory of specific area can be monitored. This is a one-time operation, and reset is required for continuous operation. In CRC MNT mode, when the CRC read is finished, CRC_FLAG occurs. In CRC validate mode, if the CRC validate fail after the CRC reading is finished, CRC_FLAG occurs. CRC_FAIL indicates the status of validate results when the CRC read is finished. If the CRC_FLAG is generated and the interrupt is enabled, interrupt service routine is served. CRC-FLAG is not cleared by hardware. CRC-TYPE 0~3 are not supported. Validate is done by comparing the CRC_MNT register and the CRC register value. CRC are not automatically initialized, you need to calculate a new CRC after CRC_H, CRC_L Clear.

Table 13. CRC mode

| CRC TYPE | CRC mode | CRC input | Condition of CRC_FLAG | Condition of CRC reset |
|--------------|----------|------------|-----------------------------------|------------------------|
| CRC_TYPE = 4 | MNT | Flash Data | After CRC reading | - |
| CRC_TYPE = 6 | Validate | Flash Data | After CRC reading & Validate fail | Validate fail |

17.1 Block diagram

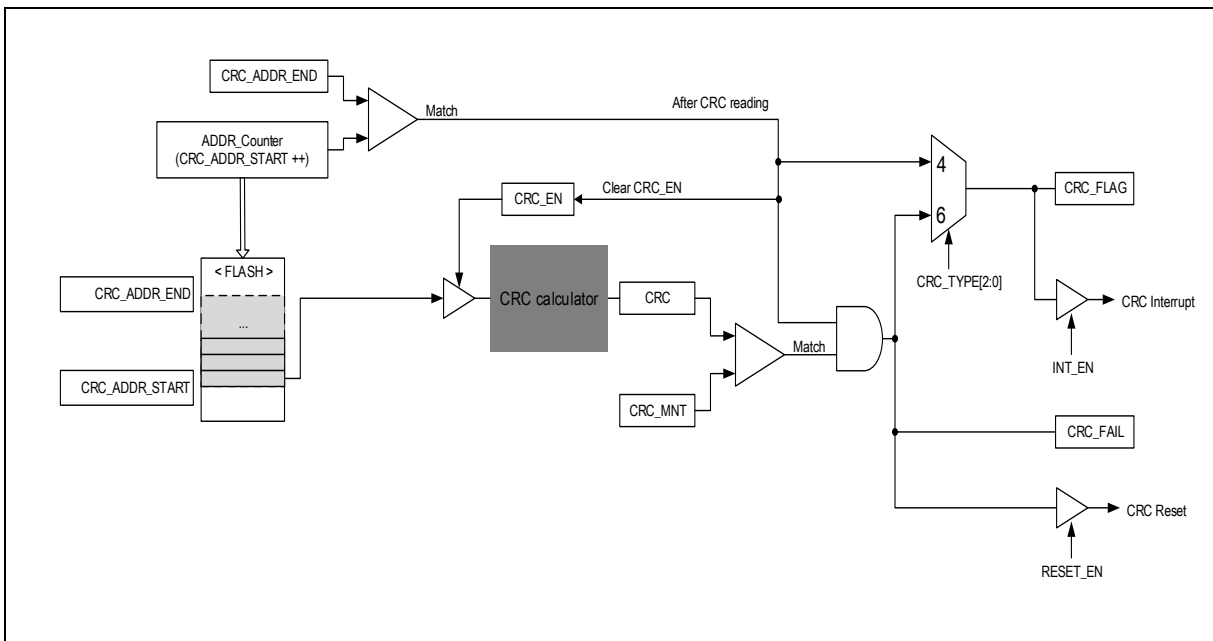


Figure 30. CRC Block Diagram

18 Power down operation

A96G166/A96A166/A96S166 has two power-down modes to minimize the power consumption of the device. In power down mode, power consumption is reduced considerably.

Three power saving functions of A96G166/A96A166/A96S166 are Main-IDLE mode, Sub-IDLE mode and STOP mode. During one of these three modes, program will be stopped.

18.1 Peripheral operation in IDLE/ STOP mode

Table 14 shows operation status of each peripheral in IDLE mode and STOP mode.

Table 14. Peripheral Operation Status during Power-down Mode

| Peripheral | IDLE mode | STOP mode |
|-------------------------|-------------------------------------|---|
| CPU | ALL CPU operations are disabled. | ALL CPU operations are disabled. |
| RAM | Retains. | Retains. |
| Basic Interval Timer | Operates continuously. | Stops (can be operated with WDTRC OSC). |
| Watch Dog Timer | Operates continuously. | Stops (can be operated with WDTRC OSC). |
| Watch Timer | Operates continuously. | Stops (can be operated with sub clock). |
| Timer0/1/2 | Operates continuously. | Halts (only when the event counter mode is enabled, timer operates normally). |
| ADC | Operates continuously. | Stops. |
| BUZ | Operates continuously. | Stops. |
| USART 0/1 | Operates continuously. | Only operates with external clock. |
| I2C | Operates continuously. | Stops. |
| Internal osc (32MHz) | Oscillates. | Stops when the system clock (fx) is fHSI. |
| WDTRC osc (128kHz) | Can be operated with setting value. | Can be operated programmable. |
| Main osc (0.4 to 12MHz) | Oscillates. | Stops when fx = fXIN. |
| Sub osc (32.768kHz) | Oscillates. | Can be operated programmable. |
| I/O Port | Retains. | Retains. |
| Control register | Retains. | Retains. |
| Address data bus | Retains. | Retains. |
| Release method | By RESET All Interrupts | <ul style="list-style-type: none"> • By RESET • Timer Interrupt (EC0, EC1) • External Interrupt • USART 0/1 by RX • WT (sub clock) • WDT • I2C(Slave mode) |

19 Reset

Table 15 shows hardware setting values of main peripherals.

Table 15. Hardware Setting Values in Reset State

| On chip hardware | initial value |
|----------------------|-----------------------------------|
| Program Counter (PC) | 0000h |
| Accumulator | 00h |
| Stack Pointer (SP) | 07h |
| Peripheral Clock | On |
| Control Register | Refer to the peripheral registers |

A96G166/A96A166/A96S166 has five types of reset sources as shown in the followings:

- External RESETB
- Power ON RESET (POR)
- WDT Overflow Reset (In the case of WDTEN = `1`)
- Low Voltage Reset (In the case of LVREN = `0`)
- OCD Reset

19.1 Reset block diagram

In this section, reset unit is described in a block diagram.

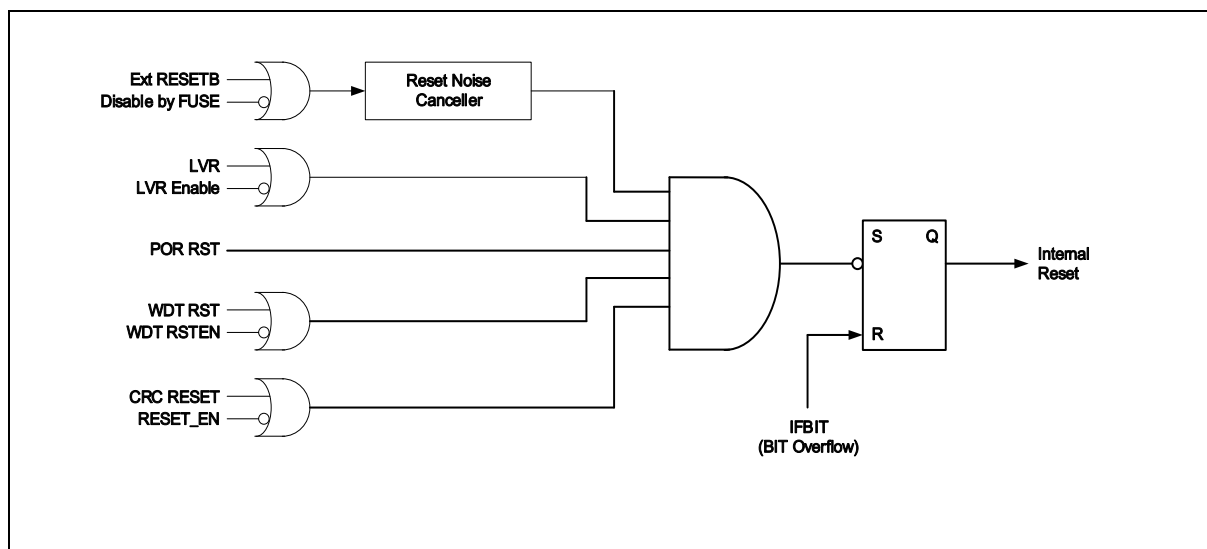


Figure 31. Reset Block Diagram

20 Memory programming

A96G166/A96A166/A96S166 has flash memory to which a program can be written, erased, and overwritten while mounted on the board. Serial ISP mode is supported.

Flash of A96G166/A96A166/A96S166 features the followings:

- Flash Size : 16Kbytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 30,000 program/erase cycles at typical voltage and temperature for flash memory
- Security feature

20.1 Memory map

20.1.1 Flash memory map

Program memory uses 16K bytes of flash memory. It is read by byte and written by byte or page. One page is 32-bytes

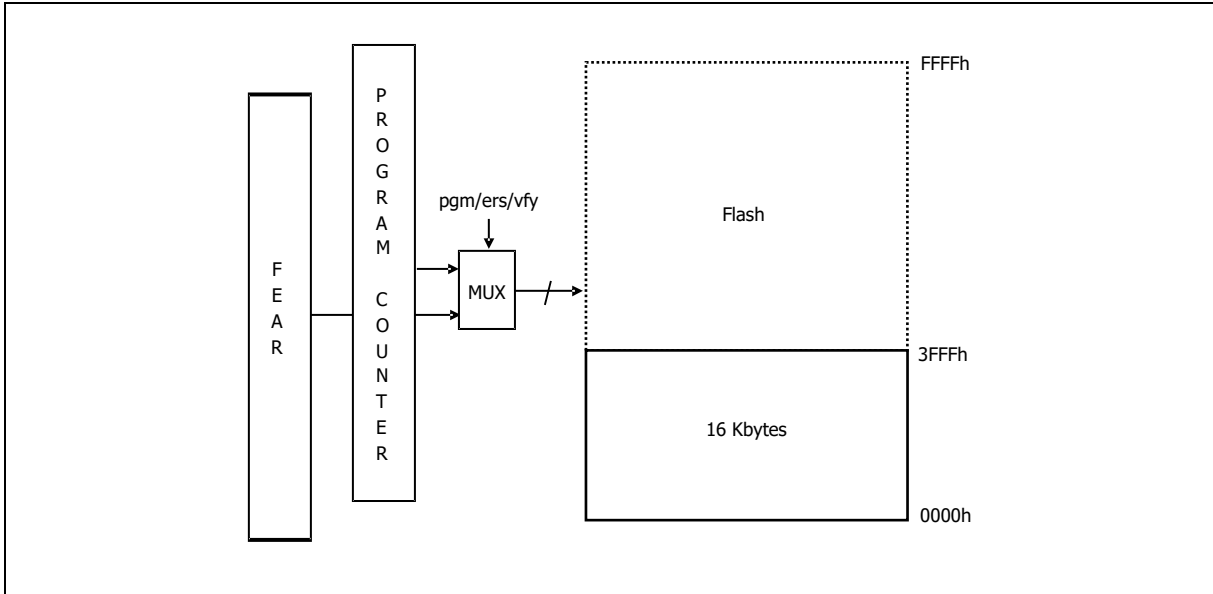


Figure 32. Flash Memory Map

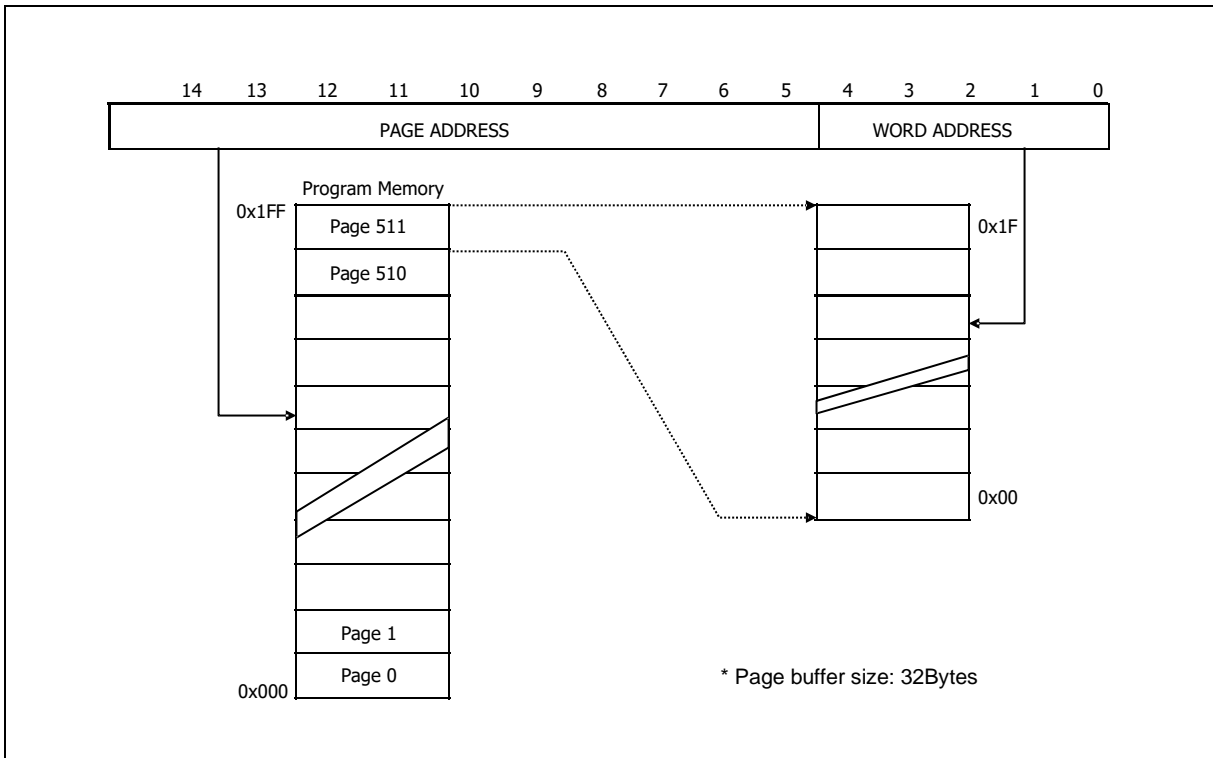


Figure 33. Address Configuration of Flash Memory

21 Electrical characteristics

21.1 Absolute maximum ratings

Table 16. Absolute Maximum Ratings

| Parameter | Symbol | Rating ^{NOTE2} | Unit | Remark |
|-------------------------|-------------------|-------------------------|------|---|
| Supply voltage | VDD | -0.3~+6.5 | V | – |
| Normal voltage pin | V _I | -0.3~VDD+0.3 | V | Voltage on any pin with respect to VSS |
| | V _O | -0.3~VDD+0.3 | V | |
| | I _{OH} | 42.5 | mA | Maximum current output sourced by (I _{OH} per I/O pin) |
| | ∑I _{OH} | 112 | mA | Maximum current (∑I _{OH}) |
| | I _{OL1} | 50 | mA | Maximum current (I _{OL1} per I/O pin) |
| | ∑I _{OL1} | 101 | mA | Maximum current (∑I _{OL1}) |
| | I _{OL2} | 160 | mA | Maximum current sunk by (I _{OL2} per I/O pin) |
| | ∑I _{OL2} | 160 | mA | Maximum current by LED Drive (∑I _{OL2}) |
| Total power dissipation | P _T | 600 | mW | – |
| Storage temperature | T _{STG} | -65~+150 | °C | – |

NOTES:

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The measured value for the parameters and conditions listed were confirmed by simulation.

21.2 Recommended operating conditions

Table 17. Recommended Operating Conditions

(T_A=-40°C ~ 85°C or T_A=-40°C ~ 105°C)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit | |
|-----------------------|------------------|-----------------------------|--------------|-----|-----|------|---|
| Operating Voltage | VDD | f _X = 32 ~ 38kHz | Sub Crystal | 1.8 | – | 5.5 | V |
| | | f _X = 4 ~10MHz | Main Crystal | 2.2 | – | 5.5 | |
| | | f _X = 4 ~12MHz | | 2.4 | – | 5.5 | |
| | | f _X = 0.5~16 MHz | Internal RC | 1.8 | – | 5.5 | |
| Operating Temperature | T _{OPR} | VDD=1.8~5.5V | -40 | – | 85 | °C | |
| | | | -40 | – | 105 | | |

21.3 A/D converter characteristics

Table 18. A/D Converter Characteristics

($T_A = -40^\circ\text{C} \sim +85^\circ\text{C}$ or $T_A = -40^\circ\text{C} \sim 105^\circ\text{C}$, $V_{DD} = 2.2\text{V} \sim 5.5\text{V}$, $V_{SS} = 0\text{V}$)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit | |
|------------------------------|-----------------------------------|----------------------------|-------------------------|-----|-----------------|------|----|
| Integral Linear Error | ILE | AVDD = 5.0V MCLK = 8MHz | – | ±4 | ±8 | LSB | |
| Differential Linearity Error | DLE | | – | ±1 | ±2 | | |
| Offset Error of Top | EOT | | – | ±4 | ±8 | | |
| Offset Error of Bottom | EOB | | – | ±2 | ±4 | | |
| Conversion Time | t _{CON} | 12-bit resolution, 8MHz | 7.5 | – | – | us | |
| Analog Input Voltage | V _{AN} | – | V _{SS} | – | V _{DD} | V | |
| Analog Input Leakage Current | I _{AN} | V _{DDREF} = 5.12V | – | 1 | 2 | uA | |
| ADC Operating Current | I _{ADC} ^{NOTE6} | Enable | V _{DD} = 5.12V | – | 1 | 2 | mA |
| | | Disable | 5.12V | – | – | 0.1 | uA |

NOTES:

1. When VDD is lower than 2.2V, the ADC resolution will get worse.
2. Zero offset error is the difference between 000000000000 and the converted output for zero input voltage (VSS).
3. Full scale error is the difference between 111111111111 and the converted output for full-scale input voltage (VDD).
4. If VDD is less than or equal to 2.2V, the resolution degrades by 1-bit whenever VDD drops 0.1V. (@ADCLK = 0.5MHz, under 2.2V, resolution has no test.)
5. ADCLK must be less than 0.5MHz. Furthermore, if ADCLK is less than 0.125MHz, it can be improved INL characteristic.
6. The measured value for the parameters and conditions listed were confirmed by simulation.

Table 19. Recommended ADC Resolution

($T_A = -40^\circ\text{C} \sim +85^\circ\text{C}$ or $T_A = -40^\circ\text{C} \sim 105^\circ\text{C}$, $V_{DD} = 2.5\text{V} \sim 5.5\text{V}$, $V_{SS} = 0\text{V}$)

| VDD [V] | Resolution | Conditions |
|---------|-----------------------|----------------|
| 2.6 | 12-bit / Upper 12-bit | ADCLK ≤ 0.5MHz |
| 2.5 | 12-bit / Upper 12-bit | |
| 2.4 | 12-bit / Upper 12-bit | |
| 2.3 | 12-bit / Upper 12-bit | |
| 2.2 | 11-bit / Upper 11-bit | |
| 2.1 | 10-bit / Upper 10-bit | |
| 2.0 | 9-bit / Upper 9-bit | |
| 1.9 | 8-bit / Upper 8-bit | |
| 1.8 | 7-bit / Upper 7-bit | |

NOTE: Guaranteed by design.

21.4 VDC1.55 reference voltage characteristics

Table 20. VDC1.55 Reference Voltage Characteristics

($T_A = -40^\circ\text{C} \sim +85^\circ\text{C}$ or $T_A = -40^\circ\text{C} \sim 105^\circ\text{C}$, $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$, $V_{SS} = 0\text{V}$)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|----------------------------|----------|------------|-----|------|-----|------|
| VDC 1.55 Reference Voltage | VDC 1.55 | – | – | 1.55 | – | V |

21.5 Power on reset characteristics

Table 21. Power-on Reset Characteristics

($T_A = -40^\circ\text{C} \sim +85^\circ\text{C}$ or $T_A = -40^\circ\text{C} \sim 105^\circ\text{C}$, $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$, $V_{SS} = 0\text{V}$)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-------------------------|---------------------------|------------|------|------|------|------|
| RESET Release Level | V_{POR} ^{NOTE} | – | – | 1.32 | – | V |
| VDD Voltage Rising Time | t_R ^{NOTE} | – | 0.05 | – | 50.0 | V/ms |
| Minimum Pulse Width | t_{LW} ^{NOTE} | – | 100 | – | – | us |
| POR Current | I_{POR} ^{NOTE} | – | – | 0.2 | – | uA |

NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.

21.6 Low voltage reset and low voltage indicator characteristics

Table 22. LVR and LVI Characteristics

($T_A = -40^\circ\text{C} \sim +85^\circ\text{C}$ or $T_A = -40^\circ\text{C} \sim 105^\circ\text{C}$, $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$, $V_{SS} = 0\text{V}$)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit | |
|---------------------|------------------------|--|-----------------------|------|------|------|----|
| Detection Level | V_{LVR} V_{LVI} | The LVR can select all levels. But LVI can select other levels except 1.61/1.68/1.77V because the minimum operating voltage is 1.8V. V_{LVR}/V_{LVI} can be measured when voltage drops (falling level). | – | 1.61 | 1.75 | V | |
| | | | 1.55 | 1.68 | 1.81 | | |
| | | | 1.63 | 1.77 | 1.91 | | |
| | | | 1.73 | 1.88 | 2.03 | | |
| | | | 1.84 | 2.00 | 2.16 | | |
| | | | 1.96 | 2.13 | 2.30 | | |
| | | | 2.10 | 2.28 | 2.46 | | |
| | | | 2.26 | 2.46 | 2.66 | | |
| | | | 2.47 | 2.68 | 2.89 | | |
| | | | 2.59 | 2.81 | 3.03 | | |
| | | | 2.82 | 3.06 | 3.30 | | |
| | | | 2.95 | 3.21 | 3.47 | | |
| | | | 3.28 | 3.56 | 3.84 | | |
| 3.43 | 3.73 | 4.03 | | | | | |
| 3.60 | 3.91 | 4.22 | | | | | |
| 3.91 | 4.25 | 4.59 | | | | | |
| Hysteresis | ΔV | – | – | 30 | 180 | mV | |
| Minimum Pulse Width | t_{LW} | – | 100 | – | – | us | |
| LVR and LVI Current | I_{BL} | Enable (Both) | VDD= 3V, @RUN Mode | – | 14.0 | 24.0 | uA |
| | | Enable (One of two) | | – | 10.0 | 18.0 | |
| | | Disable (Both) | VDD= 3V | – | – | 0.1 | |

NOTE: Guaranteed by design.

21.7 High speed internal RC oscillator characteristics

Table 23. High speed Internal RC Oscillator Characteristics

($T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ or $T_A = -40^{\circ}\text{C} \sim 105^{\circ}\text{C}$, $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$, $V_{SS} = 0\text{V}$)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--------------------|------------------------|---|-----|-----|------|------|
| Frequency | f_{IRC} | $V_{DD} = 1.8 - 5.5\text{V}$ | – | 32 | – | MHz |
| Tolerance | – | $T_A = 0^{\circ}\text{C}$ to $+50^{\circ}\text{C}$ | – | – | ±1.5 | % |
| | | $T_A = -10^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ | | | ±2.0 | |
| | | $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | | | ±2.5 | |
| | | $T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$ | | | ±5.0 | |
| Clock Duty Ratio | TOD ^{NOTE2} | – | 40 | 50 | 60 | % |
| Stabilization Time | T_{HFS} NOTE2 | – | – | – | 100 | us |
| IRC Current | I_{IRC} | Enable | – | 0.2 | – | mA |
| | | Disable | – | – | 0.1 | uA |

NOTES:

1. A 0.1uF bypass capacitor should be connected to VDD and VSS.
2. The measured value for the parameters and conditions listed were confirmed by simulation.

21.8 Low speed internal RC oscillator characteristics

Table 24. Low speed internal Oscillator Characteristics

($T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ or $T_A = -40^{\circ}\text{C} \sim 105^{\circ}\text{C}$, $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$, $V_{SS} = 0\text{V}$)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--------------------|---------------------------|---|-----|-----|-----|------|
| Frequency | f_{LSI} | $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ | 102 | 128 | 154 | kHz |
| | | $T_A = -40^{\circ}\text{C} \sim +105^{\circ}\text{C}$ | 90 | 128 | 166 | |
| Stabilization Time | T_{LSI} ^{NOTE} | – | – | – | 1 | ms |
| LSI Current | I_{LSI} | Enable | – | 1 | – | uA |
| | | Disable | – | – | 0.1 | |

NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.

21.9 DC characteristics

Table 25. DC Characteristics

 (T_A= -40°C ~ +85°C or T_A=-40°C ~ 105°C, VDD= 1.8V ~ 5.5V, VSS= 0V)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-----------------------------|---|---|----------------|-------|--------|------|
| Input High Voltage | V _{IH} | All input pins | 0.7VDD | – | VDD | V |
| Input Low Voltage | V _{IL} | All input pins | – | – | 0.3VDD | V |
| Output High Voltage | V _{OH1} | VDD=4.5V, I _{OH} =-8.57mA, All output ports; | VDD-1.0 | – | – | V |
| | V _{OH2} | VDD=4.5V, I _{OH} = -19mA, All output ports; | VDD-2.0 | – | – | V |
| Output Low Voltage | V _{OL1} | VDD=4.5V, I _{OL} = 10mA, All output ports except V _{OL2} | – | – | 1.0 | V |
| | V _{OL2} | VDD=4.5V, I _{OL} = 160mA, LEDx High sink current output | – | 1.5 | 3 | V |
| Input High Leakage Current | I _{IH1} | All input ports VDD=5.0V | – | – | 1 | uA |
| Input Low Leakage Current | I _{IL} | All input ports VDD=5.0V | -1 | – | – | uA |
| Pull-Up Resistor | R _{PU1} | VI=0V, T _A = 25°C All Input ports | VDD=5.0V 25 | 50 | 100 | KΩ |
| OSC feedback resistor | R _{X1} | XIN= VSS, XOUT= Floating TA= 25°C, VDD= 5V | 0.76 | 1.3 | 10.51 | MΩ |
| | R _{X2} | SXIN= VSS, SXOUT= Floating TA= 25°C, VDD= 5V | 6.25 | 13.53 | 36.98 | |
| Parameter | Symbol | Condition | MIN | TYP | MAX | Unit |
| Supply Current | I _{DD1} (RUN) | f _{XIN} = 12MHz, VDD= 5V | – | 2.5 | – | mA |
| | | f _{XIN} = 8MHz, VDD= 5V | – | 2.0 | – | |
| | | f _{XIN} = 4MHz, VDD= 5V | – | 1.5 | – | |
| | | f _{HSl} = 16MHz, VDD= 5V | 0.7 | – | 4.0 | |
| | | f _{LSI} = 128kHz, VDD= 5V | – | 190 | – | uA |
| | I _{DD2} (IDLE) | f _{XIN} = 12MHz, VDD= 5V | – | 1.8 | - | mA |
| | | f _{XIN} = 8MHz, VDD= 5V | – | 1.5 | – | |
| | | f _{HSl} = 16MHz, VDD= 5V | 0.5 | – | 3.0 | |
| | | f _{LSI} = 128kHz, VDD= 5V | – | 185 | – | uA |
| | I _{DD3} (STOP1) | STOP @ WDT on, VDD= 5.5V, TA=25°C | – | – | 22 | |
| I _{DD4} (STOP2) | STOP @ WDT off & LVR off, VDD= 5.5V, TA=25°C | – | – | 7 | | |

NOTES:

- Where the f_{XIN} is an external main oscillator, f_{SUB} is an external sub oscillator, the f_{HSl} and f_{LSI} are an internal RC oscillator, and the fx is the selected system clock.
- All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
- All supply current items include the current of the power-on reset (POR) block.

21.10 AC characteristics

Table 26. AC Characteristics

($T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ or $T_A = -40^{\circ}\text{C} \sim 105^{\circ}\text{C}$, $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|----------------------------------|--|---|-----|-----|-----|------|
| RESETB input low width | t_{RSL}^{NOTE} | Input, $V_{DD} = 5\text{V}$ | 50 | – | – | us |
| Interrupt input high, low width | t_{INTH}^{NOTE} , t_{INTL}^{NOTE} | All interrupt, $V_{DD} = 5\text{V}$ | 200 | – | – | ns |
| | t_{ECWH}^{NOTE} , t_{ECWL}^{NOTE} | EC_n , $V_{DD} = 5\text{V}$ ($n = 0, 1, 2$) | 200 | – | – | |
| External Counter Transition Time | t_{REC}^{NOTE} , t_{FEC}^{NOTE} | EC_n , $V_{DD} = 5\text{V}$ ($n = 0, 1, 2$) | 20 | – | – | |

NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.

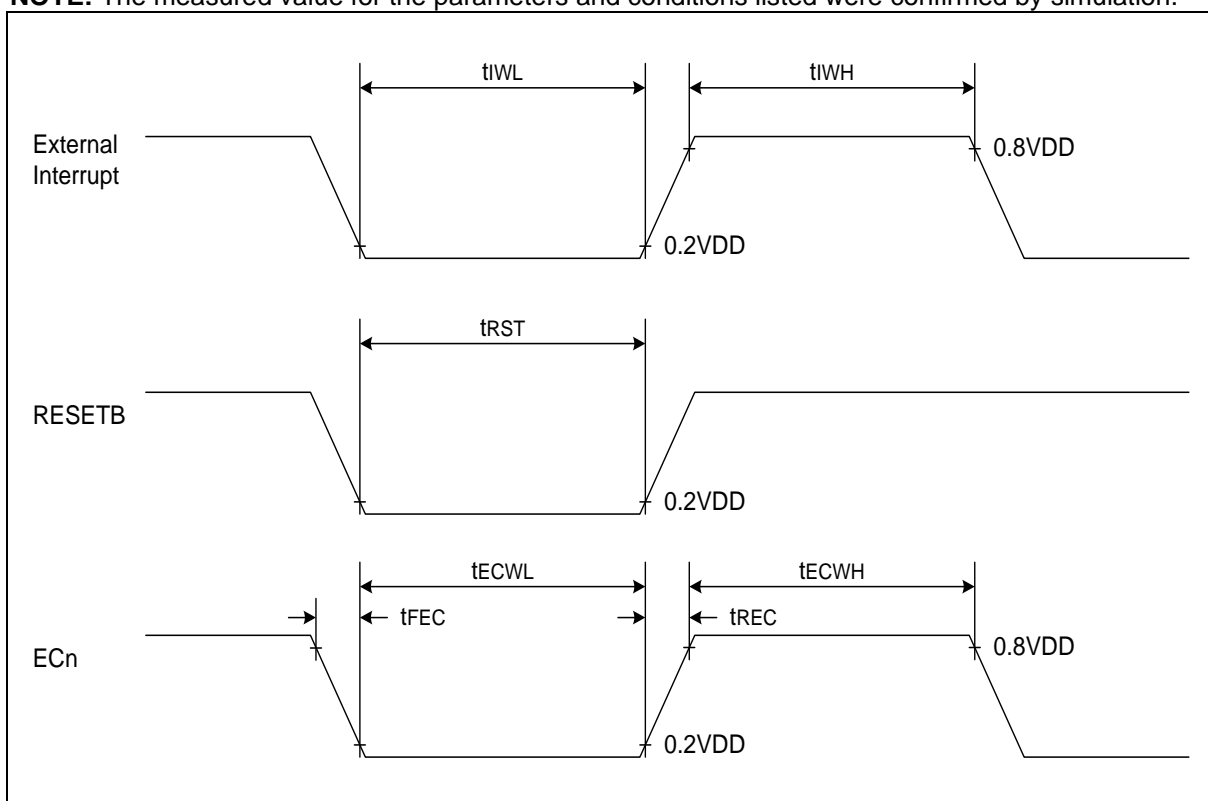


Figure 34. AC Timing

21.11 USART characteristics

The following table and figures show USART timing condition in SPI or Synchronous mode operation.

Table 27. USART Timing Characteristics in SYNC. or SPI Mode Operations

($T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ or $T_A = -40^{\circ}\text{C} \sim 105^{\circ}\text{C}$, $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$)

| Parameter | | Symbol | MIN | MAX | Unit |
|-----------------------------------|--------|------------|----------------------|------------------------|------|
| System clock period(0.5MHz~16MHz) | | t_{SCLK} | 62.5 | 2000 | ns |
| Clock (XCK) period | | t_{XCK} | $4 \times t_{SCLK}$ | $1028 \times t_{SCLK}$ | ns |
| Clock (XCK) high time | | t_{XCKH} | $2 \times t_{SCLK}$ | $514 \times t_{SCLK}$ | ns |
| Clock (XCK) low time | | t_{XCKL} | $2 \times t_{SCLK}$ | $514 \times t_{SCLK}$ | ns |
| Lead time | Master | t_{LEAD} | $0.5 \times t_{XCK}$ | $0.5 \times t_{XCK}$ | ns |
| | Slave | t_{LEAD} | $2 \times t_{SCLK}$ | — | |
| Lag time | Master | t_{LAG} | $0.5 \times t_{XCK}$ | $0.5 \times t_{XCK}$ | ns |
| | Slave | t_{LAG} | $2 \times t_{SCLK}$ | — | |
| Data setup time (inputs) | Master | t_{SIM} | $2 \times t_{SCLK}$ | $2 \times t_{SCLK}$ | ns |
| | Slave | t_{SIS} | $2 \times t_{SCLK}$ | $2 \times t_{SCLK}$ | |
| Data hold time (inputs) | Master | t_{HIM} | 10 | — | ns |
| | Slave | t_{HIS} | 10 | — | |
| Data setup time (outputs) | Master | t_{SOM} | $2 \times t_{SCLK}$ | $2 \times t_{SCLK}$ | ns |
| | Slave | t_{SOS} | $2 \times t_{SCLK}$ | $2 \times t_{SCLK}$ | |
| Data hold time (outputs) | Master | t_{HOM} | -10 | — | ns |
| | Slave | t_{HOS} | -10 | — | |
| Disable time | | t_{DIS} | $1 \times t_{SCLK}$ | $2 \times t_{SCLK}$ | ns |

NOTE:

1. In synchronous mode, Lead and Lag time for SS pin is ignored. And the case of "UCPHA=0" is also only applied to SPI mode
2. All timing is shown between 20% VDD and 80% VDD.

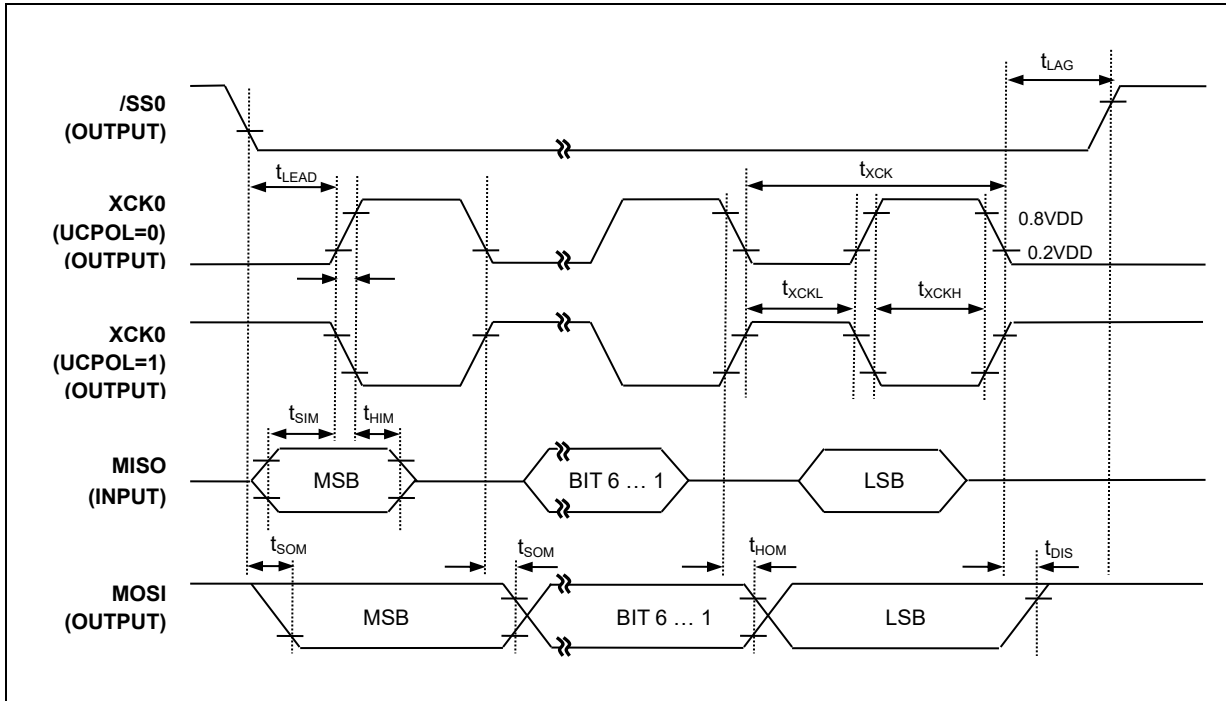
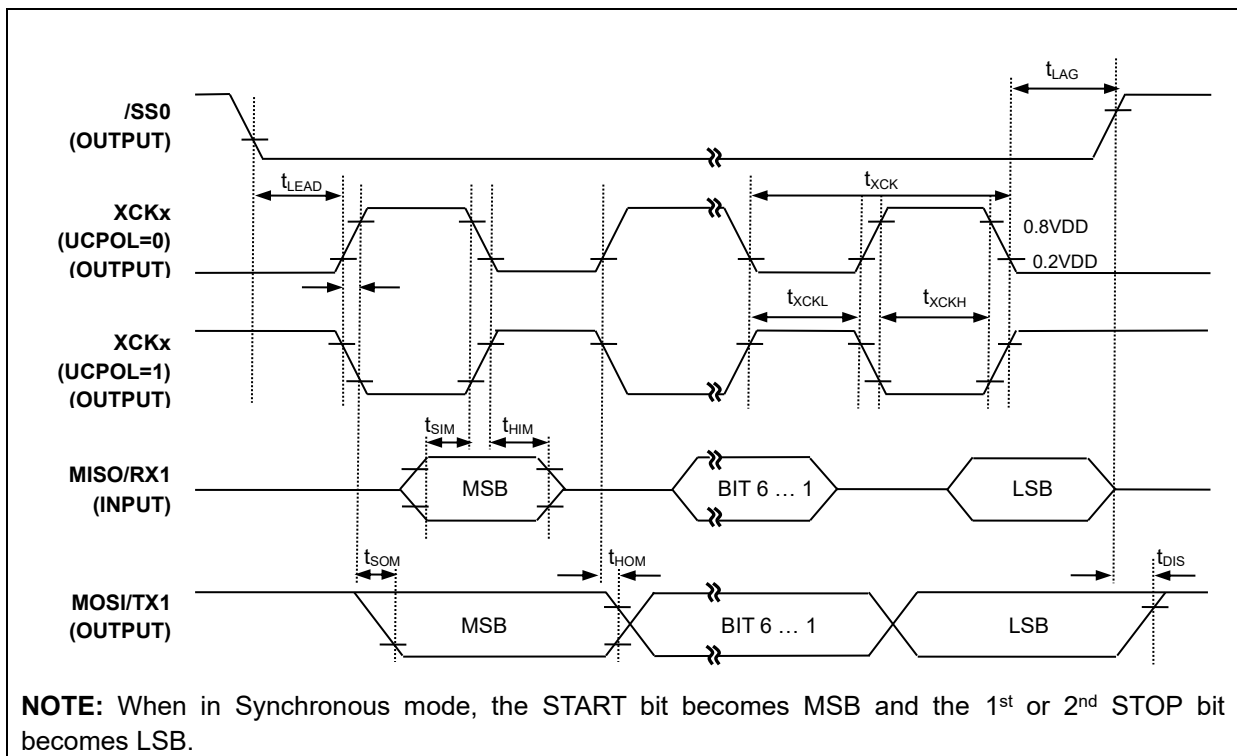


Figure 35. SPI master mode timing (UCPHA = 0, MSB first)



NOTE: When in Synchronous mode, the START bit becomes MSB and the 1st or 2nd STOP bit becomes LSB.

Figure 36. SPI/Synchronous master mode timing (UCPHA = 1, MSB first)

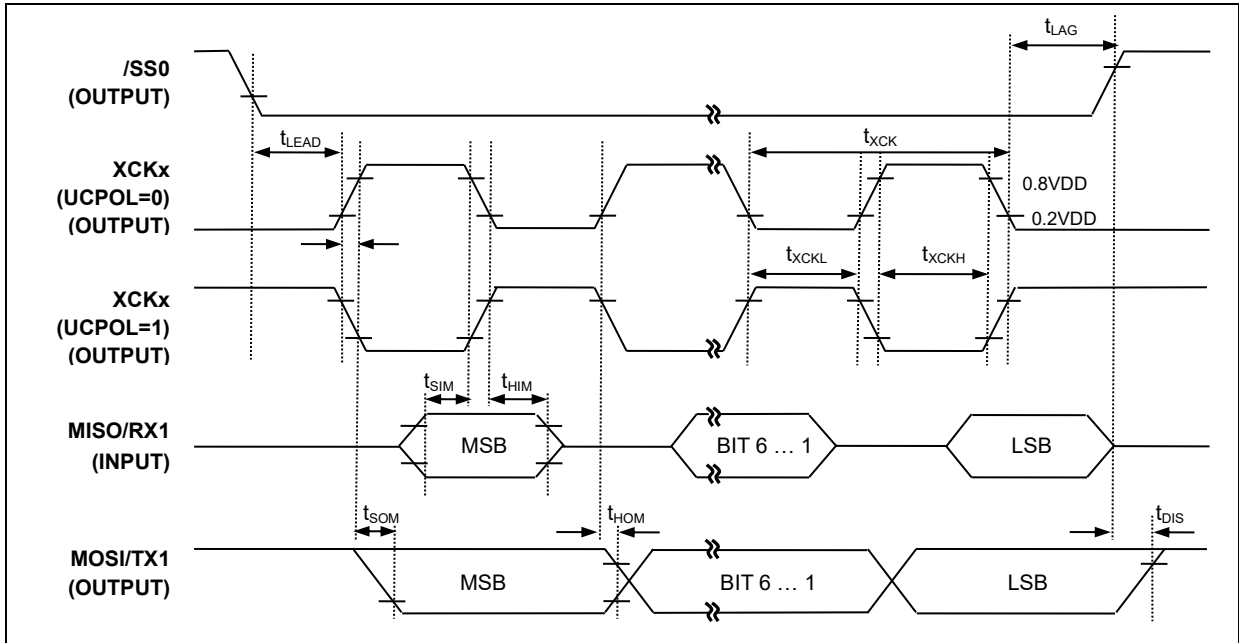
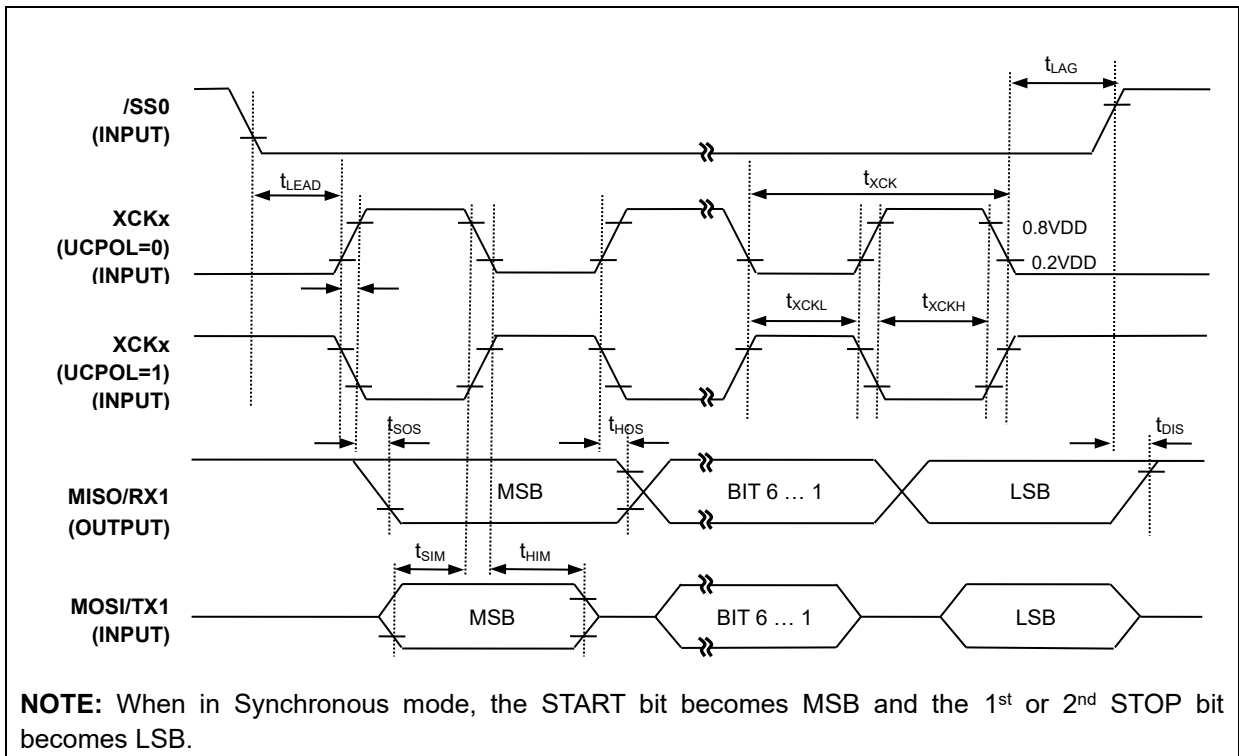


Figure 37 SPI slave mode timing (UCPHA = 0, MSB first)



NOTE: When in Synchronous mode, the START bit becomes MSB and the 1st or 2nd STOP bit becomes LSB.

Figure 38 SPI/Synchronous slave mode timing (UCPHA = 1, MSB first)

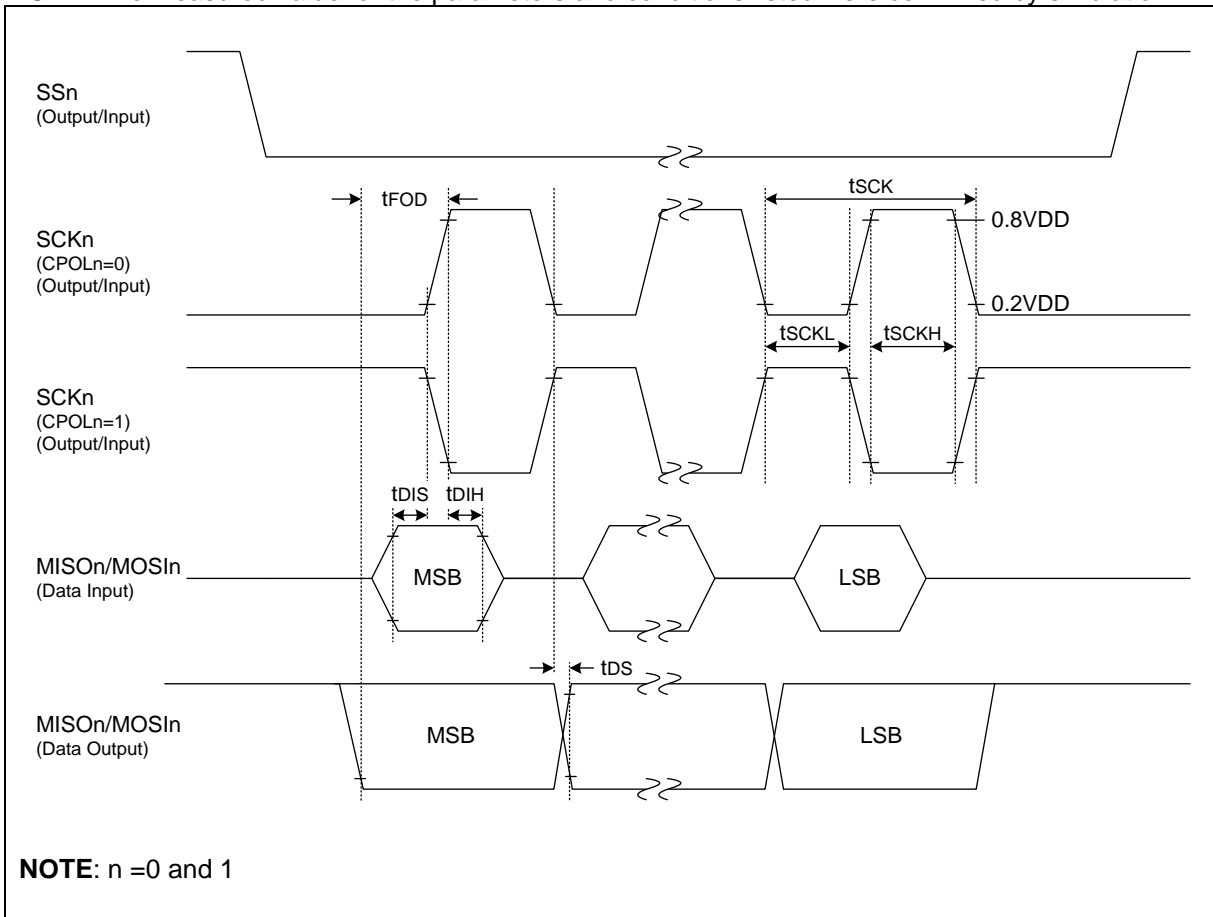
21.12 SPI characteristics

Table 28. SPI Characteristics

($T_A = -40^{\circ}\text{C} - +85^{\circ}\text{C}$ or $T_A = -40^{\circ}\text{C} \sim 105^{\circ}\text{C}$, $V_{DD} = 1.8\text{V} - 5.5\text{V}$)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|------------------------------------|---|------------------------------|-----|-----|-----|------|
| Output Clock Pulse Period | tSCK ^{NOTE} | Internal SCK source | 200 | – | – | ns |
| Input Clock Pulse Period | | External SCK source | 200 | – | – | ns |
| Output Clock High, Low Pulse Width | tSCKH ^{NOTE} , tSCKL ^{NOTE} | Internal SCK source | 70 | – | – | ns |
| Input Clock High, Low Pulse Width | | External SCK source | 70 | – | – | ns |
| First Output Clock Delay Time | tFOD ^{NOTE} | Internal/External SCK source | 100 | – | – | ns |
| Output Clock Delay Time | tDS ^{NOTE} | – | – | – | 50 | ns |
| Input Setup Time | tDIS ^{NOTE} | – | 100 | – | – | ns |
| Input Hold Time | tDIH ^{NOTE} | – | 150 | – | – | ns |

NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.



NOTE: n = 0 and 1

Figure 39. SPI0/1 Timing

21.13 I2C characteristics

Table 29. I2C Characteristics

($T_A = -40^\circ\text{C} \sim +85^\circ\text{C}$ or $T_A = -40^\circ\text{C} \sim 105^\circ\text{C}$, $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$, $f_{XIN} = 8\text{MHz}$)

| Parameter | Symbol | Standard Mode | | High-Speed Mode | | Unit | |
|----------------------------|--------------------------|---------------|-----|-----------------|-----|------|----|
| | | Min | Max | Min | Max | | |
| Clock frequency | t_{SCL}^{NOTE} | 0 | 100 | 0 | 400 | kHz | |
| Clock High Pulse Width | t_{SCLH}^{NOTE} | 4.0 | – | 0.6 | – | us | |
| Clock Low Pulse Width | t_{SCLL}^{NOTE} | 4.7 | – | 1.3 | – | | |
| Bus Free Time | t_{BF}^{NOTE} | 4.7 | – | 1.3 | – | | |
| Start Condition Setup Time | t_{STSU}^{NOTE} | 4.7 | – | 0.6 | – | | |
| Start Condition Hold Time | t_{STHD}^{NOTE} | 4.0 | – | 0.6 | – | | |
| Stop Condition Setup Time | t_{SPSU}^{NOTE} | 4.0 | – | 0.6 | – | | |
| Stop Condition Hold Time | t_{SPHD}^{NOTE} | 4.0 | – | 0.6 | – | | |
| Output Valid from Clock | t_{VD}^{NOTE} | 0 | – | 0 | – | | |
| Data Input Hold Time | t_{DIH}^{NOTE} | 0 | – | 0 | 1.0 | | |
| Data Input Setup Time | t_{DIS}^{NOTE} | 250 | – | 100 | – | | |
| | | | | | | | ns |

NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.

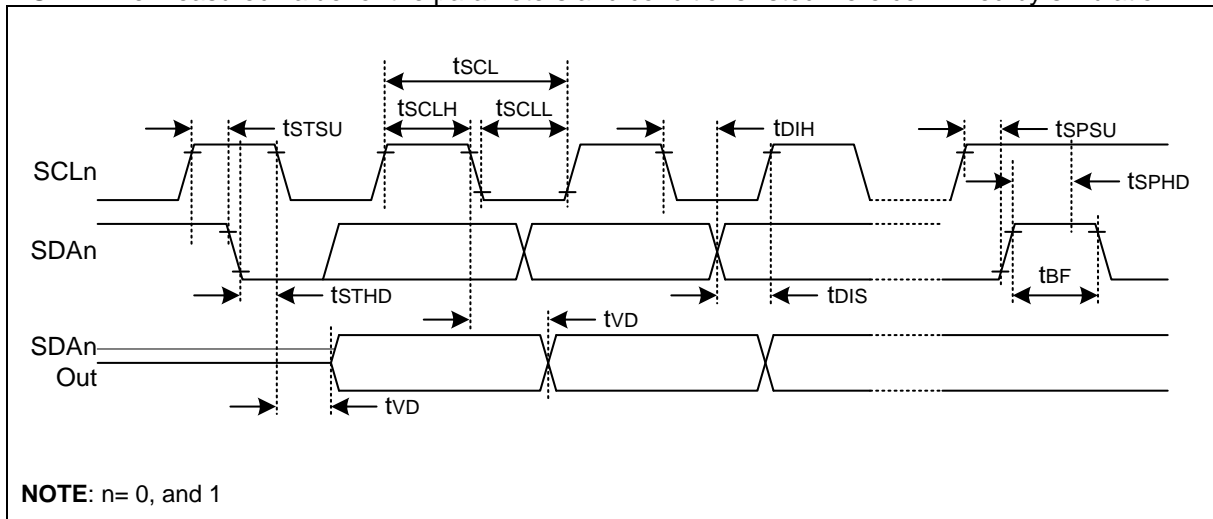


Figure 40. I2C Timing

21.14 Data retention voltage in stop mode

Table 30. Data Retention Voltage in Stop Mode

($T_A = -40^\circ\text{C} \sim +85^\circ\text{C}$ or $T_A = -40^\circ\text{C} \sim 105^\circ\text{C}$, $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-------------------------------|------------|--|-----|-----|-----|---------------|
| Data retention supply voltage | V_{DDDR} | – | 1.8 | – | 5.5 | V |
| Data retention supply current | I_{DDDR} | $V_{DDR} = 1.8\text{V}$ ($T_A = 25^\circ\text{C}$), Stop mode | – | – | 1 | μA |

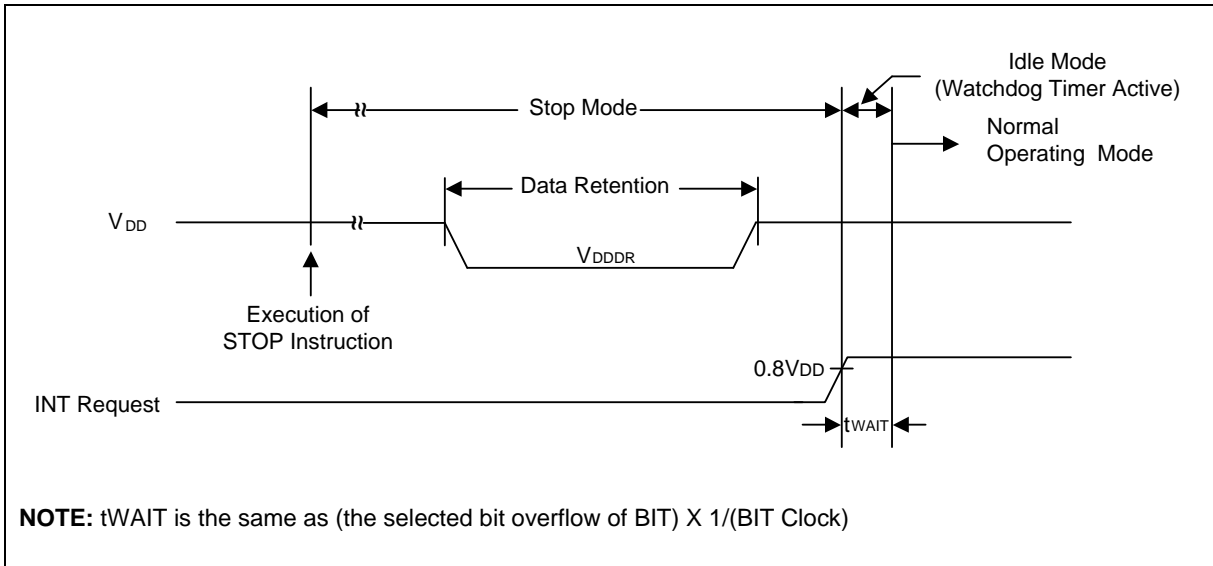


Figure 41. Stop Mode Release Timing when Initiated by an Interrupt

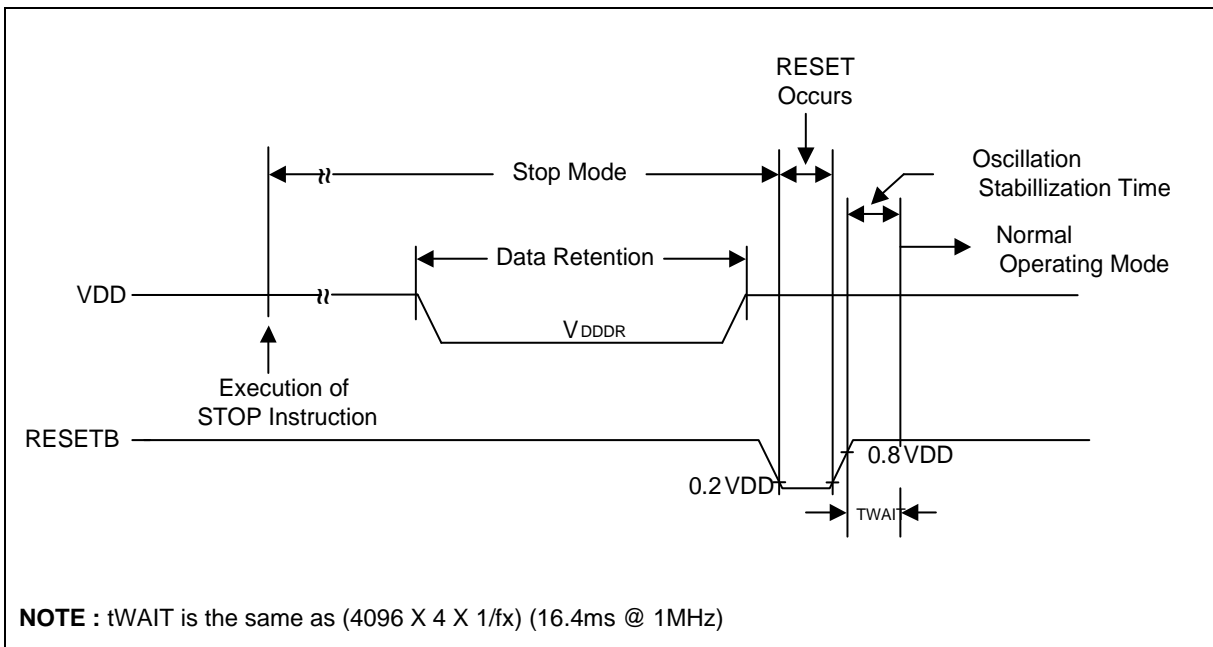


Figure 42. Stop Mode Release Timing when Initiated by RESETB

21.15 Internal flash ROM characteristics

Table 31. Internal Flash Rom Characteristics

($T_A = -40^\circ\text{C} \sim +85^\circ\text{C}$ or $T_A = -40^\circ\text{C} \sim 105^\circ\text{C}$, $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$, $V_{SS} = 0\text{V}$)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|-----------------------------|-------------------|-----------|-----|-----|--------|-------|
| Sector Write Time | t_{FSW} | – | – | 2.5 | 2.7 | ms |
| Sector Erase Time | t_{FSE} | – | – | 2.5 | 2.7 | |
| Code Write Protection Time | t_{FHL} | – | – | 2.5 | 2.7 | |
| Page Buffer Reset Time | t_{FBR} | – | – | – | 5 | us |
| Flash Programming Frequency | f_{PGM}^{NOTE2} | – | 0.4 | – | – | MHz |
| Endurance of Write/Erase | N_{FWE}^{NOTE2} | – | – | – | 30,000 | times |

NOTES:

1. During a flash operation, SCLK[1:0] of SCCR must be set to “00” or “01” (INT-RC OSC or Main X-TAL for system clock).
2. The measured value for the parameters and conditions listed were confirmed by simulation.

21.16 Main clock oscillator characteristics

Table 32. Main Clock Oscillator Characteristics

($T_A = -40^\circ\text{C} \sim +85^\circ\text{C}$ or $T_A = -40^\circ\text{C} \sim 105^\circ\text{C}$, $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$)

| Oscillator | Parameter | Condition | Min | Typ | Max | Unit |
|--------------------|----------------------------|-------------|-----|-----|------|------|
| Crystal | Main oscillation frequency | 2.2V – 5.5V | 4 | – | 10.0 | MHz |
| | | 2.4V – 5.5V | 4 | – | 12.0 | |
| Ceramic Oscillator | Main oscillation frequency | 2.0V – 5.5V | 4 | – | 10.0 | MHz |
| | | 2.4V – 5.5V | 4 | – | 12.0 | |
| External Clock | XIN input frequency | 2.0V – 5.5V | 4 | – | 10.0 | MHz |
| | | 2.4V – 5.5V | 4 | – | 12.0 | |

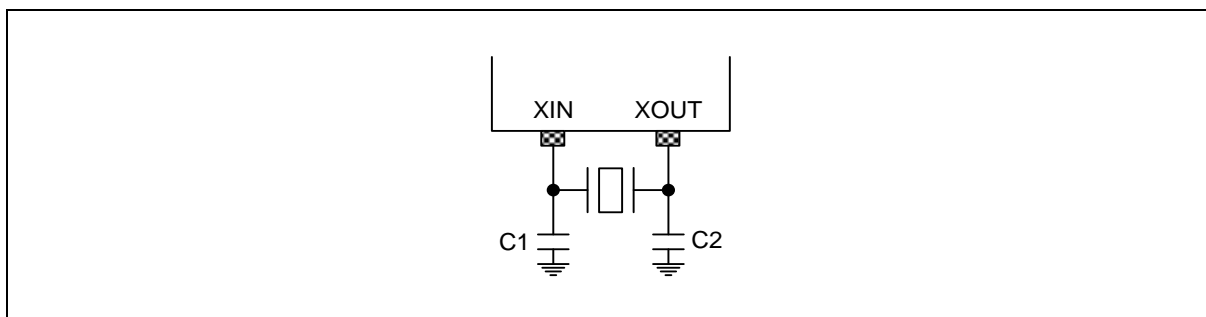


Figure 43. Crystal/Ceramic Oscillator

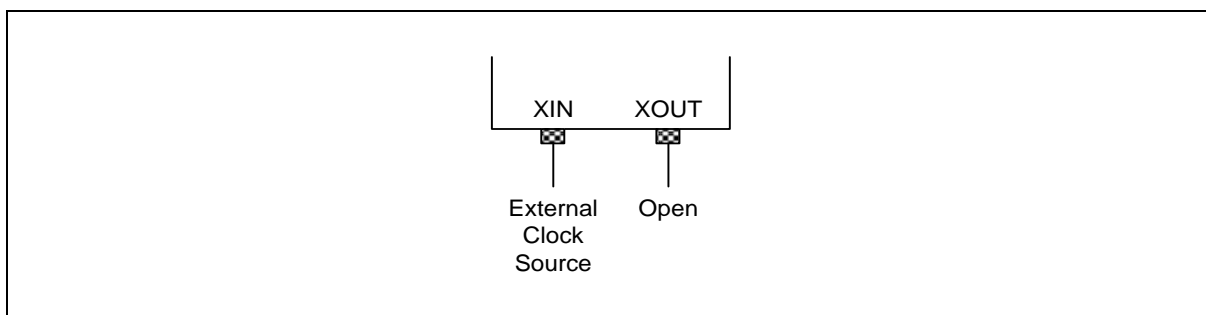


Figure 44. External Clock

21.17 Sub-clock oscillator characteristics

Table 33. Sub Clock Oscillator Characteristics

($T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ or $T_A = -40^{\circ}\text{C} \sim 105^{\circ}\text{C}$, $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$)

| Oscillator | Parameter | Condition | Min | Typ | Max | Unit |
|----------------|--|-------------|-----|--------|-----|------|
| Crystal | Sub oscillation frequency <small>NOTE</small> | 1.8V – 5.5V | 32 | 32.768 | 38 | kHz |
| External Clock | SXIN input frequency ^{NOTE} | | 32 | – | 100 | kHz |

NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.

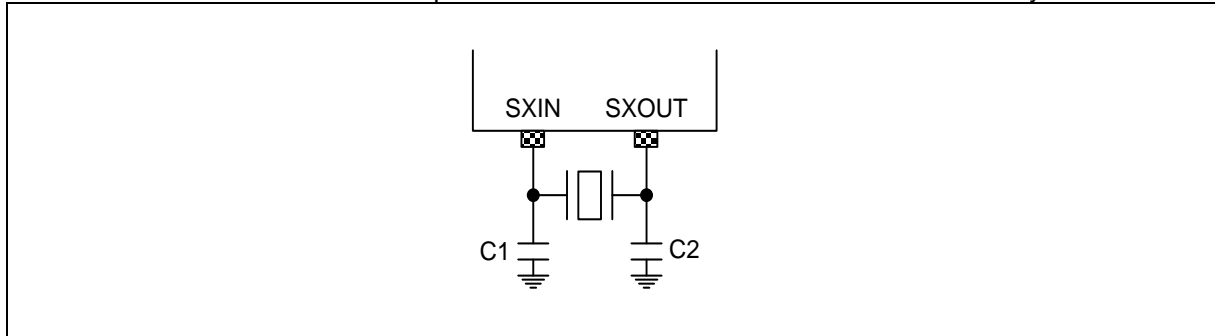


Figure 45. Crystal Oscillator

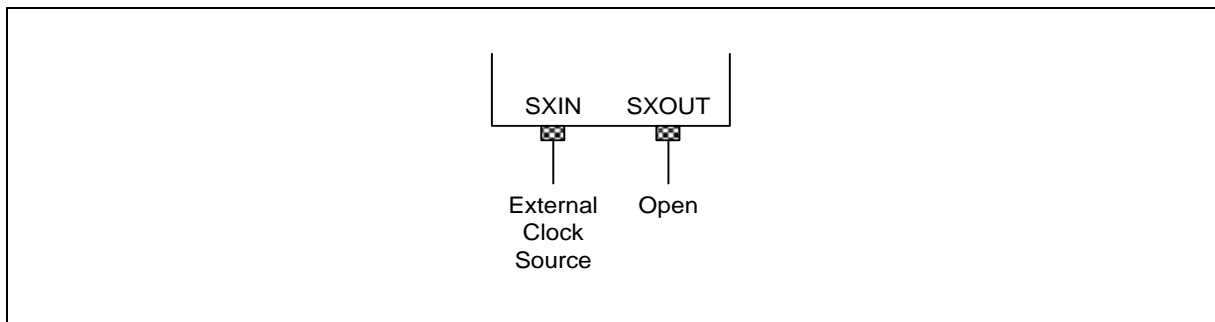


Figure 46. Crystal Oscillator

21.18 Main oscillation stabilization characteristics

Table 34. Main Oscillation Stabilization Characteristics

($T_A = -40^\circ\text{C} \sim +85^\circ\text{C}$ or $T_A = -40^\circ\text{C} \sim 105^\circ\text{C}$, $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$)

| Oscillator | Parameter | Min | Typ | Max | Unit |
|-------------------------|---|-----|-----|------|------|
| Crystal ^{NOTE} | $f_X > 4\text{MHz}$, $V_{DD} = 2.7\text{V} \sim 5.5\text{V}$, | - | - | 15 | ms |
| | $f_X > 1\text{MHz}$, $V_{DD} = 1.8\text{V}$, $T_A = -40^\circ\text{C}$ | | | 60 | |
| Ceramic ^{NOTE} | - | - | - | 10 | ms |
| External Clock | $f_{XIN} = 4$ to 12MHz XIN input high and low width (t_{XH} , t_{XL}) | 42 | - | 1250 | ns |

NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.

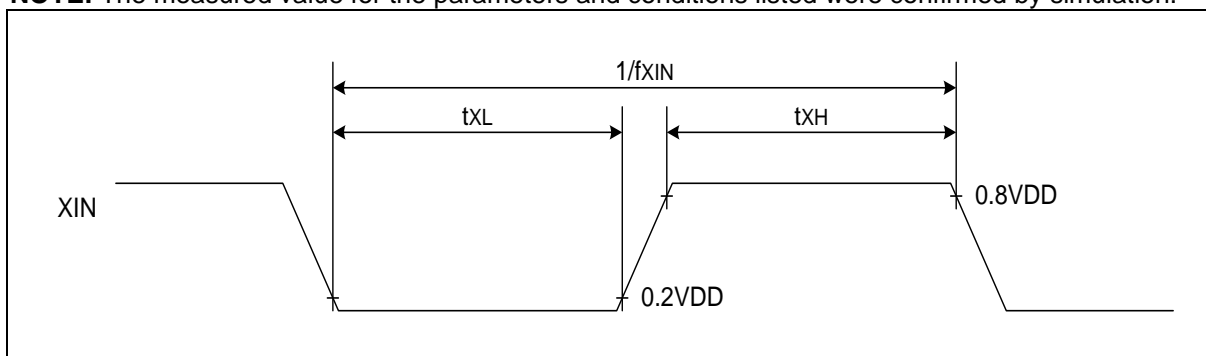


Figure 47. Clock Timing Measurement at XIN

21.19 Sub-oscillation characteristics

Table 35. Sub Oscillation Stabilization Characteristics

($T_A = -40^\circ\text{C} \sim +85^\circ\text{C}$ or $T_A = -40^\circ\text{C} \sim 105^\circ\text{C}$, $V_{DD} = 1.8\text{V} \sim 5.5\text{V}$)

| Oscillator | Parameter | Min | Typ | Max | Unit |
|-------------------------|---|-----|-----|-----|------|
| Crystal ^{NOTE} | $T_A = -40^\circ\text{C} \sim +85^\circ\text{C}$ | - | - | 10 | s |
| | $T_A = 25^\circ\text{C}$ | - | 500 | - | ms |
| External Clock | SXIN input high and low width (t_{XH} , t_{XL}) | 5 | - | 15 | us |

NOTE: The measured value for the parameters and conditions listed were confirmed by simulation.

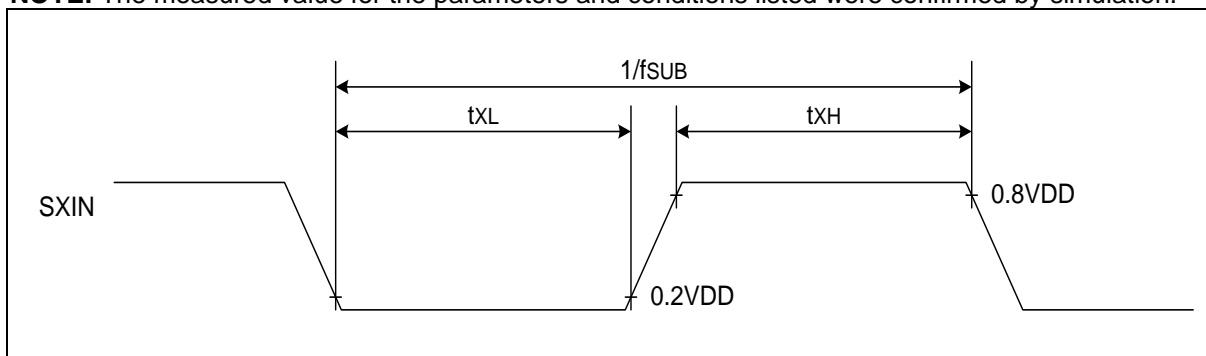


Figure 48. Clock Timing Measurement at SXIN

21.20 Operating voltage range

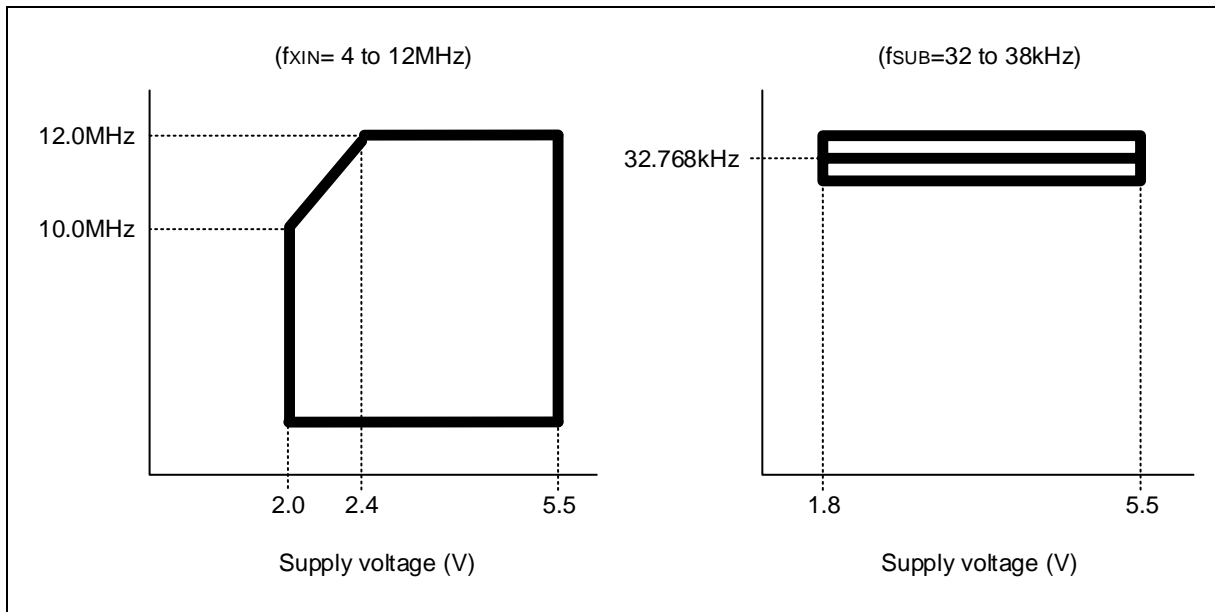


Figure 49. Operating Voltage Range

21.21 Recommended circuit and layout

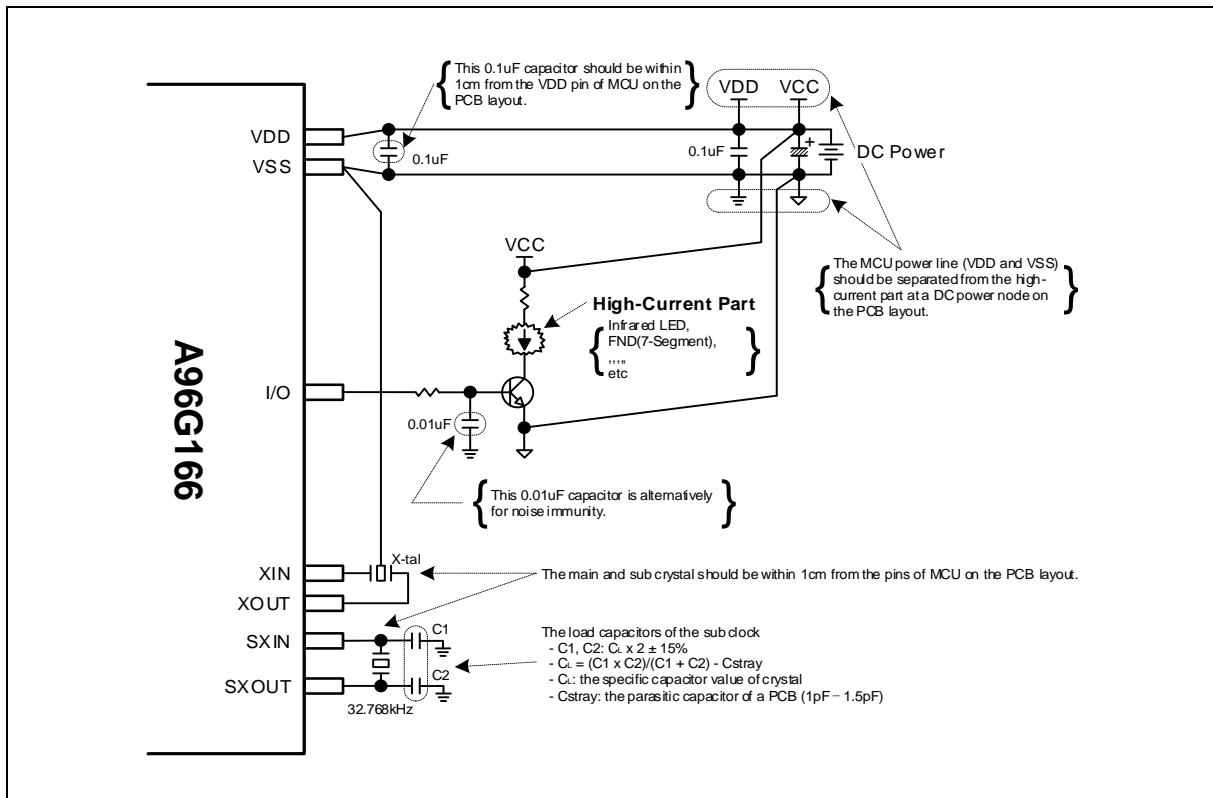


Figure 50. Recommended Voltage Range

Table 36 Reset Pin Component Values

| Item | Component | Value |
|-----------------------|-----------|-----------------------------|
| Pull-up/down resistor | R1 | 10KΩ |
| Filter capacitor | C1 | Typ. 100nF (0.1uF, example) |

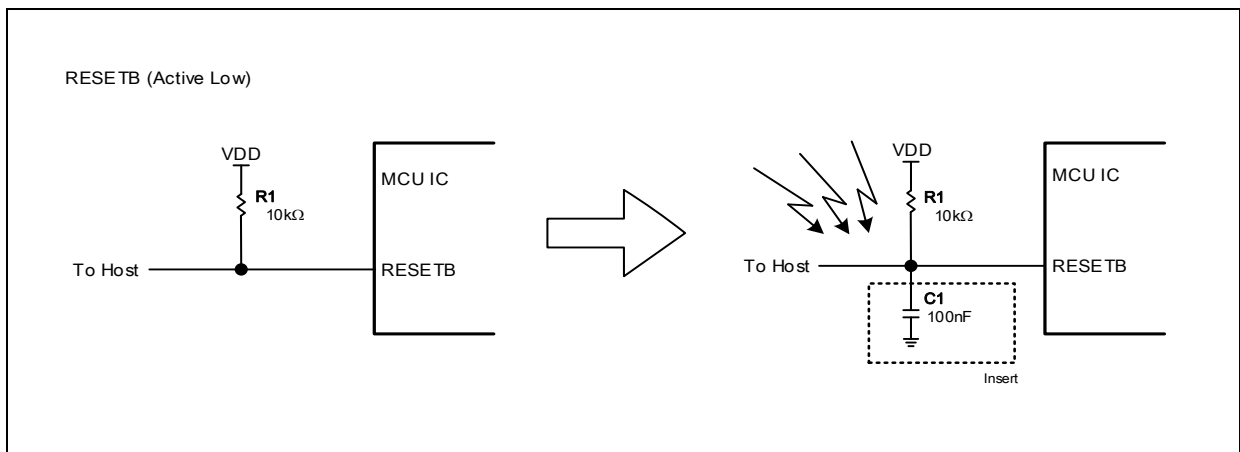


Figure 51. Filters used on a Reset Pin Diagram

21.22 Typical characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

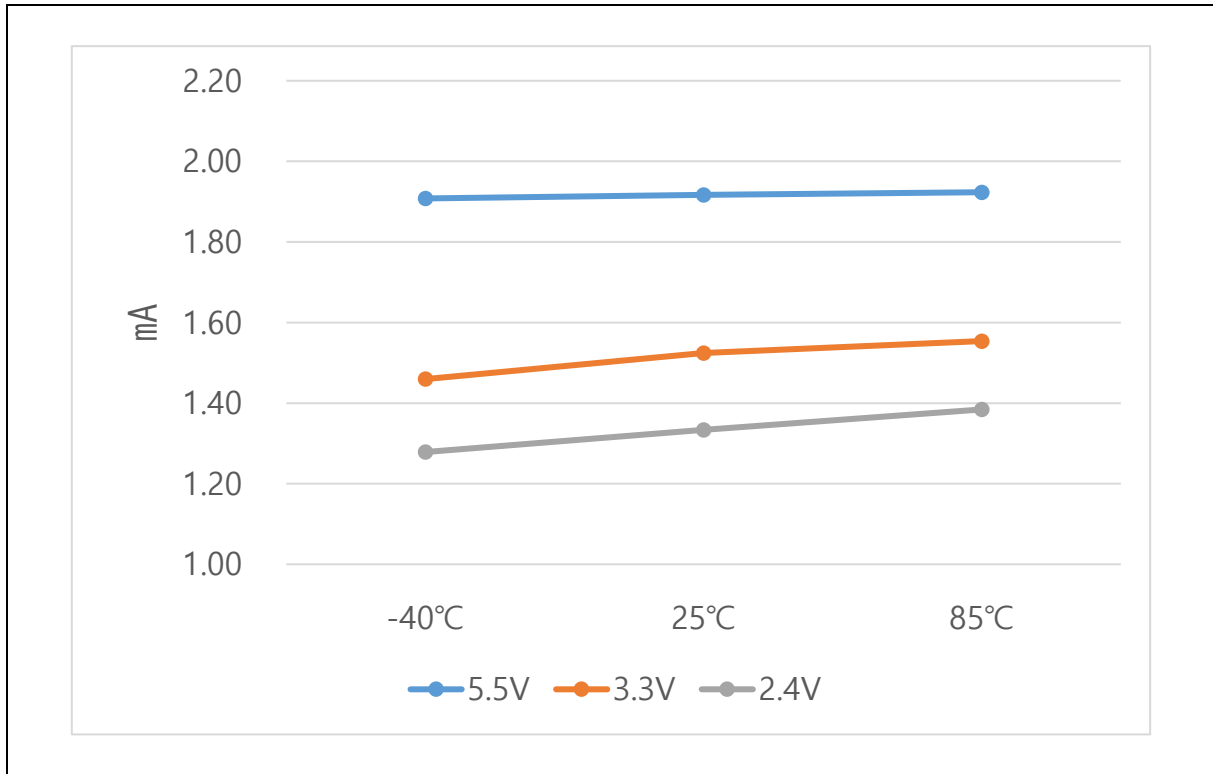


Figure 52. RUN (IDD1, fXIN = 8MHz) Current

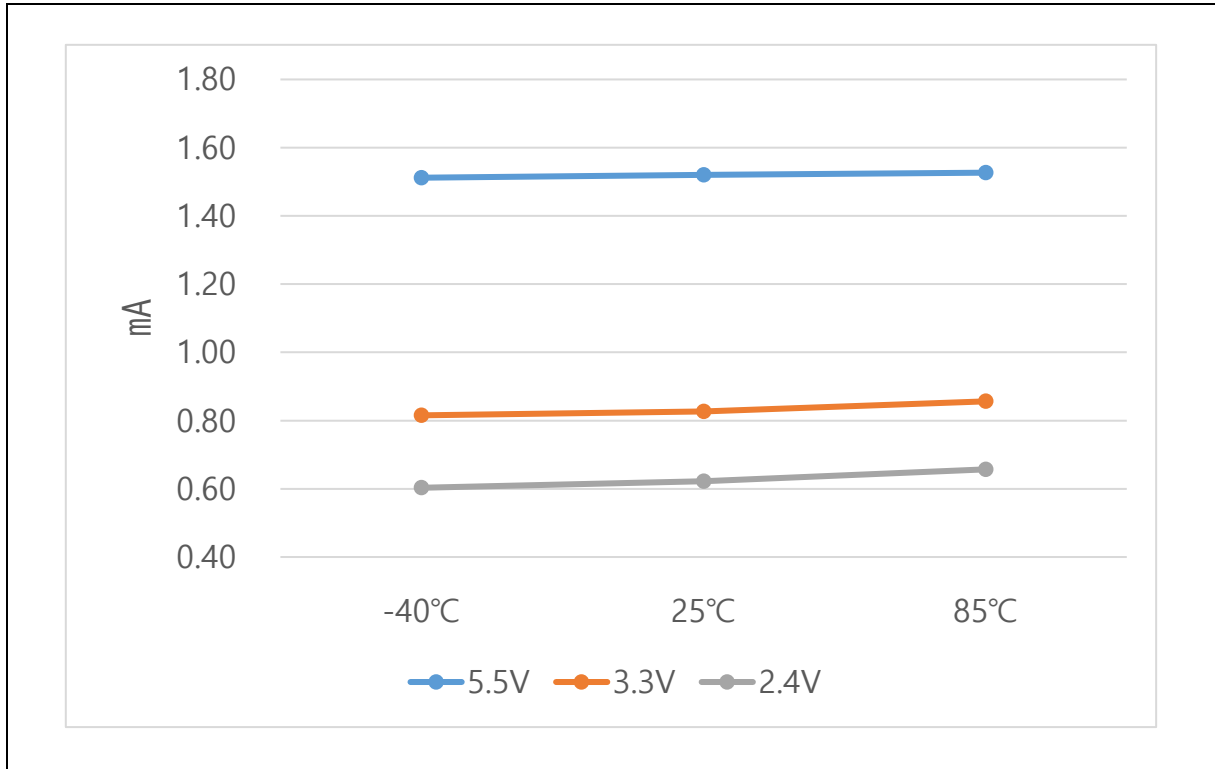


Figure 53. IDLE (IDD2, fXIN = 8MHz) Current

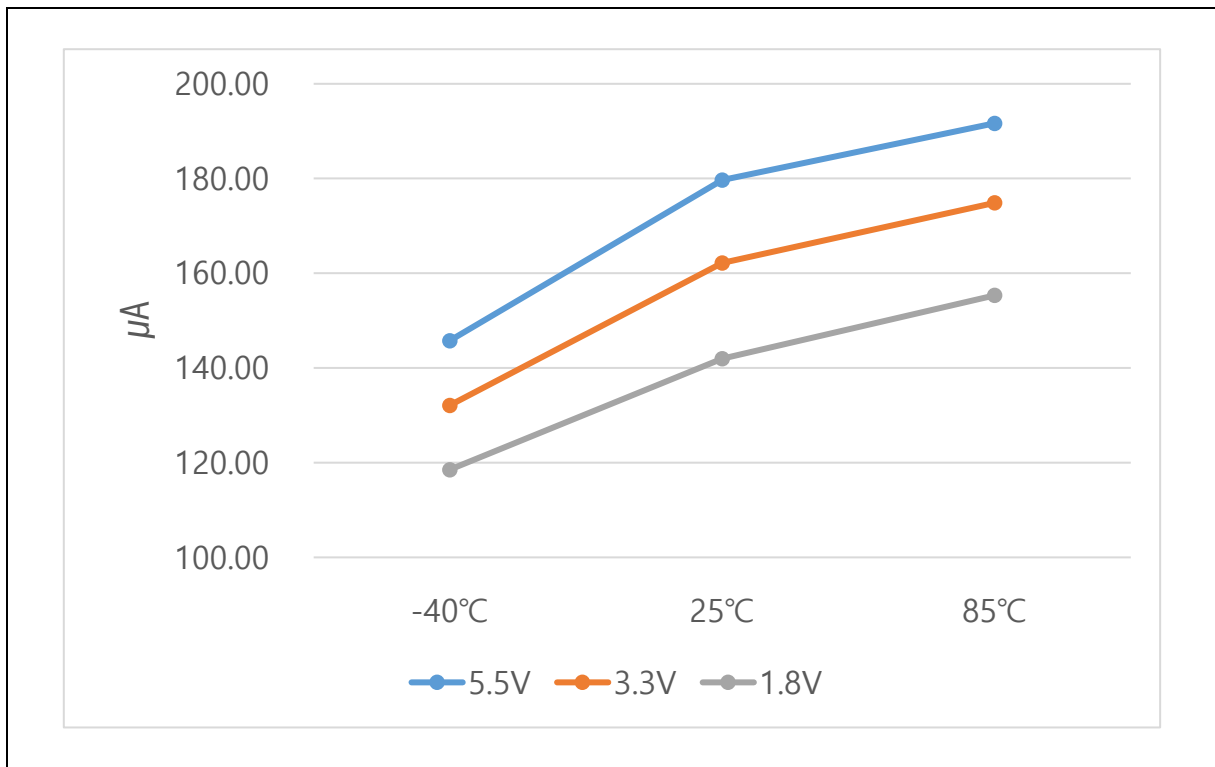


Figure 54. IDLE (IDD2, fLSI = 128kHz) Current

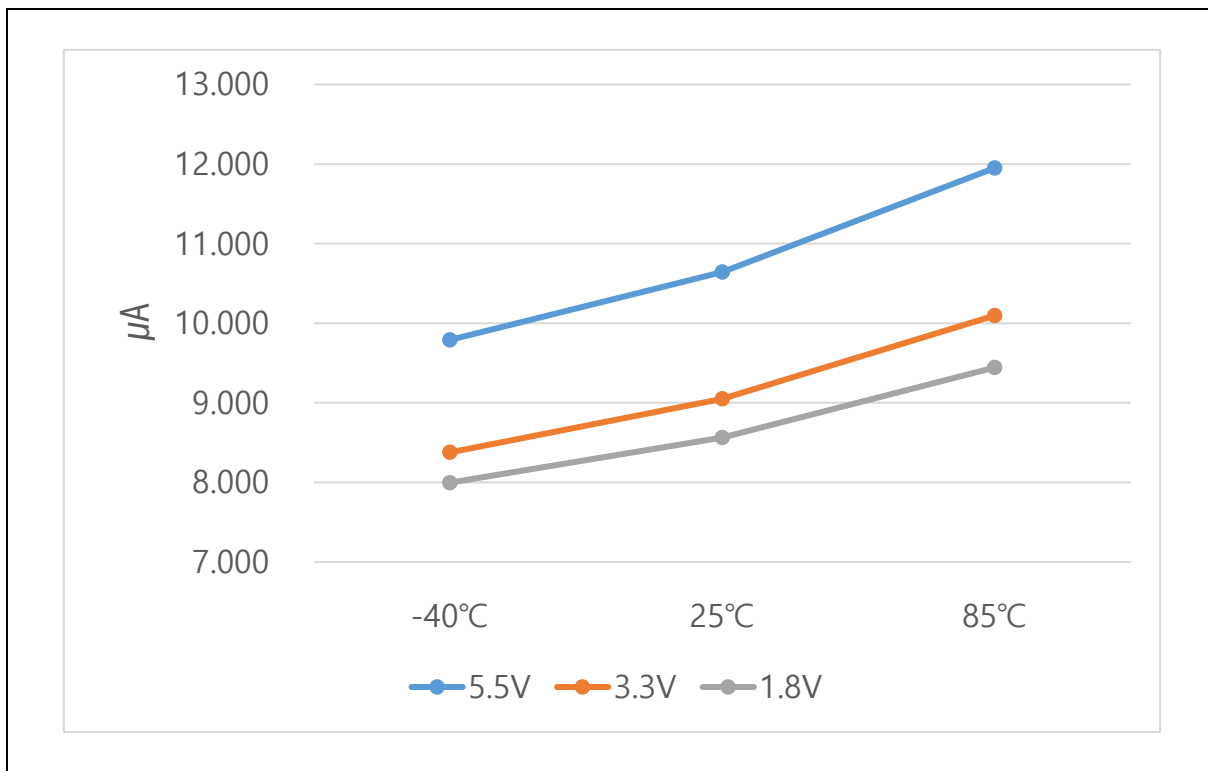


Figure 55. STOP1 (IDD3) Current

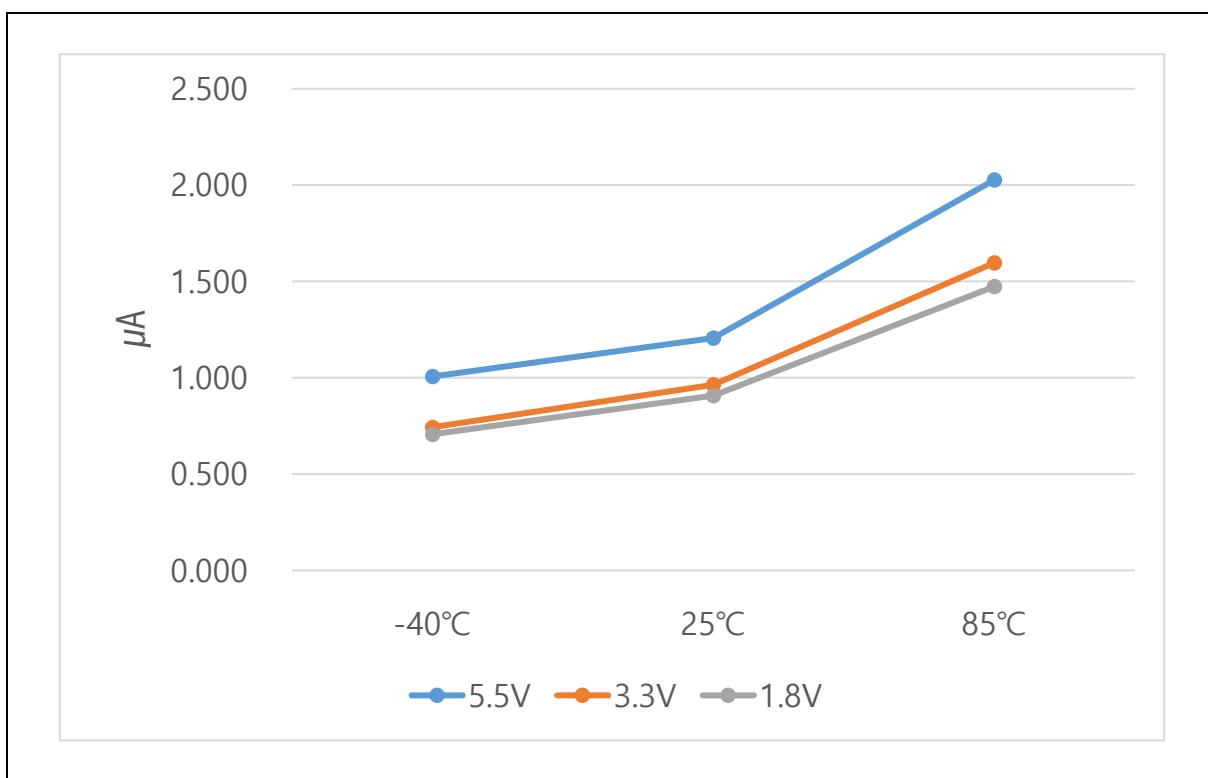


Figure 56. STOP2 (IDD4) Current

22 Development tools

This chapter introduces a wide range of development tools for microcontrollers. ABOV offers software tools, debuggers, and programmers to help a user in generating right results to match target applications. ABOV supports entire development ecosystem of the customers.

22.1 Compiler

ABOV semiconductor does not provide any compiler for A96G166/A96A166/A96S166. It is recommended to consult a compiler provider.

Since A96G166/A96A166/A96S166 has Mentor 8051 as its core, and ROM is smaller than 64Kbytes in size, a developer can use any standard 8051 compilers of other providers.

22.2 Core and debug tool information

ABOV's 8-bit microcontroller uses OCD (On-Chip Debugger) interface for debugging, which is ABOV's own interface. The OCD not only monitors and controls the core, but also supports the read and write operations of external memory and devices. In addition, it supports memory monitoring and break functions.

Debug interfaces such as OCD interface enable microcontroller to write to internal programmable memory, allowing them to support ISP (In-System Program) that makes possible to write as a single chip or as an embedded chip in the system. Table 37 provides information of the core and debug emulation interface.

Table 37. Core and Debug Information

| | Value | Description |
|-------------------------------|-----------------------|--------------------|
| Device Name | A9xXxxx | |
| Series | 94/ 95/ 96/ 97 series | |
| Core | M8051/ CM8051 | |
| Extended Stack Pointer | Yes/ no | 94, 97 series only |
| Debug Interface | OCD 1/ OCD 2 | |
| Number of Break Point | 4/ 8 | |
| Real-time Monitoring | Yes/ no | OCD 2 only |
| Run Flag Port | Yes/ no | OCD 2 option |

1. The A96G166/A96A166/A96S166 has 96 series core and OCD 1 interface.
2. The A96G166/A96A166/A96S166 can be operated with OCD II dongle too, because OCD II dongle includes all of OCD1 function.
3. The 95 series core is the old version of 96 series core.

22.2.1 Feature of 94/96/97 series core

ABOV's 8-bit microcontroller contains an M8051/CM8051 core that is an improved version of the 8051. The M8051/CM8051 core is compatible with the 8051, and reduces time of operation cycles. It makes development easier by providing the OCD debug function.

ABOV's 8-bit microcontroller has a core of 94-series, 96-series, or 97-series, that is basically compatible with the 8051 series at the instruction set level. A core of each series uses different Debug Interface respectively as shown in Table 38.

Table 38. Core and Debug Interface by Series

| | Core | Debug Interface |
|------------------|--------|-----------------|
| 96 Series | M8051 | OCD 1 |
| 97 Series | M8051 | OCD 2 |
| 94 Series | CM8051 | OCD 2 |

Features of each series are compared in Table 39.

Table 39. Feature Comparison Chart By Series and Cores

| | 96 Series | 97 Series | 94 Series |
|--|----------------------------|---------------------|------------------------------------|
| CPU Core | M8051 | M8051 | CM8051 |
| Cycle Compatible with MCS51 | 1/6 | 1/6 | No |
| OCD Function | OCD 1 | OCD 2 | OCD 2 |
| Program BUS | 8-bit | | |
| Data Bus | 8-bit IRAM/ XRAM separated | | 8-bit single SRAM |
| EA Auto Clear ^{NOTE1} | Yes | Yes | Yes |
| EA=0, Idle/ Stope Mode Wake up | Yes | Yes | Yes |
| Interrupt Priority ^{NOTE2} | 6 group x 4 level | Interrupt x 4 level | Interrupt x 2 level |
| Nested Interrupt Priority | 4 level | 4 level | Interrupt x 2 level (max. 4 times) |
| SFR BUS (read/ write) | Two ports | Two ports | Single port |
| Stack Extension | X | O | O |
| Register | SRAM | | |
| Register Bank | 4 | | |
| CPU/ Flash Clock Ratio | x 1 | | |
| Pipeline | No | No | 2-stage (IF + ID/ EX) |
| DHRY Stone Score (I8051: 1.00) | 6.0 | 6.0 | 8.4 |
| Average Instruction Set Exe. Cycle Compare with i8051 | x 6.0 | x 6.0 | x 6.4 |
| Power Consumption/ DHRY (@synthesis) | 52.27uA/ MHz | 52.27uA/ MHz | 30.19 uA/ MHz |

NOTES:

1. EA means that All Interrupt Enable bit or Disable bit (Standard 8051).
2. Group: When a programmer selects a specific interrupt (e.g. Interrupt1), Whole interrupts: 0, 6, 12, and 18 have higher priorities.
3. The A96G140/A96G148/A96A148 has the 96 series core and OCD 1 interface.
4. The A96G140/A96G148/A96A148 can be operated with the OCD II dongle too, because the OCD II dongle includes all functions of the OCD1.

ABOV's 8-bit microcontrollers maintain binary compatibility with 8051 cores; however, the cores and series have differences in performances, core functionalities, and debug interfaces.

You can see the differences of each series in the following sections.

22.2.2 OCD type of 94/96/97 series core

Cores of 96-series use OCD 1 for a debug interface, while cores of 94-series and 97-series use OCD 2 for debug interfaces. The OCD 1 and OCD 2 use the same method on the Hardware, however, the protocols are incompatible with each other.

In the OCD 2, it is able to measure the emulation time through the "Run Flag" pin.

Table 40. OCD Type of Each Series

| Series | 96-Series | 97-Series | 94-Series | Remark |
|-----------------|-----------|-----------|-----------|--------|
| OCD type | OCD 1 | OCD 2 | OCD 2 | |

In Table 41, debug interfaces of the OCD 1 and OCD 2 are compared.

Table 41. Comparison of OCD 1 and OCD 2

| | Value | Description |
|--------------|----------------------|--|
| OCD 1 | Break point MAX.8 | PC break only |
| OCD 2 | Break point MAX.12 | With RAM break — Code, XDATA, IDATA — 1/8/16/32bit compare |
| | Real-time monitoring | Code, XDATA, IDATA |
| | Frequency output | Examine CPU frequency |
| | Run Flag port | Option for run time measurement |

96 Series – OCD 1

The 96 series supports basic operations of debug interfaces such as Run, Stop, Step, Break point, register reading/writing, Memory reading/writing, and SFR reading/writing.

94 Series and 97 Series – OCD 2

The 94 series and 97 series support the features listed below, as well as the features of the OCD 1 (however, the protocol is not compatible with the OCD1):

- RTM support: CODE, XDATA, IDATA are updated during the Run Time (Real Time Monitoring available).
- Run Flag support: Emulation Time can be measured in OCD mode (using the Run Flag port).
- RAM Break support: IDATA, SFR, and XDATA break are added.

22.2.3 Interrupt priority of 94/96/97 series core

In the M8051, users can set interrupt priorities by group. The 96-series microcontroller with the basic M8051 core only supports interrupt priorities in group units. In the 94-series or 97-series microcontroller, users set interrupt priorities to have more functions than the existing functions, and can set individual priority for each interrupt source.

Table 42. Interrupt Priorities in Groups and Levels

| Series | 96-Series | 97-Series | 94-Series | Remark |
|---------------------------|----------------------|---------------|---------------|--|
| Interrupt Priority | 6 Grouped 4 Level | Fully 4 Level | Fully 4 Level | 96 Series: IP/IP (Interrupt Priority Register) 94, 97 Series: IPxL/IPxH (Interrupt Priority Register) |

96 Series

- The priorities by group is available only with IP/IP1 settings.
 - With IP/IP1 settings, users can set interrupt priorities by group unit.
 - The interrupt priority of a group unit (4 interrupts in a group) can be changed to the level between 0 and 3 according to the value of IP/IP1.

94, 97 Series

- The individual interrupt priority can be set by setting IPxL/IPxH(x=0~3).
- The individual interrupt priority can be changed to the level between 0 and 3 according to the value of IPxL/IPxH(x=0~3).

22.2.4 Extended stack pointer of 94/96/97 series core

The M8051 uses IRAM area for Stack Pointer. However, 94-series and 97-series microcontrollers use both IRAM area and XRAM area for Stack Pointer by configuring additional registers.

The XSP and XSPCR registers are involved in this functionality as described below:

- By configuring the XSP/XSPCR register, you can use the XRAM area for the Stack Pointer.
 - The XSPCR decides whether to use XRAM for Stack Pointer.
 - ◆ If XSPCR='0', IRAM is available for Stack Pointer.
 - ◆ If XSPCR='1', XRAM is available for Stack Pointer.
 - The XSP decides a position of XRAM Stack Pointer.
 - ◆ This is valid only if XSPCR='1'.

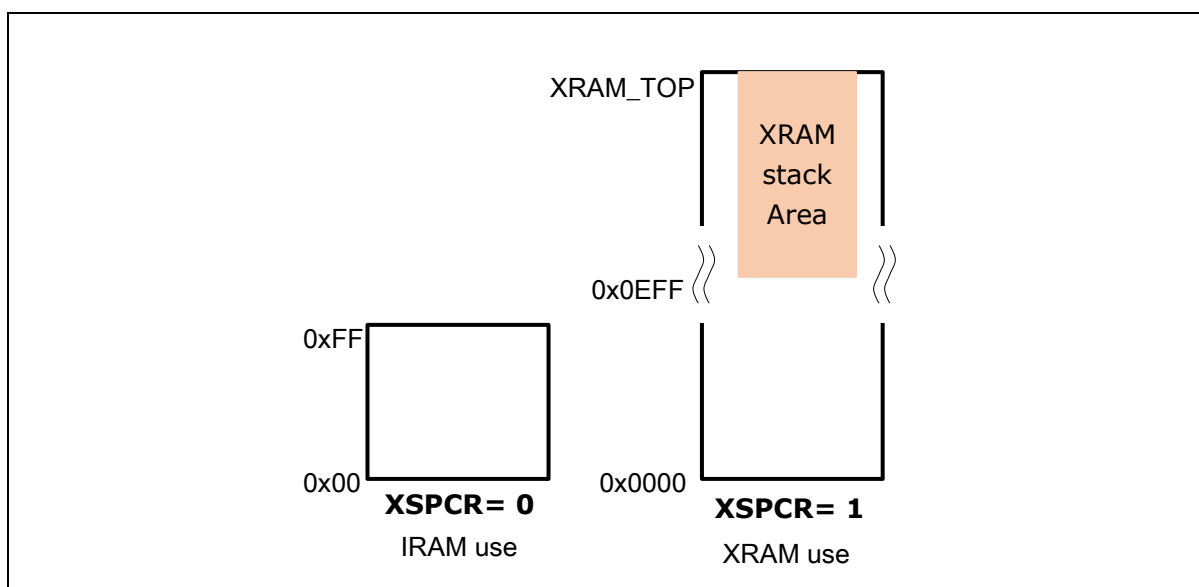


Figure 57. Configuration of the Extended Stack Pointer

$$\text{STACK_POINTER} = \{\text{XSP}[7:0], \text{SP}[7:0]\} = \text{XRAM_TOP} - \text{STACK_SIZE}$$

Ex) If only 256bytes of XRAM will be used for stack,

- XRAM_TOP = 4K(0x0FFF)
- STACK_SIZE = 256byte(0x0100)
- XSPCR= 1, XSP= 0x0E
- SP=0xFF setting
- Stack Pointer Position = 0x0FFF - 0x0100= 0x0EFF

22.3 OCD (On-chip debugger) emulator and debugger

Microcontroller with 8051 cores have an OCD (On-Chip Debugger), a debug emulation block. The OCD is connected to a target microcontroller using two lines such as DSCL and DSDA. The DSCL is used for clock signal and the DSDA is for a bi-directional data.

The two lines work for the core management and control by doing register management and execution, step execution, break point and watch functions. In addition, they control and monitor the internal memory and the device by reading and writing.

Table 43. Debug Feature by Series

| Series name | 96-series | 97-series | 94-series |
|----------------------------|-----------|-----------|-----------|
| OCD function | OCD 1 | OCD 2 | OCD 2 |
| Max. number of breakpoints | 8 | 8 | 4 |
| Saving stack in XRAM | No | Yes | Yes |
| Real time monitoring | No | Yes | Yes |
| Run flag support | No | Yes | Yes |

The OCD 2 applied to 94-series and 97-series provides the RTM (Real Time Monitoring) function that monitors internal memory and I/O status without stopping the debugging. In addition, the OCD 2 provides the breakpoint function (RAM Break Function) for the IDATA, SFR, and XDATA.

The following functions have been extended from the OCD 2:

- Emulation Time can be measured in OCD mode (using the Run Flag port)
- CODE, XDATA, IDATA are updated during the Run Time (Real Time Monitoring available).
- IDATA, SFR, XDATA break are added (RAM Break support).

Figure 58 shows the standard 10-pin connector of OCD 1 and OCD 2.

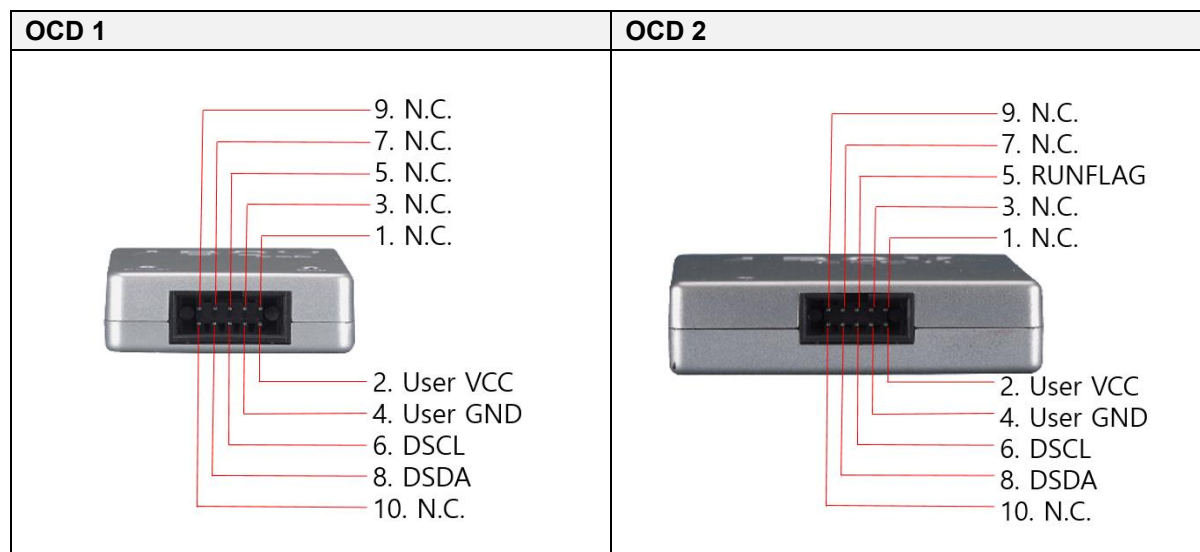


Figure 58. OCD 1 and OCD 2 Connector Pin Diagram

Table 44 describes the pins used for the OCD 1 and OCD 2.

Table 44. OCD 1 and OCD 2 Pin Description

| Pin name | Microcontroller function in Debug Mode | |
|----------|--|---|
| | I/O | Description |
| DSCL | I | Serial clock pin. Input only pin. |
| DSDA | I/O | <ul style="list-style-type: none"> Serial data pin. Output port when reading and input port when programming. IT can be assigned as input/push-pull output port. |
| VDD,VSS | — | Logic power supply pin. |

The OCD emulator supports ABOV's 8051 series MCU emulation. The OCD uses two wires that are interfaced between PC and MCU, which is attached to user's system. The OCD can read or change the value of MCU's internal memory and I/O peripherals. In addition, the OCD controls MCU's internal debugging logic. This means OCD controls emulation, step run, monitoring and many more functions regarding debugging.

The OCD debugger program runs underneath MS operating system such as MS-Windows NT/ 2000/ XP/ Vista (32-bit). If you want to see more details, please visit ABOV's website (www.abovsemi.com), and download debugger S/W and corresponding manuals.

- Connection:
 - DSCL (A96G166/A96A166/A96S166 P01 port)
 - DSDA (A96G166/A96A166/A96S166 P00 port)

Figure 59 shows pinouts of OCD connector.

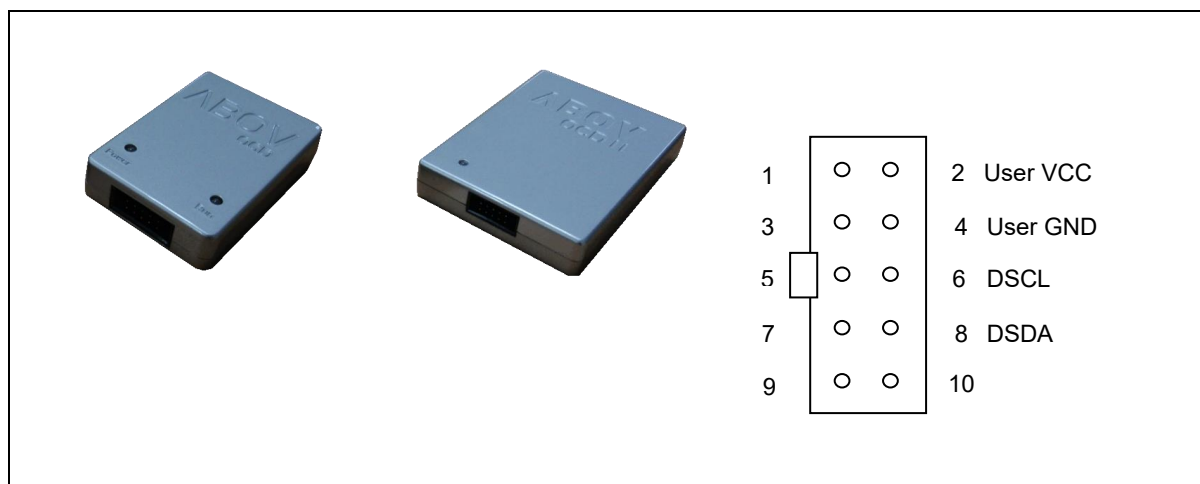


Figure 59. Debugger (OCD1/OCD2) and Pinouts

22.3.1 On-chip debug system

A96G166/A96A166/A96S166 supports On-chip debug (OCD) system. We recommend developing and debugging program with A96G1xx series. The OCD system of A96G166/A96A166/A96S166 can be used for programming the non-volatile memories and on-chip debugging.

In this section, you can find detailed descriptions for programming via the OCD interface. Table 45 introduces features of the OCD.

Table 45. OCD Features

| | |
|--|--|
| Two wire external interface | <ul style="list-style-type: none"> • 1 for serial clock input • 1 for bi-directional serial data bus |
| Debugger accesses | <ul style="list-style-type: none"> • All internal peripherals • Internal data RAM • Program Counter • Flash memory and data EEPROM memory |
| Extensive On-Chip Debugging supports for Break Conditions | <ul style="list-style-type: none"> • Break instruction • Single step break • Program memory break points on single address • Programming of Flash, EEPROM, Fuses, and Lock bits through the two-wire interface • On-Chip Debugging supported by Dr. Choice® |
| Operating frequency | The maximum frequency of a target MCU. |

Figure 60 shows a block diagram of the OCD interface and the On-chip Debug system.

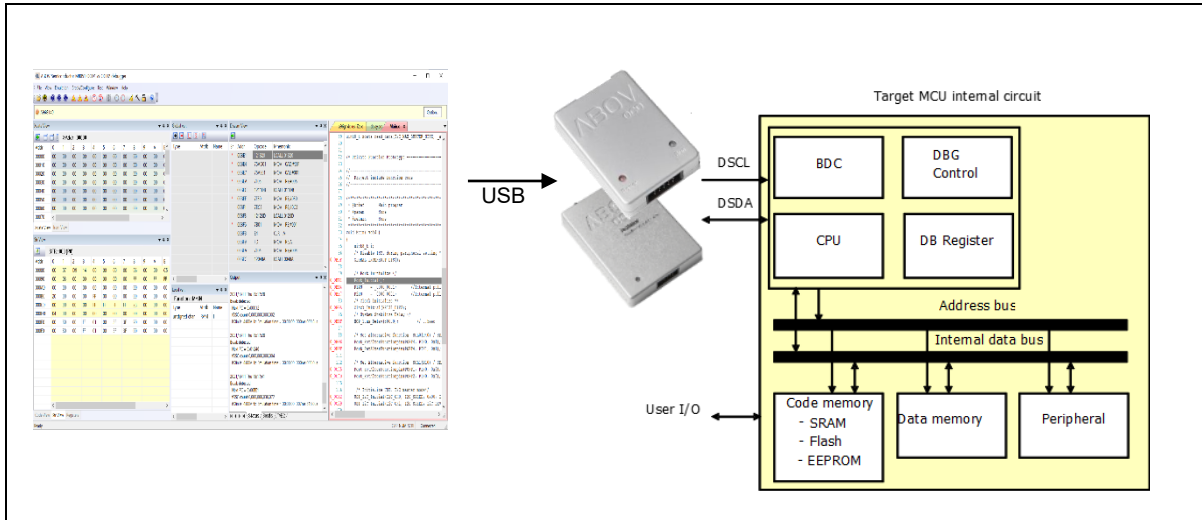


Figure 60. On-Chip Debugging System in Block Diagram

Entering debug mode

While communicating through the OCD, users can enter the microcontroller into DEBUG mode by applying power to it. This means that the microcontroller enters DEBUG mode when you place specific signals to the DSDL and DSDA at the moment of initialization when the microcontroller is powered on. This requires that you can control power of the microcontroller (VCC or VDD) and need to be careful to place capacitive loads such as large capacity condenser on a power pin.

Please remember that the microcontroller can enter DEBUG mode only when power is applied, and it cannot enter DEBUG mode once the OCD is run.

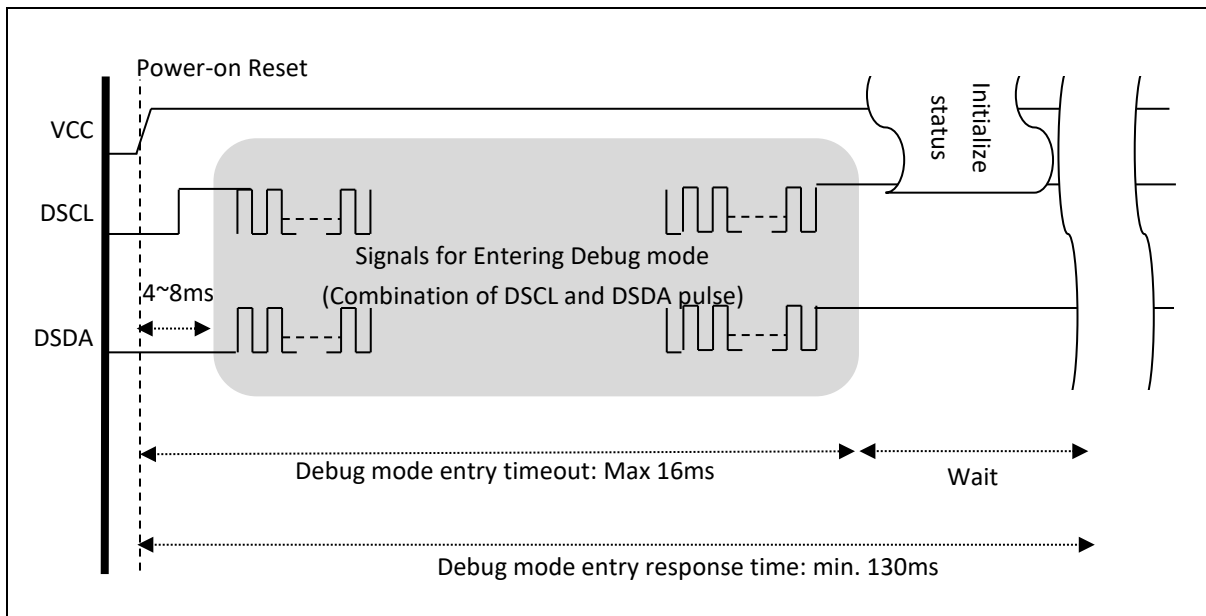


Figure 61. Timing Diagram of Debug Mode Entry

22.3.2 Two-wire communication protocol

For the OCD interface, the semi-duplex communication protocol is used through separate two wires, the DSCL and DSDA. The DSCL is used for serial clock signal and the DSDA is used for bi-directional serial address and data.

A unit packet of transmission data is 10-bit long and consists of a byte of data, 1-bit of parity, and 1-bit of acknowledge. A parity check bit and a receive acknowledge bit are transmitted to guarantee stability of the data communication. A communication packet includes a start bit and an end bit to indicate the start and end of the communication.

More detailed information of this communication protocol is listed below:

Basic transmission packet

- A 10-bit packet transmission using two-pin interface.
- A packet consists of 8-bit data, 1-bit parity and 1-bit acknowledge.
- Parity is even of '1' for 8-bit data in transmitter.
- Receiver generates acknowledge bit as '0' when transmission for 8-bit data and its parity has no error.
- When transmitter has no acknowledge (Acknowledge bit is '1' at tenth clock), error process is executed in transmitter.
- When acknowledge error is generated, host PC makes stop condition and transmits command which has error again.
- Background debugger command is composed of a bundle of packet.
- Start condition and stop condition notify the start and the stop of background debugger command respectively.

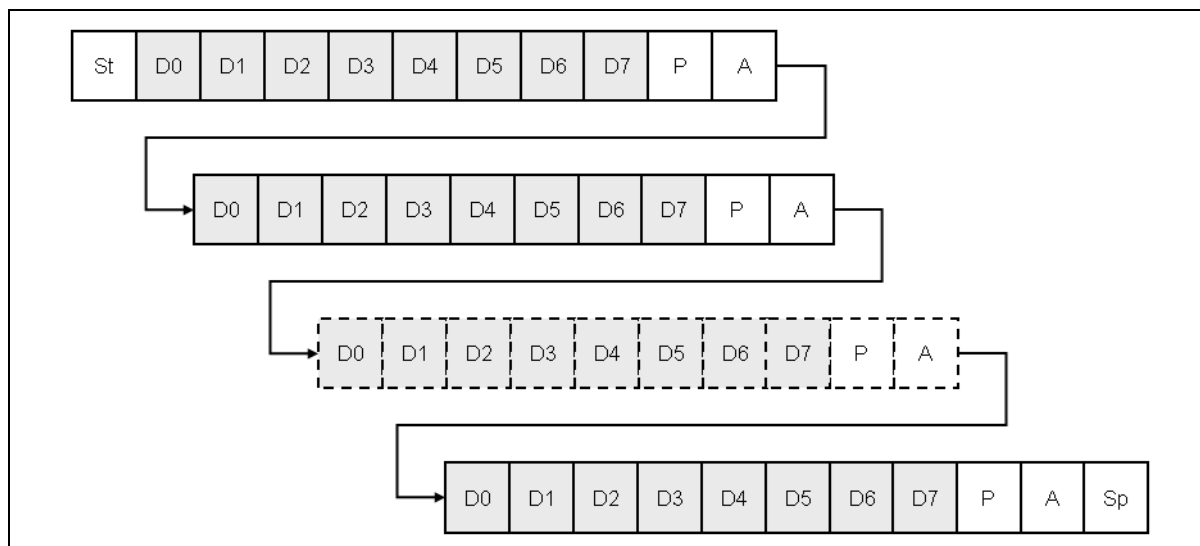


Figure 62. 10-bit Transmission Packet

Packet transmission timing

Figure 63 shows a timing diagram of a packet transmission using the OCD communication protocol.

A start bit in the figure means start of a packet and is valid when the DSDA falls from ‘H’ to ‘L’ while External Host maintains the DSCL to ‘H’. After the valid start bit, communication data is transferred and received between a Host and a microcontroller.

An end bit means end of the data transmission and is valid when the DSDA changes from ‘L’ to ‘H’ while a Debugger maintains DSCL to ‘H’. Next, the microcontroller places the bus in a wait state and processes the received data.

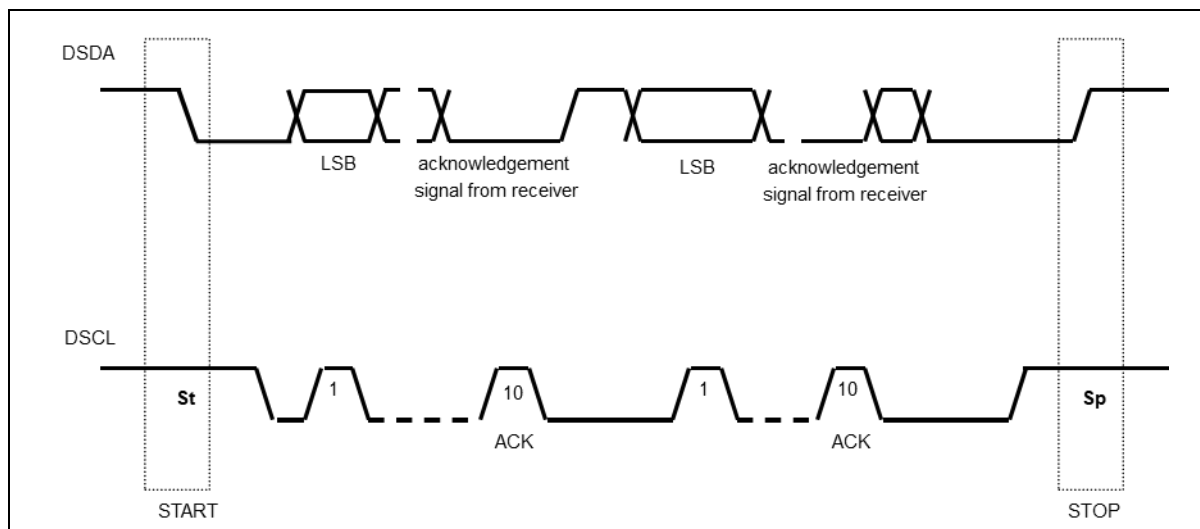


Figure 63. Data Transfer on OCD

Figure 64 shows a timing diagram of each bit based on the state of the DSCL clock and the DSDA data. Similar to I2C signal, the DSDA data is allowed to change when the DSCL is 'L'. If the data changes when DSCL is 'H', the change means 'START' or 'STOP'.

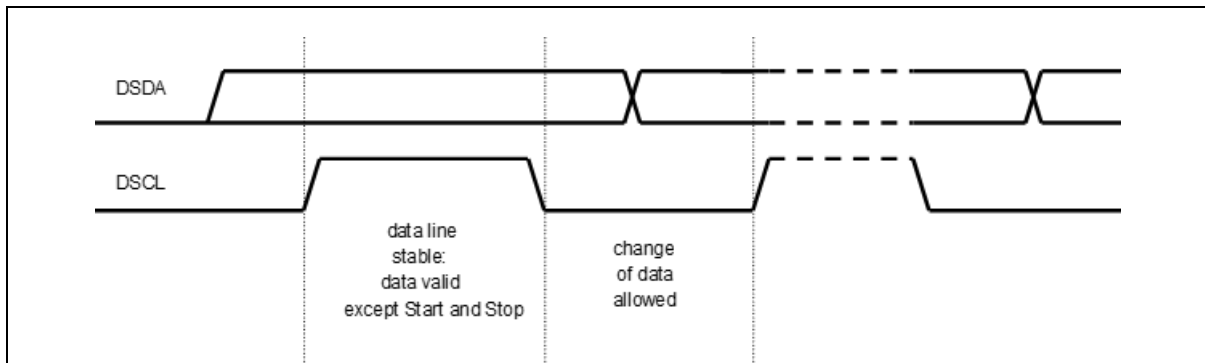


Figure 64. Bit Transfer on Serial Bus

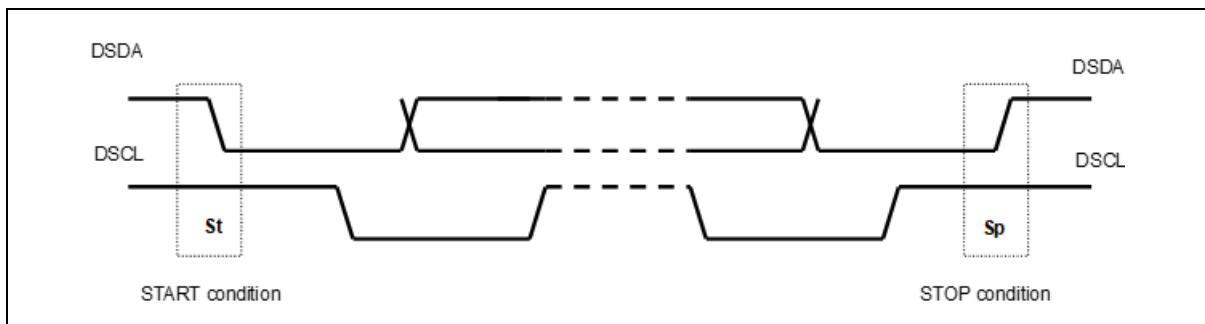


Figure 65. Start and Stop Condition

During the OCD communication, each data byte is transferred in accompany with a parity bit. When data is transferred in succession, a receiver returns the acknowledge bit to inform that it received.

As shown in Figure 66, when transferring data, a receiver outputs the DSDA to 'L' to inform the normal reception of data. If a receiver outputs DSDA to 'H', it means error reception of data.

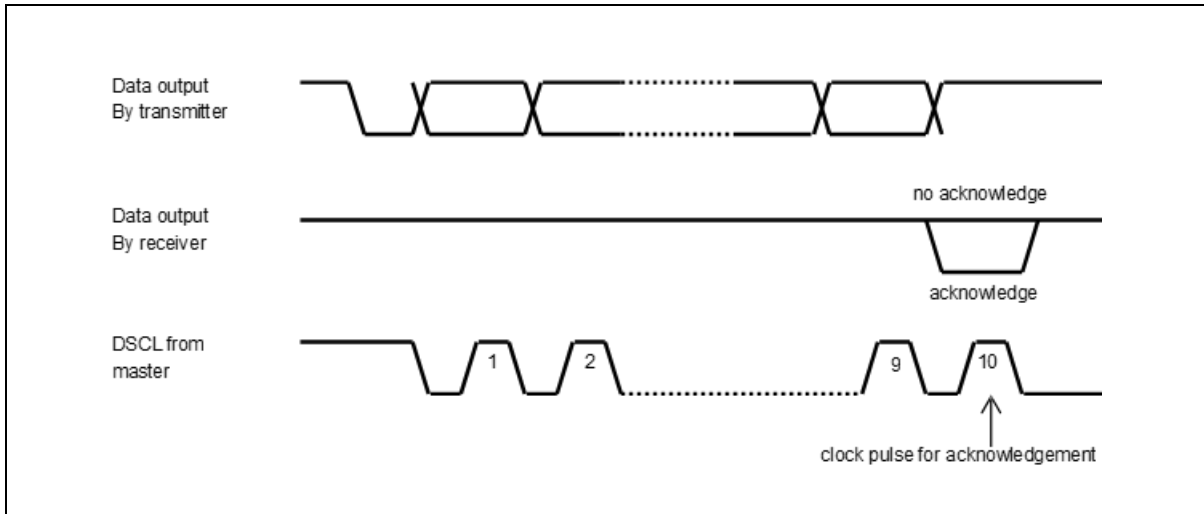


Figure 66. Acknowledge on Serial Bus

While the Host Debugger executes data communications, if a microcontroller needs communication delay or process delay, it can request communication delay to the Host Debugger.

Figure 67 shows timing diagrams where a microcontroller requests communication delay to the Host Debugger. If the microcontroller requests timing delay of the DSCL signal that the Host Debugger outputs, the microcontroller maintains the DSCL signal to 'L' to delay the clock change although the Host Debugger changes DSCL to 'H'.

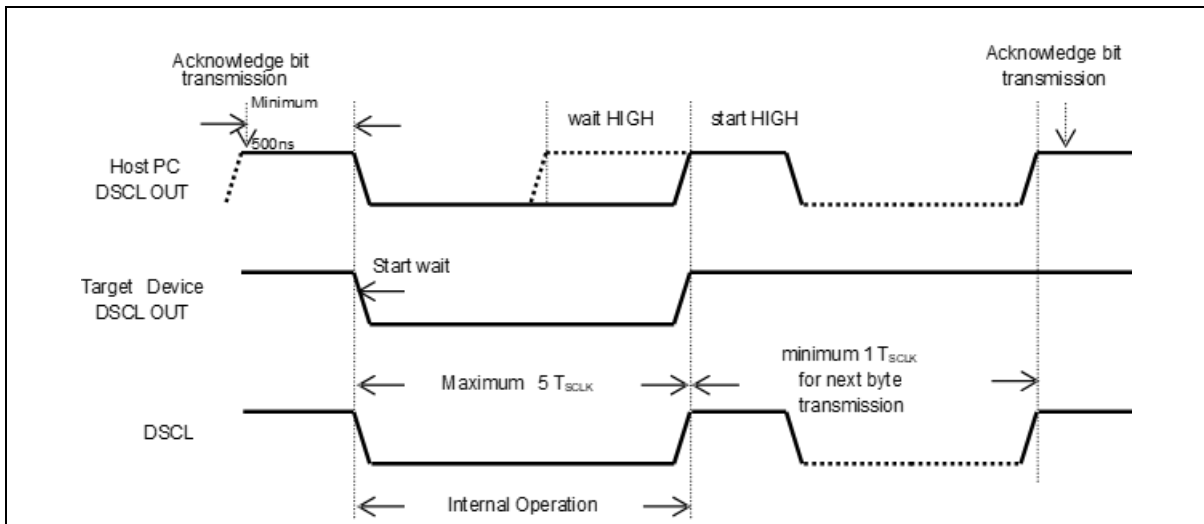


Figure 67. Clock Synchronization during Wait Procedure

22.4 Programmers

22.4.1 E-PGM+

E-PGM+ USB is a single programmer. A user can program A96G166/A96A166/A96S166 directly using the E-PGM+.

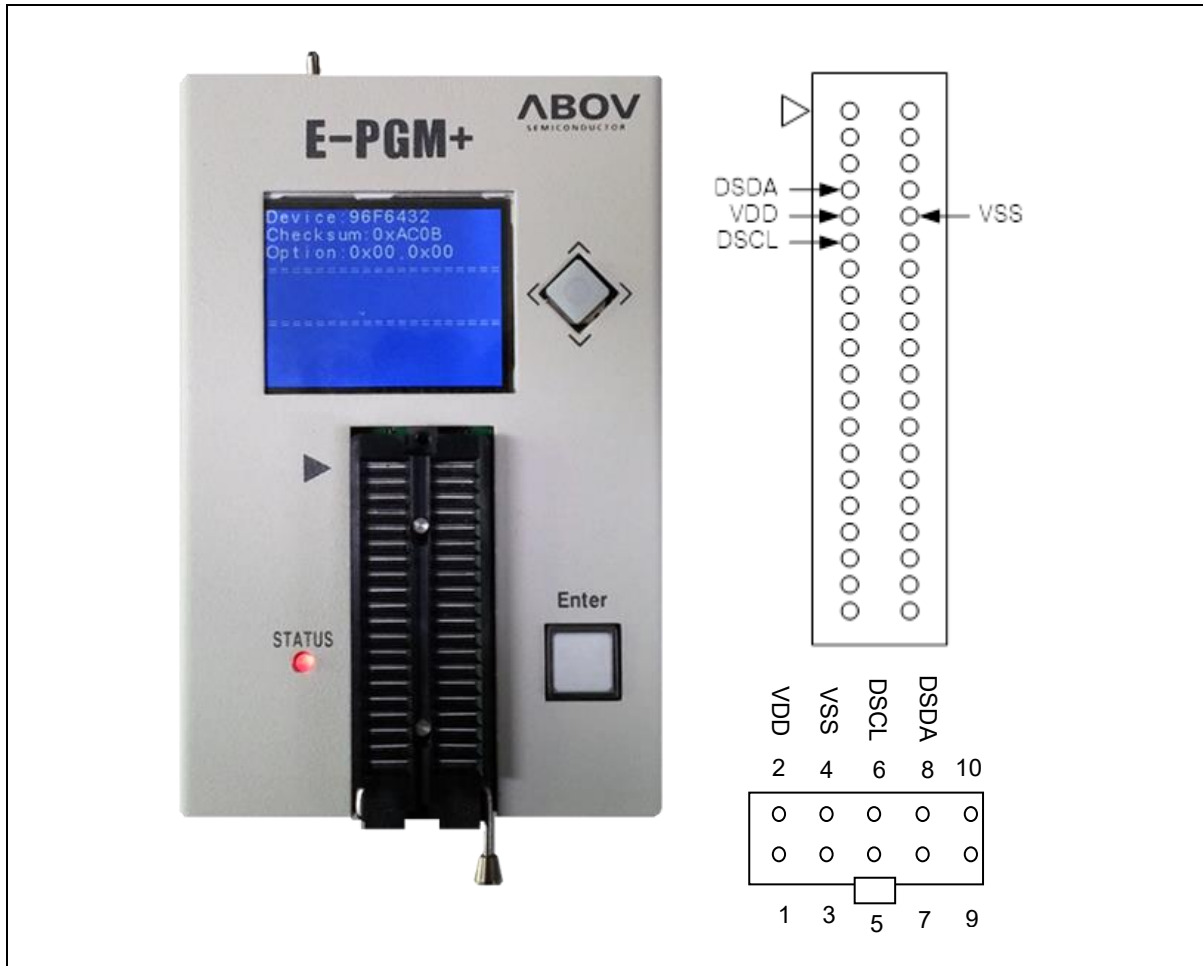


Figure 68. E-PGM+ (Single Writer) and Pinouts

22.4.2 OCD emulator

OCD emulator allows users to write code on the device too, since OCD debugger supports In System Programming (ISP). It doesn't require additional H/W, except developer's target system.

22.4.3 Gang programmer

E-Gang4 and E-Gang6 allow users to program multiple devices simultaneously. They can be run not only in PC controlled mode but also in standalone mode without the PC control.

USB interface is available, and it is easy to connect to the handler.



Figure 69. E-Gang4 and E-Gang6 (for Mass Production)

22.5 Flash programming

Program memory of A96G166/A96A166/A96S166 is a Flash type. The Flash ROM is accessed through four pins such as DSCL, DSDA, VDD and VSS in serial data format. For more information about Flash memory programming, please refer to **20 Memory programming**.

Table 46 introduces corresponding pins and I/O status.

Table 46. Pins for Flash Programming

| Pin name | Main chip pin name | During programming | |
|----------|--------------------|--------------------|--|
| | | I/O | Description |
| DSCL | P01 | I | Serial clock pin. Input only pin. |
| DSDA | P00 | I/O | Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port. |
| VDD, VSS | VDD, VSS | — | Logic power supply pin. |

22.5.1 On-board programming

Microcontroller need only four signal lines including VDD and VSS pins, tor program the Flash ROM using serial protocol. Therefore, on-board programming is possible if the programming signal lines are considered at the time the PCB of application board is designed.

22.6 Connection of transmission

OCD's two-wire communication interfaces use the Open-Drain Method (Wire-AND Bi-Directional I/O).

Normally, it is recommended to place a resistor greater than 4.7kΩ for the DSCL and DSDA respectively. The capacitive load is recommended to be less than 100pF. Outside these ranges, because the communication may not be accomplished, the connection to Debug mode is not guaranteed.

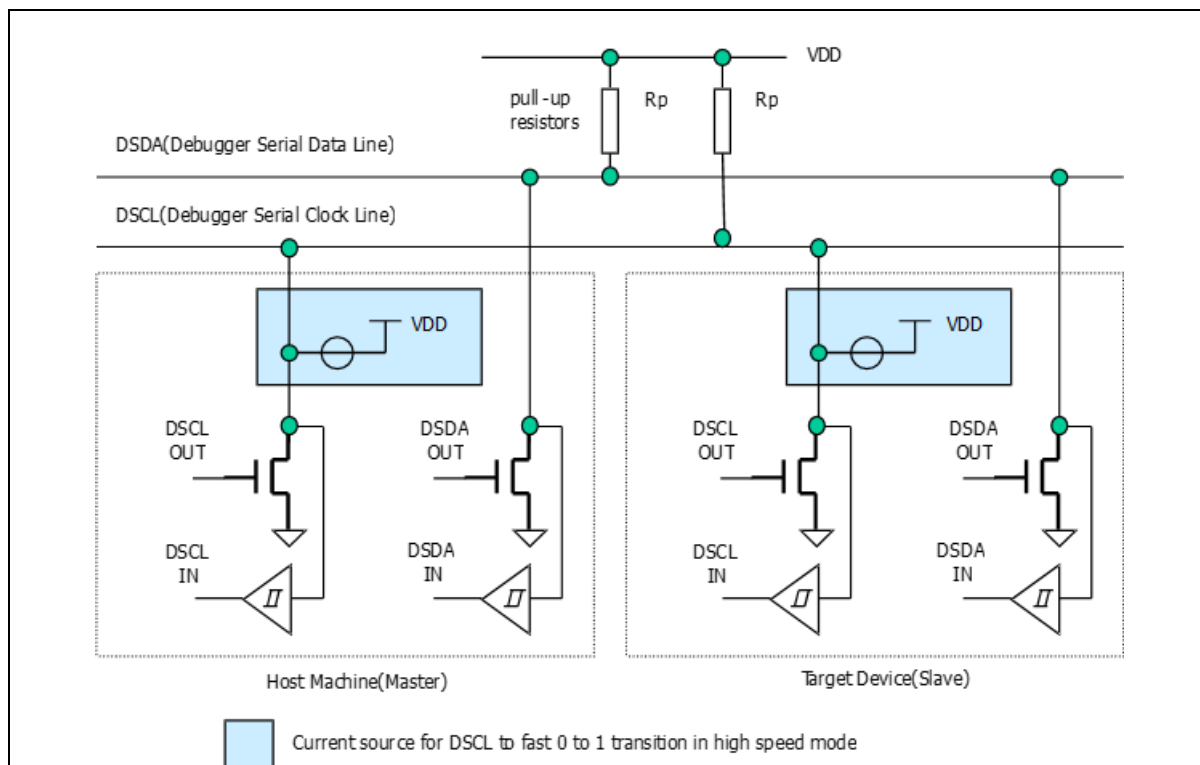


Figure 70. Connection of Transmission

22.7 Circuit design guide

To program Flash memory, programming tools require 4 signal lines, DSCL, DSDA, VDD, and VSS. When designing a PCB circuit, you should consider these 4 signal lines for on-board programming. In addition, you need to be careful when designing the related circuit of these signal pins, because rising/falling timing of the DSCL and DSDA is very important for proper programming.

When you use the OCD pins exclusively or share them with other functions, it needs to be careful, too. Figure 71 shows an example circuit where the OCD pins (DSCL and DSDA) are shared with other functions. They must be connected when debugging or executing In System Program (ISP).

Normally, the OCD pins are connected to outside to execute the predefined functions. Even when they are connected for debugging or executing ISP directly, the OCD pins are shared with other functions by using resistors as shown in Figure 71. By doing this, the OCD pins process the normal external signals and execute the OCD functions first when they are shared.

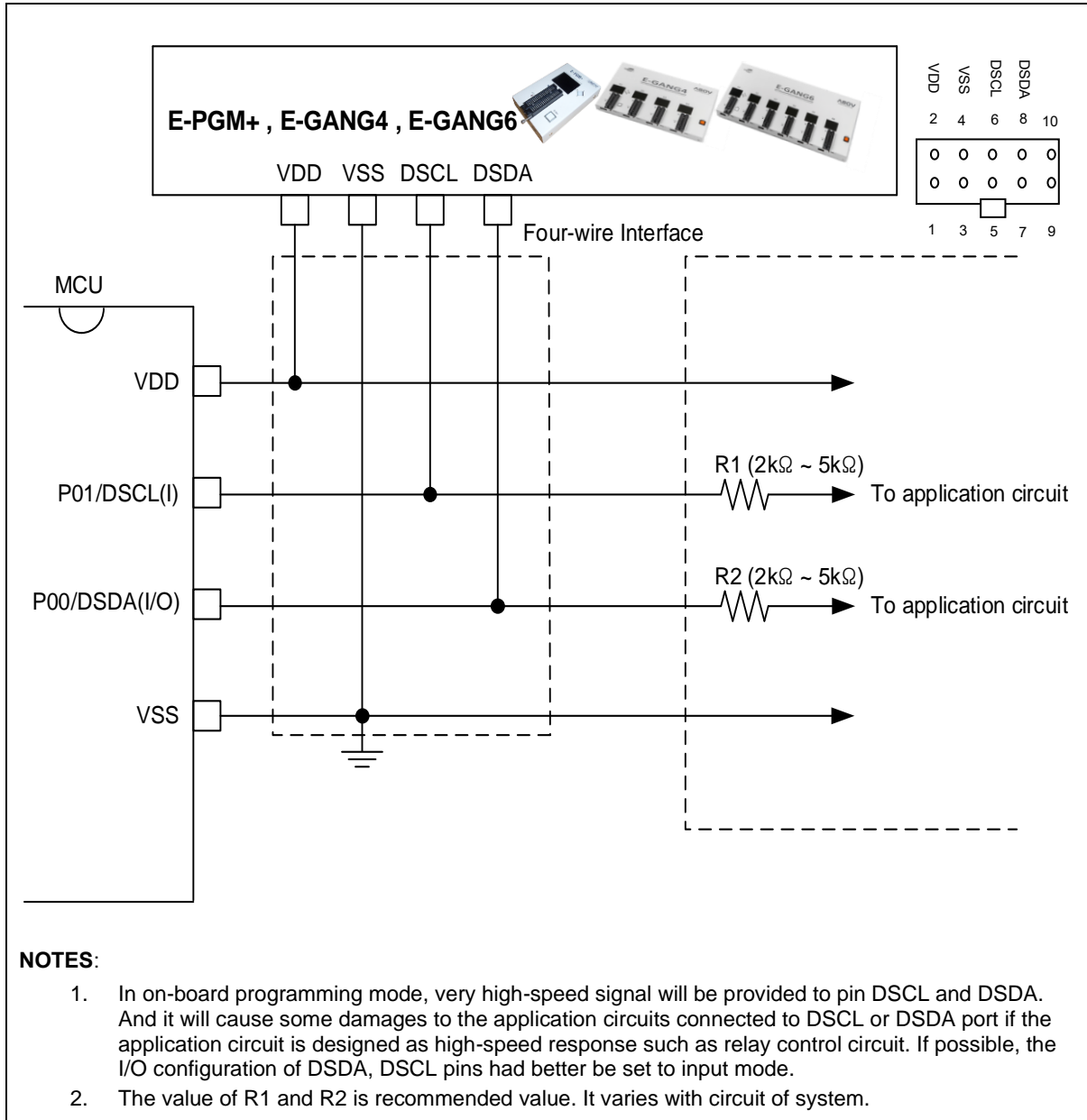


Figure 71. PCB Design Guide for On-Board Programming

23 Package information

This chapter provides A96G166/A96A166/A96S166 package information.

23.1 16 SOPN package information

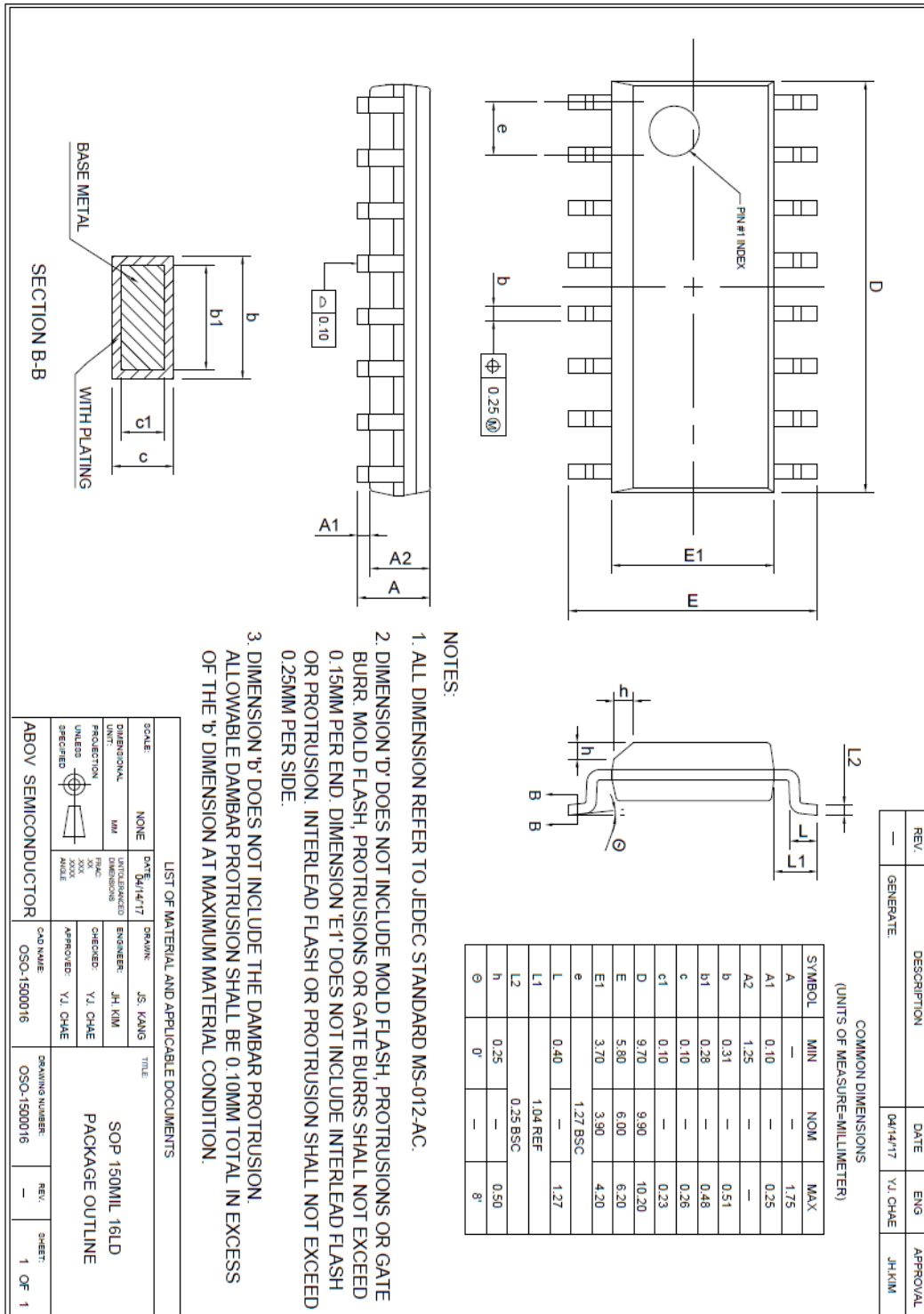


Figure 72 16 SOPN Package Outline

23.2 20 TSSOP package information

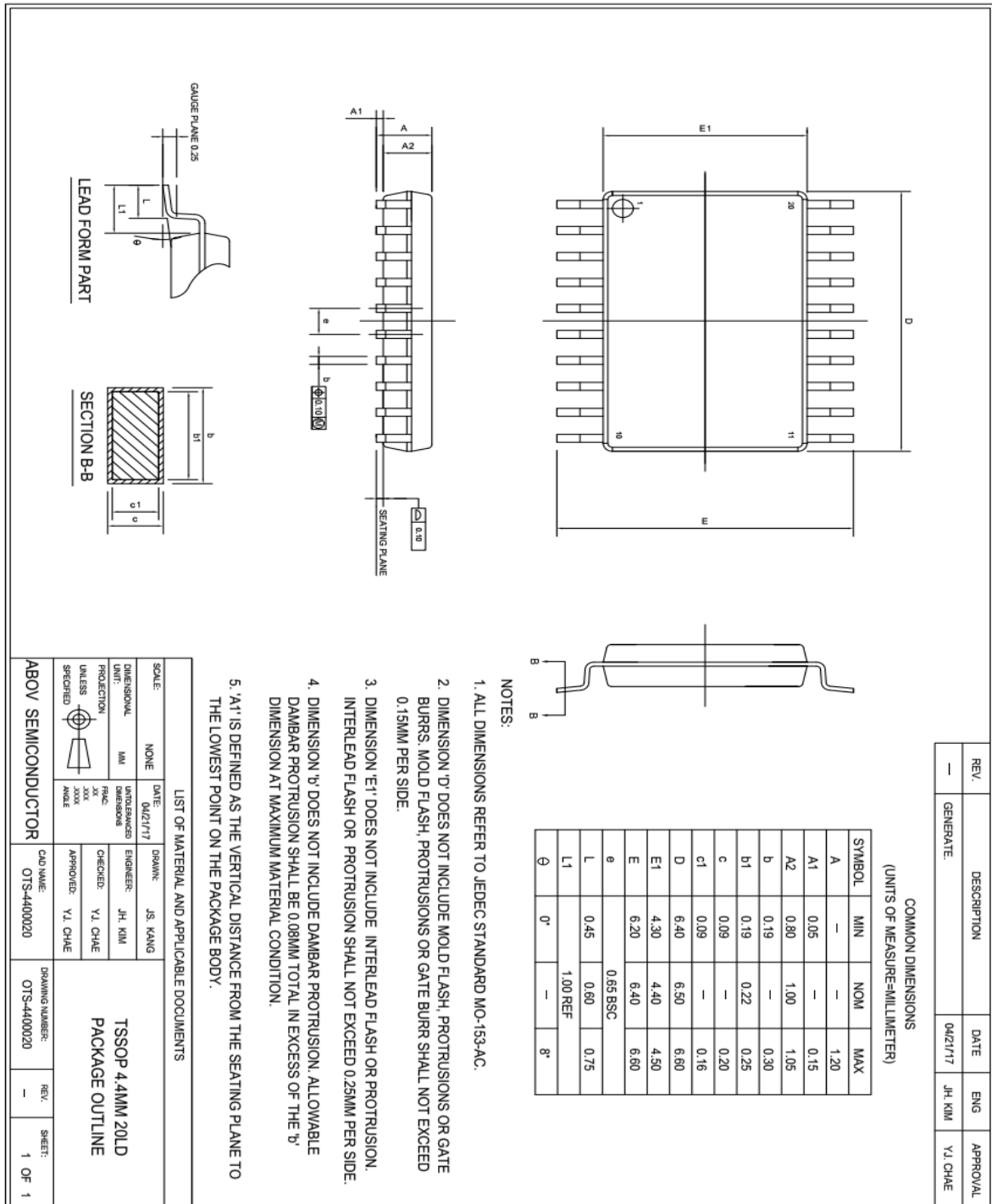


Figure 73. 20 TSSOP Package Outline

23.3 20 SOP package information

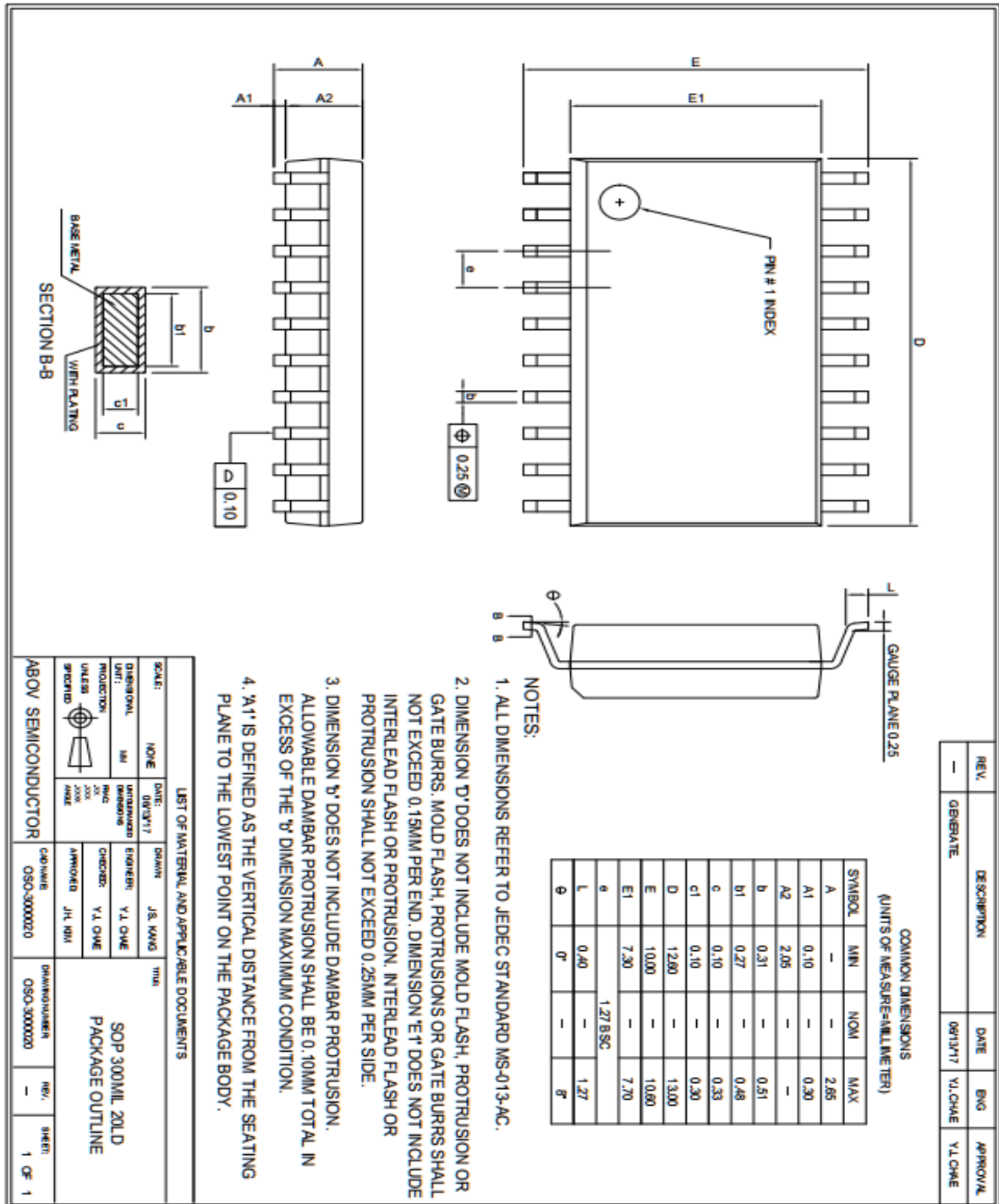


Figure 74. 20 SOP Package Outline

23.4 24 QFN package information

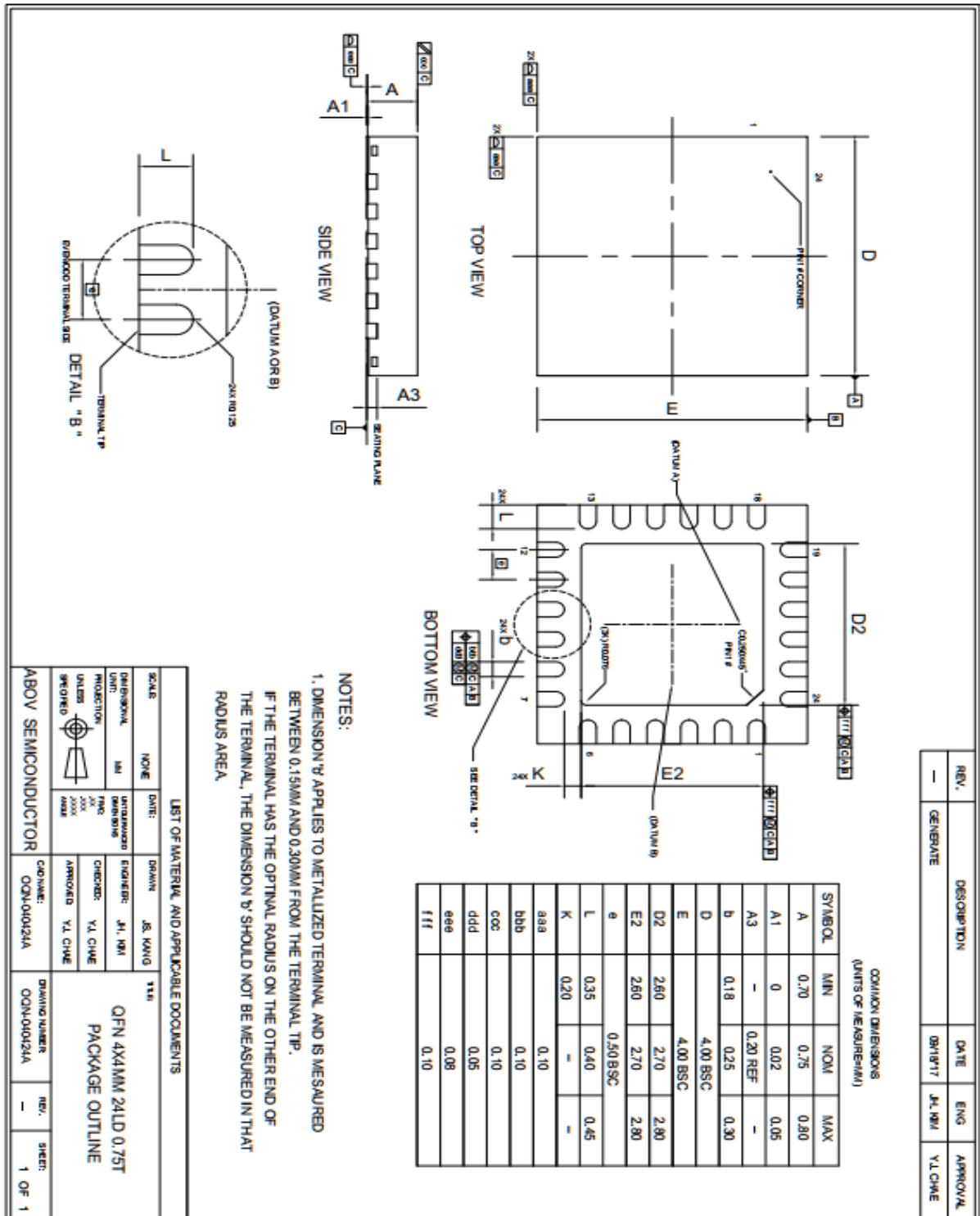


Figure 75. 24 QFN Package Outline

23.5 28 TSSOP package information

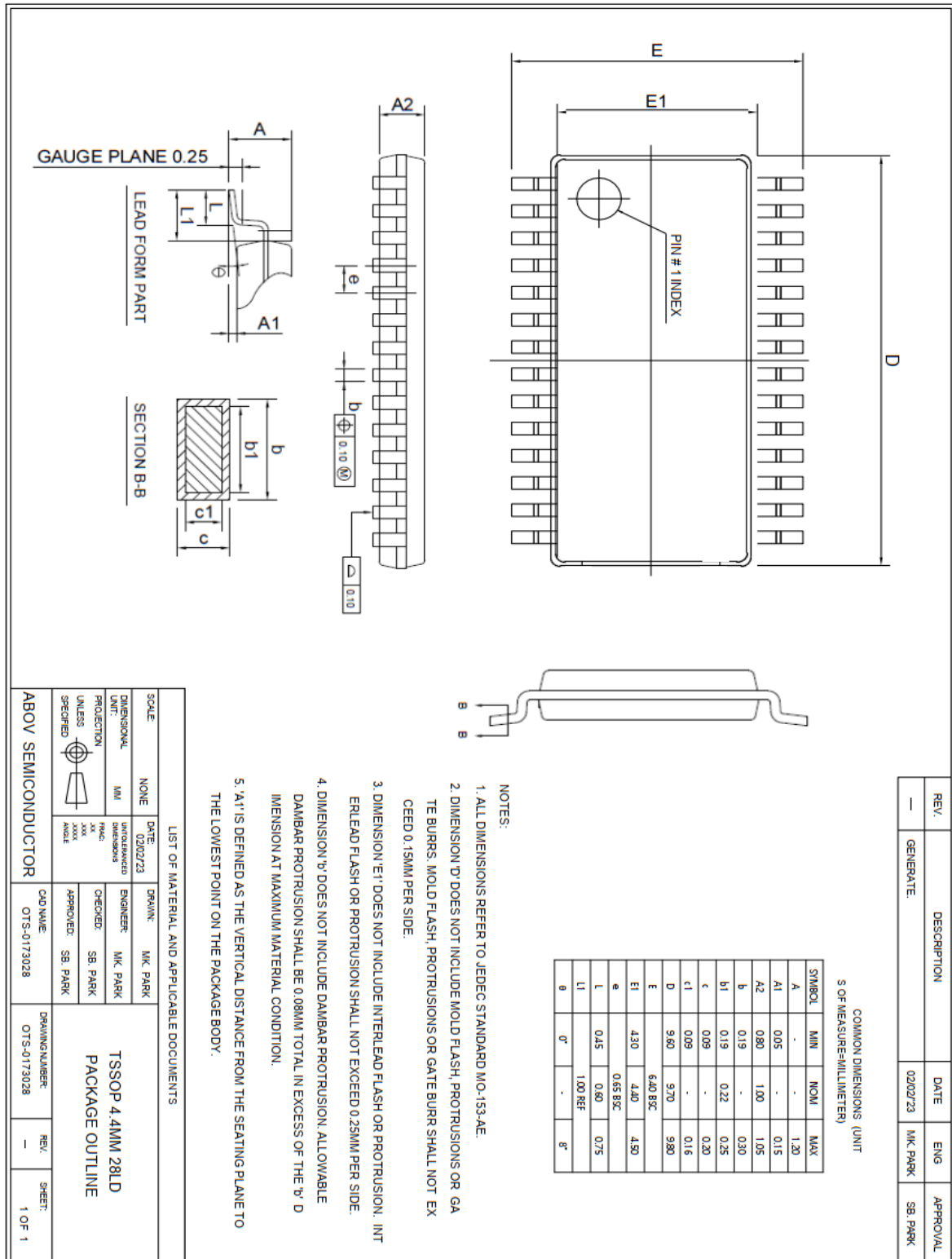


Figure 76. 28 TSSOP Package Outline

23.6 28 SOP package information

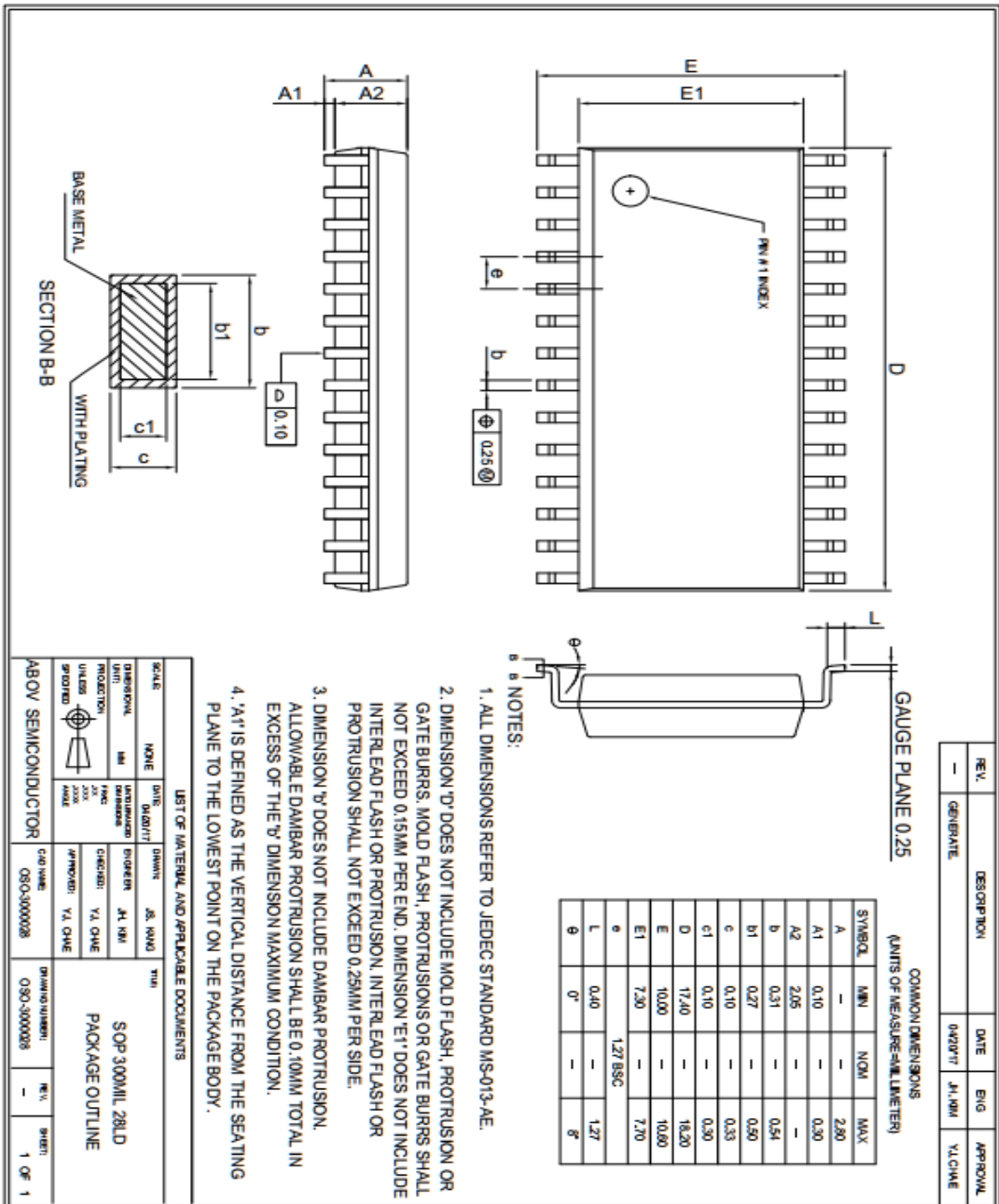


Figure 77. 28 SOP Package Outline

23.7 32 LQFP package information

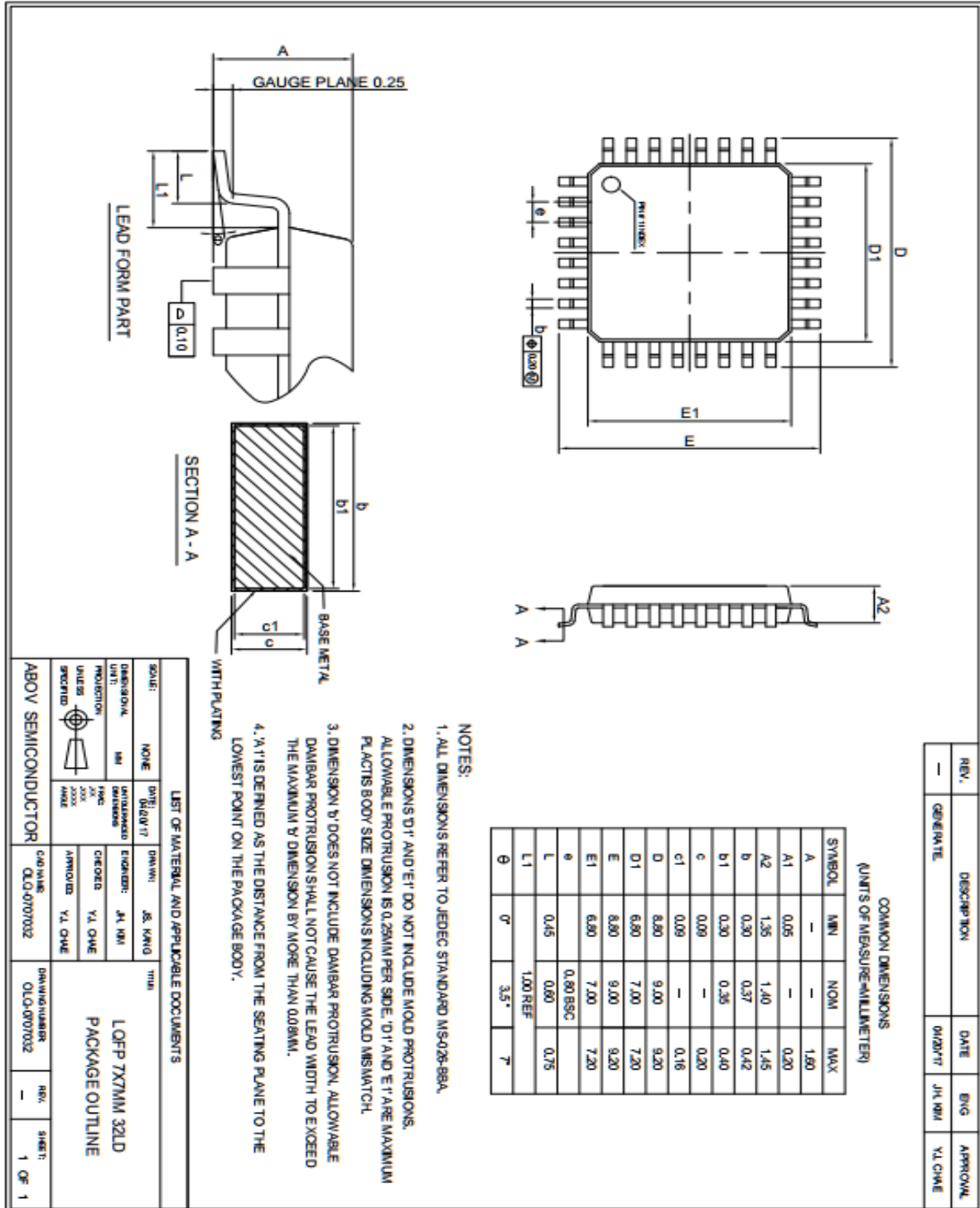


Figure 78. 32 LQFP Package Outline

24 Ordering information

Table 47. A96G166/A96A166/A96S166 Device Ordering Information

| Part number | FLASH | XRAM | IRAM | Timer (PWM) | Communication function | | ADC 12-bit (Channel) | GPIO | High current port | Package | Temperature Range |
|-------------|-------|-----------|----------|-------------|------------------------|----------|----------------------|------|-------------------|-----------|-------------------|
| | | | | | USART | I2C | | | | | |
| A96G166KN | 16KB | 512 bytes | 256bytes | 3 | 2 | 1 | 15 inputs | 30 | 8 | 32 LQFP | -40°C~+85°C |
| A96G166GD | | | | 3 | 2 | 1 | 12 inputs | 26 | 8 | 28 SOP | |
| A96G166GR | | | | 3 | 2 | 1 | 12 inputs | 26 | 8 | 28 TSSOP | |
| A96G166LU* | | | | 3 | 2 | 1 | 11 inputs | 22 | 4 | 24 QFN | |
| A96G166FD | | | | 3 | 1 | 1 | 8 inputs | 18 | 4 | 20 SOP | |
| A96A166FD | | | | 3 | 2 | 1 | 10 inputs | 18 | 2 | 20 SOP | |
| A96G166FR | | | | 3 | 1 | 1 | 8 inputs | 18 | 4 | 20 TSSOP | |
| A96S166FR* | | | | 3 | 1 | 1 | 8 inputs | 18 | 4 | 20 TSSOP | |
| A96G166AE* | | | | 3 | 2 | 1 | 7 inputs | 14 | 3 | 16 SOPN | |
| A96G166KN2 | | | | 16KB | 512 bytes | 256bytes | 3 | 2 | 1 | 15 inputs | |
| A96G166GD2 | 3 | 2 | 1 | | | | 12 inputs | 26 | 8 | 28 SOP | |
| A96G166GR2 | 3 | 2 | 1 | | | | 12 inputs | 26 | 8 | 28 TSSOP | |
| A96G166LU2* | 3 | 2 | 1 | | | | 11 inputs | 22 | 4 | 24 QFN | |
| A96G166FD2 | 3 | 1 | 1 | | | | 8 inputs | 18 | 4 | 20 SOP | |
| A96A166FD2 | 3 | 2 | 1 | | | | 10 inputs | 18 | 2 | 20 SOP | |
| A96G166FR2 | 3 | 1 | 1 | | | | 8 inputs | 18 | 4 | 20 TSSOP | |
| A96S166FR2* | 3 | 1 | 1 | | | | 8 inputs | 18 | 4 | 20 TSSOP | |
| A96G166AE* | 3 | 2 | 1 | | | | 7 inputs | 14 | 3 | 16 SOPN | |

* For available options or further information on the devices with “*” marks, please contact [the ABOV sales offices](#).

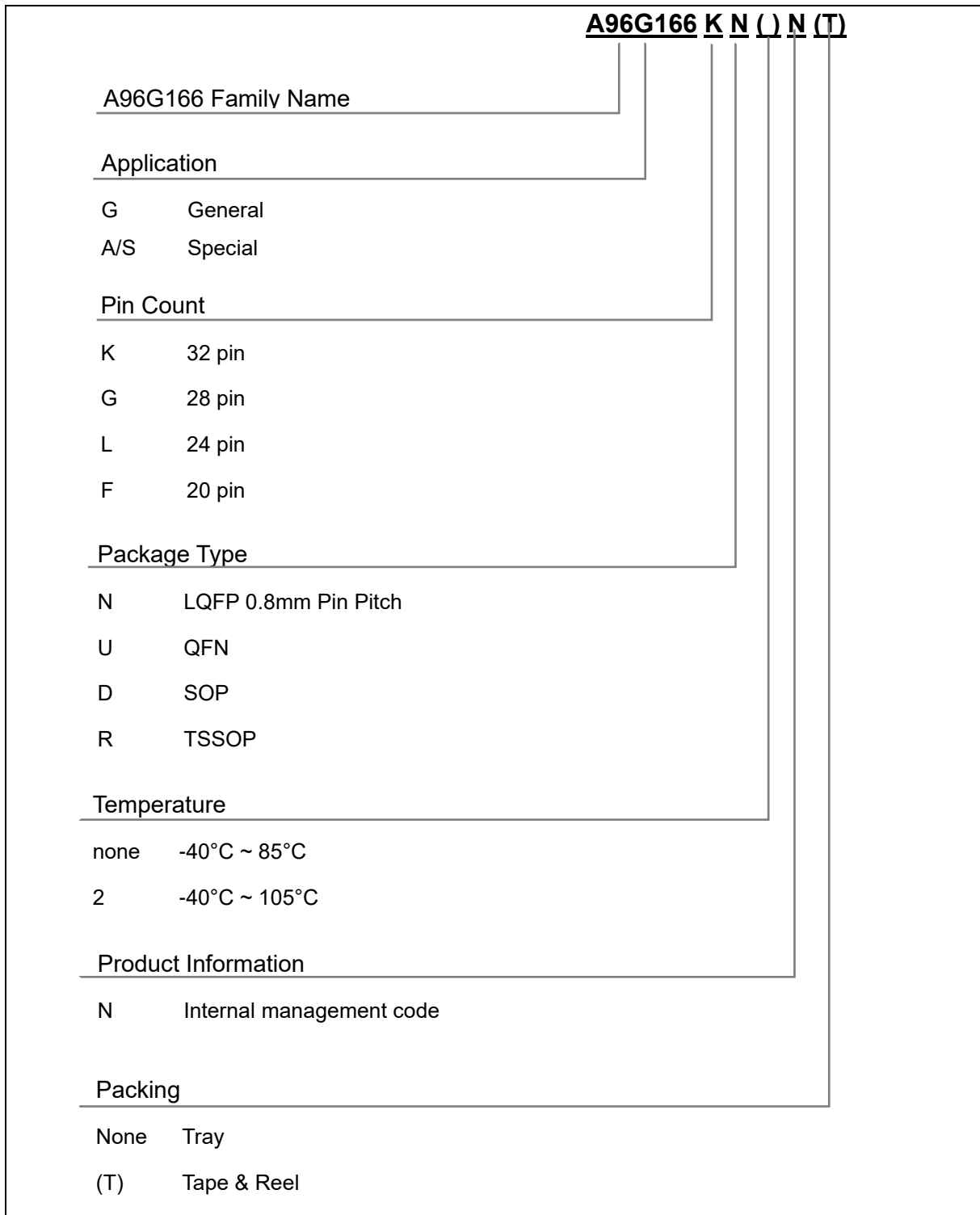


Figure 79. A96G166/A96A166/A96S166 Device Numbering Nomenclature

Appendix

Instruction table

Instructions are either 1, 2 or 3 bytes long as listed in the 'Bytes' column below. Each instruction takes either 1, 2 or 4 machine cycles to execute as listed in the following table. 1 machine cycle comprises 2 system clock cycles.

Table 48. Instruction Table

| ARITHMETIC | | | | |
|-------------------|---|--------------|---------------|-----------------|
| Mnemonic | Description | Bytes | Cycles | Hex code |
| ADD A,Rn | Add register to A | 1 | 1 | 28-2F |
| ADD A,dir | Add direct byte to A | 2 | 1 | 25 |
| ADD A,@Ri | Add indirect memory to A | 1 | 1 | 26-27 |
| ADD A,#data | Add immediate to A | 2 | 1 | 24 |
| ADDC A,Rn | Add register to A with carry | 1 | 1 | 38-3F |
| ADDC A,dir | Add direct byte to A with carry | 2 | 1 | 35 |
| ADDC A,@Ri | Add indirect memory to A with carry | 1 | 1 | 36-37 |
| ADDC A,#data | Add immediate to A with carry | 2 | 1 | 34 |
| SUBB A,Rn | Subtract register from A with borrow | 1 | 1 | 98-9F |
| SUBB A,dir | Subtract direct byte from A with borrow | 2 | 1 | 95 |
| SUBB A,@Ri | Subtract indirect memory from A with borrow | 1 | 1 | 96-97 |
| SUBB A,#data | Subtract immediate from A with borrow | 2 | 1 | 94 |
| INC A | Increment A | 1 | 1 | 04 |
| INC Rn | Increment register | 1 | 1 | 08-0F |
| INC dir | Increment direct byte | 2 | 1 | 05 |
| INC @Ri | Increment indirect memory | 1 | 1 | 06-07 |
| DEC A | Decrement A | 1 | 1 | 14 |
| DEC Rn | Decrement register | 1 | 1 | 18-1F |
| DEC dir | Decrement direct byte | 2 | 1 | 15 |
| DEC @Ri | Decrement indirect memory | 1 | 1 | 16-17 |
| INC DPTR | Increment data pointer | 1 | 2 | A3 |
| MUL AB | Multiply A by B | 1 | 4 | A4 |
| DIV AB | Divide A by B | 1 | 4 | 84 |
| DAA | Decimal Adjust A | 1 | 1 | D4 |

Table 48. Instruction Table (continued)

| LOGICAL | | | | |
|---------------|---------------------------------------|-------|--------|----------|
| Mnemonic | Description | Bytes | Cycles | Hex code |
| ANL A,Rn | AND register to A | 1 | 1 | 58-5F |
| ANL A,dir | AND direct byte to A | 2 | 1 | 55 |
| ANL A,@Ri | AND indirect memory to A | 1 | 1 | 56-57 |
| ANL A,#data | AND immediate to A | 2 | 1 | 54 |
| ANL dir,A | AND A to direct byte | 2 | 1 | 52 |
| ANL dir,#data | AND immediate to direct byte | 3 | 2 | 53 |
| ORL A,Rn | OR register to A | 1 | 1 | 48-4F |
| ORL A,dir | OR direct byte to A | 2 | 1 | 45 |
| ORL A,@Ri | OR indirect memory to A | 1 | 1 | 46-47 |
| ORL A,#data | OR immediate to A | 2 | 1 | 44 |
| ORL dir,A | OR A to direct byte | 2 | 1 | 42 |
| ORL dir,#data | OR immediate to direct byte | 3 | 2 | 43 |
| XRL A,Rn | Exclusive-OR register to A | 1 | 1 | 68-6F |
| XRL A,dir | Exclusive-OR direct byte to A | 2 | 1 | 65 |
| XRL A,@Ri | Exclusive-OR indirect memory to A | 1 | 1 | 66-67 |
| XRL A,#data | Exclusive-OR immediate to A | 2 | 1 | 64 |
| XRL dir,A | Exclusive-OR A to direct byte | 2 | 1 | 62 |
| XRL dir,#data | Exclusive-OR immediate to direct byte | 3 | 2 | 63 |
| CLR A | Clear A | 1 | 1 | E4 |
| CPL A | Complement A | 1 | 1 | F4 |
| SWAP A | Swap Nibbles of A | 1 | 1 | C4 |
| RL A | Rotate A left | 1 | 1 | 23 |
| RLC A | Rotate A left through carry | 1 | 1 | 33 |
| RR A | Rotate A right | 1 | 1 | 03 |
| RRC A | Rotate A right through carry | 1 | 1 | 13 |

Table 48. Instruction Table (continued)

| DATA TRANSFER | | | | |
|----------------|---------------------------------------|-------|--------|----------|
| Mnemonic | Description | Bytes | Cycles | Hex code |
| MOV A,Rn | Move register to A | 1 | 1 | E8-EF |
| MOV A,dir | Move direct byte to A | 2 | 1 | E5 |
| MOV A,@Ri | Move indirect memory to A | 1 | 1 | E6-E7 |
| MOV A,#data | Move immediate to A | 2 | 1 | 74 |
| MOV Rn,A | Move A to register | 1 | 1 | F8-FF |
| MOV Rn,dir | Move direct byte to register | 2 | 2 | A8-AF |
| MOV Rn,#data | Move immediate to register | 2 | 1 | 78-7F |
| MOV dir,A | Move A to direct byte | 2 | 1 | F5 |
| MOV dir,Rn | Move register to direct byte | 2 | 2 | 88-8F |
| MOV dir,dir | Move direct byte to direct byte | 3 | 2 | 85 |
| MOV dir,@Ri | Move indirect memory to direct byte | 2 | 2 | 86-87 |
| MOV dir,#data | Move immediate to direct byte | 3 | 2 | 75 |
| MOV @Ri,A | Move A to indirect memory | 1 | 1 | F6-F7 |
| MOV @Ri,dir | Move direct byte to indirect memory | 2 | 2 | A6-A7 |
| MOV @Ri,#data | Move immediate to indirect memory | 2 | 1 | 76-77 |
| MOV DPTR,#data | Move immediate to data pointer | 3 | 2 | 90 |
| MOVC A,@A+DPTR | Move code byte relative DPTR to A | 1 | 2 | 93 |
| MOVC A,@A+PC | Move code byte relative PC to A | 1 | 2 | 83 |
| MOVX A,@Ri | Move external data(A8) to A | 1 | 2 | E2-E3 |
| MOVX A,@DPTR | Move external data(A16) to A | 1 | 2 | E0 |
| MOVX @Ri,A | Move A to external data(A8) | 1 | 2 | F2-F3 |
| MOVX @DPTR,A | Move A to external data(A16) | 1 | 2 | F0 |
| PUSH dir | Push direct byte onto stack | 2 | 2 | C0 |
| POP dir | Pop direct byte from stack | 2 | 2 | D0 |
| XCH A,Rn | Exchange A and register | 1 | 1 | C8-CF |
| XCH A,dir | Exchange A and direct byte | 2 | 1 | C5 |
| XCH A,@Ri | Exchange A and indirect memory | 1 | 1 | C6-C7 |
| XCHD A,@Ri | Exchange A and indirect memory nibble | 1 | 1 | D6-D7 |

Table 48. Instruction Table (continued)

| BOOLEAN | | | | |
|-----------------|---------------------------------|--------------|---------------|-----------------|
| Mnemonic | Description | Bytes | Cycles | Hex code |
| CLR C | Clear carry | 1 | 1 | C3 |
| CLR bit | Clear direct bit | 2 | 1 | C2 |
| SETB C | Set carry | 1 | 1 | D3 |
| SETB bit | Set direct bit | 2 | 1 | D2 |
| CPL C | Complement carry | 1 | 1 | B3 |
| CPL bit | Complement direct bit | 2 | 1 | B2 |
| ANL C,bit | AND direct bit to carry | 2 | 2 | 82 |
| ANL C,/bit | AND direct bit inverse to carry | 2 | 2 | B0 |
| ORL C,bit | OR direct bit to carry | 2 | 2 | 72 |
| ORL C,/bit | OR direct bit inverse to carry | 2 | 2 | A0 |
| MOV C,bit | Move direct bit to carry | 2 | 1 | A2 |
| MOV bit,C | Move carry to direct bit | 2 | 2 | 92 |

Table 48. Instruction Table (continued)

| BRANCHING | | | | |
|------------------|--|--------------|---------------|-----------------|
| Mnemonic | Description | Bytes | Cycles | Hex code |
| ACALL addr 11 | Absolute jump to subroutine | 2 | 2 | 11→F1 |
| LCALL addr 16 | Long jump to subroutine | 3 | 2 | 12 |
| RET | Return from subroutine | 1 | 2 | 22 |
| RETI | Return from interrupt | 1 | 2 | 32 |
| AJMP addr 11 | Absolute jump unconditional | 2 | 2 | 01→E1 |
| LJMP addr 16 | Long jump unconditional | 3 | 2 | 02 |
| SJMP rel | Short jump (relative address) | 2 | 2 | 80 |
| JC rel | Jump on carry = 1 | 2 | 2 | 40 |
| JNC rel | Jump on carry = 0 | 2 | 2 | 50 |
| JB bit,rel | Jump on direct bit = 1 | 3 | 2 | 20 |
| JNB bit,rel | Jump on direct bit = 0 | 3 | 2 | 30 |
| JBC bit,rel | Jump on direct bit = 1 and clear | 3 | 2 | 10 |
| JMP @A+DPTR | Jump indirect relative DPTR | 1 | 2 | 73 |
| JZ rel | Jump on accumulator = 0 | 2 | 2 | 60 |
| JNZ rel | Jump on accumulator ≠0 | 2 | 2 | 70 |
| CJNE A,dir,rel | Compare A, direct jne relative | 3 | 2 | B5 |
| CJNE A,#d,rel | Compare A, immediate jne relative | 3 | 2 | B4 |
| CJNE Rn,#d,rel | Compare register, immediate jne relative | 3 | 2 | B8-BF |
| CJNE @Ri,#d,rel | Compare indirect, immediate jne relative | 3 | 2 | B6-B7 |
| DJNZ Rn,rel | Decrement register, jnz relative | 2 | 2 | D8-DF |
| DJNZ dir,rel | Decrement direct byte, jnz relative | 3 | 2 | D5 |

Table 48. Instruction Table (continued)

| MISCELLANEOUS | | | | |
|---|--|--------------|---------------|-----------------|
| Mnemonic | Description | Bytes | Cycles | Hex code |
| NOP | No operation | 1 | 1 | 00 |
| ADDITIONAL INSTRUCTIONS (selected through EO[7:4]) | | | | |
| Mnemonic | Description | Bytes | Cycles | Hex code |
| MOVC @(DPTR++), A | M8051W/M8051EW-specific instruction supporting software download into program memory | 1 | 2 | A5 |
| TRAP | Software break command | 1 | 1 | A5 |

In the above table, entries such as E8-EF indicate continuous blocks of hex opcodes used for 8 different registers. Register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as '11→F1' (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the destination address.

CJNE instructions use abbreviation of #d for immediate data; other instructions use #data as an abbreviation.

Revision history

| Date | Revision | Description |
|------------|----------|---|
| 2019.10.29 | 1.00 | First creation |
| 2019.11.07 | 1.01 | Modified temperature specification. Updated "21.3 A/D converter characteristics" on page 67. |
| 2019.12.03 | 1.02 | Updated "21.5 Power on reset characteristics" on page 68. Updated "21.6 Low voltage reset and low voltage indicator characteristics" on page 68. |
| 2020.04.20 | 1.03 | Updated Figure 3 |
| 2020.05.22 | 1.04 | Modified "Low voltage reset and low voltage indicator characteristics" |
| 2020.06.08 | 1.05 | Changed the name of P1DB to P12DB at Table 4. SFR Map Summary. Changed the name of each bit for P12DB at P12DB register description. Corrected the I/O symbol of LED0 ~ LED7 to O at Table 3. Normal Pin Description. Corrected an address typo of FPCR0, RTOCH0 and RTOCL0 register. Deleted AVREF at Figure 26. 12-bit ADC Block Diagram. Deleted Figure 58. A/D Power (AVREF) Pin with a Capacitor. Changed the maximum analog input voltage to VDD at Table 18. A/D Converter Characteristics. Updated Basic Interval Timer Block Diagram at Figure 19. Added the description of V_{LVD}/V_{LVI} at Table 22. LVR and LVI Characteristics. Extended maximum operating temperature up to 105°C as well as 85°C. |
| 2020.07.16 | 1.06 | Enhanced the minimum ADC operation voltage to 2.2V at Table 18. A/D Converter Characteristics. Deleted Analog Reference Voltage item at Table 18. A/D Converter Characteristics. Added the note of "Guaranteed by design" at Table 19. Recommended ADC Resolution. Corrected the conditions of Input High/Low Leakage Current and Supply Current at Table 25. DC Characteristics. Corrected the symbol of package type at Figure 79. A96G166/A96A166/A96S166 Device Numbering Nomenclature. Added 16 SOPN package at Figure 2 A96G166 16SOPN Pin Assignment, Table 3. Normal Pin Description and Figure 72 16 SOPN Package Outline. Added A96G166AE at Table 47. A96G166/A96A166/A96S166 Device Ordering Information. Updated the table and figures for USART characteristics in 21 Electrical characteristics. Corrected the typo for Flash size at Figure 1. A96G166/A96A166/A96S166 Block Diagram. |
| 2020.07.31 | 1.07 | Corrected the typo of P2FSRH and P3FSRL at 5.3 P2 port and 5.4 P3 port paragraph. |
| 2020.08.31 | 1.08 | Advanced Flash Endurance times from 10,000 to 30,000. |
| 2020.09.28 | 1.09 | Updated the initial value in Table 6. SFR Map. |
| 2021.01.13 | 1.10 | Added a new device of A96A166FD. Modified the bit position of EIPOL1 at 6.11.6 Interrupt register description. Modified the invalid number of USART at Table 2. A96G166/A96A166/A96S166 Device Features and Peripheral Counts. |

| | | |
|------------|------|---|
| 2021.04.02 | 1.11 | Corrected the typo of P3FSRL and IE2 at 6.5.2 Register description for P3 and 7.11.1 Interrupt Enable Register (IE, IE1, IE2, and IE3). |
| 2021.04.22 | 1.12 | Corrected the description of CONFIGURE OPTION 1 register at 19.6 Configure option. Updated High Speed Internal RC Oscillator Tolerance at Table 23. High Speed Internal RC Oscillator Characteristics. Corrected the frequency unit from KHz to kHz. Added details of the feature on page 1. |
| 2021.05.20 | 1.13 | Updated the U1STAT SFR address(0xF8 → 0xF7) |
| 2022.04.11 | 1.14 | Added 4 Central processing unit. Updated 22 Development tools chapter. Marked simulation data in 21 Electrical characteristics. Added Figure 51. Filters used on a Reset Pin Diagram and Table 36 Reset Pin Component Values on page 85. Deleted the table of Input/Output Capacitance in Electrical Characteristics. Corrected the address of UnSTAT at Figure 29. USARTn Block Diagram(n=0,1). Corrected the description for WDTRTI of WDTCR register in User's Manual. |
| 2022.08.19 | 1.15 | Corrected the order of Configure option registers. Corrected the description of CONFIGURE OPTION 3 register. |
| 2022.10.13 | 1.16 | Revised the font of this document |
| 2023.03.31 | 1.17 | Corrected the graph of Figure 52~ Figure 56 at 21.22 Typical Characteristics Modified the A96G166 24 QFN Pin Assignment. Updated External resetb input time |
| 2023.07.12 | 1.18 | Updated the A96G166 28 TSSOP Pin Assignment |

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