A94B114

CMOS Single Chip 8-bit MCU with 12-bit ADC Comparator and PWM controlling Dead-band For Small Home Appliance

Datasheet Version 1.04

Features

Core

- 8-bit CISC CM8051-S core
  (8051 Compatible, 1 clocks per cycle)

8 Kbytes On-Chip FLASH

- Endurance : 10,000 times (Sector 0~247)
  50,000 timers (Sector 248~255)
- Retention : 10 years
- In-System Programming (ISP)

256 bytes IRAM / 256 bytes XRAM

General Purpose I/O (GPIO)

- Normal I/O : 18 Port
  (P0[7:0], P1[5:0], P2[3:0])

Timer/Counter

- 8-bit Timer x 1-ch (T0)
- 16-bit Timer x 2-ch (T1, T2)

Programmable Pulse Generation

- Pulse generation (by T1/T2)
- 16-bit PWM with inverters
  and Dead-band control x 1ch (by T1)

Comparator

- Selectable internal reference Comparator.
- External (CMN0, CMN1)
- Internal (1.6V, 2.2V)

Watchdog Timer (WDT)

- 8-bit x 1-ch
- RCWDT with LFO

USART

- 8-bit× 1-ch

I2C

- 8-bit× 1-ch

12-bit A/D Converter

- 10 Input channels

Power Down Mode

- IDLE, STOP mode

Sub-Active mode

- System used by internal 128kHz Ring oscillator (LFO/2)

Power On Reset

- Reset release level (1.4V)

Low Voltage Reset

- 1 level detect (1.75)

Low Voltage Indicator

- 4 level detect (2.40/ 2.90/ 3.90/ 4.20V)

Interrupt Sources

- External Interrupts
- (EINT0~2, EINT10, EINT11, EINT12) (4)
- Timer(0/1/2) (3)
- WDT (1)
- LVI (1)
- USART (2)
- I2C (1)
- ADC (1)
- BIT (1)
- CRC (1)
- Comparator (1)

Internal Oscillator

- Internal High Frequency Oscillator :
  32MHz TYP ±1.5% (TA= 25°C)
- Internal Low Frequency Oscillator :
  256kHz ±10% (TA= -40~+85°C, Normal/IDLE)
  168kHz ±15% (TA= +25°C, STOP)
  168kHz ±20% (TA= -40~+85°C, STOP)

Operating Voltage and Frequency

- 1MHz ~ 16MHz
  Internal Clock : TA= -40~+85°C, VDD=2.0V ~ 5.5V
  External Crystal : TA= -40~+85°C, VDD=2.7V ~ 5.5V

Oscillator Type

- 0.4~16 MHz Crystal or Ceramic for main clock

Minimum Instruction Execution Time

- 62.5ns (@16MHz main clock)

CMOS Single Chip 8-bit MCU with 12-bit ADC Comparator and PWM controlling Dead-band For Small Home Appliance

Operating temperature

- Commercial grade (-40℃ to +85℃)
- Industrial grade (-40℃ to +105℃)

Package Type

- 20-SOP
- 20-TSSOP
- 16-SOPN

Product selection table

Table 1. Device Summary

Part Number	Flash	XRAM	IRAM	ADC 12-bit	Comparator	PWM (Dead-band)	Int. Low Freq. OSC	Package
A94B114FR	8KB	256 bytes	256 bytes	10	1	16-bit x1	256kHz ±10%	20 TSSOP
A94B114FD	8KB	256 bytes	256 bytes	10	1	16-bit x1	256kHz ±10%	20 SOP
A94B114AE	8KB	256 bytes	256 bytes	8	1	16-bit x1	256kHz ±10%	16 SOPN

Contents

List of figures

List of tables

1 Description

A94B114 is an advanced CMOS 8-bit microcontroller with 8Kbytes of FLASH. This is a powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications.

1.1 Device overview

In this section, features of A94B114 and peripheral counts are introduced.

Table 2. A94B114 Device Features and Peripheral Counts

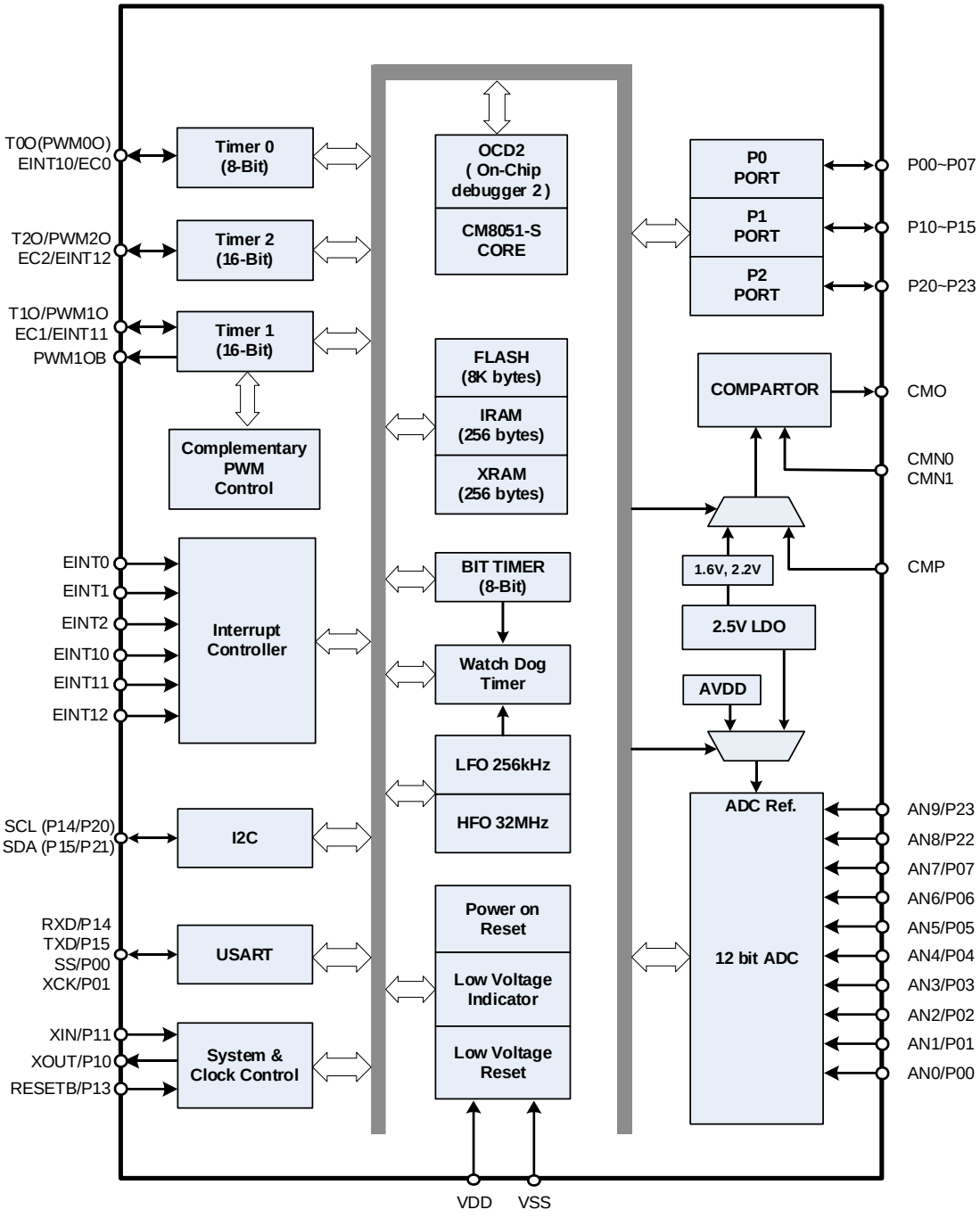
Peripherals		Description
Core	CPU	8-bit CISC CM8051-S core (8051 Compatible, 1 clock per cycle)
	Interrupt	Up to 16 peripheral interrupts supported. • EINT0 to 2, EINT10, EINT11, EINT12 (4) • TIMER (0/1/2) (3) • WDT (1) • LVI (1) • BIT (1) • USART Rx/Tx (2) • I2C (1) • ADC (1) • CRC (1) • COMPARATOR (1)
Memory	ROM (FLASH) capacity	• 8Kbytes FLASH with self-read and write capability • In-system programming (ISP) • Retention : 10 years • Endurance: 10,000times (Sector 0~247) 50,000times (Sector 248~255)
	IRAM	256Bytes
	XRAM	256Bytes
Programmable pulse generation		• Pulse generation (by T1/T2) • 16-bit PWM with inverters and Dead-band control (by T1)
Minimum instruction execution time		• 62.5ns (@ 16MHz main clock)
Power down mode		• STOP mode • IDLE mode
General Purpose I/O (GPIO)		• Normal I/O: 18ports

Table 1. A94B114 Device Features and Peripheral Counts (continued)

Peripherals		Description
Reset	Power on reset	Reset release level: 1.4V
	Low voltage reset	• 1 levels detect • 1.75V
Low voltage indicator		• 4 levels detect • 2.40/2.90/3.90/4.20V
Timer/counter		• Basic interval timer (BIT) 8-bit x 1-ch. • Watchdog timer (WDT) 8-bit x 1-ch. • 8-bit x 1-ch (T0), 16-bit x 2-ch (T1/T2)
Comparator		• Selectable internal reference Comparator • External (CMN0, CMN1) • Internal (1.6V, 2.2V)
Communication function	USART	• 8-bit USART x 1-ch or 8-bit SPI x 1-ch • 0% error baud rate
	I2C	• 8-bit I2C x 1-ch
12-bit A/D converter		10 input channels
Oscillator type		• 0.4MHz to 16MHz crystal or ceramic for main clock
Internal RC oscillator		• HFO 32MHz ±1.5% (T_A=+25°C) • LFO 256KHz ±10%(T_A= -40~ +85°C@Normal/IDLE Mode) • LFO 168KHz ±15%(T_A= +25°C @STOP Mode) • LFO 168KHz ±20%(T_A= -40 ~ +85°C @STOP Mode) • Watchdog Timer RC Oscillator(LFO/2 = 128KHz)
Operating voltage and frequency		• 2.7V to 5.5V @ 0.4MHz to 16MHz with crystal • 2.0V to 5.5V @ 1MHz to 16MHz with internal RC
Operating temperature		-40℃ to +85℃
Package		• Pb-free packages • 20 SOP, 20 TSSOP • 16 SOPN

1.2 A94B114 block diagram

In this section, A94B114 device with peripherals is described in a block diagram.



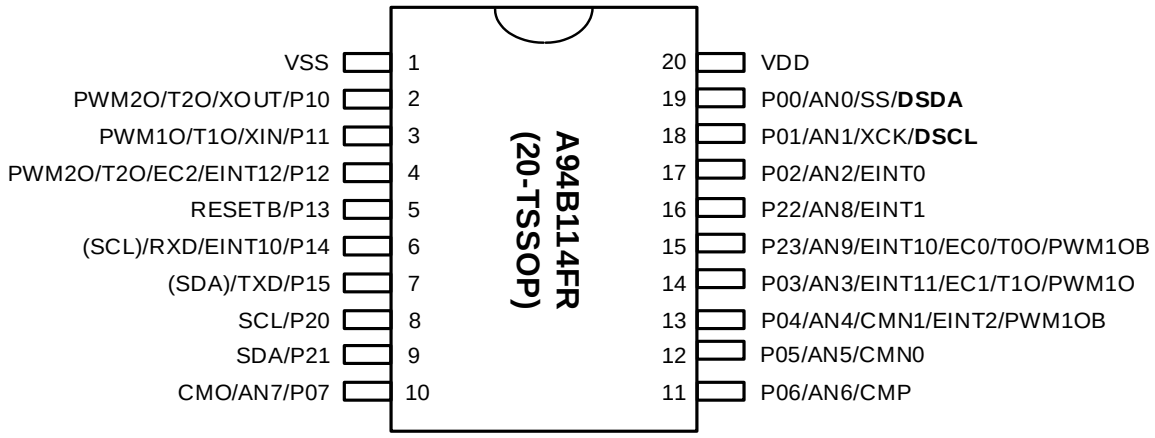
NOTE: The P20, P21, P22 and P23 are not available in the 16-Pin package.

Figure 1. A94B114 Block Diagram

2 Pinouts and pin description

In this chapter, A94B114 device pinouts and pin descriptions are introduced.

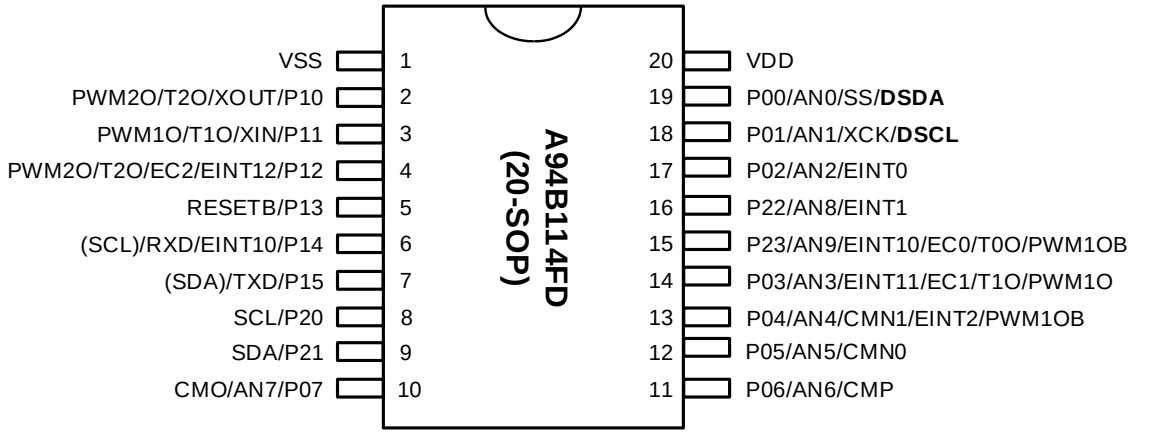
2.1 Pinouts



NOTES:

1. The programmer (PGMplusLC, E-PGM+) uses P0[1:0] pin as DSCL, DSDA.
2. The SDA/SCL lines for I2C can be configured on the P20/P21 (P14/P15) pins by software control.
3. To use T1O/PWM1O as pin3 (P11), set Sub-function and set it to Output High.
4. To use T2O/PWM2O as pin2 (P10), set Sub-function and set it to Output Low.

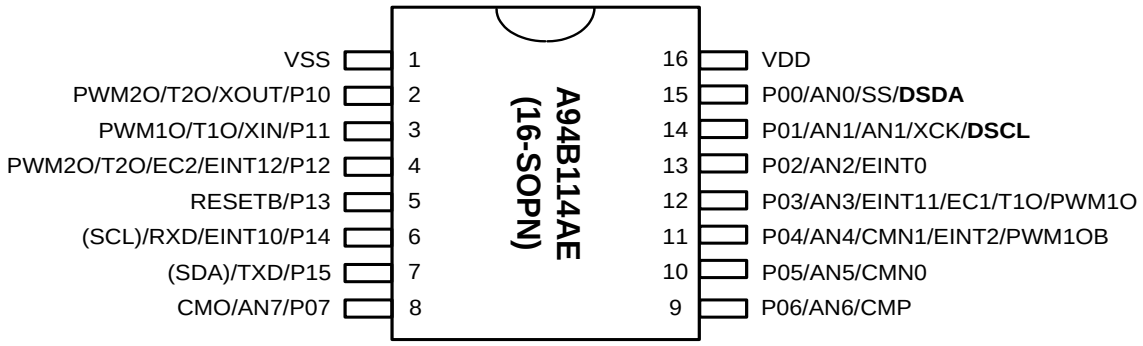
Figure 2. A94B114 20TSSOP Pin Assignment



NOTES:

1. The programmer (PGMplusLC, E-PGM+) uses P0[1:0] pin as DSCL, DSDA.
2. The SDA/SCL lines for I2C can be configured on the P20/P21 (P14/P15) pins by software control.
3. To use T1O/PWM1O as pin3 (P11), set Sub-function and set it to Output High.
4. To use T2O/PWM2O as pin2 (P10), set Sub-function and set it to Output Low.

Figure 3. A94B114FD 20SOP Pin Assignment



NOTES:

1. The programmer (PGMplusLC, E-PGM+) uses P0[1:0] pin as DSCL, DSDA.
2. The P20, P21, P22 and P23 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 16-pin package is used.
3. The SDA/SCL lines for I2C can be configured on the P20/P21 (P14/P15) pins by software control.
4. To use T1O/PWM1O as pin3 (P11), set Sub-function and set it to Output High.
5. To use T2O/PWM2O as pin2 (P10), set Sub-function and set it to Output Low.

Figure 4. A94B114 16SOPN Pin Assignment

2.2 Pin description

Table 3. Normal Pin Description

Pin no.		PIN Name	I/O(1)	Description	Remark
20-pin	16-pin				
19	15	P00*	IOUS	Port 0 bit 0 Input/output	
		AN0	IA	ADC input ch-0	
		SS	IO	USART slave select signal	
		DSDA	IOU	OCD debugger data input/output	Pull-up
18	14	P01*	IOUS	Port 0 bit 1 Input/output	
		AN1	IA	ADC input ch-1	
		XCK	IO	USART clock signal	
		DSCL	IOU	OCD debugger clock	Pull-up
17	13	P02*	IOUS	Port 0 bit 2 Input/output	
		AN2	IA	ADC input ch-2	
		EINT0	I	External interrupt input ch-0	
14	12	P03*	IOUS	Port 0 bit 3 Input/output	
		AN3	IA	ADC input ch-3	
		EINT11	I	External interrupt input ch-11	
		EC1	I	Time 1(Event Capture) input	
		T1O	O	Timer 1 interval output	
		PWM1O	O	Timer 1 PWM output	
13	11	P04*	IOUS	Port 0 bit 4 Input/output	
		AN4	IA	ADC input ch-4	
		EINT2	I	External interrupt input ch-2	
		CMN1	IA	Comparator input channel 1 (-)	
		PWM1OB	O	Timer 1 PWM complementary output	
12	10	P05*	IOUS	Port 0 bit 5 Input/output	
		AN5	IA	ADC input ch-5	
		CMN0	IA	Comparator input channel 0 (-)	
11	9	P06*	IOUS	Port 0 bit 6 Input/output	
		AN6	IA	ADC input ch-6	
		CMP	IA	Comparator input channel (+)	
10	8	P07*	IOUS	Port 0 bit 7 Input/output	
		AN7	IA	ADC input ch-7	
		CMO	OA	Comparator output channel	

Table 4. Normal Pin Description (continued)

Pin no.		PIN Name	I/O[1]	Description	Remark
20-pin	16-pin				
2	2	P10*	IOUS	Port 1 bit 0 Input/output	
		XOUT	O	Main Oscillator Output	
		T2O	O	Timer 2 interval output	
		PWM2O	O	Timer 2 PWM output	
3	3	P11*	IOUS	Port 1 bit 1 Input/output	
		XIN	I	Main Oscillator Input	
		T1O	O	Timer 1 interval output	
		PWM1O	O	Timer 1 PWM output	
4	4	P12*	IOUS	Port 1 bit 2 Input/output	
		EINT12	I	External interrupt input ch-12	
		EC2	I	Timer 2(Event Capture) input	
		T2O	O	Timer 2 Interval output	
		PWM2O	O	Timer 2 PWM output	
5	5	P13*	IOUS	Port 1 bit 3 Input/output	
		RESETB	IU	Reset pin	Pull-up
6	6	P14*	IOUS	Port 1 bit 4 Input/output	
		RXD	I	USART data receive /SPI MISO	
		SCL	IO	I2C clock signal	
		EINT10	I	External interrupt input ch-10	
7	7	P15*	IOUS	Port 1 bit 5 Input/output	
		TXD	O	USART data transmit /SPI MOSI	
		SDA	IO	I2C data signal	
8	-	P20*	IOUS	Port 2 bit 0 Input/output	
		SCL	IO	I2C clock signal	
9	-	P21*	IOUS	Port 2 bit 1 Input/output	
		SDA	IO	I2C data signal	
16	-	P22*	IOUS	Port 2 bit 2 Input/output	
		AN8	IA	ADC input ch-8	
		EINT1	I	External interrupt input ch-1	

Table 5. Normal Pin Description (continued)

Pin no.		PIN Name	I/O(1)	Description	Remark
20-pin	16-pin				
15	-	P23*	IOUS	Port 2 bit 3 Input/output	
		AN9	IA	ADC input ch-9	
		EINT10	I	External interrupt input ch-10	
		EC0	I	Timer 0(Event Capture) input	
		T0O	O	Timer 0 interval output	
		PWM1OB	O	Timer 0 PWM complementary output	
20	16	VDD	P	VDD	
1	1	VSS	P	VSS	

NOTES:

1. The P20, P21, P22 and P23 are not in the 16-Pin package.
2. The P13/RESETB pin is configured as one of the P13 and the RESETB pin by the “CONFIGURE OPTION”.
3. If the P00 and P01 pins are connected to the programmer during power-on reset, the pins are automatically configured as In-System programming pins.
4. The P00 and P01 pins are configured as inputs with internal pull-up resistor only during the reset or power-on reset.
5. (1) I=Input, O=Output, U=Pull-up, D=Pull-down, S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
6. The * means ‘Selected pin function after reset condition

3 Port structures

In this chapter, two port structures are introduced in figures 1 and 2 regarding general purpose I/O port and external interrupt I/O port respectively.

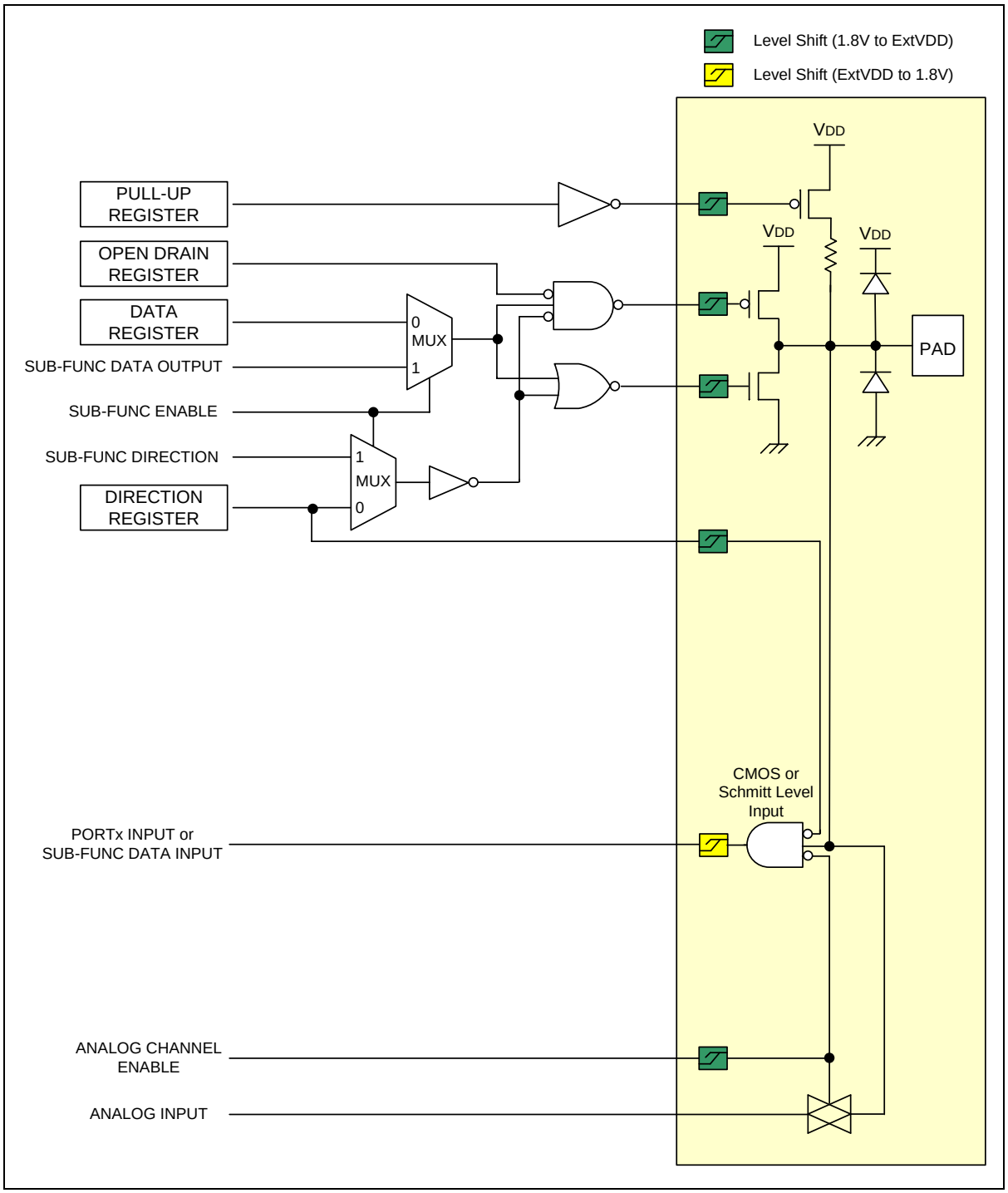


Figure 5. General Purpose I/O Port

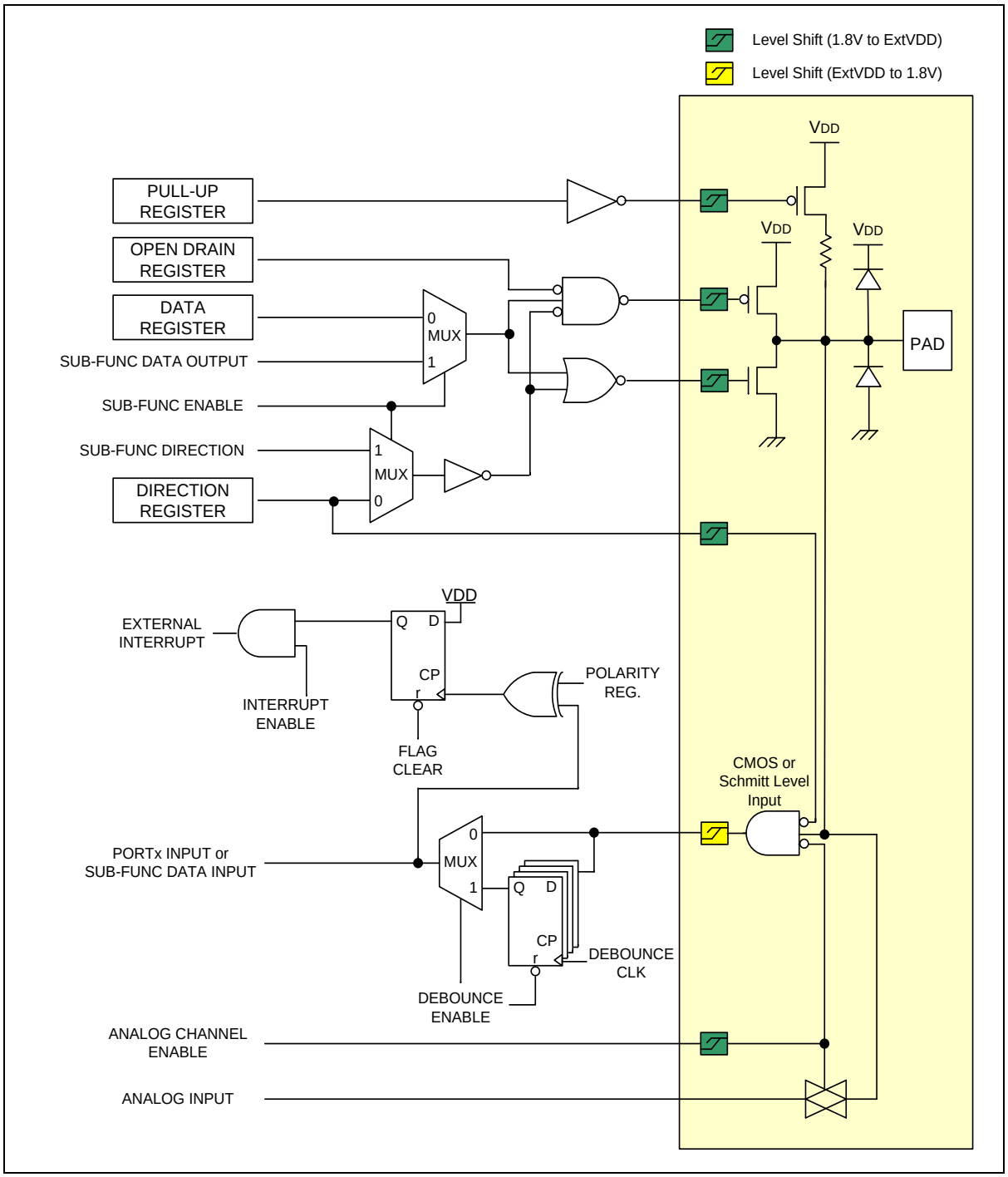


Figure 6. External Interrupt I/O Port

4 Memory organization

A94B114 addresses two separate memory spaces:

- Program memory
- Data memory

By means of this logical separation of the memory, 8-bit CPU address can access the Data Memory more rapidly. 16-bit Data Memory address is generated through the DPTR register.

A94B114 provides on-chip 8Kbytes of the ISP type flash program memory, which readable and writable. Internal data memory (IRAM) is 256bytes and it includes the stack area. External data memory (XRAM) is 256bytes.

4.1 Program memory

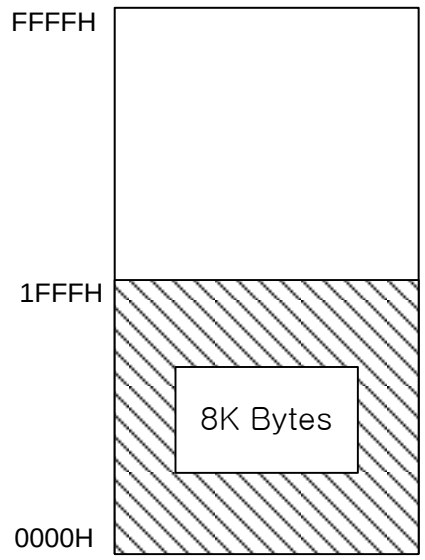
A 16-bit program counter is capable of addressing up to 64Kbytes, and A94B114 has just 8Kbytes program memory space.

Figure 7 shows a map of the lower part of the program memory.

After reset, CPU begins execution from location 0000H. Each interrupt is assigned a fixed location in the program memory. An interrupt causes the CPU to jump to the corresponding location, where it commences execution of the service routine.

An external interrupt 11, for example, is assigned to location 000BH. If the external interrupt 11 is going to be used, its service routine must begin at location 000BH. If the interrupt is not going to be used, its service location is available as general purpose program memory. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within an interval of 8-bytes.

Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.



NOTE: The 8Kbytes includes the Interrupt Vector Region.

Figure 7. Program Memory Map

4.2 Data memory

Internal data memory space is divided into three blocks, which are generally referred to as lower 128bytes, upper 128bytes, and SFR space. Internal data memory addresses are always one byte wide, which implies an address space of 256bytes. In fact, the addressing modes for the internal data memory can accommodate up to 384bytes by using a simple trick. Direct addresses higher than 7FH access one memory space, while indirect addresses higher than 7FH access a different memory space. Thus as shown in figure 10, the upper 128bytes and SFR space occupy the same block of addresses, 80H through FFH, although they are physically separate entities.

The lower 128bytes of RAM are present in all 8051 devices as mapped in figure 11. The lowest 32bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16bytes above the register banks form a block of bit-addressable memory space. The 8051 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All of the bytes in the lower 128bytes can be accessed by either direct or indirect addressing. The upper 128bytes of RAM can only be accessed by indirect addressing. These spaces are used for data RAM and stack.

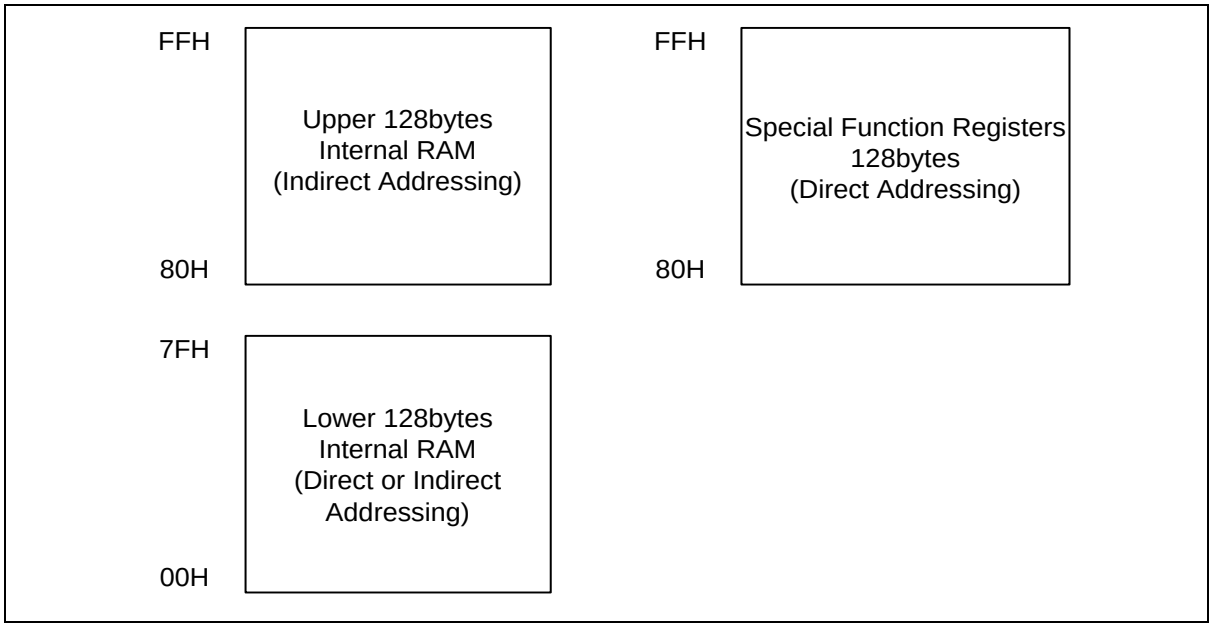


Figure 8. Data Memory Map

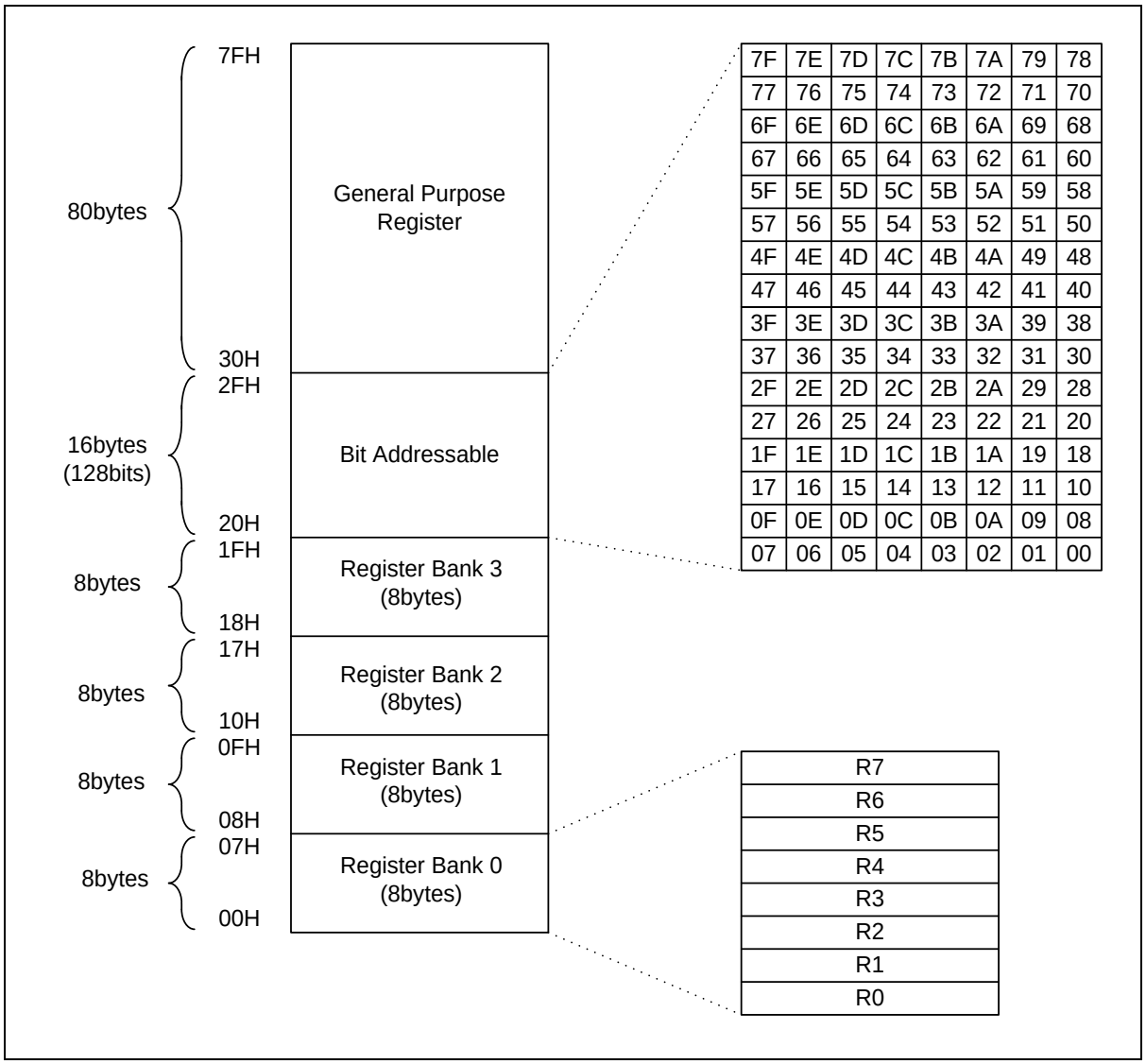
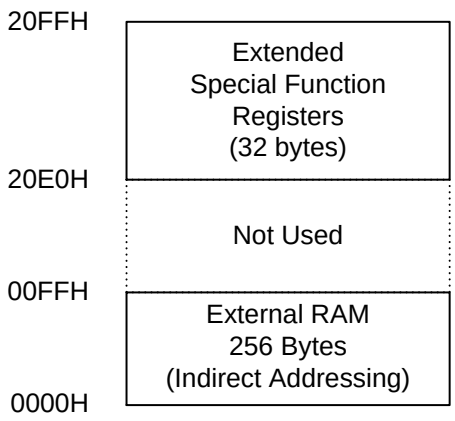


Figure 9. Lower 128bytes of RAM

4.3 External data memory

A94B114 has 256bytes of XRAM and 32bytes XSFR. This area has no relation with RAM/FLASH. It can be read and written to through SFR with 8-bit unit.



NOTE: XSFR (Extended Special Function Registers) can be declared and used as listed in the followings:

```
#define     CRC_CON         *(volatile unsigned char xdata *) 0x20E0
#define     CRC_H           *(volatile unsigned char xdata *) 0x20E3
#define     CRC_L           *(volatile unsigned char xdata *) 0x20E4
```

Figure 10. XDATA Memory Area

4.4 SFR map

4.4.1 SFR map summary

Table 6. SFR Map Summary

—	Reserved
	M8051 compatible

	00H/8H[1]	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
0F8H	I2CSR	I2CMR	I2CSCLLR	I2CSCLHR	I2CSDAHR	I2CDR	I2CSAR	I2CSAR1
0F0H	B	FEMR	FECR	FESR	FETCR	FEARL	FEARM	FEARH
0E8H	IP	IP1	IP2	UCTRL4	FPCR	–	I2CMR1	–
0E0H	ACC	UCTRL1	UCTRL2	UCTRL3	USTAT	UBAUD	UDATA	–
0D8H	OSCCR	SCCR	–	–	–	–	CMPDBT	–
0D0H	PSW	–	–	–	–	–	CMPCR	CMPTR
0C8H	IE2	EIFLAG	–	–	T1CDRL	T1CDRH	T1DDRL	T1DDRH
0C0H	IE1	–	T2CRL	T2CRH	T2ADRL	T2ADRH	T2BDRL	T2BDRH
0B8H	IE	–	T1CRL	T1CRH	T1ADRL	T1ADRH	T1BDRL	T1BDRH
0B0H	IRQ2	–	–	P0FSR_L	P0FSR_H	P1FSR_L	P1FSR_H	P2FSR
0A8H	IRQ1	–	LDOCR	P2IO	P2PU	P2OD	P2DB	–
0A0H	IRQ0	–	EO	P1IO	P1PU	P1OD	P1DB	–
98H	RSFR	–	ILVL	P0IO	P0PU	P0OD	P0DB	–
90H	P2	–	T0CR	T0CNT	T0DR/ T0CDR	ADCM	ADCM1/ ADCRL	ADCRH
88H	P1	LVIR	IOFFSET	EIPOL0	EIPOL1	WDTMR	WDTR/ WDTCR	SYSCON_AR
80H	P0	SP	DPL/ DPL1	DPH/ DPH1	DBTSR	BITCNT	BITCR	PCON

NOTE: 00H/8H, these registers are bit-addressable.

Table 7. XSFR Map Summary

	00H/8H[1]	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
20F8H	–	–	–	–	—	—	—	—
20F0H	–	–	–	–	–	–	—	—
20E8H	–	–	–	CRC_ADDR_START_M	CRC_ADDR_START_L	CRC_ADDR_END_M	CRC_ADDR_END_L	—
20E0H	CRC_CON	–	–	CRC_H	CRC_L	CRC_MNT_H	CRC_MNT_L	—

4.4.2 SFR map

Table 8. SFR Map

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
80H	P0 Data Register	P0	R/W	0	0	0	0	0	0	0	0
81H	Stack Pointer	SP	R/W	0	0	0	0	0	1	1	1
82H	Data Pointer Register Low	DPL	R/W	0	0	0	0	0	0	0	0
83H	Data Pointer Register High	DPH	R/W	0	0	0	0	0	0	0	0
82H	Data Pointer Register Low 1	DPL1	R/W	0	0	0	0	0	0	0	0
83H	Data Pointer Register High 1	DPH1	R/W	0	0	0	0	0	0	0	0
84H	De-bounce Time Selection Register	DBTSR	R/W	0	0	0	0	0	0	0	0
85H	Basic Interval Timer Counter Register	BITCNT	R	0	0	0	0	0	0	0	0
86H	Basic Interval Timer Control Register	BITCR	R/W	0	0	0	0	0	1	0	0
87H	Power Control Register	PCON	R/W	–	–	–	–	0	0	0	0
88H	P1 Data Register	P1	R/W	–	–	0	0	0	0	0	0
89H	Low Voltage Indicator Control Register	LVIR	R/W	0	0	0	0	0	0	0	0
8AH	Interrupt Offset Register	IOFFSET	W	0	0	0	0	0	0	0	0
8BH	External Interrupt Polarity Register 0	EIPOL0	R/W	0	0	0	0	0	0	0	0
8CH	External Interrupt Polarity Register 1	EIPOL1	R	0	0	0	0	0	0	0	0
8DH	Watch Dog Timer Mode Register	WDTMR	R/W	0	0	1	1	1	0	1	1
8EH	Watch Dog Timer Data Register	WTDR	W	1	1	1	1	1	1	1	1
	Watch Dog Timer Counter Register	WTCR	R	0	0	0	0	0	0	0	0
8FH	System Control Access Register	SYSCON_AR	R/W	0	0	0	0	0	0	0	0
90H	P2 Data Register	P2	R/W	–	–	–	–	0	0	0	0
91H	Reserved	–	–	–							
92H	Timer 0 Control Register	T0CR	R/W	0	0	0	0	0	0	0	0
93H	Timer 0 Counter Register	T0CNT	R	0	0	0	0	0	0	0	0
94H	Timer 0 Data Register	T0DR	R/W	1	1	1	1	1	1	1	1
	Timer 0 Capture Data Register	T0CDR	R	0	0	0	0	0	0	0	0
95H	A/D Converter Mode Register	ADCM	R/W	1	0	0	0	1	1	1	1
96H	A/D Converter Mode 1 Register	ADCM1	W	0	0	0	0	0	0	0	1
	A/D Converter Data Low Register	ADCRL	R	0	0	0	0	0	0	0	0
97H	A/D Converter Data High Register	ADCRH	R	0	0	0	0	0	0	0	0
98H	Reset Source Flag Register	RSFR	R/W	1	0	0	0	0	1	0	0
99H	Reserved	–	–	–							
9AH	Interrupt nesting level Register	ILVL	R/W	0	0	0	0	0	0	0	0
9BH	P0 Direction Register	P0IO	R/W	0	0	0	0	0	0	0	0
9CH	P0 Pull-up Resistor Selection Register	P0PU	R/W	0	0	0	0	0	0	0	0
9DH	P0 Open-drain Selection Register	P0OD	R/W	0	0	0	0	0	0	0	0
9EH	P0 De-bounce Time Selection Register	P0DB	R/W	0	0	0	0	0	0	0	0
9FH	Reserved	–	–	–							

Table 8. SFR Map (continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
A0H	Interrupt Request Register 0	IRQ0	0	0	0	0	0	0	0	0	0
A1H	Reserved	–	–	–							
A2H	Extended Operation Register	EO	R/W	–	–	–	–	–	–	–	0
A3H	P1 Direction Register	P1IO	R/W	0	0	0	0	0	0	0	0
A4H	P1 Pull-up Resistor Selection Register	P1PU	R/W	0	0	0	0	0	0	0	0
A5H	P1 Open-drain Selection Register	P1OD	R/W	0	0	0	0	0	0	0	0
A6H	P1 De-bounce Time Selection Register	P1DB	R/W	0	0	0	0	0	0	0	0
A7H	Reserved	–	–	–							
A8H	Interrupt Request Register 1	IRQ1	0	0	0	0	0	0	0	0	0
A9H	Reserved	–	–	–							
AAH	LDO Control Register	LDOCR	R/W	0	0	0	0	0	0	0	0
ABH	P2 Direction Register	P2IO	R/W	0	0	0	0	0	0	0	0
ACH	P2 Pull-up Resistor Selection Register	P2PU	R/W	0	0	0	0	0	0	0	0
ADH	P2 Open-drain Selection Register	P2OD	R/W	0	0	0	0	0	0	0	0
AEH	P2 De-bounce Time Selection Register	P2DB	R/W	0	0	0	0	0	0	0	0
AFH	Reserved	–	–	–							
B0H	Interrupt Request Register 2	IRQ2	R/W	0	0	0	0	0	0	0	0
B1H	Reserved	–	–	–							
B2H	Reserved	–	–	–							
B3H	P0 Function Selection Low Register	P0FSRL	R/W	0	0	0	0	0	0	0	0
B4H	P0 Function Selection High Register	P0FSRH	R/W	0	0	0	0	0	0	0	0
B5H	P1 Function Selection Low Register	P1FSRL	R/W	0	0	0	0	0	0	0	0
B6H	P1 Function Selection High Register	P1FSRH	R/W	0	0	0	0	0	0	0	0
B7H	P2 Function Selection Register	P2FSR	R/W	0	0	0	0	0	0	0	0
B8H	Interrupt Enable Register	IE	R/W	0	–	–	0	0	0	0	0
B9H	Reserved	–	–	–							
BAH	Timer 1 Control Low Register	T1CRL	R/W	0	0	0	0	0	0	0	0
BBH	Timer 1 Counter High Register	T1CRH	R/W	0	0	0	0	0	0	0	0
BCH	Timer 1 A Data Low Register	T1ADRL	R/W	1	1	1	1	1	1	1	1
BDH	Timer 1 A Data High Register	T1ADRH	R/W	1	1	1	1	1	1	1	1
BEH	Timer 1 B Data Low Register	T1BDRL	R/W	1	1	1	1	1	1	1	1
BFH	Timer 1 B Data High Register	T1BDRH	R/W	1	1	1	1	1	1	1	1

Table 8. SFR Map (continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
C0H	Interrupt Enable Register 1	IE1	R/W	–	0	0	0	0	0	0	0
C1H	Reserved	–	–	–							
C2H	Timer 2 Control Low Register	T2CRL	R/W	0	0	0	0	0	0	0	0
C3H	Timer 2 Control High Register	T2CRH	R/W	0	0	0	0	0	0	0	0
C4H	Timer 2 A Data Low Register	T2ADRL	R/W	1	1	1	1	1	1	1	1
C5H	Timer 2 A Data High Register	T2ADRH	R/W	1	1	1	1	1	1	1	1
C6H	Timer 2 B Data Low Register	T2BDRL	R/W	1	1	1	1	1	1	1	1
C7H	Timer 2 B Data High Register	T2BDRH	R/W	1	1	1	1	1	1	1	1
C8H	Interrupt Enable Register 2	IE2	R/W	–	–	–	–	0	0	0	0
C9H	External Interrupt Flag Register	EIFLAG	R/W	–	–	–	–	–	0	0	0
CAH	Reserved	–	–	–							
CBH	Reserved	–	–	–							
CCH	Timer 1 C Data Low Register	T1CDRL	R/W	1	1	1	1	1	1	1	1
CDH	Timer 1 C Data High Register	T1CDRH	R/W	1	1	1	1	1	1	1	1
CEH	Timer 1 D Data Low Register	T1DDRL	R/W	1	1	1	1	1	1	1	1
CFH	Timer 1 D Data High Register	T1DDRH	R/W	1	1	1	1	1	1	1	1
D0H	Program Status Word Register	PSW	R/W	0	0	0	0	0	0	0	0
D1H	Reserved	–	–	–							
D2H	Reserved	–	–	–							
D3H	Reserved	–	–	–							
D4H	Reserved	–	–	–							
D5H	Reserved	–	–	–							
D6H	Comparator Control Register	CMPCR	R/W	0	0	0	0	0	0	0	1
D7H	Comparator Trigger Control Register	CMPTR	R/W	0	0	0	0	0	0	0	0
D8H	Oscillator Control Register	OSCCR	R/W	0	0	0	0	0	1	0	0
D9H	System Clock Control Register	SCCR	R/W	0	1	0	0	0	0	0	0
DAH	Reserved	–	–	–							
DBH	Reserved	–	–	–							
DCH	Reserved	–	–	–							
DDH	Reserved	–	–	–							
DEH	Comparator De-bounce Time Register	CMPDBT	R/W	0	0	0	0	1	1	1	1
DFH	Reserved	–	–	–							

Table 8. SFR Map (continued)

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
E0H	Accumulator Register	ACC	R/W	0	0	0	0	0	0	0	0
E1H	USART Control Register 1	UCTRL1	R/W	0	0	0	0	0	0	0	0
E2H	USART Control Register 2	UCTRL2	R/W	0	0	0	0	0	0	0	0
E3H	USART Control Register 3	UCTRL3	R/W	0	0	0	0	–	0	0	0
E4H	USART Status Register	USTAT	R/W	1	0	0	0	0	0	0	0
E5H	USART Baud Rate Generation Register	UBAUD	R/W	1	1	1	1	1	1	1	1
E6H	USART Data Register	UDATA	R/W	0	0	0	0	0	0	0	0
E7H	Reserved	–	–	–							
E8H	Interrupt Priority Register	IP	R/W	0	0	0	0	0	0	0	0
E9H	Interrupt Priority Register 1	IP1	R/W	0	0	0	0	0	0	0	0
EAH	Interrupt Priority Register 2	IP2	R/W	0	0	0	0	0	0	0	0
EBH	USART Control Register 4	UCTRL4	R/W	0	0	0	0	–	0	0	0
ECH	USART Floating Point Counter	FPCR	R/W	0	0	0	0	0	0	0	0
EDH	Reserved	–	–	–							
EEH	I2C Mode Register 1	I2CMR1	R/W	0	0	0	0	0	0	0	0
EFH	Reserved	–	–	–							
F0H	B Register	B	R/W	0	0	0	0	0	0	0	0
F1H	Flash Mode Register	FEMR	R/W	0	0	0	0	0	0	0	0
F2H	Flash Control Register	FECR	R/W	0	0	0	0	0	0	1	1
F3H	Flash Status Register	FESR	R/W	1	0	0	0	0	0	0	0
F4H	Flash Time Control Register	FETCR	R/W	0	0	0	0	0	0	0	0
F5H	Flash Address Low Register	FEARL	R/W	0	0	0	0	0	0	0	0
F6H	Flash Address Middle Register	FEARM	R/W	0	0	0	0	0	0	0	0
F7H	Flash Address High Register	FEARH	R/W	0	0	0	0	0	0	0	0
F8H	I2C Status Register	I2CSR	R/W	0	0	0	0	0	0	0	0
F9H	I2C Mode Register	I2CMR	R/W	0	0	0	0	0	0	0	0
FAH	I2C SCL Low Period Register	I2CSCLLR	R/W	0	0	0	0	0	0	0	0
FBH	I2C SCL High Period Register	I2CSCLHR	R/W	0	0	1	1	1	1	1	1
FCH	I2C SDA Hold Time Register	I2CSDAHR	R/W	0	0	0	0	0	0	0	0
FDH	I2C Data Register	I2CDR	R/W	1	1	1	1	1	1	1	1
FEH	I2C Slave Address Register	I2CSAR	R/W	0	0	0	0	0	0	0	0
FFH	I2C Slave Address 1 Register	I2CSAR1	R/W	0	0	0	0	0	0	0	0

Table 9. XSFR Map

Address	Function	Symbol	R/W	@Reset							
				7	6	5	4	3	2	1	0
20E0H	CRC Control Register	CRC_CON	R/W	0	0	0	0	0	0	0	0
20E1H	Reserved	–	–	–							
20E2H	Reserved	–	–	–							
20E3H	CRC High Register	CRC_H	R/W	0	0	0	0	0	0	0	0
20E4H	CRC Low Register	CRC_L	R/W	0	0	0	0	0	0	0	0
20E5H	CRC Monitor High Register	CRC_MNT_H	R/W	0	0	0	0	0	0	0	0
20E6H	CRC Monitor Low Register	CRC_MNT_L	R/W	0	0	0	0	0	0	0	0
20E7H	Reserved	–	–	–							
20E8H	Reserved	–	–	–							
20E9H	Reserved	–	–	–							
20EAH	Reserved	–	–	–							
20EBH	CRC Start Address Middle Register	CRC_ADDR_START_M	R/W	0	0	0	0	0	0	0	0
20ECH	CRC Start Address Low Register	CRC_ADDR_START_L	R/W	0	0	0	0	0	0	0	0
20EDH	CRC End Address Middle Register	CRC_ADDR_END_M	R/W	0	0	0	0	0	0	0	0
20EEH	CRC End Address Low Register	CRC_ADDR_END_L	R/W	0	0	0	0	0	0	0	0
20EFH	Reserved	–	–	–							
20F0H	Reserved	–	–	–							
20F1H	Reserved	–	–	–							
20F2H	Reserved	–	–	–							
20F3H	Reserved	–	–	–							
20F4H	Reserved	–	–	–							
20F5H	Reserved	–	–	–							
20F8H	Reserved	–	–	–							
20F9H	Reserved	–	–	–							
20FAH	Reserved	–	–	–							
20FBH	Reserved	–	–	–							
20FCH	Reserved	–	–	–							
20FDH	Reserved	–	–	–							
20FEH	Reserved	–	–	–							
20FFH	Reserved	–	–	–							

5 I/O ports

A94B114 has four groups of I/O ports (P0 ~ P2). Each port can be easily configured by software as I/O pin, internal pull up and open-drain pin to meet various system configurations and design requirements. P0, P1 and P2 includes a function that can generate interrupt signals according to state of a pin.

5.1 P0 port

5.1.1 P0 port description

P0 is an 8-bit I/O port. P0 control registers consist of P0 data register (P0), P0 direction register (P0IO), P0 debounce enable register (P0DB), P0 pull-up resistor selection register (P0PU), and P0 open-drain selection register (P0OD). Refer to the port function selection registers for the P0 function selection.

5.2 P1 port

5.2.1 P1 port description

P1 is a 6-bit I/O port. P1 control registers consist of P1 data register (P1), P1 direction register (P1IO), P1 debounce enable register (P1DB), P1 pull-up resistor selection register (P1PU), and P1 open-drain selection register (P1OD). Refer to the port function selection registers for the P1 function selection.

5.3 P2 port

5.3.1 P2 port description

P2 is a 4-bit I/O port. P2 control registers consist of P2 data register (P2), P2 direction register (P2IO), P2 debounce enable register (P2DB), P2 pull-up resistor selection register (P2PU) and P2 open-drain selection register (P2OD). Refer to the port function selection registers for the P2 function selection.

6 Interrupt controller

A94B114 supports up to 16 interrupt sources. The interrupts have separate enable register bits associated with them, allowing software control. In addition, they have four levels of priority assigned to themselves.

A non-maskable interrupt source is always enabled with a higher priority than any other interrupt sources, and is not controllable by software.

Interrupt controller of A94B114 has following features:

- Request receive from the 16 interrupt sources
- 2 levels of priority
- Multi Interrupt possibility
- 4 interrupt nesting levels
- A request of higher priority level is served first, when multiple requests of different priority levels are received simultaneously.
- Each interrupt source can be controlled by EA bit and each IEx bit
- Interrupt latency of 3 to 9 machine cycles in single interrupt system

A non-maskable interrupt is always enabled, while maskable interrupts are enabled through four pairs of interrupt enable registers (IE, IE1 and IE2). Each bit of IE, IE1, and IE2 registers individually enables/disables the corresponding interrupt source. Overall control is provided by bit 7 of IE (EA). When EA is set to ‘0’, all interrupts are disabled: when EA is set to ‘1’, interrupts are individually enabled or disabled through the other bits of the interrupt enable registers. The EA bit is always cleared to ‘0’ jumping to an interrupt service vector and set to ‘1’ executing the [RETI] instruction. The A94B114 supports a two-level priority scheme. Each maskable interrupt is individually assigned to one of four priority levels according to IP, IP1 and IP2.

Figure 11 shows the Interrupt Priority Level. Priority can be set by configuring a corresponding bit field of IP0, IP1 and IP2 registers. Each bit of IP0, IP1 and IP2 corresponds to each interrupt and defines one of 2 priority levels of each interrupt. High level interrupt always has higher priority than low level interrupt.

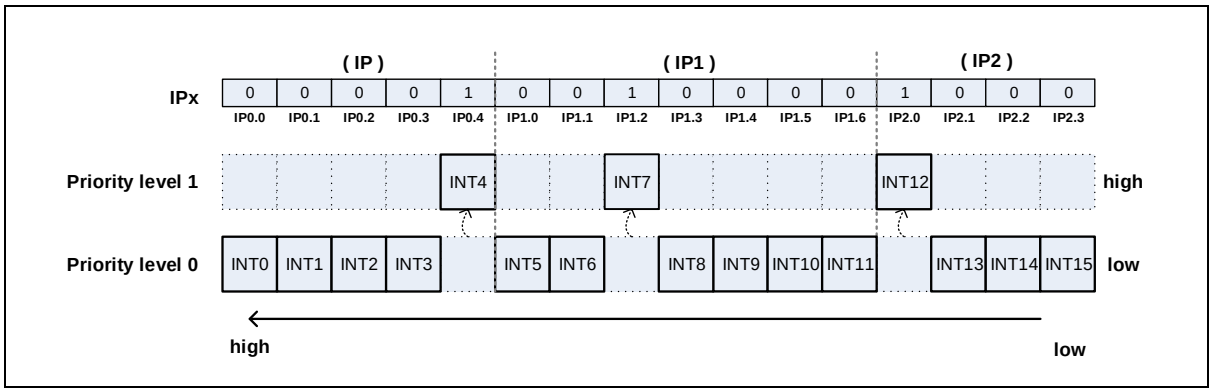
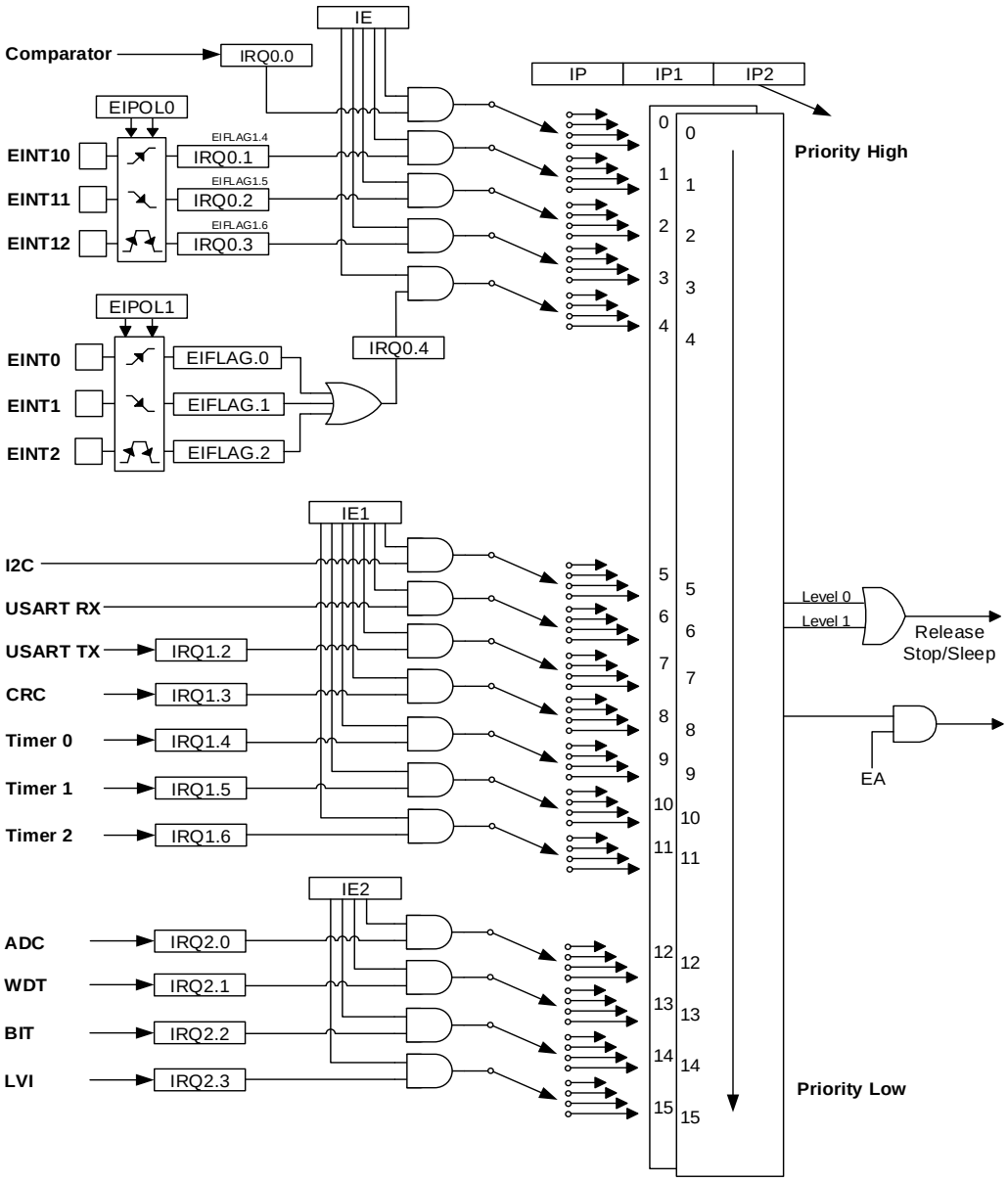


Figure 11. Interrupt Priority Level

This device support only 4 level interrupt nesting. Interrupt nesting level register (ILVL) has the current nesting level. If current nesting level is 4 and other interrupt having higher priority occur, it might cause a malfunction.

6.1 Block diagram



NOTES:

1. The release signal for stop/idle mode may be generated by all interrupt sources which are enabled without reference to the priority level.
2. An interrupt request is delayed while data are written to IE, IE1, IE2, IP, IP1, IP2 and PCON register.

Figure 12. Interrupt Controller Block Diagram

6.2 Interrupt vector table

Interrupt controller of A94B114 supports 16 interrupt sources as shown in table 8. When interrupt is served, long call instruction (LCALL) is executed and program counter jumps to the vector address. All interrupt requests have their own priority order.

Table 10. Interrupt Vector Address Table

Interrupt Source	Symbol	Interrupt enable bit	Priority	Mask	Vector address
Hardware Reset	RESETB	—	0	Non-Maskable	0000H
Comparator Interrupt	INT0	IE.0	1	Maskable	0003H
External Interrupt 10	INT1	IE.1	2	Maskable	000BH
External Interrupt 11	INT2	IE.2	3	Maskable	0013H
External Interrupt 12	INT3	IE.3	4	Maskable	001BH
External Interrupt 0/1/2	INT4	IE.4	5	Maskable	0023H
I2C Interrupt	INT5	IE1.0	6	Maskable	002BH
USART Rx Interrupt	INT6	IE1.1	7	Maskable	0033H
USART Tx Interrupt	INT7	IE1.2	8	Maskable	003BH
CRC Interrupt	INT8	IE1.3	9	Maskable	0043H
T0 Match Interrupt	INT9	IE1.4	10	Maskable	004BH
T1 Match Interrupt	INT10	IE1.5	11	Maskable	0053H
T2 Match Interrupt	INT11	IE1.6	12	Maskable	005BH
ADC Interrupt	INT12	IE2.0	13	Maskable	0063H
WDT Interrupt	INT13	IE2.1	14	Maskable	006BH
BIT Interrupt	INT14	IE2.2	15	Maskable	0073H
LVI Interrupt	INT15	IE2.3	16	Maskable	007BH

For maskable interrupt execution, EA bit must be set as ‘1’ and specific interrupt must be enabled by writing ‘1’ to associated bit in the IEx. If an interrupt request is received, the specific interrupt request flag is set to ‘1’. And it remains ‘1’ until CPU accepts interrupt. If the interrupt is served, the interrupt request flag will be cleared automatically.

7 Clock generator

As shown in figure 24, a clock generator produces basic clock pulses which provide a system clock for CPU and peripheral hardware. It contains main-frequency clock oscillator. The main clock can operate easily by attaching a crystal between the XIN and XOUT pin, respectively. The main clock can be also obtained from the external oscillator. In this case, it is necessary to put the external clock signal into the XIN pin and open the XOUT pin. The default system clock is 32MHz INT-RC Oscillator and the default division rate is two. In order to stabilize system internally, it is used 32MHz INT-RC oscillator on POR.

Oscillators in the clock generator are introduced in the followings:

- Calibrated high internal RC oscillator (HFO) : 32MHz
  - INT-RC OSC/2 (16MHz, default system clock)
  - INT-RC OSC/4 (8MHz)
  - INT-RC OSC/8 (4MHz)
  - INT-RC OSC/16 (1MHz)
- Main crystal oscillator (0.4~16MHz)
- Internal Ring oscillator (LFO) : 256KHz

7.1 Clock generator block diagram

In this section, a clock generator of A94B114 is described in a block diagram.

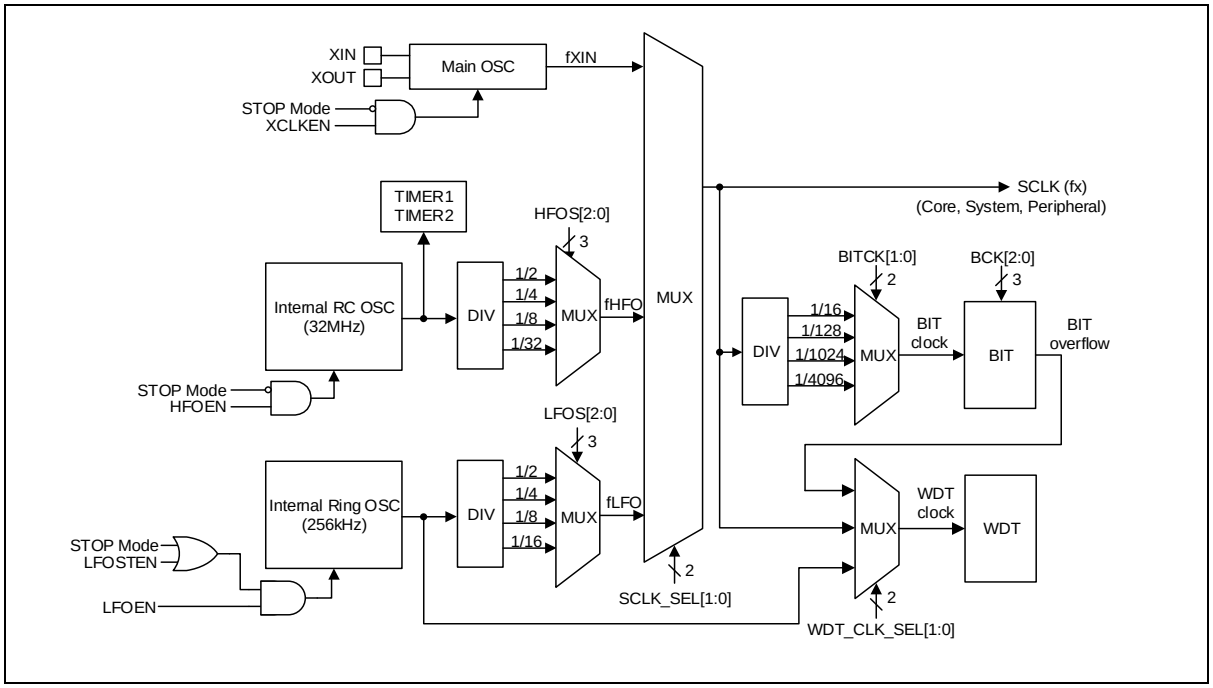


Figure 13. Clock Generator Block Diagram

8 Basic interval timer

A94B114 has a free running 8-bit Basic Interval Timer (BIT). BIT generates the time base for watchdog timer counting, and provides a basic interval timer interrupt.

BIT of A94B114 features the followings:

- As timer function, timer interrupt occurrence

NOTE: Since BIT Clock uses system clock, even if LFO (256KHz) is used as system clock, it cannot be used in STOP.

8.1 BIT block diagram

In this section, basic interval timer of A94B114 is described in a block diagram.

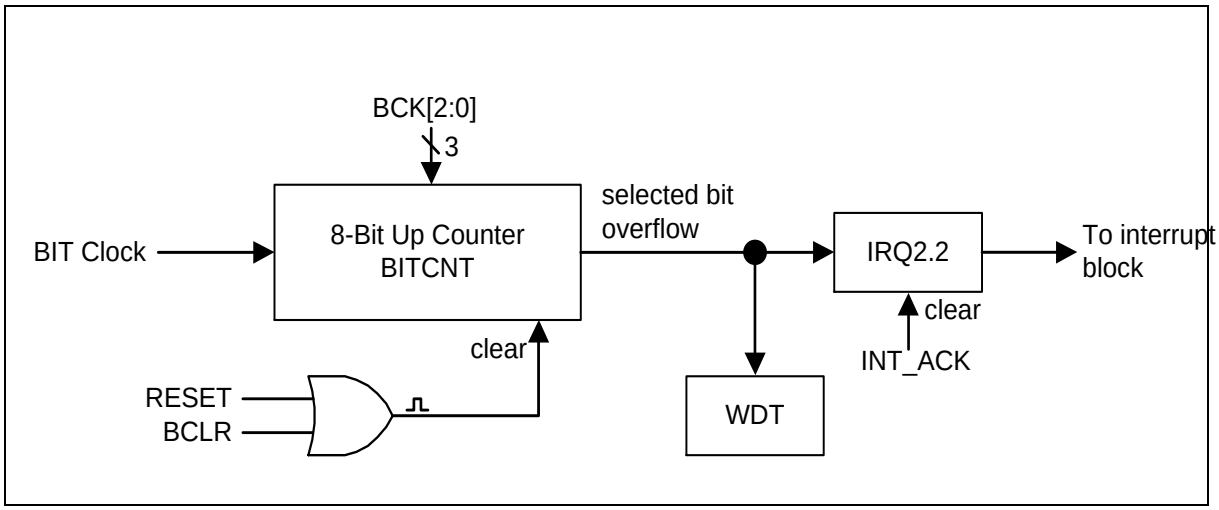


Figure 14. Basic Interval Timer Block Diagram

9 Watchdog timer

Watchdog timer (WDT) rapidly detects the CPU malfunction such as endless looping caused by noise or something like that, and resumes the CPU to the normal state. Watchdog timer signal for malfunction detection can be used as either a CPU reset or an interrupt request. When the watchdog timer is not being used for malfunction detection, it can be used as a timer to generate an interrupt at fixed intervals.

It is possible to use free running 8-bit timer mode or watch dog timer mode by setting WDT_RESET_EN bit. If WDT_CLR is set to '1', the WDT counter value is cleared and counts up. After 1 machine cycle, this bit is cleared to '0' automatically.

The WDT consists of an 8-bit binary counter and a watchdog timer data register. When value of the 8-bit binary counter is equal to the 8 bits of WDTR, an interrupt request flag is generated. This can be used as a watchdog timer interrupt or a reset signal of CPU in accordance with a bit WDT_RESET_EN.

Input clock source of the WDT selects one of the system clock, ring oscillator, and BIT overflow. An interval between watchdog timer interrupts is decided by WDT_CLK_DIV and WDTR set value. The equation can be described as the followings:

$$WDT\_TIME[s] = \frac{WDT\_CLK\_DIV \times (WDTR\ value + 1)}{fx\ or\ fLFO\ or\ fBIT}$$

NOTES:

3. LFO Clock is different between Normal / IDLE mode and Stop mode.
4. LFO Clock is 256KHz for Normal / IDLE mode and 168KHz for Stop Mode. (Typical)

9.1 WDT block diagram

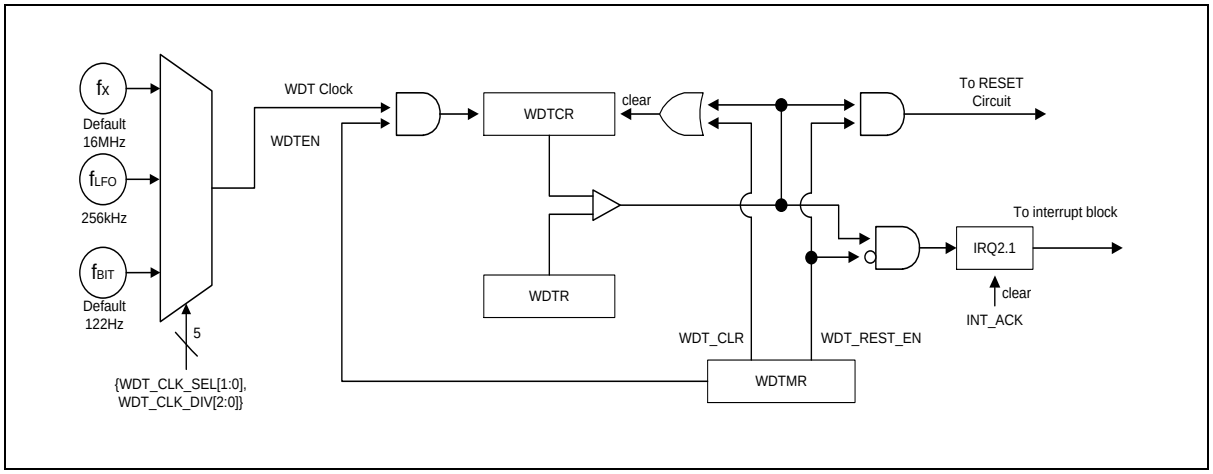


Figure 15. Watch Dog Timer Block Diagram

10 Timer 0/1/2

10.1 Timer 0

An 8-bit timer 0 consists of a multiplexer, a timer 0 counter register, a timer 0 data register, a timer 0 capture data register and a timer 0 control register (T0CNT, T0DR, T0CDR, T0CR).

Timer 0 operates in one of three modes introduced in the followings:

- 8-bit timer/counter mode
- 8-bit PWM output mode
- 8-bit capture mode

Timer/counter 0 can be clocked by an internal or an external clock source (EC0). The clock source is selected by clock selection logic which is controlled by clock selection bits T0CK[2:0].

- TIMER0 clock source: f_X/2, 4, 8, 32, 128, 512, 2048 and EC0

In capture mode, data is captured into input capture data register (T0CDR) by EINT10. In timer/counter mode, whenever counter value is equal to T0DR, T0O port toggles. In addition, timer 0 outputs PWM waveform through PWM0O port in the PWM mode.

Table 11. Timer 0 Operating Mode

T0EN	T0MS[1:0]	T0CK[2:0]	Timer 0
1	00	XXX	8-bit Timer/Counter Mode
1	01	XXX	8-bit PWM Mode
1	1X	XXX	8-bit Capture Mode

10.1.1 Timer 0 block diagram

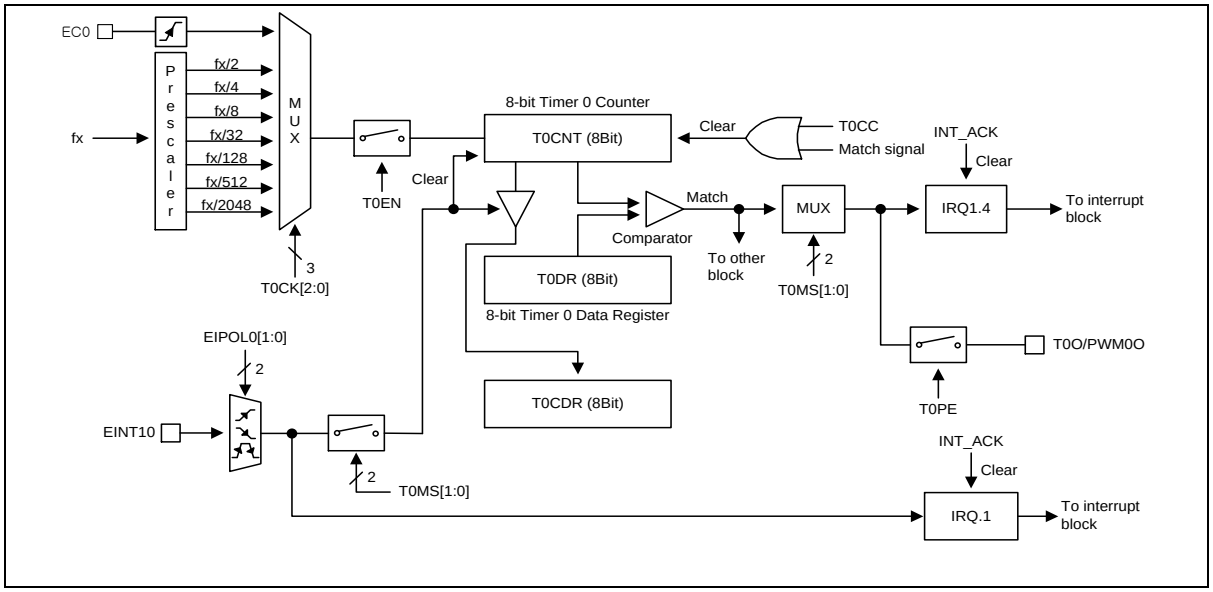


Figure 16. 8-bit Timer 0 Block Diagram

10.2 Timer 1

A 16-bit timer 1 consists of multiplexer, timer 1 A data register high/low, timer 1 B data register high/low, timer1 C data register high/low, timer1 D data register high/low and timer 1 control register high/low

(T1ADRH, T1ADRL, T1BDRH, T1BDRL, T1CRH, T1CRL, T1DRH, T1DRL).

Timer 1 operates in one of the following modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 1 uses an internal clock or an external clock (EC1) as an input clock source. The clock sources are introduced below, and one is selected by clock selection logic which is controlled by clock selection bits (T1CK[2:0]).

- TIMER 1 clock source: f_X/1, 2, 4, 8, 64, 512, 2048 and EC1

In capture mode, the data is captured into input capture data register (T1BDRH/T1BDRL) by EINT11. Timer 1 results in the comparison between counter and data register through T1O port in timer/counter mode. In addition, Timer 1 outputs PWM waveform through PWM1Oport in the PPG mode.

Table 12. TIMER 1 Operating Modes

T1EN	P1FSRL[4:3]	T1MS[1:0]	T1CK[2:0]	Timer 1
1	11	00	XXX	16 Bit Timer/Counter Mode
1	00	01	XXX	16 Bit Capture Mode
1	11	10	XXX	16 Bit PPG Mode(one-shot mode)
1	11	11	XXX	16 Bit PPG Mode(repeat mode)

10.2.1 16-bit timer 1 block diagram

In this section, a 16-bit timer 1 is described in a block diagram.

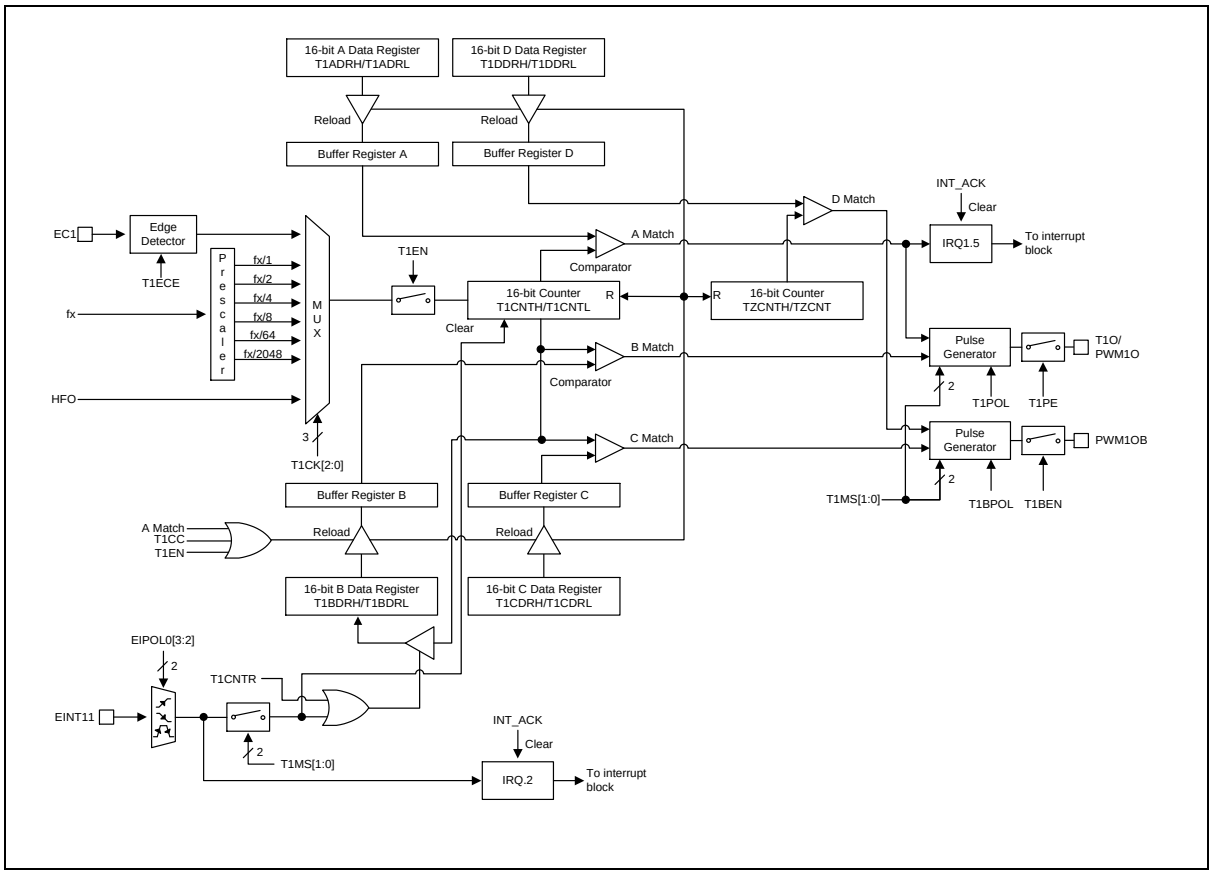


Figure 17. 16-bit Timer 1 Block Diagram

10.3 Timer 2

A 16-bit timer 2 consists of a multiplexer, timer 2 A data high/low register, timer 2 B data high/low register and timer 2 control high/low register (T2ADRH, T2ADRL, T2BDRH, T2BDRL, T2CRH, and T2CRL).

Timer 2 operates in one of the following modes:

- 16-bit timer/counter mode
- 16-bit capture mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

The timer/counter 2 can be clocked by an internal or an external clock source (EC2). The clock source is selected by a clock selection logic, controlled by clock selection bits (T2CK[2:0]).

- TIMER 2 clock source: fX/1, 2, 4, 8, 64, 2048, HFO and EC2

In capture mode, data is captured into input capture data registers (T2BDRH/T2BDRL) by EINT12. In timer/counter mode, whenever counter value is equal to T2ADRH/L, T2O port toggles. In addition, the timer 2 outputs PWM waveform to PWM2O port in the PPG mode.

Table 13. TIMER 2 Operating Modes

T2EN	P1FSRL[6:5]	T2MS[1:0]	T2CK[2:0]	Timer 2
1	01	00	XXX	16 Bit Timer/Counter Mode

1	00	01	XXX	16 Bit Capture Mode
1	01	10	XXX	16 Bit PPG Mode(one-shot mode)
1	01	11	XXX	16 Bit PPG Mode(repeat mode)

10.3.1 16-bit timer 2 block diagram

In this section, a 16-bit timer 2 is described in a block diagram.

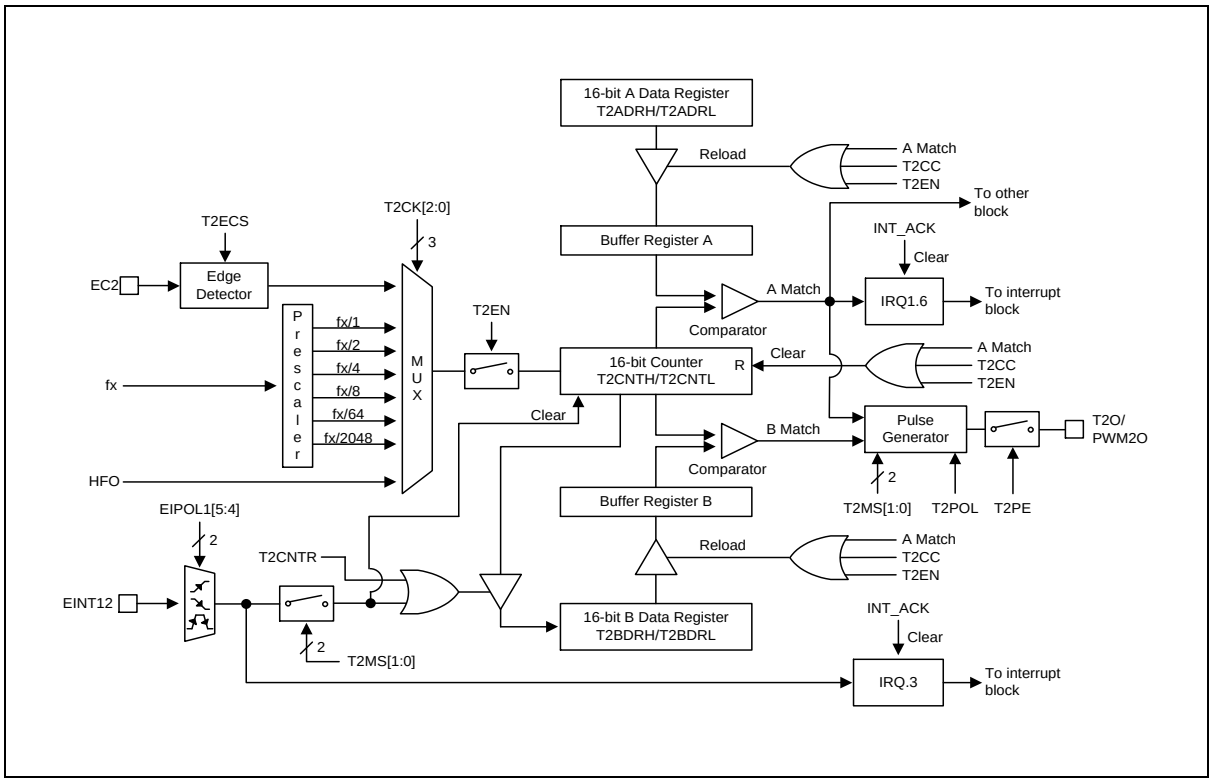


Figure 18. 16-bit Timer 2 Block Diagram

11 12-bit ADC

Analog-to-digital converter (ADC) of A94B114 allows conversion of an analog input signal to corresponding 12-bit digital value. This A/D module has tenth analog inputs. Output of the multiplexer becomes input into the converter which generates the result through successive approximation.

The A/D module has four registers which are the A/D converter mode register (ADCM), A/D converter mode register 1 (ADCM1), A/D converter result register (ADCHR), and A/D converter result low register (ADCLR). ADSEL[3:0] bits are used to select channels to be converted.

To executing A/D conversion, ADST bit is set to ‘1’. Registers ADCDRH and ADCDRL contain the result of A/D conversion. When the conversion is completed, the result is loaded into ADCHR and ADCLR, A/D conversion status bit AFLAG is set to ‘1’, and A/D interrupt is set. During the A/D conversion, AFLAG bit is read as ‘0’.

If using STBY (power down) bit, the ADC is disabled. When restarting after resetting the STBY bit (ADC power enable), during some cycles, ADC conversion value may have an inaccurate value.

Also internal timer, external generating event, comparator and the timer can start ADC. At this time, the interrupt enable of trigger sources is not required. If only the interrupt generation condition of each trigger source is satisfied, ADC starts.

ADC Conversion Time = ADCLK * 60 cycles

Please remember that the ADC requires at least 20us for conversion time, so the conversion time must be set bigger than 20us.

11.1 Block diagram

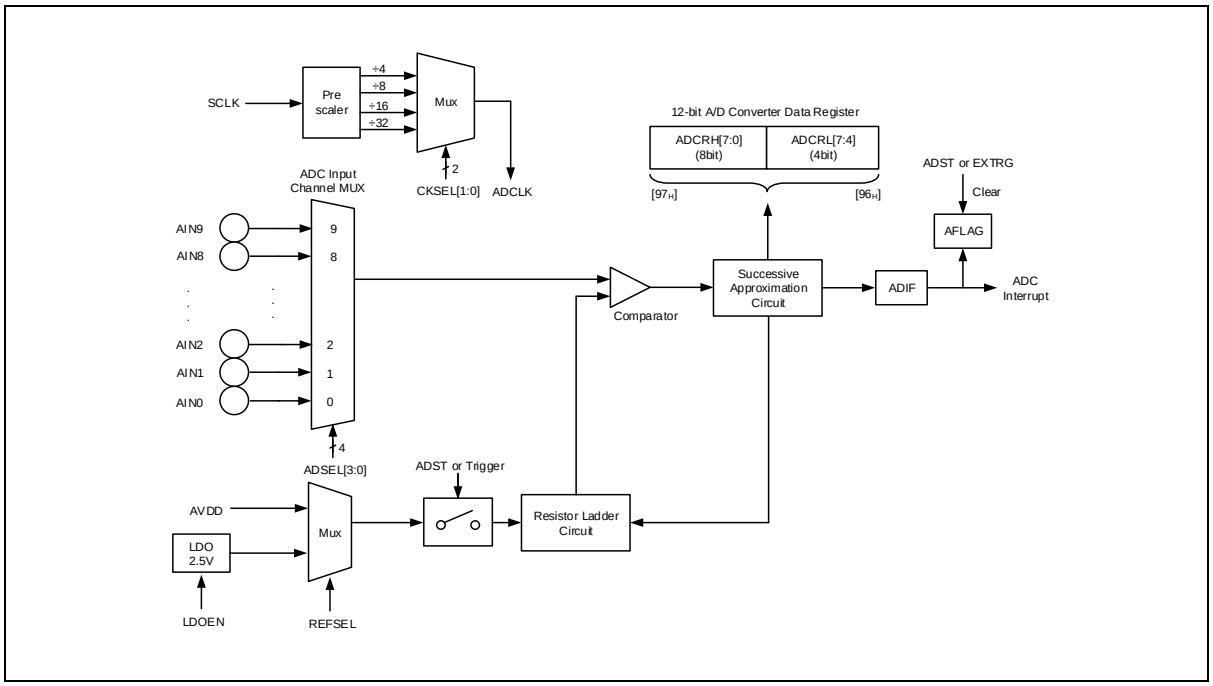


Figure 19. 12-bit ADC Block Diagram

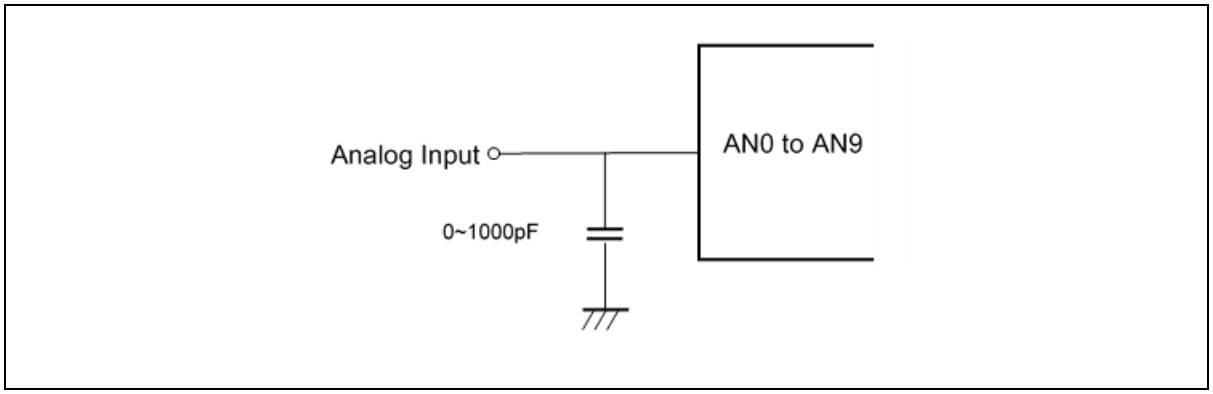


Figure 20. A/D Analog Input Pin with a Capacitor

12 Comparator

The A9B114 contains analog comparators which can be easily used to compare the external input voltage with internally reference or externally reference voltage. ADC and Comparator have the same input. When the comparator input voltage is larger than the reference voltage comparator output status is '1' and interrupt flag is generated. The Comparator interrupt flag is assigned to one interrupt vector. Comparator output debounce clock and length can be set.

The internal reference of the comparator is the resistor distribution method. When AVDD is selected, the reference value is 5V. At this time, 1.6V and 2.2V can be selected as the internal reference voltage of the comparator. If AVDD is below 5V, the internal reference value is reduced at a constant rate. However, when Low Drop Out (LDO) is selected, 1.6V and 2.2V are normally selected as 2.5V reference.

12.1 Comparator block diagram

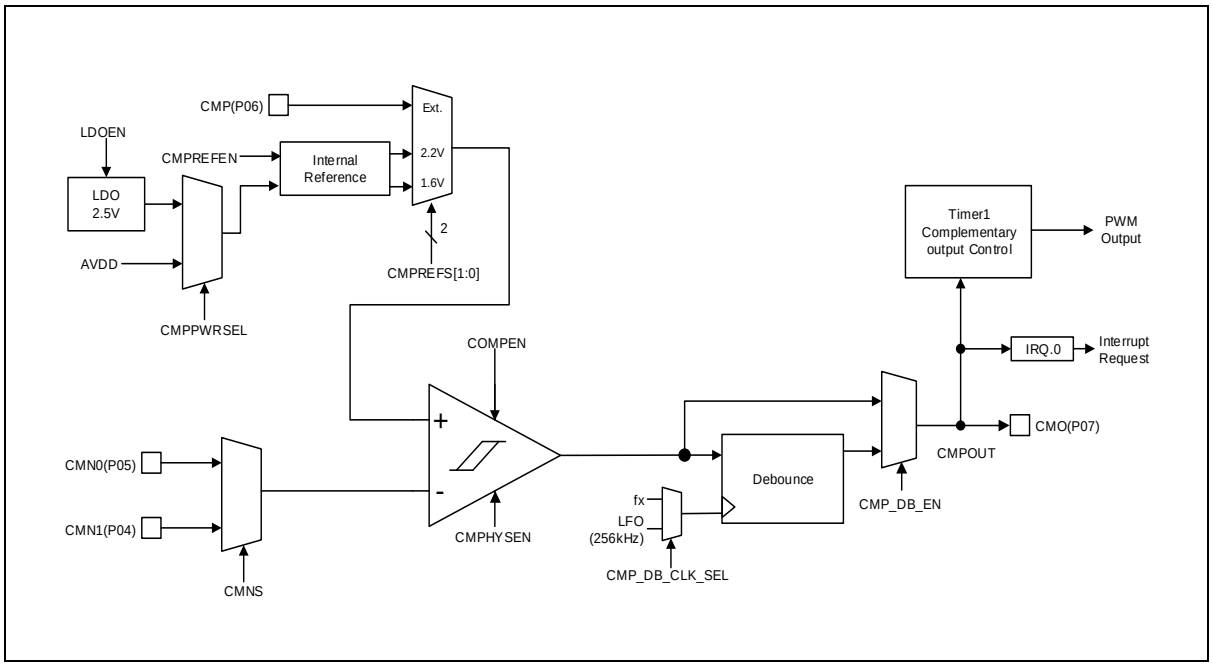


Figure 21. Comparator Block Diagram

13 USART

Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication device. USART of A94B114 features the followings:

- Full Duplex Operation (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation
- Master or Slave Clocked Synchronous and SPI Operation
- Supports all four SPI Modes of Operation (Mode 0, 1, 2, 3)
- LSB First or MSB First Data Transfer @SPI mode
- High Resolution Baud Rate Generator
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits
- Odd or Even Parity Generation and Parity Check Supported by Hardware
- Data OverRun Detection
- Framing Error Detection
- Digital Low Pass Filter
- Three Separate Interrupts on TX Complete, TX Data Register Empty and RX Complete
- Double Speed Asynchronous Communication Mode

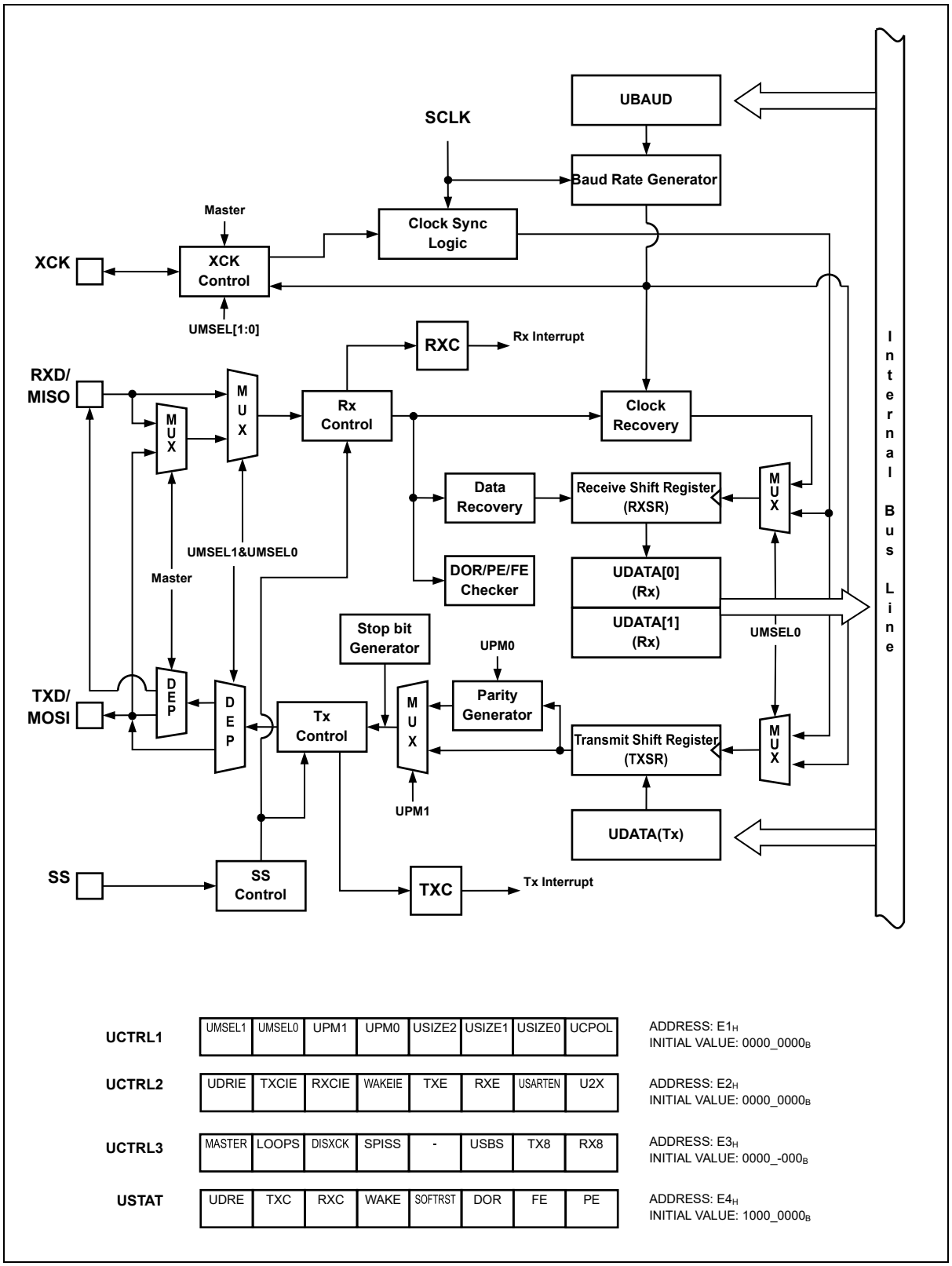
USART has three main parts such as a Clock Generator, Transmitter and Receiver.

Clock Generation logic consists of a synchronization logic for external clock input used by synchronous or SPI slave operation, and a baud rate generator for asynchronous or master (synchronous or SPI) operation.

Transmitter consists of a single write buffer, a serial shift register, parity generator and control logic for handling different serial frame formats. Write buffer allows a continuous transfer of data without any delay between frames.

Receiver is the most complex part of the USART2 module due to its clock and data recovery units. Recovery unit is used for asynchronous data reception. In addition to the recovery unit, the Receiver includes a parity checker, a shift register, a two level receive FIFO (UDATA) and control logic. The Receiver supports the same frame formats as the Transmitter and can detect Frame Error, Data OverRun and Parity Errors.

13.1 Block diagram



UCTRL1	UMSEL1	UMSEL0	UPM1	UPM0	USIZE2	USIZE1	USIZE0	UCPOL	ADDRESS: $E1_H$ INITIAL VALUE: 0000_0000_B
UCTRL2	UDRIE	TXCIE	RXCIE	WAKEIE	TXE	RXE	USARTEN	U2X	ADDRESS: $E2_H$ INITIAL VALUE: 0000_0000_B
UCTRL3	MASTER	LOOPS	DISXCK	SPISS	-	USBS	TX8	RX8	ADDRESS: $E3_H$ INITIAL VALUE: 0000_-000_B
USTAT	UDRE	TXC	RXC	WAKE	SOFTRST	DOR	FE	PE	ADDRESS: $E4_H$ INITIAL VALUE: 1000_0000_B

Figure 22. USART Block Diagram

14 I2C

The I2C is one of industrial standard serial communication protocols, and which uses 2 bus lines Serial Data Line (SDA) and Serial Clock Line (SCL) to exchange data. Because both SDA and SCL lines are open-drain output, each line needs pull-up resistor. The features are as shown below.

- Compatible with I2C bus standard
- Multi-master operation
- Up to 400KHz data transfer speed
- 7-bit address
- Support two slave addresses
- Both master and slave operation
- Bus busy detection

14.1 Block diagram

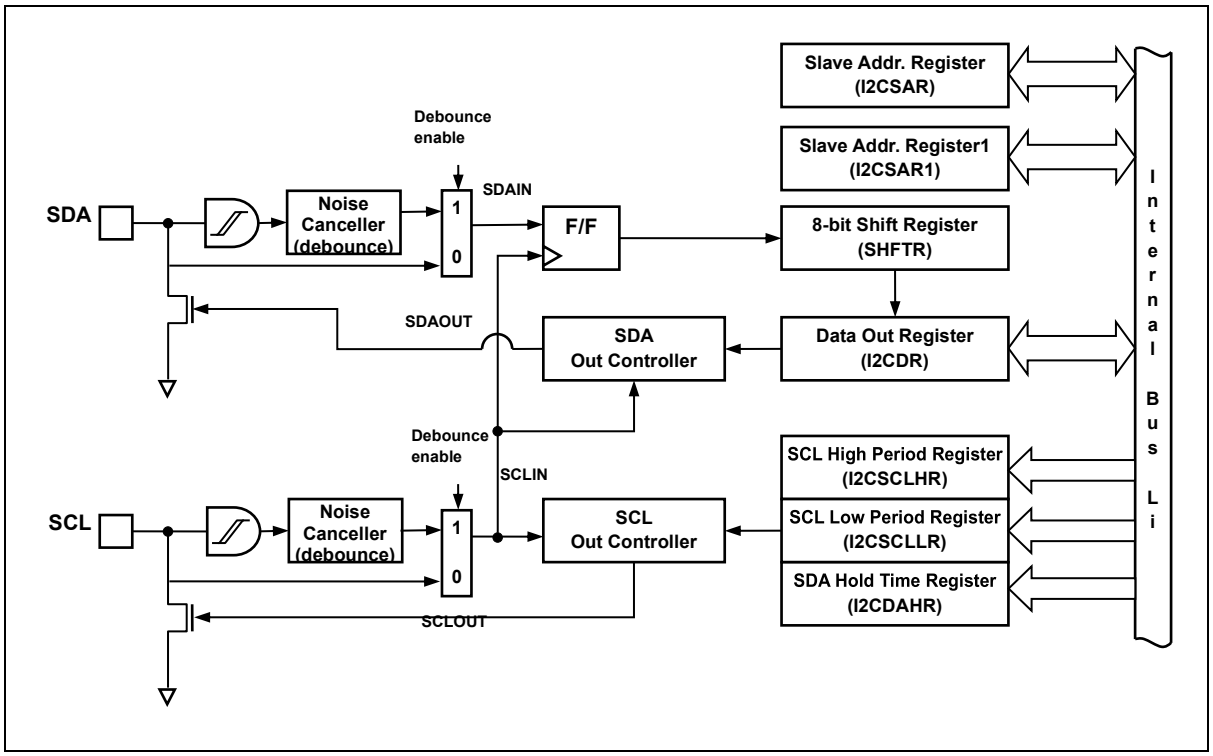


Figure 23. I2C Block Diagram

15 CRC

Using the CRC, it can be monitor the memory of the specified area. This is a one-time operation, and reset is required for continuous operation. In CRC MNT mode, when the CRC read is finished, CRC_FLAG occurs. In CRC validate mode, if the CRC validate fail after the CRC reading is finished, CRC_FLAG occurs. CRC_FAIL indicates the status of validate results when the CRC read is finished. If the CRC_FLAG is generated and the interrupt is enabled, interrupt service routine is served. CRC-FLAG is not cleared by hardware. CRC-TYPE 0~3 are not supported. Validate is done by comparing the CRC_MNT register and the CRC register value. CRC are not automatically initialized, you need to calculate a new CRC after CRC_H, CRC_L Clear. Block diagram

Table 14. CRC Modes

CRC TYPE	CRC mode	Input	Condition of CRC_FLAG	Condition of CRC reset
CRC_TYPE = 4	MNT	FLASH	After CRC reading	Validate fail
CRC_TYPE = 5	MNT	IXRAM	After CRC reading	Validate fail
CRC_TYPE = 6	Validate	FLASH	After CRC reading & Validate fail	Validate fail
CRC_TYPE = 7	Validate	IXRAM	After CRC reading & Validate fail	Validate fail

15.1 Block diagram

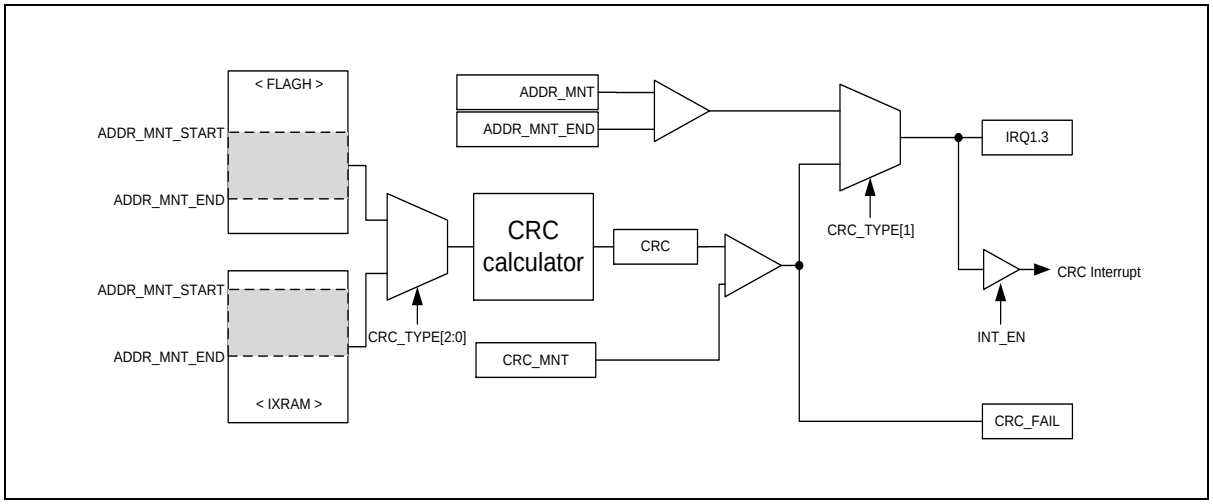


Figure 24. CRC Block Diagram

16 Power down operation

The A94B114 has two power-down modes to minimize the power consumption of the device. In power down mode, power consumption is reduced considerably. The device provides two kinds of power saving functions, IDLE and STOP mode. In two modes, program is stopped.

16.1 Peripheral operation in IDLE/ STOP mode

Table 28 shows operation status of each peripheral in IDLE mode and STOP mode.

Table 15. Peripheral Operation Status during Power Down Mode

Peripheral	IDLE mode	STOP mode
CPU	ALL CPU operations are disabled.	ALL CPU operations are disabled.
RAM	Retains.	Retains.
Basic Interval Timer	Operates continuously.	Stops.
Watch Dog Timer	Operates continuously.	Stops (Can be operated with Ring OSC)
Timer0~2	Operates continuously.	Halts (only when the event counter mode is enabled, timer operates normally).
ADC	Operates continuously.	Stops.
Comparator	Operates continuously.	Stops (can be operated with WDTRC OSC).
USART	Operates continuously.	Stops.
I2C	Operates continuously.	Stops.
Internal RC OSC (16MHz)	Oscillates.	Stops when the system clock (fx) is fIRC
Internal Ring OSC (256KHz)	Can be operated with setting value.	Can be operated programmable.
Main OSC (0.4~12MHz)	Oscillates.	Stops when fx = fXIN.
I/O Port	Retains.	Retains.
Control Register	Retains.	Retains.
Address Data Bus	Retains.	Retains.
Release Method	By RESET, All Interrupts(Except LVI)	By RESET, Timer Interrupt(EC), External Interrupt, I2C Interrupt, Comparator Interrupt, USART by RX, WDT

17 Reset

Table 30 shows hardware setting values of main peripherals.

Table 16. Hardware Setting Values in Reset State

On Chip Hardware	Initial Value
Program Counter (PC)	0000h
Accumulator	00h
Stack Pointer (SP)	07h
Peripheral Clock	On
Control Register	Refer to the Peripheral Registers

A94B114 has five types of reset sources as shown in the followings:

- External RESETB
- Power ON RESET (POR)
- WDT Overflow Reset (In the case of WDTEN = `1`)
- Low Voltage Reset (In the case of LVREN = `0 `)

17.1 Reset block diagram

In this section, reset unit is described in a block diagram.

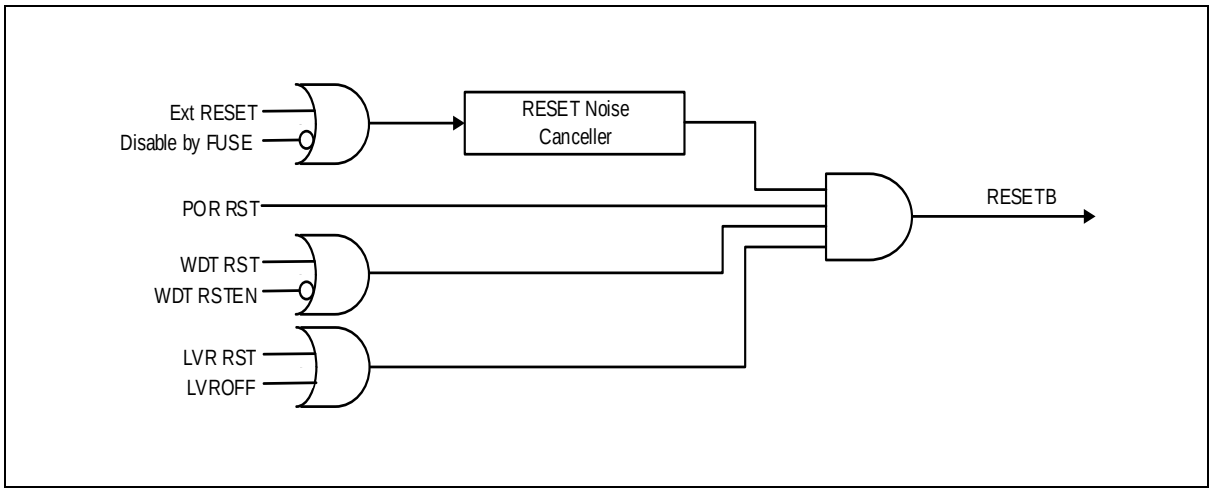


Figure 25. Reset Block Diagram

18 Memory programming

A94B114 has flash memory to which a program can be written, erased, and overwritten while mounted on a board. This device support the self program/ erase mode in user soft mode in SRAM-jump. Serial ISP mode is supported.

Flash of A94B114 features the followings:

- Flash Size : 8Kbytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 10,000 program/erase cycles at typical voltage and temperature for flash memory
- Security feature

18.1 Memory map

18.1.1 Flash memory map

Program memory uses 8K bytes of flash memory. It is read by byte and written by page. One page is 32-bytes

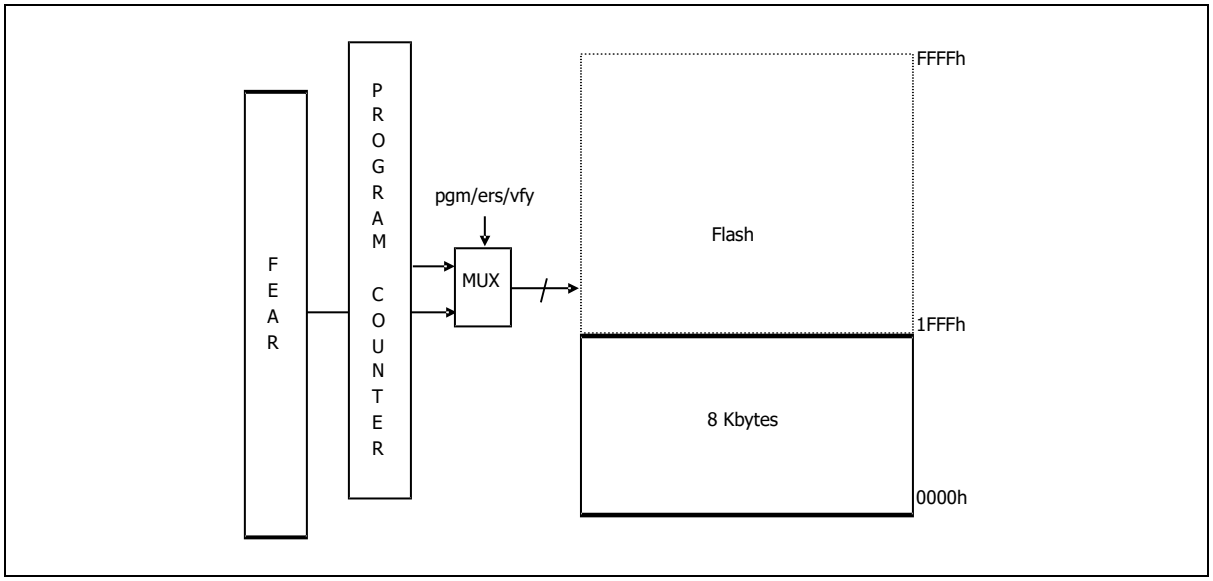


Figure 26. Flash Memory Map

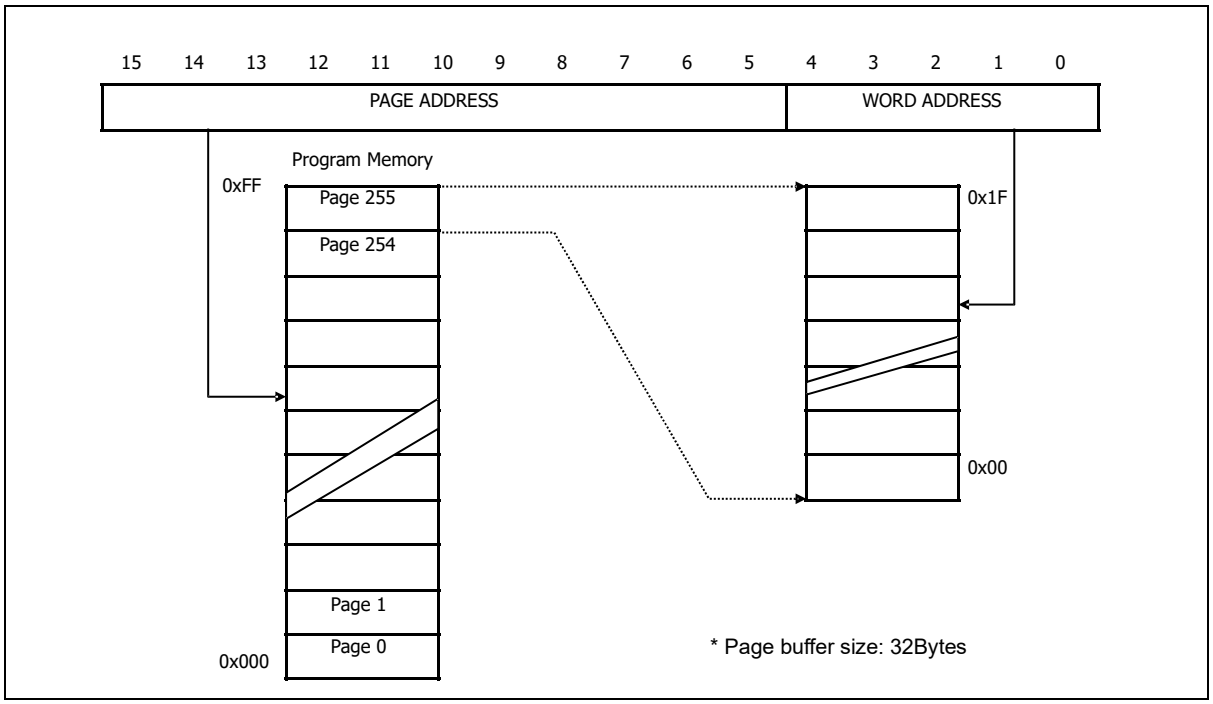


Figure 27. Address Configuration of Flash Memory

19 Electrical characteristics

19.1 Absolute maximum ratings

Table 17. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply Voltage	VDD	-0.3~+6.5	V	–
Normal Voltage Pin	V_I	0.3~VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	0.3~VDD+0.3	V	
	I_{OH}	-15	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	$\sum I_{OH}$	-80	mA	Maximum current ($\sum I_{OH}$)
	I_{OL}	30	mA	Maximum current (I_{OL} per I/O pin)
	$\sum I_{OL}$	160	mA	Maximum current ($\sum I_{OL}$)
Total Power Dissipation	P_T	400	mW	–
Storage Temperature	T_{STG}	-65~+150	°C	–

NOTE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

19.2 Recommended operating conditions

Table 18. Recommended Operating Conditions

(T_A=-40°C ~ 85°C)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Operating Voltage	VDD	f_X= 1, 4, 8, 16MHz	HFO	2.0	–	5.5	V
		f_X= 256KHz	LFO				
		f_X= 0.4 ~ 16MHz	Crystal	2.4	–	5.5	
Operating Temperature	T_{OPR}	VDD=2.0~5.5V (Internal RC) VDD=2.7~5.5V (Crystal)		-40	–	85	°C

19.3 Low Drop-out Characteristics

Table 19. Low Drop-out Characteristics

(T_A=-40°C ~ 85°C, AVDD=2.7~5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
LDO Output Voltage	V_{LDO}	T_A=-40~85℃	2.450	2.5	2.550	V
		T_A=25℃	2.470	2.5	2.530	
Quiescent Current	I_Q	AVDD=5.5V	–	300	400	uA
Load Current	I_L	Dropout Voltage=0.2V	–	–	1	mA

19.4 A/D converter characteristics

Table 20. A/D Converter Characteristics

(T_A=-40°C ~ +85°C, VDD=2.5V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Resolution	–	–	–	12	–	bit
Integral Non-Linearity	INL	Analog Reference NOTE Voltage = 2.7V ~ 5.5V (VDD ref) ADC Clock= 2MHz (VDD ref)	–	–	±5	LSB
Differential Non-Linearity	DNL		–	–	±3	
Offset Error of Top	EOT		–	±4	±8	
Offset Error of Bottom	EOB		–	±2	±4	
LDO Ref. Integral Non-Linearity	LDO_INL	Voltage = 1.25V (LDO ref) ADC Clock= 500KHz (LDO ref)	–	±15	–	LSB
		Voltage = 2.50V (LDO ref) ADC Clock= 500KHz (LDO ref)	–	±20	–	
LDO Ref. Differential Non-Linearity	LDO_DNL	Voltage = 2.5V ~ 5.5V (LDO ref) ADC Clock= 500KHz (LDO ref)	–	–	±3	us
LDO Ref. Offset Error of Top	LDO_EOT		–	±4	±8	
LDO Ref. Offset Error of Bottom	LDO_EOB		–	±2	±3	
Conversion Time	t_{CON}	AVREF = 3.0V ~ 5.5V	20	–	–	us
		AVREF = 2.7V ~ 5.5V	30	–	–	
		AVREF = 2.4V ~ 5.5V	60	–	–	
Analog Input Voltage	V_{AN}	–	VSS	–	VDD	V
Analog Reference Voltage	VDDREF	***NOTE**	2.2	–	VDD	V
	LDOREF	–	–	2.5	–	
Analog Input Leakage Current	I_{AN}	VDDREF=5.12V	–	–	2	mA

Table 40. A/D Converter Characteristics (continued)

(T_A=-40°C ~ +85°C, VDD=2.5V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
ADC Operating Current	I_{ADC}	Enable	VDD=5.12V	–	1	2	mA
		Disable		–	–	0.1	uA

NOTES:

5. If the Analog reference voltage is lower than 2.7V and the ADC Clock is faster than 2MHz, ADC resolution will be degraded. (Analog Reference = VDDREF) If the Analog reference voltage is lower than 2.5V and the ADC Clock is faster than 500KHz, ADC resolution will be degraded. (Analog Reference = LDOREF)
6. When LDO Reference is used, ADC gain can be affected by LDO output variation.

19.5 Low voltage reset and low voltage indicator characteristics

Table 21. LVR and LVI Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Detection Level	V_{LVR} V_{LVI}	The LVR can select 1.75V but LVI can select other levels except 1.75V		-	1.75	1.9	V
				2.2	2.4	2.6	
				2.7	2.9	3.1	
				3.6	3.9	4.2	
				3.9	4.2	4.5	
Hysteresis	△V	–		–	50	–	mV
LVR and LVI Current	I_{LVR}	LVR 1.75V	VDD= 5V	–	1	–	uA
		LVI except 1.75V		–	–	50	

19.6 Power on reset characteristics

Table 22. Power-on Reset Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	V_{POR}	–	–	1.25	–	V
VDD Voltage Rising Time	t_R	–	0.05	–	5.0	V/ms
POR Current	I_{POR}	–	–	0.1	–	uA

19.7 High internal RC oscillator characteristics

Table 23. High Internal RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Frequency	f_{IRC}	V_{DD} = 2.0 – 5.5V		–	32	–	MHz
Tolerance	–	T_A = 25°C	With 0.1uF Bypass capacitor	–	±1.5	–	%
		T_A = 0°C to +50°C		-2.5	–	2.5	
		T_A = -40°C to +85°C		-3.0	–	3.0	
Stabilization Time	T_{HFS}	–		–	1	–	ms
Operating Current	I_{HFO}	Enable		–	0.4	–	mA

19.8 Low internal RC oscillator characteristics

Table 24. Ring-Oscillator Characteristics

(T_A=-40°C ~ +85°C, AVDD=2.2V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	$IDD_{(RMS)}$	–	–	100	200	uA
	$ISTOP_{(RMS)}$	–	–	12	100	nA
Comparator Input Offset Voltage	V_{OS}	@Trim Comparator	–	±10	–	mV
		@Trim Comparator + LDO Internal Ref		±25	–	
		@Trim Comparator + AVDD Internal Ref	–	±25	–	
		No Trim, Comparator Only	–	±40	–	
Propagation Delay	$t_{PD}(t_{PHL})$		–	0.08	0.15	us
Hysteresis	t_{HYS}	HYS_EN_I='High' (Except input offset)	–	±16	±20	mV
Internal VREF Stabilization Time	t_{WKUP}		4	–	–	us

19.9 DC characteristics

Table 25. DC Characteristics

(T_A= -40°C ~ +85°C, VDD= 2.0V ~ 5.5V, VSS= 0V, f_{XIN}= 16MHz)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input High Voltage	V_{IH1}	P0, P1, P2	0.7VDD	–	VDD	V
Input Low Voltage	V_{IL1}	P0, P1, P2	–	–	0.3VDD	V
Output High Voltage	V_{OH1}	VDD=3.3V, I_{OH}=-4mA, All output ports	VDD-1.0	–	–	V
	V_{OH2}	VDD=5V, I_{OH}=-8mA, All output ports	VDD-2.0	–	–	V
Output Low Voltage	V_{OL1}	VDD=3.3V, I_{OL}= 5mA, All output ports	–	–	1.0	V
	V_{OL2}	VDD=5V, I_{OL}= 10mA, All output ports	–	–	1.0	V
Input High Leakage Current	I_{IH}	All input ports	–	–	1	uA
Input Low Leakage Current	I_{IL}	All input ports	-1	–	–	uA
Pull-Up Resistor	R_{PU1}	VI=0V, T_A= 25°C All Input ports	25	50	100	KΩ
Supply Current	I_{DD1} (RUN)	Run Mode, f_X=16MHz (HFO/2)	–	3	6	mA
	I_{DD2} (IDLE)	IDLE Mode, f_X=16MHz	–	0.8	1.6	mA
	I_{DD3} (RUN_LFO)	Run Mode, f_X=128KHz (LFO/2)	–	1	2.5	mA
	I_{DD4} (STOP1)	STOP1 Mode, LFO Enable	–	5	20	uA
	I_{DD5} (STOP2)	STOP2 Mode, LFO Disable, LVR Disable	–	2.5	5	uA

19.10 AC characteristics

Table 26. AC Characteristics

(T_A= -40°C ~ +85°C, VDD= 2.0V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESETB input low width	t_{RSL}	Input, VDD= 5V	–	500	–	us
Interrupt input high, low width	t_{INTH}, t_{INTL}	All interrupt, VDD= 5V	125	–	–	ns
External Counter Input High, Low Pulse Width	t_{ECWH}, t_{ECWL}	Ecn, V_{DD} = 5V	125	–	–	
External Counter Transition Time	t_{REC}, t_{FEC}	Ecn, V_{DD} = 5V	–	–	20	

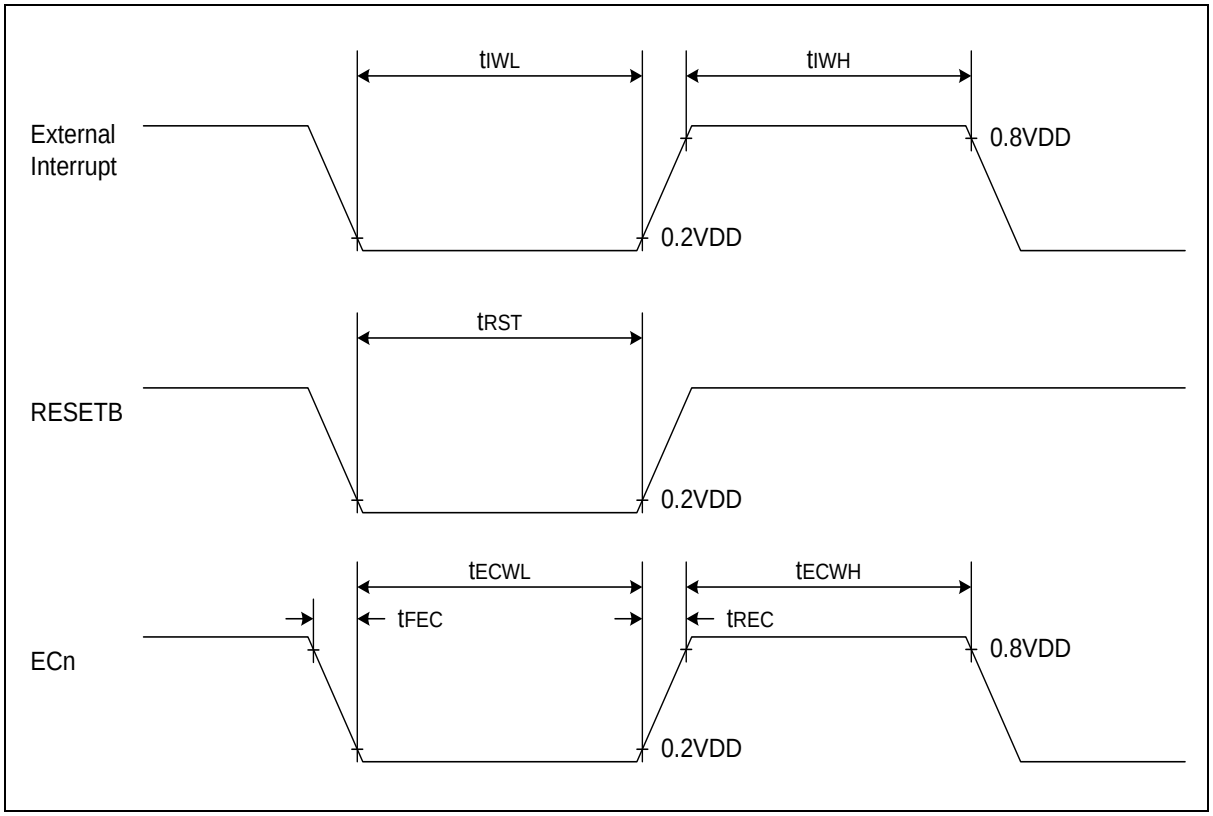


Figure 28. AC Timing

19.11 USART characteristics

Table 27. USART Characteristics

(T_A= -40°C ~ +85°C, VDD=2.0V ~ 5.5V, f_{XIN}=16MHz)

Parameter	Symbol	MIN	TYP	MAX	Unit
Serial port clock cycle time	t_{SCK}	1800	t_{CPU} x 16	2200	ns
Output data setup to clock rising edge	t_{S1}	8100	t_{CPU} x 13	–	ns
Clock rising edge to input data valid	t_{S2}	–	–	590	ns
Output data hold after clock rising edge	t_{H1}	t_{CPU}- 50	t_{CPU}	–	ns
Input data hold after clock rising edge	t_{H2}	0	–	–	ns
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	720	t_{CPU} x 8	1280	ns

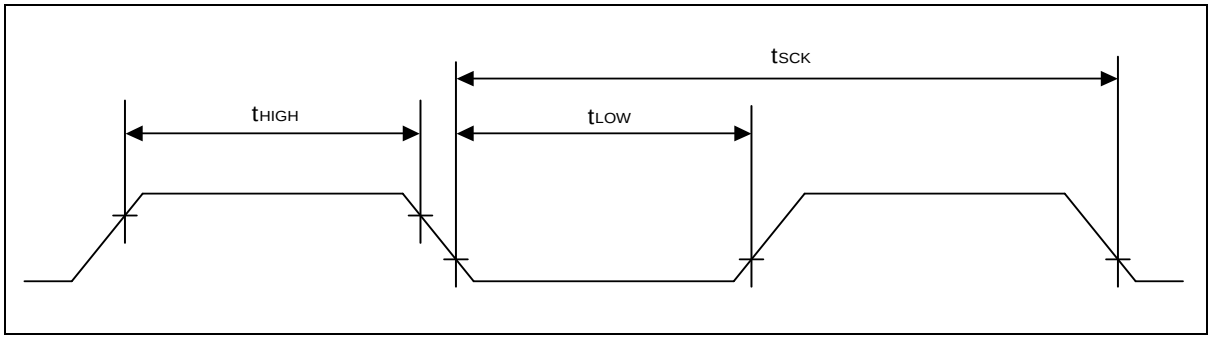


Figure 29. Waveform for USART Timing Characteristics

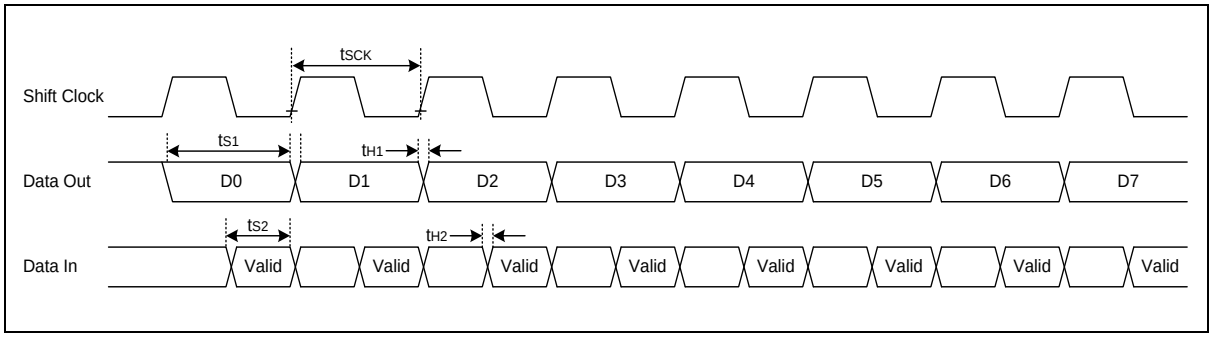


Figure 30. Timing Waveform for the USART Module

19.12 SPI characteristics

Table 28. SPI Characteristics

(T_A=-40°C– +85°C, VDD=2.0V – 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Clock Pulse Period	tSCK	Internal SCK source	200	–	–	ns
Input Clock Pulse Period		External SCK source	200	–	–	
Output Clock High, Low Pulse Width	tSCKH, tSCKL	Internal SCK source	70	–	–	
Input Clock High, Low Pulse Width		External SCK source	70	–	–	
First Output Clock Delay Time	tFOD	Internal/External SCK source	100	–	–	
Output Clock Delay Time	tDS	–	–	–	50	
Input Setup Time	tDIS	–	100	–	–	
Input Hold Time	tDIH	–	150	–	–	

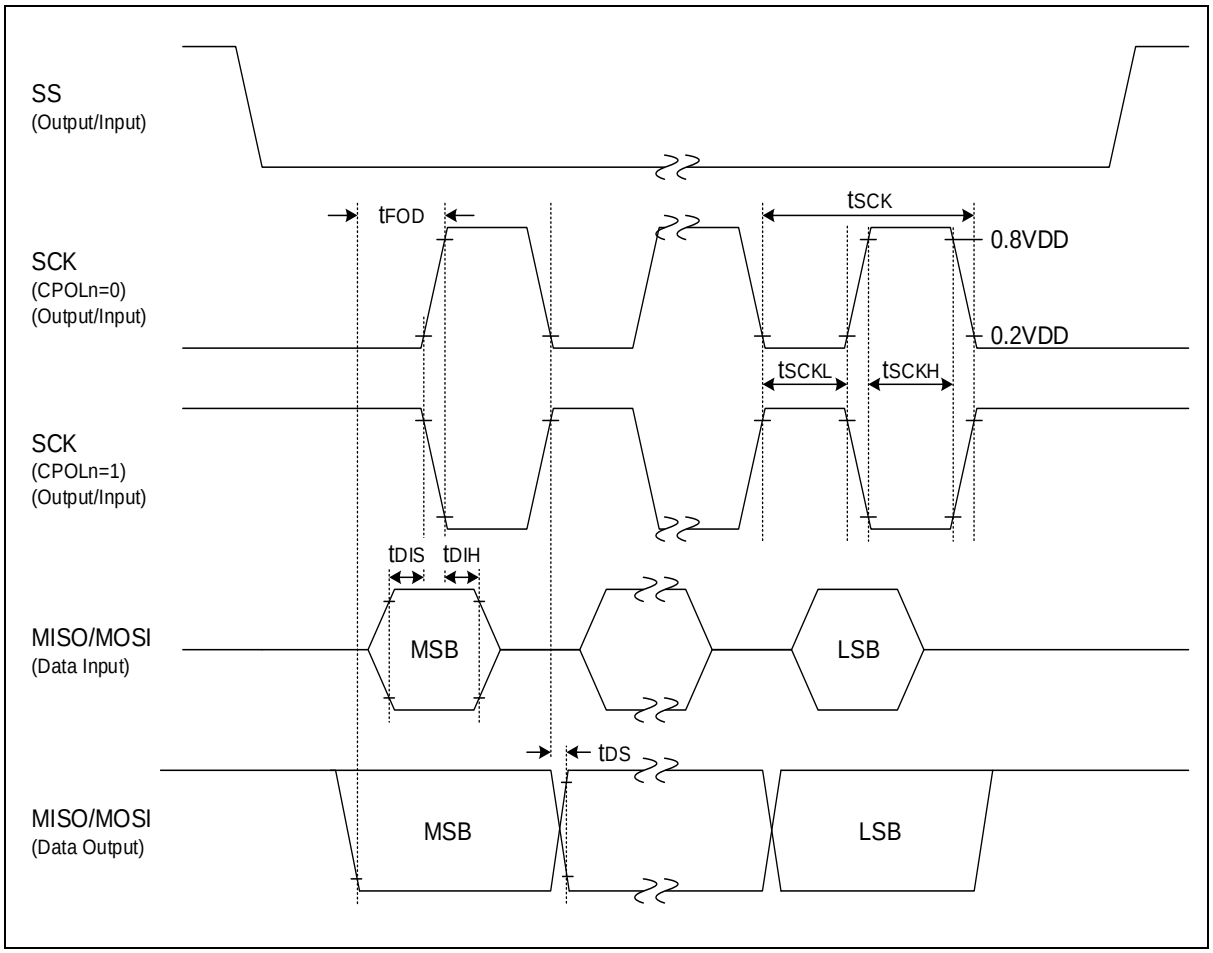


Figure 31. SPI Timing

19.13 UART characteristics

Table 29. UART Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V, f_{XIN}=16MHz)

Parameter	Symbol	MIN	TYP	MAX	Unit
Serial port clock cycle time	t_{SCK}	1800	t_{CPU} x 16	2200	ns
Output data setup to clock rising edge	t_{S1}	810	t_{CPU} x 13	–	ns
Clock rising edge to input data valid	t_{S2}	–	–	590	ns
Output data hold after clock rising edge	t_{H1}	t_{CPU}- 50	t_{CPU}	–	ns
Input data hold after clock rising edge	t_{H2}	0	–	–	ns
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	720	t_{CPU} x 8	1280	ns

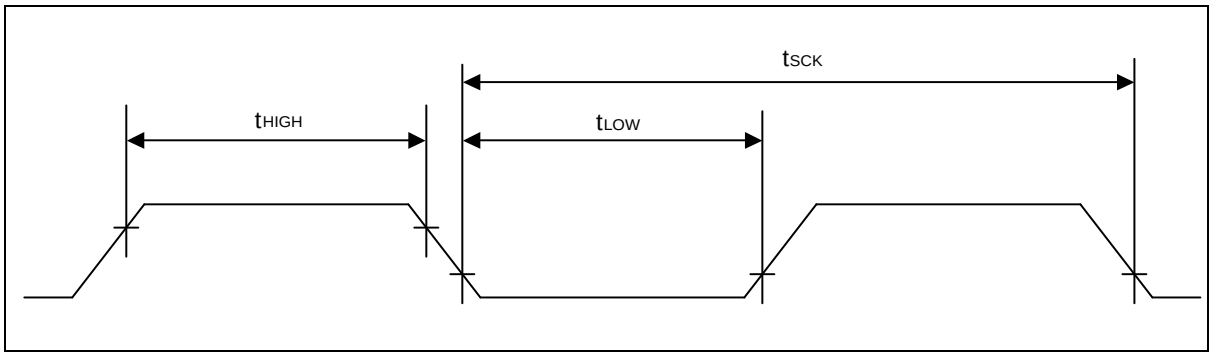


Figure 32. Waveform for UART Timing Characteristics

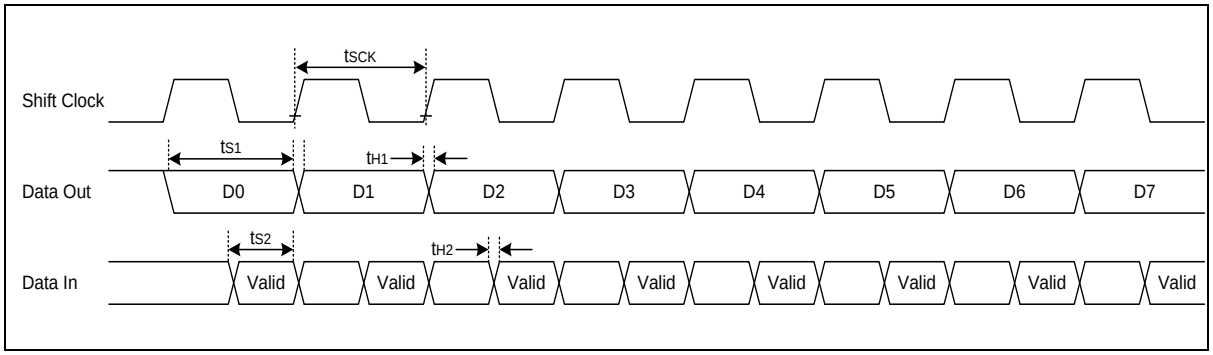


Figure 33. Timing Waveform for the UART Module

19.14 I2C characteristics

Table 30. I2C0/1 Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V)

Parameter	Symbol	Standard Mode		High-Speed Mode		Unit
		MIN	MAX	MIN	MAX	
Clock frequency	tSCL	0	100	0	400	KHz
Clock High Pulse Width	tSCLH	4.0	–	0.6	–	us
Clock Low Pulse Width	tSCLL	4.7	–	1.3	–	
Bus Free Time	tBF	4.7	–	1.3	–	
Start Condition Setup Time	tSTSU	4.7	–	0.6	–	
Start Condition Hold Time	tSTHD	4.0	–	0.6	–	
Stop Condition Setup Time	tSPSU	4.0	–	0.6	–	
Stop Condition Hold Time	tSPHD	4.0	–	0.6	–	
Output Valid from Clock	tVD	0	–	0	–	
Data Input Hold Time	tDIH	0	–	0	1.0	
Data Input Setup Time	tDIS	250	–	100	–	ns

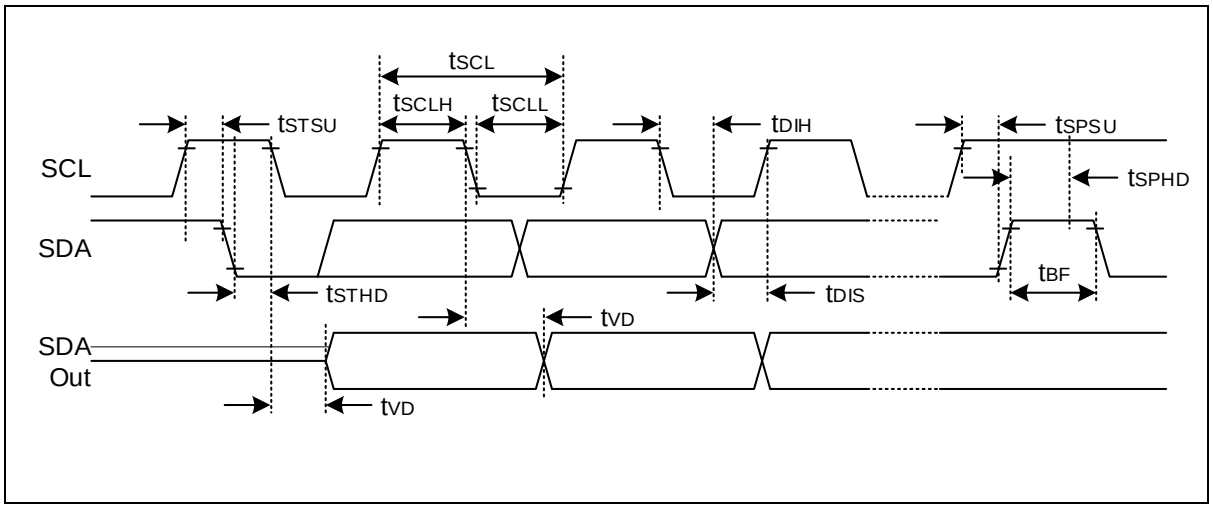


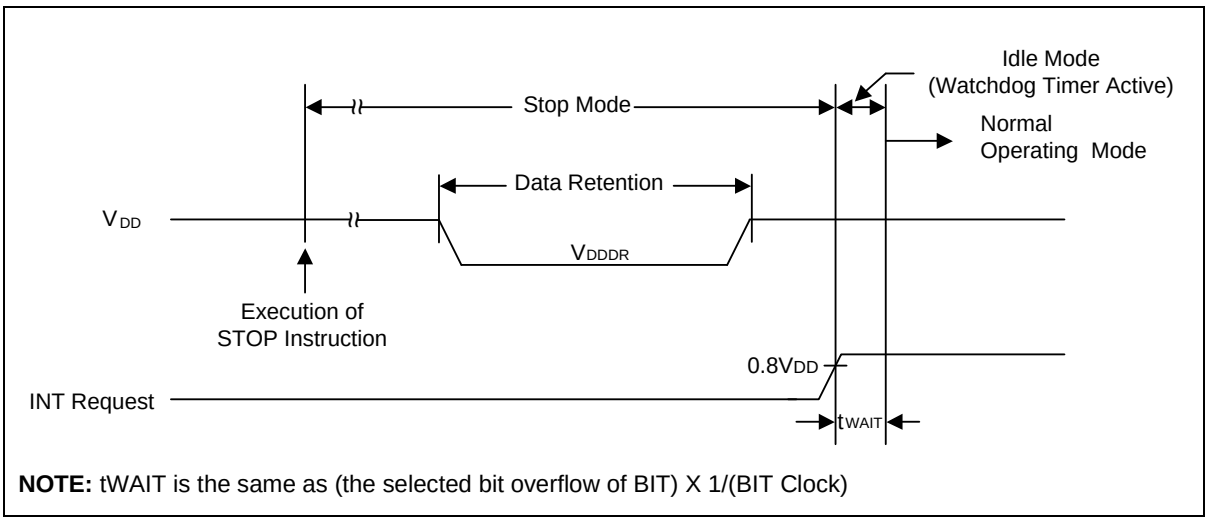
Figure 34. I2C Timing

19.15 Data retention voltage in stop mode

Table 31. Data Retention Voltage in Stop Mode

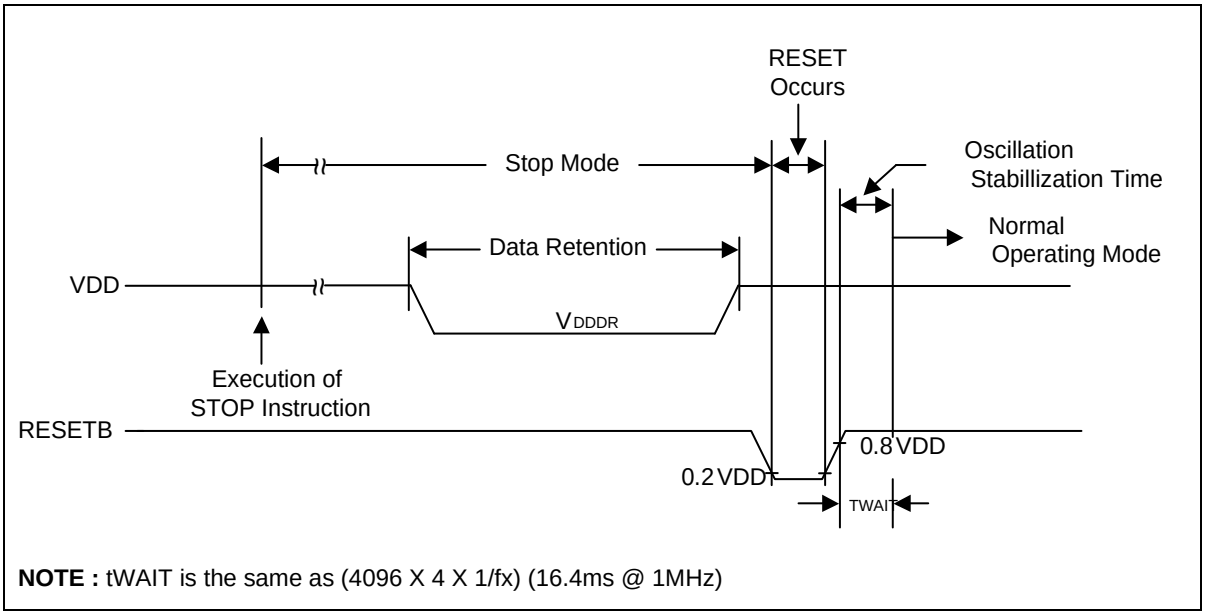
(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	VDDR= 1.8V, (T_A= 25°C), Stop mode	–	–	1	uA



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 35. Stop Mode Release Timing when Initiated by an Interrupt



NOTE : tWAIT is the same as (4096 X 4 X 1/fx) (16.4ms @ 1MHz)

Figure 36. Stop Mode Release Timing when Initiated by RESETB

19.16 Internal flash ROM characteristics

Table 32. Internal Flash ROM Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Sector Write Time	t_{FSW}	–	–	2.5	2.7	ms
Sector Erase Time	t_{FSE}	–	–	2.5	2.7	
Code Write Protection Time	t_{FHL}	–	–	2.5	2.7	
Page Buffer Reset Time	t_{FBR}	–	–	–	5	us
Flash Programming Frequency	f_{PGM}	–	1.25	–	–	KHz
Endurance of Write/Erase	NF_{WE}	–	–	–	10,000	Cycles

19.16.1 Configure Option Control

Table 33. Internal Flash ROM Characteristics (Sectors 248 to 255)

(T_A=25°C, VDD=2.0V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Sector Write Time	t_{FSW}	–	–	2.5	2.7	ms
Sector Erase Time	t_{FSE}	–	–	2.5	2.7	
Code Write Protection Time	t_{FHL}	–	–	2.5	2.7	
Page Buffer Reset Time	t_{FBR}	–	–	–	5	us
Flash Programming Frequency	f_{PGM}	–	1.25	–	–	KHz
Endurance of Write/Erase	NF_{WE}	–	–	–	50,000	Cycles

NOTE: During a flash operation, SCLK[1:0] of SCCR must be set to “00” or “01” (HFO or Main Crystal for system clock).

19.17 Input/output capacitance

Table 34. Input / Output Capacitance

(T_A=-40°C ~ +85°C, VDD=0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Capacitance	C_{IN}	fx= 1MHz Unmeasured pins are connected to VSS	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

NOTE: Guaranteed by design, not tested in production.

19.18 Main clock oscillator characteristics

Table 35. Main Clock Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V)

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Main oscillation frequency	2.0V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	16.0	
Ceramic Oscillator	Main oscillation frequency	2.0V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	16.0	
External Clock	XIN input frequency	2.0V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	16.0	

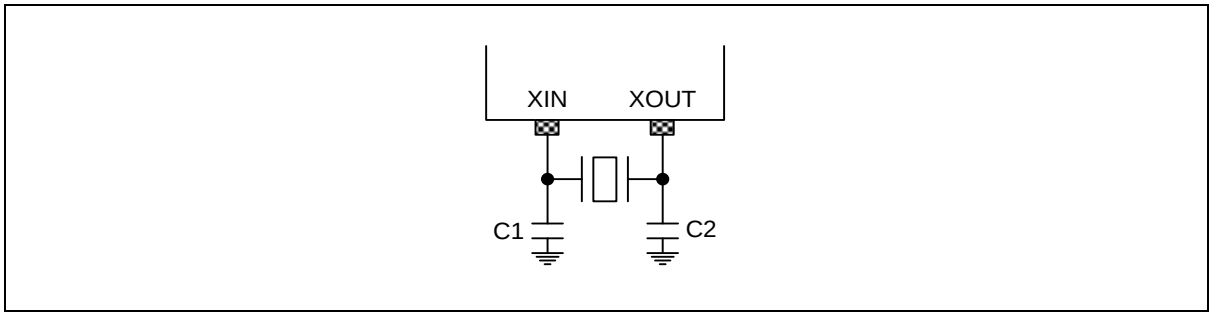


Figure 37. Main Clock Oscillator Characteristics

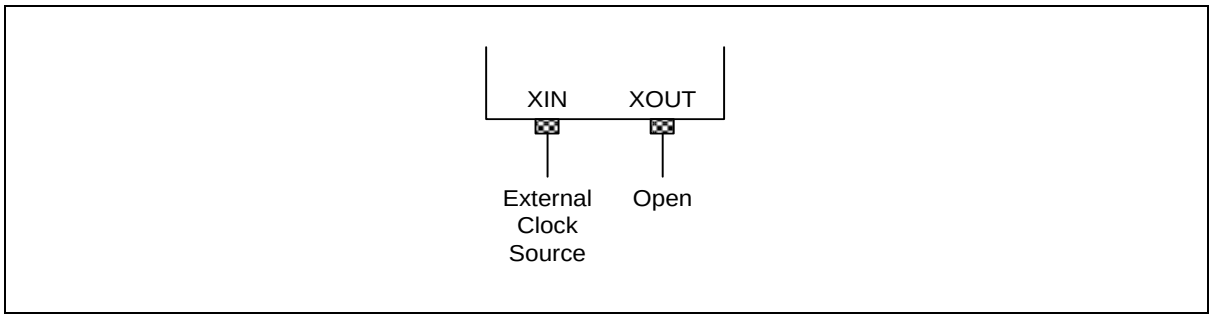


Figure 38. External Clock

19.19 Main oscillation stabilization characteristics

Table 36. Main Oscillation Stabilization Characteristics

(T_A=-40°C ~ +85°C, VDD=2.0V ~ 5.5V)

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	fx > 1MHz Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	–	–	60	ms
Ceramic		–	–	10	ms
External Clock	f_{XIN} = 0.4 to 16MHz XIN input high and low width (t_{XH}, t_{XL})	42	–	1250	ns

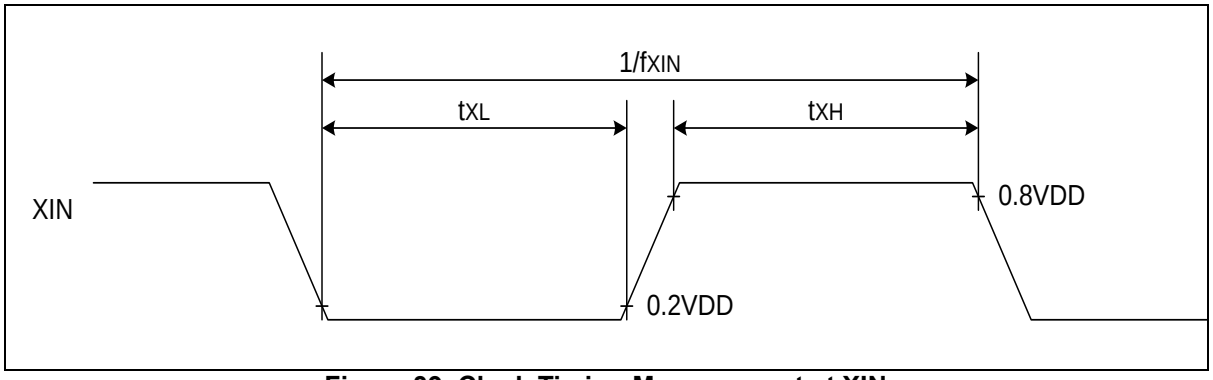


Figure 39. Clock Timing Measurement at XIN

19.20 Operating voltage range

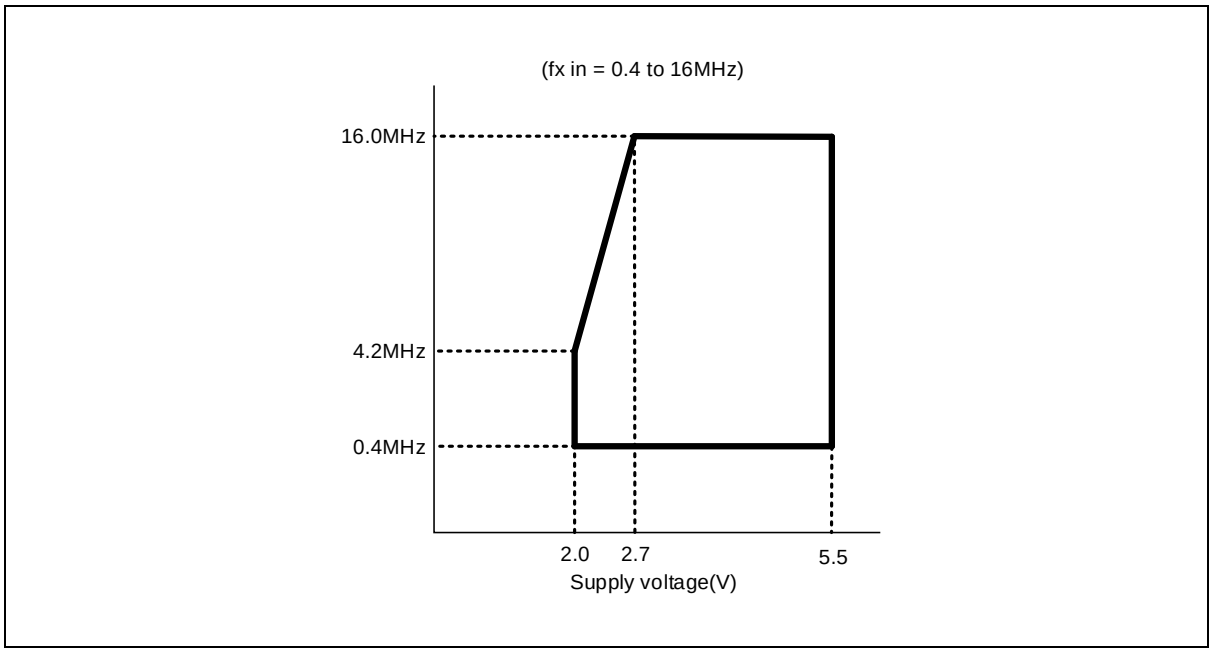


Figure 40. Operating Voltage Range

19.21 Recommended circuit and layout

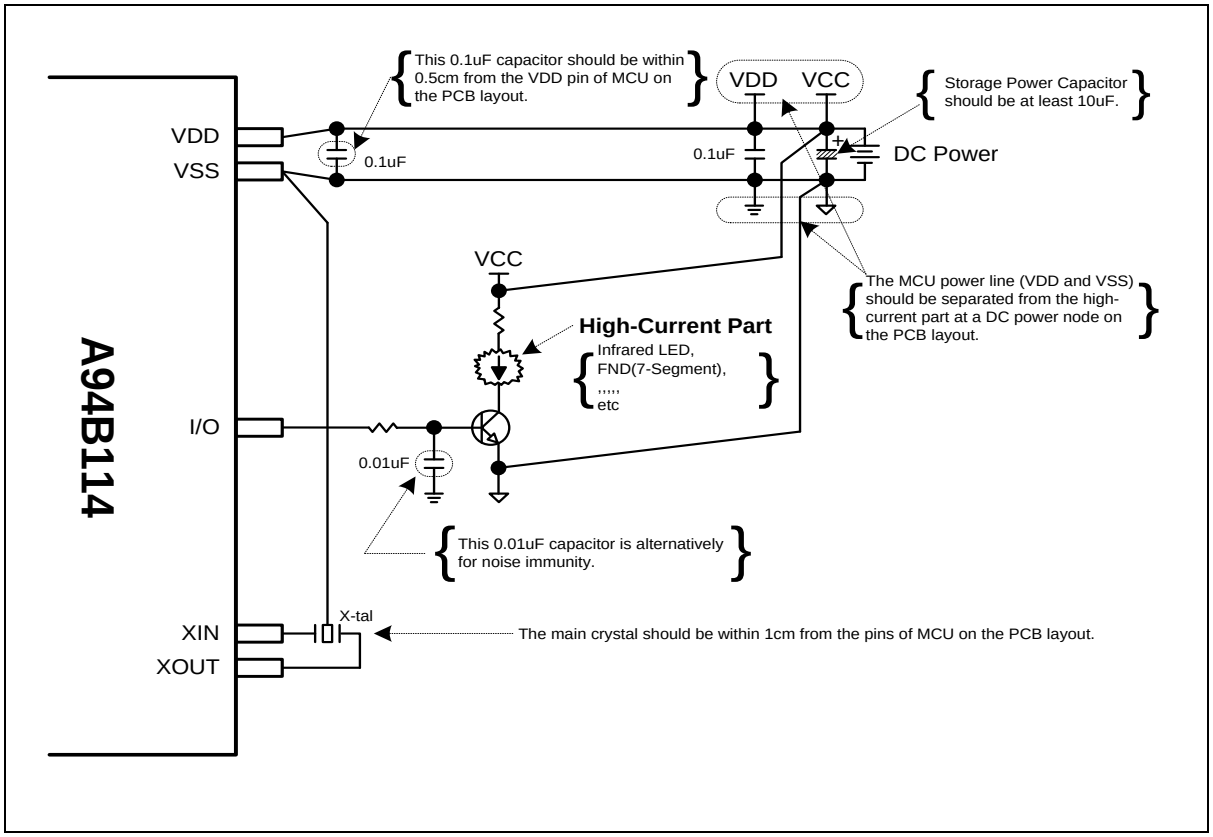


Figure 41. Recommended Voltage Range

19.22 Typical characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range. The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean – 3σ) respectively where σ is standard deviation.

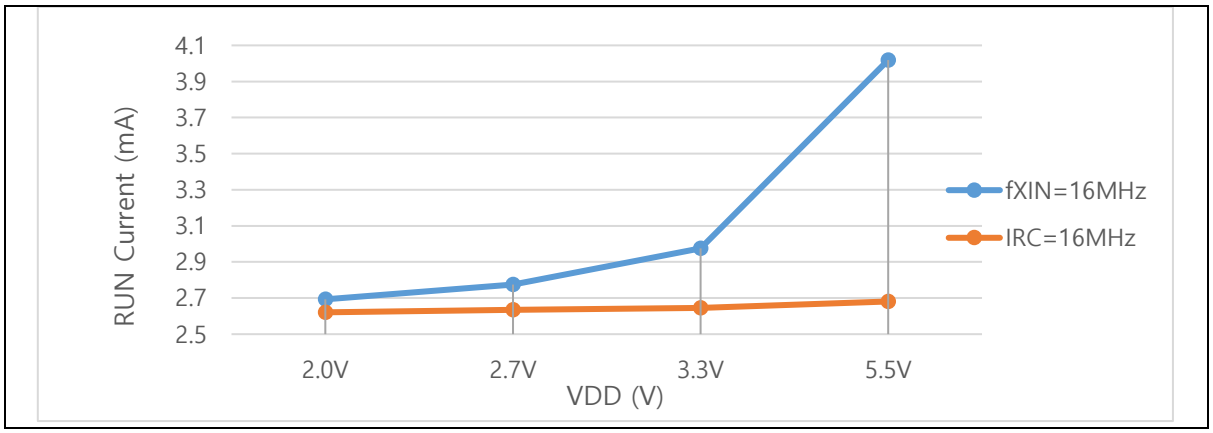


Figure 42. RUN (IDD1) Current

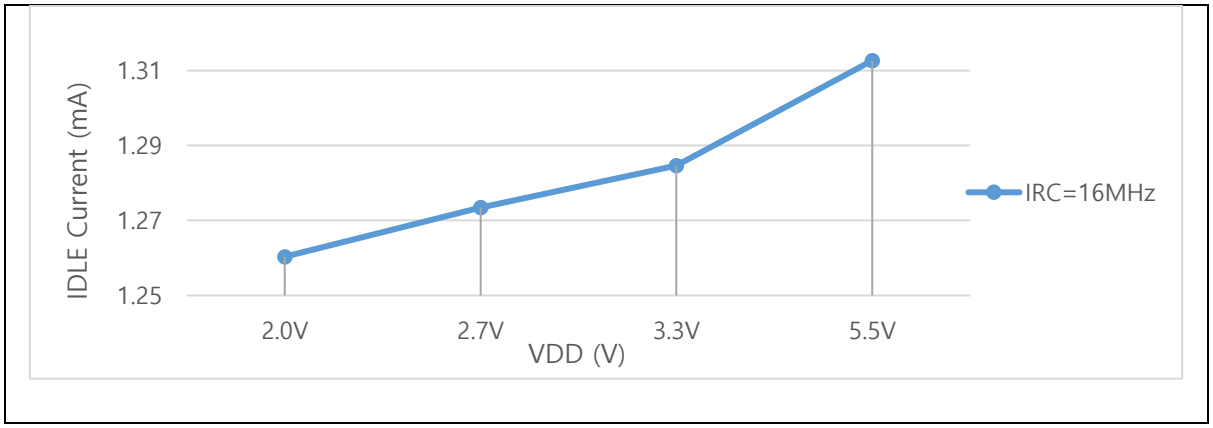


Figure 43. IDLE (IDD2) Current

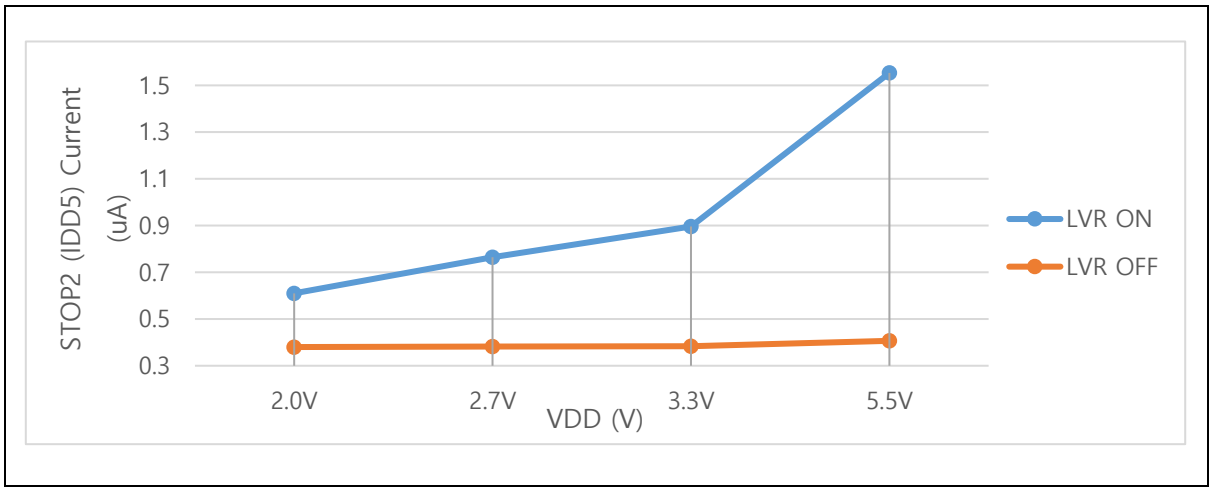


Figure 44. STOP (IDD5) Current

20 Development tools

This chapter introduces wide range of development tools for A94B114. ABOV offers software tools, debuggers, and programmers to help a user in generating right results to match target applications. ABOV supports entire development ecosystem of the customers.

20.1 Compiler

ABOV semiconductor does not provide any compiler for A94B114. It is recommended to consult a compiler provider. But the CPU core of A94B114 is CM8051-S core, you can use all kinds of third party's standard 8051 compiler like Keil C Compiler, Open Source SDCC (Small Device C Compiler). These compilers' output debug information can be integrated with our OCD2 emulator and debugger. Refer to OCD2 manual for more details.

20.2 OCD (On-chip debugger) emulator and debugger

The OCD emulator supports ABOV's 8051 series MCU emulation. The OCD uses two wires interfacing between PC and MCU, which is attached to user's system. The OCD can read or change the value of MCU's internal memory and I/O peripherals. In addition, the OCD controls MCU's internal debugging logic. This means OCD controls emulation, step run, monitoring and many more functions regarding debugging.

The OCD debugger program runs underneath MS operating system such as MS-Windows NT/ 2000/ XP/ Vista (32-bit). If a user wants to see more details, it is recommend to refer to OCD debugger manual by visiting ABOV's website (http://www.abovsemiii.com) and downloading debugger S/W and corresponding manuals.

- Connection:
  - DSCL (A94B114 P01 port)
  - DSDA (A94B114 P00 port)

Figure 45 shows pinouts of OCD connector.

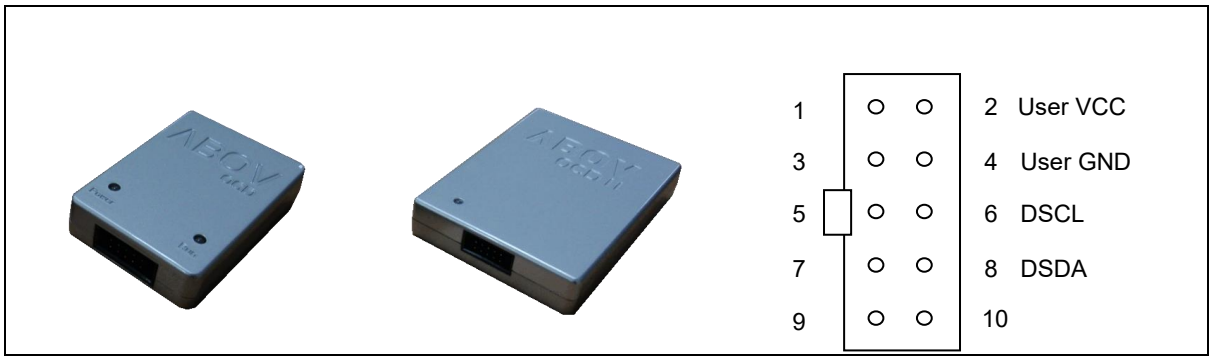


Figure 45. Debugger (OCD1/OCD2) and Pinouts

20.3 Programmers

20.3.1 E-PGM+

E-PGM+ USB is a single programmer. A user can program A94B114 directly using the E-PGM+.

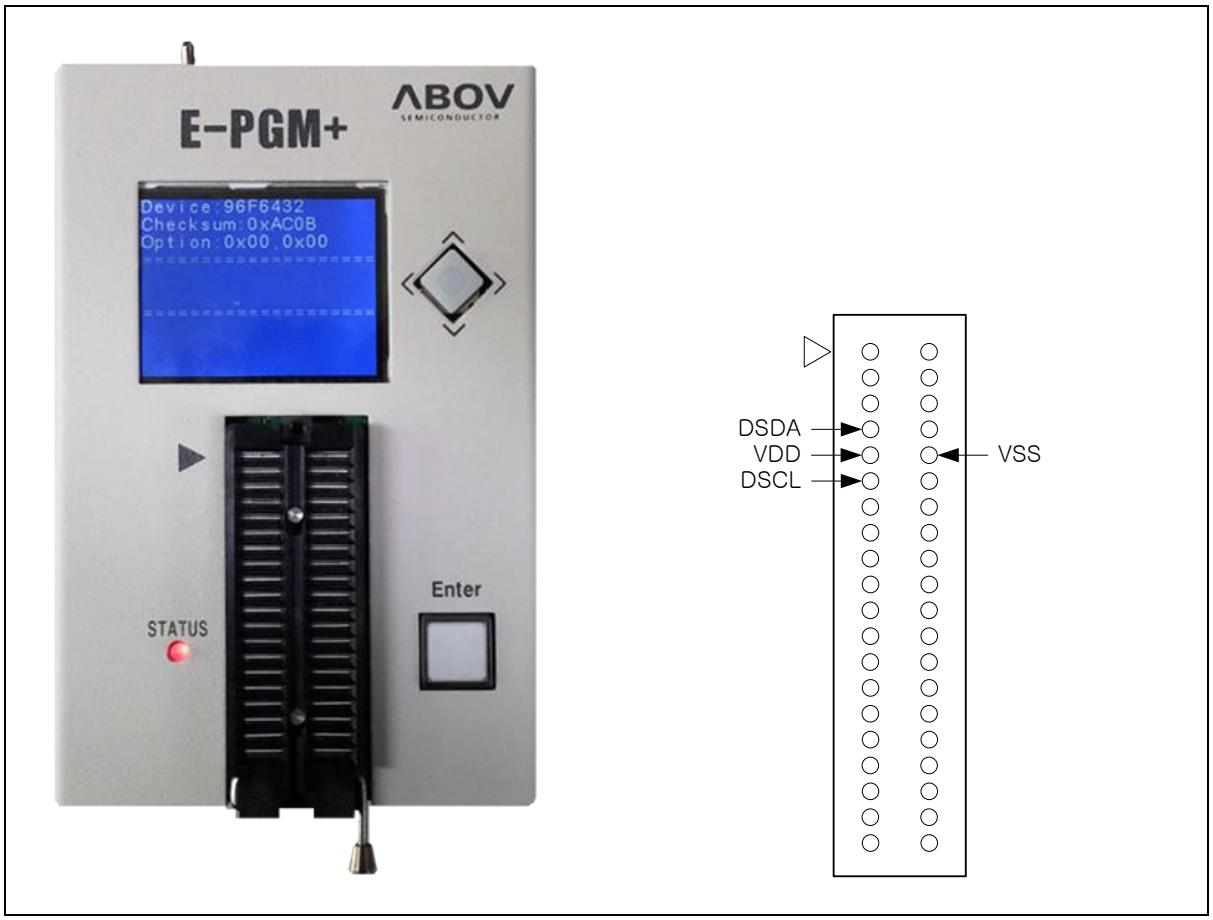


Figure 46. E-PGM+ (Single Writer) and Pinouts

20.3.2 PGMPlusLC2

PGMPlusLC2 is for ISP(In System Programming). It is used to write into the MCU Which is already mounted on target board using 10pin cable.

Features :

- PGMplusLC2 is low cost writing Tool.
- USB interface is supported.
- Not need USB driver installation.
- Connect the external power adaptor(5V@2A).
- Supported high voltage Max 18V.
- PGMplusLC2 is based on PC environment.
- PGMplusLC2 is faster than PGMplusLC.
- Transmission speed is 64KB/s

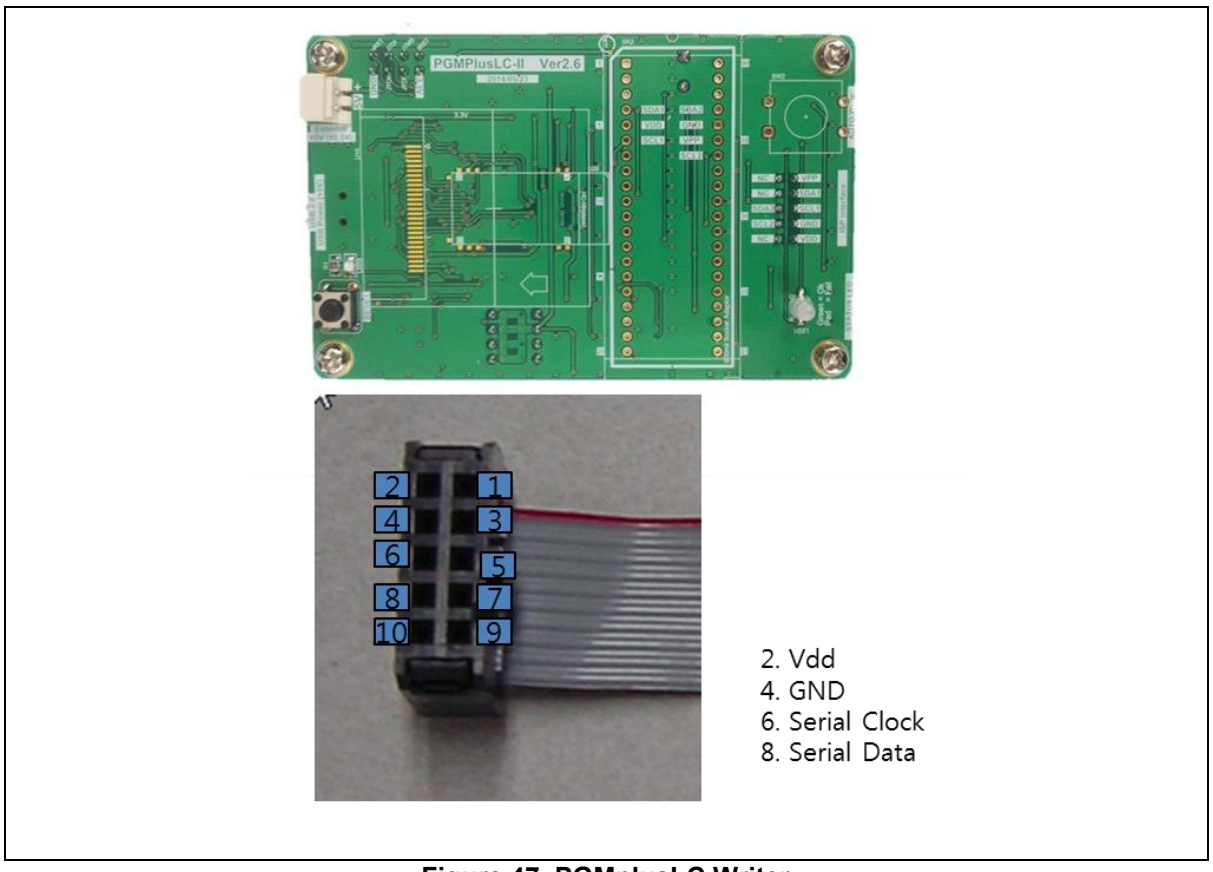


Figure 47. PGMplusLC Writer

20.3.3 Gang programmer

E-Gang4 and E-Gang6 allows a user to program on multiple devices at a time. They run not only in PC controlled mode but also in standalone mode without PC control. USB interface is available and it is easy to connect to the handler.

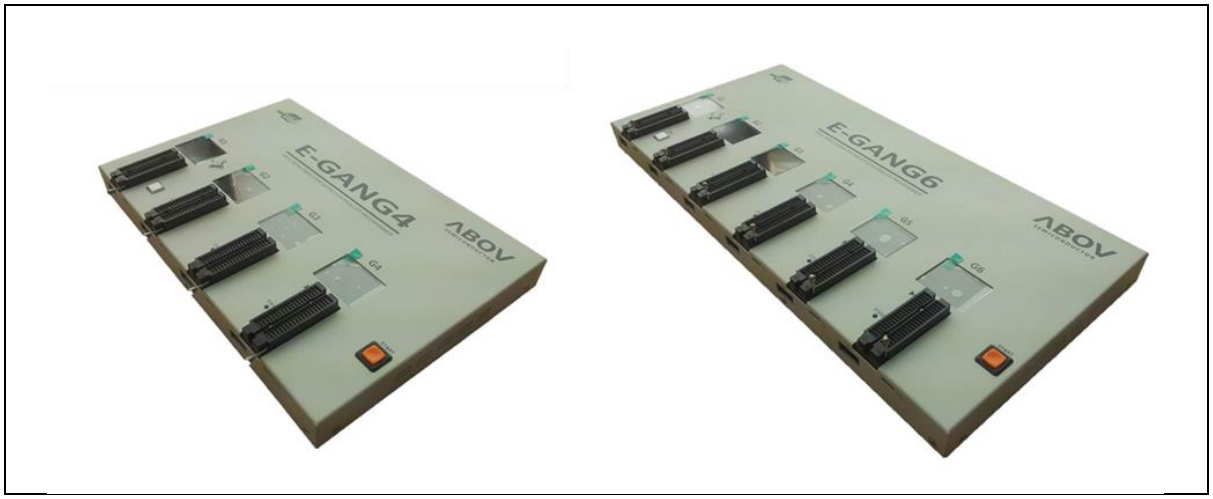
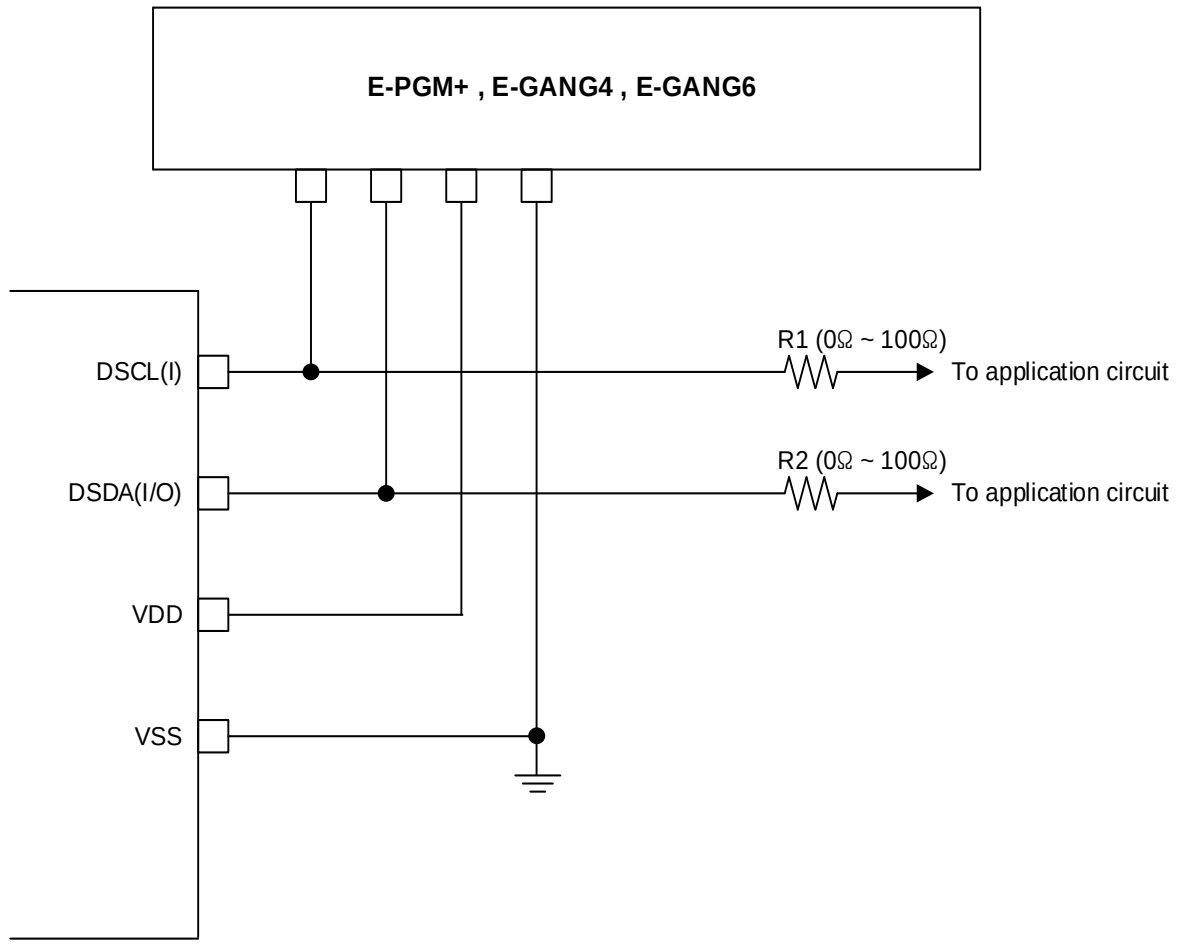


Figure 48. Gang Programmer

20.4 Circuit Design Guide

When programming flash memory, the programming tool needs 4 signal lines, DSCL, DSDA, VDD, and VSS. If a user designs a PCB circuit, the user should consider the usage of these 4 signal lines for the on-board programming.

Please be careful to design the related circuit of these signal pins because rising/falling timing of DSCL and DSDA is very important for proper programming.



NOTES:

7. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
8. The value of R1 and R2 is recommended value. It varies with circuit of system.
9. When using LFO (Low Frequency Oscillator), it is recommended that the resistance value of R2 is 100 ohms. Because the internal De-bounce circuit does not operate normally at low clocks, this prevents Glitch from corrupting OCD communication.

Figure 49. PCB Design Guide for On-Board Programming

20.5 On-chip debug system

A94B114 can use On-chip debug (OCD). On-chip debug system (OCD) of A94B114 can be used for programming the non-volatile memories and on-chip debugging. Detail descriptions for programming via the OCD interface can be found in the following chapter.

Table 37. OCD Features

Two wire external interface	• 1 for serial clock input • 1 for bi-directional serial data bus
Debugger accesses	• All internal peripherals • Internal data RAM • Program Counter • Flash memory and data EEPROM memory
Extensive On-Chip Debugging supports for Break Conditions	• Break instruction • Single step break • Program memory break points on single address • Programming of Flash, EEPROM, Fuses, and Lock bits through the two-wire interface • On-Chip Debugging supported by Dr. Choice®
Operating frequency	The maximum frequency of a target MCU.

Figure 50 shows a block diagram of the OCD interface and the On-chip Debug system.

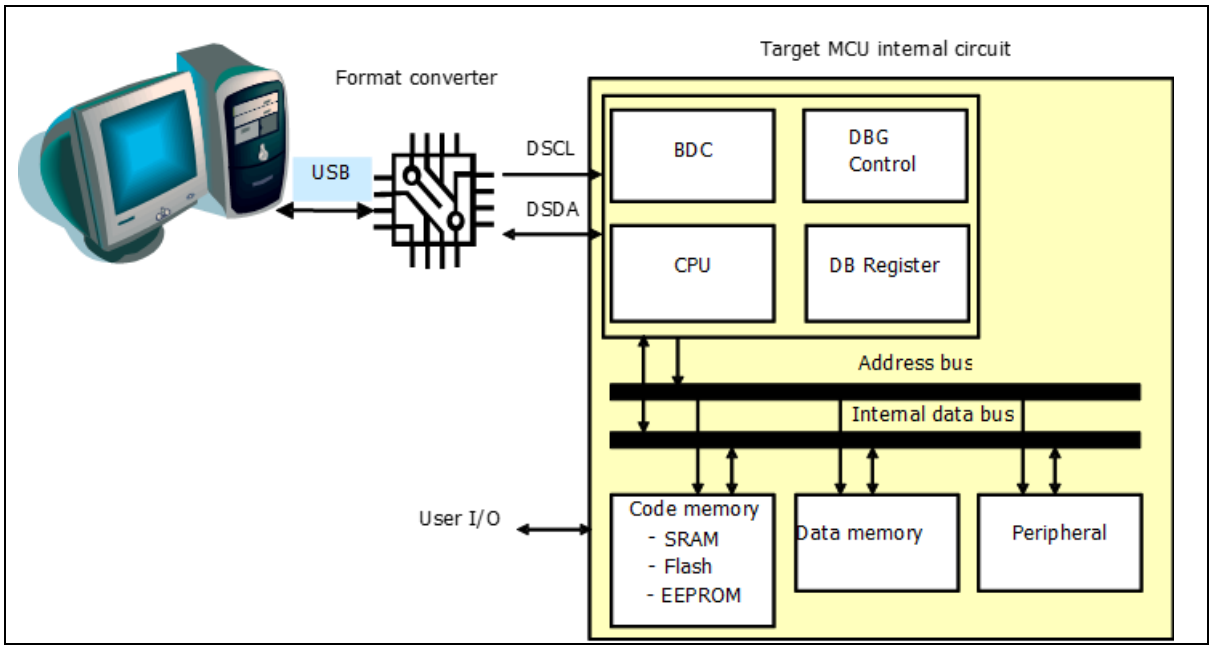


Figure 50. On-Chip Debugging System in Block Diagram

20.5.1 Two-pin external interface

Basic transmission packet

- 10-bit packet transmission using two-pin interface.
- 1-packet consists of 8-bit data, 1-bit parity and 1-bit acknowledge.
- Parity is even of '1' for 8-bit data in transmitter.
- Receiver generates acknowledge bit as '0' when transmission for 8-bit data and its parity has no error.
- When transmitter has no acknowledge (Acknowledge bit is '1' at tenth clock), error process is executed in transmitter.
- When acknowledge error is generated, host PC makes stop condition and transmits command which has error again.
- Background debugger command is composed of a bundle of packet.
- Start condition and stop condition notify the start and the stop of background debugger command respectively.

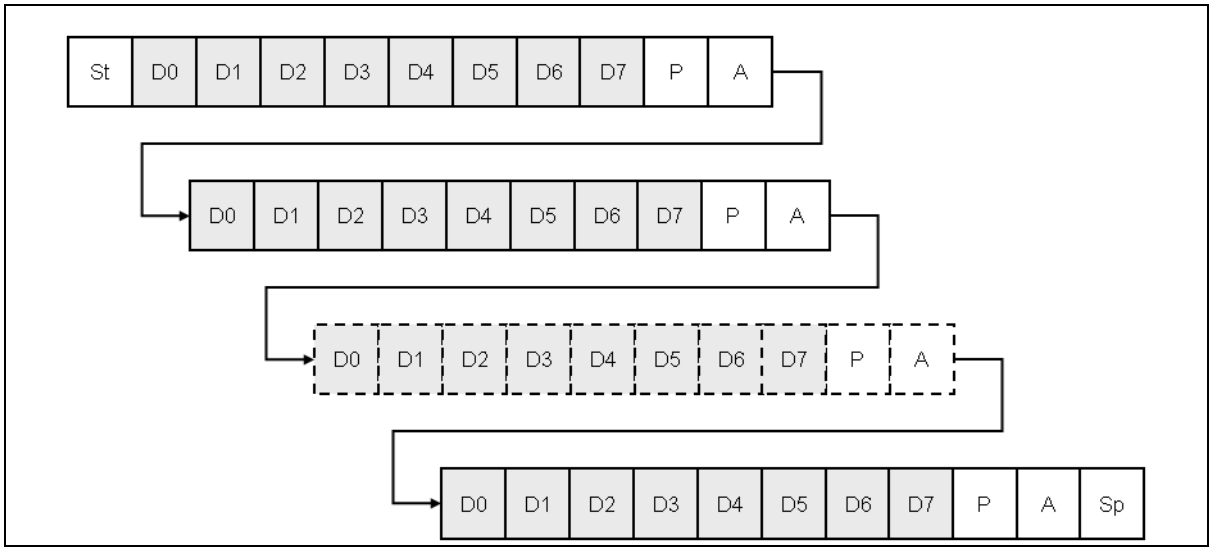


Figure 51. 10-bit Transmission Packet

Packet transmission timing

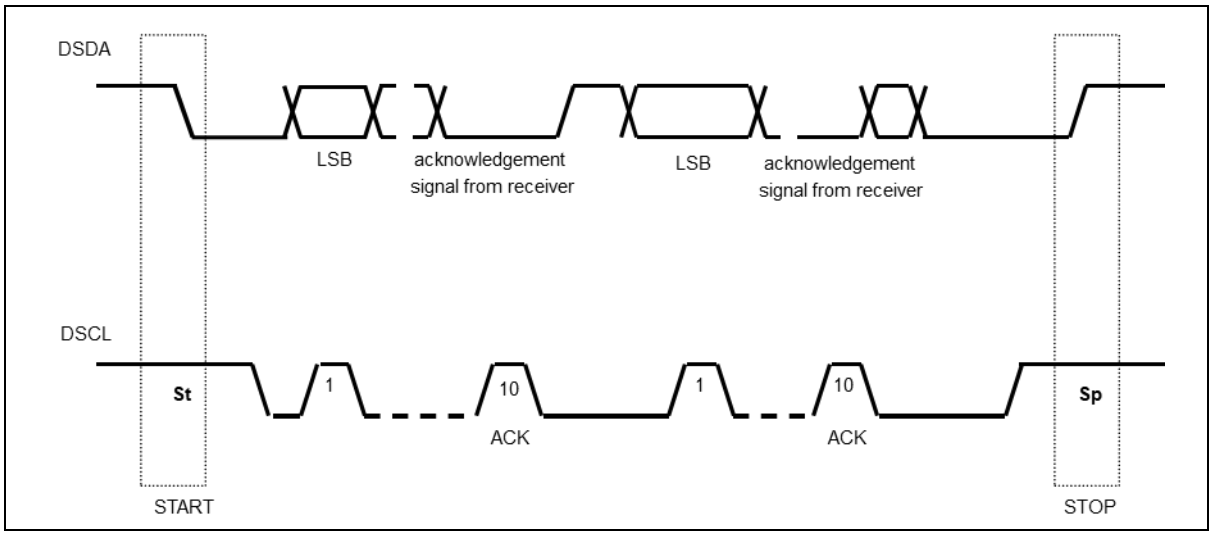


Figure 52. Data Transfer on Twin Bus

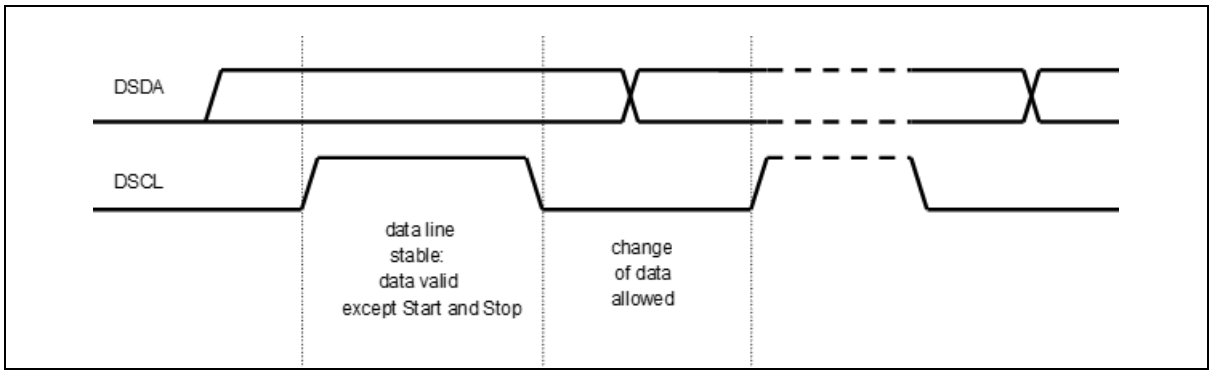


Figure 53. Bit Transfer on Serial Bus

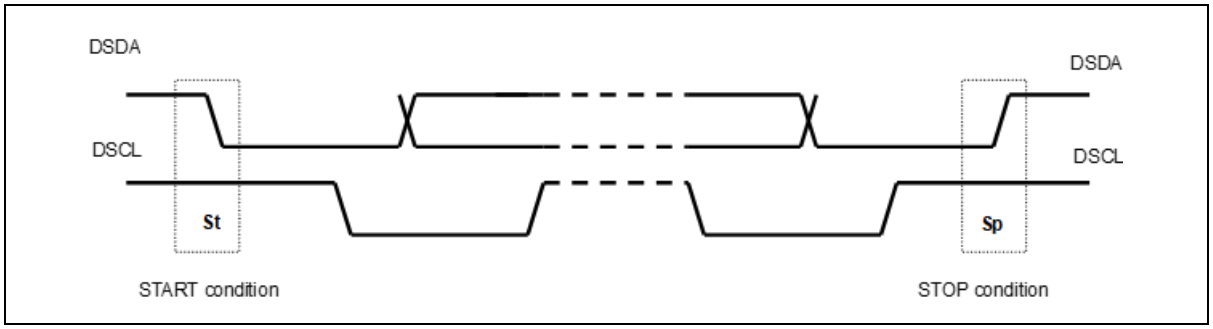


Figure 54. Start and Stop Condition

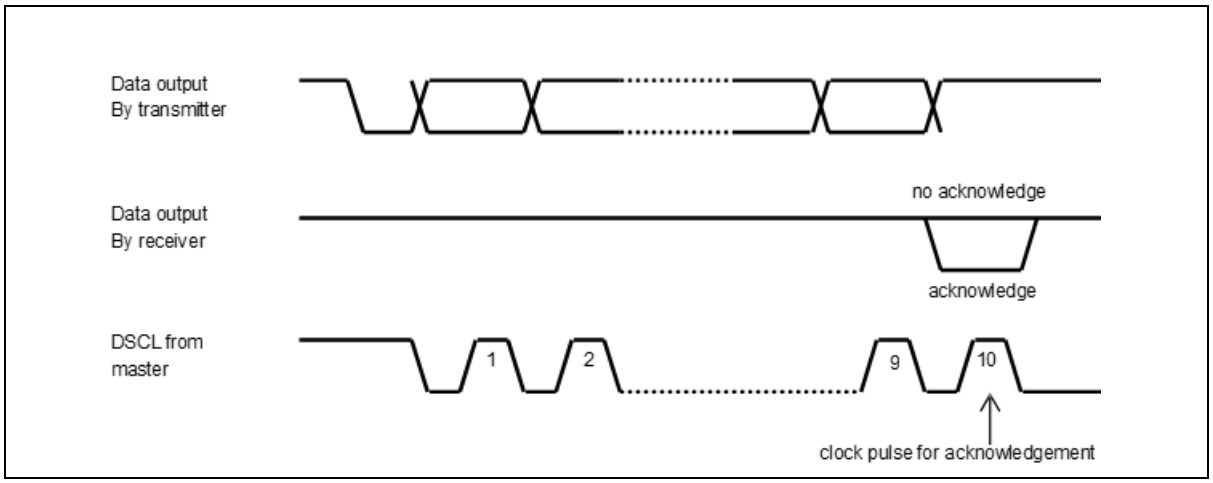


Figure 55. Acknowledge on Serial Bus

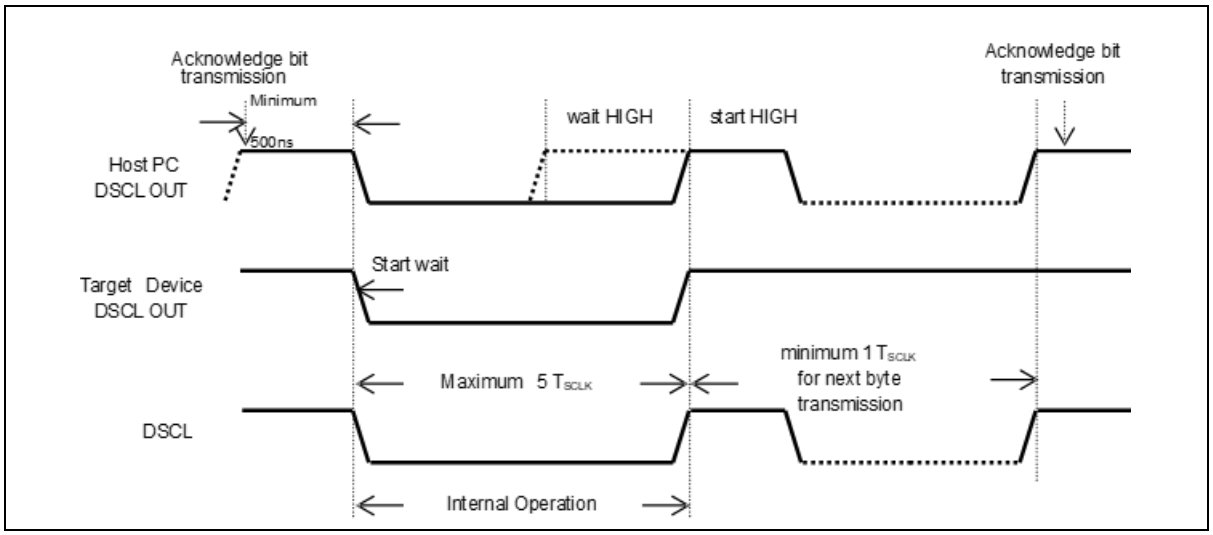


Figure 56. Clock Synchronization during Wait Procedure

Connection of transmission

Two-pin interface connection uses open-drain (wire-AND bidirectional I/O).

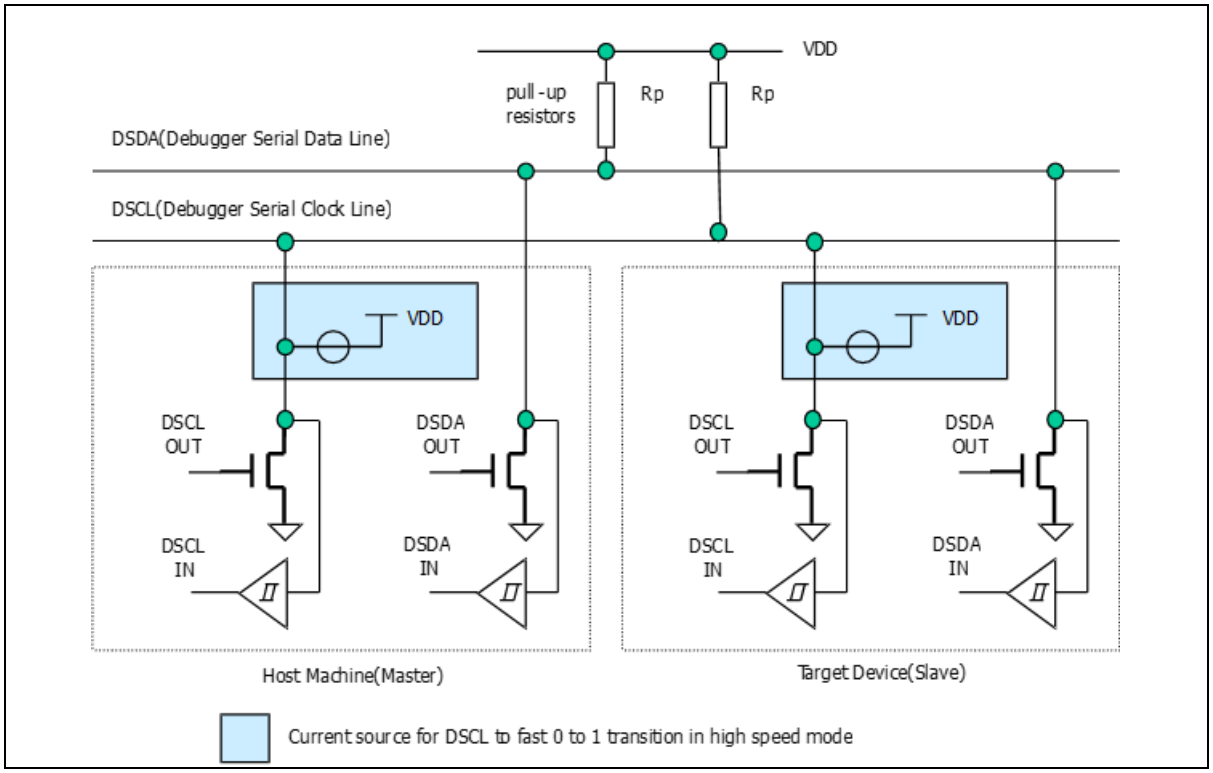


Figure 57. Connection of Transmission

21 Package information

This chapter provides A94B114 package information.

21.1 20 TSSOP package information

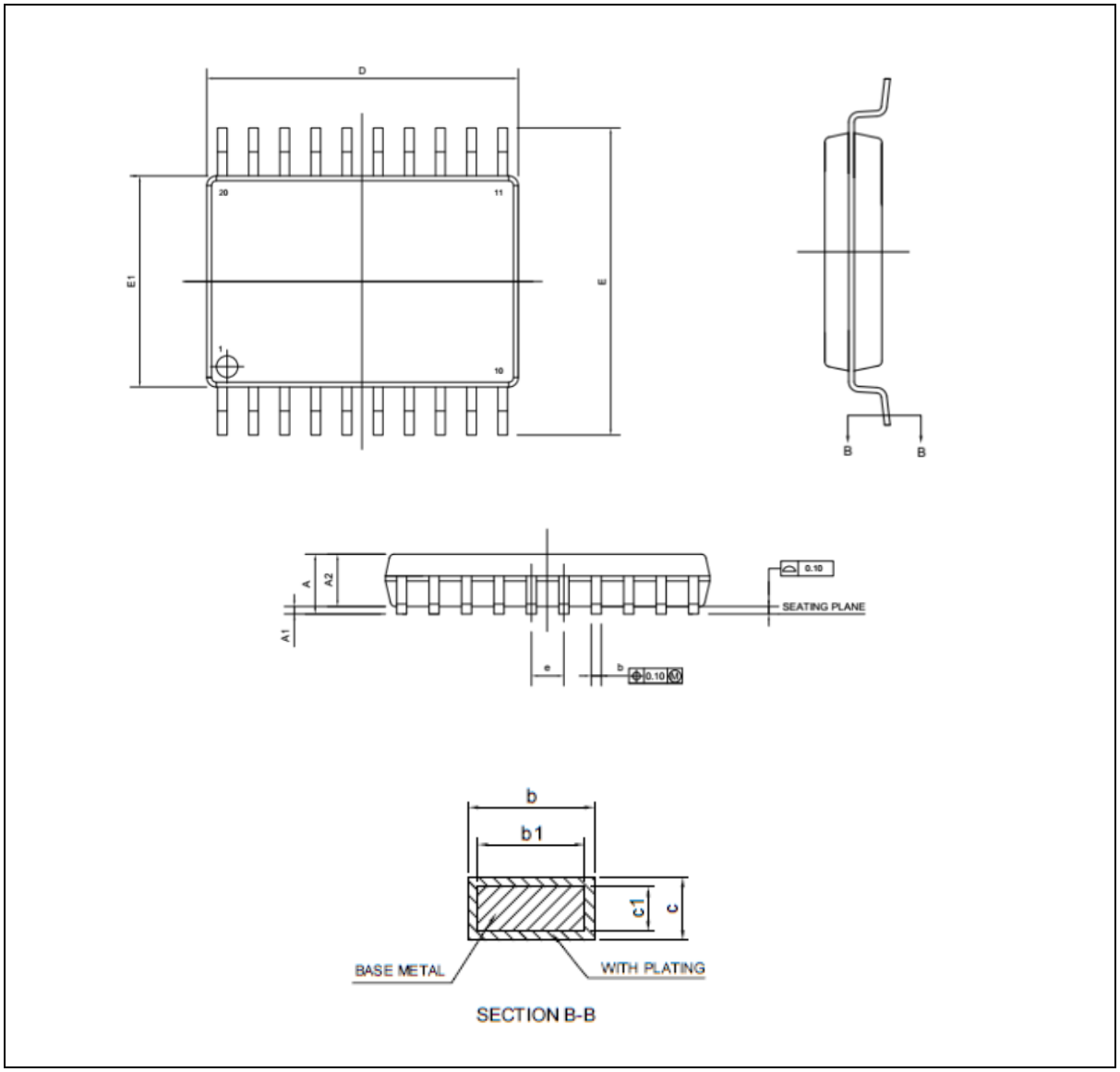


Figure 58. 20 TSSOP Package Outline

Table 38. 20 TSSOP Package Mechanical Data

Symbol	Min.	Nom.	Max.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
b1	0.19	0.22	0.25
c	0.09	—	0.20
c1	0.09	—	0.16
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
Θ	**0°**	—	8°

NOTES:

10. All dimensions refer to JEDEC standard MO-153-AC.
11. Dimension ‘D’ does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.
12. Dimension ‘E1’ does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side.
13. Dimension ‘b’ does not include dambar protrusion. Allowable dambar protrusion shall be 0.10 mm total in excess of the ‘b’ dimension maximum material condition.
14. ‘A1’ is defined as the vertical distance from the seating plane to the lowest point on the package body.
15. Units of measure = millimeter

21.2 20 SOP package information

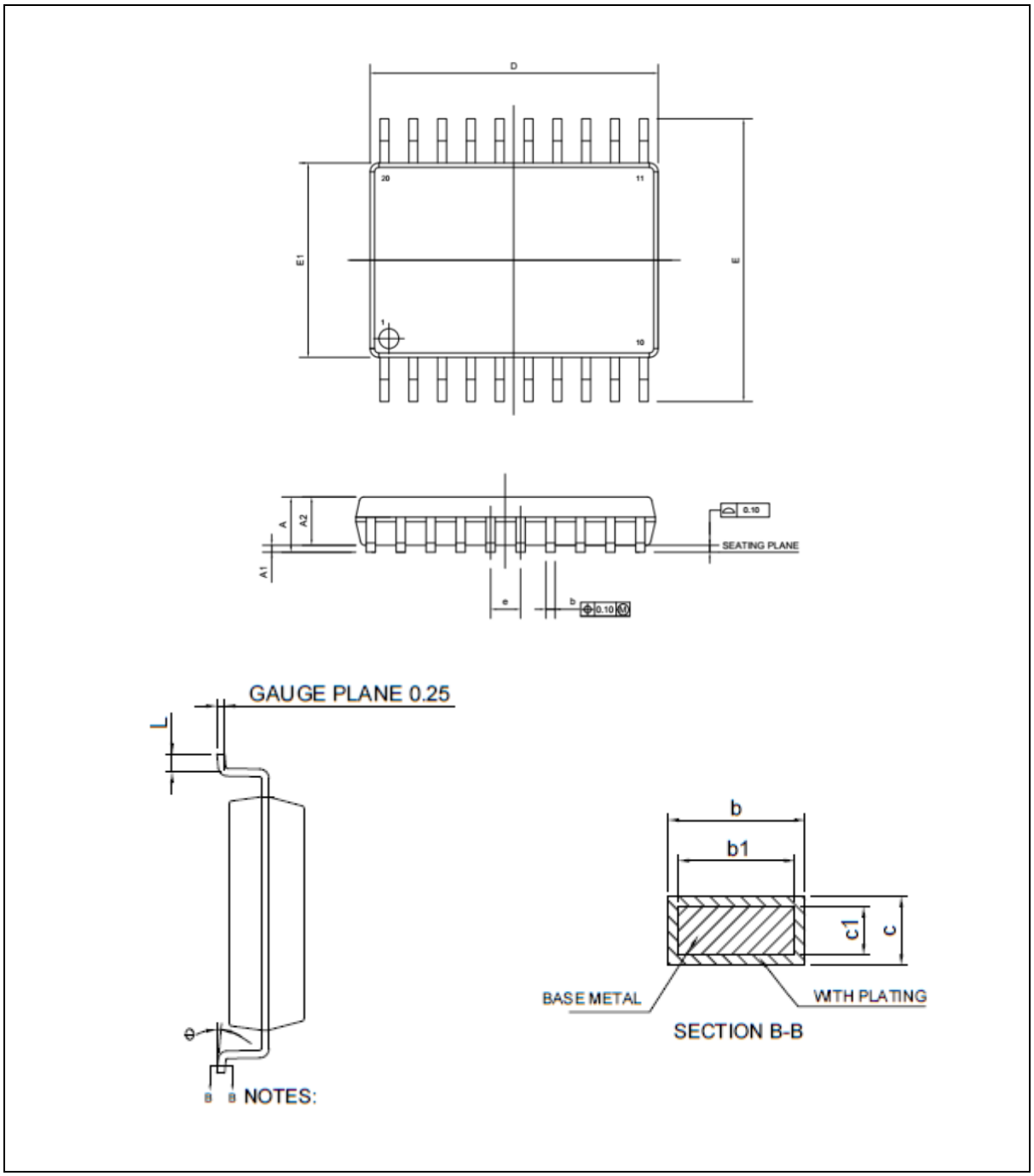


Figure 59. 20 SOP Package Outline

Table 39. 20 SOP Package Mechanical Data

Symbol	Min.	Nom.	Max.
A	—	—	2.65
A1	0.10	—	0.30
A2	2.05	—	—
b	0.31	—	0.51
b1	0.27	—	0.48
c	0.10	—	0.33
c1	0.10	—	0.30
D	12.60	—	13.00
E	10.00	—	10.60
E1	7.30	—	7.70
e	1.27 BSC		
L	0.40	—	1.27
Θ	0°	—	8°

NOTES:

16. All dimensions refer to JEDEC standard MS-013-AC.
17. Dimension ‘D’ does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.
18. Dimension ‘E1’ does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side.
19. Dimension ‘b’ does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the ‘b’ dimension at maximum material condition.
20. ‘A1’ is defined as the vertical distance from the seating plane to the lowest point on the package body.
21. Units of measure = millimeter

21.3 16 SOPN package information

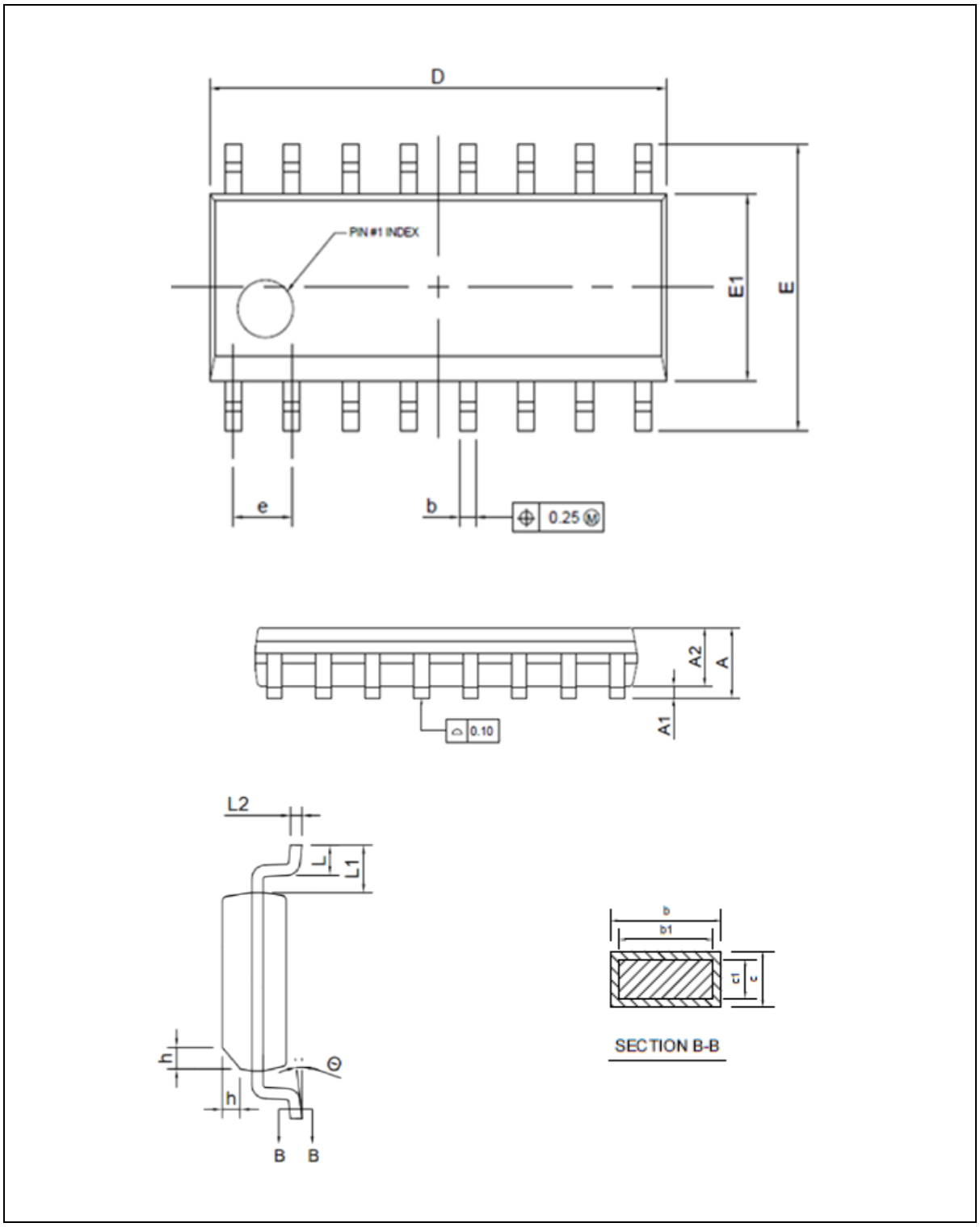


Figure 60. 16 SOPN Package Outline

Table 40. 16 SOPN Package Mechanical Data

Symbol	Min.	Nom.	Max.
A	—	—	1.75
A1	0.10	—	0.25
A2	1.25	—	—
b	0.31	—	0.51
B1	0.28	—	0.48
c	0.10	—	0.26
c1	0.10	—	0.23
D	9.70	9.90	10.20
E	5.80	6.00	6.20
E1	3.70	3.90	4.20
e	1.27 BSC		
L	0.40	—	1.27
L1	1.04 BSC		
L2	0.25 BSC		
h	0.25	—	0.50
Θ	0°	—	8°

NOTES:

22. All dimensions refer to JEDEC standard MS-012-AC.
23. Dimension ‘D’ does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side. Dimension ‘E1’ does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side.
24. Dimension ‘b’ does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the ‘b’ dimension at maximum material condition.
25. Units of measure = millimeter

22 Ordering information

Table 41. A94B114 Device Ordering Information

Device name	FLASH	XRAM	IRAM	ADC	I/O PORT	Package
A94B114FR	8Kbytes	256bytes	256bytes	10inputs	18	20 TSSOP
A94B114FD				10inputs	18	20 SOP
A94B114AE				8inputs	14	16 SOPN

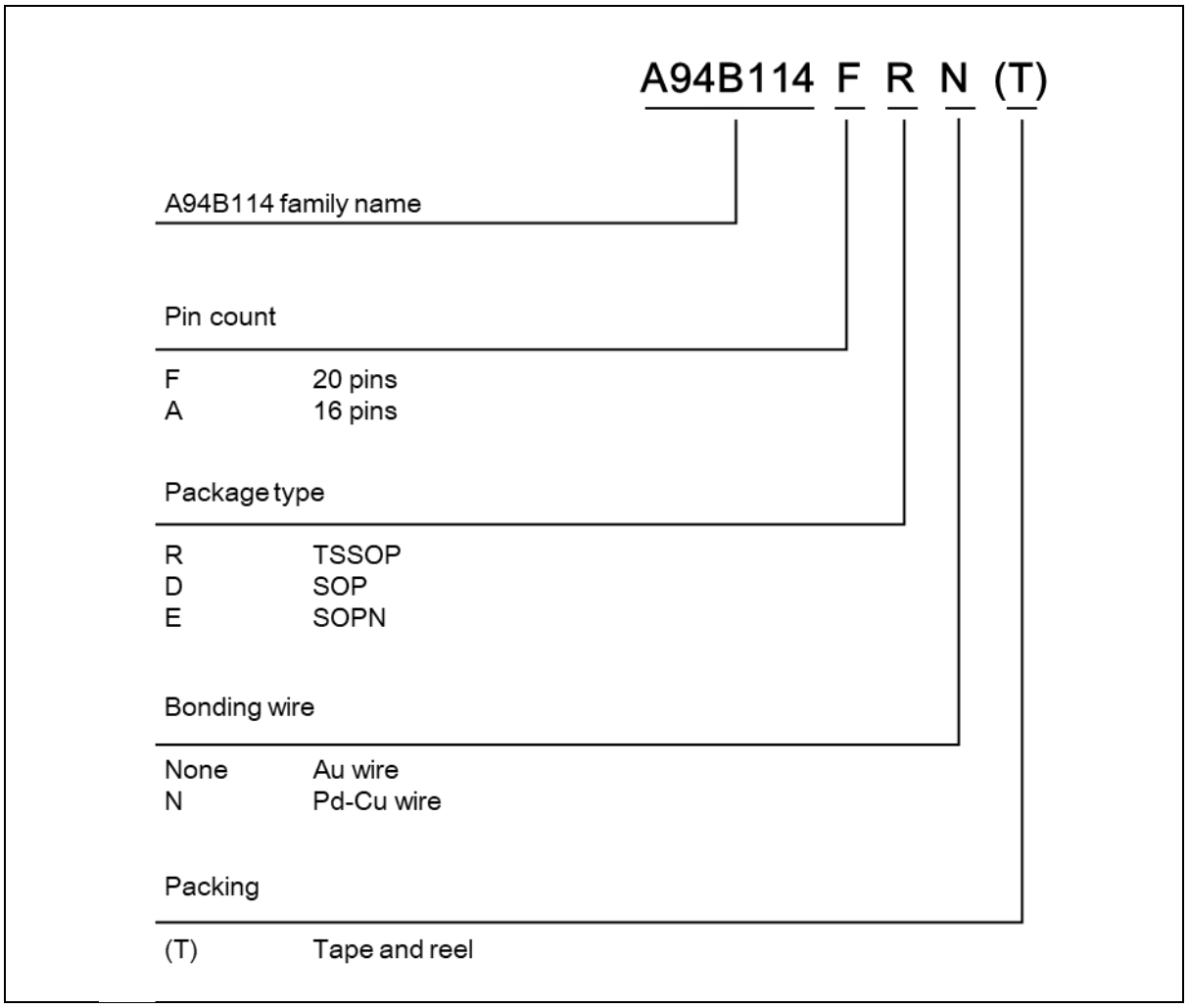


Figure 61. A94B114 Device Numbering Nomenclature

Appendix

Instruction table

Instructions are either1, 2 or 3bytes long as listed in the 'Bytes' column below. Each instruction takes either 1, 2, 3, 4 or 5 machine cycles to execute as listed in the following table. 1 machine cycle comprises 1 system clock cycles.

Table 42. Instruction Table

ARITHMETIC				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ADD A,Rn	Add register to A	1	2	28-2F
ADD A,dir	Add direct byte to A	2	3	25
ADD A,@Ri	Add indirect memory to A	1	3	26-27
ADD A,#data	Add immediate to A	2	2	24
ADDC A,Rn	Add register to A with carry	1	2	38-3F
ADDC A,dir	Add direct byte to A with carry	2	3	35
ADDC A,@Ri	Add indirect memory to A with carry	1	3	36-37
ADDC A,#data	Add immediate to A with carry	2	2	34
SUBB A,Rn	Subtract register from A with borrow	1	2	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	3	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	3	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	2	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	2	08-0F
INC dir	Increment direct byte	2	3	05
INC @Ri	Increment indirect memory	1	3	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	2	18-1F
DEC dir	Decrement direct byte	2	3	15
DEC @Ri	Decrement indirect memory	1	3	16-17
INC DPTR	Increment data pointer	1	1	A3
MUL AB	Multiply A by B	1	8	A4
DIV AB	Divide A by B	1	8	84
~~DA A~~ ~~NOTE1~~	~~Decimal Adjust A~~	~~1~~	~~1~~	~~D4~~

Table 42. Instruction Table (continued)

LOGICAL				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ANL A,Rn	AND register to A	1	2	58-5F
ANL A,dir	AND direct byte to A	2	3	55
ANL A,@Ri	AND indirect memory to A	1	3	56-57
ANL A,#data	AND immediate to A	2	2	54
ANL dir,A	AND A to direct byte	2	3	52
ANL dir,#data	AND immediate to direct byte	3	3	53
ORL A,Rn	OR register to A	1	2	48-4F
ORL A,dir	OR direct byte to A	2	3	45
ORL A,@Ri	OR indirect memory to A	1	3	46-47
ORL A,#data	OR immediate to A	2	2	44
ORL dir,A	OR A to direct byte	2	3	42
ORL dir,#data	OR immediate to direct byte	3	3	43
XRL A,Rn	Exclusive-OR register to A	1	2	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	3	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	3	66-67
XRL A,#data	Exclusive-OR immediate to A	2	2	64
XRL dir,A	Exclusive-OR A to direct byte	2	3	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	3	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13

Table 42. Instruction Table (continued)

DATA TRANSFER				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOV A,Rn	Move register to A	1	2	E8-EF
MOV A,dir	Move direct byte to A	2	3	E5
MOV A,@Ri	Move indirect memory to A	1	3	E6-E7
MOV A,#data	Move immediate to A	2	2	74
MOV Rn,A	Move A to register	1	2	F8-FF
MOV Rn,dir	Move direct byte to register	2	3	A8-AF
MOV Rn,#data	Move immediate to register	2	2	78-7F
MOV dir,A	Move A to direct byte	2	2	F5
MOV dir,Rn	Move register to direct byte	2	2	88-8F
MOV dir,dir	Move direct byte to direct byte	3	3	85
MOV dir,@Ri	Move indirect memory to direct byte	2	3	86-87
MOV dir,#data	Move immediate to direct byte	3	3	75
MOV @Ri,A	Move A to indirect memory	1	2	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	3	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	3	76-77
MOV DPTR,#data	Move immediate to data pointer	3	3	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative PC to A	1	2	83
MOVX A,@Ri	Move external data (A8) to A	1	2	E2-E3
MOVX A,@DPTR	Move external data (A16) to A	1	2	E0
MOVX @Ri,A	Move A to external data (A8)	1	1	F2-F3
MOVX @DPTR,A	Move A to external data (A16)	1	1	F0
PUSH dir	Push direct byte onto stack (except PUSH SP)[NOTE1]	2	3	C0
POP dir	Pop direct byte from stack (except POP SP)[NOTE1]	2	3	D0
XCH A,Rn	Exchange A and register	1	2	C8-CF
XCH A,dir	Exchange A and direct byte	2	4	C5
XCH A,@Ri	Exchange A and indirect memory	1	3	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	3	D6-D7

Table 42. Instruction Table (continued)

BOOLEAN				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	3	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	3	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	3	B2
ANL C,bit	AND direct bit to carry	2	3	82
ANL C,/bit	AND direct bit inverse to carry	2	3	B0
ORL C,bit	OR direct bit to carry	2	3	72
ORL C,/bit	OR direct bit inverse to carry	2	3	A0
MOV C,bit	Move direct bit to carry	2	3	A2
MOV bit,C	Move carry to direct bit	2	3	92
ACALL addr 11	Absolute jump to subroutine	2	4	11→F1
LCALL addr 16	Long jump to subroutine	3	2	12
RET	Return from subroutine	1	4	22
RETI	Return from interrupt	1	4	32
AJMP addr 11	Absolute jump unconditional	2	3	01→E1
LJMP addr 16	Long jump unconditional	3	4	02
SJMP rel	Short jump (relative address)	2	3	80
JC rel	Jump on carry = 1	2	3	40
JNC rel	Jump on carry = 0	2	3	50
JB bit,rel	Jump on direct bit = 1	3	5	20
JNB bit,rel	Jump on direct bit = 0	3	5	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	5	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	3	60
JNZ rel	Jump on accumulator ≠0	2	3	70

Table 42. Instruction Table (continued)

BOOLEAN				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
CJNE A,dir,rel	Compare A, direct jne relative	3	5	B5
CJNE A,#d,rel	Compare A, immediate jne relative	3	4	B4
CJNE Rn,#d,rel	Compare register, immediate jne relative	3	4	B8-BF
CJNE @Ri,#d,rel	Compare indirect, immediate jne relative	3	5	B6-B7
DJNZ Rn,rel	Decrement register, jnz relative	2	4	D8-DF
DJNZ dir,rel	Decrement direct byte, jnz relative	3	5	D5
NOP	No operation	1	1	00

NOTE: PUSH SP, POP SP, and DA instruction behave differently from 8051 operations. The use of this instruction only occurs when using the assembly language, and its use is very limited. Refer to “ERRATA_ABOV_94 CPU (CM8051) Incompatible Instruction” for more details.

In the above table, entries such as E8-EF indicate continuous blocks of hex opcodes used for 8 different registers. Register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as ‘11→F1’ (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the destination address.

CJNE instructions use abbreviation of #d for immediate data; other instructions use #data as an abbreviation.

Revision history

Date	Revision	Description
2019.12.17	1.00	1st creation
2020.02.04	1.01	Added the disclaimer and modified the distributor.
2021.05.20	1.02	Updated 16.1 Peripheral operation in IDLE/ STOP mode.
2022.04.19	1.03	Corrected the typos at Table 10. Interrupt Vector Address Table.
2022.11.02	1.04	Revised the font of this document

Korea

Regional Office, Seoul
R&D, Marketing & Sales
8th Fl., 330, Yeongdong-daero,
Gangnam-gu, Seoul,
06177, Korea

Tel: +82-2-2193-2200
Fax: +82-2-508-6903
http://www.abovsemi.com/

HQ, Ochang
R&D, QA, and Test Center
93, Gangni 1-gil, Ochang-eup,
Cheongwon-gun,
Chungcheongbuk-do,
28126, Korea

Tel: +82-43-219-5200
Fax: +82-43-217-3534
http://www.abovsemi.com/

Domestic Sales Manager
Tel: +82-2-2193-2206
Fax: +82-2-508-6903
Email: sales_kr@abov.co.kr

Global Sales Manager
Tel: +82-2-2193-2281
Fax: +82-2-508-6903
Email: sales_gl@abov.co.kr

China Sales Manager
Tel: +86-755-8287-2205
Fax: +86-755-8287-2204
Email: sales_cn@abov.co.kr