CMOS Single-chip 8-bit Microcontroller with 12-bit A/D Converter and LCD Driver

Main features

- **8-bit Microcontroller With High Speed 8051 CPU**
- **Basic MCU Function**
  - 48 Kbytes Flash Code Memory
  - 1280 bytes SRAM(IRAM 256 bytes + XRAM 1024 bytes)
- **Built-in Analog Function**
  - Power-On Reset and Low Voltage Detect Reset
  - Internal 8 MHz HFIRC Oscillator (±1.0%, T_A= -10 ~ +55°C, User trim)
  - Internal 32 kHz LFIRC Oscillator (±5.0%, T_A= -10 ~ +55°C)
  - Watchdog Timer RC Oscillator (5kHz)
- **Peripheral Features**
  - 12-bit Analog to Digital Converter (5 inputs)
  - LCD Driver (32 Segments x 8 Commons)
  - 16-bit CRC/Checksum Generator
  - Built-in Transistor for IR LED Drive
- **I/O and Packages**
  - 13 I/O, 46 Shared I/O with LCD signal
  - 64LQFP, 64QFN, 48LQFP, 48QFN
  - Pb-free package
- **Operating Conditions**
  - 1.8V to 5.5V Wide Voltage Range
  - -40°C to 85°C Temperature Range
- **Application**
  - Home appliance, Industrial Control

A96R739

Datasheet

Rev. 1.04

Revised 23 July, 2024

Revision history

Revision	Date	Revision list
1.0	2017.11.27	Published this book.
1.1	2018.04.27	Updated 64-Pin QFN-0909/48-Pin QFN-0707 package diagrams in Chapter 4. Package Diagram.
1.2	2018.09.07	Change Max and Min value of REM Output High Current in 7.11 DC Characteristics. Add Device Nomenclature. Add notes about External Interrupt register in Chapter 10.12.7 Register Description for Interrupt. More descriptions in Chapter 11.8.3 16-bit Capture Mode. Change Figure 11.31 16-Bit Capture Mode for Timer 3. Change Figure 11.34 16-Bit Timer 3 Block Diagram. Fix the typo.
1.3	2022.12.22	Modify a font
1.03	2023.05.08	Changed the format of the revision number to “X.YY” according to internal policy.
1.04	2024.07.23	Revised this book. Added the new pin assignment for 48LQFP(A96R739CK).

1 Overview

1.1 Description

The A96R739 is advanced CMOS 8-bit microcontroller with 48 Kbytes of FLASH. This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This provides the following features : 48 Kbytes of FLASH, 256 bytes of IRAM, 1024 bytes of XRAM, general purpose I/O, basic interval timer, watchdog timer, 8/16-bit timer/counter, carrier generation, watch timer, buzzer driving port, 12-bit A/D converter, LCD driver, 16-bit CRC/Checksum Generator, Built-in Transistor for I.R LED Drive, on-chip POR, LVR, LVI, on-chip oscillator and clock circuitry. The A96R739 also supports power down modes to reduce power consumption.

Device name	FLASH	IRAM	XRAM	ADC	I/O PORT	Package
A96R739RL	48 Kbytes	256 bytes	1024 bytes	5 inputs	59	64LQFP-1010
A96R739RU				5 inputs	59	64QFN-0909
A96R739CL				2 inputs	43	48LQFP-0707
A96R739CK				2 inputs	45	48LQFP-0707
A96R739CU				2 inputs	43	48QFN-0707

Table 1 Ordering Information of A96R739

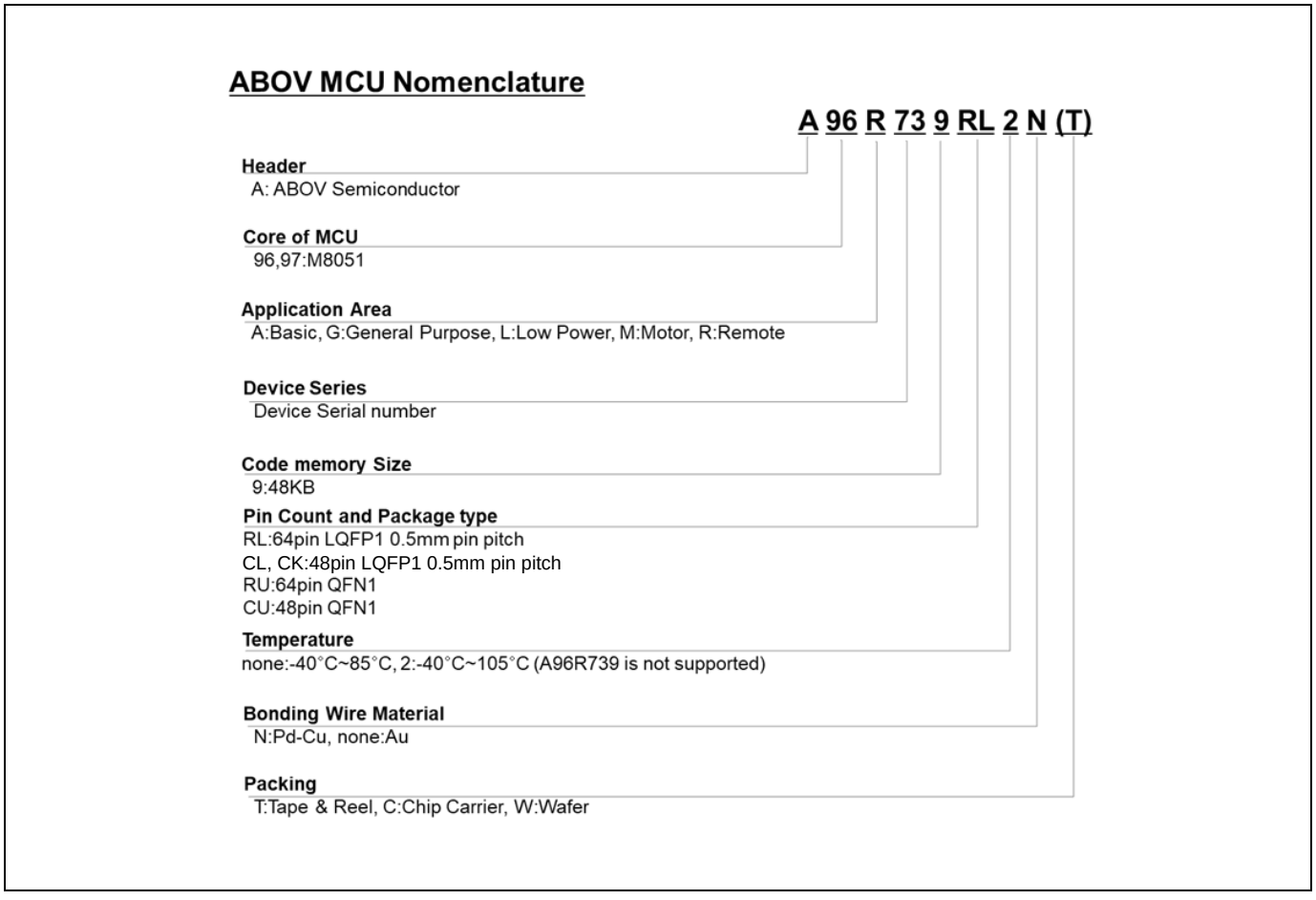


Figure 1 Device Nomenclature

1.2 Features

- **CPU**
  - 8-bit CISC core (M8051, 2 clocks per cycle)
- **ROM (FLASH) Capacity**
  - 48 Kbytes Flash with self read/write capability
  - On Chip debug and In-System Programming(ISP)
  - Endurance : 10,000 times(Sector 0~763)
    100,000 times(Sector 764~767)
  - Retention : 10 years
- **256 bytes IRAM**
- **1024 bytes XRAM**
  - 38 bytes including LCD display RAM
- **General Purpose I/O (GPIO)**
  - Normal I/O : 13 Ports
    (P4[7], P5[6:0], P6[4:0])
  - LCD shared I/O : 46 Ports
    (P0[7:0], P1[7:0], P2[7:0], P3[6:0], P4[6:0], P7[7:0])
- **Basic Interval Timer (BIT)**
  - 8-bit× 1-ch
- **Watch Dog Timer (WDT)**
  - 8-bit× 1-ch
  - 5kHz internal RC oscillator
- **Timer/Counter**
  - 8-bit× 2-ch(T0/T1), 16-bit× 2-ch (T2/T3)
  - 16-bit Interval Timer × 1ch
- **Carrier Generation**
  - Carrier generation (by T1), T3 Clock source
- **Programmable Pulse Generation**
  - Pulse generation (by T2/T3)
  - 8-Bit PWM (by T0)
- **Watch Timer (WT)**
  - 3.91ms/0.25s/0.5s/1s/1min interval at 32.768kHz
- **Buzzer**
  - 8-bit× 1-ch
- **UART**
  - 8-bit× 1-ch
- **12-bit A/D Converter**
  - 5 Input channels
- **LCD Driver**
  - 32 Segments and 8 Common
  - 1/2, 1/3, 1/4, 1/5, 1/6, 1/8 duty selectable
  - Voltage booster and 16-step contrast control
- **16-Bit CRC/Checksum Generator**
  - Auto and User CRC/Checksum mode
- **Built-in Transistor for I.R LED Drive**
  - IOL = 630mA at 3V and VOL = 1.0V
- **Power On Reset**
  - Reset release level (1.4V)
- **Low Voltage Reset**
  - 14 level detect (1.60/2.05/2.15/2.25/2.37/2.50/2.65/ 2.82/ 3.01/ 3.22/3.47/3.76/4.10/4.51V)
- **Low Current Low Voltage Reset**
  - 1.80V ± 90mV, 0.9uA Operating Current
- **Low Voltage Indicator**
  - 13 level detect (2.05/2.15/2.25/2.37/2.50/2.65/2.82/ 3.01/ 3.22/ 3.47/ 3.76/ 4.10/ 4.51V)
- **Interrupt Sources**
  - External Interrupts
    (EINT0 ~ EINT7, EINT10, EINT12, EINT13) (11)
  - Timer0/1/2/3 (5), Interval Timer (1)
  - WDT (1), BIT (1), WT (1)
  - ADC (1), UART (2), LVI (1)
- **Internal RC Oscillator**
  - HFIRC frequency:
    8MHz ±1.0% (T_A= -10 ~ +55°C, User trim)
  - LFIRC frequency:
    32kHz ±5.0% (T_A= -10 ~ +55°C)
- **Power Down Mode**
  - STOP, IDLE mode
- **Operating Voltage and Frequency**
  - 1.8V ~ 5.5V (@ 32 ~ 38kHz with SX-tal)
  - 2.0V ~ 5.5V (@ 0.4 ~ 4.2MHz with X-tal, Crystal)
  - 1.8V ~ 5.5V (@ 0.4 ~ 4.2MHz with X-tal, Ceramic)
  - 2.4V ~ 5.5V (@ 0.4 ~ 8.0MHz with X-tal)
  - 3.0V ~ 5.5V (@ 0.4 ~ 12.0MHz with X-tal)
  - 1.8V ~ 5.5V (@ 0.5MHz ~ 8MHz with HFIRC)
  - 1.8V ~ 5.5V (@ 4kHz ~ 32kHz with LFIRC)
  - Voltage dropout converter included for core
- **Minimum Instruction Execution Time**
  - 167ns (@12MHz main clock)
  - 61us (@ 32.768kHz sub clock)
- **Operating Temperature**
  - –40 ~ +85℃
- **Oscillator Type**
  - 0.4-12MHz Crystal or Ceramic for main clock
  - 32.768kHz Crystal for sub clock
- **Package Type**
  - 64-Pin LQFP-1010/48-Pin LQFP-0707
  - 64-Pin QFN-0909/48-Pin QFN-0707
  - Pb-free package

1.3 Development tools

1.3.1 Compiler

We do not provide the compiler. Please contact the third parties.

The core of A96R739 is Mentor 8051. And, device ROM size is smaller than 64k bytes. Developer can use all kinds of third party's standard 8051 compiler.

1.3.2 OCD(On-chip debugger) emulator and debugger

The OCD (On Chip Debug) emulator supports ABOV Semiconductor's 8051 series MCU emulation.

The OCD interface uses two-wire interfacing between PC and MCU which is attached to user's system. The OCD can read or change the value of MCU internal memory and I/O peripherals. And the OCD also controls MCU internal debugging logic, it means OCD controls emulation, step run, monitoring, etc.

The OCD Debugger program works on all Microsoft-Windows operating system.

If you want to see more details, please refer to OCD debugger manual. You can download debugger S/W and manual from our web-site(www.abovsemi.com).

Connection:

- DSCL (A96R739 P33 port)
- DSDA (A96R739 P32 port)

OCD connector diagram: Connect OCD with user system

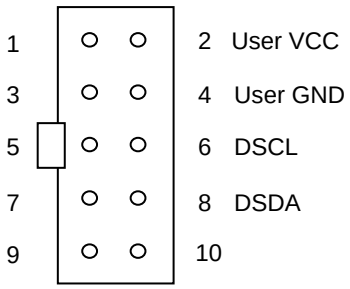


Figure 2 Debugger(OCD1/OCD2) and Pin description

1.3.3 Programmer

Single programmer :

E-PGM+ : It programs MCU device directly.

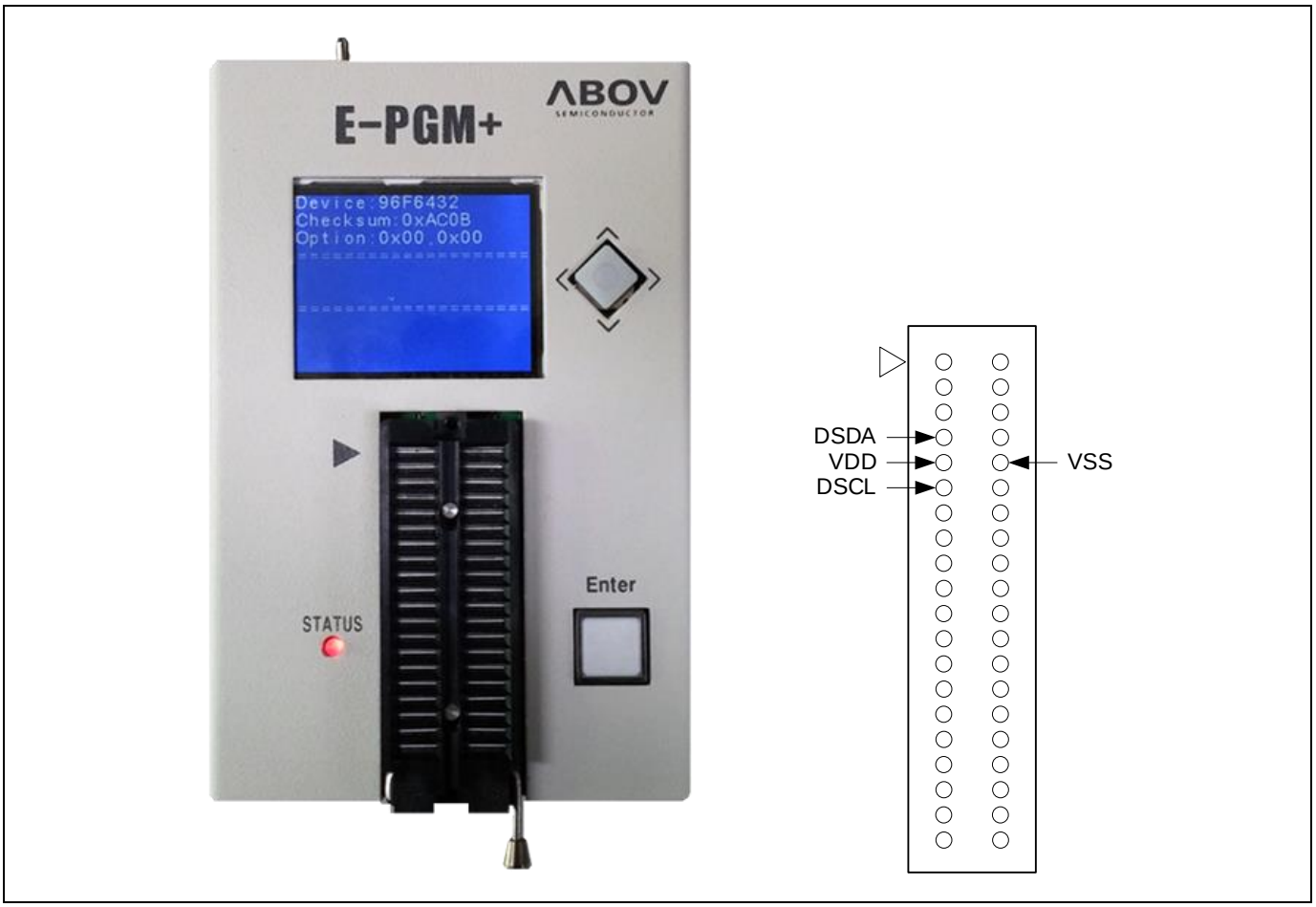


Figure 3 E-PGM+(Single writer)

OCD emulator:

It can write code to MCU device too, because OCD debugger supports ISP (In System Programming).It does not require additional H/W, except developer's target system.

Gang programmer: E-GANG4 and E-GANG6

- It can run PC controlled mode.
- It can run standalone without PC control too.
- USB interface is supported.
- Easy to connect to the handler.

Figure 4 E-GANG4 and E-GANG6 (for Mass Production)

1.4 MTP programming

1.4.1 Overview

The program memory of A96R739 is MTP Type. This flash is accessed by serial data format. There are four pins(DSCL, DSDA, VDD, VSS) for programming/reading the flash.

Pin name	Main chip pin name	During programming	
		I/O	Description
DSCL	P33	I	Serial clock pin. Input only pin.
DSDA	P32	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	-	Logic power supply pin.

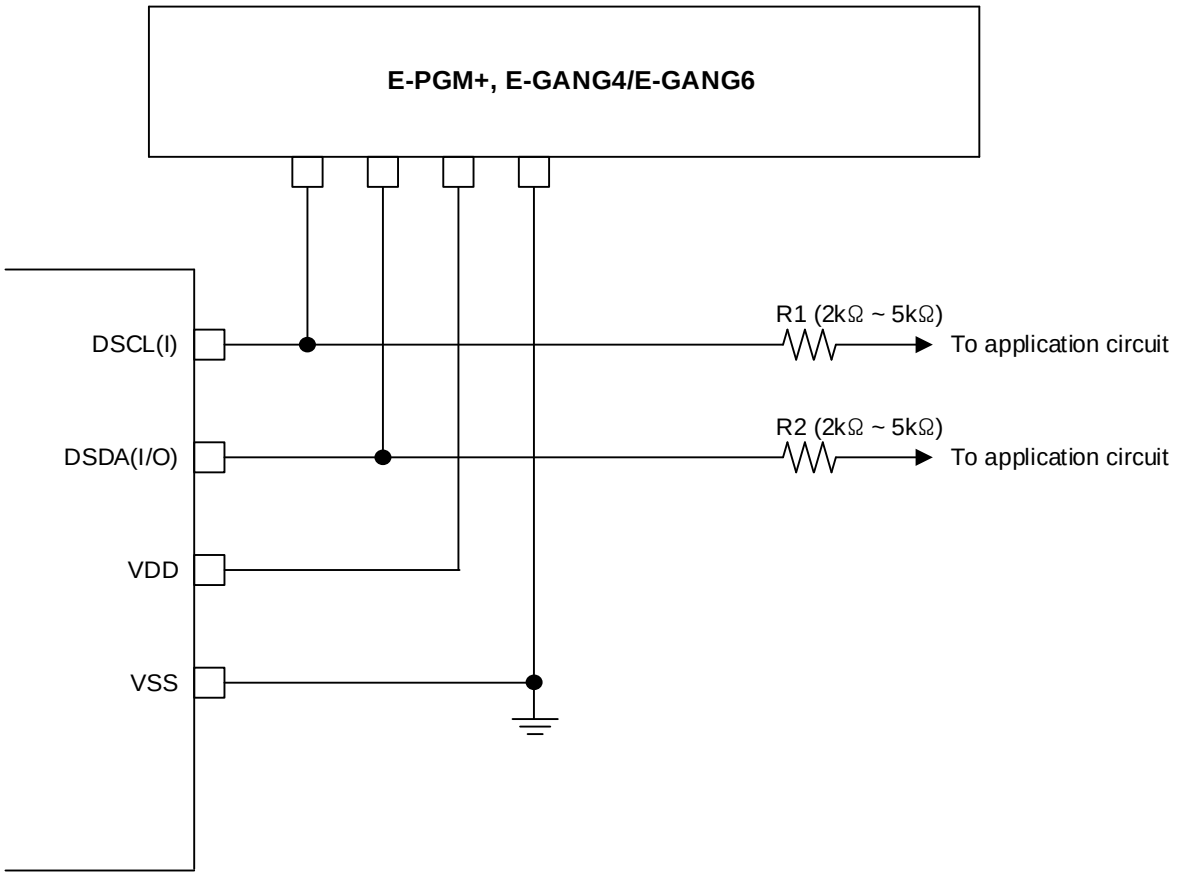
Table 2 Descriptions of pins which are used to programming/reading the Flash

1.4.2 On-Board programming

The A96R739 needs only four signal lines including VDD and VSS pins for programming FLASH with serial protocol. Therefore the on-board programming is possible if the programming signal lines are considered when the PCB of application board is designed.

1.4.3 Circuit Design Guide

At the FLASH programming, the programming tool needs 4 signal lines that are DSCL, DSDA, VDD and VSS. When you design the PCB circuits, you should consider the usage of these signal lines for the on-board programming. Please be careful to design the related circuit of these signal pins because rising/falling timing of DSCL and DSDA is very important for proper programming.



NOTE)

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1 and R2 is recommended value. It varies with circuit of system.

Figure 5 PCB design guide for on board programming

2 Block diagram

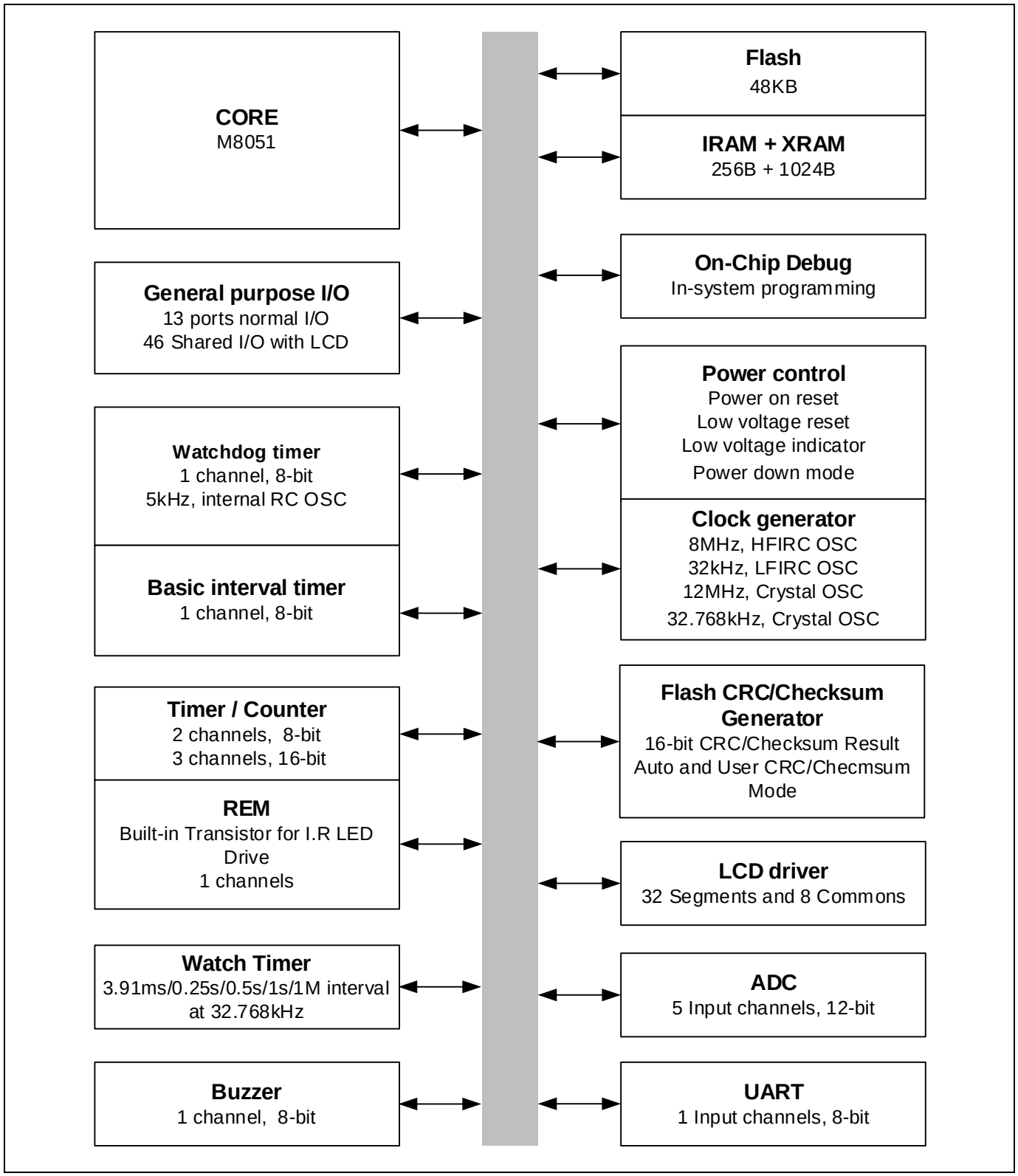
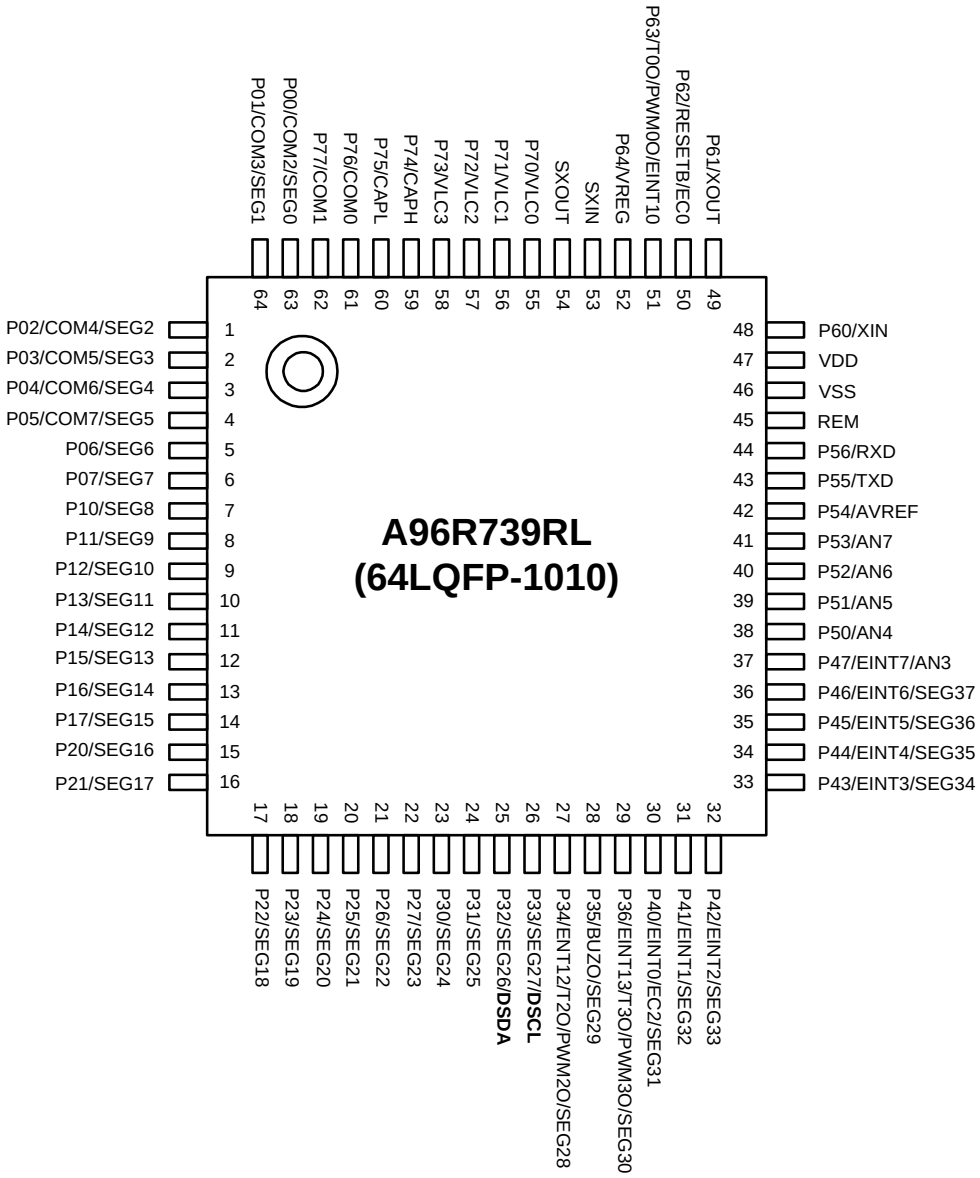


Figure 6 Block diagram of A96R739

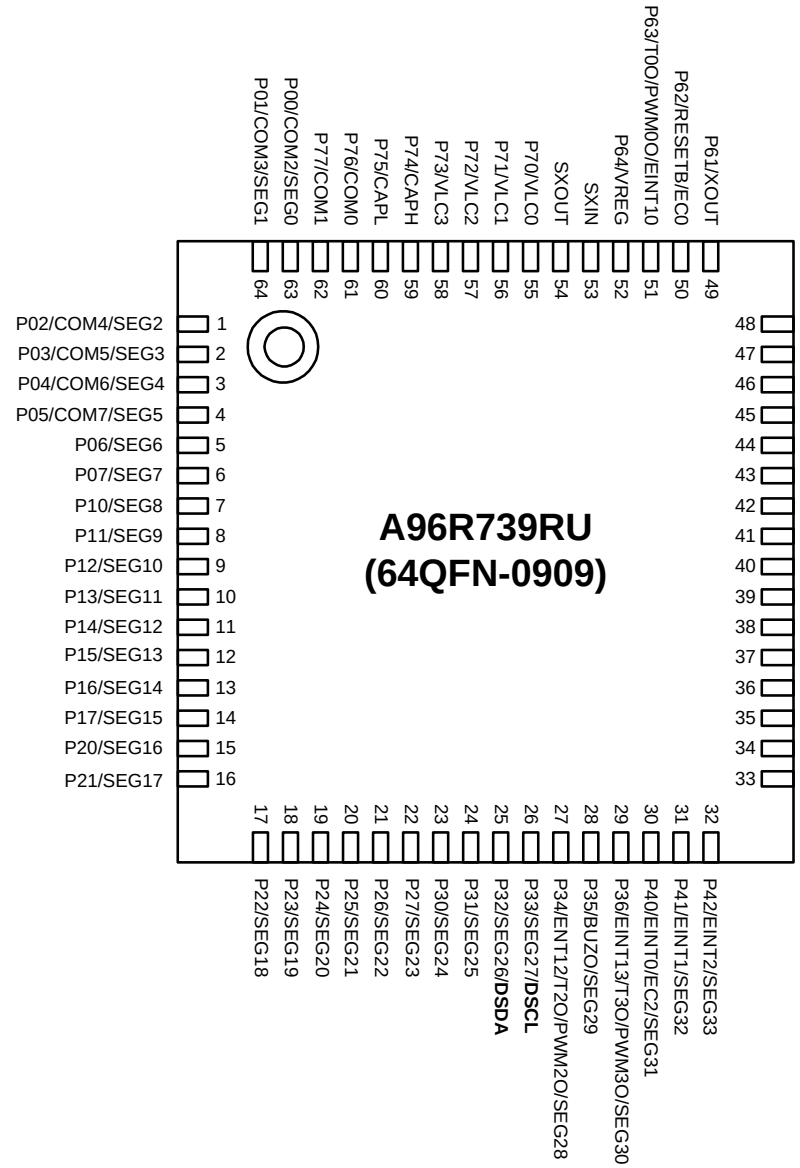
3 Pin assignment



NOTE)

1. On On-Chip Debugging, ISP uses P3[3:2] pin as DSCL, DSDA.

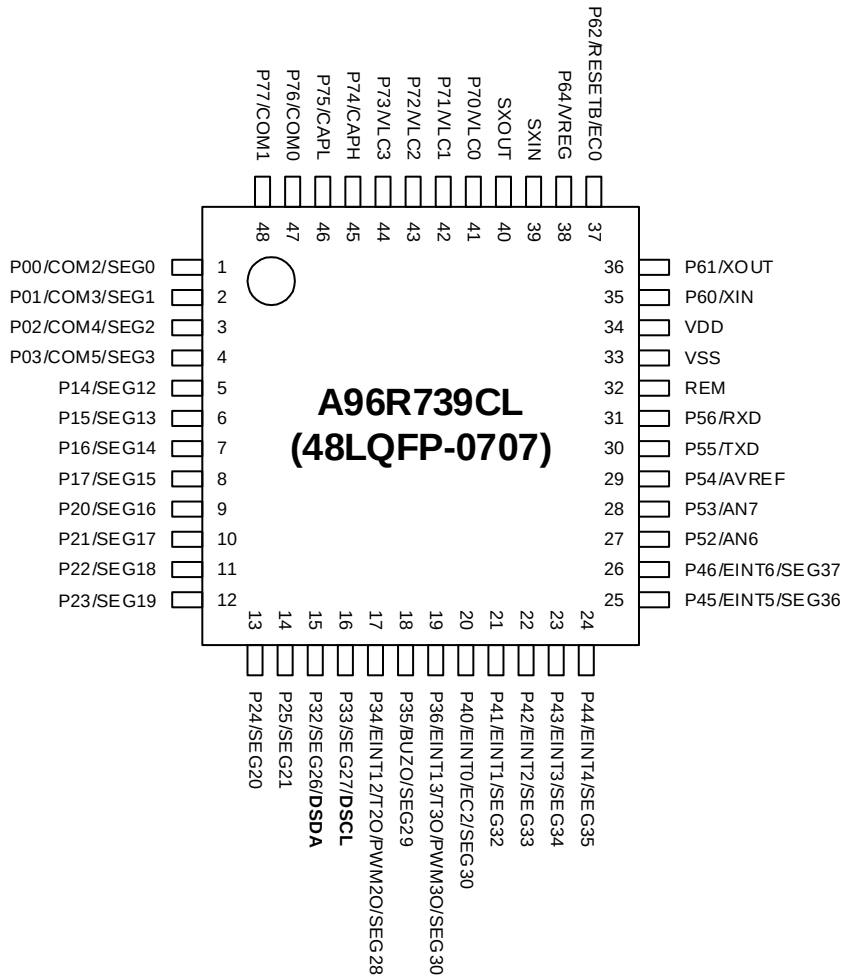
Figure 7 A96R739RL 64LQFP Pin Assignment



NOTE)

1. On On-Chip Debugging, ISP uses P3[3:2] pin as DSCL, DSDA.

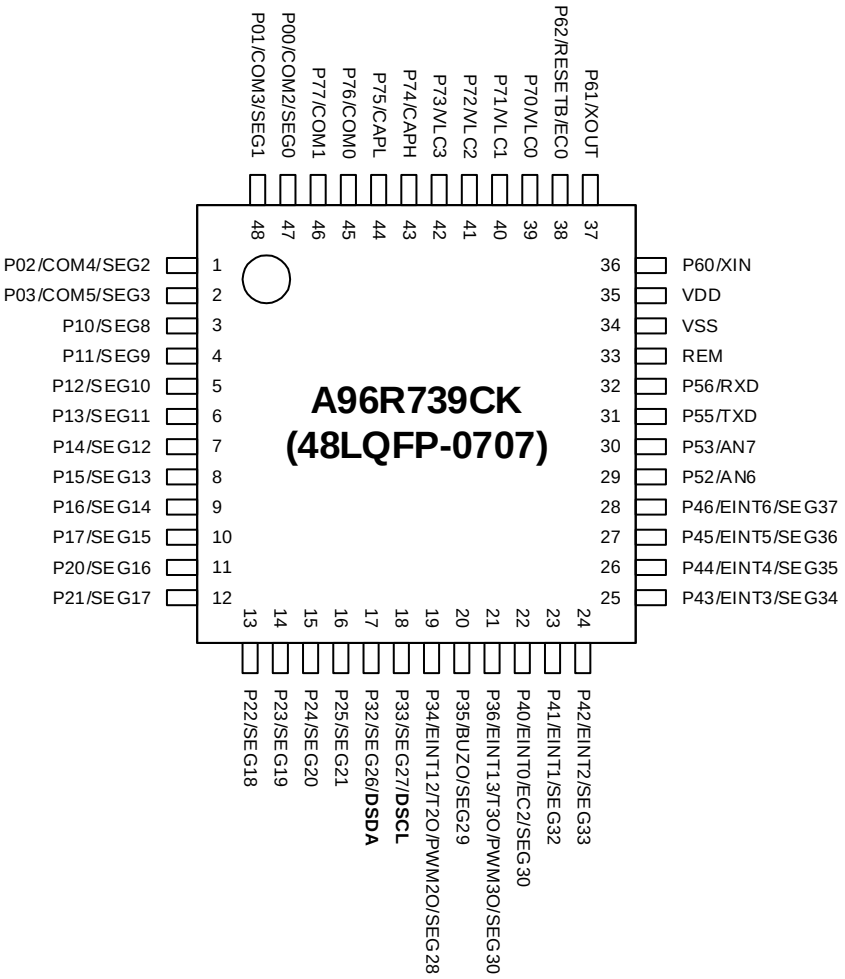
Figure 8 A96R739RU 64QFN Pin Assignment



NOTE)

1. On On-Chip Debugging, ISP uses P3[3:2] pin as DSCL, DSDA.
2. The P04-P07, P10-P13, P26-P27, P30-P31, P47, P50-P51 and P63 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 48-pin package(A96R739CL) is used.

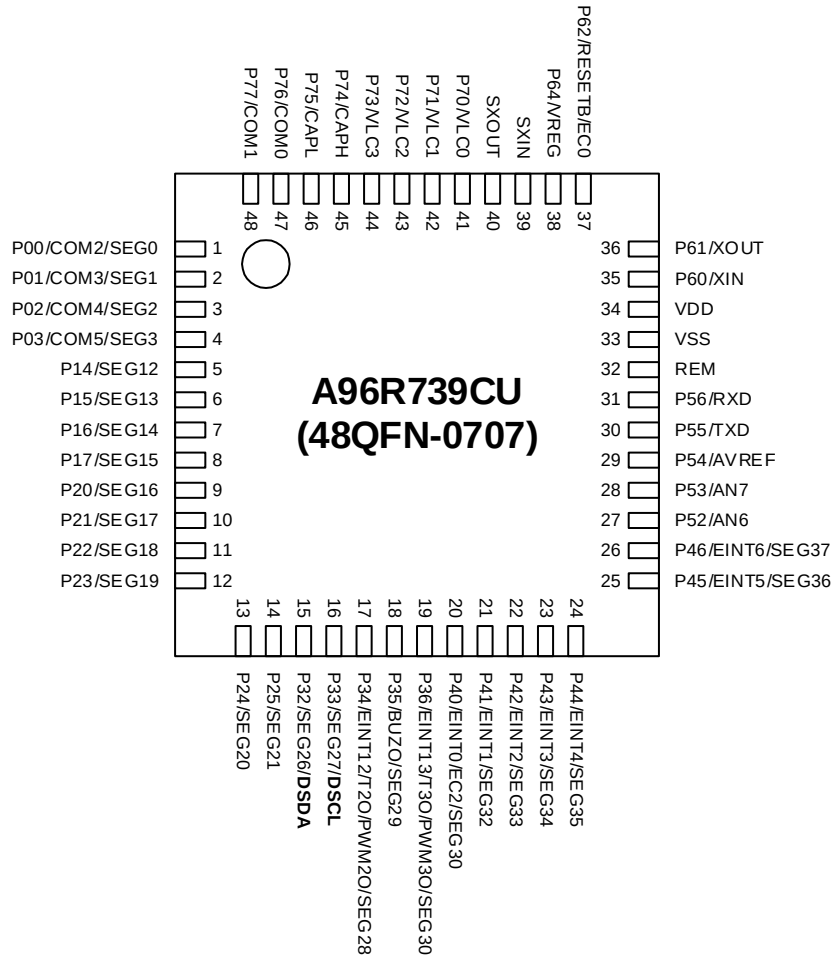
Figure 9 A96R739CL 48LQFP Pin Assignment



NOTE)

1. On On-Chip Debugging, ISP uses P3[3:2] pin as DSCL, DSDA.
2. The P04-P07, P26-P27, P30-P31, P47, P50-P51, P54 and P63-P64 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 48-pin package(A96R739CK) is used.

Figure 10 A96R739CK 48LQFP Pin Assignment



NOTE)

1. On On-Chip Debugging, ISP uses P3[3:2] pin as DSCL, DSDA.
2. The P04-P07, P10-P13, P26-P27, P30-P31, P47, P50-P51 and P63 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 48-pin package(A96R739CU) is used.

Figure 11 A96R739CU 48QFN Pin Assignment

4 Package Diagram

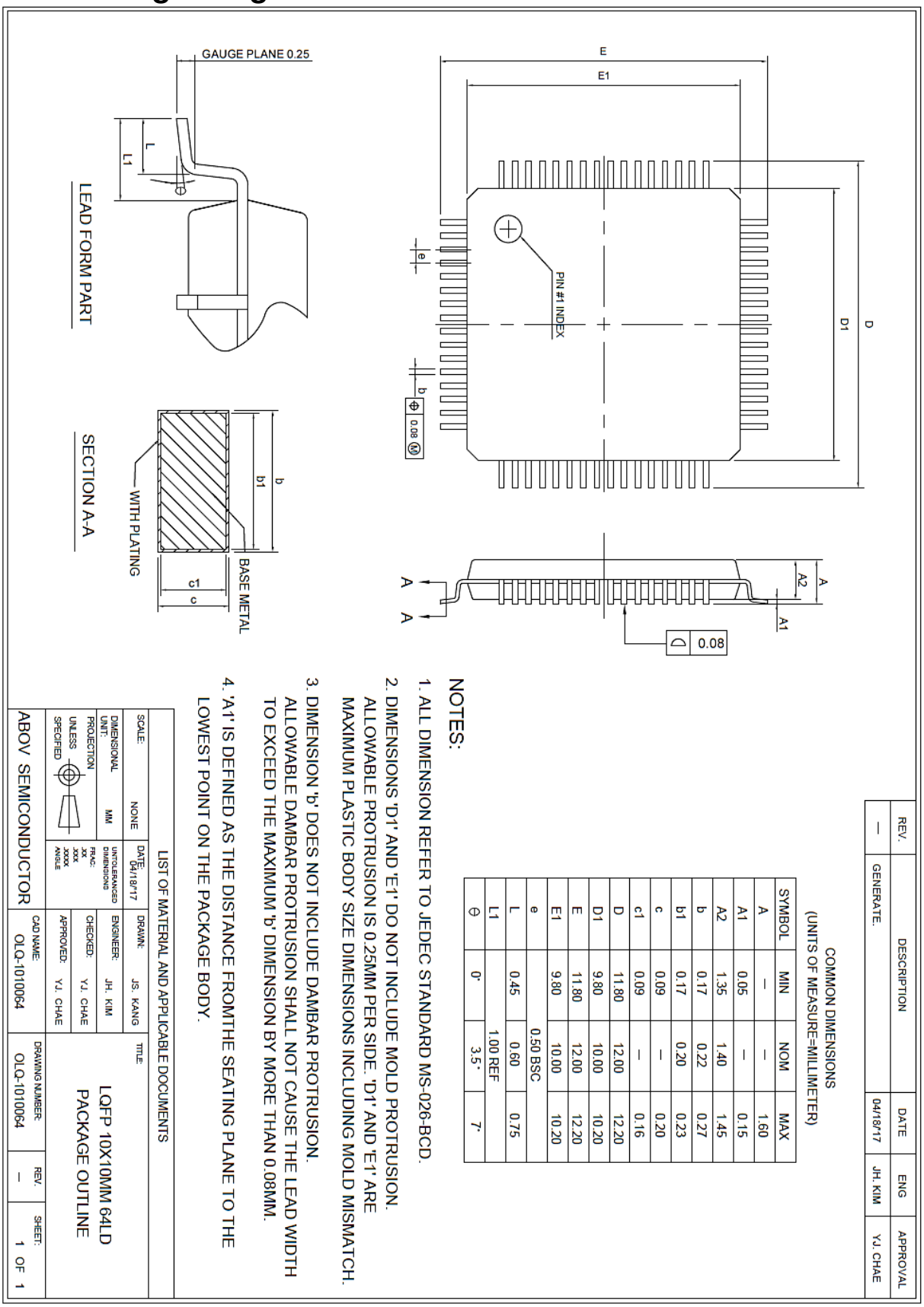
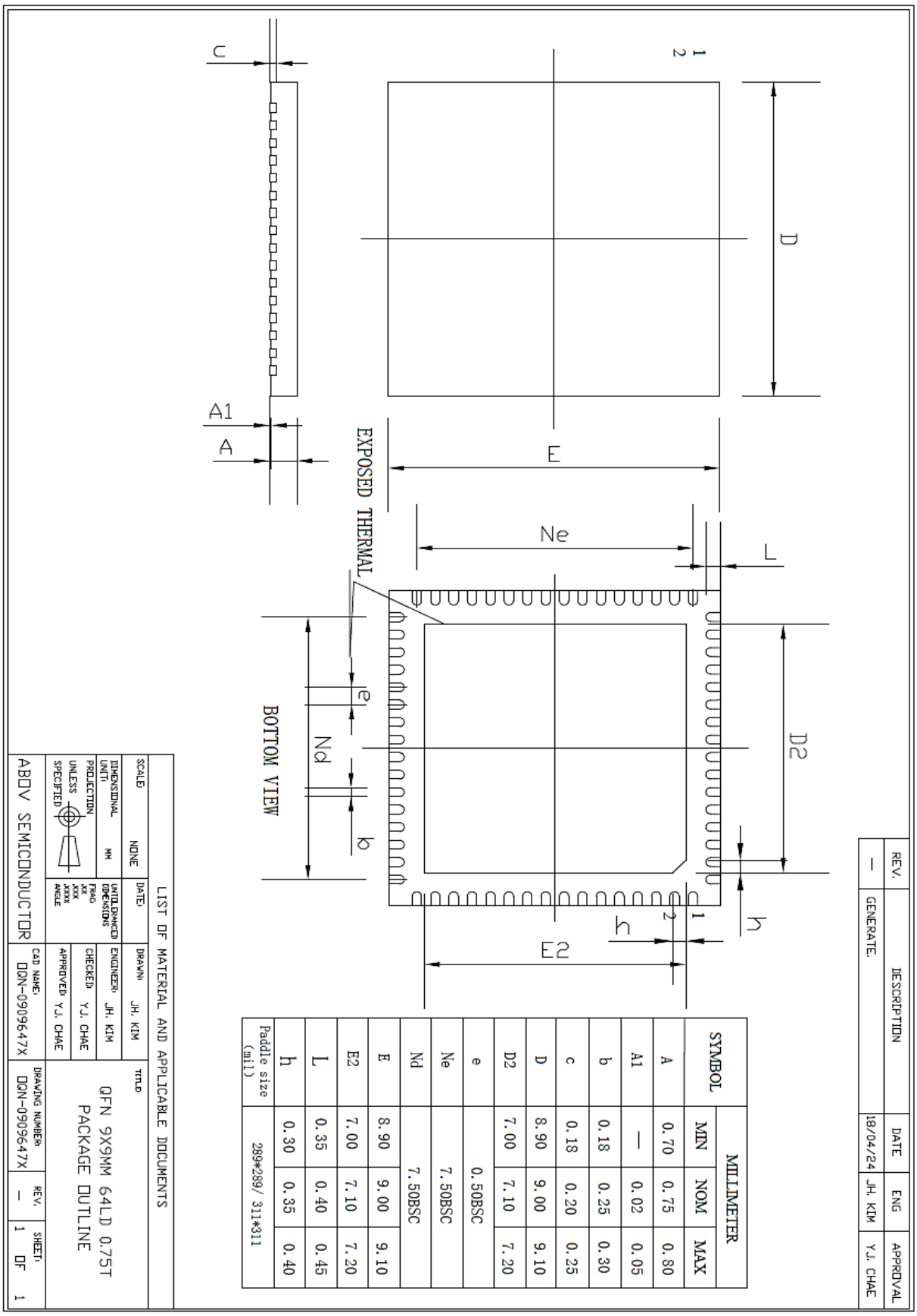


Figure 12 64-Pin LQFP-1010 Package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	8.90	9.00	9.10
D2	7.00	7.10	7.20
e	0.50BSC		
Ne	7.50BSC		
Nd	7.50BSC		
E	8.90	9.00	9.10
E2	7.00	7.10	7.20
L	0.35	0.40	0.45
h	0.30	0.35	0.40
Paddle size (mil)	289*289/ 311*311		

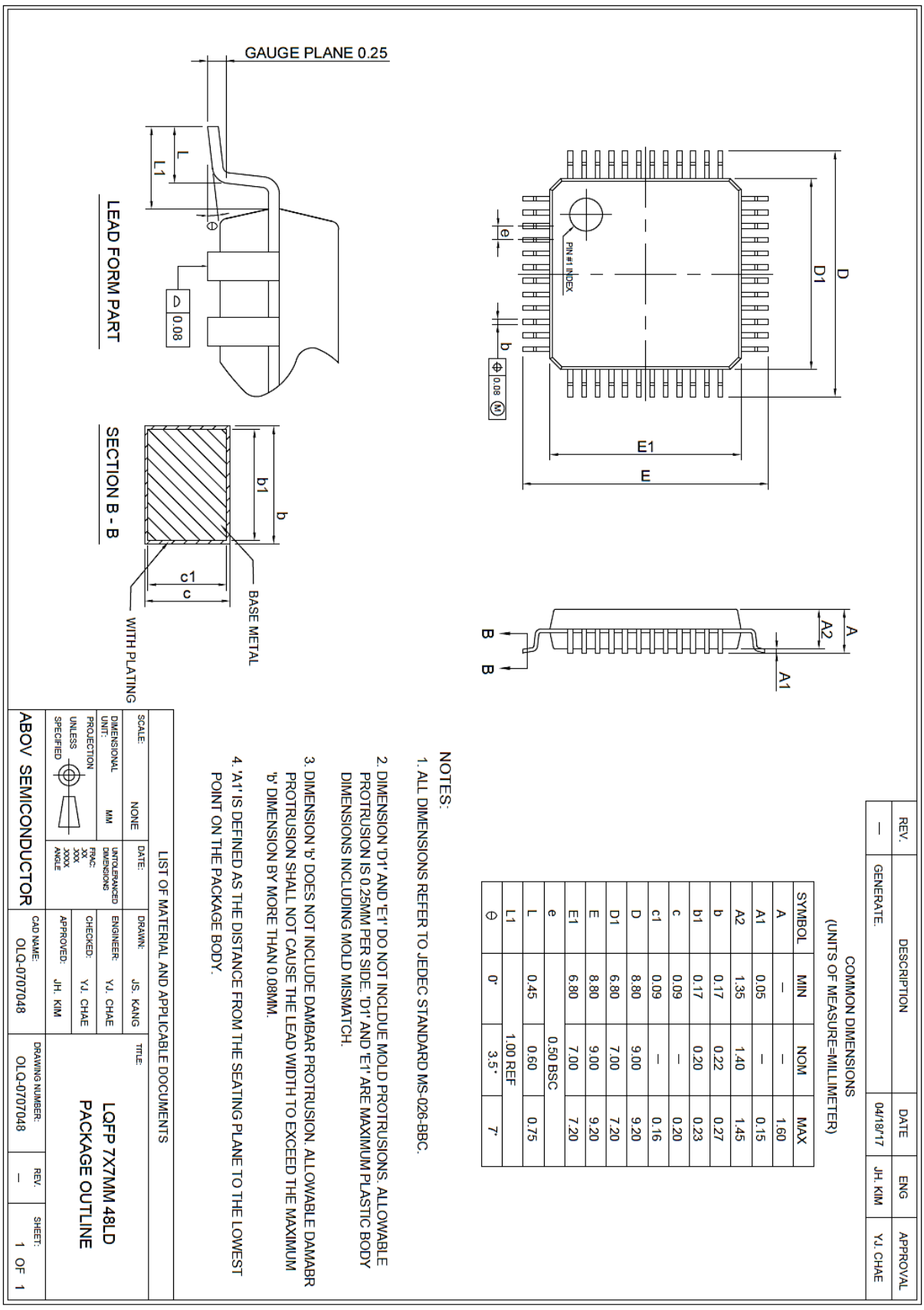
REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	18/04/24	JH. KIM	YJ. CHAE

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE
DIMENSIONAL UNIT: MM
PROJECTION
UNLESS SPECIFIED
UNTOLERANCED DIMENSIONS: FRAC XX XXX XXXX ANGLE
DATE:
ENGINEER: JH. KIM
CHECKED: YJ. CHAE
APPROVED: YJ. CHAE
DRAWN: JH. KIM
TITLE: QFN 9X9MM 64LD 0.75T PACKAGE OUTLINE
CAD NAME: DQN-0909647X
DRAWING NUMBER: DQN-0909647X
REV.: —
SHEET: 1 OF 1

ABOV SEMICONDUCTOR

Figure 13 64-Pin QFN-0909 Package



REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/18/17	JH. KIM	YJ. CHAE

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e		0.50 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026-BBC.
2. DIMENSION 'D1' AND 'E1' DO NOT INCLDUE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. 'D1' AND 'E1' ARE MAXIMUM PLASTIC BODY DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMABR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 'b' DIMENSION BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE:	DRAWN: JS. KANG	TITLE: LQFP 7X7MM 48LD PACKAGE OUTLINE	
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS	ENGINEER: YJ. CHAE		
PROJECTION	FRAC: XX ±XX .XXX ±XXX ANGLE	CHECKED: YJ. CHAE		
UNLESS SPECIFIED:		APPROVED: JH. KIM		
ABOV SEMICONDUCTOR	CAD NAME: OLQ-0707048	DRAWING NUMBER: OLQ-0707048	REV: —	SHEET: 1 OF 1

Figure 14 48-Pin LQFP-0707 Package

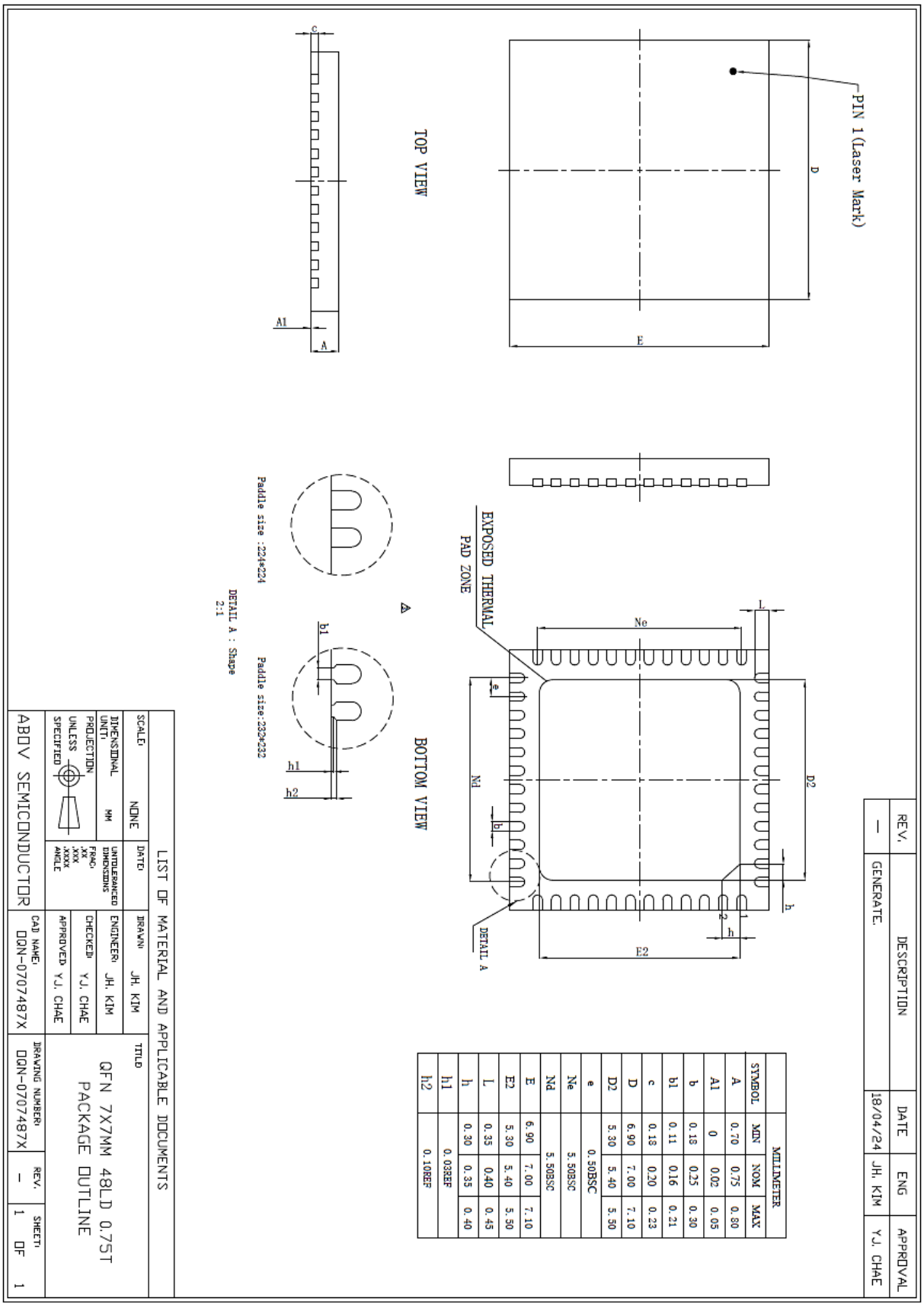


Figure 15 48-Pin QFN-0707 Package

5 Pin Description

PIN name	I/O	Function	@RESET	Shared with
P00	I/O	Port 0 is a bit-programmable I/O port which can be configured as an input, a push-pull output or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P04–P07 are not in the A96R739CL/CK/CU package.	Input	COM2/SEG0
P01				COM3/SEG1
P02				COM4/SEG2
P03				COM5/SEG3
P04				COM6/SEG4
P05				COM7/SEG5
P06				SEG6
P07				SEG7
P10	I/O	Port 1 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P10–P13 are not in the A96R739CL/CU package.	Input	SEG8
P11				SEG9
P12				SEG10
P13				SEG11
P14				SEG12
P15				SEG13
P16				SEG14
P17				SEG15
P20	I/O	Port 2 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P26–P27 are not in the A96R739CL/CK/CU package.	Input	SEG16
P21				SEG17
P22				SEG18
P23				SEG19
P24				SEG20
P25				SEG21
P26				SEG22
P27				SEG23
P30	I/O	Port 3 is a bit-programmable I/O port which can be configured as an input (P32 – P36: Schmitt trigger input), a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P30–P31 are not in the A96R739CL/CK/CU package.	Input	SEG24
P31				SEG25
P32				SEG26/DSDA
P33				SEG27/DSCL
P34				ENIT12/T2O/PWM2O/SEG28
P35				BUZO/SEG29
P36				EINT13/T3O/PWM3O/SEG30
P40	I/O	Port 4 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P47 is not in the A96R739CL/CK/CU package.	Input	EINT0/EC2/SEG31
P41				EINT1/SEG32
P42				EINT2/SEG33
P43				EINT3/SEG34
P44				EINT4/SEG35
P45				EINT5/SEG36
P46				EINT6/SEG37
P47				EINT7/AN3

Table 3 Normal Pin Description

PIN name	I/O	Function	@RESET	Shared with
P50	I/O	Port 5 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P50–P51 are not in the A96R739CL/CU package. The P50–P51 and P54 are not in the A96R739CK package.	Input	AN4
P51				AN5
P52				AN6
P53				AN7
P54				AVREF
P55				TXD
P56				RXD
P60	I/O	Port 6 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P63 is not in the A96R739CL/CU package. The P63-P64 are not in the A96R739CK package.	Input	XIN
P61				XOUT
P62				RESETB/EC0
P63				T0O/PWM0O/ENT10
P64				VREG
P70	I/O	Port 7 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	VLC0
P71				VLC1
P72				VLC2
P73				VLC3
P74				CAPL
P75				CAPH
P76				COM0
P77				COM1
EINT10	I/O	External interrupt and Timer 0 capture input	Input	P63/T0O/PWM0O
EINT12	I/O	External interrupt and Timer 2 capture input	Input	P34/T2O/PWM2O/SEG28
EINT13	I/O	External interrupt and Timer 3 capture input	Input	P36/T3O/PWM3O/SEG30
EINT0	I/O	External interrupt inputs	Input	P40/EC2/SEG31
EINT1				P41/SEG32
EINT2				P42/SEG33
EINT3				P43/SEG34
EINT4				P44/SEG35
EINT5				P45/SEG36
EINT6				P46/SEG37
EINT7				P47/AN3
T0O	I/O	Timer 0 interval output	Input	P63/PWM0O/EINT10
T2O	I/O	Timer 2 interval output	Input	P34/PWM2O/ENIT12/SEG28
T3O	I/O	Timer 3 interval output	Input	P36/PWM3O/ENIT13/SEG30
PWM0O	I/O	Timer 0 PWM output	Input	P63/T0O/EINT10
PWM2O	I/O	Timer 2 pulse output	Input	P34/T2O/ENT12/SEG28
PWM3O	I/O	Timer 3 pulse output	Input	P36/T3O/ENT13/SEG30
EC0	I/O	Timer 0 event count input	Input	P62/RESETB
EC2	I/O	Timer 2 event count input	Input	P40/EINT0/SEG31
REM	O	High current n-channel open-drain output for driving I.R. LED.	Output	–
BUZO	I/O	Buzzer signal output	Input	P35/SEG29
TXD	I/O	UART data output	Input	P55
RXD	I/O	UART data input	Input	P56

Table 3. Normal Pin Description (Continued)

PIN name	I/O	Function	@RESET	Shared with
AN3	I/O	A/D converter analog input channels	Input	P47/EINT7
AN4				P50
AN5				P51
AN6				P52
AN7				P53
VLC0–VLC3	I/O	LCD bias voltage pins	Input	P70–P73
CAPH	I/O	Capacitor terminals for voltage booster	Input	P74
CAPL			Input	P75
COM0	I/O	LCD common signal outputs	Input	P76
COM1				P77
COM2				P00/SEG0
COM3				P01/SEG1
COM4				P02/SEG2
COM5				P03/SEG3
COM6				P04/SEG4
COM7				P05/SEG5
SEG0	I/O	LCD segment signal outputs	Input	P00/COM2
SEG1				P01/COM3
SEG2				P02/COM4
SEG3				P03/COM5
SEG4				P04/COM6
SEG5				P05/COM7
SEG6				P06
SEG7				P07
SEG8–SEG15				P10–P17
SEG16–SEG23				P20–P27
SEG24				P30
SEG25				P31
SEG26				P32/DSDA
SEG27				P33/DSCL
SEG28				P34/EINT12/T2O/PWM2O
SEG29				P35/BUZO
SEG30				P36/EINT13/T3O/PWM3O
SEG31				P40/EINT0/EC2
SEG32				P41/EINT1
SEG33				P42/EINT2
SEG34				P43/EINT3
SEG35				P44/EINT4
SEG36				P45/EINT5
SEG37				P46/EINT6

Table 3. Normal Pin Description (Continued)

PIN name	I/O	Function	@RESET	Shared with
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by “CONFIGURE OPTION”	Input	P62/EC0
DSDA	I/O	On chip debugger data input/output	Input	P32/SEG26
DSCL	I/O	On chip debugger clock input	Input	P33/SEG27
XIN	I/O	Main oscillator pins	Input	P60
XOUT				P61
SXIN, SXOUT	I/O	Sub oscillator pins	Input	–
VREG	I/O	Regulator voltage output for sub clock. 0.1uF capacitor needed.	Input	P64
AVREF	I/O	A/D converter reference voltage	Input	P54
VDD, VSS	–	Power input pins	–	–

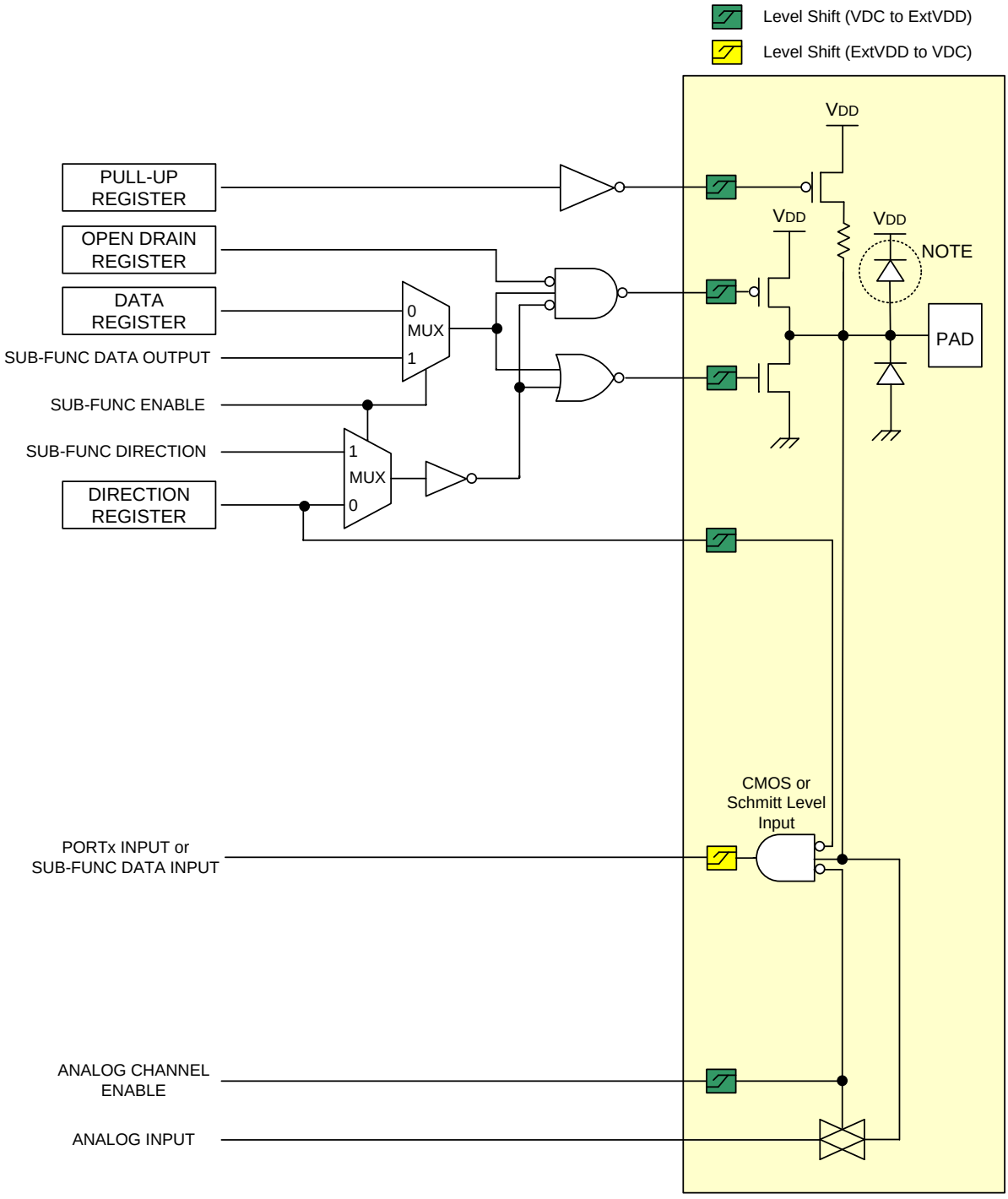
Table 3. Normal Pin Description (Concluded)

NOTE)

1. The P62/RESETB/EC0 pin is configured as one of the P62/EC0 and the RESETB pin by the “CONFIGURE OPTION”.
2. If the P32/SEG26/DSDA and P33/SEG27/DSCL pins are connected to an emulator during reset or power-on reset, the pins are automatically configured as the debugger pins.
3. The P32/SEG26/DSDA and P33/SEG27/DSCL pins are configured as inputs with an internal pull-up resistor only during the reset or power-on reset.
4. The P60/XIN and P61/XOUT pins are configured as a function pin by software control.
5. The P64/VREG pins are configured as a function pin by software control.
6. The P64/VREG pin should be configured as a VREG alternative function if a sub oscillator is used.
7. The P04-P07, P10-P13, P26-P27, P30-P31, P47, P50-P51 and P63 are not in the 48-pin package (A96R739CL/A96R739CU).
8. The P04-P07, P26-P27, P30-P31, P47, P50-P51, P54 and P63-P64 are not in the 48-pin package (A96R739CK).

6 Port Structures

6.1 General Purpose I/O Port

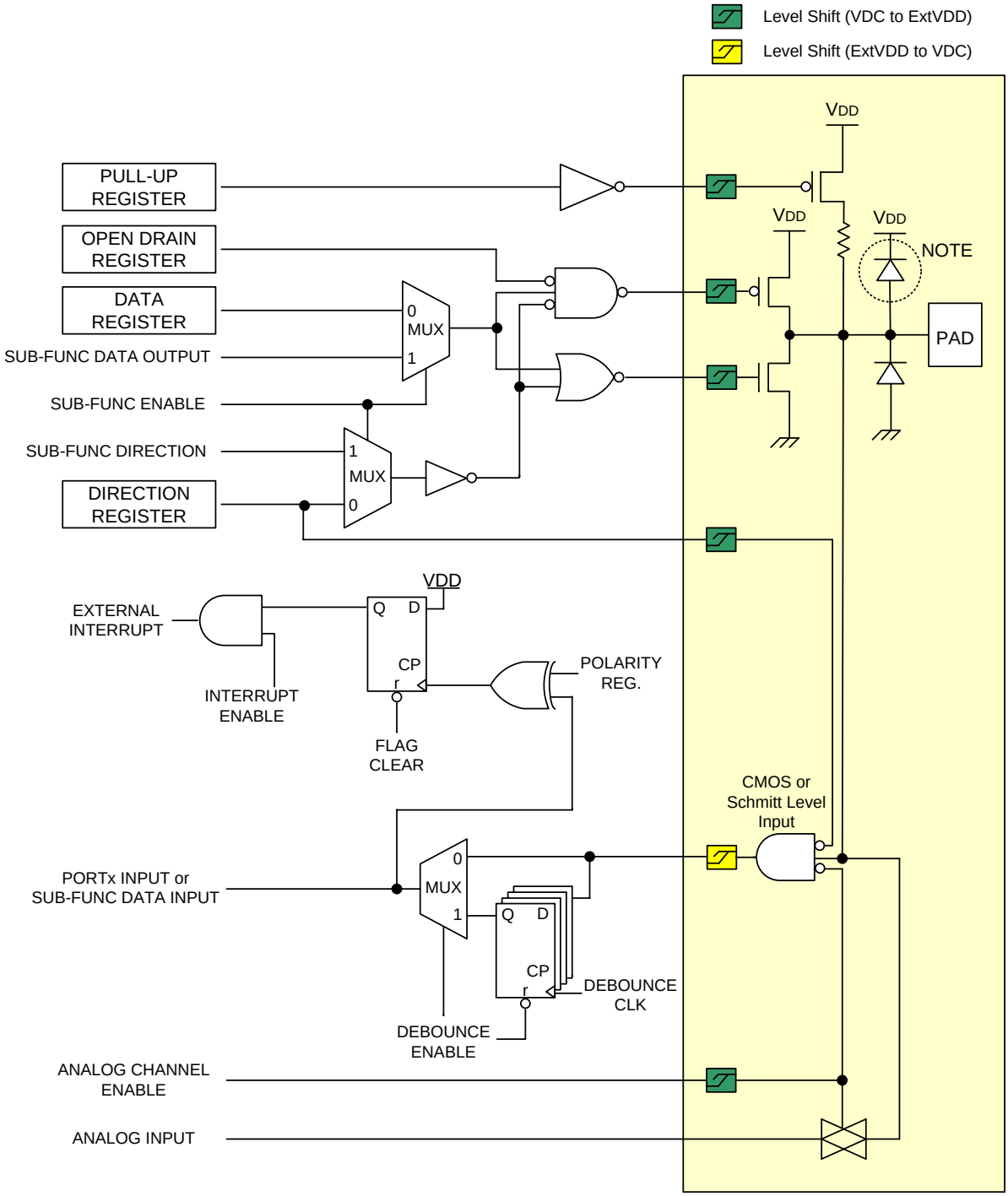


NOTE)

1. The P00-P07, P10-P17, P20-P27, P30–P36, P40-P46 and P70-P77 pins(COM, SEG, VLC, CAPH/L) do not have diode between VDD and PAD.

Figure 16 General Purpose I/O Port

6.2 External Interrupt I/O Port



NOTE)

1. The P00-P07, P10-P17, P20-P27, P30–P36, P40-P46 and P70-P77 pins(COM, SEG, VLC, CAPH/L) do not have diode between VDD and PAD.

Figure 17 External Interrupt I/O Port

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Supply Voltage	VDD	-0.3 – +6.5	V	–
Normal Pin	V_I	-0.3 – VDD+0.3	V	Voltage on any pin with respect to Vss
	V_O	-0.3 – VDD+0.3	V	
	I_{OH}	-10	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	ΣI_{OH}	-80	mA	Maximum current (ΣI_{OH})
	I_{OL}	60	mA	Maximum current sunk by (I_{OL} per I/O pin)
	ΣI_{OL}	120	mA	Maximum current (ΣI_{OL})
REM Output Pin	I_{OL}	800	mA	Maximum current sunk by REM pin
Total Power Dissipation	P_T	600	mW	–
Storage Temperature	T_{STG}	-65 – +150	°C	–

Table 4 Absolute Maximum Ratings

NOTE)

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

(T_A=-40°C ~ +85°C)

Parameter	Symbol	Conditions			Min	Max	Units
Operating Voltage	VDD	fx = 32 – 38kHz	SX-tal		1.8	5.5	V
		fx = 0.4 – 4.2MHz	X-tal	Ceramic	1.8	5.5	
				Crystal	2.0	5.5	
		fx = 0.4 – 8MHz	X-tal		2.4	5.5	
		fx = 0.4 – 12MHz			3.0	5.5	
		fx = 0.5 – 8MHz	HFIRC		1.8	5.5	
		fx = 4.0 – 32kHz	LFIRC		1.8	5.5	
Operating Temperature	T_{OPR}	VDD = 1.8 – 5.5V			-40	85	°C

Table 5 Recommended Operating Conditions

7.3 A/D Converter Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Resolution	–	–		–	12	–	bit
Integral Non-Linear	INL	AVREF=2.7V – 5.5V, fx=8MHz		–	–	±6	LSB
Differential Non-Linearity	DNL			–	–	±1	
Top Offset Error	TOE			–	–	±5	
Zero Offset Error	ZOE			–	–	±5	
Conversion Time	t_{CONV}	AVREF=4.0V – 5.5V		20	–	–	us
		AVREF=3.0V – 5.5V		30	–	–	
		AVREF=2.7V – 5.5V		60	–	–	
Analog Input Voltage	V_{AIN}	–		VSS	–	AVREF	V
Analog Reference Voltage	AVREF	–		1.8	–	VDD	
Band Gap Reference Value(4)	VAL_{BGR}	VDD=3.3V, TA=25°C, MSB align, 8 times average(5), Internal Reference (REFSEL=0), Different from CNFMRR0/1 values and ADC result (“CNFMRR0/1” – “ADC result”)		–	–	±50	LSB
A/DC Input Leakage Current	I_{AIN}	AVREF=5.12V		–	–	10	uA
A/DC Current	I_{ADC}	Enable	VDD=5.12V	–	1	2	mA
		Disable		–	–	0.1	uA

Table 6 A/D Converter Characteristics

NOTE)

1. Zero offset error is the difference between 000000000000 and the converted output for zero input voltage (VSS).
2. Top offset error is the difference between 111111111111 and the converted output for top input voltage (AVREF).
3. If AVREF is less than 2.7V, the resolution degrades by 1-bit whenever AVREF drops 0.1V. (@ADCLK = 0.5MHz, Under 2.7V resolution has no test.)
4. The CNFMRR0/1 register of XRAM has an AD/C result value which reads V_{BGR} voltage at VDD=3.3V. The CNFMRR0 has the value of ADCDRL[7:0] and CNFMRR1 has the value of ADCDRH[7:0].
5. It recommends to calculate 8 times average of remainder excluding minimum and maximum value.

7.4 Power-On Reset Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Reset Release Level	V_{POR}	–	–	1.4	–	V
Hysteresis	ΔV	–	–	0.2	–	V
VDD Voltage Rising Time	t_R	0.5V – 2.0V	0.05	–	30.0	V/ms
POR Current	I_{POR}	–	–	0.2	–	uA

Table 7 Power-on Reset Characteristics

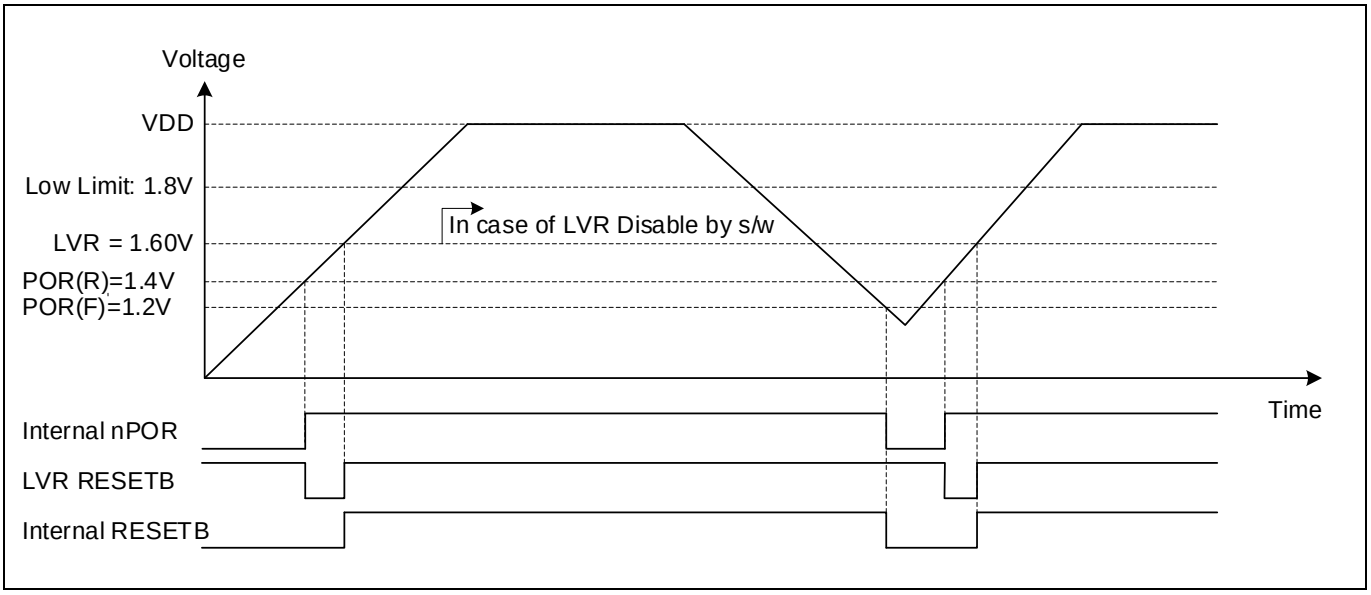


Figure 18 Power-on Reset Timing

7.5 Low Voltage Reset and Low Voltage Indicator Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Detection Level	V_{LVR} V_{LVI}	The LVR can select all levels but LVI can select other levels except 1.60V.		–	1.60	1.79	V
				1.90	2.05	2.20	
				2.00	2.15	2.30	
				2.10	2.25	2.40	
				2.22	2.37	2.52	
				2.35	2.50	2.65	
				2.45	2.65	2.85	
				2.62	2.82	3.02	
				2.81	3.01	3.21	
				3.02	3.22	3.42	
				3.27	3.47	3.67	
				3.46	3.76	4.06	
				3.80	4.10	4.40	
				4.21	4.51	4.81	
LVR Hysteresis	ΔV	–		–	50	150	mV
LVI Hysteresis	ΔV	–		–	10	100	
Minimum Pulse Width	t_{LW}	–		100	–	–	us
LVR and LVI Current	I_{BL}	Enable (Both)	VDD=3V, Run mode	–	14.0	24.0	uA
		Enable (One of two)		–	10.0	18.0	
		Disable (Both)	VDD=3V	–	–	0.1	

Table 8 LVR and LVI Characteristics

7.6 Low Current Low Voltage Reset Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Detection Level	V_{LVR}	T_A = - 10°C to + 55°C	1.71	1.80	1.89	V
Hysteresis	ΔV	–	–	25	100	mV
LVR Current	I_{BL}	VDD=3V, T_A = 25°C	–	0.9	1.5	uA

Table 9 Low Current LVR Characteristics

7.7 High Frequency Internal RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Frequency	f_{HFIRC}	VDD = 2.0V – 5.5V		–	8	–	MHz
Tolerance	–	T_A = -10°C to + 55°C	With 0.1uF bypass capacitor	-2.0	–	+2.0	%
		T_A = - 20°C to + 85°C		-3.0	–	+3.0	
		T_A = - 40°C to + 85°C		-4.0	–	+4.0	
		T_A = -10°C to + 55°C (User trim, Using only E-PGM +)		-1.0	–	+1.0	
Clock duty ratio	TOD	–		40	50	60	%
Stabilization Time	t_{HFS}	–		–	–	100	us
HFIRC Current	I_{HFIRC}	Enable		–	0.2	–	mA
		Disable		–	–	0.1	uA

Table 10 High Frequency Internal RC Oscillator Characteristics

NOTE)

1. User Trimming means the calibration of HFIRC frequency. Using E-PGM +.
2. To ensure ±1.0% tolerance of HFIRC frequency, it is necessary to do User Trimming.
3. Guaranteed by design, but might be On-Board programming after SMT process.
   (HFIRC Calibration with high temperature can cause the shift of the frequency, be sure to calibrate Enough to cool to near room temperature after SMT process)

7.8 Low Frequency Internal RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Frequency	f_{LFIRC}	VDD = 2.0V – 5.5V		–	32	–	kHz
Tolerance	–	T_A = -10°C to + 55°C	With 0.1uF bypass capacitor	-5.0	–	+5.0	%
Clock duty ratio	TOD	–		40	50	60	%
Stabilization Time	t_{LFS}	–		–	–	1	ms
LFIRC Current	I_{LFIRC}	Enable	VDD=5V	–	5	–	uA
		Disable		–	–	0.1	

Table 11 Low Frequency Internal RC Oscillator Characteristics

7.9 Internal Watch-Dog Timer RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{WDTRC}	–	2	5	10	kHz
Stabilization Time	t_{WDTS}	–	–	–	1	ms
WDTRC Current	I_{WDTRC}	Enable	–	1	–	uA
		Disable	–	–	0.1	

Table 12 Internal WDTRC Oscillator Characteristics

7.10 LCD Voltage Characteristics

(T_A= -40°C ~ +85°C, VDD=2.0V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
LCD Voltage	V_{LC3}	Voltage booster enabled, 1/2 bias	Typx0.93	1.0+(Nx0.05)	Typx1.07	V
		Voltage booster enabled, 1/3 and 1/4 bias	Typx0.93	0.75	Typx1.07	
				0.79		
				0.83		
				0.86		
				0.90		
				0.94		
				0.98		
				1.01		
				1.05		
				1.09		
				1.13		
				1.16		
				1.20		
				1.24		
				1.28		
				1.31		
LCD Mid Bias Voltage	$V_{LC0/1/2}$	Voltage booster enabled, 1/2 bias, No panel load, VDD=3V	Typx0.9	2xVLC3	Typx1.1	V
	$V_{LC0/1}$	Voltage booster enabled, 1/3 bias, No panel load, VDD=3V	Typx0.9	3xVLC3	Typx1.1	
	V_{LC2}		Typx0.9	2xVLC3	Typx1.1	
	V_{LC0}	Voltage booster enabled, 1/4 bias, No panel load, VDD=3V	Typx0.9	4xVLC3	Typx1.1	
	V_{LC1}		Typx0.9	3xVLC3	Typx1.1	
	V_{LC2}		Typx0.9	2xVLC3	Typx1.1	
	V_{LC1}	Voltage booster disabled, LCD dividing resistor, VDD=2.7V to 5.5V, 1/4 bias, LCD clock = 0Hz, V_{LC0}=VDD	Typ-0.2	0.75xVDD	Typ+0.2	V
	V_{LC2}		Typ-0.2	0.5xVDD	Typ+0.2	
	V_{LC3}		Typ-0.2	0.25xVDD	Typ+0.2	
LCD Driver Output Impedance	R_{LO}	V_{LCD}=3V, I_{LOAD}=±10uA	–	5	10	kΩ
LCD Bias Dividing Resistor	R_{LCD1}	Internal resistor mode, T_A = 25°C	20	30	40	kΩ
	R_{LCD2}		40	60	80	
	R_{LCD3}		80	120	160	
LCD Block Current	I_{LCD}	Voltage booster mode, VDD=3V, V_{LCD}=3.15V, 1/3Bias	–	3	6	uA

Table 13 LCD Voltage Characteristics

NOTE)

1. Where N is the value of LCDCCR register (N = 0 to 15).

7.11 DC Characteristics

(T_A= -40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS= 0V, f_{XIN}= 12MHz)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input High Voltage	V_{IH1}	P32-P36, P4, P5, P6, RESETB		0.8VDD	–	VDD	V
	V_{IH2}	All input pins except V_{IH1}		0.7VDD	–	VDD	
Input Low Voltage	V_{IL1}	P32-P36, P4, P5, P6, RESETB		–	–	0.2VDD	V
	V_{IL2}	All input pins except V_{IL1}		–	–	0.3VDD	
Output High Voltage	V_{OH}	VDD=4.5V, I_{OH} = – 2mA; All output ports except REM pin		VDD-1.0	–	–	V
Output Low Voltage	V_{OL}	VDD=4.5V, I_{OL}=15mA; All output ports except REM pin		–	–	1.0	V
Output High Current	I_{OH}	VDD=4.5V, V_{OH} = 3.5V; All output ports except REM pin		-2	–	–	mA
Output Low Current	I_{OL}	VDD=4.5V, V_{OL} = 1.0V; All output ports except REM pin		15	–	–	mA
REM Output High Current	I_{OH1}	VDD=3.0V, V_{OH}=2.0V, ROTS=1		–	-10	-5	mA
REM Output Low Current	I_{OL1}	VDD=3.0V, V_{OL}=1.0V, TA=25°C	ROTS=1	2.5	5.0	–	mA
	I_{OL2}		ROTS=0, RIOL=3	470	630	–	
Input high leakage current	I_{IH}	All Input ports		–	–	1	uA
Input low leakage current	I_{IL}	All Input ports		-1	–	–	uA
Pull-up resistor	R_{PU1}	VI=0V, TA=25°C, All Input ports	VDD=5V	50	80	110	kΩ
			VDD=3V	100	155	210	
	R_{PU2}	VI=0V, TA=25°C, RESETB	VDD=5V	150	250	400	
			VDD=3V	300	500	700	
OSC feedback resistor	R_{X1}	XIN=VDD, XOUT=VSS TA=25°C, VDD=5V FBS = 0 (Configure Option 2 : 3FH)		600	1200	2000	kΩ
		XIN=VDD, XOUT=VSS TA=25°C, VDD=5V FBS = 1 (Configure Option 2 : 3FH)		250	500	750	
	R_{X2}	SXIN=VDD, SXOUT=VSS TA=25°C, VDD=5V		2500	5000	10000	kΩ

Table 14 DC Characteristics

7.11 DC Characteristics (Continued)

(T_A= -40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS= 0V, f_{XIN}= 12MHz)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply current	I_{DD1} (Run)	f_{XIN}=12MHz, VDD=5V±10%		–	3.0	6.0	mA
		f_{XIN}=8MHz, VDD=3V±10%		–	2.0	4.0	
		f_{HFIRC}=8MHz, VDD=5V±10%		–	2.0	4.0	
	I_{DD2} (Idle)	f_{XIN}=12MHz, VDD=5V±10%		–	2.0	4.0	mA
		f_{XIN}=8MHz, VDD=3V±10%		–	1.0	2.0	
		f_{HFIRC}=8MHz, VDD=5V±10%		–	1.0	2.0	
	I_{DD3} (Run)	f_{SUB}=32.768kHz	VDD=3V±10%, TA=25°C	–	90.0	180.0	uA
		f_{LFIRC}=32kHz		–	90.0	180.0	
	I_{DD4} (Idle)	f_{SUB}=32.768kHz		–	4.0	8.0	uA
		f_{LFIRC}=32kHz		–	6.0	12.0	
	I_{DD5}	Stop, VDD=3V±10%, TA=25°C		–	0.5	2.7	uA

Table 15 Table 7.11 DC Characteristics (Continued)

NOTE)

1. Where the f_{XIN} is an external main oscillator, the f_{SUB} is an external sub oscillator, the f_{HFIRC} is an internal high frequency RC oscillator, the f_{LFIRC} is an internal low frequency RC oscillator and the fx is the selected system clock.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current items include the current of the power-on reset (POR) block.

7.12 AC Characteristics

(T_A= -40°C ~ +85°C, VDD=1.8V ~ 5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RESETB input low width	t_{RST}	VDD = 5 V	10	–	–	us
Interrupt Input High, Low width	t_{IWH}, t_{IWL}	All interrupts, VDD = 5 V	200	–	–	ns
External Counter Input High, Low Pulse Width	t_{ECWH}, t_{ECWL}	ECn, VDD = 5 V (n=0, 2)	200	–	–	
External Counter Transition Time	t_{REC}, t_{FEC}	ECn, VDD = 5 V (n=0, 2)	20	–	–	
REM port High, Low width	t_{REMWH}, t_{REMWL}	REM, VDD = 5 V	5	–	–	us

Table 16 AC Characteristics

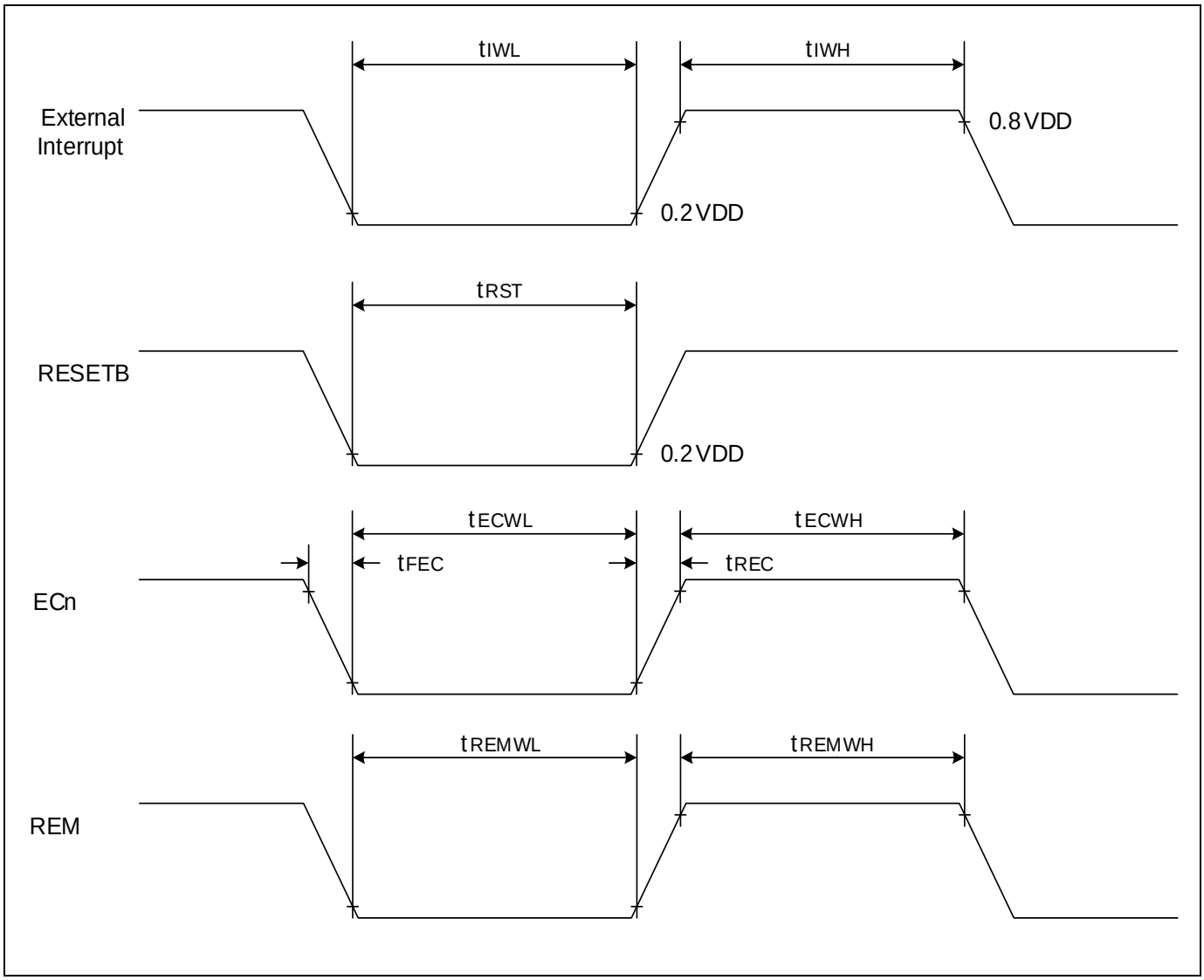


Figure 19 AC Timing

7.13 UART TIMING CHARACTERISTICS

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, f_{XIN}=11.1MHz)

Parameter	Symbol	Min	Typ	Max	Units
Serial port clock cycle time	t_{SCK}	1250	t_{CPU} x 16	1650	ns
Output data setup to clock rising edge	t_{S1}	590	t_{CPU} x 13	–	
Clock rising edge to input data valid	t_{S2}	–	–	590	
Output data hold after clock rising edge	t_{H1}	t_{CPU} – 50	t_{CPU}	–	
Input data hold after clock rising edge	t_{H2}	0	–	–	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	470	t_{CPU} x 8	970	

Table 17 UART TIMING CHARACTERISTICS

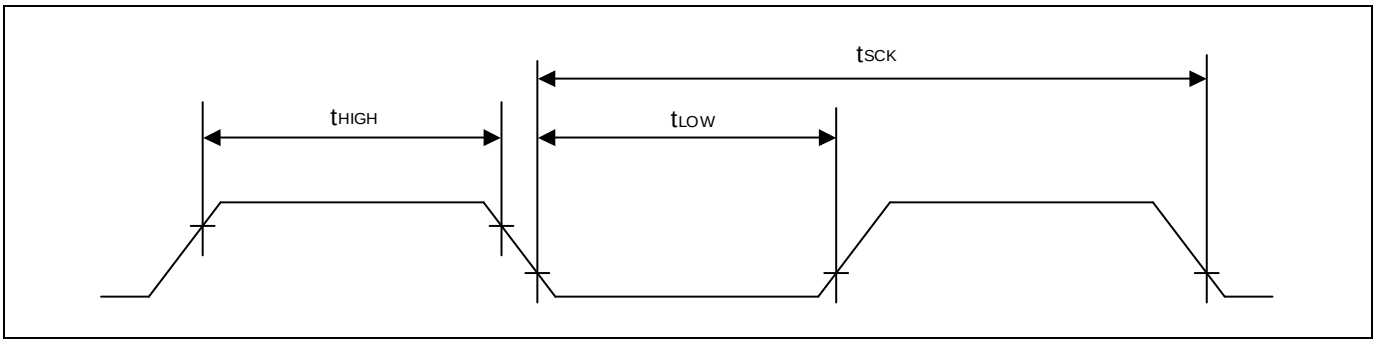


Figure 20 Waveform for UART Timing

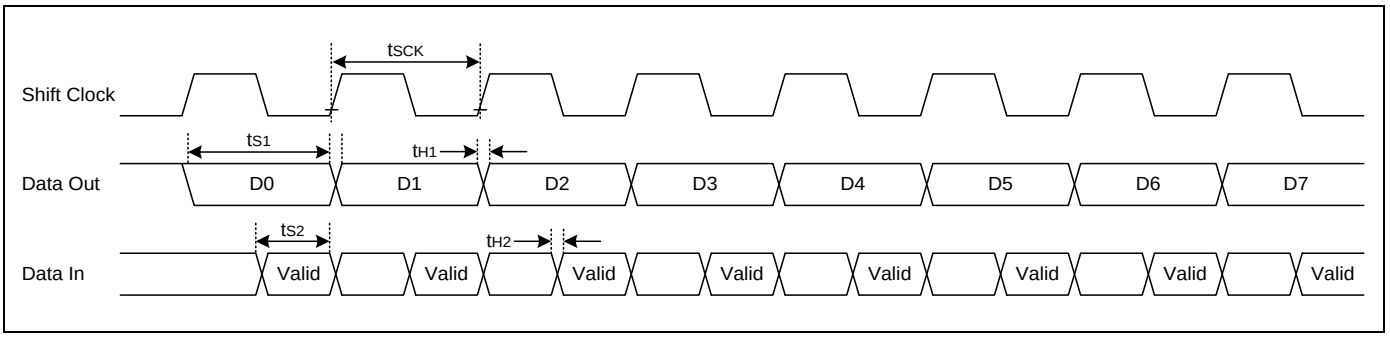


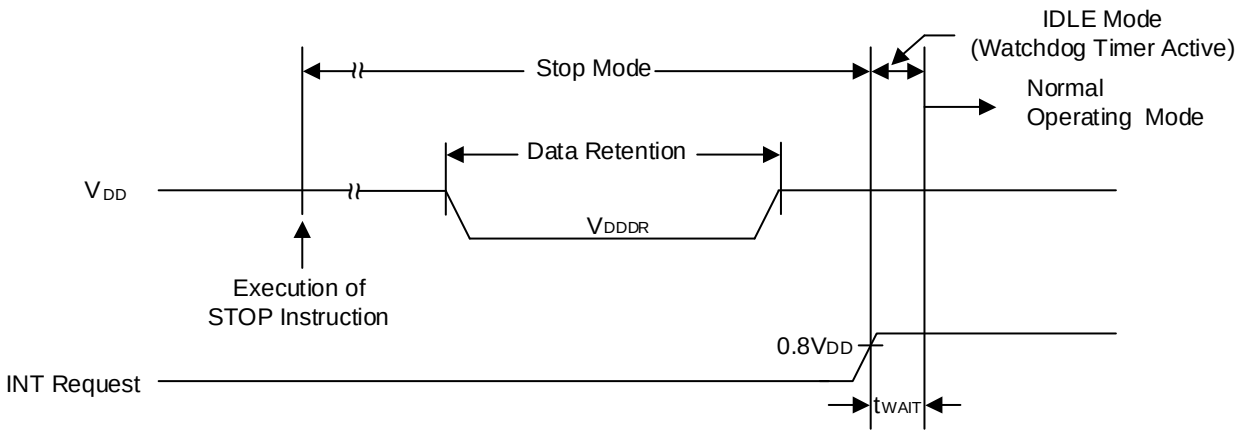
Figure 21 Timing Waveform for UART Module

7.14 Data Retention Voltage in Stop Mode

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V)

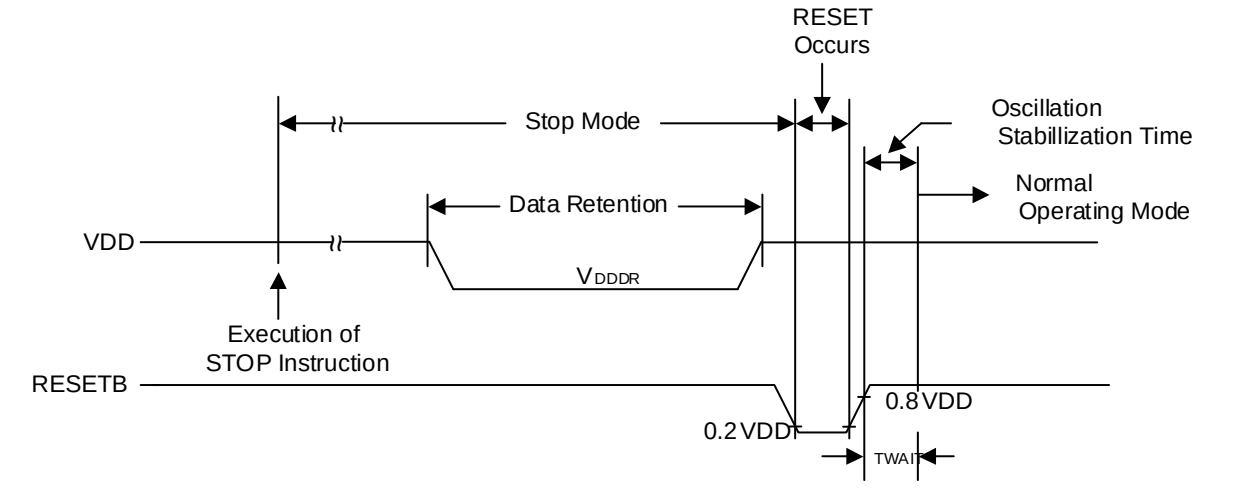
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data retention supply voltage	V_{DDDR}	–	1.0	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8V (T_A = 25°C), Stop mode	–	–	1	uA

Table 18 Data Retention Voltage in Stop Mode



NOTE) tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 22 Stop Mode Release Timing when Initiated by an Interrupt



NOTE) tWAIT is the same as (4096 X 4 X 16/f_{IRC}) = (16.4 ms at fx=1MHz).

Figure 23 Stop Mode Release Timing when Initiated by RESETB

7.15 Internal Flash Rom Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Sector Write Time	t_{FSW}	–	–	2.5	2.7	ms
Sector Erase Time	t_{FSE}	–	–	2.5	2.7	
Hard-Lock Time	t_{FHL}	–	–	2.5	2.7	
Page Buffer Reset Time	t_{FBR}	–	–	–	5	us
Flash Programming Voltage	v_{PGM}	–	2.0	–	5.5	V
Flash Programming Frequency	f_{PGM}	–	0.4	–	–	MHz
Endurance of Write/Erase	NF_{WE}	Sector 0 to 763	–	–	10,000	Times
		Sector 764 to 767 (256 bytes)	–	–	100,000	
Flash Data Retention Time	t_{RT}	–	10	–	–	Years

Table 19 Internal Flash Rom Characteristics

NOTE)

1. During a flash operation, SCLK[1:0] of SCCR must be set to “00” or “01” (HF INT-RC OSC or Main X-TAL for system clock).

7.16 Input/Output Capacitance

(T_A=-40°C ~ +85°C, VDD=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Capacitance	C_{IN}	fx=1MHz Unmeasured pins are connected to Vss	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

Table 20 Input/Output Capacitance

7.17 Main Clock Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V)

Oscillator	Parameter	Conditions	Min	Typ.	Max	Units
Crystal	Main oscillation frequency	2.0 V – 5.5 V	0.4	–	4.2	MHz
		2.4 V – 5.5 V	0.4	–	8.0	
		3.0 V – 5.5 V	0.4	–	12.0	
Ceramic Oscillator	Main oscillation frequency	1.8 V – 5.5 V	0.4	–	4.2	
		2.4 V – 5.5 V	0.4	–	8.0	
		3.0 V – 5.5 V	0.4	–	12.0	
External Clock	XIN input frequency	1.8 V – 5.5 V	0.4	–	4.2	MHz
		2.4 V – 5.5 V	0.4	–	8.0	
		3.0 V – 5.5 V	0.4	–	12.0	

Table 21 Main Clock Oscillator Characteristics

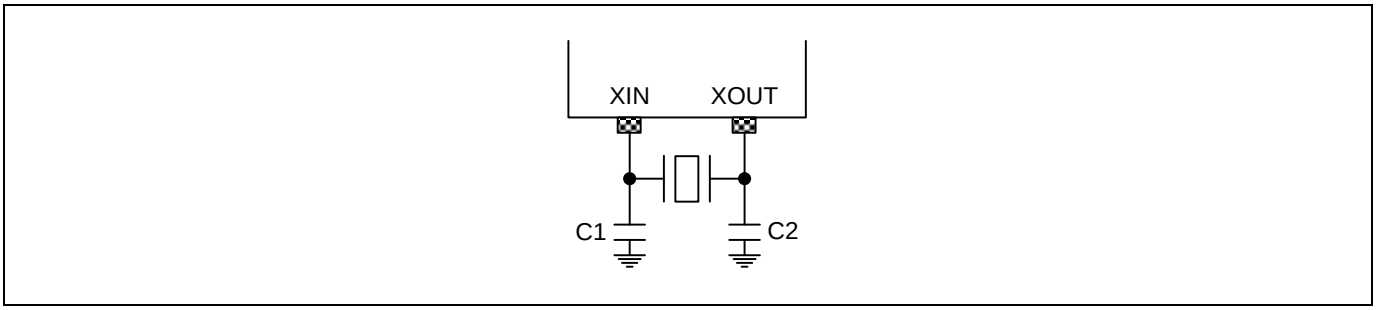


Figure 24 Crystal/Ceramic Oscillator

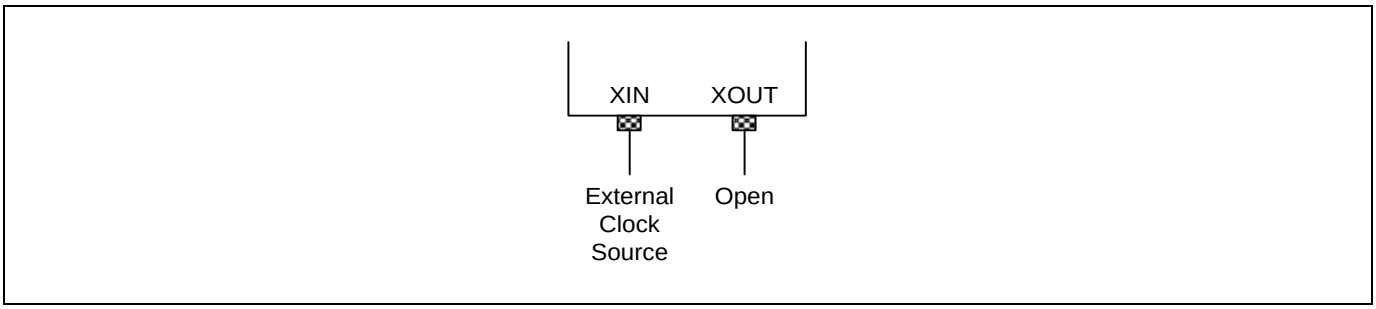


Figure 25 External Clock

7.18 Sub Clock Oscillator Characteristics

(T_A= -40°C ~ +85°C, VDD=1.8V ~ 5.5V)

Oscillator	Parameter	Conditions	Min	Typ.	Max	Units
Crystal	Sub oscillation frequency	1.8 V – 5.5 V	32	32.768	38	kHz
External Clock	SXIN input frequency		32	–	100	

Table 22 Sub Clock Oscillator Characteristics

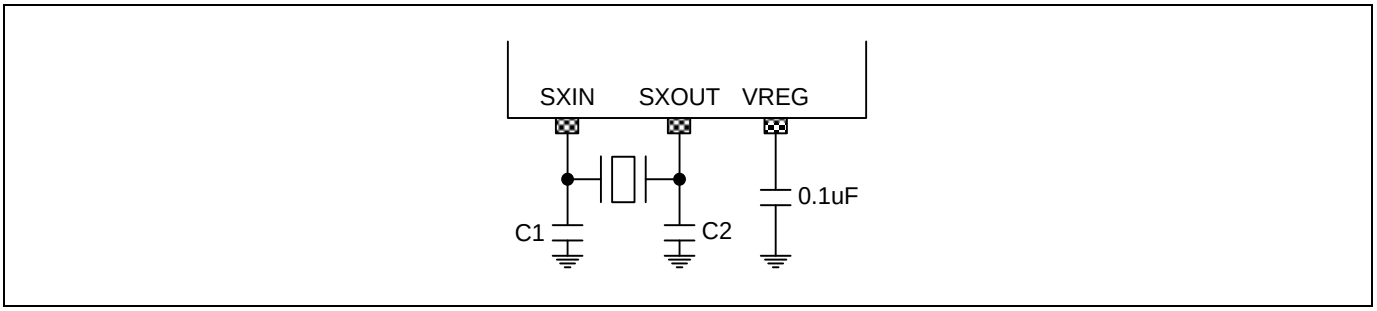


Figure 26 Crystal Oscillator

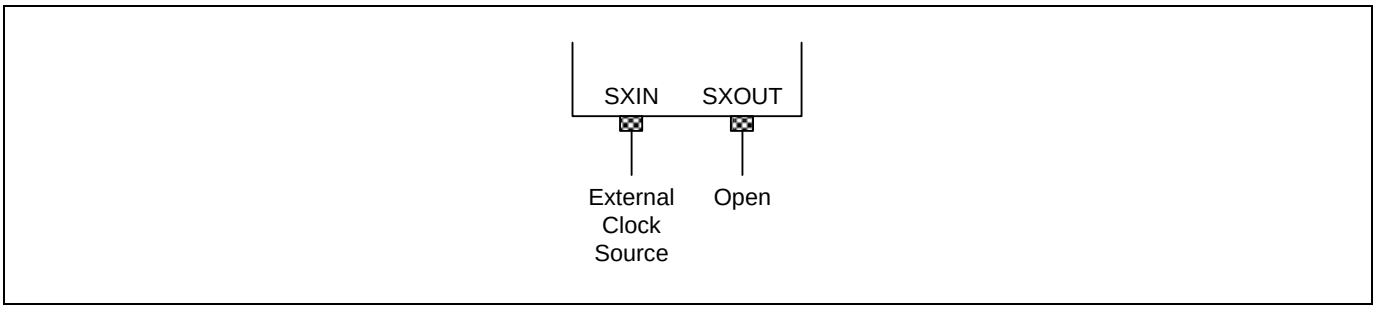


Figure 27 External Clock

7.19 Main Oscillation Stabilization Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V)

Oscillator	Conditions	Min	Typ.	Max	Units
Crystal	fXIN ≥ 1 MHz, VDD= 2.0V ~ 5.5V Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	–	–	60	ms
Ceramic	fXIN ≥ 1 MHz, VDD= 1.8V ~ 5.5V Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	–	–	10	
External Clock	fXIN = 0.4 to 12 MHz XIN input high and low width (t_{XL}, t_{XH})	42	–	1250	ns

Table 23 Main Oscillation Stabilization Characteristics

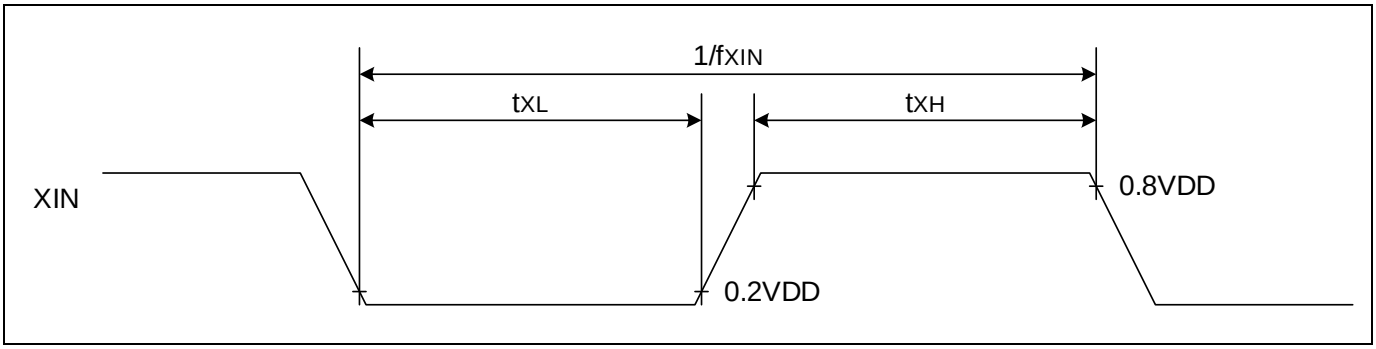


Figure 28 Clock Timing Measurement at XIN

7.20 Sub Oscillation Stabilization Characteristics

(T_A= -40°C ~ +85°C, VDD=1.8V ~ 5.5V)

Oscillator	Conditions	Min	Typ.	Max	Units
Crystal	–	–	–	10	sec
	VDD = 3.0V, T_A = 25°C	–	0.7	1.5	
External Clock	SXIN input high and low width (t_{XL}, t_{XH})	5	–	15	us

Table 24 Sub Oscillation Stabilization Characteristics

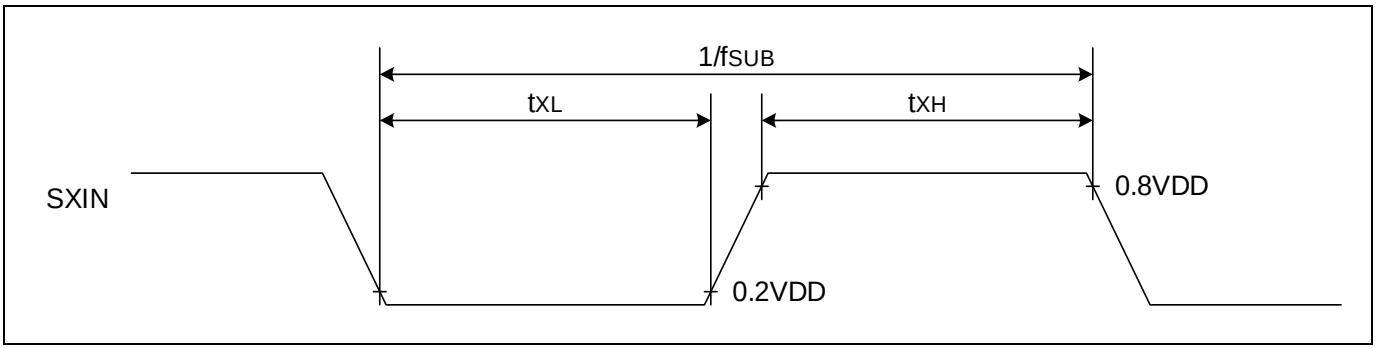


Figure 29 Clock Timing Measurement at SXIN

7.21 Operating Voltage Range

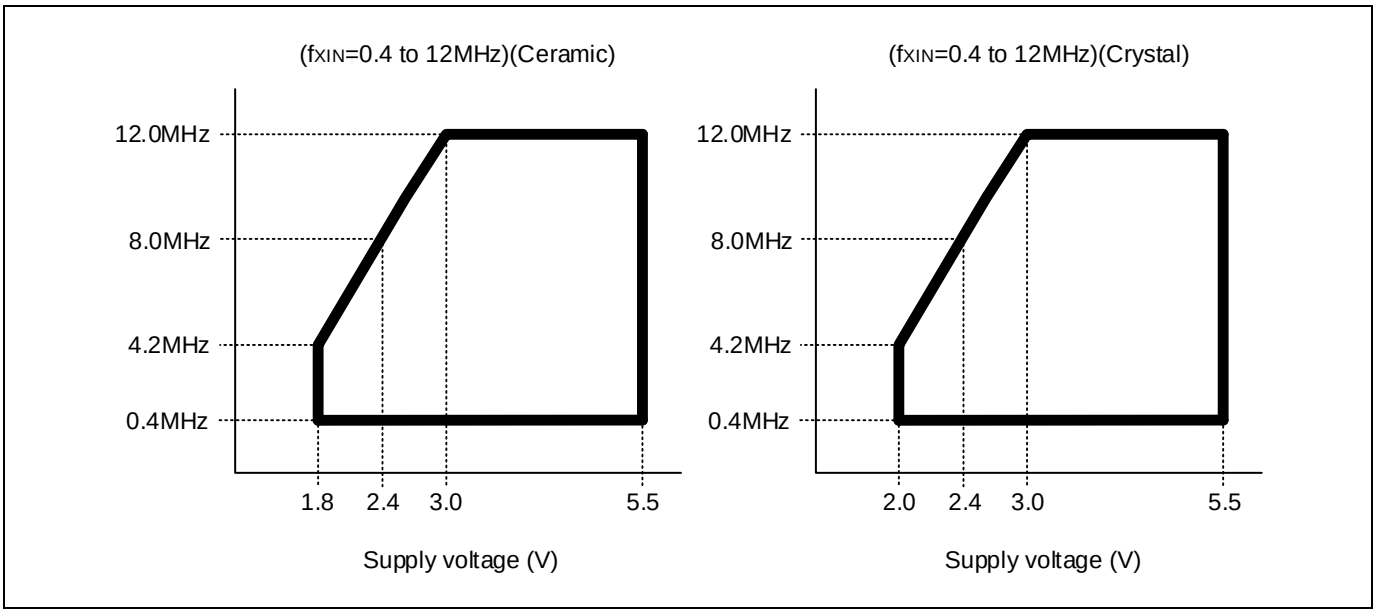


Figure 30 Operating Voltage Range (Main OSC)

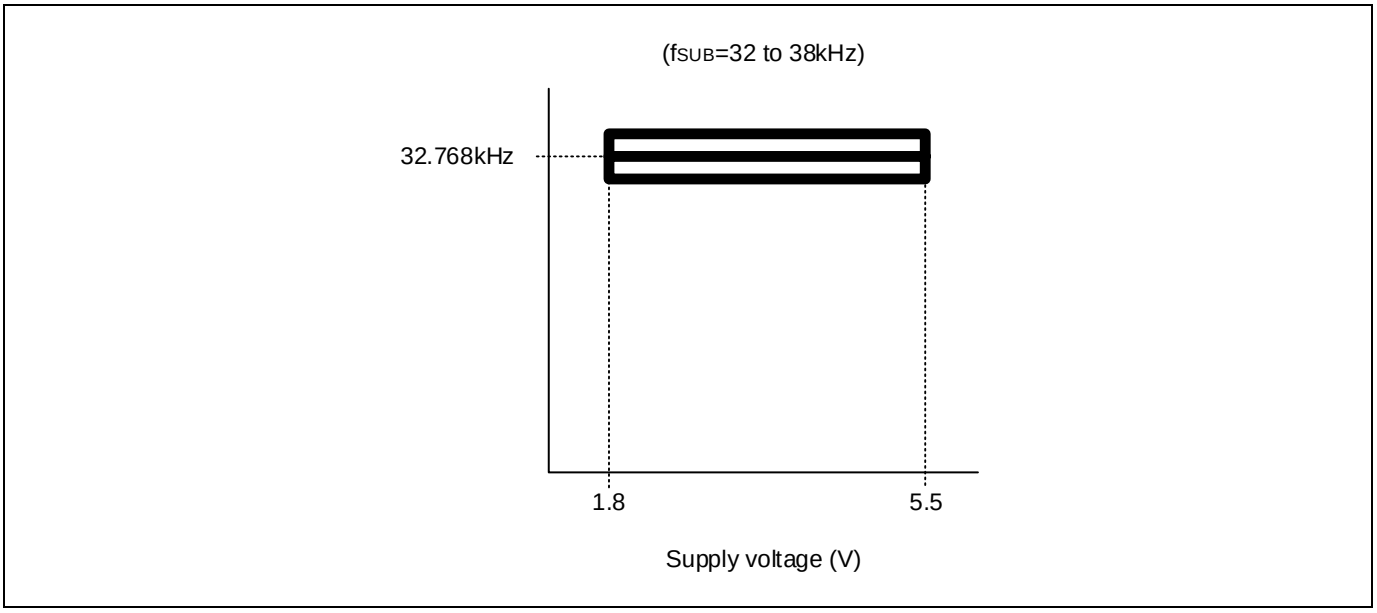


Figure 31 Operating Voltage Range (Sub OSC)

7.22 Recommended Circuit and Layout

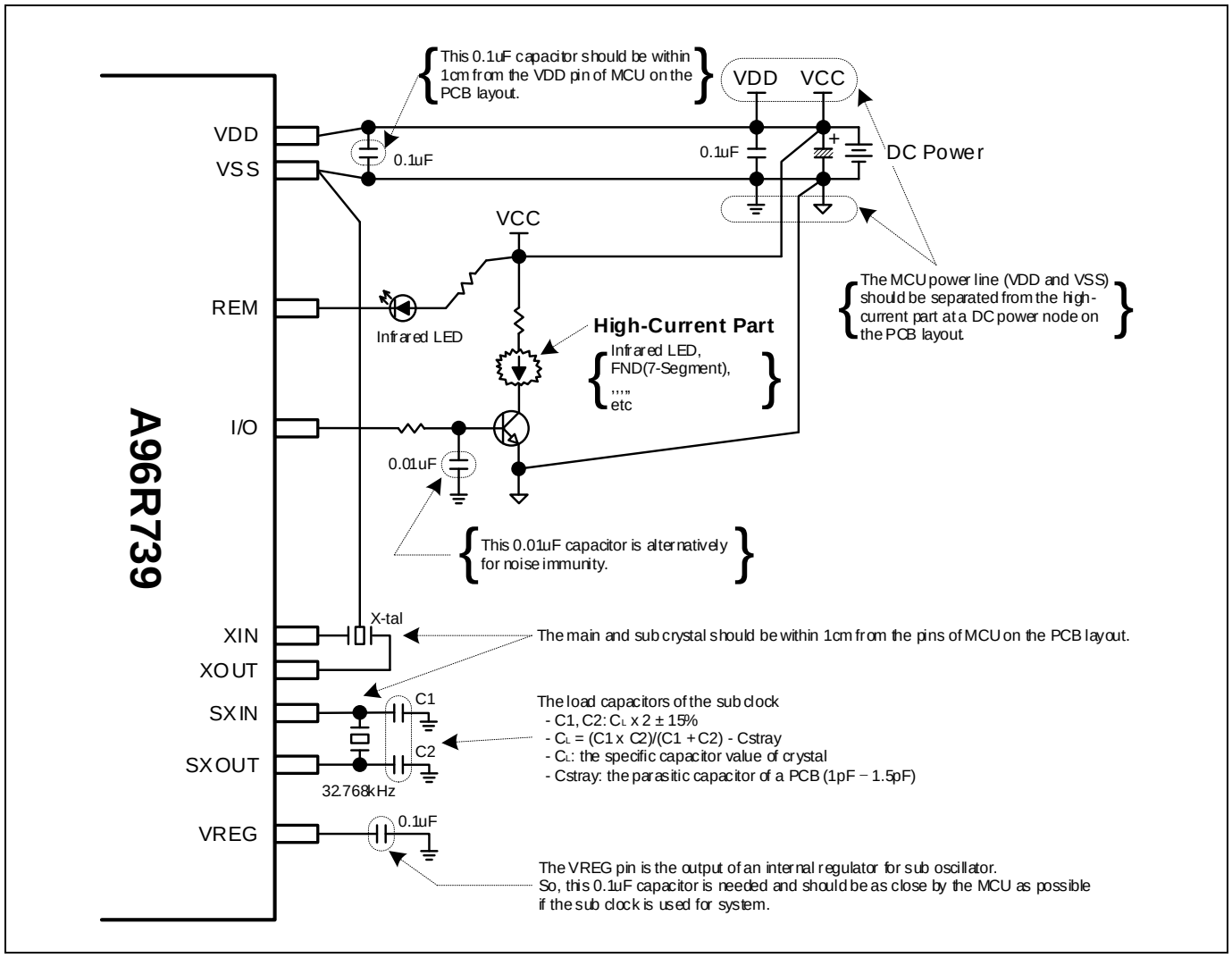


Figure 32 Recommended Circuit and Layout

7.23 Recommended Circuit for Remote controller

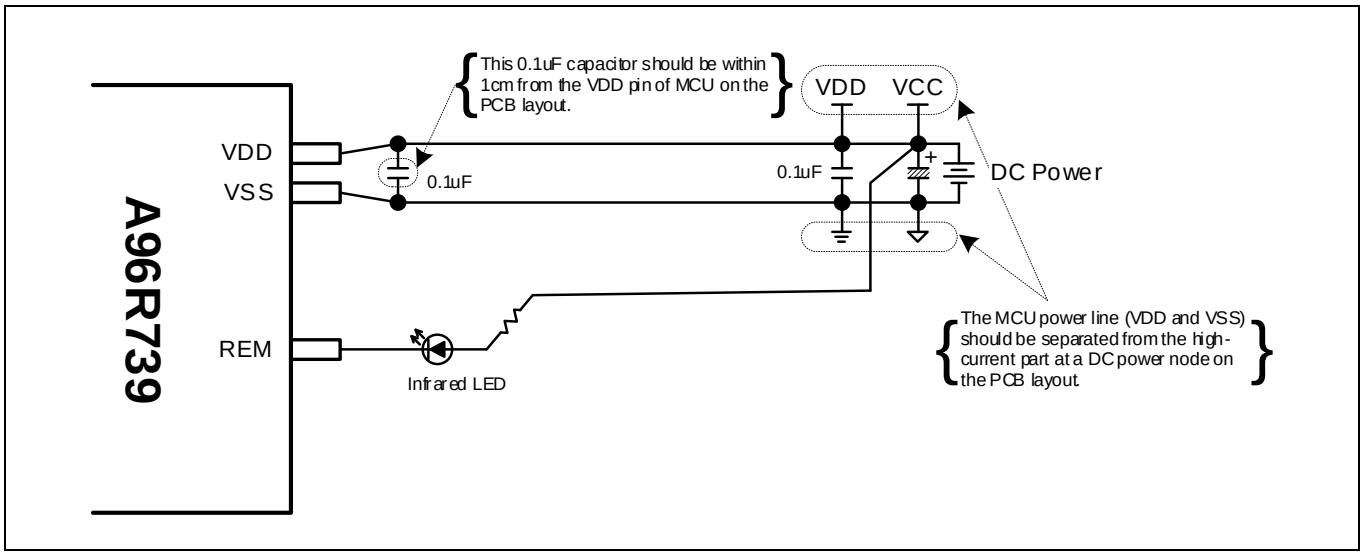
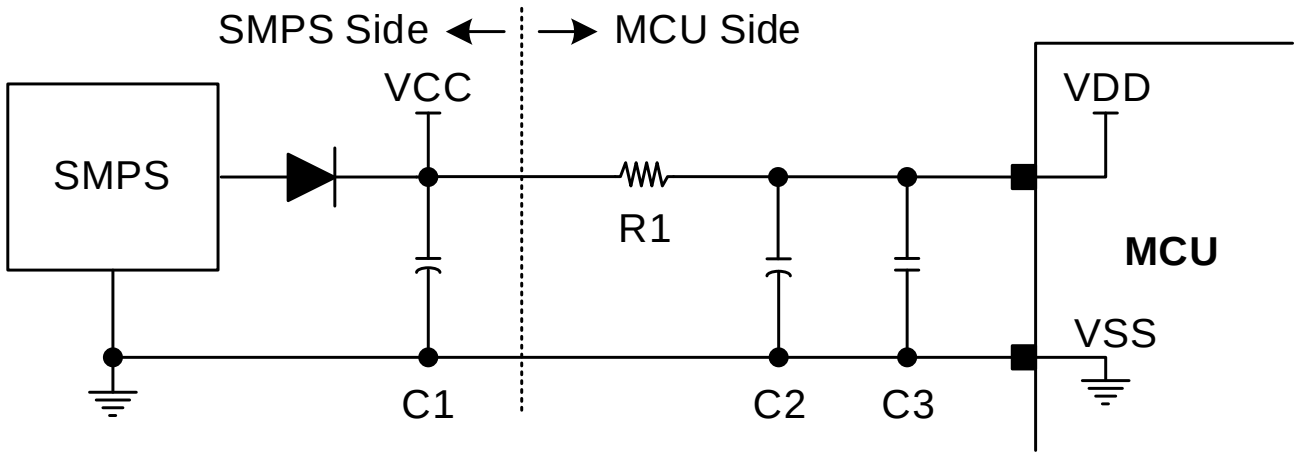


Figure 33 Recommended Circuit for Remote controller

7.24 Recommended Circuit and Layout with SMPS Power



NOTE)

1. The C1 capacitor is to flatten out the voltage of the SMPS power, VCC.
   √ Recommended C1: 470uF/25V more.
2. The R1 and C2 are the RC filter for VDD and suppress the ripple of VCC.
   √ Recommended R1: 10Ω - 20Ω
   √ Recommended C2: 47uF/25V more
   √ The R1 and C2 should be as close by the C3 as possible.
3. The C3 capacitor is used for temperature compensation because an electrolytic capacitor becomes worse characteristics at low temperature.
   √ Recommended C3: ceramic capacitor 2.2uF more
   √ The C3 should be within 1cm from VDD pin of MCU on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc) when the SMPS supplies the VDD of MCU.

Figure 34 Recommended Circuit and Layout with SMPS Power

7.25 Typical Characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

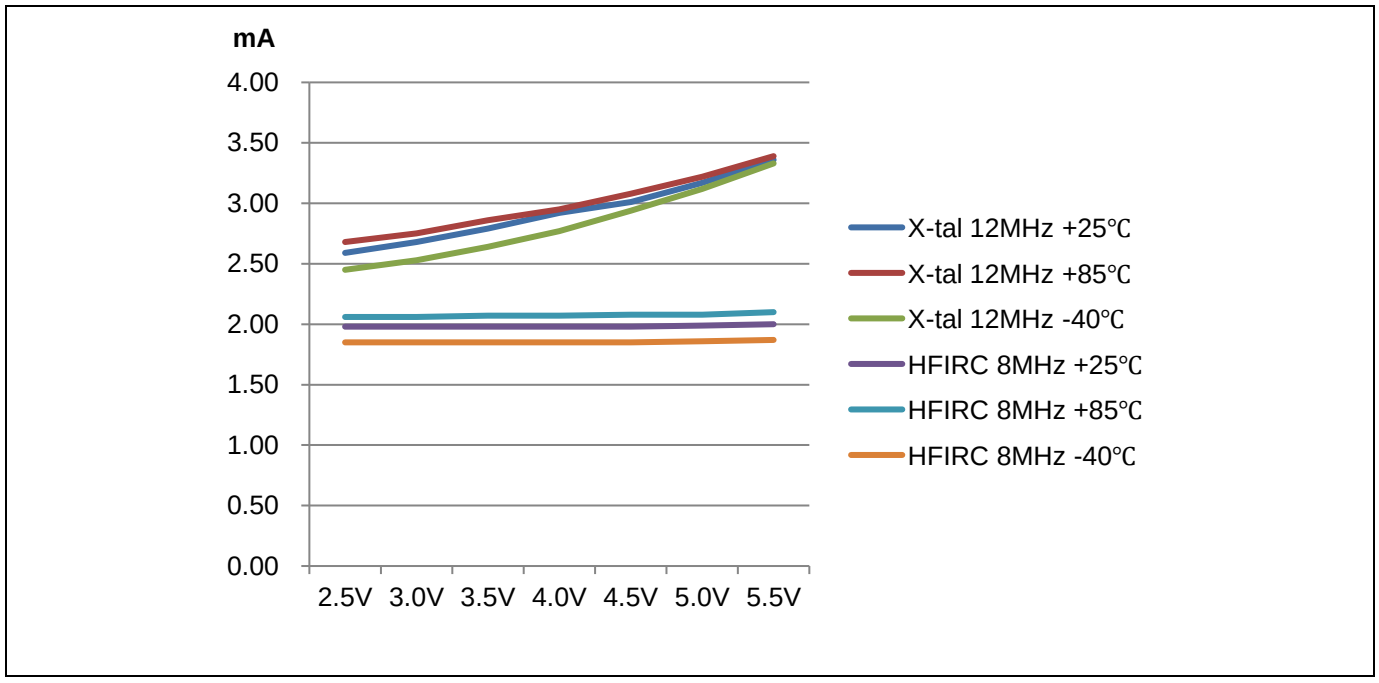


Figure 35 RUN (IDD1) Current

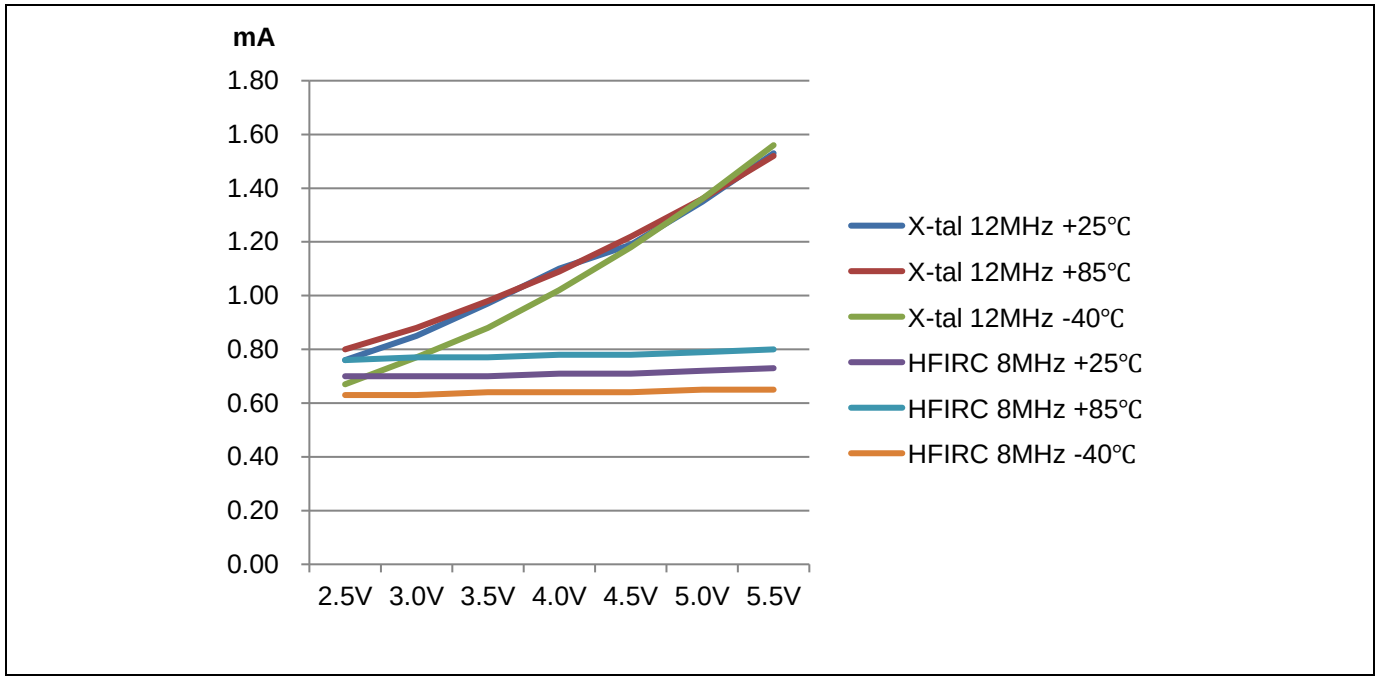


Figure 36 IDLE (IDD2) Current

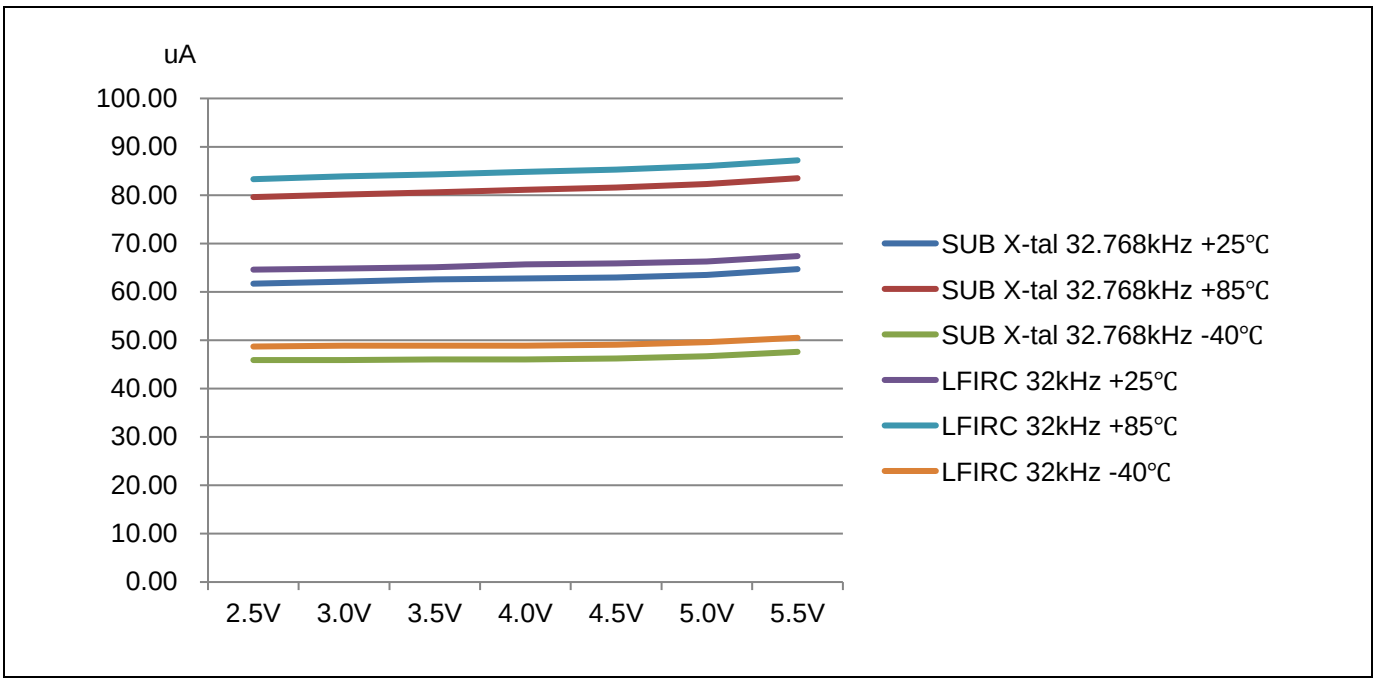


Figure 37 RUN (IDD3) Current

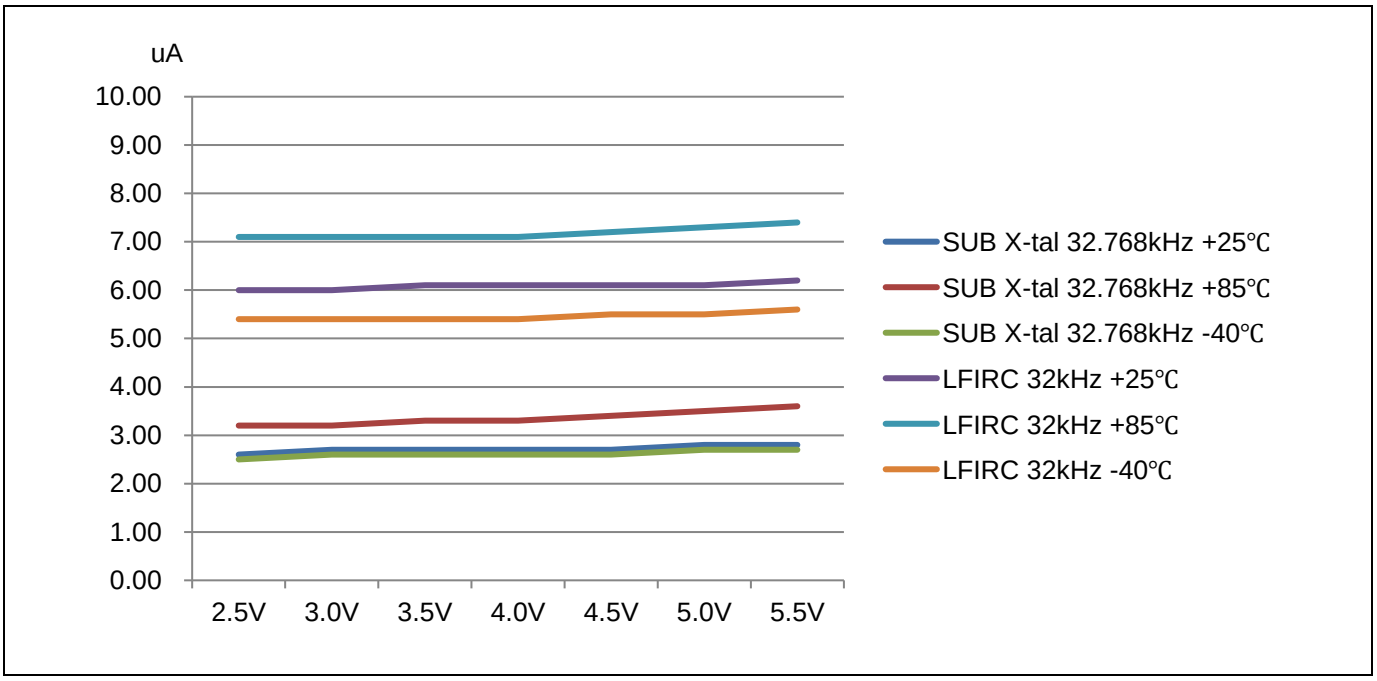


Figure 38 IDLE (IDD4) Current

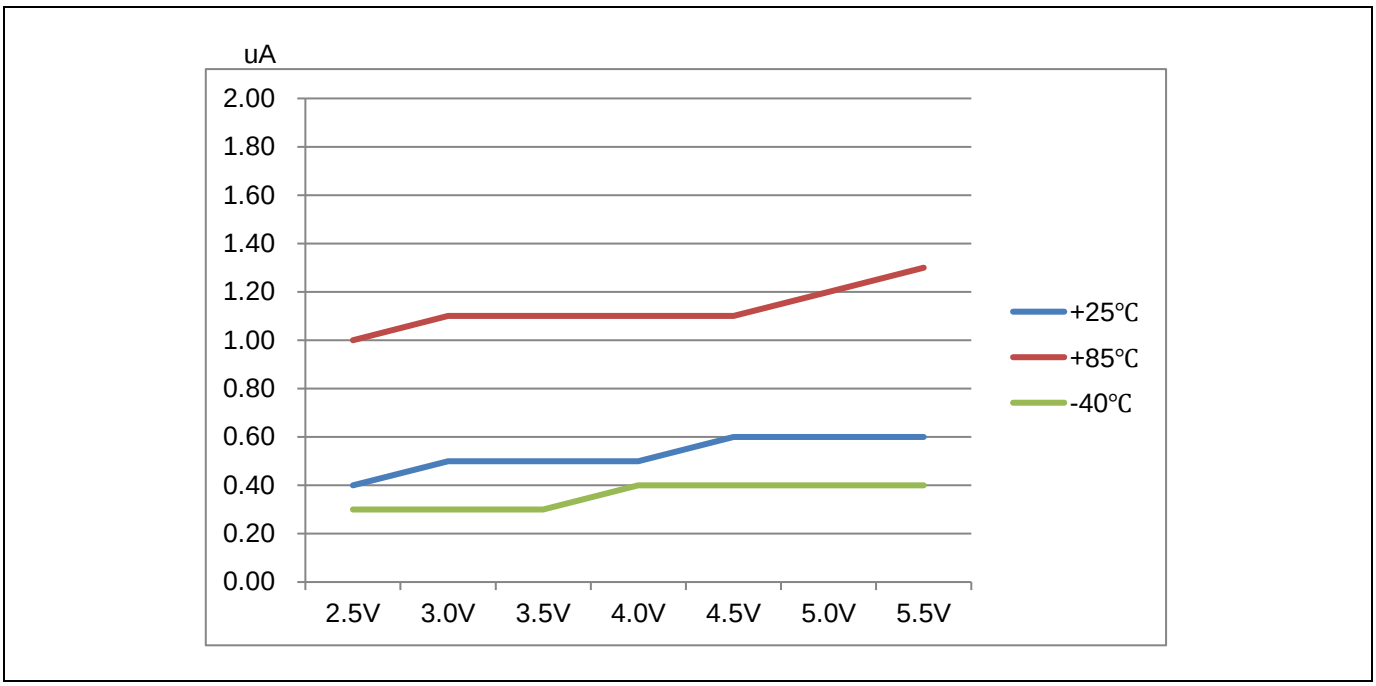


Figure 39 STOP (IDD5) Current

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