ABOV SEMICONDUCTOR Co., Ltd.
8-BIT MICROCONTROLLERS

# MC96F7864S

*Data Sheet (Ver. 1.03)*

# REVISION HISTORY

**VERSION 0.1 (December 8, 2021)**

**VERSION 0.5 (January 25, 2022)**

Fix the typos.

Change Internal VDC voltage value in A/D Converter characteristics.

Change Sector Erase Time typ/max value in Internal Flash Rom characteristics

Change RLCD1 min/max value in LCD Voltage characteristics.

**VERSION 0.6 (February 16, 2022)**

Change “IDD1~IDD5” in DC electrical characteristics.

Change LVR/LVI current typ/max value in LVR and LVI characteristics.

Change PLL parameter in PLL characteristics.

**VERSION 0.7 (February 25, 2022)**

Add IDD graph in Typical characteristics.

**VERSION 1.0 (April 19, 2022)**

Add MC96F7664SL 64LQFP-1010 Package

**VERSION 1.1 (November 17, 2022)**

Add POR graph in Power-On Reset characteristics.

**VERSION 1.2 (November 22, 2022)**

Add Revision history.

**VERSION 1.3 (November 23, 2022)**

Add comment in Electrical Characteristics.

**VERSION 1.03 (May 08, 2023)**

Changed the format of the revision number to “X.YY” according to internal policy.

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# MC96F7864S

## CMOS SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 12-BIT A/D CONVERTER

## 1. Overview

### 1.1 Description

The MC96F7864S is advanced CMOS 8-bit microcontroller with 64k bytes of FLASH. This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This provides the following features : 64k bytes of FLASH, 256 bytes of IRAM, 3,072 bytes of XRAM , general purpose I/O, basic interval timer, watchdog timer, 8/16-bit timer/counter, 16-bit PPG output, 8-bit PWM output, 10-bit PWM output, watch timer, buzzer driving port, SPI, UART, I2C, 12-bit A/D converter, LCD driver, on-chip POR, LVR, LVI, on-chip oscillator and clock circuitry. The MC96F7864S also supports power saving modes to reduce power consumption.

| Device Name | FLASH | XRAM | IRAM | ADC | I/O PORT | Package |
|---|---|---|---|---|---|---|
| MC96F7864SL<br>MC96F7664SL<br>MC96F7664SL14 | 64k bytes | 3,072 bytes | 256 bytes | 12 channel<br>10 channel<br>10 channel | 71<br>55<br>55 | 80 LQFP-1212<br>64 LQFP-1010<br>64 LQFP-1414 |

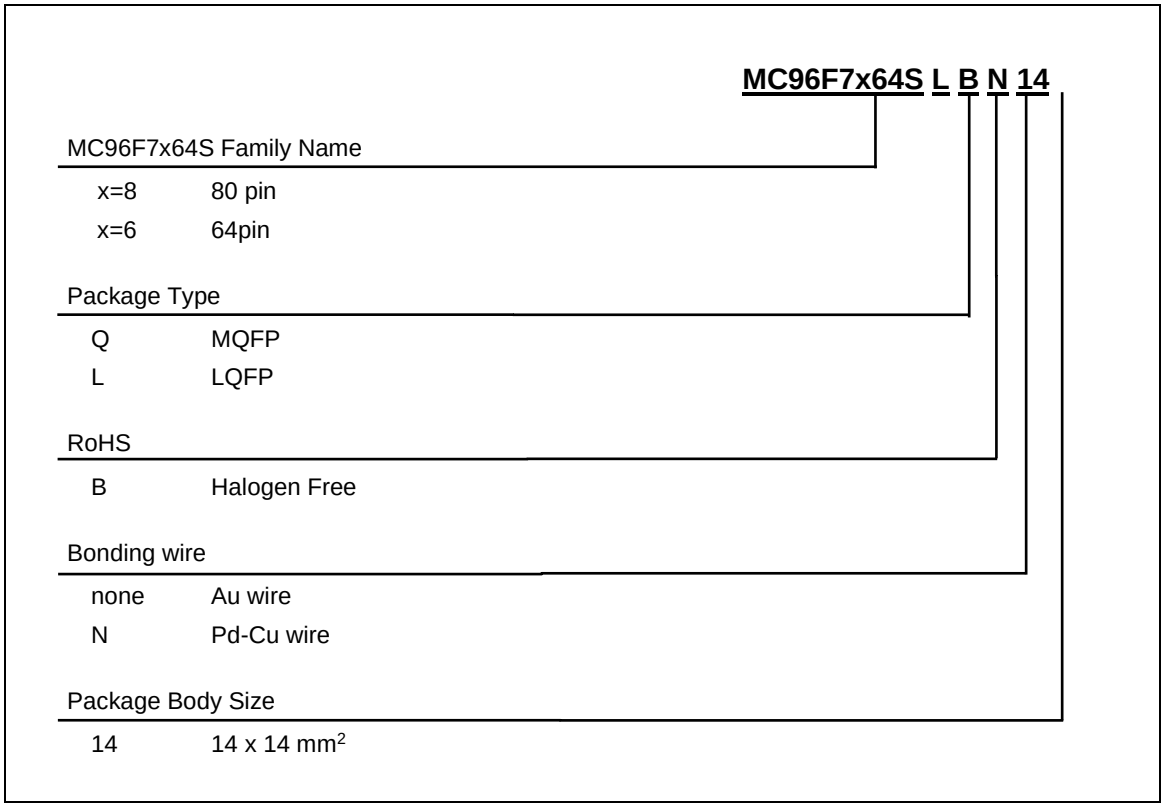



**Figure 1.1 Device Nomenclature**

## 1.2 Features

- **CPU**
  - 8 Bit CISC Core (8051 Compatible)
- **ROM (FLASH) Capacity**
  - 64k Bytes
  - Flash with self read/write capability
  - Parity bit check function for flash fail detection
  - On chip debug and In-system programming (ISP)
  - Endurance : 10,000 times (Sector 0~1019)
    100,000 times (Sector 1020~1023)
  - Retention : 10 years
- **256 Bytes IRAM**
- **3,072 Bytes XRAM**
  - (40 Bytes including LCD display RAM)
- **General Purpose I/O (GPIO)**
  - Normal I/O : 21 Ports
    (P0, P1, P6[6:2])
  - LCD shared I/O : 50 Ports
    (P2, P3, P4, P5, P6[1:0], P7, P8)
- **Basic Interval Timer (BIT)**
  - 8Bit × 1ch
  - **Watch Dog Timer (WDT)**
  - 8Bit × 1ch
  - 5kHz internal RC oscillator
- **10Bit PWM Generator**
  - Emergency/Shot stop available
- **Timer/ Counter**
  - 8Bit × 3ch (T0/T1/T2), 16Bit × 4ch (T3/T4/T5/T6)
  - 8Bit × 2ch (T7/T8) or 16 Bit × 1ch (T7)
- **Programmable Pulse Generation**
  - 8Bit PWM (by T0/T1/T2)
  - Pulse generation (by T3/T4/T5/T6)
  - 6-ch 10Bit PWM for Motor (by T8)
- **Watch Timer (WT)**
  - 3.91ms/0.25s/0.5s/1s/1m interval at 32.768kHz
- **Buzzer**
  - 8Bit × 1ch
- **SPI**
  - 8Bit × 2ch
- **UART**
  - 8Bit × 3ch
- **USI (UART + SPI + I2C)**
  - 8Bit UART × 2ch, 8Bit SPI × 2ch, and I2C × 2ch
- **LCD Driver**
  - 36 Segments and 8 Common terminals
  - Internal or external resistor bias
  - Capacitor bias (Voltage Booster)
  - 16-step contrast control
  - 1/2, 1/3, 1/4, 1/5, 1/6, and 1/8 duty selectable
  - 1/2, 1/3, and 1/4 bias selectable
- **12 Bit A/D Converter**
  - 12 Input channels
- **Power On Reset**
  - Reset release level (1.4V)
- **Low Voltage Reset**
  - 14 level detect (1.60V/ 2.00V/ 2.10V/ 2.20V/ 2.32V/ 2.44V/ 2.59V/ 2.75V/ 2.93V/ 3.14V/ 3.38V/ 3.67V/ 4.00V/ 4.40V)
- **Low Voltage Indicator**
  - 13 level detect (2.00V/ 2.10V/ 2.20V/ 2.32V/ 2.44V/ 2.59V/ 2.75V/ 2.93V/ 3.14V/ 3.38V/ 3.67V/ 4.00V/ 4.40V)
  - External reference detect
- **Interrupt Sources**
  - External Interrupts
    (EINT0~9, EINT10~18) (19)
  - Timer(0/1/2/3/4/5/6/7/8) (13)
  - WDT (1)
  - BIT (1)
  - WT (1)
  - PWM (3)
  - SPI 2/3 (2)
  - UART 2/3/4 (6)
  - USI0/1 (4)
  - ADC (1)
- **Internal RC Oscillator**
  - Internal RC frequency:
    16MHz ±1.5% ($T_A$= 0 ~ +50°C)
- **Power Down Mode**
  - STOP, IDLE mode

- **Operating Voltage and Frequency**
  - 1.8V ~ 5.5V (@32 ~ 38kHz with X-tal)
  - 1.8V ~ 5.5V (@0.4 ~ 4.2MHz with X-tal)
  - 2.7V ~ 5.5V (@0.4 ~ 12.0MHz with X-tal)
  - 1.8V ~ 5.5V (@0.5 ~ 8.0MHz with Internal RC)
  - 2.0V ~ 5.5V (@0.5 ~ 16.0MHz with Internal RC)
  - 2.0V ~ 5.5V (@1.0 ~ 16.0MHz with PLL)
  - Voltage dropout converter included for core
- **Minimum Instruction Execution Time**
  - 125ns (@ 16MHz main clock)
  - 61μs (@t 32.768kHz sub clock)
- **Operating Temperature:** – 40 ~ + 85℃
- **Oscillator Type**
  - 0.4-12MHz Crystal or Ceramic for main clock
  - 32.768kHz Crystal for sub clock
  - Phase locked loop (Max. 16.4MHz with sub clock)
- **Package Type**
  - 80 LQFP-1212
  - 64 LQFP-1010
  - 64 LQFP-1414
  - Pb-free package

## 1.3 Ordering Information

**Table 1-1 Ordering Information of MC96F7864S**

| Device name | ROM size | IRAM size | XRAM size | Package |
|---|---|---|---|---|
| MC96F7864SL | 64k bytes FLASH | 256 bytes | 3,072 bytes | 80 LQFP-1212 |
| MC96F7664SL | | | | 64 LQFP-1010 |
| MC96F7664SL14 | | | | 64 LQFP-1414 |

## 1.4 Development Tools

### 1.4.1 Compiler

We do not provide the compiler. Please contact the third parties.

The core of MC96F7864S is Mentor 8051. And, device ROM size is smaller than 64k bytes. Developer can use all kinds of third party's standard 8051 compiler.

### 1.4.2 OCD emulator and debugger

The OCD (On Chip Debug) emulator supports ABOV Semiconductor's 8051 series MCU emulation.

The OCD interface uses two-wire interfacing between PC and MCU which is attached to user's system. The OCD can read or change the value of MCU internal memory and I/O peripherals. And the OCD also controls MCU internal debugging logic, it means OCD controls emulation, step run, monitoring, etc.

The OCD Debugger program works on Microsoft-Windows NT, 2000, XP, Vista (32bit) operating system.

If you want to see more details, please refer to OCD debugger manual. You can download debugger S/W and manual from our web-site.

Connection:

- DSCL (MC96F7864S P14 port)
- DSDA (MC96F7864S P15 port)

OCD connector diagram: Connect OCD with user system

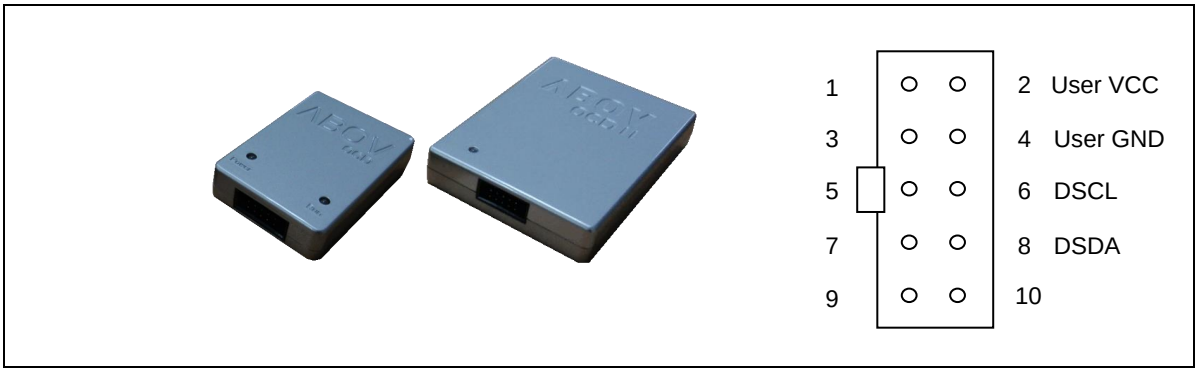



**Figure 1.2 Debugger(OCD1/OCD2) and Pin description**

### 1.4.3 Programmer

Single programmer:

E-PGM+ : It programs MCU device directly.

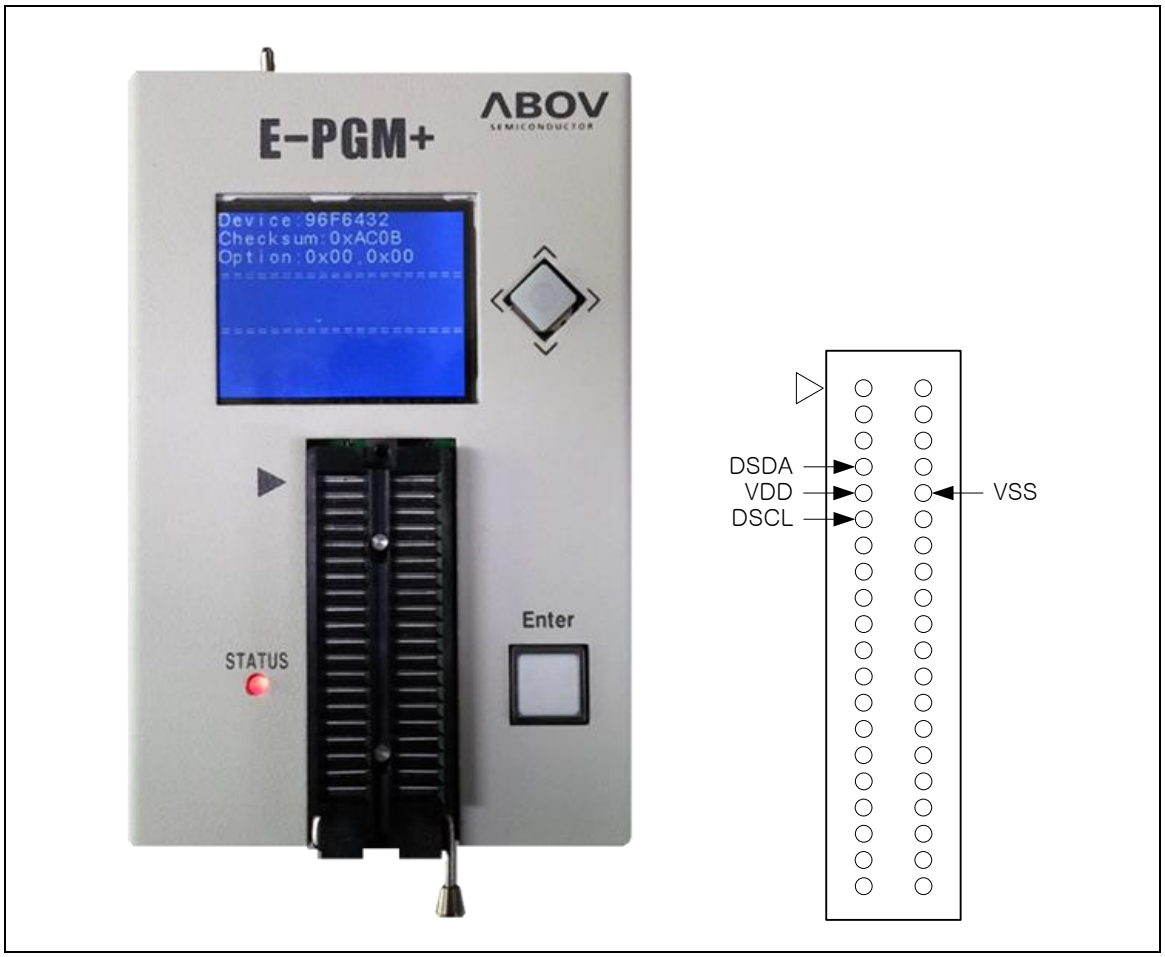



**Figure 1.3 E-PGM+(Single writer)**

OCD emulator: It can write code in MCU device too, because OCD debugging supports ISP (In System Programming).

It does not require additional H/W, except developer's target system.

Gang programmer: E-GANG4 and E-GANG6

- It can run PC controlled mode.
- It can run standalone without PC control too.
- USB interface is supported.
- Easy to connect to the handler.

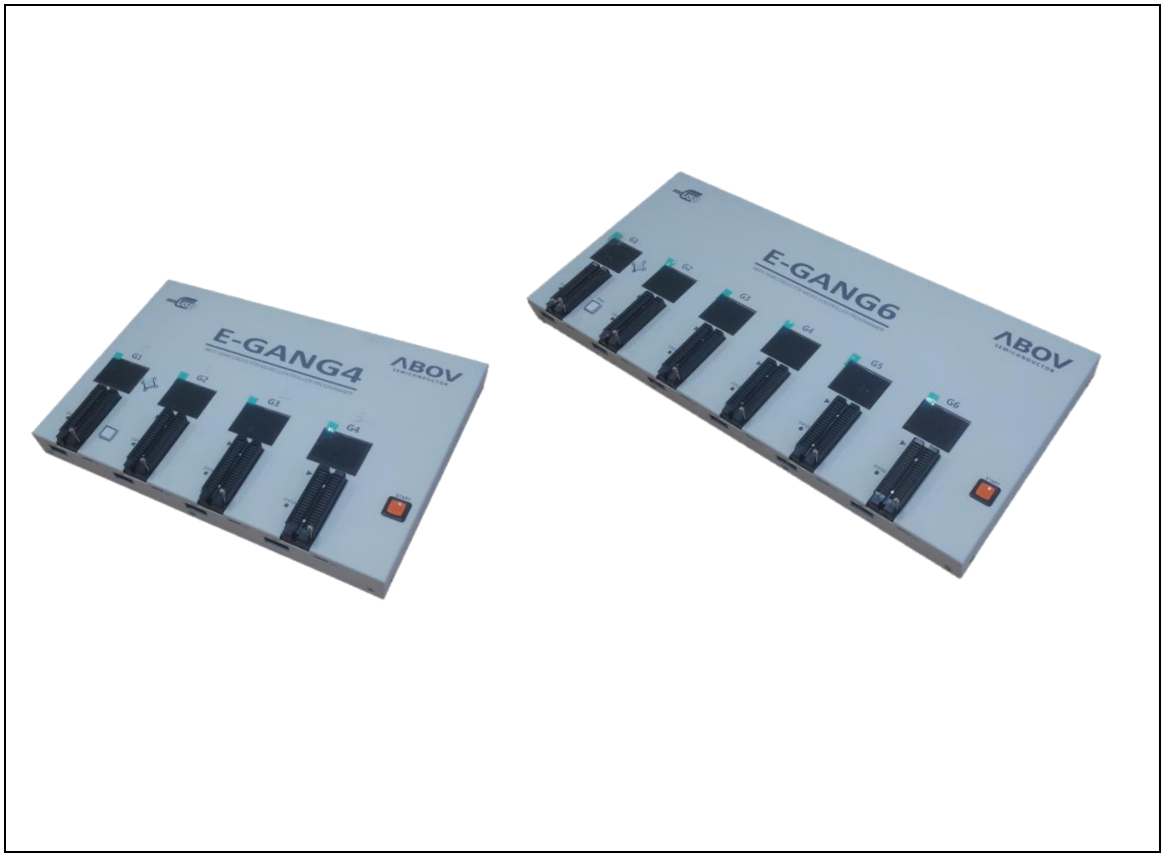



**Figure 1.4 E-GANG4 and E-GANG6 (for Mass Production)**

## 2. Block Diagram

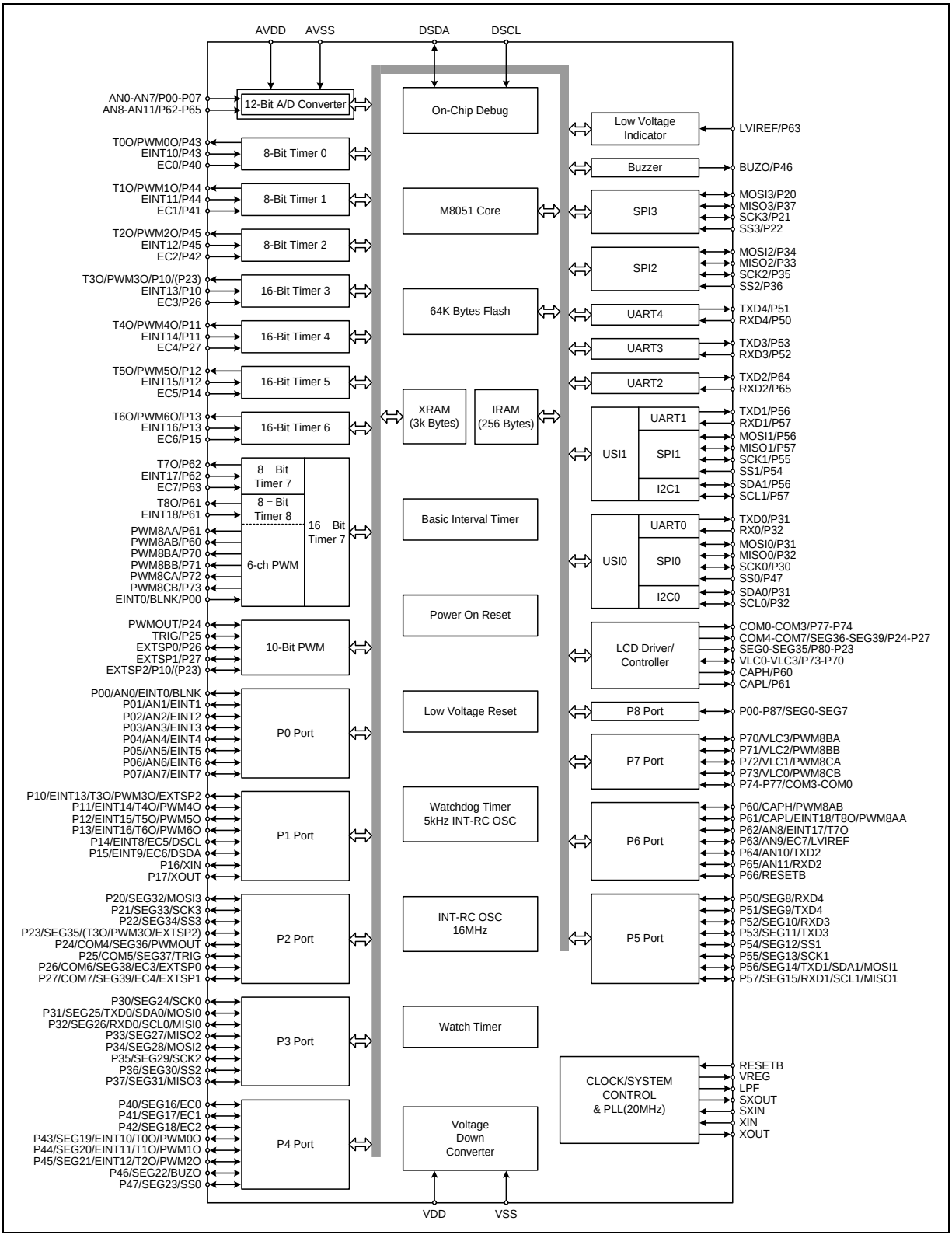



**Figure 2.1 Block Diagram**

NOTE) The P06-P07, P20-P23, P36-P37, and P8 are not in the 64-pin package.

## 3. Pin Assignment

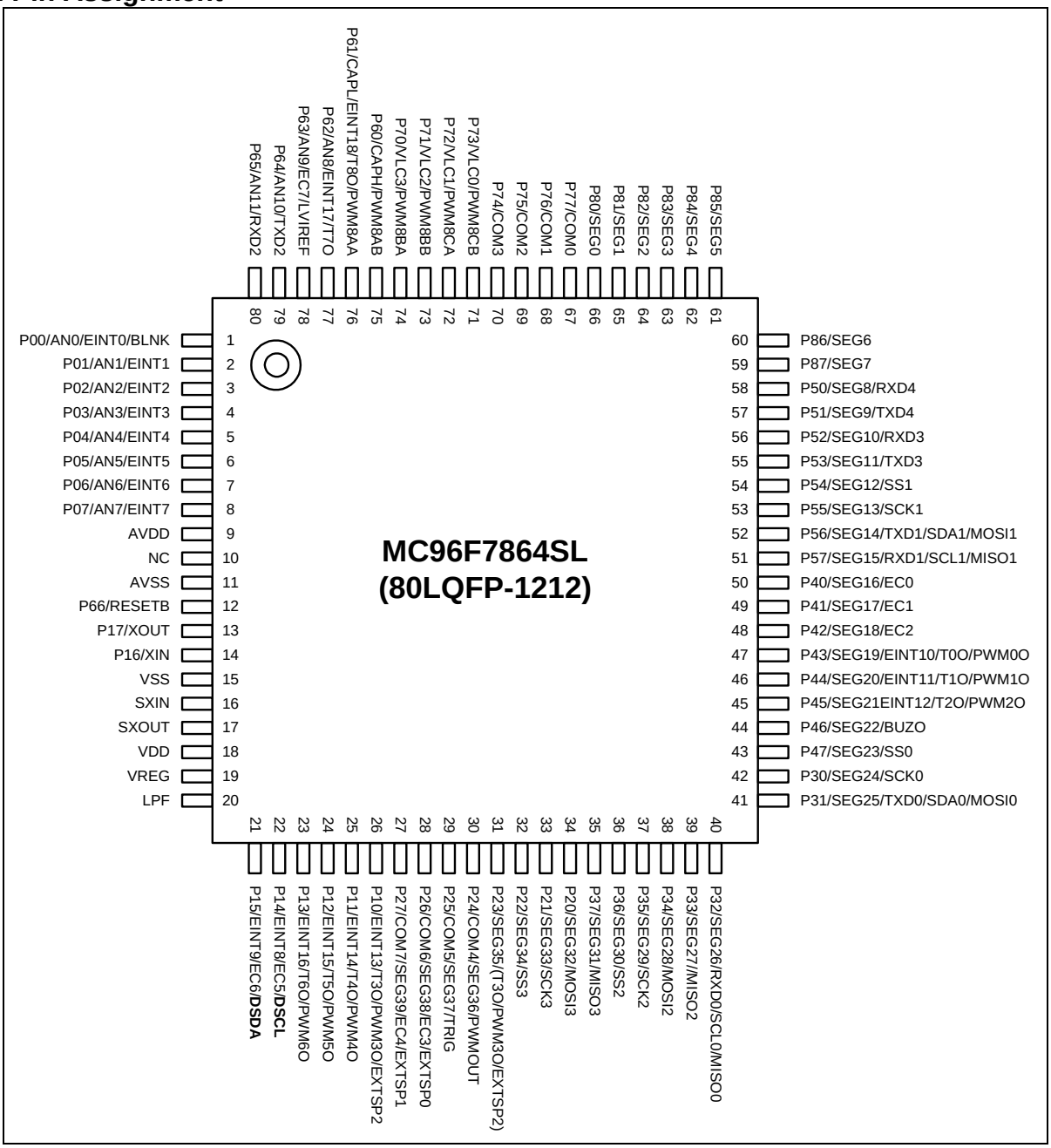



**Figure 3.1 MC96F7864SL 80LQFP-1212 Pin Assignment**

NOTES) 1. On On-Chip Debugging, ISP uses P1[5:4] pin as DSDA, DSCL.
2. The pin in parentheses can be configured by software control.

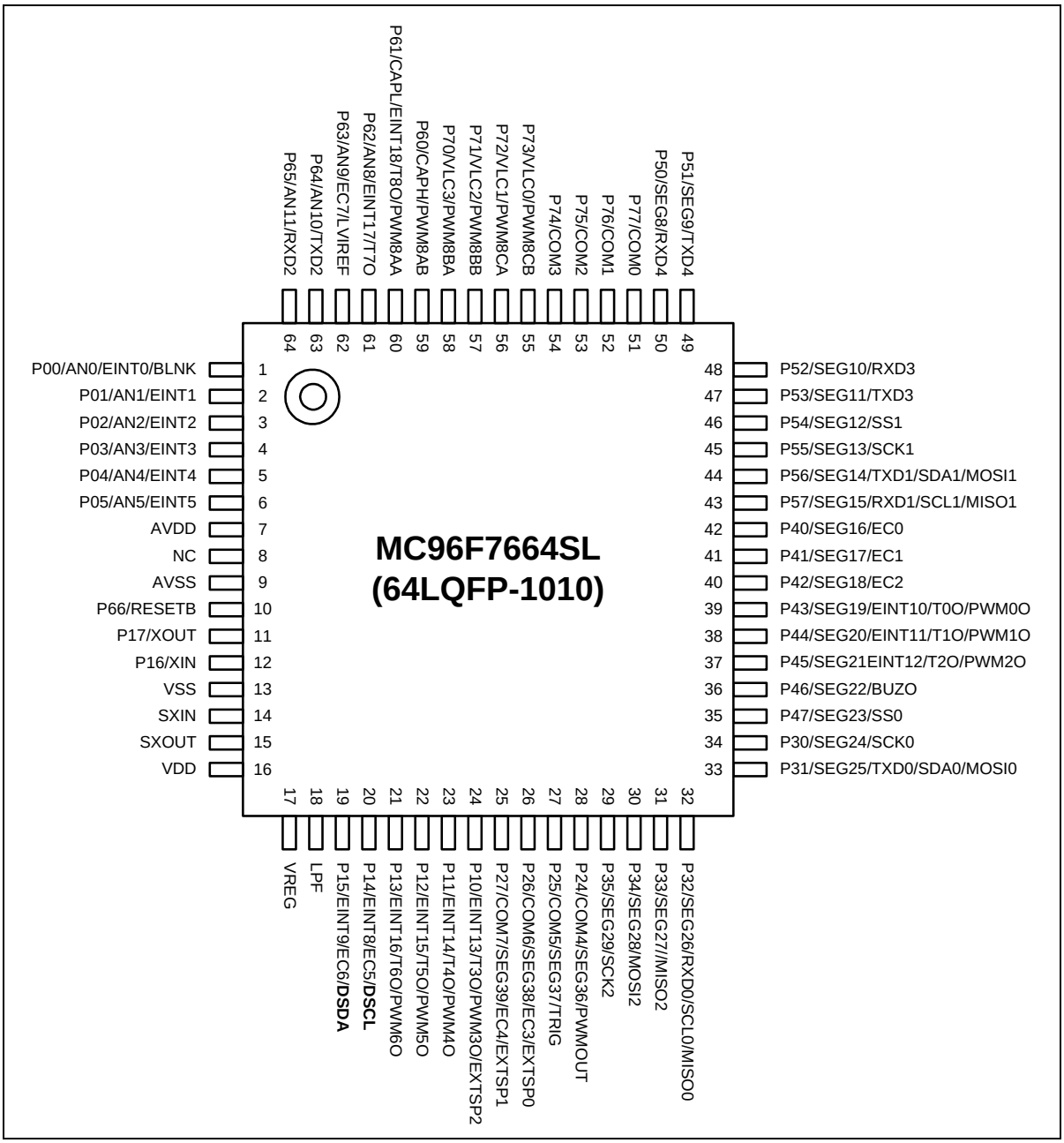



**Figure 3.2 MC96F7664SL 64LQFP-1010 Pin Assignment**

NOTES) 1. On On-Chip Debugging, ISP uses P1[5:4] pin as DSDA, DSCL.
2. The P06-P07, P20-P23, P36-P37, and P8 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 64-pin package is used.

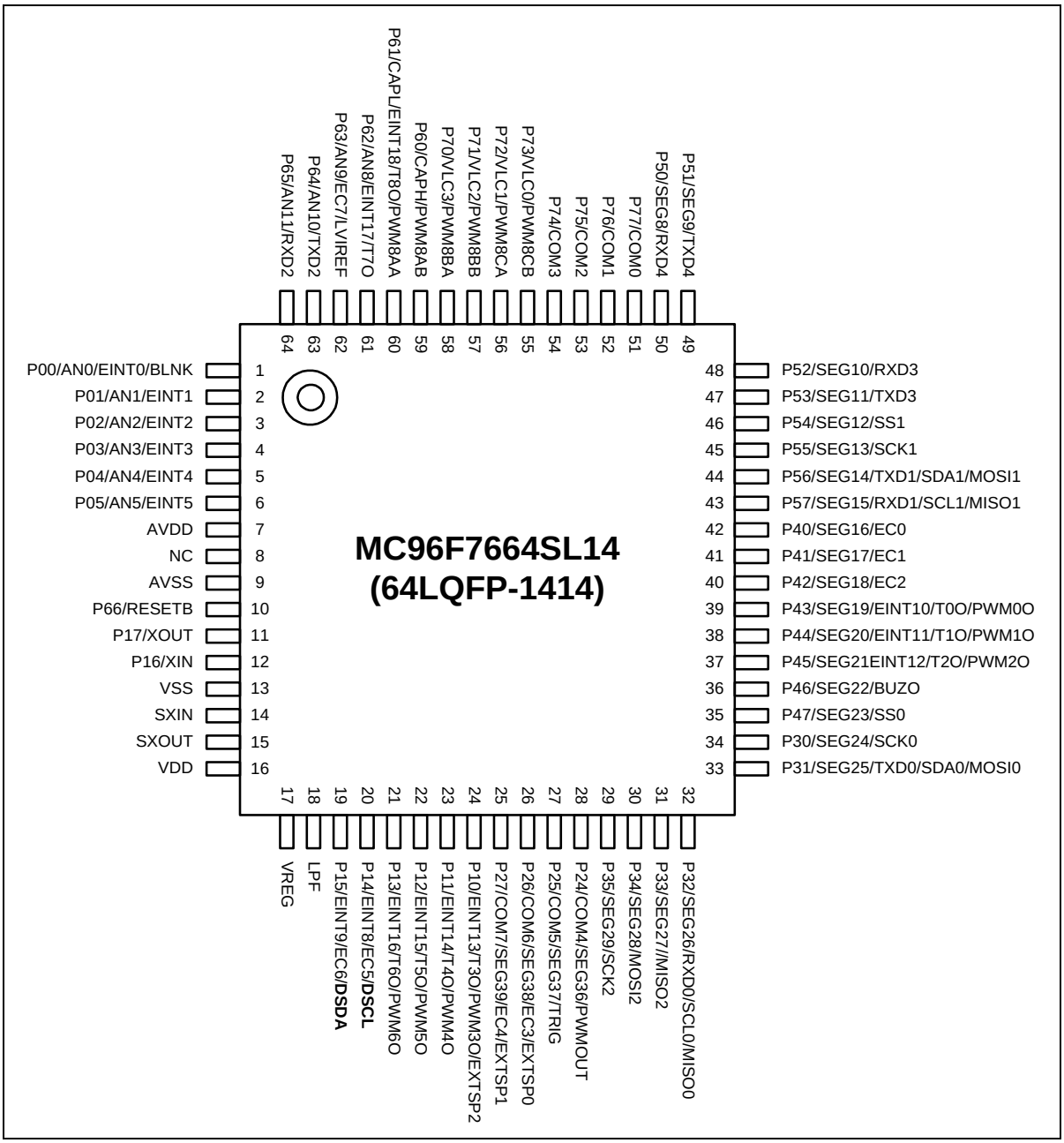
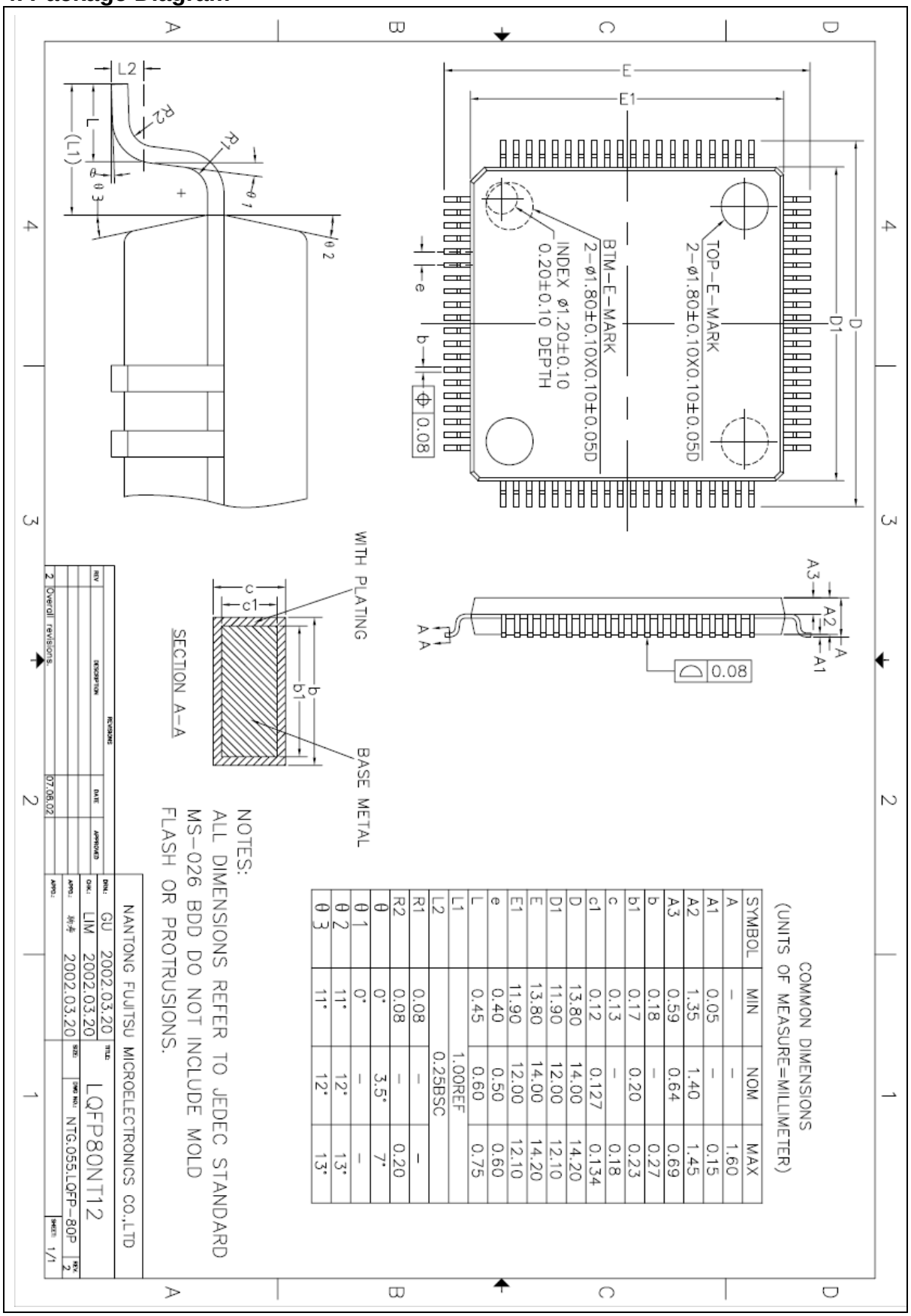



**Figure 3.3 MC96F7664SL14 64LQFP-1414 Pin Assignment**

NOTES) 1. On On-Chip Debugging, ISP uses P1[5:4] pin as DSDA, DSCL.
2. The P06-P07, P20-P23, P36-P37, and P8 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 64-pin package is used.

## 4. Package Diagram




COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | – | – | 1.60 |
| A1 | 0.05 | – | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | – | 0.27 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | – | 0.18 |
| c1 | 0.12 | 0.127 | 0.134 |
| D | 13.80 | 14.00 | 14.20 |
| D1 | 11.90 | 12.00 | 12.10 |
| E | 13.80 | 14.00 | 14.20 |
| E1 | 11.90 | 12.00 | 12.10 |
| e | 0.40 | 0.50 | 0.60 |
| L | 0.45 | 0.60 | 0.75 |
| L1 | | 1.00REF | |
| L2 | | 0.25BSC | |
| R1 | 0.08 | – | – |
| R2 | 0.08 | – | 0.20 |
| θ | 0° | 3.5° | 7° |
| θ1 | 0° | – | – |
| θ2 | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° |

**Figure 4.1 80-Pin LQFP-1212 Package (Ass'y site: NFME)**

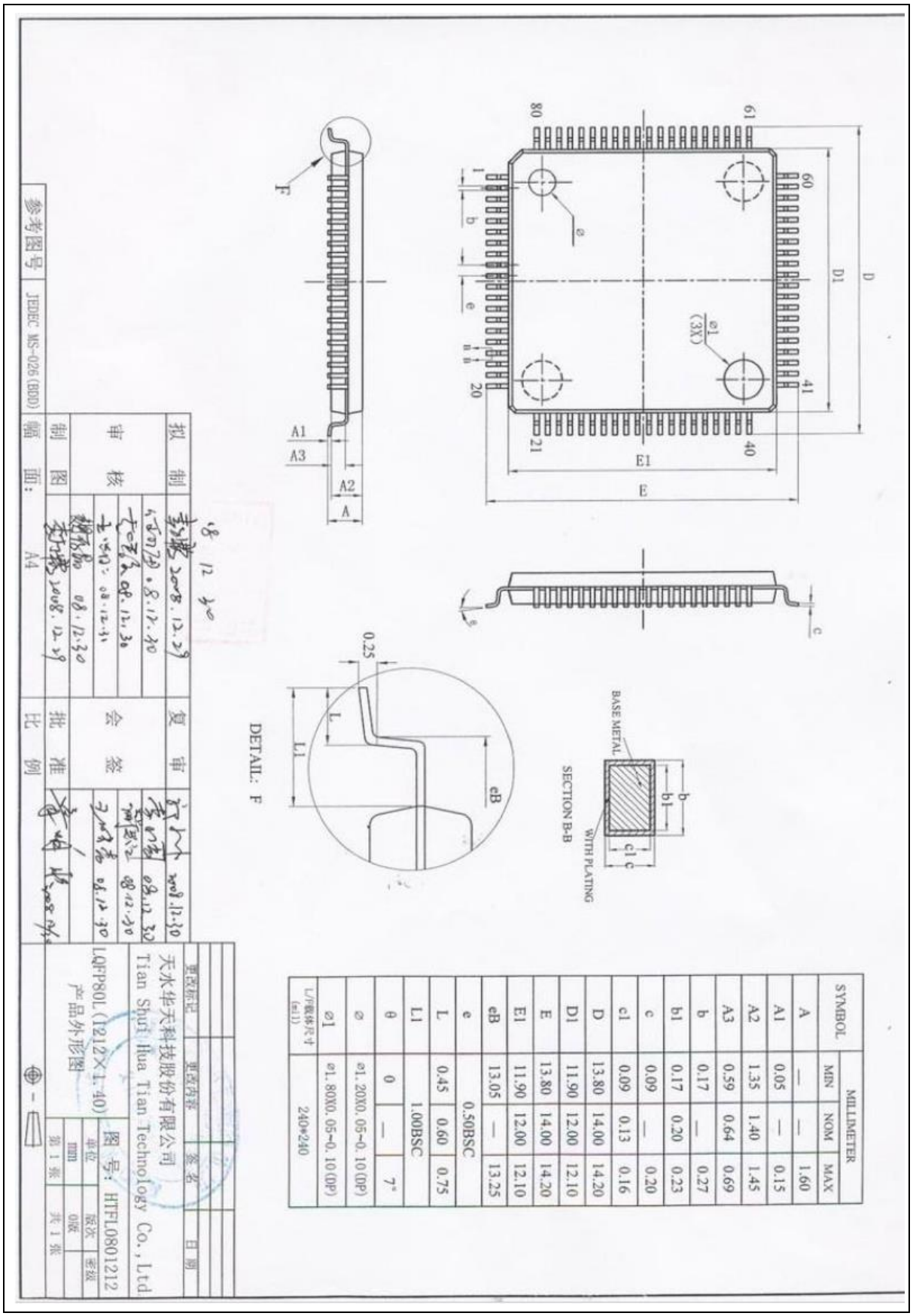
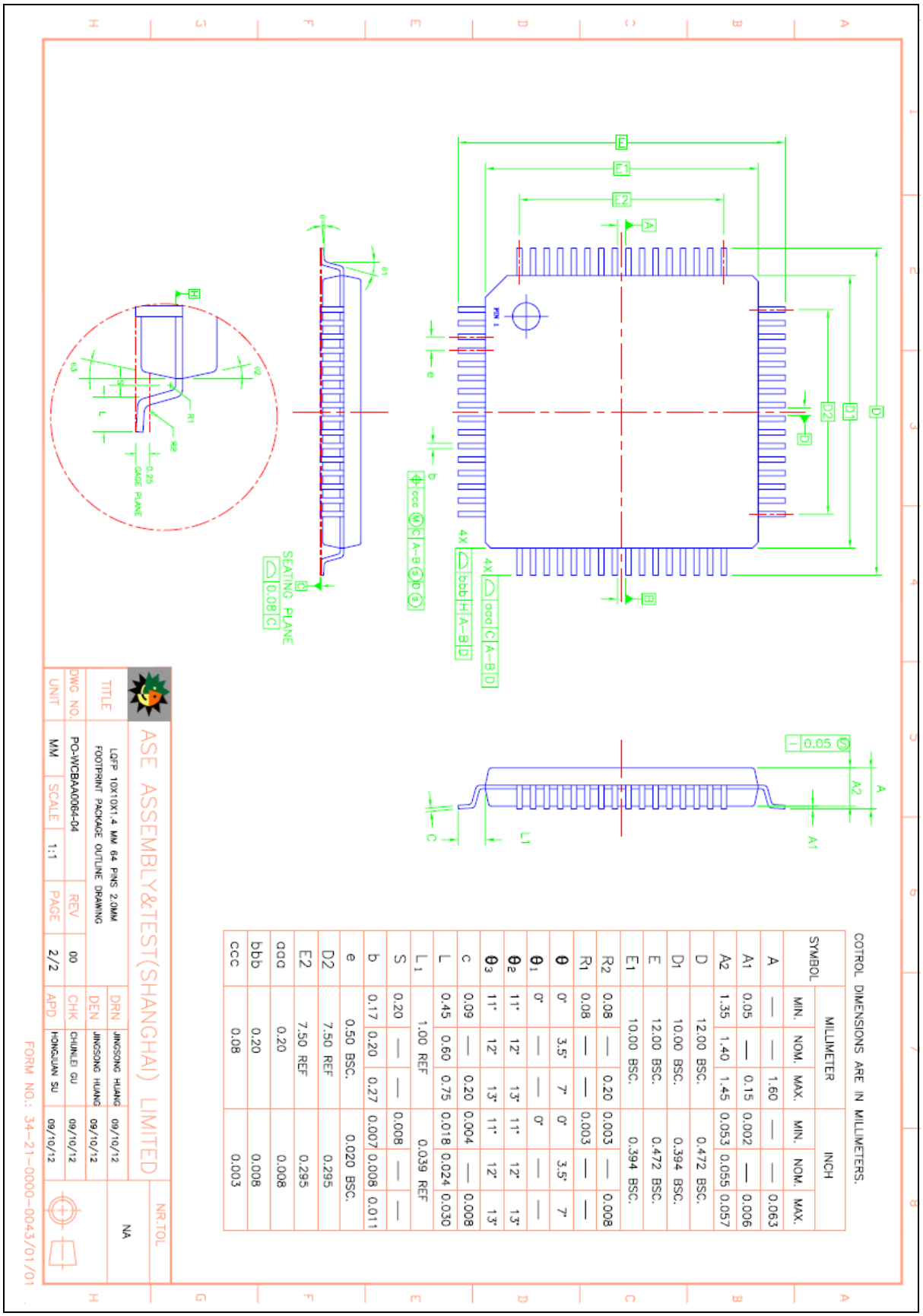


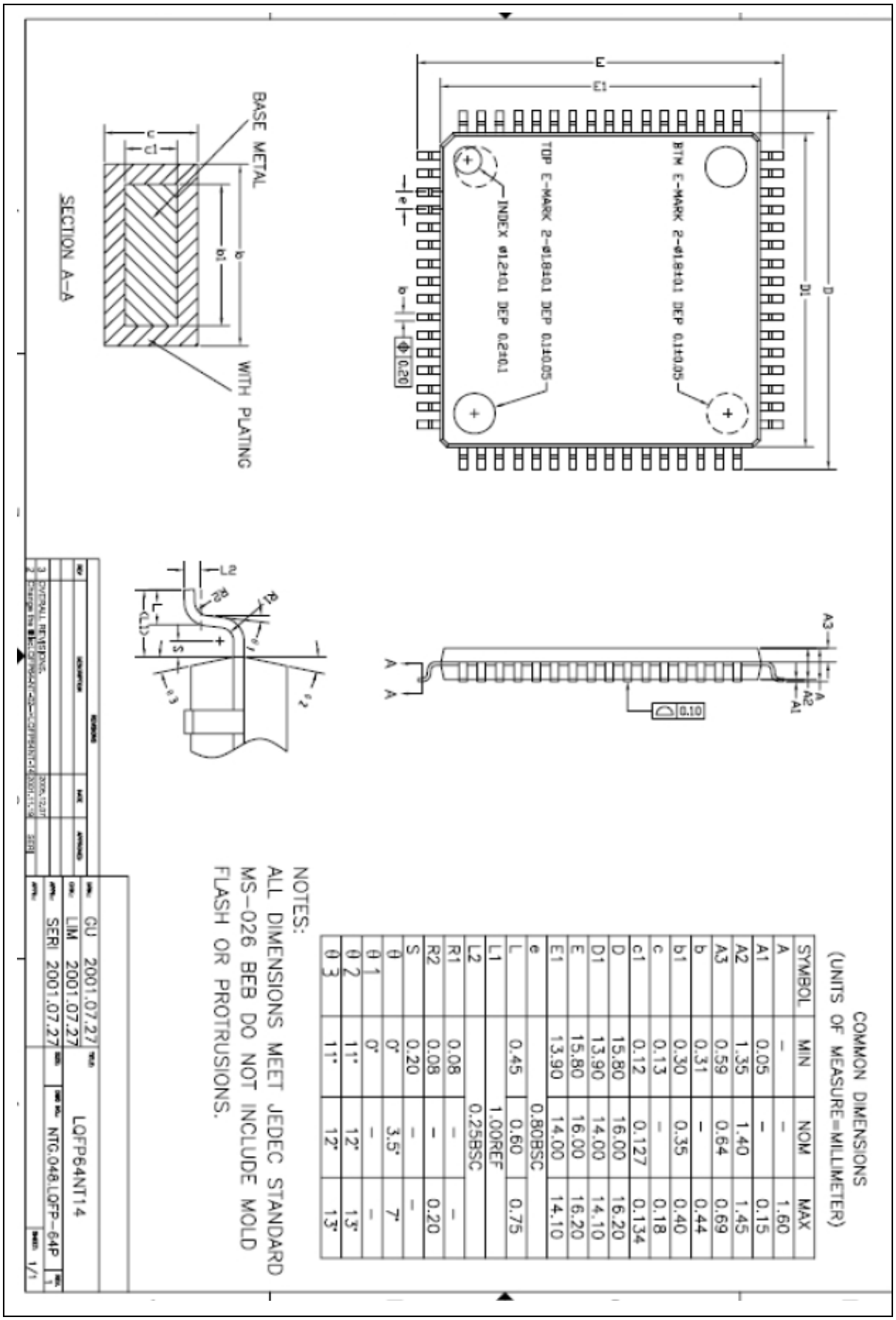

**Figure 4.2 80-Pin LQFP-1212 Package (Ass'y site: TSHT)**




COTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.60 | — | — | 0.063 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | 12.00 BSC. | | | 0.472 BSC. | | |
| D1 | 10.00 BSC. | | | 0.394 BSC. | | |
| E | 12.00 BSC. | | | 0.472 BSC. | | |
| E1 | 10.00 BSC. | | | 0.394 BSC. | | |
| R2 | 0.08 | — | 0.20 | 0.003 | — | 0.008 |
| R1 | 0.08 | — | — | 0.003 | — | — |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | — | — | 0° | — | — |
| θ2 | 11° | 12° | 13° | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| S | 0.20 | — | — | 0.008 | — | — |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 |
| e | 0.50 BSC. | | | 0.020 BSC. | | |
| D2 | 7.50 REF | | | 0.295 | | |
| E2 | 7.50 REF | | | 0.295 | | |
| aaa | 0.20 | | | 0.008 | | |
| bbb | 0.20 | | | 0.008 | | |
| ccc | 0.08 | | | 0.003 | | |

**Figure 4.3 64-Pin LQFP-1010 Package**




COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | – | – | 1.60 |
| A1 | 0.05 | – | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.31 | – | 0.44 |
| b1 | 0.30 | 0.35 | 0.40 |
| c | 0.13 | – | 0.18 |
| c1 | 0.12 | 0.127 | 0.134 |
| D | 15.80 | 16.00 | 16.20 |
| D1 | 13.90 | 14.00 | 14.10 |
| E | 15.80 | 16.00 | 16.20 |
| E1 | 13.90 | 14.00 | 14.10 |
| e | | 0.80BSC | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | | 1.00REF | |
| L2 | | 0.25BSC | |
| R1 | 0.08 | – | – |
| R2 | 0.08 | – | 0.20 |
| S | 0.20 | – | – |
| θ | 0° | 3.5° | 7° |
| θ1 | 0° | – | – |
| θ2 | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° |

**Figure 4.4 64-Pin LQFP-1414 Package**

# 5. Pin Description

**Table 5-1 Normal Pin Description**

| PIN Name | I/O | Function | @RESET | Shared with |
|---|---|---|---|---|
| P00 | I/O | Port 0 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output.<br>A pull-up resistor can be specified in 1-bit unit.<br>The P06-P07 are not in the 64-Pin package. | Input | AN0/EINT0/BLNK |
| P01 | | | | AN1/EINT1 |
| P02 | | | | AN2/EINT2 |
| P03 | | | | AN3/EINT3 |
| P04 | | | | AN4/EINT4 |
| P05 | | | | AN5/EINT5 |
| P06 | | | | AN6/EINT6 |
| P07 | | | | AN7/EINT7 |
| P10 | I/O | Port 1 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output.<br>A pull-up resistor can be specified in 1-bit unit. | Input | EINT13/T3O/PWM3O/EXTSP2 |
| P11 | | | | EINT14/T4O/PWM4O |
| P12 | | | | EINT15/T5O/PWM5O |
| P13 | | | | EINT16/T6O/PWM6O |
| P14 | | | | EINT8/EC5/DSCL |
| P15 | | | | EINT9/EC6/DSDA |
| P16 | | | | XIN |
| P17 | | | | XOUT |
| P20 | I/O | Port 2 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output.<br>A pull-up resistor can be specified in 1-bit unit.<br>The P20 – P23 are not in the 64-pin package. | Input | SEG32/MOSI3 |
| P21 | | | | SEG33/SCK3 |
| P22 | | | | SEG34/SS3 |
| P23 | | | | SEG35/(T3O/PWM3O/EXTSP2) |
| P24 | | | | COM4/SEG36/PWMOUT |
| P25 | | | | COM5/SEG37/TRIG |
| P26 | | | | COM6/SEG38/EC3/EXTSP0 |
| P27 | | | | COM7/SEG39/EC4/EXTSP1 |
| P30 | I/O | Port 3 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output.<br>A pull-up resistor can be specified in 1-bit unit.<br>The P36-P37 are not in the 64-Pin package. | Input | SEG24/SCK0 |
| P31 | | | | SEG25/TXD0/SDA0/MOSI0 |
| P32 | | | | SEG26/RXD0/SCL0/MISO0 |
| P33 | | | | SEG27/MISO2 |
| P34 | | | | SEG28/MOSI2 |
| P35 | | | | SEG29/SCK2 |
| P36 | | | | SEG30/SS2 |
| P37 | | | | SEG31/MISO3 |
| P40 | I/O | Port 4 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output.<br>A pull-up resistor can be specified in 1-bit unit. | Input | SEG16/EC0 |
| P41 | | | | SEG17/EC1 |
| P42 | | | | SEG18/EC2 |
| P43 | | | | SEG19/EINT10/T0O/PWM0O |
| P44 | | | | SEG20/EINT11/T1O/PWM1O |
| P45 | | | | SEG21/EINT12/T2O/PWM2O |
| P46 | | | | SEG22/BUZO |
| P47 | | | | SEG23/SS0 |

**Table 5-1 Normal Pin Description (Continued)**

| PIN Name | I/O | Function | @RESET | Shared with |
|---|---|---|---|---|
| P50 | I/O | Port 5 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output.<br>A pull-up resistor can be specified in 1-bit unit. | Input | SEG8/RXD4 |
| P51 | | | | SEG9/TXD4 |
| P52 | | | | SEG10/RXD3 |
| P53 | | | | SEG11/TXD3 |
| P54 | | | | SEG12/SS1 |
| P55 | | | | SEG13/SCK1 |
| P56 | | | | SEG14/TXD1/SDA1/MOSI1 |
| P57 | | | | SEG15/RXD1/SCL1/MISO1 |
| P60 | I/O | Port 6 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output.<br>A pull-up resistor can be specified in 1-bit unit. | Input | CAPH/PWM8AB |
| P61 | | | | CAPL/EINT18/T8O/PWM8AA |
| P62 | | | | AN8/EINT17/T7O |
| P63 | | | | AN9/EC7/LVIREF |
| P64 | | | | AN10/TXD2 |
| P65 | | | | AN11/RXD2 |
| P66 | | | | RESETB |
| P70 | I/O | Port 7 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output.<br>A pull-up resistor can be specified in 1-bit unit. | Input | VLC3/PWM8BA |
| P71 | | | | VLC2/PWM8BB |
| P72 | | | | VLC1/PWM8CA |
| P73 | | | | VLC0/PWM8CB |
| P74 | | | | COM3 |
| P75 | | | | COM2 |
| P76 | | | | COM1 |
| P77 | | | | COM0 |
| P80 | I/O | Port 8 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output.<br>A pull-up resistor can be specified in 1-bit unit.<br>The P8 is not in the 64-Pin package. | Input | SEG0 |
| P81 | | | | SEG1 |
| P82 | | | | SEG2 |
| P83 | | | | SEG3 |
| P84 | | | | SEG4 |
| P85 | | | | SEG5 |
| P86 | | | | SEG6 |
| P87 | | | | SEG7 |
| EINT0 | I/O | External interrupt inputs | Input | P00/AN0/BLNK |
| EINT1 | | | | P01/AN1 |
| EINT2 | | | | P02/AN2 |
| EINT3 | | | | P03/AN3 |
| EINT4 | | | | P04/AN4 |
| EINT5 | | | | P05/AN5 |
| EINT6 | | | | P06/AN6 |
| EINT7 | | | | P07/AN7 |
| EINT8 | | | | P14/EC5/DSCL |
| EINT9 | | | | P15/EC6/DSDA |
| EINT10 | I/O | External interrupt and Timer 0 capture input | Input | P43/SEG19/T0O/PWM0O |
| EINT11 | I/O | External interrupt and Timer 1 capture input | Input | P44/SEG20/T1O/PWM1O |

| | | | | |
|---|---|---|---|---|
| EINT12 | I/O | External interrupt and Timer 2 capture input | Input | P45/SEG21/T2O/PWM2O |

**Table 5-1 Normal Pin Description (Continued)**

| PIN Name | I/O | Function | @RESET | Shared with |
|---|---|---|---|---|
| EINT13 | I/O | External interrupt and Timer 3 capture input | Input | P10/T3O/PWM3O/EXTSP2 |
| EINT14 | I/O | External interrupt and Timer 4 capture input | Input | P11/T4O/PWM4O |
| EINT15 | I/O | External interrupt and Timer 5 capture input | Input | P12/T5O/PWM5O |
| EINT16 | I/O | External interrupt and Timer 6 capture input | Input | P13/T6O/PWM6O |
| EINT17 | I/O | External interrupt and Timer 7 capture input | Input | P62/AN8/T7O |
| EINT18 | I/O | External interrupt and Timer 8 capture input | Input | P61/CAPL/T8O/PWM8AA |
| T0O | I/O | Timer 0 interval output | Input | P43/SEG19/EINT10/PWM0O |
| T1O | I/O | Timer 1 interval output | Input | P44/SEG20/EINT11/PWM1O |
| T2O | I/O | Timer 2 interval output | Input | P45/SEG21/EINT12/PWM2O |
| T3O | I/O | Timer 3 interval output | Input | P10/EINT13/PWM3O/EXTSP2 |
| T4O | I/O | Timer 4 interval output | Input | P11/EINT14/PWM4O |
| T5O | I/O | Timer 5 interval output | Input | P12/EINT15/PWM5O |
| T6O | I/O | Timer 6 interval output | Input | P13/EINT16/PWM6O |
| T7O | I/O | Timer 7 interval output | Input | P62/AN8/EINT17 |
| T8O | I/O | Timer 8 interval output | Input | P61/CAPL/EINT18/PWM8AA |
| PWM0O | I/O | Timer 0 PWM output | Input | P43/SEG19/EINT10/T0O |
| PWM1O | I/O | Timer 1 PWM output | Input | P44/SEG20/EINT11/T1O |
| PWM2O | I/O | Timer 2 PWM output | Input | P45/SEG21/EINT12/T2O |
| PWM3O | I/O | Timer 3 pulse output | Input | P10/EINT13/T3O/EXTSP2 |
| PWM4O | I/O | Timer 4 pulse output | Input | P11/EINT14/T4O |
| PWM5O | I/O | Timer 5 pulse output | Input | P12/EINT15/T5O |
| PWM6O | I/O | Timer 6 pulse output | Input | P13/EINT16/T6O |
| PWM8AA | I/O | Timer 8's 6-ch PWM outputs | Input | P61/CAPL/EINT18/T8O |
| PWM8AB | | | | P60/CAPH |
| PWM8BA | | | | P70/VLC3 |
| PWM8BB | | | | P71/VLC2 |
| PWM8CA | | | | P72/VLC1 |
| PWM8CB | | | | P73/VLC0 |
| BLNK | I/O | External sync signal input for 6-ch PWMs | Input | P00/AN0/EINT0 |
| EC0 | I/O | Timer 0 event count input | Input | P40/SEG16 |
| EC1 | I/O | Timer 1 event count input | Input | P41/SEG17 |
| EC2 | I/O | Timer 2 event count input | Input | P42/SEG18 |
| EC3 | I/O | Timer 3 event count input | Input | P26/COM6/SEG38/EXTSP0 |
| EC4 | I/O | Timer 4 event count input | Input | P27/COM7/SEG39/EXTSP1 |
| EC5 | I/O | Timer 5 event count input | Input | P14/EINT8/DSCL |
| EC6 | I/O | Timer 6 event count input | Input | P15/EINT9/DSDA |
| EC7 | I/O | Timer 7 event count input | Input | P63/AN9/LVIREF |
| SCK0 | I/O | Serial 0 clock input/output | Input | P30/SEG24 |

| | | | | |
|---|---|---|---|---|
| SCK1 | I/O | Serial 1 clock input/output | Input | P55/SEG13 |
| SCK2 | I/O | Serial 2 clock input/output | Input | P35/SEG29 |
| SCK3 | I/O | Serial 3 clock input/output | Input | P21/SEG33 |

**Table 5-1 Normal Pin Description (Continued)**

| PIN Name | I/O | Function | @RESET | Shared with |
|---|---|---|---|---|
| MOSI0 | I/O | Serial 0 data input/output | Input | P31/SEG25/TXD0/SDA0 |
| MOSI1 | I/O | Serial 1 data input/output | Input | P56/SEG14/TXD1/SDA1 |
| MOSI2 | I/O | Serial 2 data input/output | Input | P34/SEG28 |
| MOSI3 | I/O | Serial 3 data input/output | Input | P20/SEG32 |
| MISO0 | I/O | Serial 0 data input/output | Input | P32/SEG26/RXD0/SCL0 |
| MISO1 | I/O | Serial 1 data input/output | Input | P57/SEG15/RXD1/SCL1 |
| MISO2 | I/O | Serial 2 data input/output | Input | P33/SEG27 |
| MISO3 | I/O | Serial 3 data input/output | Input | P37/SEG31 |
| SS0 | I/O | Slave 0 select input | Input | P47/SEG23 |
| SS1 | I/O | Slave 1 select input | Input | P54/SEG12 |
| SS2 | I/O | Slave 2 select input | Input | P36/SEG30 |
| SS3 | I/O | Slave 3 select input | Input | P22/SEG34 |
| TXD0 | I/O | UART 0 data output | Input | P31/SEG25/SDA0/MOSI0 |
| TXD1 | I/O | UART 1 data output | Input | P56/SEG14/SDA1/MOSI1 |
| TXD2 | I/O | UART 2 data output | Input | P64/AN10 |
| TXD3 | I/O | UART 3 data output | Input | P53/SEG11 |
| TXD4 | I/O | UART 4 data output | Input | P51/SEG9 |
| RXD0 | I/O | UART 0 data input | Input | P32/SEG26/SCL0/MISO0 |
| RXD1 | I/O | UART 1 data input | Input | P57/SEG15/SCL1/MISO1 |
| RXD2 | I/O | UART 2 data input | Input | P65/AN11 |
| RXD3 | I/O | UART 3 data input | Input | P52/SEG10 |
| RXD4 | I/O | UART 4 data input | Input | P50/SEG8 |
| SCL0 | I/O | I2C 0 clock input/output | Input | P32/SEG26/RXD0/MISO0 |
| SCL1 | I/O | I2C 1 clock input/output | Input | P57/SEG15/RXD1/MISO1 |
| SDA0 | I/O | I2C 0 data input/output | Input | P31/SEG25/TXD0/MOSI0 |
| SDA1 | I/O | I2C 1 data input/output | Input | P56/SEG14/TXD1/MOSI1 |
| BUZO | I/O | Buzzer signal output | Input | P46/SEG22 |
| AN0 | I/O | A/D converter analog input channels | Input | P00/EINT0/BLNK |
| AN1 | | | | P01/EINT1 |
| AN2 | | | | P02/EINT2 |
| AN3 | | | | P03/EINT3 |
| AN4 | | | | P04/EINT4 |
| AN5 | | | | P05/EINT5 |
| AN6 | | | | P06/EINT6 |
| AN7 | | | | P07/EINT7 |
| AN8 | | | | P62/EINT17/T7O |
| AN9 | | | | P63/EC7/LVIREF |
| AN10 | | | | P64/TXD2 |
| AN11 | | | | P65/RXD2 |
| LVIREF | I/O | Low voltage indicator reference voltage | Input | P63/AN9/EC7 |

**Table 5-1 Normal Pin Description (Continued)**

| PIN Name | I/O | Function | @RESET | Shared with |
|---|---|---|---|---|
| VLC0 | I/O | LCD bias voltage pins | Input | P73/PWM8CB |
| VLC1 | | | | P72/PWM8CA |
| VLC2 | | | | P71/PWM8BB |
| VLC3 | | | | P70/PWM8BA |
| CAPH | I/O | Capacitor terminals for voltage booster | Input | P60/PWM8AB |
| CAPL | | | | P61/EINT18/T8O/PWM8AA |
| COM0–COM3 | I/O | LCD common signal outputs | Input | P77–P74 |
| COM4 | | | | P24/SEG36/PWMOUT |
| COM5 | | | | P25/SEG37/TRIG |
| COM6 | | | | P26/SEG38/EC3/EXTSP0 |
| COM7 | | | | P27/SEG39/EC4/EXTSP1 |
| SEG0–SEG7 | I/O | LCD segment signal outputs | Input | P80–P87 |
| SEG8 | | | | P50/RXD4 |
| SEG9 | | | | P51/TXD4 |
| SEG10 | | | | P52/RXD3 |
| SEG11 | | | | P53/TXD3 |
| SEG12 | | | | P54/SS1 |
| SEG13 | | | | P55/SCK1 |
| SEG14 | | | | P56/TXD1/SDA1/MOSI1 |
| SEG15 | | | | P57/RXD1/SCL1/MISO1 |
| SEG16–SEG18 | | | | P40–P42/EC0–EC2 |
| SEG19 | | | | P43/EINT10/T0O/PWM0O |
| SEG20 | | | | P44/EINT11/T1O/PWM1O |
| SEG21 | | | | P45/EINT12/T2O/PWM2O |
| SEG22 | | | | P46/BUZO |
| SEG23 | | | | P47/SS0 |
| SEG24 | | | | P30/SCK0 |
| SEG25 | | | | P31/TXD0/SDA0/MOSI0 |
| SEG26 | | | | P32/RXD0/SCL0/MISO0 |
| SEG27 | | | | P33/MISO2 |
| SEG28 | | | | P34/MOSI2 |
| SEG29 | | | | P35/SCK2 |
| SEG30 | | | | P36/SS2 |
| SEG31 | | | | P37/MISO3 |
| SEG32 | | | | P20/MOSI3 |
| SEG33 | | | | P21/SCK3 |
| SEG34 | | | | P22/SS3 |
| SEG35 | | | | P23/(T3O/PWM3O/EXTSP2) |
| SEG36 | | | | P24/COM4/PWMOUT |
| SEG37 | | | | P25/COM5/TRIG |
| SEG38 | | | | P26/COM6/EC3/EXTSP0 |
| SEG39 | | | | P27/COM7/EC4/EXTSP1 |

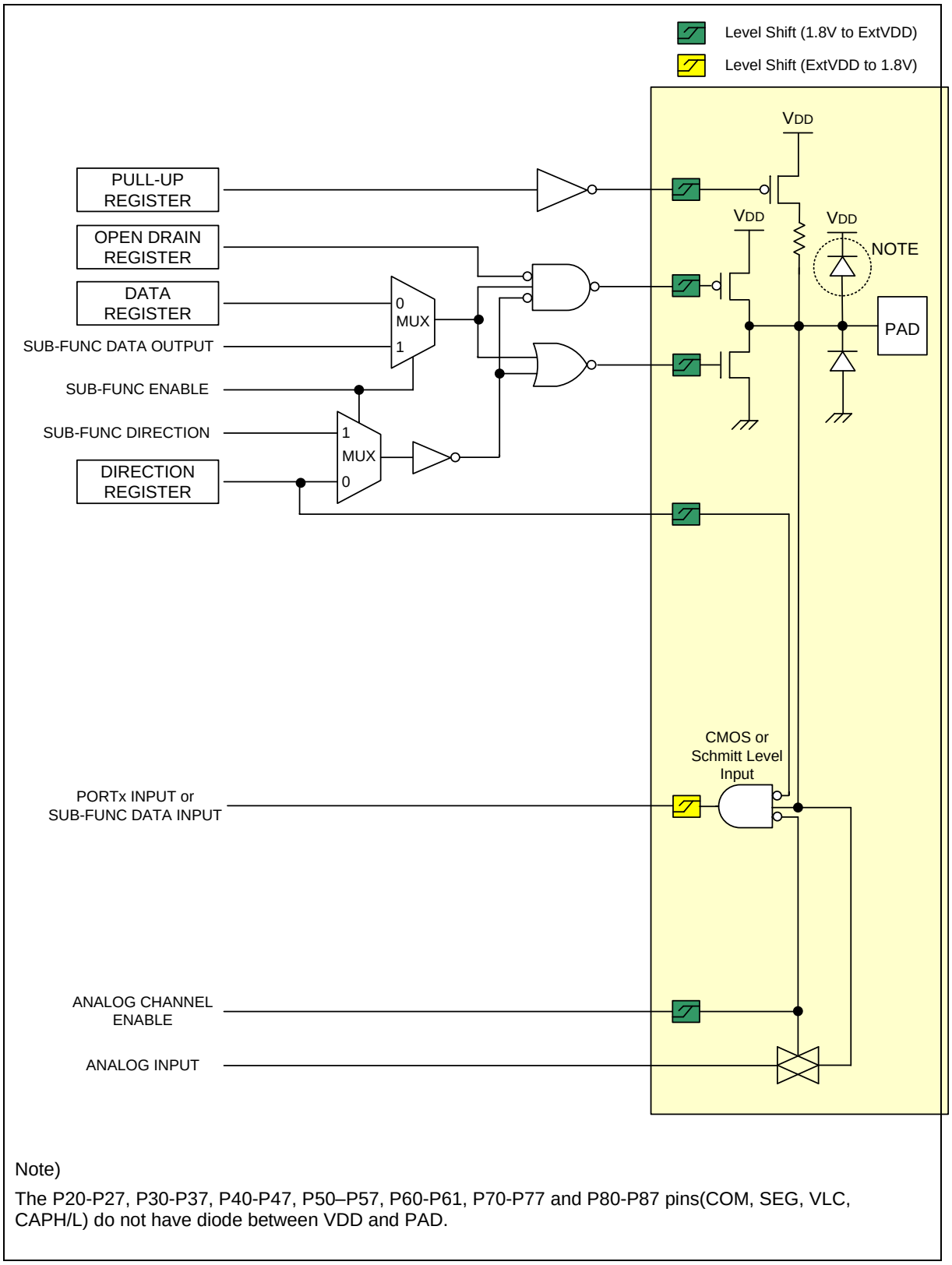
**Table 5-1 Normal Pin Description (Continued)**

| PIN Name | I/O | Function | @RESET | Shared with |
|---|---|---|---|---|
| PWMOUT | I/O | 10-bit PWM output | Input | P24/COM4/SEG36 |
| TRIG | I/O | External trigger input for PWM generator | Input | P25/COM5/SEG37 |
| EXTSP0 | I/O | External shot/emergency stop inputs for PWM generator | Input | P26/COM6/SEG38/EC3 |
| EXTSP1 | | | | P27/COM7/SEG39/EC4 |
| EXTSP2 | | | | P10/EINT13/T3O/PWM3O |
| RESETB | I/O | System reset pin with a pull-up resistor when it is selected as the RESETB by CONFIGURE OPTION | Input | P66 |
| DSDA | I/O | On chip debugger data input/output (NOTE3,4) | Input | P15/EINT9/EC6 |
| DSCL | I/O | On chip debugger clock input (NOTE3,4) | Input | P14/EINT8/EC5 |
| XIN | I/O | Main oscillator pins | Input | P16 |
| XOUT | | | | P17 |
| SXIN | – | Sub oscillator pins | – | – |
| SXOUT | | | | – |
| LPF | – | Loop filter pump output for PLL | – | – |
| VREG | – | Regulator voltage output for sub clock 0.1uF capacitor needed | – | – |
| AVDD, AVSS | – | Analog power input pins | – | – |
| VDD, VSS | – | Digital Power input pins | – | – |

NOTES) 1. The P06-P07, P20-P23, P36-P37, and P8 are not in the 64-Pin package.
2. The P66/RESETB pin is configured as one of the P66 and the RESETB pin by the “CONFIGURE OPTION.”
3. If the P14/EINT8/EC5/DSCL and P15/EINT9/EC6/DSDA pins are connected to an emulator during the reset or power-on reset, the pins are automatically configured as the debugger pins.
4. The P14/EINT8/EC5/DSCL and P15/EINT9/EC6/DSDA pins are configured as inputs with internal pull-up resistors only during the reset or power-on reset.
5. The P17/XOUT and P16/XIN pins are configured as a function pin by software control.

# 6. Port Structures

## 6.1 General Purpose I/O Port

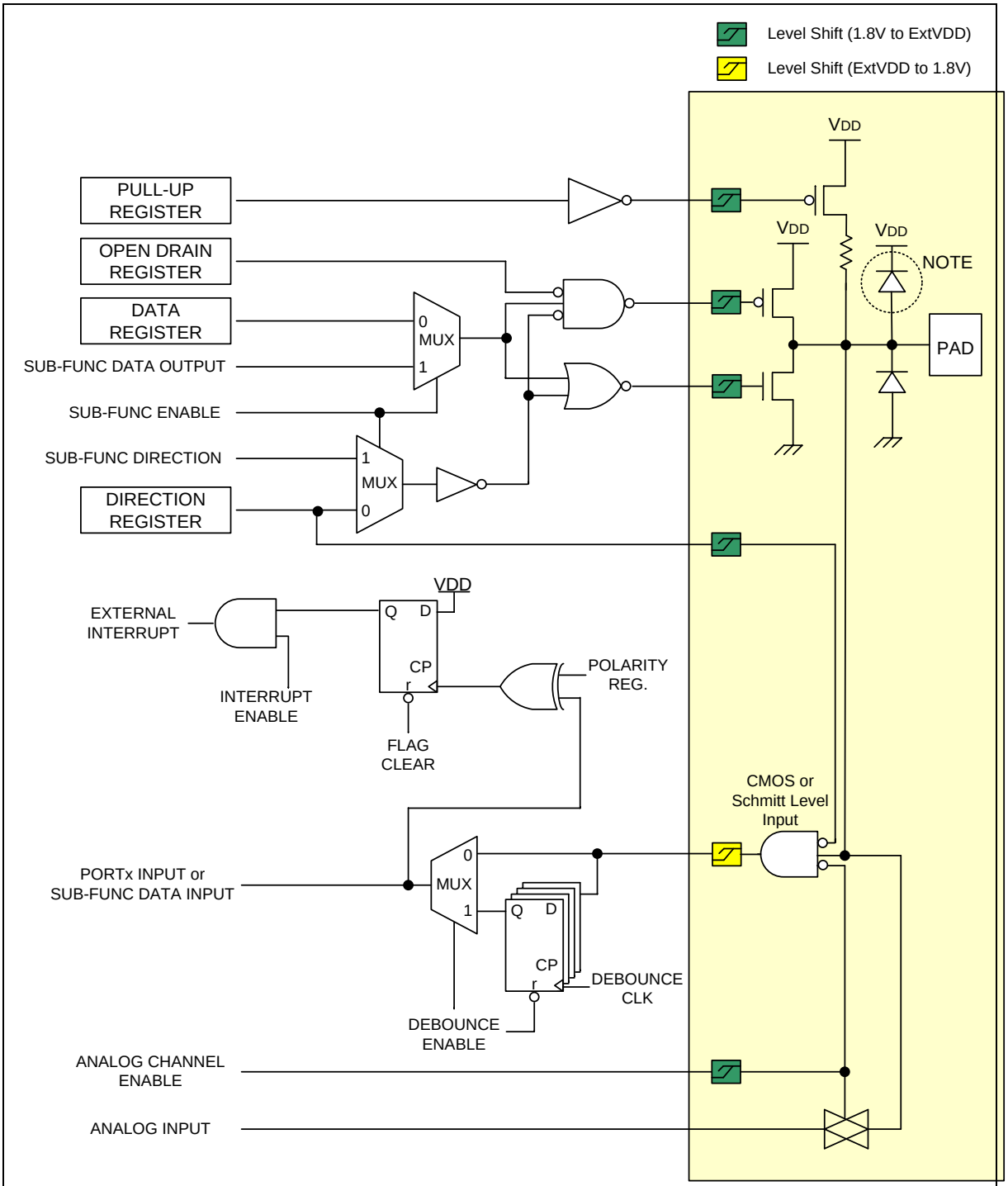



Note)

The P20-P27, P30-P37, P40-P47, P50–P57, P60-P61, P70-P77 and P80-P87 pins(COM, SEG, VLC, CAPH/L) do not have diode between VDD and PAD.

**Figure 6.1 General Purpose I/O Port**

## 6.2 External Interrupt I/O Port




Note)

The P20-P27, P30-P37, P40-P47, P50–P57, P60-P61, P70-P77 and P80-P87 pins(COM, SEG, VLC, CAPH/L) do not have diode between VDD and PAD.

**Figure 6.2 External Interrupt I/O Port**

# 7. Electrical Characteristics

All device parameter data in this document are valid over the device silicon fabrication process window.

## 7.1 Absolute Maximum Ratings

**Table 7-1 Absolute Maximum Ratings**

| Parameter | Symbol | Rating | Unit | Note |
|---|---|---|---|---|
| Supply Voltage | VDD | -0.3 ~ +6.5 | V | – |
| Normal Voltage Pin | $V_I$ | -0.3 ~ VDD+0.3 | V | Voltage on any pin with respect to VSS |
| | $V_O$ | -0.3 ~ VDD+0.3 | V | |
| | $I_{OH}$ | -10 | mA | Maximum current output sourced by ($I_{OH}$ per I/O pin) |
| | $\sum I_{OH}$ | -80 | mA | Maximum current ($\sum I_{OH}$) |
| | $I_{OL}$ | 60 | mA | Maximum current sunk by ($I_{OL}$ per I/O pin) |
| | $\sum I_{OL}$ | 120 | mA | Maximum current ($\sum I_{OL}$) |
| Total Power Dissipation | $P_T$ | 600 | mW | – |
| Storage Temperature | $T_{STG}$ | -65 ~ +150 | °C | – |

NOTE) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## 7.2 Recommended Operating Conditions

**Table 7-2 Recommended Operating Conditions**

($T_A$= -40°C ~ +85°C)

| Parameter | Symbol | Conditions | | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| Operating Voltage | VDD | $f_X$= 32 ~ 38kHz | SX-tal | 1.8 | – | 5.5 | V |
| | | $f_X$= 0.4 ~ 4.2MHz | X-tal | 1.8 | – | 5.5 | |
| | | $f_X$= 0.4 ~ 12.0MHz | | 2.7 | – | 5.5 | |
| | | $f_X$= 0.5 ~ 8.0MHz | Internal RC | 1.8 | – | 5.5 | |
| | | $f_X$= 0.5 ~ 16.0MHz | | 2.0 | – | 5.5 | |
| | | $f_X$= 1.0 ~ 16.0MHz | PLL | 2.0 | – | 5.5 | |
| Operating Temperature | $T_{OPR}$ | VDD= 1.8 ~ 5.5V | | -40 | – | 85 | °C |

## 7.3 A/D Converter Characteristics

**Table 7-3 A/D Converter Characteristics**

($T_A$= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VDD=AVDD, VSS=AVSS=0V)

| Parameter | Symbol | Conditions | | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | – | – | | – | 12 | – | bit |
| Integral Non-Linear | INL | AVDD= 2.7V – 5.5V<br>fx= 8MHz | | – | – | ±6 | LSB |
| Differential Non-Linearity | DNL | | | – | – | ±1 | |
| Top Offset Error | TOE | | | – | – | ±5 | |
| Zero Offset Error | ZOE | | | – | – | ±5 | |
| Conversion Time | $t_{CONV}$ | 12bit resolution, 8MHz | | 20 | – | – | µs |
| Analog Input Voltage | $V_{AIN}$ | – | | AVSS | – | AVDD | V |
| Internal VDC Voltage | VDD15 | – | | – | 1.55 | – | V |
| Analog Input Leakage Current | $I_{AIN}$ | AVDD= 5.12V | | – | – | 2 | µA |
| ADC Current | $I_{ADC}$ | Enable | AVDD= 5.12V | – | 1 | 2 | mA |
| | | Disable | | – | – | 0.1 | µA |

NOTES) 1. Zero offset error is the difference between 000000000000 and the converted output for zero input voltage (AVSS).

2. Top scale error is the difference between 111111111111 and the converted output for top input voltage (AVDD).
3. When AVDD is lower than 2.7V, the ADC resolution is worse.

## 7.4 Power-On Reset Characteristics

**Table 7-4 Power-on Reset Characteristics**

($T_A$= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V)

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| RESET Release Level | $V_{POR}$ | – | – | 1.4 | – | V |
| VDD Voltage Rising Time | $t_R$ | – | 0.05 | – | 30.0 | V/ms |
| POR Current | $I_{POR}$ | – | – | 0.2 | – | μA |

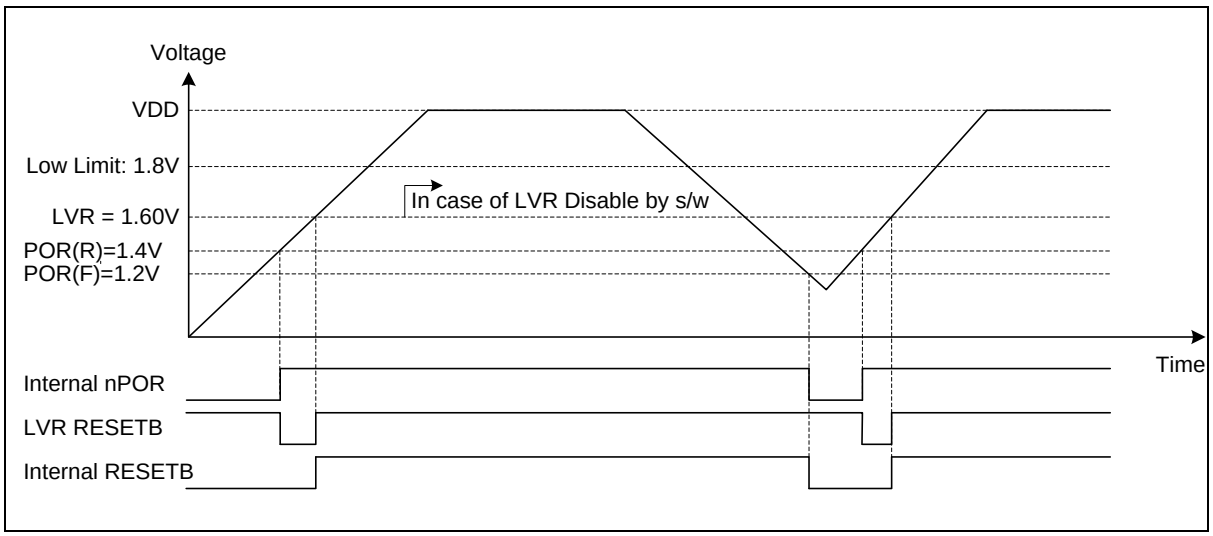



**Figure 7.1 Power-on Reset Timing**

## 7.5 Low Voltage Reset and Low Voltage Indicator Characteristics

**Table 7-5 LVR and LVI Characteristics**

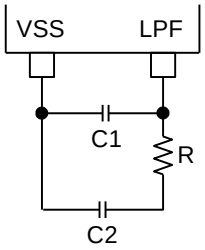
($T_A$= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V)

| Parameter | Symbol | Conditions | | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| Detection Level | $V_{LVR}$<br>$V_{LVI}$ | The LVR can select all levels but LVI can select other levels except 1.60V. | | – | 1.60 | 1.79 | V |
| | | | | 1.85 | 2.00 | 2.15 | |
| | | | | 1.95 | 2.10 | 2.25 | |
| | | | | 2.05 | 2.20 | 2.35 | |
| | | | | 2.17 | 2.32 | 2.47 | |
| | | | | 2.29 | 2.44 | 2.59 | |
| | | | | 2.39 | 2.59 | 2.79 | |
| | | | | 2.55 | 2.75 | 2.95 | |
| | | | | 2.73 | 2.93 | 3.13 | |
| | | | | 2.94 | 3.14 | 3.34 | |
| | | | | 3.18 | 3.38 | 3.58 | |
| | | | | 3.37 | 3.67 | 3.97 | |
| | | | | 3.70 | 4.00 | 4.30 | |
| | | | | 4.10 | 4.40 | 4.70 | |
| Hysteresis | △V | – | | – | 50 | 150 | mV |
| Minimum Pulse Width | $t_{LW}$ | – | | 100 | – | – | μs |
| LVR and LVI Current | $I_{BL}$ | Enable (Both) | VDD= 3V RUN Mode | – | 3 | 6 | μA |
| | | Enable (One of two) | | – | 2 | 5 | |
| | | Disable (Both) | VDD= 3V | – | – | 0.1 | |

## 7.6 Phase Locked Loop Characteristics

**Table 7-6 Phase Locked Loop Characteristics**

($T_A$= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V)

| Parameter | Symbol | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Input Frequency Range | – |  | – | 32.768 | – | kHz |
| Output Frequency Range | $f_{VCO}$ | | 1.024 | – | 16.384 | MHz |
| Clock Duty Ratio | $T_{OD}$ | | 45 | 50 | 55 | % |
| Tolerance | – | | – | – | ±1 | % |
| Settling Time | $t_D$ | | – | 10 | 100 | ms |
| PLL Current | $I_{PLL}$ | Enable, $f_{VCO}$=16.384MHz | – | 0.5 | 1.0 | mA |
| | | Disable | – | – | 0.1 | µA |

NOTE) Where R= 6.8kΩ, C1=820pF, and C2= 10nF.

## 7.7 Internal RC Oscillator Characteristics

**Table 7-7 Internal RC Oscillator Characteristics**

($T_A$= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V)

| Parameter | Symbol | Conditions | | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| Frequency | $f_{IRC}$ | $V_{DD}$ = 2.0V to 5.5 V | | – | 16 | – | MHz |
| Tolerance | – | $T_A$ = 0°C to +50°C | With 0.1uF Bypass Capacitor | – | – | ±1.5 | % |
| | | $T_A$ = -20°C to +85°C | | | | ±2.5 | |
| | | $T_A$ = -40°C to +85°C | | | | ±3.5 | |
| Clock Duty Ratio | TOD | – | | 40 | 50 | 60 | % |
| Stabilization Time | $T_{HFS}$ | – | | – | – | 100 | µs |
| IRC Current | $I_{IRC}$ | Enable | | – | 0.2 | – | mA |
| | | Disable | | – | – | 0.1 | µA |

Note: A 0.1uF Bypass capacitor should be connected to VDD and VSS. Refer to the “Recommend Circuit and Layout”.

## 7.8 Internal Watch-Dog Timer RC Oscillator Characteristics

**Table 7-8 Internal WDTRC Oscillator Characteristics**

($T_A$= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V)

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Frequency | $f_{WDTRC}$ | – | 2 | 5 | 10 | kHz |
| Stabilization Time | $t_{WDTS}$ | – | – | – | 1 | ms |
| WDTRC Current | $I_{WDTRC}$ | Enable | – | 1 | – | µA |
| | | Disable | – | – | 0.1 | |

## 7.9 LCD Voltage Characteristics

**Table 7-9 LCD Voltage Characteristics**

($T_A$= -40°C ~ +85°C, VDD= 2.0V ~ 5.5V, VSS= 0V)

| Parameter | Symbol | Conditions | | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| LCD Voltage | $V_{LC3}$ | Voltage booster enabled, 1/4 bias | LCDCCR=0000b | Typx0.93 | 0.75 | Typx1.07 | V |
| | | | LCDCCR=0001b | | 0.79 | | |
| | | | LCDCCR=0010b | | 0.83 | | |
| | | | LCDCCR=0011b | | 0.86 | | |
| | | | LCDCCR=0100b | | 0.90 | | |
| | | | LCDCCR=0101b | | 0.94 | | |
| | | | LCDCCR=0110b | | 0.98 | | |
| | | | LCDCCR=0111b | | 1.01 | | |
| | | | LCDCCR=1000b | | 1.05 | | |
| | | | LCDCCR=1001b | | 1.09 | | |
| | | | LCDCCR=1010b | | 1.13 | | |
| | | | LCDCCR=1011b | | 1.16 | | |
| | | | LCDCCR=1100b | | 1.20 | | |
| | | | LCDCCR=1101b | | 1.24 | | |
| | | | LCDCCR=1110b | | 1.28 | | |
| | | | LCDCCR=1111b | | 1.31 | | |
| LCD Mid Bias Voltage | $V_{LC0}$ | Voltage booster enabled, 1/4 bias, No panel load, VDD=3V | | Typx0.95 | 4xVLC3 | Typx1.05 | V |
| | $V_{LC1}$ | | | Typx0.95 | 3xVLC3 | Typx1.05 | |
| | $V_{LC2}$ | | | Typx0.95 | 2xVLC3 | Typx1.05 | |
| | $V_{LC1}$ | Voltage booster disabled, VDD=2.7V to 5.5V, 1/4 bias, LCD clock = 0Hz, VLC0=VDD | | Typ-0.2 | 0.75xVDD | Typ+0.2 | V |
| | $V_{LC2}$ | | | Typ-0.2 | 0.5xVDD | Typ+0.2 | |
| | $V_{LC3}$ | | | Typ-0.2 | 0.25xVDD | Typ+0.2 | |
| LCD Driver Output Impedance | $R_{LO}$ | VLCD=3V, ILOAD=±10uA | | – | 5 | 10 | kΩ |
| LCD Bias Dividing Resistor | $R_{LCD1}$ | Internal resistor mode, $T_A$ = 25 C | Low | 7.0 | 10 | 13.0 | kΩ |
| | $R_{LCD2}$ | | Mid | 35 | 50 | 65 | |
| | $R_{LCD3}$ | | High | 75 | 100 | 125 | |
| LCD Block Current | $I_{LCD}$ | Voltage booster mode, VDD=3V, VLCD=3.15V, 1/3Bias | | – | 3 | 6 | μA |

## 7.10 DC Characteristics

**Table 7-10 DC Characteristics**

($T_A$= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V, $f_{XIN}$= 12MHz)

| Parameter | Symbol | Conditions | | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH1}$ | P0~P6, RESETB | | 0.8VDD | – | VDD | V |
| | $V_{IH2}$ | All input pins except $V_{IH1}$ | | 0.7VDD | – | VDD | V |
| | $V_{IH3}$ | P20, P33, P34, P37;<br>3V Interface mode | | 2.4 | – | VDD | V |
| Input Low Voltage | $V_{IL1}$ | P0~P6, RESETB | | – | – | 0.2VDD | V |
| | $V_{IL2}$ | All input pins except $V_{IL1}$ | | – | – | 0.3VDD | V |
| Output High Voltage | $V_{OH}$ | VDD= 4.5V, $I_{OH}$= -2mA,<br>All output ports; | | VDD-1.0 | – | – | V |
| Output Low Voltage | $V_{OL1}$ | VDD=4.5V, $I_{OL1}$= 10mA;<br>All output ports except $V_{OL2}$ | | – | – | 1.0 | V |
| | $V_{OL2}$ | VDD= 4.5V, $I_{OL2}$= 15mA ;<br>P10~P13, P23~P24, P4 | | – | – | 1.0 | V |
| Output High Current | $I_{OH}$ | VDD=4.5V, $V_{OH}$ = 3.5V;<br>All output ports | | -2 | – | – | mA |
| Output Low Current | $I_{OL1}$ | VDD=4.5V, $V_{OL}$ = 1.0V;<br>All output ports except $I_{OL2}$ | | 10 | – | – | mA |
| | $I_{OL2}$ | VDD=4.5V, $V_{OL}$ = 1.0V;<br>P10~P13, P23~P24, P4 | | 15 | – | – | mA |
| Input High Leakage Current | $I_{IH}$ | All input ports | | – | – | 1 | µA |
| Input Low Leakage Current | $I_{IL}$ | All input ports | | -1 | – | – | µA |
| Pull-Up Resistor | $R_{PU1}$ | VI=0V,<br>$T_A$= 25°C<br>All Input ports | VDD=5.0V | 25 | 50 | 100 | kΩ |
| | | | VDD=3.0V | 50 | 100 | 200 | |
| | $R_{PU2}$ | VI=0V,<br>$T_A$= 25°C<br>RESETB | VDD=5.0V | 150 | 250 | 400 | kΩ |
| | | | VDD=3.0V | 300 | 500 | 700 | |
| OSC feedback resistor | $R_{X1}$ | XIN= VDD, XOUT= VSS<br>$T_A$= 25°C, VDD= 5V | | 600 | 1200 | 2000 | kΩ |
| | $R_{X2}$ | SXIN=VDD, SXOUT=VSS<br>$T_A$= 25 °C ,VDD=5V | | 2500 | 5000 | 10000 | |

**Table 7-10 DC Characteristics (Continued)**

($T_A$= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V, $f_{XIN}$= 12MHz)

| Parameter | Symbol | Condition | | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|---|
| Supply Current | $I_{DD1}$ (RUN) | $f_{XIN}$= 12MHz, VDD= 5V±10% | | – | 2.5 | 5.0 | mA |
| | | $f_{XIN}$= 10MHz, VDD= 3V±10% | | – | 1.6 | 3.2 | |
| | | $f_{IRC}$= 8MHz, VDD= 5V±10% | | – | 1.3 | 2.6 | |
| | | $f_{XIN}$= 4MHz, VDD= 3V±10% | | – | 0.9 | 1.8 | |
| | $I_{DD2}$ (IDLE) | $f_{XIN}$= 12MHz, VDD= 5V±10% | | – | 1.2 | 2.4 | mA |
| | | $f_{XIN}$= 10MHz, VDD= 3V±10% | | – | 0.7 | 1.4 | |
| | | $f_{IRC}$= 8MHz, VDD= 5V±10% | | – | 0.6 | 1.2 | |
| | | $f_{XIN}$= 4MHz, VDD= 3V±10% | | – | 0.4 | 0.8 | |
| | $I_{DD3}$ | $f_{XIN}$= 32.768kHz VDD= 3V±10% $T_A$= 25°C PSAVE=1 | Sub RUN | – | 45.0 | 90.0 | µA |
| | $I_{DD4}$ | | Sub IDLE | – | 3.5 | 7.0 | µA |
| | $I_{DD5}$ | STOP, VDD= 5V±10%, $T_A$= 25°C | | – | 0.5 | 3.0 | µA |

NOTES) 1. Where the $f_{XIN}$ is an external main oscillator, the $f_{SUB}$ is an external sub oscillator, the $f_{IRC}$ is an internal RC oscillator, the fPLL is the output frequency of the PLL (phase locked-loop), and the fx is the selected system clock.

2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.

3. All supply current items include the current of the power-on reset (POR) block.

## 7.11 AC Characteristics

**Table 7-11 AC Characteristics**

($T_A$= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V)

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| RESETB input low width | $t_{RST}$ | Input, VDD= 5V | 10 | – | – | μs |
| Interrupt input high, low width | $t_{IWH}$, $t_{IWL}$ | All interrupt, VDD= 5V | 200 | – | – | ns |
| External Counter Input High, Low Pulse Width | $t_{ECWH}$, $t_{ECWL}$ | ECn, VDD = 5 V (n= 0, 1, 2, 3, 4, 5, 6, 7) | 200 | – | – | |
| External Counter Transition Time | $t_{REC}$, $t_{FEC}$ | ECn, VDD = 5 V (n= 0, 1, 2, 3, 4, 5, 6, 7) | 20 | – | – | |

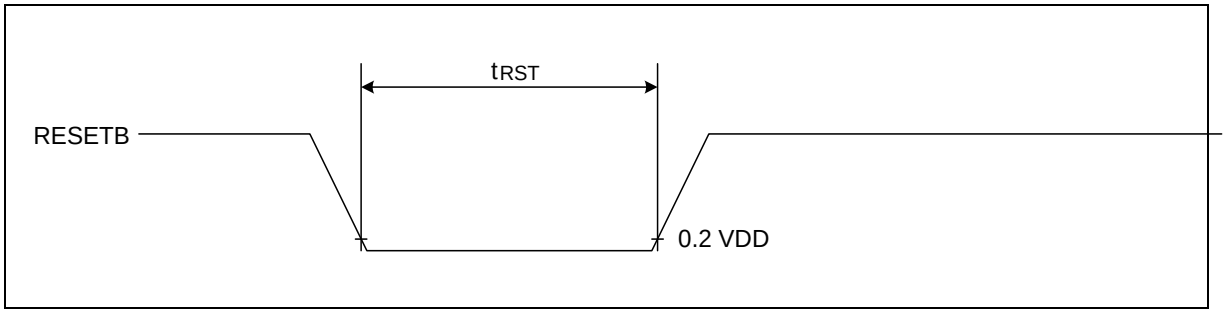



**Figure 7.2 Input Timing for RESETB**

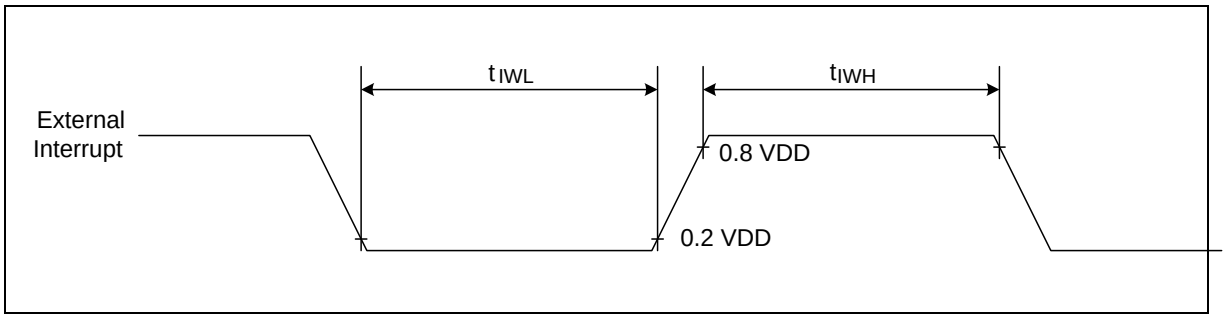



**Figure 7.3 Input Timing for External Interrupts**

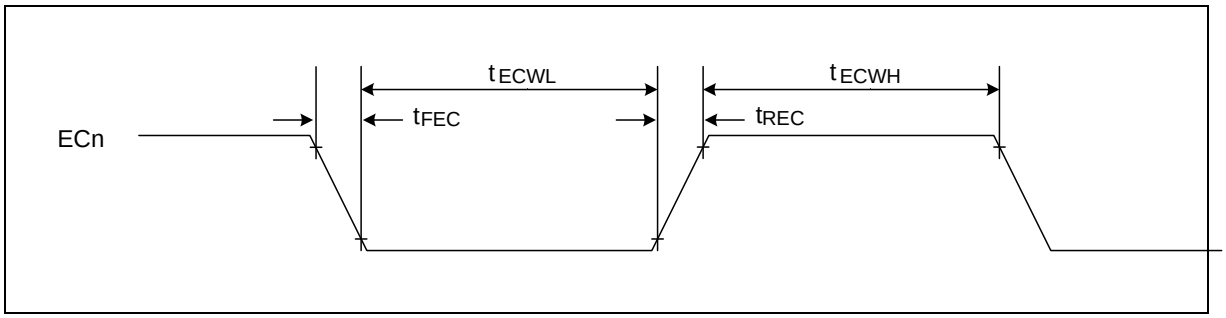



**Figure 7.4 Input Timing for EC0, EC1, EC2, EC3, EC4, EC5, EC6, EC7**

## 7.12 SPI Characteristics

**Table 7-12 SPI Characteristics**

($T_A$= -40°C – +85°C, VDD= 1.8V – 5.5V)

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Output Clock Pulse Period | $t_{SCK}$ | Internal SCK source | 200 | – | – | ns |
| Input Clock Pulse Period | | External SCK source | 200 | – | – | |
| Output Clock High, Low Pulse Width | $t_{SCKH}$, $t_{SCKL}$ | Internal SCK source | 70 | – | – | |
| Input Clock High, Low Pulse Width | | External SCK source | 70 | – | – | |
| First Output Clock Delay Time | $t_{FOD}$ | Internal/External SCK source | 100 | – | – | |
| Output Clock Delay Time | $t_{DS}$ | – | – | – | 50 | |
| Input Setup Time | $t_{DIS}$ | – | 100 | – | – | |
| Input Hold Time | $t_{DIH}$ | – | 150 | – | – | |

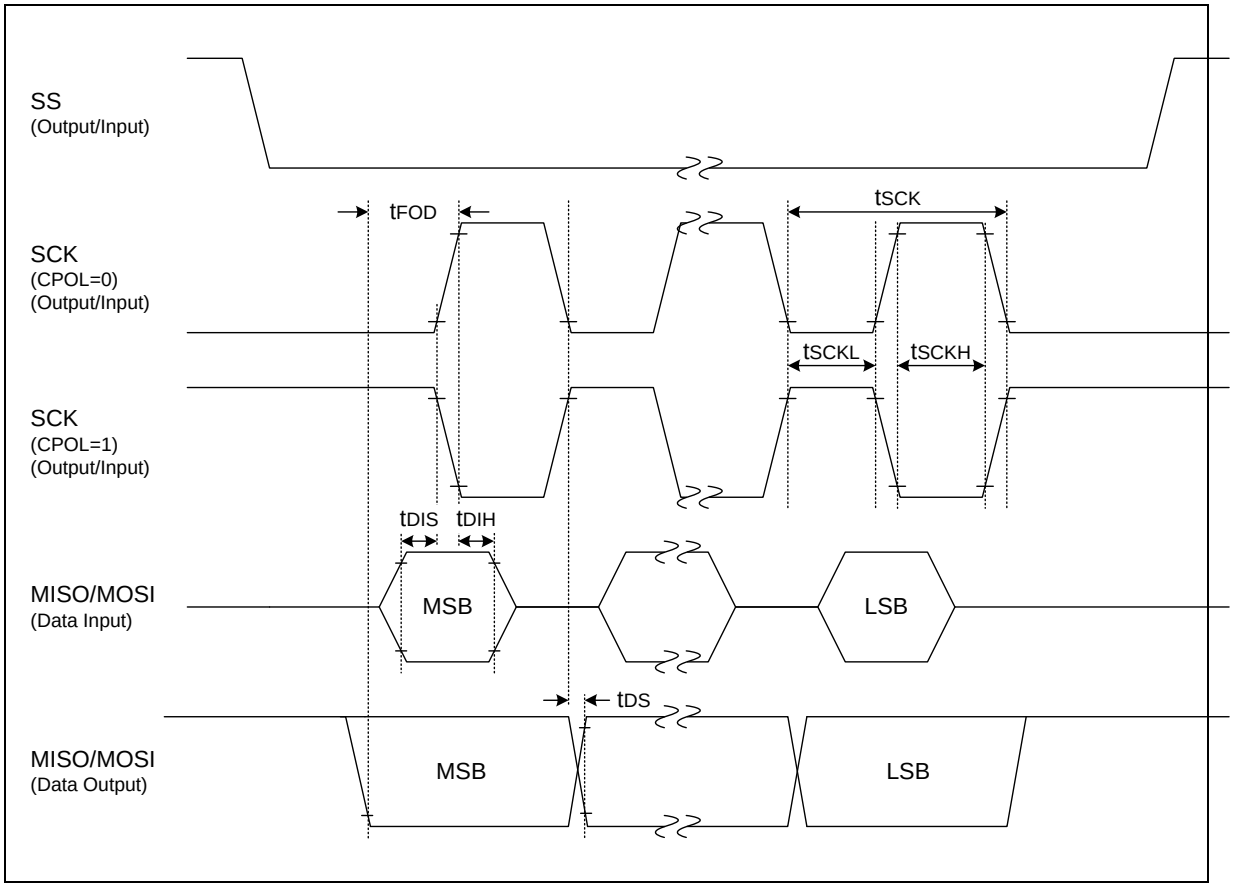



**Figure 7.5 SPI Timing**

## 7.13 UART Characteristics

**Table 7-13 UART Characteristics**

($T_A$= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, $f_{XIN}$=11.1MHz)

| Parameter | Symbol | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|
| Serial port clock cycle time | $t_{SCK}$ | 1250 | $t_{CPU}$ x 16 | 1650 | ns |
| Output data setup to clock rising edge | $t_{S1}$ | 590 | $t_{CPU}$ x 13 | – | ns |
| Clock rising edge to input data valid | $t_{S2}$ | – | – | 590 | ns |
| Output data hold after clock rising edge | $t_{H1}$ | $t_{CPU}$ - 50 | $t_{CPU}$ | – | ns |
| Input data hold after clock rising edge | $t_{H2}$ | 0 | – | – | ns |
| Serial port clock High, Low level width | $t_{HIGH}$, $t_{LOW}$ | 470 | $t_{CPU}$ x 8 | 970 | ns |

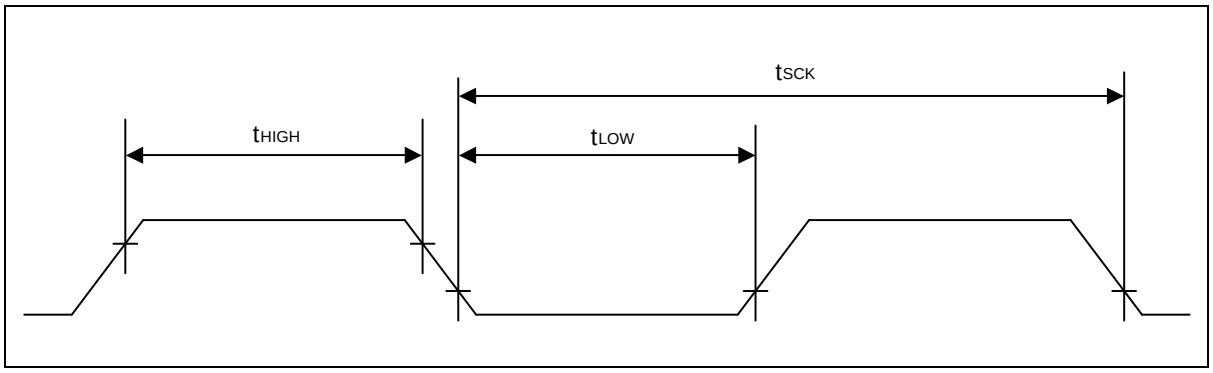



**Figure 7.6 Waveform for UART Timing Characteristics**

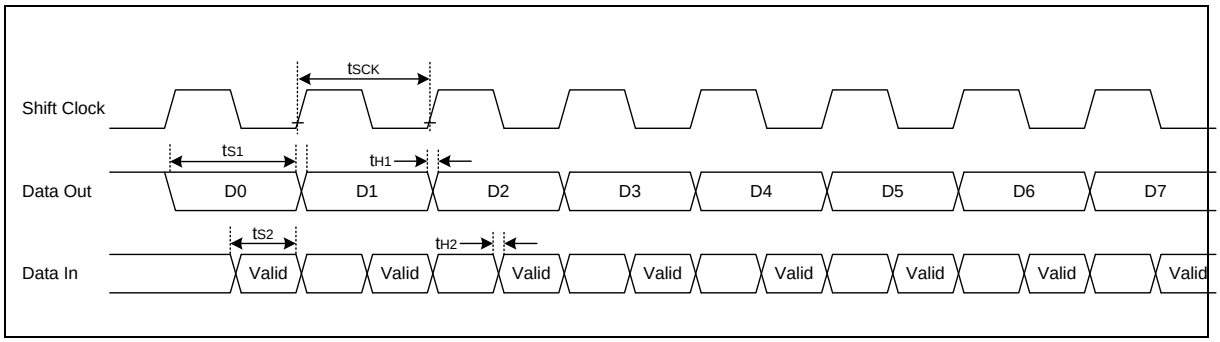



**Figure 7.7 Timing Waveform for the UART Module**

## 7.14 I2C Characteristics

**Table 7-14 I2C Characteristics**

($T_A$= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V)

| Parameter | Symbol | Standard Mode | | High-Speed Mode | | Unit |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| Clock frequency | $t_{SCL}$ | 0 | 100 | 0 | 400 | kHz |
| Clock High Pulse Width | $t_{SCLH}$ | 4.0 | – | 0.6 | – | μs |
| Clock Low Pulse Width | $t_{SCLL}$ | 4.7 | – | 1.3 | – | |
| Bus Free Time | $t_{BF}$ | 4.7 | – | 1.3 | – | |
| Start Condition Setup Time | $t_{STSU}$ | 4.7 | – | 0.6 | – | |
| Start Condition Hold Time | $t_{STHD}$ | 4.0 | – | 0.6 | – | |
| Stop Condition Setup Time | $t_{SPSU}$ | 4.0 | – | 0.6 | – | |
| Stop Condition Hold Time | $t_{SPHD}$ | 4.0 | – | 0.6 | – | |
| Output Valid from Clock | $t_{VD}$ | 0 | – | 0 | – | |
| Data Input Hold Time | $t_{DIH}$ | 0 | – | 0 | 1.0 | |
| Data Input Setup Time | $t_{DIS}$ | 250 | – | 100 | – | ns |

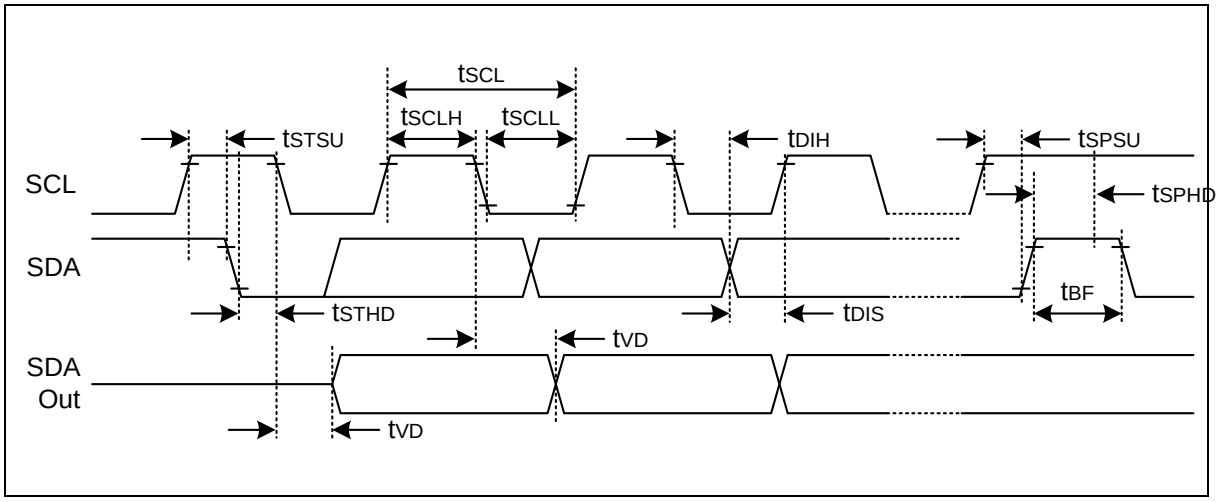


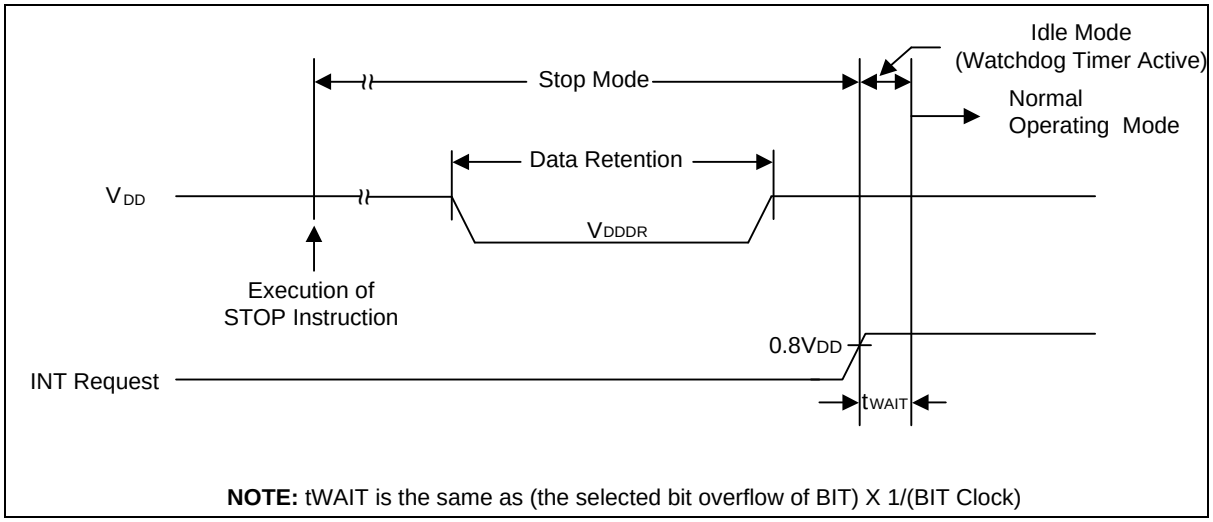

**Figure 7.8 I2C Timing**

## 7.15 Data Retention Voltage in Stop Mode

**Table 7-15 Data Retention Voltage in Stop Mode**

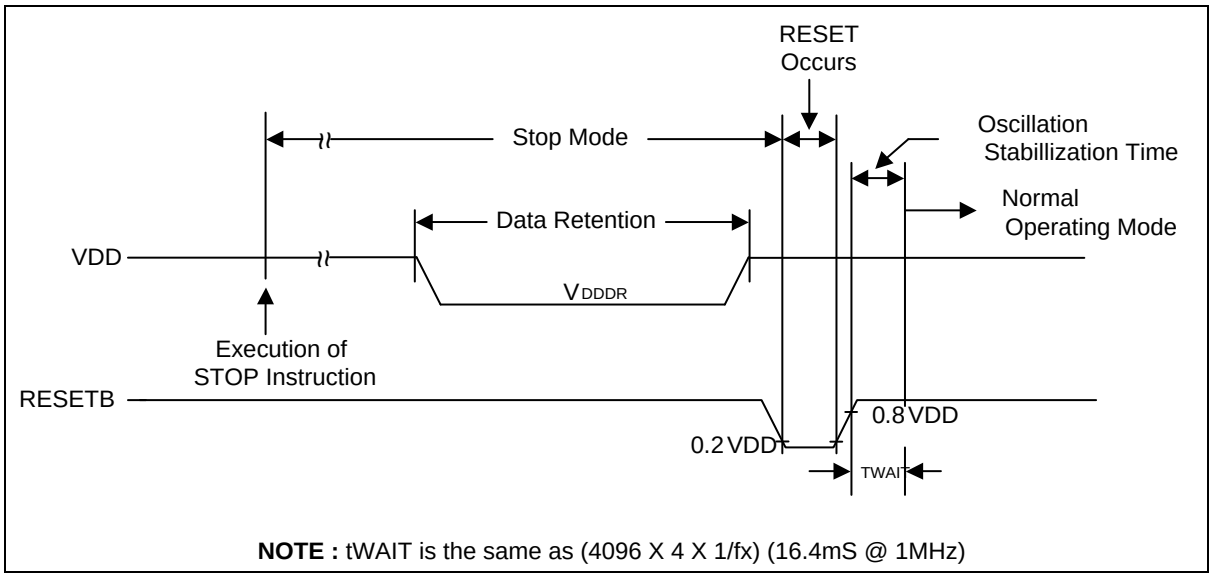
($T_A$= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V)

| Parameter | Symbol | Conditions | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | – | 1.0 | – | 5.5 | V |
| Data retention supply current | $I_{DDDR}$ | VDDR= 1.0V, ($T_A$= 25°C), Stop mode | – | – | 1 | μA |




**NOTE:** tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

**Figure 7.9 Stop Mode Release Timing when Initiated by an Interrupt**




**NOTE :** tWAIT is the same as (4096 X 4 X 1/fx) (16.4mS @ 1MHz)

**Figure 7.10 Stop Mode Release Timing when Initiated by RESETB**

## 7.16 Internal Flash Rom Characteristics

**Table 7-16 Internal Flash Rom Characteristics**

($T_A$= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V)

| Parameter | Symbol | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Sector Write Time | $t_{FSW}$ | – | – | 2.5 | 2.7 | ms |
| Sector Erase Time | $t_{FSE}$ | – | – | 3.0 | 3.3 | |
| Code Write Protection Time | $t_{FHL}$ | – | – | 2.5 | 2.7 | |
| Page Buffer Reset Time | $t_{FBR}$ | – | – | – | 5 | μs |
| Flash Programming Voltage | $V_{PGM}$ | – | 2.0 | – | 5.5 | |
| Flash Programming Frequency | $f_{PGM}$ | – | 0.4 | – | – | MHz |
| Endurance of Write/Erase (Sector 0~1019) | $NF_{WE}$ | 25°C | – | – | 10,000 | Times |
| Endurance of Write/Erase (Sector 1020~1023) | | | | | 100,000 | Times |
| Flash Data Retention Time | $t_{RT}$ | – | 10 | – | – | Years |

NOTE) During a flash operation, SCLK[1:0] of SCCR must be set to “00” or “01” (INT-RC OSC or Main X-TAL for system clock).

## 7.17 Input/Output Capacitance

**Table 7-17 Input/Output Capacitance**

($T_A$= -40°C ~ +85°C, VDD= 0V)

| Parameter | Symbol | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | fx= 1MHz<br>Unmeasured pins are connected to VSS | – | – | 10 | pF |
| Output Capacitance | $C_{OUT}$ | | | | | |
| I/O Capacitance | $C_{IO}$ | | | | | |

## 7.18 Main Clock Oscillator Characteristics

**Table 7-18 Main Clock Oscillator Characteristics**

($T_A$= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V)

| Oscillator | Parameter | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Crystal | Main oscillation frequency | 1.8V – 5.5V | 0.4 | – | 4.2 | MHz |
| | | 2.7V – 5.5V | 0.4 | – | 12.0 | |
| Ceramic Oscillator | Main oscillation frequency | 1.8V – 5.5V | 0.4 | – | 4.2 | MHz |
| | | 2.7V – 5.5V | 0.4 | – | 12.0 | |
| External Clock | XIN input frequency | 1.8V – 5.5V | 0.4 | – | 4.2 | MHz |
| | | 2.7V – 5.5V | 0.4 | – | 12.0 | |

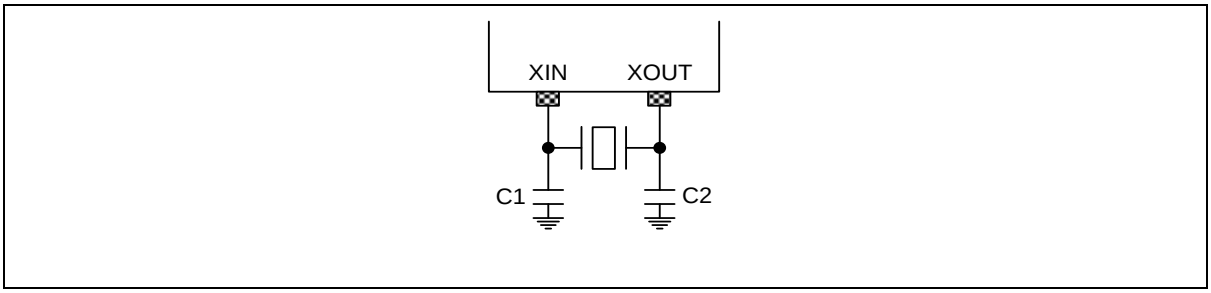



**Figure 7.11 Crystal/Ceramic Oscillator**

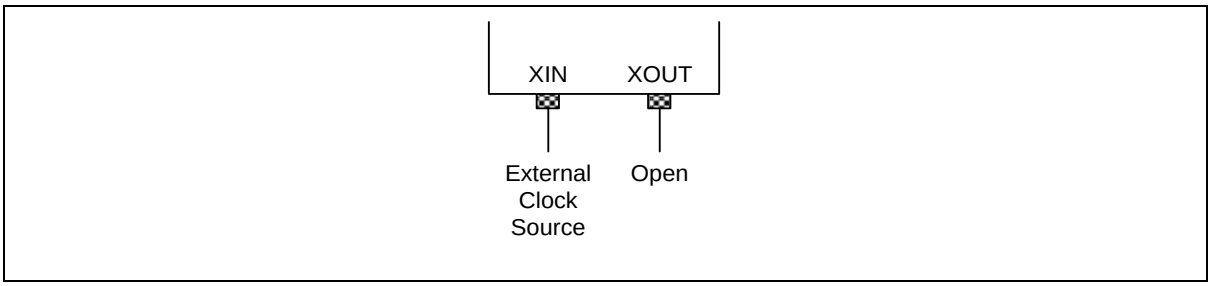



**Figure 7.12 External Clock**

## 7.19 Sub Clock Oscillator Characteristics

**Table 7-19 Sub Clock Oscillator Characteristics**

($T_A$= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V)

| Oscillator | Parameter | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Crystal | Sub oscillation frequency | 1.8V – 5.5V | 32 | 32.768 | 38 | kHz |
| External Clock | SXIN input frequency | | 32 | – | 100 | kHz |

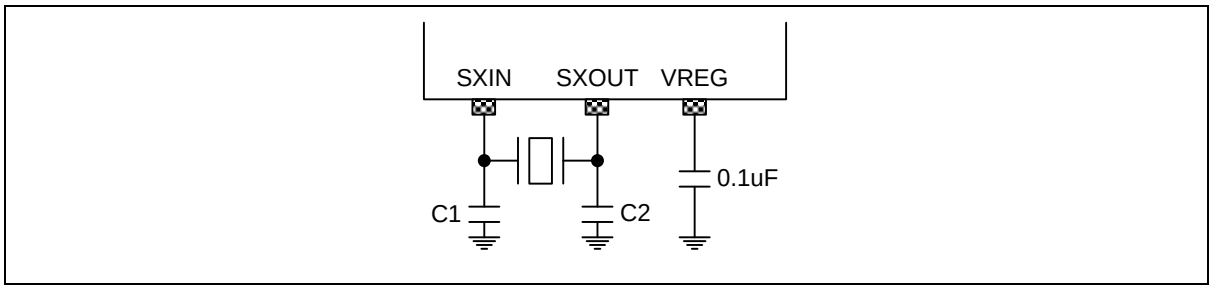



**Figure 7.13 Crystal Oscillator**

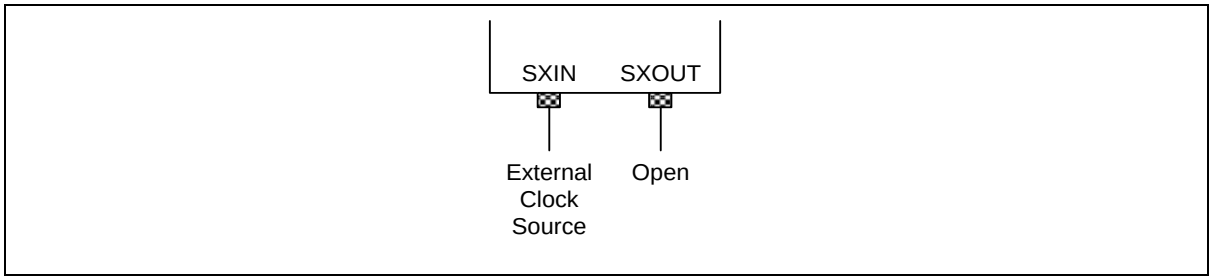



**Figure 7.14 External Clock**

## 7.20 Main Oscillation Stabilization Characteristics

**Table 7-20 Main Oscillation Stabilization Characteristics**

($T_A$= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V)

| Oscillator | Parameter | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|
| Crystal | fx > 1MHz<br>Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range. | – | – | 60 | ms |
| Ceramic | | – | – | 10 | ms |
| External Clock | $f_{XIN}$ = 0.4 to 12MHz<br>XIN input high and low width ($t_{XH}$, $t_{XL}$) | 31 | – | 1250 | ns |

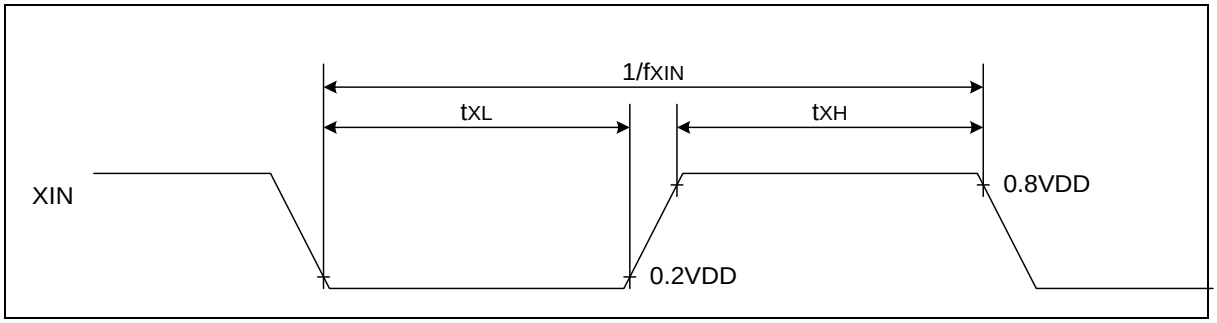



**Figure 7.15 Clock Timing Measurement at XIN**

## 7.21 Sub Oscillation Characteristics

**Table 7-21 Sub Oscillation Stabilization Characteristics**

($T_A$= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V)

| Oscillator | Parameter | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|
| Crystal | – | – | – | 10 | s |
| External Clock | SXIN input high and low width ($t_{XH}$, $t_{XL}$) | 5 | – | 15 | μs |

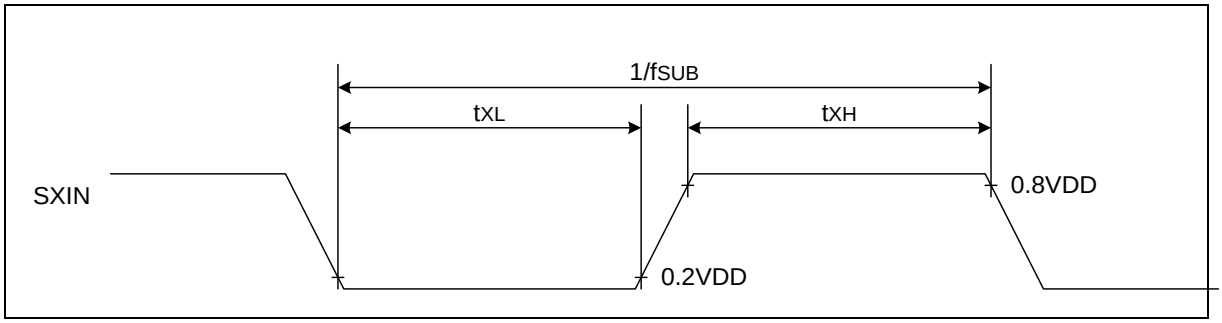



**Figure 7.16 Clock Timing Measurement at SXIN**

## 7.22 Operating Voltage Range

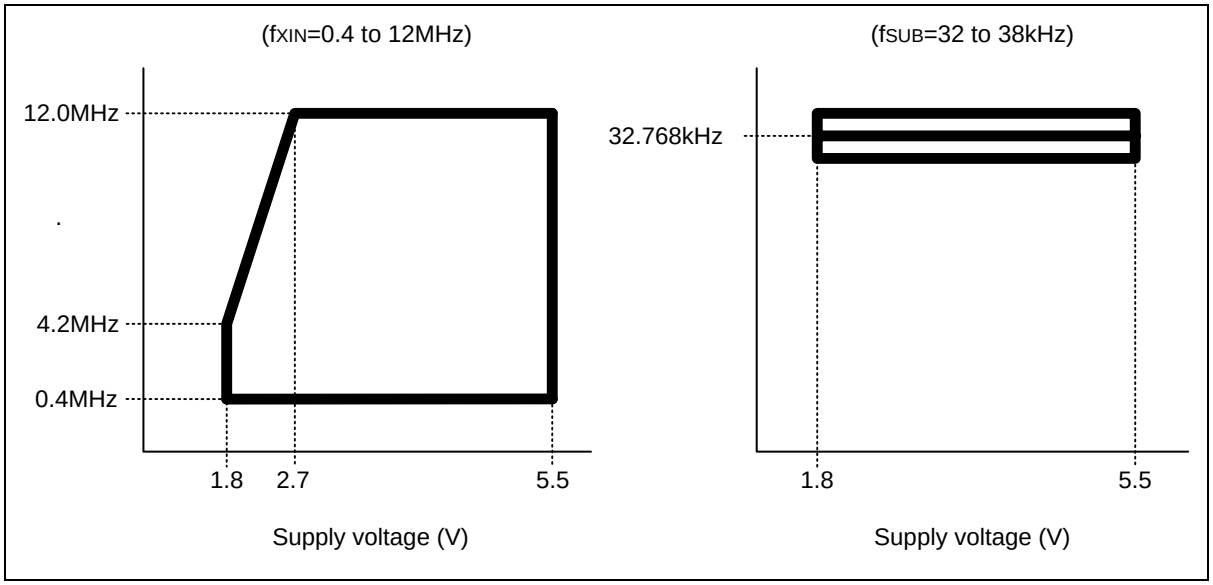



**Figure 7.17 Operating Voltage Range**

## 7.23 Recommended Circuit and Layout

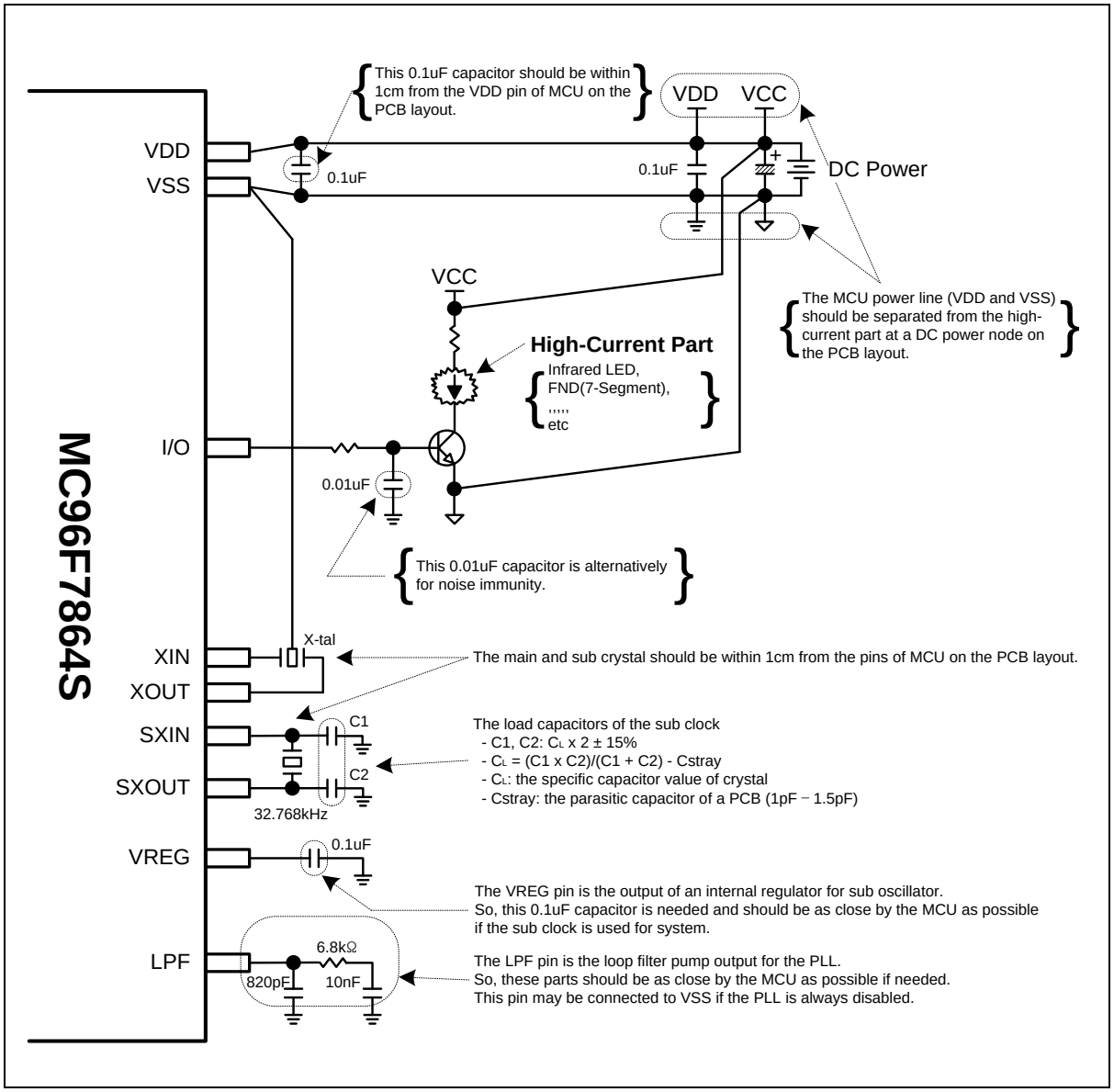
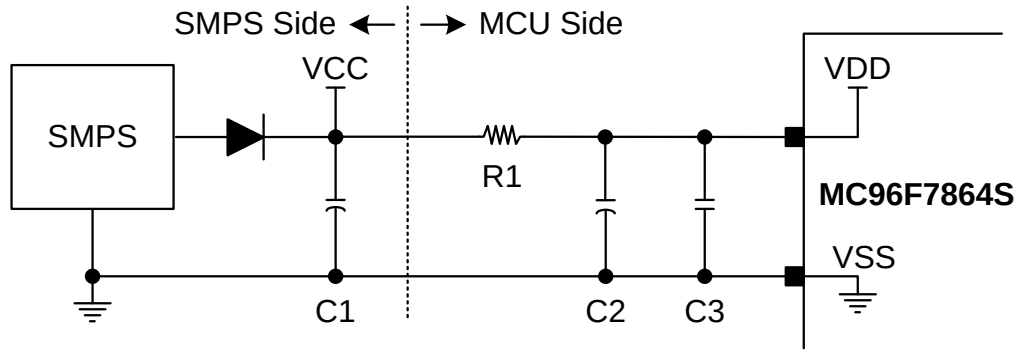



**Figure 7.18 Recommended Circuit and Layout**

## 7.24 Recommended Circuit and Layout with SMPS Power




1. The C1 capacitor is to flatten out the voltage of the SMPS power, VCC.
   √ Recommended C1: 470uF/25V more.
2. The R1 and C2 are the RC filter for VDD and suppress the ripple of VCC.
   √ Recommended R1: 10Ω - 20Ω
   √ Recommended C2: 47uF/25V more
   √ The R1 and C2 should be as close by the C3 as possible.
3. The C3 capacitor is used for temperature compensation because an electrolytic capacitor becomes worse characteristics at low temperature.
   √ Recommended C3: ceramic capacitor 2.2uF more
   √ The C3 should be within 1cm from VDD pin of MCU on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc) when the SMPS supplies the VDD of MCU.

**Figure 7.19 Recommended Circuit and Layout with SMPS Power**

## 7.25 Typical Characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

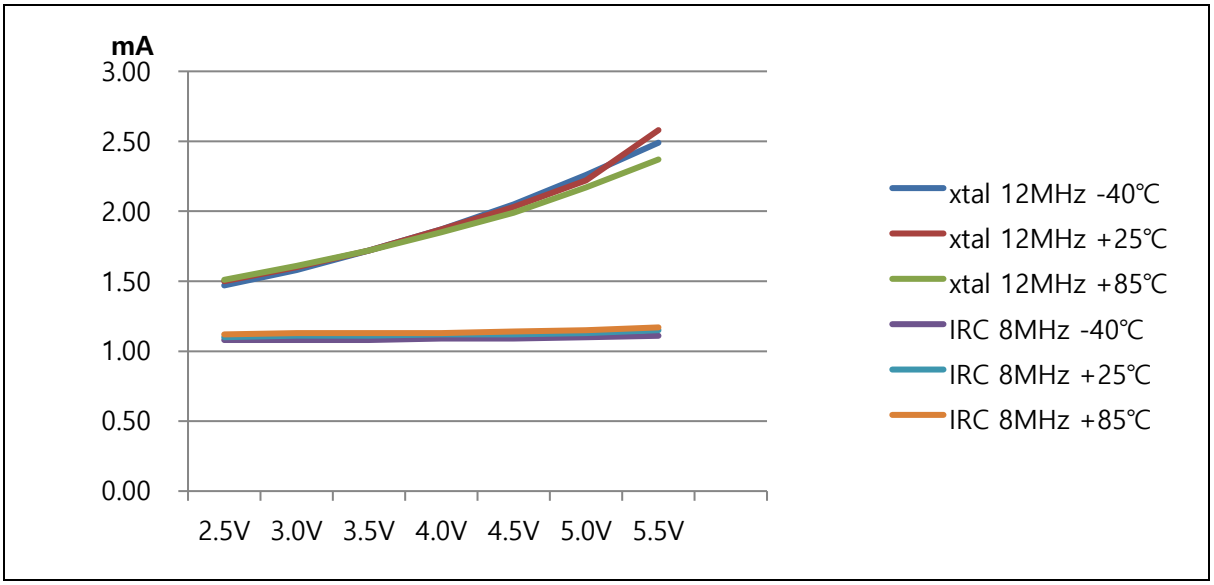



**Figure 7.20 RUN (IDD1 ) Current**

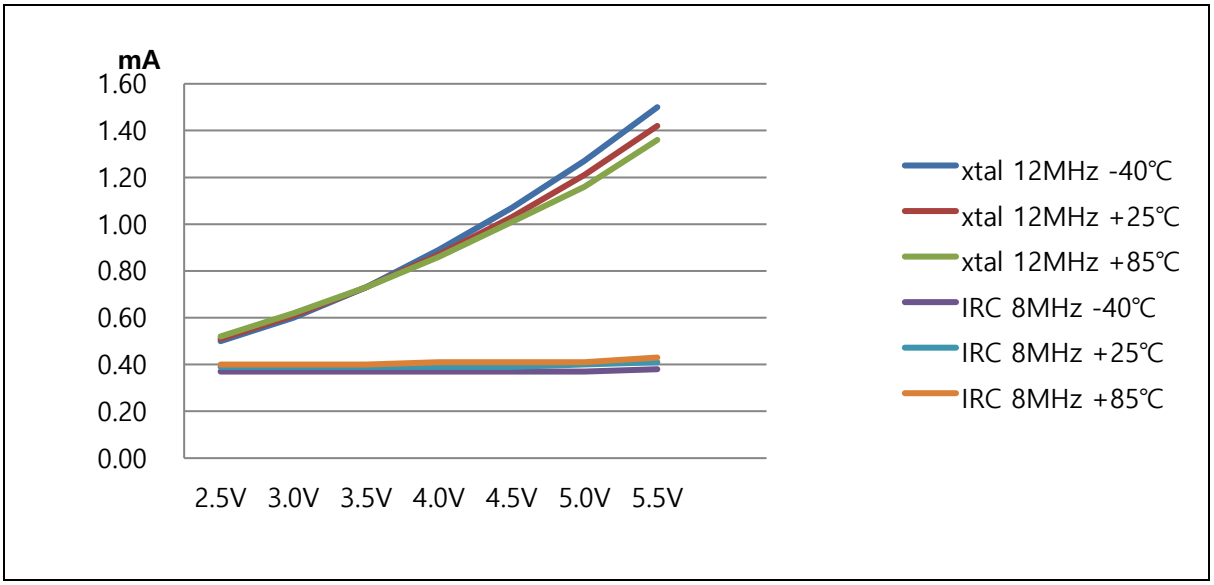



**Figure 7.21 IDLE (IDD2) Current**

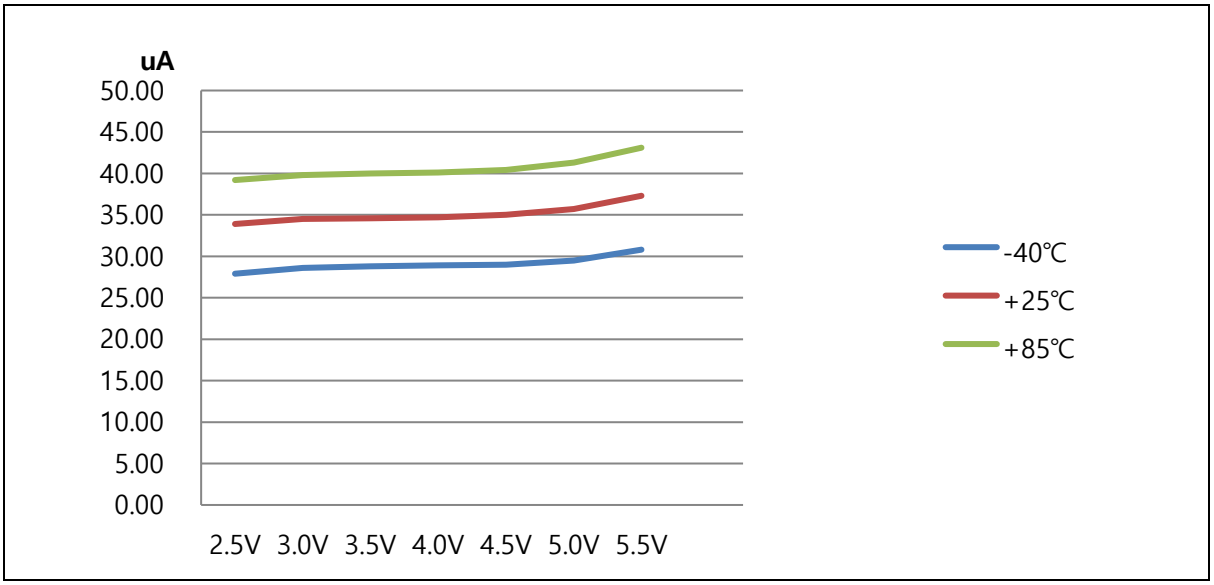



**Figure 7.22 SUB RUN (IDD3) Current**

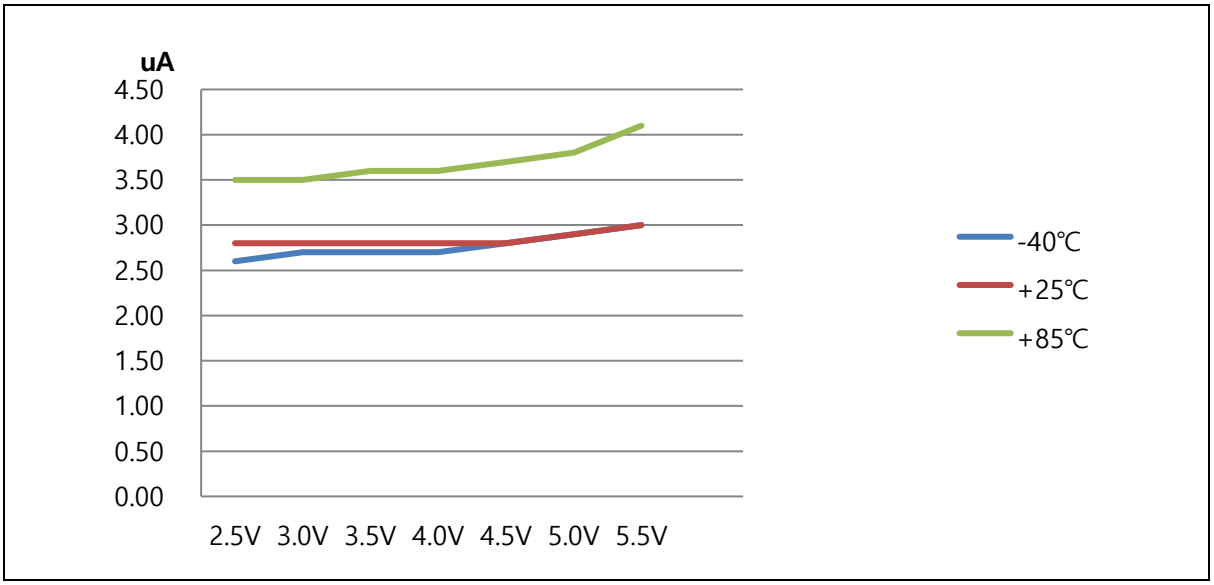



**Figure 7.23 SUB IDLE (IDD4) Current**

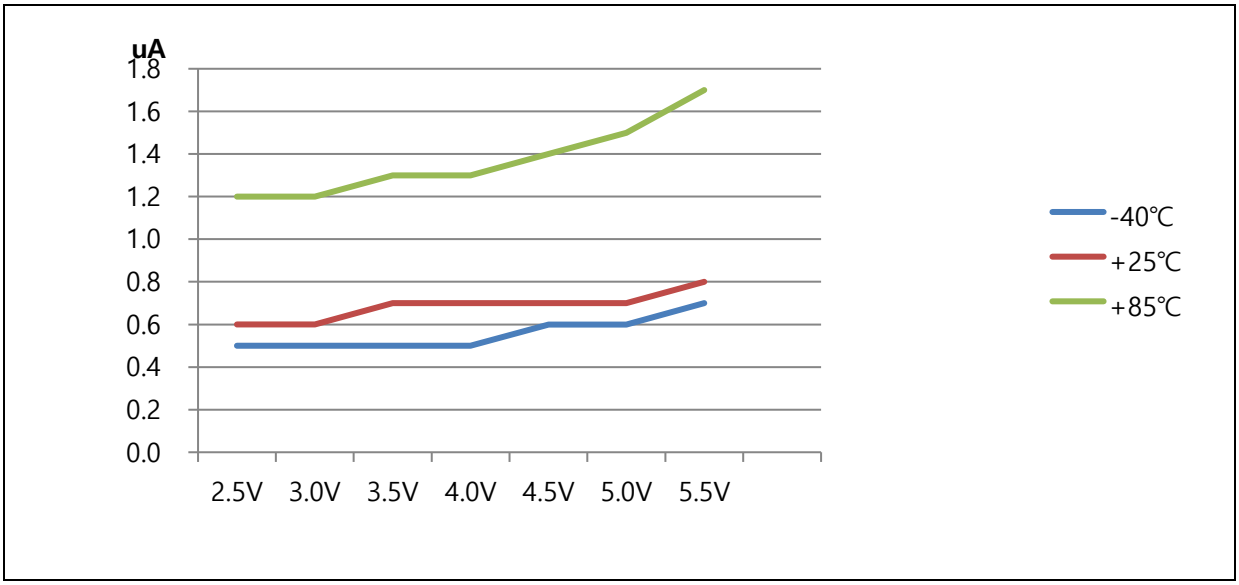



**Figure 7.24 STOP (IDD5) Current**

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