A33M116, A33M114
Datasheet

32-bit Cortex-M3 based High-performance Microcontroller
Flash 256KB, Data Flash 32KB, SRAM 16KB
Advanced Motor Control PWM

DS Rev. 1.04

Features

Core
- High performance Cortex-M3 core
- Maximum operating frequency 96MHz

Memories
- 256/128KB code flash memory
- 32KB data flash memory, 16KB SRAM

Clock, reset and power management
- Two main operating clocks: HCLK, PCLK
- Two system reset: cold reset, warm reset
- Power management mode: Run mode, Sleep mode, Stop mode

Interrupt management
- Nested Vector Interrupt Controller (NVIC) with 86 interrupt sources

Timers
- Watchdog Timer
- Free-run Timer
- Eight general purpose timers
  - Periodic, one-shot, PWM, capture mode

Communication interfaces
- 4 UARTs, 2 I2Cs, 2 SPIs

Motor Pulse-Width Modulation
- Two MPWM generators

Quadrature Encoder Interface
- Two QEI channels

12-bit 1.3Msps ADC
- Two unit, 22-channels inputs

Analog front end
- Four Op-Amps and comparators

CRC generator
- 7/8/16/32-bit CRC generator

Development support
- SWD interface

Four types of package options
- LQFP64-1010 (0.5mm pitch)
- LQFP64-1212 (0.65mm pitch)
- LQFP48-0707 (0.5mm pitch)
- LQFP44-1010 (0.8mm pitch)

Operating temperature
- Commercial grade (-40℃ to +105℃)

Operating voltage
- 2.5 to 5.5V (Exceptionally, the ADC operates from 2.7 to 5.5V)

Applications
- Refrigerator, Washing machine, Dryer, Dishwasher, Water Purifier, Blender
- Pump
- FAN

Product selection table

Table 1. Device Summary

Device name	Flash	SRAM	SPI	UART	I2C	OPAMP (COMP)	TIMER	MPWM	ADC	I/O ports	Package
A33M116RL	256KB	16KB	2	4	2	4	8	2	16	56	LQFP-64
A33M116RM*	256KB	16KB	2	4	2	4	8	2	16	56	LQFP-64
A33M114RL*	128KB	16KB	2	4	2	4	8	2	16	56	LQFP-64
A33M116CL*	256KB	16KB	2	3	2	4	8	2	20	45	LQFP-48
A33M114CL*	128KB	16KB	2	3	2	4	8	2	20	45	LQFP-48
A33M114SN*	128KB	16KB	2	3	2	4	8	2	16	41	LQFP-44

* For available options or further information on the devices marked with "*", please contact the ABOV sales offices.

Contents

List of figures

List of tables

1 Description

A33M11x series is a 32-bit high-performance microcontroller with up to 256KB of flash memory. It is a powerful microcontroller which provides effective solutions to various electrical appliances which require both low power consumption and high performance.

1.1 Device overview

In this section, features of A33M11x series and peripheral counts are introduced.

Table 2. A33M11x Series Features and Peripheral Counts

Peripherals		Description
Core	CPU	• Maximum operating frequency: 96MHz • 32-bit ARM Cortex-M3 CPU • CPU register set: — Uses general-purpose registers specified by the 32-bit Thumb®-2 instruction set — Main stack pointer (MSP) and process stack pointer (PSP): R13 — Link register (LR): R14 — Program counter (PC): R15 • Data ordering format: Little-Endian • Harvard Architecture • AHB/APB
	Interrupt	• NVIC (Nested-Vectored Interrupt Controller) • Up to 86 peripheral interrupts supported. • Assignable with 16 different priority levels
Memory	Code flash	• Capacity : — A33M116: 256KB code flash memory — A33M114: 128KB code flash memory • A high-capacity code flash memory built in • Max 28MHz flash access speed • 512-B, 2-KB erases • Bulk erase • Read protection • Self-programming • CRC code generation and verification for the flash memory • Endurance: 10,000 cycles • Retention: 10 years

Table 2. A33M11x Series Features and Peripheral Counts (continued)

Peripherals		Description
	Data Flash	• Capacity: 32 KB • Max 28MHz access speed • 512-B, 2-KB erases • CRC code generation and verification for the flash memory • Endurance: 100,000 Cycle • Retention: 10 years
	BOOT ROM	• Executes the processor's boot mode when receiving an input at the boot pin from an external circuit • UART boot modes • In-system programming — A user can program data into the internal flash memory by setting an application board.
	SRAM	• Capacity: 16 KB • Usable as a program's work area • High-speed execution enables the execution of time-critical codes • Part of the SRAM can be remapped into an interrupt vector area
System Control Unit (SCU)	Operating frequency	• Up to 96Mhz
	Clock	• High speed internal oscillator (HSI) — 32MHz (±1.5% @-40℃ to +105℃) • Low speed internal oscillator (LSI) — 500KHz (±30% @-40℃ to +105℃) • External main oscillator (HSE): 4MHz to 16MHz • Phase-locked loop (PLL) frequency generator generates a high-speed clock (up to 96MHz)
System Control Unit (SCU)	Clock monitoring	• System Fail-Safe function by Clock Monitoring — External main oscillator(HSE) — Main system clock (MCLK)
	Operating mode	• RUN mode • SLEEP mode • STOP mode
	Reset	• nRESET pin reset • Core reset • Software reset • POR (Power On Reset) • LVR (Low Voltage Reset) • WDTR (Watch Dog Timer Reset) • Reset due to clock oscillating error
	LDO	• Low-dropout (LDO) regulator built in for low-voltage operation
	POR	• The POR generator detects an internal VDC voltage and generates a reset signal
	LVI	• Supports interrupts • Supports wake-up from sleep mode
	Wake-up	• Wake-up by a general-purpose input/output (GPIO) pin • Wake-up by a free-run timer (FRT) • Wake-up by a watchdog timer (WDT) • Wake-up by a low-voltage indicator (LVI) • Wake-up by a Systick timer (SYSTICK)
General Purpose I/O (GPIO)		• Input/output (I/O) port for general purposes • LQFP-64 — I/O pins: 56 • LQFP-48 — I/O pins: 45 • LQFP-44 — I/O pins: 41

Table 2. A33M11x Series Features and Peripheral Counts (continued)

Peripherals		Description
		• Each pin can be set for one of the following modes: — Push-pull output — Open drain output — Input • The use of each pin can be set by setting the mux • Each pin can be configured as an external interrupt source, either the high-/low-level interrupt or the rising-/falling-edge interrupt • Pull-up/pull-down/debouncing can be set for each pin • Drive strength can be adjusted for each port pin • Each pin bit can be individually set/reset • Wake-up events triggered by external asynchronous inputs
Direct Memory Access Controller (DMA)		• 8-ch direct memory access (DMA) support peripherals • 8-/16-/32-bit data transfers • Compatible with 15 different types of peripherals — SPI0, SPI1, UART0, UART1, UART2, UART3, CRC, ADC0, ADC1
TIMER	16-bit Timer	• General-purpose 16-bit up-count timer • 8 channels — 8 timer n capture port (TnIO) input channels — 8 timer n output port (TnIO) output channels • Timer operating modes — Periodic timer mode — One-shot mode — PWM mode — Capture mode • Interrupt events — Timer/counter match interrupt — Timer overflow interrupt • Input clock selection — Clocks are freely selectable through the miscellaneous clock control registers (MCCRs) — External clocks are selectable • Timer signals can be generated through TnIO pins • 10-bit prescaler
	WDT	• 32-bit down-count timer • Reset and periodic interrupts • Clocks are freely selectable through the miscellaneous clock control registers (MCCRs) • Eight different prescalers are selectable
	FRT	• 32-bit free-run timer — Capable of calculating the internal system time — 32-bit up-count timer • Interrupt events — Period interrupt — Overflow interrupt
Serial Interface	UART	• A total of four 16450 asynchronous serial communication ports • Configurable standard asynchronous communication bits (start, stop, and parity) • Flexible communication available through programming — 5- to 8-bit data transfers — Even-/odd-/non-parity generation and checking — 1-, 1.5-, or 2-stop bit generation and checking • 8-bit fraction controller and 16-bit baud rate generator
	SPI	• Two synchronous serial communication port channels • Master/slave operation

Table 2. A33M11x Series Features and Peripheral Counts (continued)

Peripherals		Description
		• Loop-back mode • Programmable and flexible communication — 8-/9-/16-/17-bit data transmit/receive — SPI clock speed — Both least significant bit (LSB)-first and most significant bit (MSB)-first modes available
	I2C	• Standard I2C communication protocol • Two channels supported • Master and slave modes supported for each channel • 7-bit addressing supported for slave mode • SCL signal's high/low periods and SDA signal's hold time settable
Motor Pulse-Width Modulation	MPWM	• Two MPWM generators • Six channels (high and low signals of phases U, V, and W) generate different waveforms • 16-bit up-/down-counters • Six ADC trigger sources • Interrupt events — Bottom interrupts — Top (period) interrupts • Interval interrupt mode • Falling/rising dead time applicable • A special operating mode: — Phases U, V, and W are independently controlled — Different carrier counters running for phases U, V, and W — Different duties and periods configurable for phases U, V, and W — Different interrupts used for phases U, V, and W — Capture functionality • Protection and over-voltage detection supported
Quadrature Encoder Interface	QEI	• Two QEI channels • Three input pins for two phase signals and an index pulse • Programmable noise input filters • Displays counter pulses and counter direction • 32-bit up-/down-counters • Velocity capture using a timer
12-bit A/D Converter	ADC	• Two independent ADC blocks • 22 analog input channels • A number of operating modes: — Single conversion — Sequence conversion — Burst conversion — Multiple conversion • Up to eight sequential conversions supported • Software triggers supported • Three internal trigger sources (MPWM and timers) supported • Sample time and hold time are adjustable
Analog Front End	AFE	• 4 channels of OPAMP that can operate independently of the comparator • Available to connect with ADC
Cyclic Redundancy Check	CRC	• CRC operating modes: — CRC32 (0x04C1_1DB7) — CRC16 (0x8005) — CRC8 (0x07) — CRC7 (0x09) • Input/output data reversion supported • Compatible with DMA

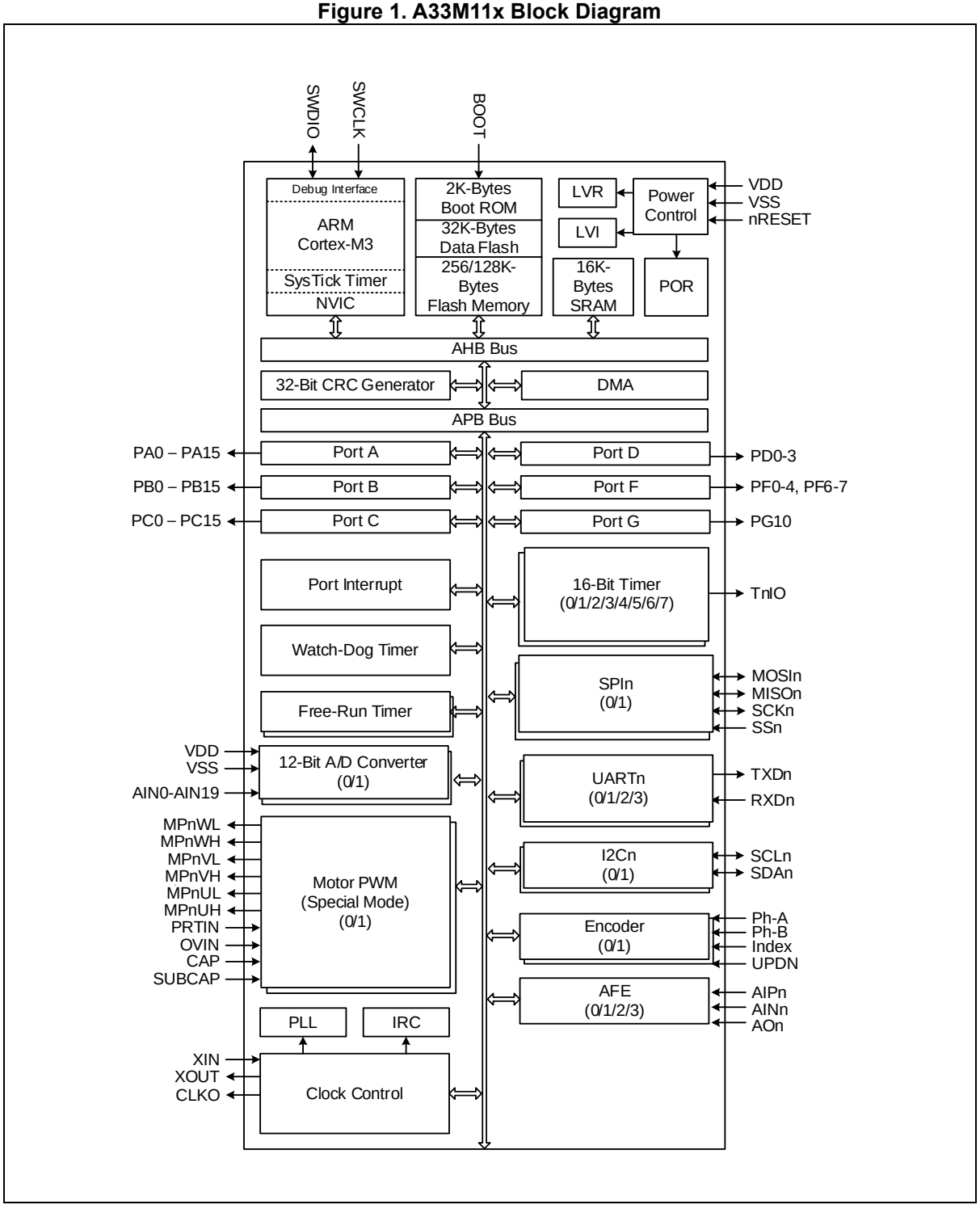
Table 2. A33M11x Series Features and Peripheral Counts (continued)

Peripherals	Description
Operating Voltage	• 2.5V to 5.5V
Operating temperature	• Commercial grade (-40℃ to +105℃)
Package	• Three types of package options — LQFP-64 — LQFP-48 — LQFP-44

1.2 Block diagram

In this section, the A33M11x series with peripherals is described in block diagram.

Figure 1. A33M11x Block Diagram



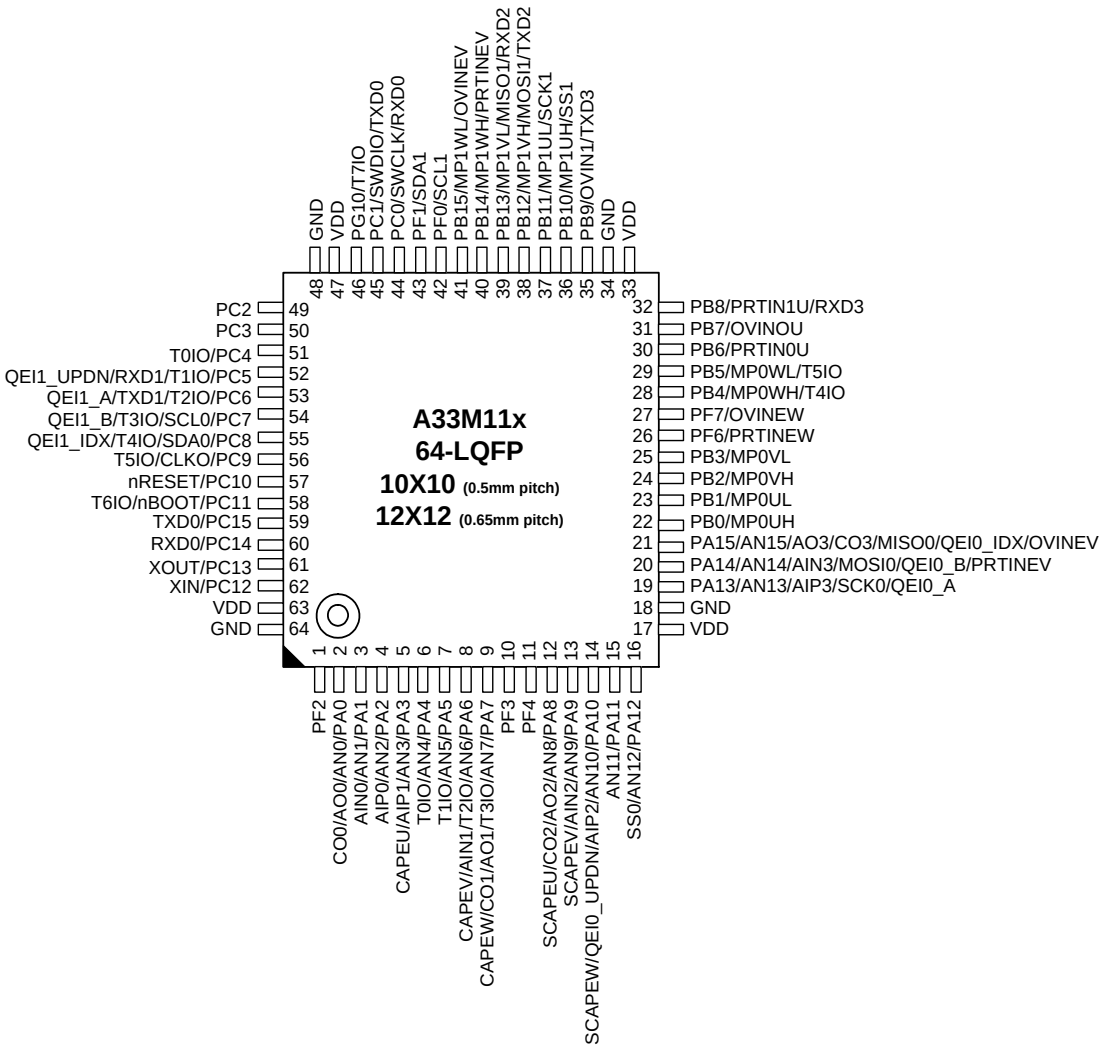
2 Pinouts and pin descriptions

In this chapter, pinouts and pin descriptions of the A33M11x series are introduced.

2.1 Pinouts

2.1.1 A33M116RL/A33M116RM/A33M114RL (LQFP-64)

Figure 2. LQFP 64 Pinouts

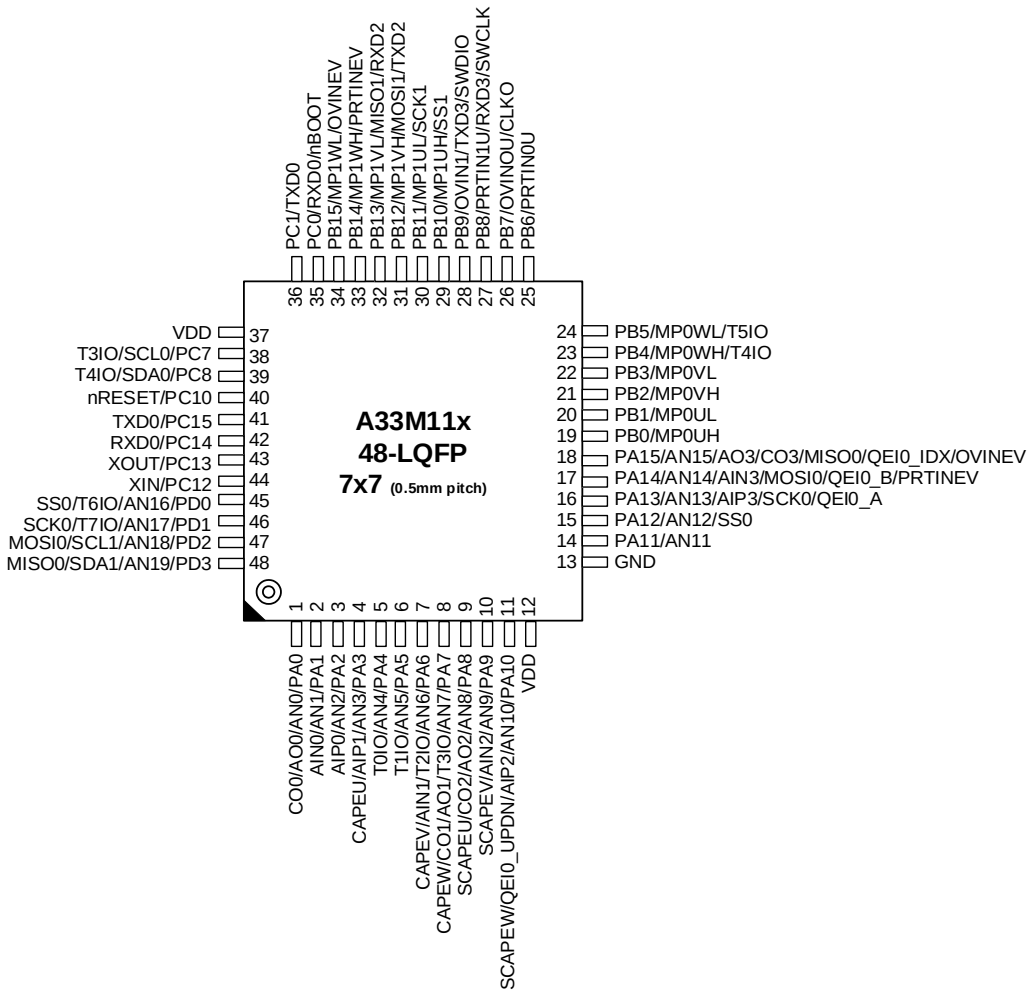


NOTES:

1. PC[8:7] are Open-drain pins. When using a port corresponding to these pins for Timer, I2C, QEI, etc., applications must use external Pull-up resistors.
2. Since the 64-pin package, the 48-pin and 44-pin package of the A33M11x series have different Boot pins and SWD pins (SWDIO, SWCLK), users need to be careful to set ports.
   - 64-pin package: PC0(PC_MR1.P0MUX:0b011/SWCLK), PC1(PC_MR1.P1MUX:0b011/SWDIO), PC11(PC_MR2.P11MUX:0b011/nBOOT)
   - 48-pin and 44-pin package: PB8(PB_MR2.P8MUX:0b100/SWCLK), PB9(PB_MR2.P9MUX:0b100/SWDIO), PC0(PC_MR1.P0MUX:0b100/nBOOT)

2.1.2 A33M116CL/A33M114CL (LQFP-48)

Figure 3. LQFP 48 Pinouts

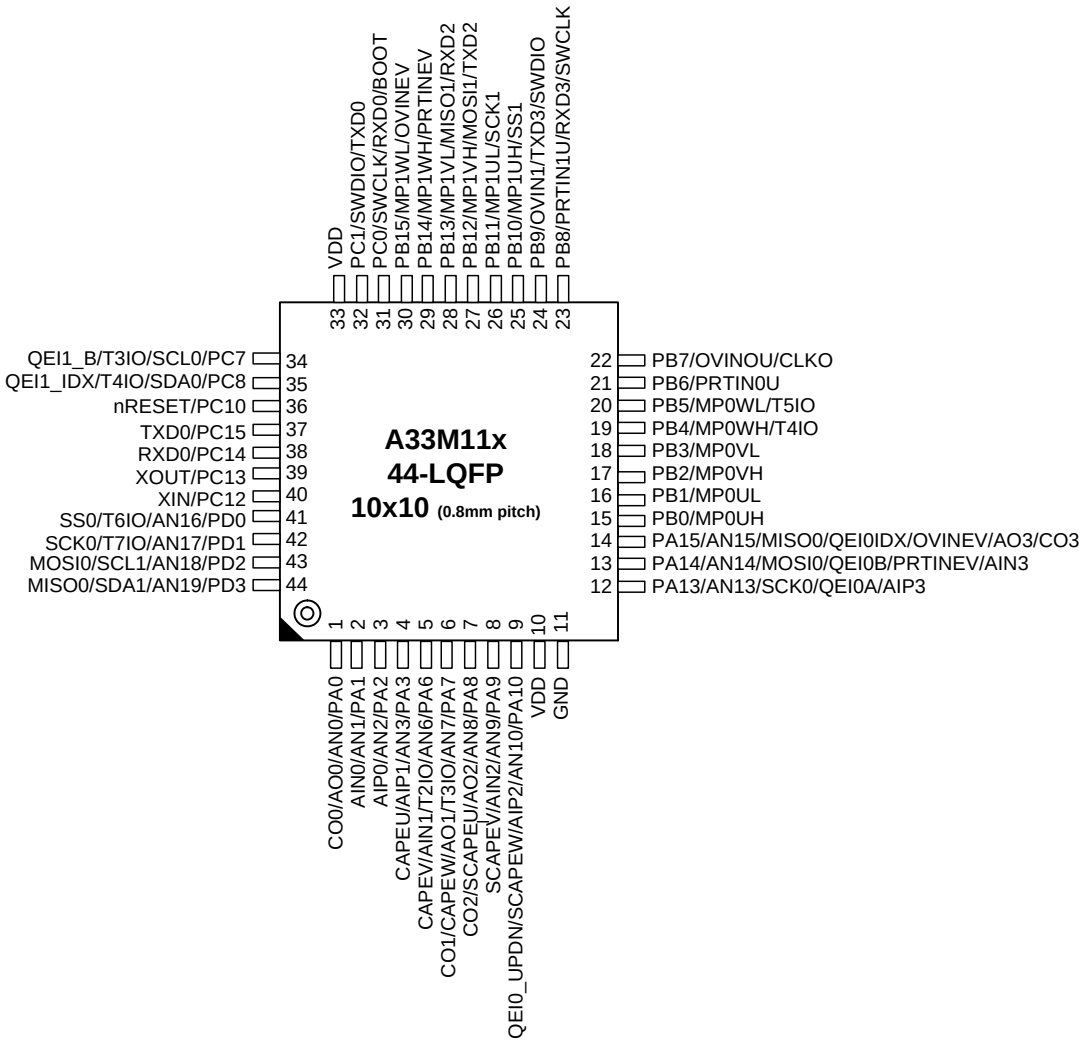


NOTES:

1. PC[8:7] are Open-drain pins. When using a port corresponding to these pins for Timer, I2C, QEI, etc., applications must use external Pull-up resistors.
2. Since the 64-pin package, the 48-pin and 44-pin package of the A33M11x series have different Boot pins and SWD pins (SWDIO, SWCLK), users need to be careful to set ports.
   - 64-pin package: PC0(PC_MR1.P0MUX:0b011/SWCLK), PC1(PC_MR1.P1MUX:0b011/SWDIO), PC11(PC_MR2.P11MUX:0b011/nBOOT)
   - 48-pin and 44-pin package: PB8(PB_MR2.P8MUX:0b100/SWCLK), PB9(PB_MR2.P9MUX:0b100/SWDIO), PC0(PC_MR1.P0MUX:0b100/nBOOT)

2.1.3 A33M114SN (LQFP-44)

Figure 4. LQFP 44 Pinouts



NOTES:

3. PC[8:7] are Open-drain pins. When using a port corresponding to these pins for Timer, I2C, QEI, etc., applications must use external Pull-up resistors.
4. Since the 64-pin package, the 48-pin and 44-pin package of the A33M11x series have different Boot pins and SWD pins (SWDIO, SWCLK), users need to be careful to set ports.
   - 64-pin package: PC0(PC_MR1.P0MUX:0b011/SWCLK), PC1(PC_MR1.P1MUX:0b011/SWDIO), PC11(PC_MR2.P11MUX:0b011/nBOOT)
   - 48-pin and 44-pin package: PB8(PB_MR2.P8MUX:0b100/SWCLK), PB9(PB_MR2.P9MUX:0b100/SWDIO), PC0(PC_MR1.P0MUX:0b100/nBOOT)

2.2 Pin description

Pin configuration information in Table 3 contains two pairs of power/ground and other dedicated pins. These multi-function pins have up to five selections of functions including GPIO. Configuration including pin ordering can be changed without notice.

Table 3. Pin Description

Pin no.			Pin name	Type	Description	Remark
64-pin	48-pin	44-pin				
1	-	-	PF2*	IOUDS	PORT F Bit 2 Input/Output	
2	1	1	PA0*	IOUDS	PORT A Bit 0 Input/Output	
			AN0	IA	Analog Input 0	
			AO0	AO	OPAMP0 Output	
			CO0	AO	Comparator0 Output	
3	2	2	PA1*	IOUDS	PORT A Bit 1 Input/Output	
			AN1	IA	Analog Input 1	
			AIN0	IO	OPAMP0 & Comparator0 Analog Input (-)	
4	3	3	PA2*	IOUDS	PORT A Bit 2 Input/Output	
			AN2	IA	Analog Input 2	
			AIP0	IO	OPAMP0 & Comparator0 Analog Input (+)	
5	4	4	PA3*	IOUDS	PORT A Bit 3 Input/Output	
			AN3	IA	Analog Input 3	
			AIP1	IO	OPAMP1 & Comparator1 Analog Input (+)	
			CAPEU	I	Extend PWM Capture U phase	
6	5	-	PA4*	IOUDS	PORT A Bit 4 Input/Output	
			AN4	IA	Analog Input 4	
			T0IO	IO	Timer 0 Input/Output	
7	6	-	PA5*	IOUDS	PORT A Bit 5 Input/Output	
			AN5	IA	Analog Input 5	
			T1IO	IO	Timer 1 Input/Output	
8	7	5	PA6*	IOUDS	PORT A Bit 6 Input/Output	
			AN6	IA	Analog Input 6	
			T2IO	IO	Timer 2 Input/Output	
			AIN1	IO	OPAMP1 & Comparator1 Analog Input (-)	
			CAPEV	I	Extend PWM Capture V phase	
9	8	6	PA7*	IOUDS	PORT A Bit 7 Input/Output	
			AN7	IA	Analog Input 7	
			T3IO	IO	Timer 3 Input/Output	
			AO1	AO	OPAMP1 Output	
			CO1	AO	Comparator1 Output	
			CAPEW	I	Extend PWM Capture W phase	
10	-	-	PF3*	IOUDS	PORT F Bit 3 Input/Output	
11	-	-	PF4*	IOUDS	PORT F Bit 4 Input/Output	

Table 3. Pin Description (continued)

Pin no.			Pin name	Type	Description	Remark
64-pin	48-pin	44-pin				
12	9	7	PA8*	IOUDS	PORT A Bit 8 Input/Output	
			AN8	IA	Analog Input 8	
			AO2	AO	OPAMP2 Output	
			CO2	AO	Comparator2 Output	
			SCAPEU	I	Extend PWM Sub Capture U phase	
13	10	8	PA9*	IOUDS	PORT A Bit 9 Input/Output	
			AN9	IA	Analog Input 9	
			AIN2	IO	OPAMP2 & Comparator 2 Analog Input (-)	
			SCAPEV	I	Extend PWM Sub Capture V phase	
14	11	9	PA10*	IOUDS	PORT A Bit 10 Input/Output	
			AN10	IA	Analog Input 10	
			AIP2	IO	OPAMP2 & Comparator2 Analog Input (+)	
			SCAPEU	I	Extend PWM Sub Capture U phase	
			QEI0_UDPN	O	QEI0 Output of Phase Direction	
15	14	-	PA11*	IOUDS	PORT F Bit 11 Input/Output	
			AN11	IA	Analog Input 11	
16	15	-	PA12*	IOUDS	PORT F Bit 12 Input/Output	
			AN12	IA	Analog Input 12	
			SS0	IO	SPI Channel 0 Select Signal Input/Output	
17	12	10	VDD	P	VDD	
18	13	11	GND	P	Ground	
19	16	12	PA13*	IOUDS	PORT A Bit 13 Input/Output	
			AN13	IA	Analog Input 13	
			SCK0	IO	SPI Channel 1 Clock Input/Output	
			QEI0_A	I	Input of QEI0 Phase A	
			AIP3	IO	OPAMP3 & Comparator3 Analog Input (+)	
20	17	13	PA14*	IOUDS	PORT A Bit 14 Input/Output	
			AN14	IA	Analog Input 14	
			MOSI0	IO	SPI Channel 0 Master Out/Slave In Signal	
			QEI0_B	I	Input of QEI0 Phase B	
			PRTINEV	I	Extend PWM Phase V Protection Input	
			AIN3	IO	OPAMP3 & Comparator3 Analog Input (-)	
21	18	14	PA15*	IOUDS	PORT A Bit 15 Input/Output	
			AN15	IA	Analog Input 15	
			MISO0	IO	SPI Channel 0 Master In/Slave Out Signal	
			QEI0_IDX	I	Input of QEI0 Index	
			OVINEV	I	Extend PWM Phase V Over-voltage Input	
			AO3	AO	OPAMP3 Output	
			CO3	AO	Comparator3 Output	
22	19	15	PB0*	IOUDS	PORT B Bit 0 Input/Output	
			MP0UH	O	PWM0 UH Output	
23	20	16	PB1*	IOUDS	PORT B Bit 1 Input/Output	
			MP0UL	O	PWM Channel 0 UL Output	
24	21	17	PB2*	IOUDS	PORT B Bit 2 Input/Output	
			MP0VH	O	PWM Channel 0 VH Output	
25	22	18	PB3*	IOUDS	PORT B Bit 3 Input/Output	
			MP0VL	O	PWM Channel 0 VL Output	
26	-	-	PF6*	IOUDS	PORT F Bit 6 Input/Output	
			PRTINEW	I	Extend PWM Phase W Protection Input	
27	-	-	PF7*	IOUDS	PORT F Bit 7 Input/Output	
			OVINEW	I	Extend PWM Phase W Over-voltage Input	
28	23	19	PB4*	IOUDS	PORT B Bit 4 Input/Output	
			MP0WH	Output	PWM Channel 0 WH Output	
			T4IO	IO	Timer 4 Input/Output	
29	24	20	PB5*	IOUDS	PORT B Bit 5 Input/Output	
			MP0WL	O	PWM Channel 0 WL Output	
			T5IO	IO	Timer 5 Input/Output	
30	25	21	PB6*	IOUDS	PORT B Bit 6 Input/Output	
			PRTIN0U	I	PWM0 Protection Input Signal Extend PWM 0 Phase U Protection Input	
31	26	22	PB7*	IOUDS	PORT B Bit 7 Input/Output	
			OVIN0U	I	PWM0 Over-voltage Input Signal Extend PWM 0 Phase U Over voltage Input	
			CLKO	O	System Clock Output	
32	27	23	PB8*	IOUDS	PORT B Bit 8 Input/Output	
			PRTIN1U	I	PWM1 Protection Input Signal Extend PWM 1 Phase U Protection Input	

Table 3. Pin Description (continued)

Pin no.			Pin name	Type	Description	Remark
64-pin	48-pin	44-pin				
			RXD3	I	UART Channel 3 RXD Input	
			SWCLK	I	SWD Clock Input	
33	-	-	VDD	P	VDD	
34	-	-	GND	P	Ground	
35	28	24	PB9*	IOUDS	PORT B Bit 9 Input/Output	
			OVIN1U	I	PWM1 Over-voltage Input Signal Extend PWM 1 Phase U Over voltage Input	
			TXD3	O	UART Channel 3 TXD Output	
			SWDIO	IO	SWD Data Input/Output	
36	29	25	PB10*	IOUDS	PORT B Bit 10 Input/Output	
			MP1UH	O	PWM Channel 1 UH Output	
			SS1	IO	SPI Channel 1 Select Signal Input/Output	
37	30	26	PB11*	IOUDS	PORT B Bit 11 Input/Output	
			MP1UL	O	PWM Channel 1 UL Output	
			SCK1	IO	SPI Channel 1 Clock Input/Output	
38	31	27	PB12*	IOUDS	PORT B Bit 12 Input/Output	
			MP1VH	O	PWM Channel 1 VH Output	
			MOSI1	IO	SPI Channel 1 Master Out/Slave In Signal	
			TXD2	O	UART Channel 2 TXD Output	
39	32	28	PB13*	IOUDS	PORT B Bit 13 Input/Output	
			MP1VL	O	PWM Channel 1 VL Output	
			MISO1	IO	SPI Channel 1 Master In/Slave Out Signal	
			RXD2	I	UART Channel 2 RXD Input	
40	33	29	PB14*	IOUDS	PORT B Bit 14 Input/Output	
			MP1WH	O	PWM Channel 1 WH Output	
			PRTINEV	I	Extend PWM Phase V Protection Input	
41	34	30	PB15*	IOUDS	PORT B Bit 15 Input/Output	
			MP1WL	O	PWM Channel 1 WL Output	
			OVINEV	I	Extend PWM Phase V Over-voltage Input	
42	-	-	PF0*	IOUDS	PORT F Bit 0 Input/Output	
			SCL1	O	I2C Channel 1 Output	
43	-	-	PF1*	IOUDS	PORT F Bit 1 Input/Output	
			SDA1	IO	I2C Channel 1 SDA Input/Output	
44	35	31	PC0	IOUDS	PORT C Bit 0 Input/Output	
			SWCLK*	I	SWD Clock Input	Pull-up
			RXD0	I	UART Channel 0 RXD Input	
			nBOOT	I	Boot Mode Selection Input	
45	36	32	PC1	IOUDS	PORT C Bit 1 Input/Output	
			SWDIO*	IO	SWD Data Input/Output	Pull-up
			TXD0	O	UART Channel 0 TXD Output	
46	-	-	PG10*	IOUDS	PORT G Bit 10 Input/Output	
			T7IO	IO	Timer 7 Input/Output	
47	37	33	VDD	P	VDD	
48	-	-	GND	P	Ground	
49	-	-	PC2*	IOUDS	PORT C Bit 2 Input/Output	
50	-	-	PC3*	IOUDS	PORT C Bit 3 Input/Output	
51	-	-	PC4*	IOUDS	PORT C Bit 4 Input/Output	
			T0IO	IO	Timer 0 Input/Output	
52	-	-	PC5*	IOUDS	PORT C Bit 5 Input/Output	
			T1IO	IO	Timer 1 Input/Output	
			RXD1	I	UART Channel 1 RXD Input	
			QEI1_UPDN	O	QEI1 Output of Phase Direction	
53	-	-	PC6*	IOUDS	PORT C Bit 6 Input/Output	
			T2IO	IO	Timer 2 Input/Output	
			TXD1	O	UART Channel 1 TXD Output	
			QEI1_A	I	Input of QEI1 Phase A	
54	38	34	PC7*	IOUDS	PORT C Bit 7 Input/Output	
			T3IO	IO	Timer 3 Input/Output	
			SCL0	O	I2C Channel 0 Output	Open-drain
			QEI1_B	I	Input of QEI1 Phase B	
55	39	35	PC8*	IOUDS	PORT C Bit 8 Input/Output	
			T4IO	IO	Timer 4 Input/Output	
			SDA0	IO	I2C Channel 0 SDA Input/Output	Open-drain
			QEI1_IDX	I	Input of QEI1 Index	
56	-	-	PC9*	IOUDS	PORT C Bit 9 Input/Output	

Table 3. Pin Description (continued)

Pin no.			Pin name	Type	Description	Remark
64-pin	48-pin	44-pin				
			T5IO	IO	Timer 5 Input/Output	
			CLKO	O	System Clock Output	
57	40	36	PC10	IOUDS	PORT C Bit 10 Input/Output	
			nRESET*	I	External Reset Input	Pull-up
58	-	-	PC11	IOUDS	PORT C Bit 11 Input/Output	
			T6IO	IO	Timer 6 Input/Output	
			nBOOT*	I	Boot Mode Selection Input	Pull-up
59	41	37	PC15*	IOUDS	PORT C Bit 15 Input/Output	
			TXD0	O	UART Channel 0 TXD Output	
60	42	38	PC14*	IOUDS	PORT C Bit 14 Input/Output	
			RXD0	I	UART Channel 0 RXD Input	
61	43	39	PC13*	IOUDS	PORT C Bit 13 Input/Output	
			XOUT	OA	External Crystal Oscillator Output	
62	44	40	PC12*	IOUDS	PORT C Bit 12 Input/Output	
			XIN	IA	External Crystal Oscillator Input	
-	45	41	PD0*	IOUDS	PORT D Bit 0 Input/Output	
			AN16	IA	Analog Input 16	
			T6IO	IO	Timer 6 Input/Output	
			SS0	IO	SPI Channel 0 Select Signal Input/Output	
-	46	42	PD1*	IOUDS	PORT D Bit 1 Input/Output	
			AN17	IA	Analog Input 17	
			T7IO	IO	Timer 7 Input/Output	
			SCK0	IO	SPI Channel 0 Clock Input/Output	
-	47	43	PD2*	IOUDS	PORT D Bit 2 Input/Output	
			AN18	IA	Analog Input 18	
			MOSI0	IO	SPI Channel 0 Mast Out/Slave Out Signal	
			SCL1	O	I2C Channel 0 Output	
-	48	44	PD3*	IOUDS	PORT D Bit 3 Input/Output	
			AN19	IA	Analog Input 19	
			MISO0	IO	SPI Channel 0 Master In/Slave Out Signal	
			SDA1	IO	I2C Channel 0 SDA Input/Output	
63	-		VDD	P	VDD	
64	-		GND	P	Ground	

NOTES:

1. I=Input, O=Output, U=Pull-up, D=Pull-down, S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
2. * means 'selected pin function after reset condition', which is a 64-pin standard.(The initial value of the pin is different depending on the package type)
3. Pin order may be changed with revision notice.
4. PC11 (nBOOT), PC10 (nRESET), PC1 (SWDIO) and PC0 (SWCLK) are the default pull-up pins.
5. Do not configure unused pins as floating inputs.
6. After a reset, the internal pull-up for the boot pin is enabled.
7. After a reset, the internal pull-up for the serial wire clock (SWCLK) and the serial wire data I/O (SWDIO) is enabled.
8. The SWCLK and SWDIO pins should not be switched to other functions while they are being used.
9. PC7-8 pins are open-drain ports.
10. When a function other than a clock is set through the PC12 (XIN) and PC13 (XOUT) pins, other functions than the set clock will not operate normally if the clock is enabled by software.

3 System and memory overview

3.1 System architecture

Main system of A33M11x series consists of the followings:

- ARM® Cortex-M3 core
- General purpose DMA
- Internal SRAM, Flash memory
- Two AHB buses

3.1.1 Cortex-M3 core

The ARM® Cortex-M3 processor is a low-power processor that features low gate count, low interrupt latency, and low-cost debug. The processor is designed for embedded, high-level applications that require fast interrupt response, including microcontrollers, automatic and industrial control systems.

For detailed information on the Cortex-M3, refer to document DDI337 provided by the ARM.

3.1.2 Interrupt controller

Table 4. Interrupt Vector Map

Priority	Vector address	Interrupt source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Handler
-14	0x0000_0008	NMI Handler
-13	0x0000_000C	Hard Fault Handler
-12	0x0000_0010	MemManage Handler
-11	0x0000_0014	BusFault Handler
-10	0x0000_0018	UsageFault Handler
-9	0x0000_001C	Reserved
-8	0x0000_0020	
-7	0x0000_0024	
-6	0x0000_0028	
-5	0x0000_002C	SVCall Handler
-4	0x0000_0030	Debug Monitor Handler
-3	0x0000_0034	Reserved
-2	0x0000_0038	PenSV Handler
-1	0x0000_003C	SysTick Handler

Table 4. Interrupt Vector Map (continued)

Priority	Vector Address	Interrupt Source
0	0x0000_0040	LVI
1	0x0000_0044	SYSCLKFAIL
2	0x0000_0048	HSEFAIL
3	0x0000_004C	Reserved
4	0x0000_0050	
5	0x0000_0054	
6	0x0000_0058	WDT
7	0x0000_005C	Reserved
8	0x0000_0060	FRT0
9	0x0000_0064	Reserved
10	0x0000_0068	
11	0x0000_006C	CFMC
12	0x0000_0070	DFMC
13	0x0000_0074	Reserved
14	0x0000_0078	
15	0x0000_007C	TIMER0
16	0x0000_0080	TIMER1
17	0x0000_0084	TIMER2
18	0x0000_0088	TIMER3
19	0x0000_008C	TIMER4
20	0x0000_0090	TIMER5
21	0x0000_0094	TIMER6
22	0x0000_0098	TIMER7
23	0x0000_009C	Reserved
24	0x0000_00A0	
25	0x0000_00A4	
26	0x0000_00A8	
27	0x0000_00AC	
28	0x0000_00B0	
29	0x0000_00B4	
30	0x0000_00B8	
31	0x0000_00BC	QEI0
32	0x0000_00C0	QEI1

Table 4. Interrupt Vector Map (continued)

Priority	Vector Address	Interrupt Source
33	0x0000_00C4	Reserved
34	0x0000_00C8	
35	0x0000_00CC	
36	0x0000_00D0	GIPOA
37	0x0000_00D4	GPIOB
38	0x0000_00D8	GPIOC
39	0x0000_00DC	GPIOD
40	0x0000_00E0	Reserved
41	0x0000_00E4	GPIOF
42	0x0000_00E8	GPIOG
43	0x0000_00EC	Reserved
44	0x0000_00F0	
45	0x0000_00F4	MPWM0PROT
46	0x0000_00F8	MPWM0OVV
47	0x0000_00FC	MPWM0(U)
48	0x0000_0100	MPWM0(V)
49	0x0000_0104	MPWM0(W)
50	0x0000_0108	MPWM1PROT
51	0x0000_010C	MPWM1OVV
52	0x0000_0110	MPWM1(U)
53	0x0000_0114	MPWM1(V)
54	0x0000_0118	MPWM1(W)
55	0x0000_011C	SPI0
56	0x0000_0120	SPI1
57	0x0000_0124	Reserved
58	0x0000_0128	
59	0x0000_012C	
60	0x0000_0130	I2C0
61	0x0000_0134	I2C1
62	0x0000_0138	Reserved
63	0x0000_013C	UART0
64	0x0000_0140	UART1
65	0x0000_0144	UART2
66	0x0000_0148	UART3
67	0x0000_014C	Reserved
68	0x0000_0150	
69	0x0000_0154	
70	0x0000_0158	
71	0x0000_015C	
72	0x0000_0160	
73	0x0000_0164	
74	0x0000_0168	ADC0
75	0x0000_016C	ADC1
76	0x0000_0170	Reserved
77	0x0000_0174	
78	0x0000_0178	
79	0x0000_017C	AFE0
80	0x0000_0180	AFE1
81	0x0000_0184	AFE2
82	0x0000_0188	AFE3
83	0x0000_018C	Reserved
84	0x0000_0190	
85	0x0000_0194	CRC

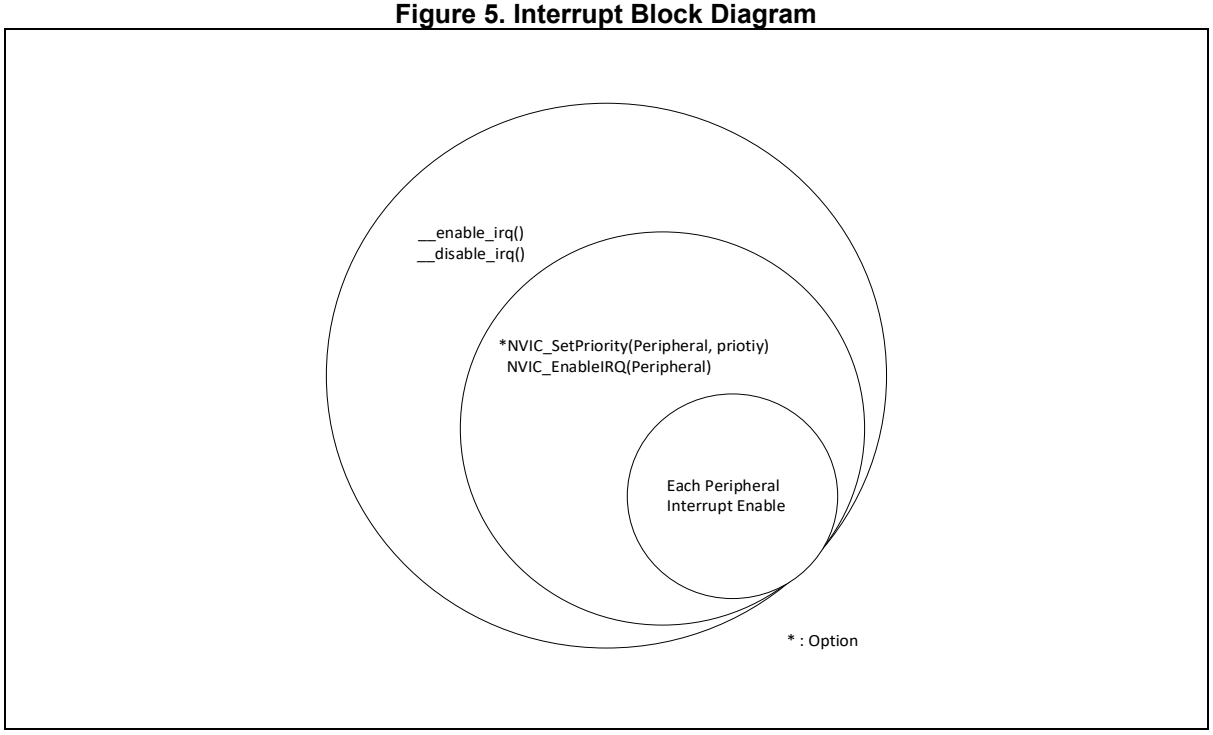
NOTES:

1. Each Interrupt Priority Level Register occupies 1 byte (8 bits).NVIC registers in the Cortex-M3 processor

can only be accessed using word-size transfers, so for each access, four Interrupt Priority Level Registers are accessed at the same time.
** __NVIC_PRIO_BITS = 4

2. Figure 5 is a caution when using Peripheral Interrupts. Interrupt don’t work if only peripheral interrupts are enabled. Enable the function in core to enable interrupt.
* __enable_irq > NVCI_EnableIRQ(Peripheral) > Each Peripheral Interrupt

Figure 5. Interrupt Block Diagram



3.2 Memory organization

Program memory, data memory, registers and I/O ports are organized in the same address space.

3.2.1 Register boundary address

Table 5 gives the boundary address assigned for each peripheral of the A33M11x series.

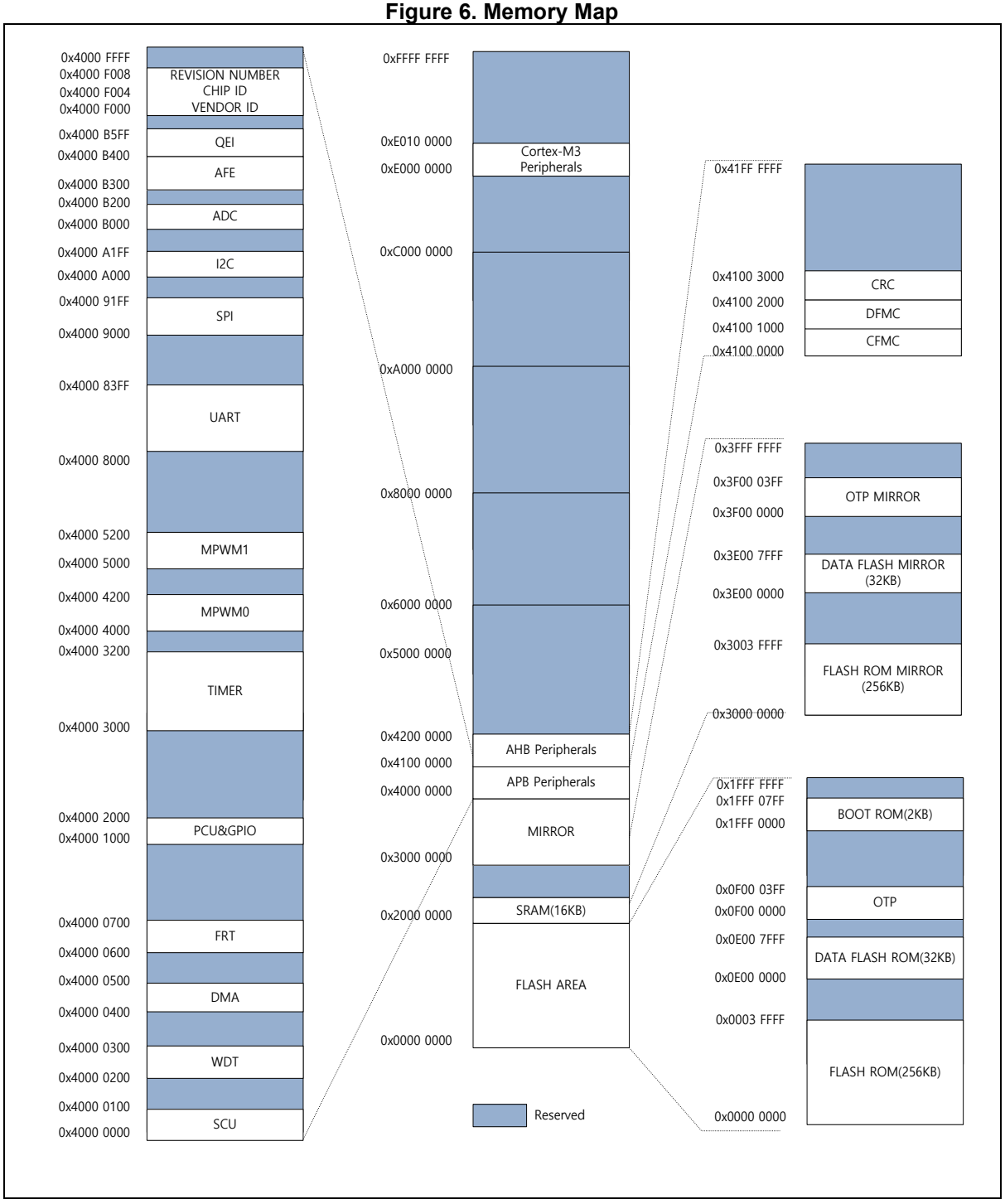
Table 5. A33M11x Memory Boundary Addresses

Boundary address	Memory area
0x4000_0000	SCU
0x4000_0200	WDT
0x4000_0400	DMA 0/1/2/3/4/5/6/7
0x4000_0600	FRT
0x4000_1000	PCU A/B/C/D/F/G
0x4000_3000	TIMER 0/1/2/3/4/5/6/7
0x4000_4000	MPWM0
0x4000_5000	MPWM1
0x4000_8000	UART 0/1/2/3
0x4000_9000	SPI 0/1
0x4000_A000	I2C 0/1
0x4000_B000	ADC 0/1
0x4000_B300	AFE 0/1/2/3
0x4000_B400	QEI 0/1
0x4100_0000	CFMC
0x4100_1000	DFMC
0x4100_2000	CRC
0x2000_0000	Internal SRAM

3.2.2 Memory map

Figure 6 shows addressable memory space in memory map.

Figure 6. Memory Map



3.2.3 Embedded SRAM

The A33M11x series has a block of 0-wait on-chip SRAM. Size of the SRAM is 16KB and its base address is 0x2000_0000.

This SRAM memory area is usually used for data memory and stack memory. Sometimes the code is dumped into the SRAM memory for fast operation or flash erase/programming operation. This device does not support memory remap strategy. So, jump and return are required to perform the code in SRAM memory area.

3.2.4 Flash memory overview

The A33M11x series provides internal 256KB code flash memory and a controller. This is enough to control the general system. Self-programming is available and ISP and SWD programming is also supported in boot mode or in debugging mode.

Instruction and data cache buffer are present and overcome the low bandwidth flash memory. CPU can access flash memory with one wait state up to 28MHz bus frequency.

3.2.5 Boot mode

3.2.5.1 Boot mode pins

The A33M11x series has a boot mode option to program internal flash memory. Boot mode can be entered by setting BOOT pin to ‘L’ at reset timing (Normal state is ‘H’).

Boot mode supports both of UART boot:

- UART boot uses TXD0/RXD0 ports.

Pins for the boot mode are listed in Table 6.

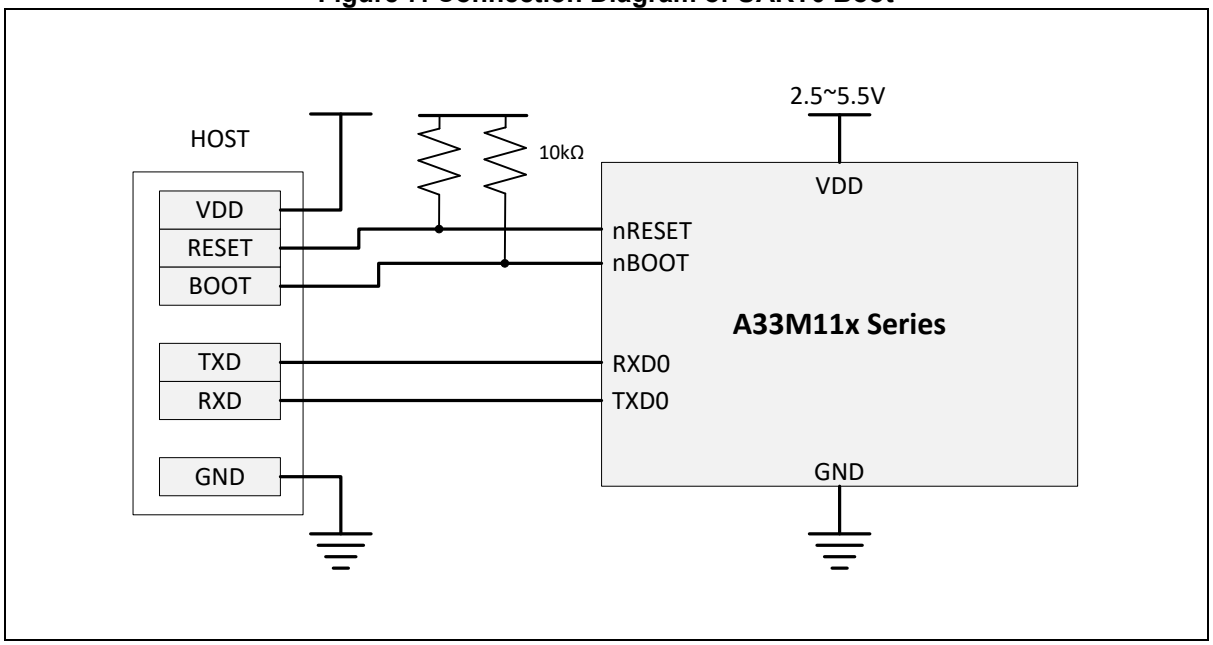
Table 6. Boot Mode Pin List

Block	Pin name	Direction	Description
SYSTEM	nRESET/PC10	I	Reset input signal
	nBOOT/PC11	I	Boot mode setting pin
UART0	RXD0/PC14	I	UART boot receive data
	TXD0/PC15	O	UART boot transmit data

3.2.5.2 Boot mode connections

Users can design a target board using boot mode ports such as UART0. Sample connection diagrams of boot mode are introduced in the following figures:

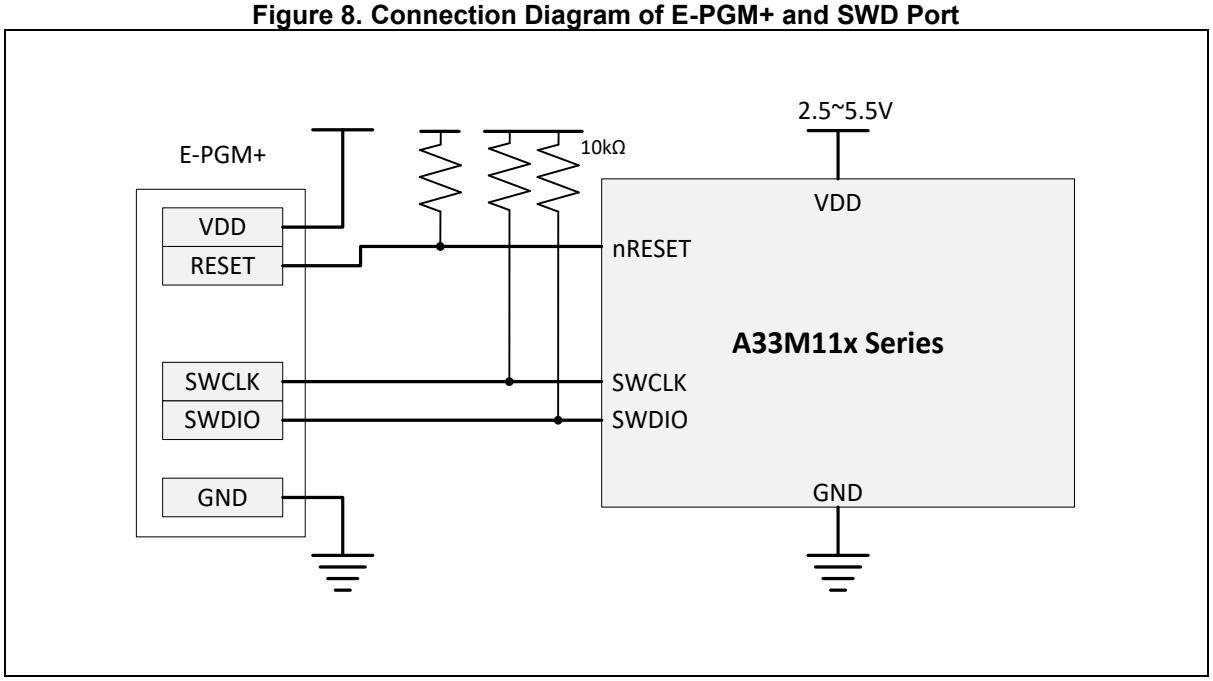
Figure 7. Connection Diagram of UART0 Boot



3.2.5.3 SWD mode connections

Users can use SWD mode for writing with E-PGM+. This mode can be used for writing & debugging.

Figure 8. Connection Diagram of E-PGM+ and SWD Port



4 System Control Unit (SCU)

A33M11x series has a built-in intelligent power control block which manages system analog blocks and operating modes. System Control Unit (SCU) block controls an internal reset and clock signals to maintain optimize system performance and power dissipation.

Four pins in Table 7 are assigned for SCU block

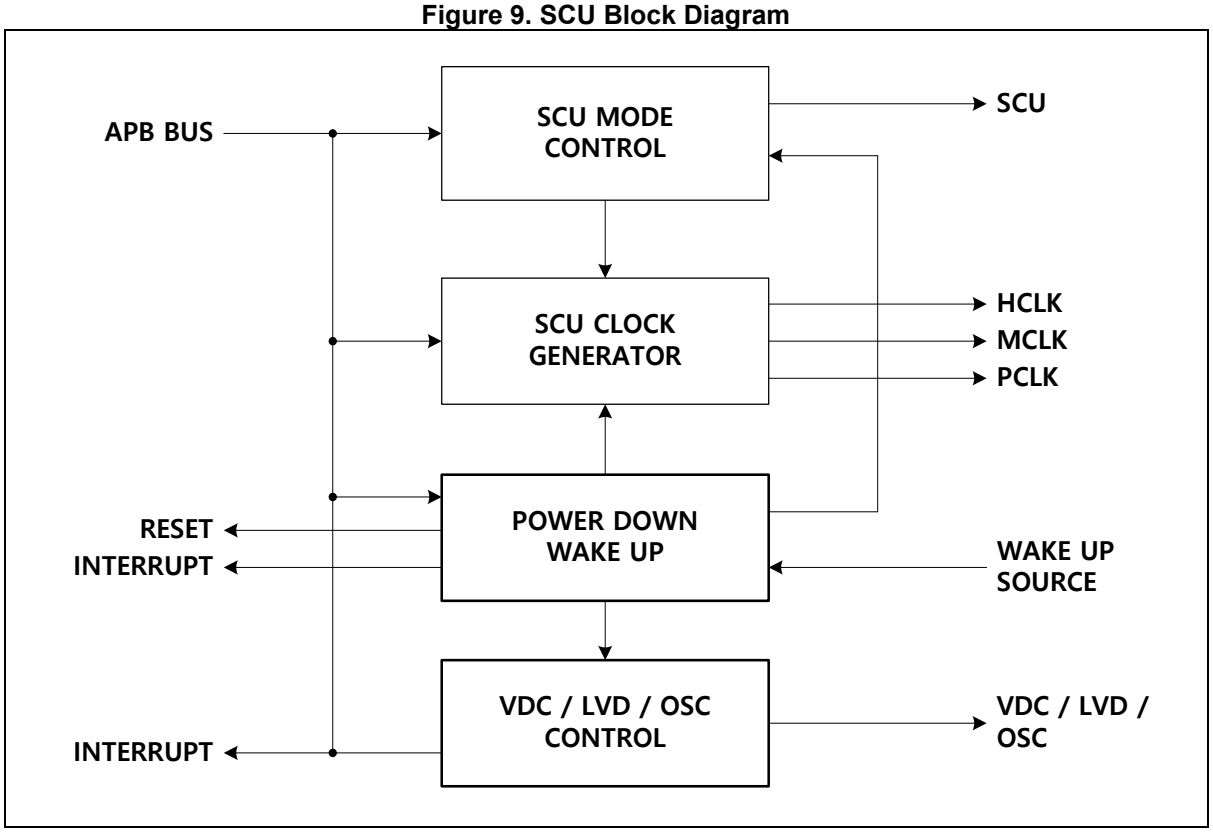
Table 7. SCU Pins

Pin name	Type	Description
nRESET	I	External Reset Input
XIN/XOUT	OSC	External Crystal Oscillator
CLKO	O	Clock Output Monitoring Signal

4.1 SCU block diagram

In this subsection, SCU block diagram is introduced in Figure 9.

Figure 9. SCU Block Diagram

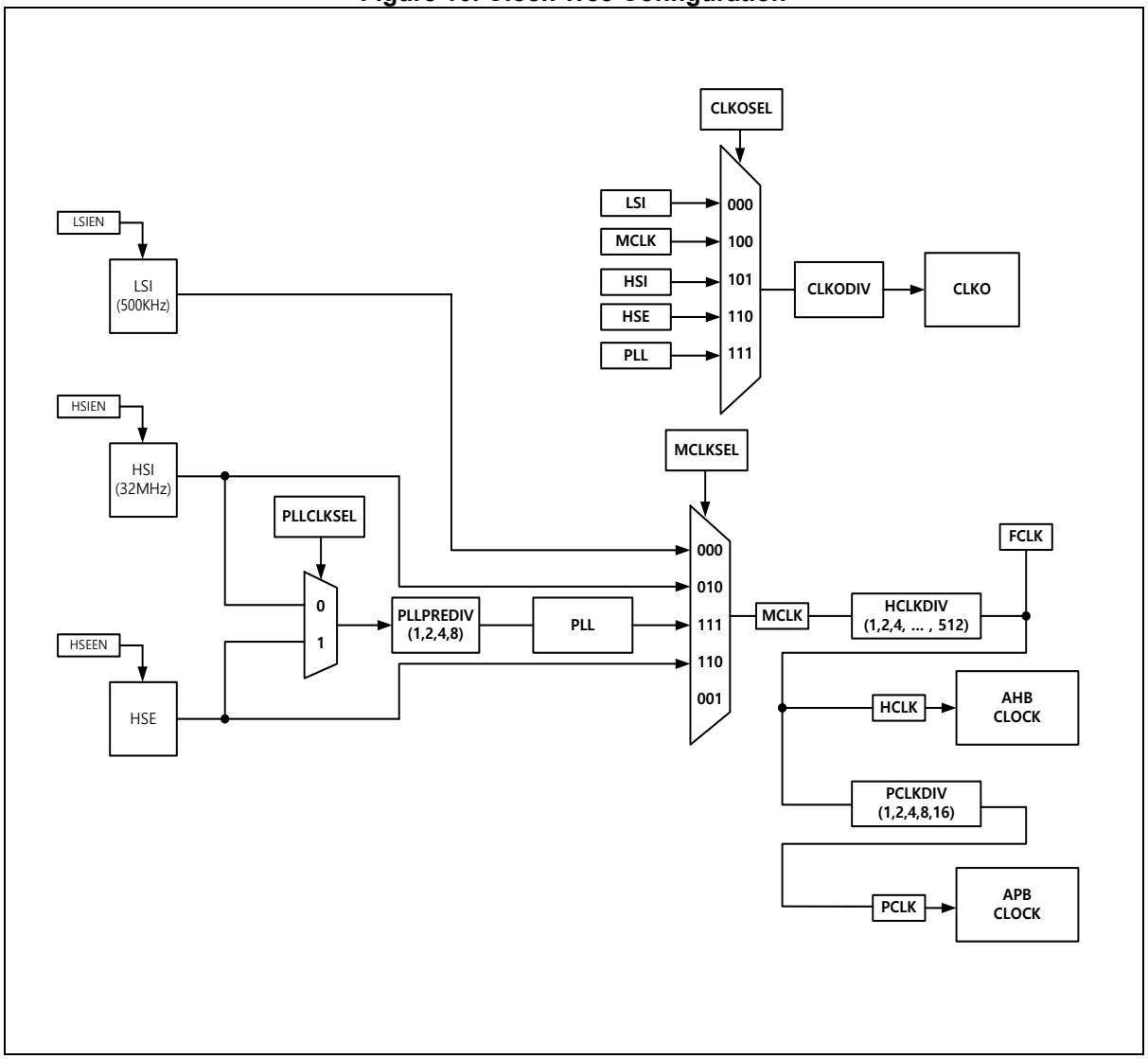


4.2 Clock system

A33M11x series has two main operating clocks. One is HCLK which produces a clock signal both for CPU and AHB bus system. The other is PCLK which produces a clock signal for peripheral systems.

A user can keep the clock system variation under software control. Through Figure 10 and Table 8, users learn about the clock system of A33M11x devices and clock sources.

Figure 10. Clock Tree Configuration



All multiplexers switching clock sources have a glitch-free circuit in each. So, a clock can be switched without glitch risks. When a user tries to change a clock mux control, both of clock sources must be alive. If one of them is not alive, clock change operation is stopped and system will be halted and not be recovered.

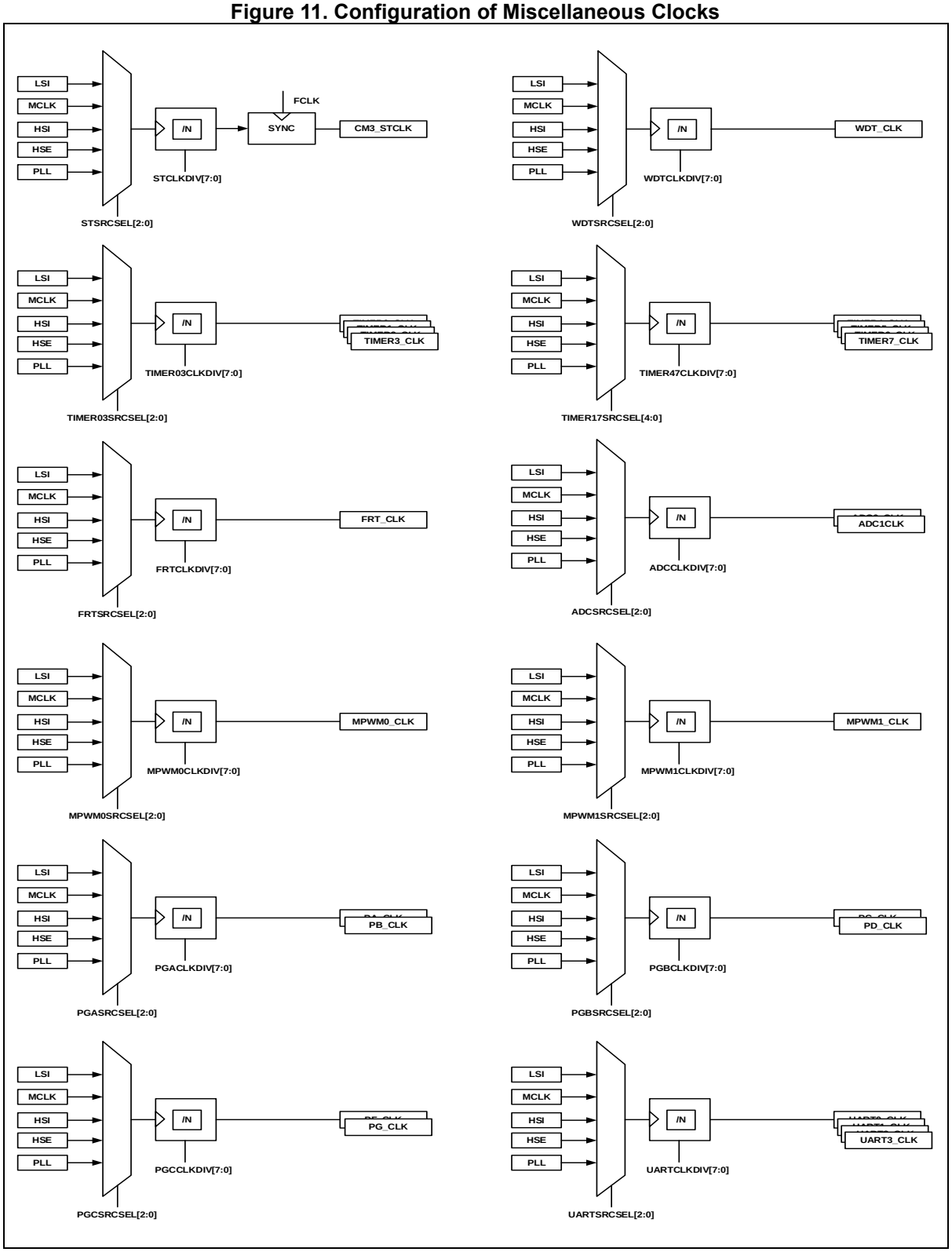
Table 8. Clock Sources

Clock name	Frequency	Description
HSE	4MHz to 16MHz	High Speed External Oscillator
PLL Clock	8MHz to 96MHz	On-chip PLL
HSI	32MHz	High Speed Internal OSC
LSI	500KHz	Low Speed Internal OSC

4.2.1 Configuration of miscellaneous clocks

The A33M11x series supports the “miscellaneous clocks” feature, which allows for assigning each peripheral with a different clock source (MCLK, HSE, PLL, LSI or HSI) at a different frequency division ratio. You can set each peripheral’s clock source and its frequency divider in the corresponding SCU_MCCR register. The supported division ratio can be one ranging from 1 to 255.

Figure 11. Configuration of Miscellaneous Clocks



4.2.2 HCLK clock domain

The HCLK is fed to the CPU and AHB. The Cortex-M3 CPU requires two clocks, the HCLK and FCLK. The FCLK stays enabled except in stop mode, whereas the HCLK can be disabled in idle mode.

The buses and memories are clocked by the HCLK. As the bus clock frequency is limited to a maximum of 96MHz, the HCLK frequency must not exceed 96MHz.

4.2.3 PCLK clock domain

The PCLK is used as a clock for any peripherals. Whether to enable or disable the PCLK for each peripheral is determined with the SCU_PCER registers; each peripheral block's registers cannot be read unless its PCLK input is enabled. And the PCLK stops operating in stop mode.

4.2.4 Clock configuration procedure

After the MCU is powered on, the LSI (500KHz) is initially enabled as the system clock source by default in the system operation sequence. Other clock sources are initially set by the user while the system is clocked by the LSI. The HSI (32MHz) can be enabled with SCU_CSCR (clock source control register). Before enabling the HSE block, the pin mux configuration should be set for XIN and XOUT. You must be careful not to affect other bits of PCC_MR and PCC_CR during this process. Once the HSE block has been enabled, you must wait for the crystal oscillation to stabilize.

The MCLK can be changed with SCU_SCCR (system clock source register). Figure 12 shows an example of how the system clock changes.

※ If you change the main clock from LSI (500kHz) to PLL 80MHz or higher, it is recommended to change it gradually in the order shown below:

— Change order: LSI → HSE → PLL

① Once the MCU is powered on, the system clock source is LSI (500kHz).

② Initialize Data and instruction cache, and then set flash wait to 7.

③ Set XIN and XOUT on pin MUX to use the HSE.

④ Enable the HSE.

⑤ Set additional time of about 1ms for clock stabilization.

⑥ Enable the PLL.

⑦ Set additional time of about 1us for clock stabilization.

⑧ Set the PLL options.

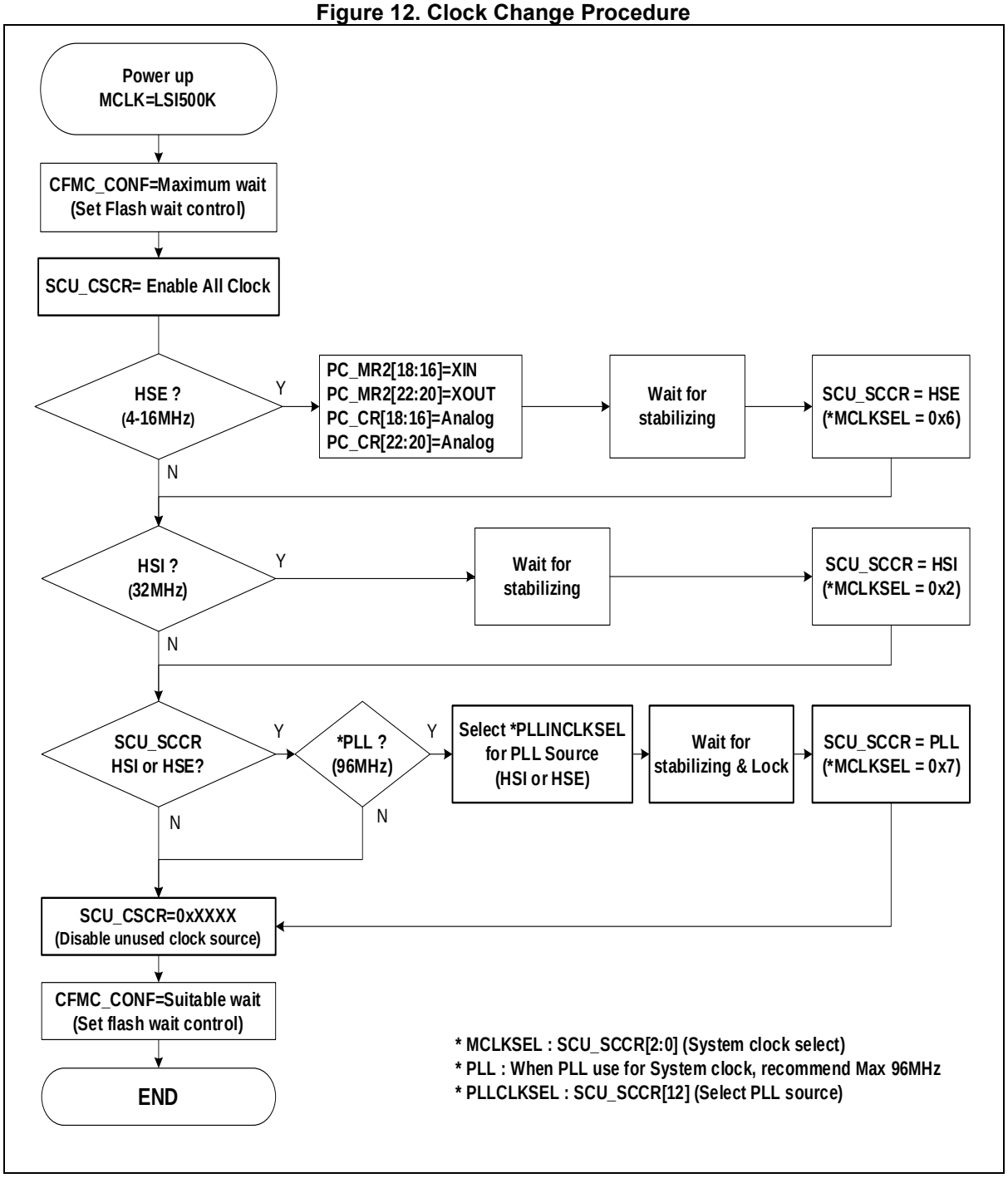
⑨ Set the HCLK to the MCLK divided by 2, and the PCLK to the HCLK.

⑩ Change the system clock source as the PLL.

⑪ Set the HCLK to the MCLK divided by 1, and the PCLK to the HCLK.

⑫ Set flash wait to 3.

Figure 12. Clock Change Procedure



When you speed up the system clock to the maximum operating frequency, you should check flash wait control configuration. Flash read access time is one of limitation factor for performance. The wait control recommendation is suggested in Table 9.

Table 9. Flash Wait Control Recommendation

FMCONF.WAIT	FLASH access wait	Available max. system clock frequency
0000	0-clock wait	Up to 28MHz
0001	1-clock wait	Up to 56MHz
0010	2-clock wait	Up to 84MHz
0011	3-clock wait	Up to 96MHz
0100	4-clock wait	Up to 96MHz
0101	5-clock wait	Up to 96MHz
0110	6-clock wait	Up to 96MHz
0111	7-clock wait	Up to 96MHz
1000	8-clock wait	Up to 96MHz
1001	9-clock wait	Up to 96MHz
1010	10-clock wait	Up to 96MHz
1011	11-clock wait	Up to 96MHz
1100	12-clock wait	Up to 96MHz
1101	13-clock wait	Up to 96MHz
1110	14-clock wait	Up to 96MHz
1111	15-clock wait	Up to 96MHz

Figure 13 shows how to set the peripheral clock. Selecting a peripheral clock is a typical method of MCCRn and PCLK.

Figure 13. Peripheral Clock Select (n = 1, 2, 3, 4, 5, 6 and 7)

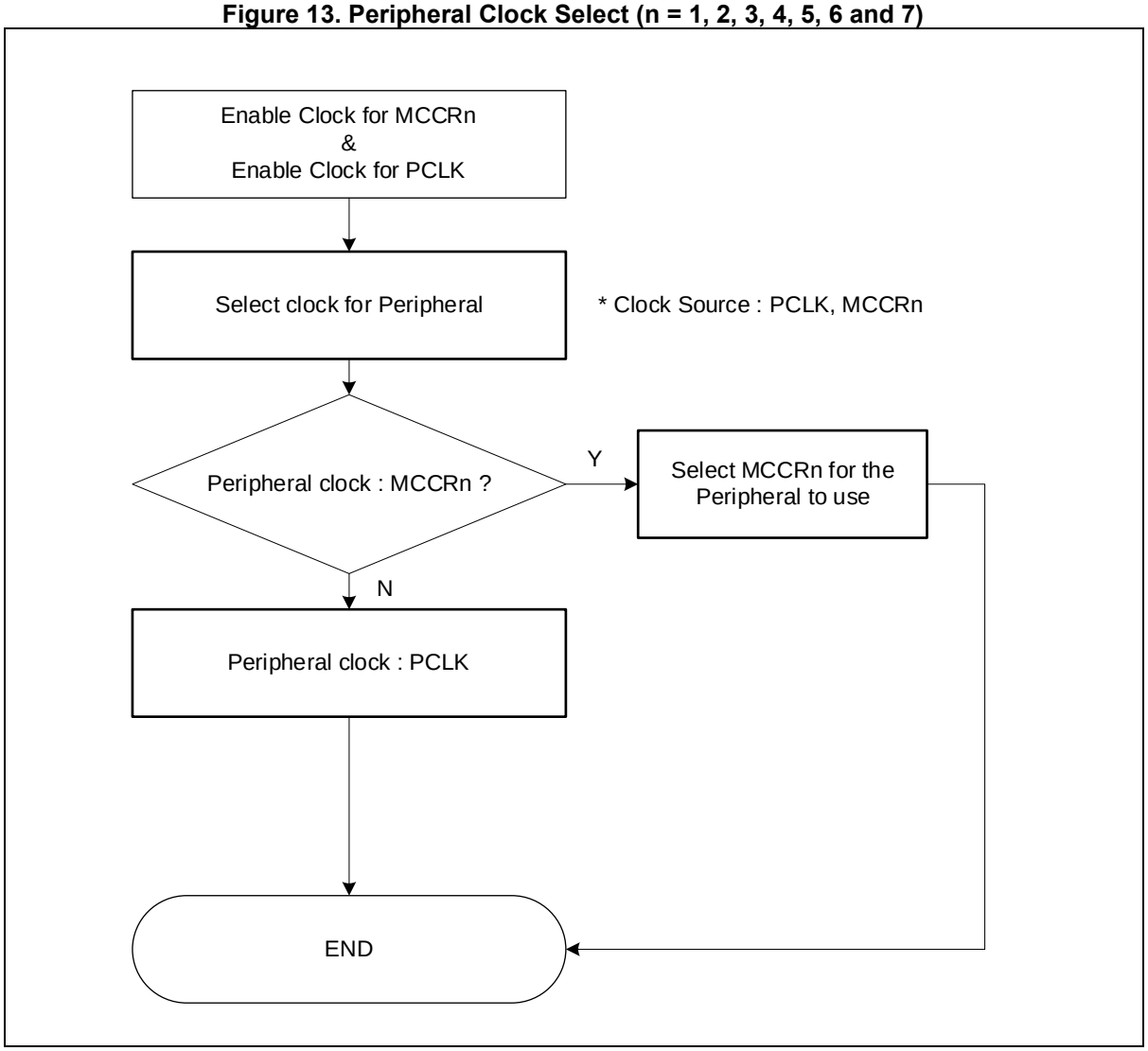


Table 10. Peripheral Clock Select

Peripheral	MCCRn	PCLK
Systick	MCCR1	O
WDT		O
MPWM0	MCCR2	N/A
MPWM1		N/A
TIMER03	MCCR3	O
TIMER47		O
ADC	MCCR4	O
PGAD		N/A
PGBD	MCCR5	N/A
PGCD		N/A
FRT	MCCR6	N/A
UART	MCCR7	N/A

4.3 Reset

The A33M11x series has two system reset options. One is a cold reset that is effective during power up or down sequence. The other is a warm reset which is generated by several reset sources. A reset event makes a chip to turn to an initial state. Reset sources of the cold reset and the warm reset are listed in Table 11.

Table 11. Reset Sources of Cold Reset and Warm Reset

	Cold reset	Warm reset
Reset sources	• POR	• nRESET Pin reset • LVR reset • WDT reset • MCLK Fail reset • HSE Fail reset • S/W reset • CPU request reset

4.3.1 Cold reset

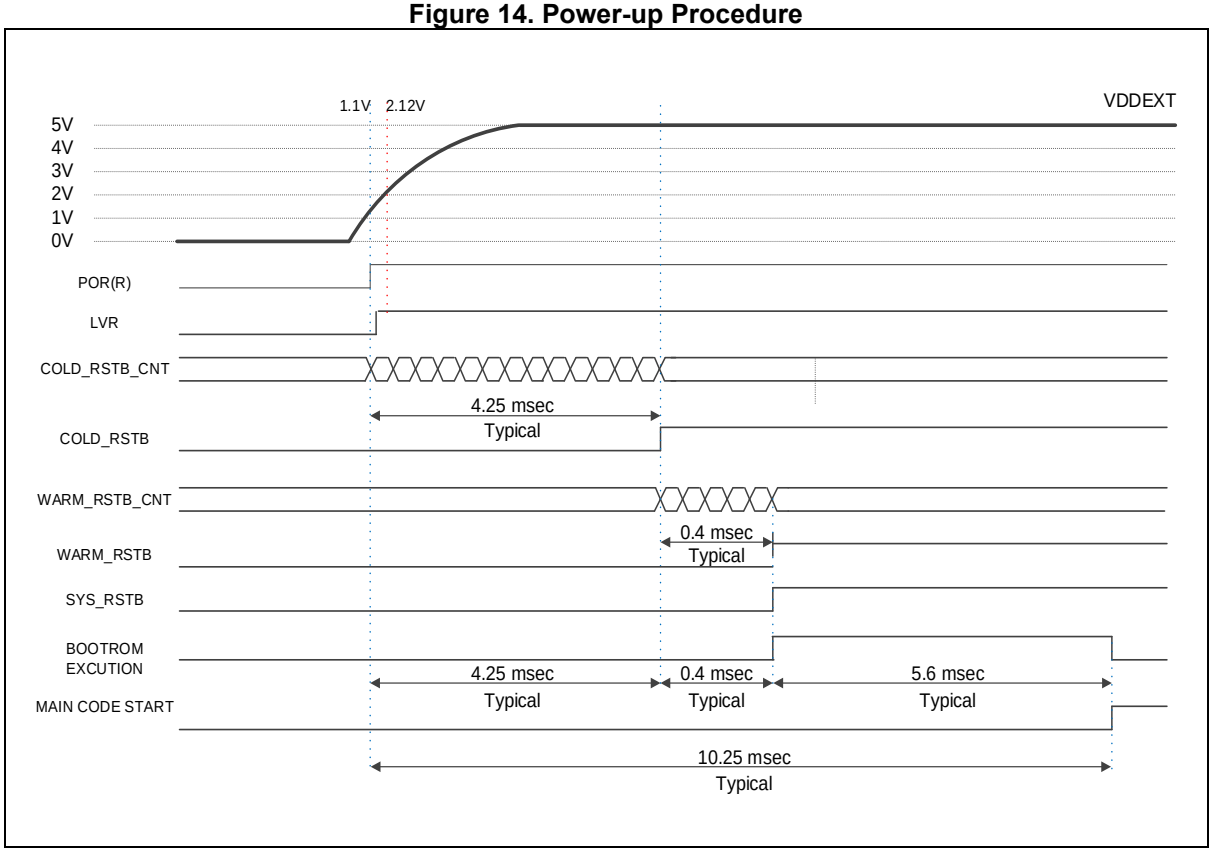
A cold reset plays an important role during a power-up process and affects the entire process of system booting.

The internal VDC becomes active as soon as the External VDD is turn on. The internal POR is triggered when the External VDD is determined to reach 1.1V based on the amount of the internal VDC output. During the cold reset process, when the applied voltage exceeds 1.1V, the LSI clock is enabled.

After the stabilization of the internal VDC level for 4.25msec, the internal logic is initialized. And then, when the external VDD voltage rises above the LVR voltage level (2.12V), the cold reset is released and, after a waiting time of 0.4ms for warm reset synchronization, booting begins.

Figure 14 shows the power-up process and the initial reset waveforms.

Figure 14. Power-up Procedure

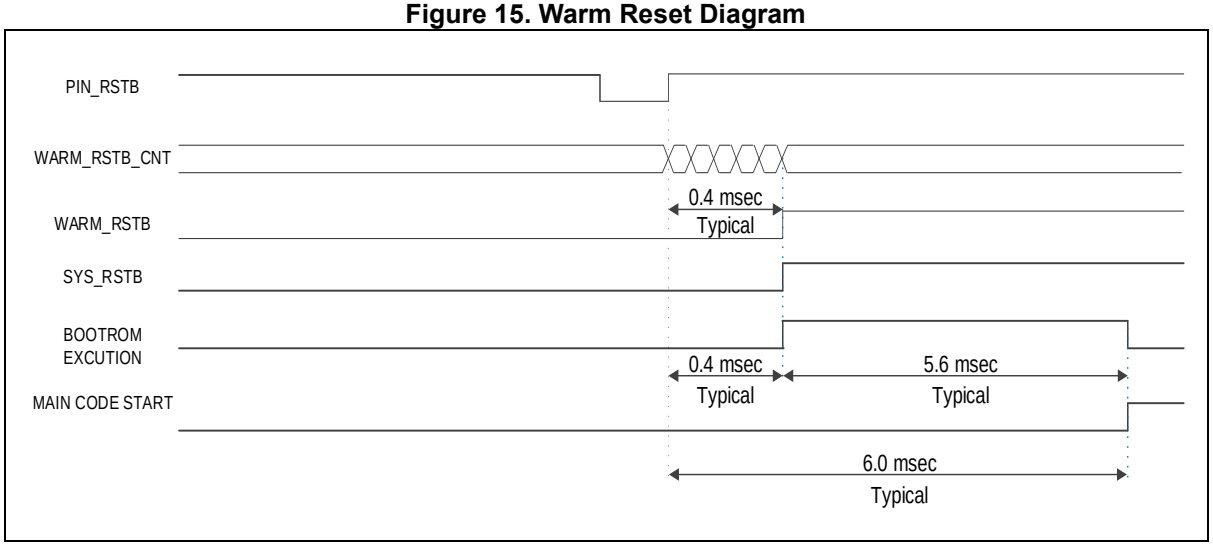


4.3.2 Warm reset

A warm reset event is triggered for system initialization when the conditions of an internally set reset source are met.

Warm reset sources are enabled or disabled by configuring SCU_RSER (reset source enable register), and their occurrence is written to SCU_RSSR (reset source status register). Which devices are to be initialized by a warm reset is determined by the settings of SCU_PRER (peripheral reset enable register). Using this register, a user can allow or disallow the initialization of each individual device.

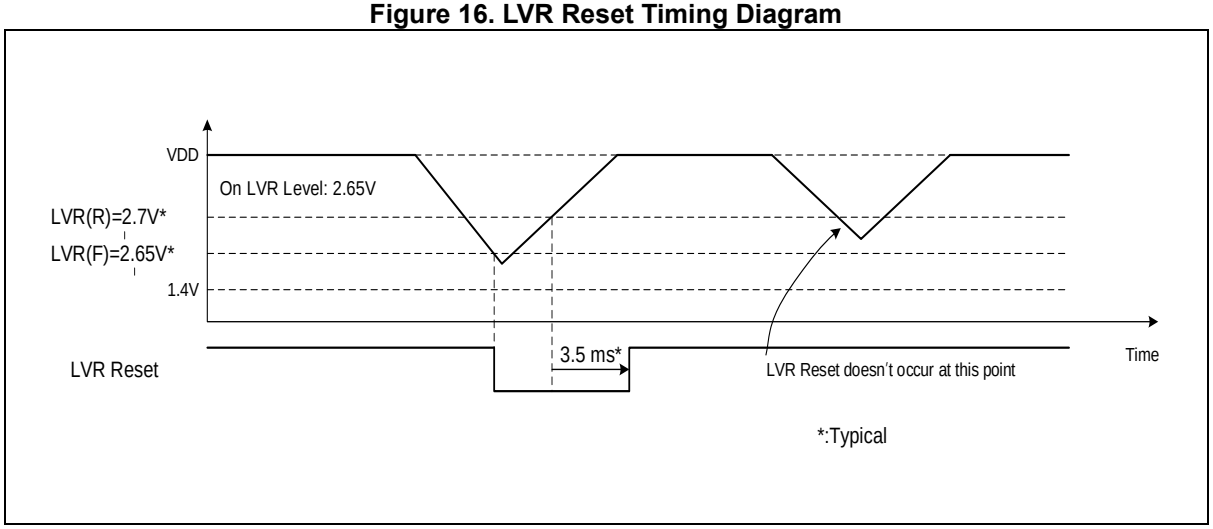
Figure 15. Warm Reset Diagram



4.3.3 LVR reset

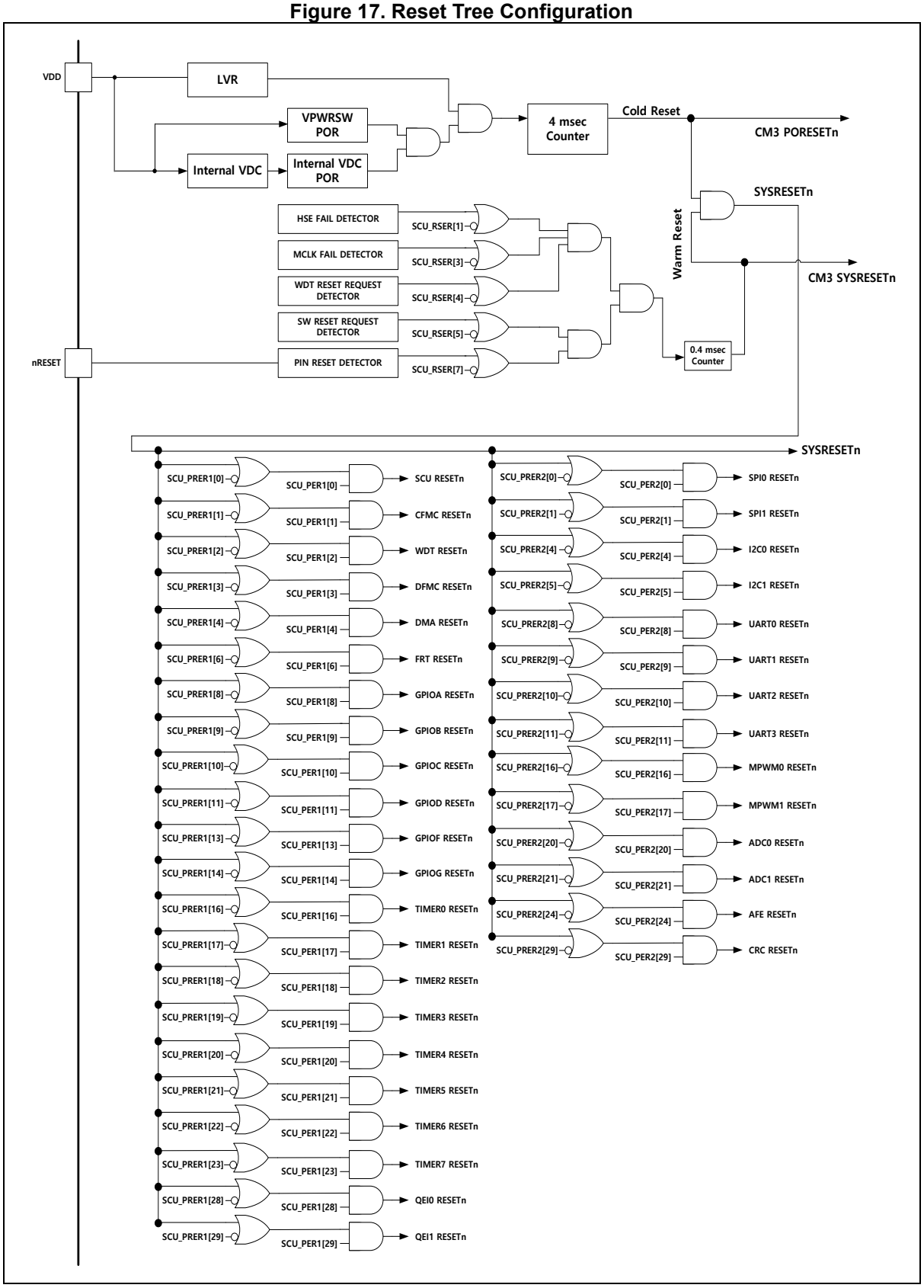
An LVR event is triggered when the operating voltage drops below a certain level during the MCU's operation. A user can choose to set the MCU to perform a reset or an interrupt when an LVR event is triggered. This low voltage reset is a warm reset. See the description on warm resetting for details.

Figure 16. LVR Reset Timing Diagram



4.3.4 Reset tree

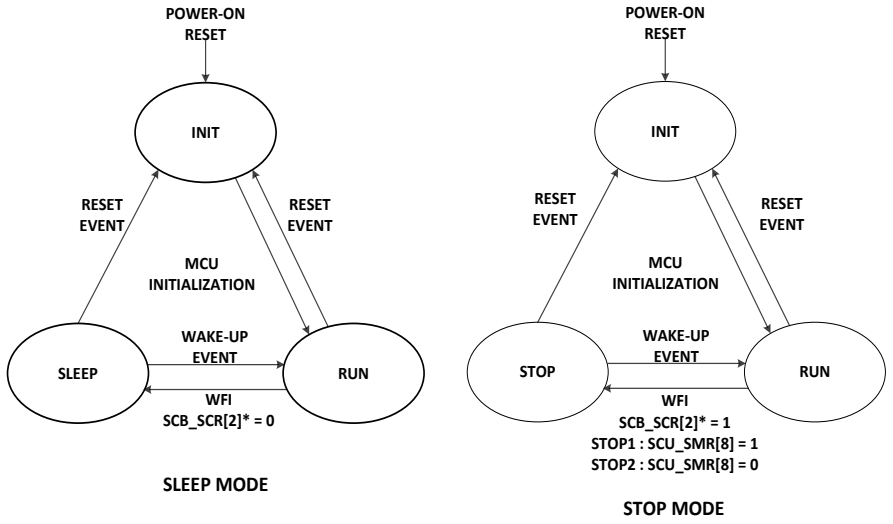
Figure 17. Reset Tree Configuration



4.4 Operation mode

INIT mode is an initial state of the chip when a reset is asserted. In RUN mode, CPU shows the maximum performance with high-speed clock system. SLEEP mode and two power down modes (STOP1, STOP2) can be used as a low power consumption mode. In the low power consumption mode, power is effectively managed to reduce power consumption by halting processor core and unused peripherals. Figure 18 describes transition between the operation modes.

Figure 18. Transition between Operation Modes



NOTE: * means that SCB_SCR is System Register in System Control Block.

Table 12. Operation Mode

MODE	Condition	After wake-up event	After reset event
RUN	POWER ON	N/A	INIT
SLEEP	WFI (Wait for Interrupt): SCB_SCR[2]*=0	RUN	INIT
STOP1	WFI (Wait for Interrupt): SCB_SCR[2]*=1, SCU_SMR[8] =1	RUN	INIT
STOP2	WFI (Wait for Interrupt): SCB.SCR[2]*=1, SCU_SMR[8] =0	RUN	INIT

NOTE: SCB_SCR is System Control Register in System Control Block

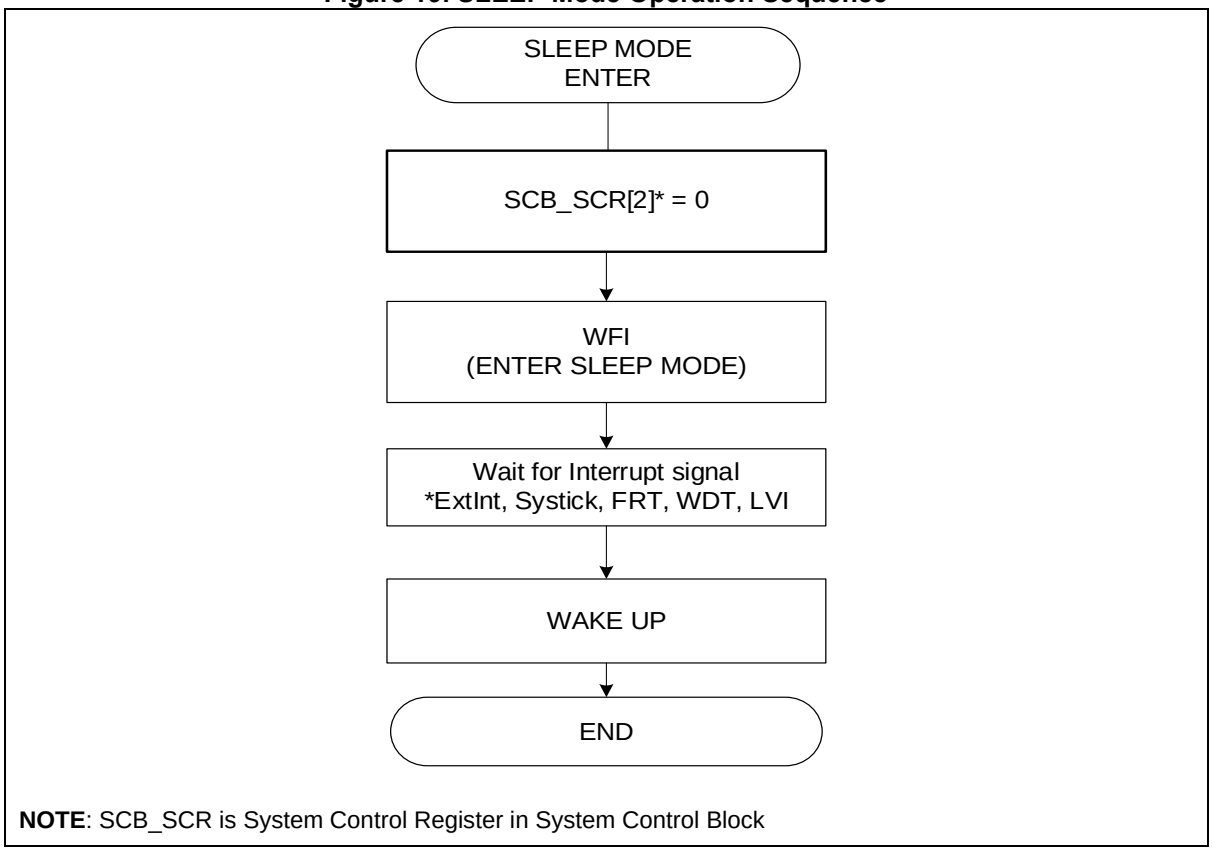
4.4.1 RUN mode

In RUM mode, CPU and the peripheral hardware operate with a high-speed clock. After a reset followed by INIT state, the system enters in RUN mode.

4.4.2 SLEEP mode

Once the MCU enters in SLEEP mode, the CPU becomes inactive. By setting the PER and the PCER registers, a user can determine which peripherals are to be inactive in SLEEP mode.

Figure 19. SLEEP Mode Operation Sequence



NOTE: SCB_SCR is System Control Register in System Control Block

4.4.3 STOP mode

When the core goes under stop state using WFI instruction, the chip enters in STOP mode. STOP mode is divided into STOP1 and STOP2 modes.

To enter STOP1 mode, first set SCU_SMR[8]=1 and use the WFI command. In STOP1 mode, all peripherals except WDT and FRT of internal VDC domain are in power off state. To enter STOP2 mode, first set SCU_SMR[8]=0 and use the WFI command. In STOP2 mode, all peripherals of internal VDC domain are stopped. To wake up in STOP mode, an interrupt request must be generated and can be selected in the SCU_WUER register. Stabilization time is 4ms after wakeup event occurs.

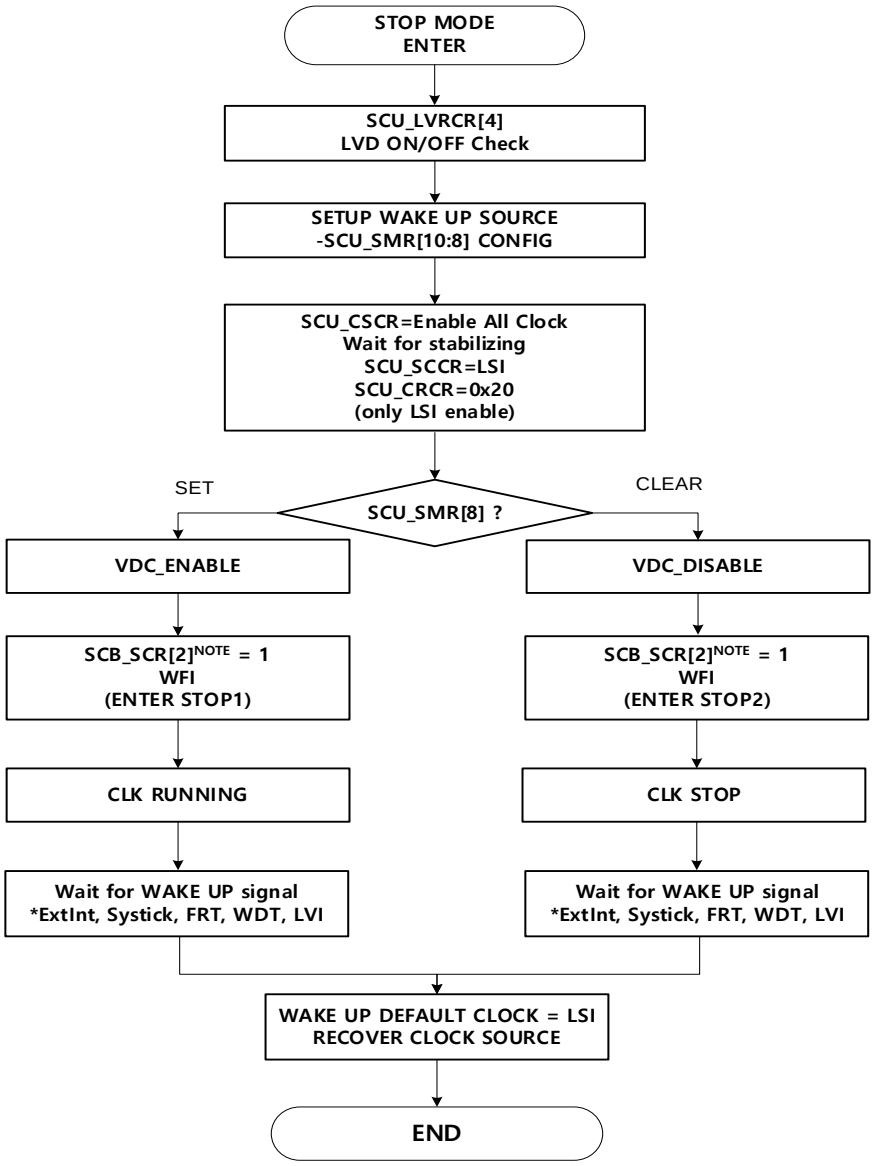
When entering STOP mode, LSI500K is automatically selected as the MCLK, HSE is selected as the PLL input clock, and all clock sources are automatically disabled. These are maintained after wakeup. If the SCU_SMR register is used, a function that automatically disables system clocks such as HSE, PLL, HSI, and LSI may not be used.

Table 13. STOP Mode Configuration

Mode	Condition	Wakeup source
STOP1	WFI SCB_SCR[2]* = 1 SCU_SMR[8] = 1	Source included in WUER
STOP2	WFI SCB_SCR[2]* = 1 SCU_SMR[8] = 0	Source included in WUER

NOTE: SCB_SCR is System Control Register in System Control Block

Figure 20. STOP Mode Operation Sequence



NOTE: SCB_SCR is System Control Register in System Control Block

Table 14 lists configurable clocks in each operating mode.

Table 14. Configurable Clocks in Each Operating Mode

Mode	Core	Peri.	IP				
			VDC	PLL	LSI	HSI	HSE
RUN	ON	User-defined	ON	User-defined	User-defined	User-defined	User-defined
SLEEP	OFF	User-defined	ON	User-defined	User-defined	User-defined	User-defined
STOP1	OFF	Only WDT, FRT on	ON	User-defined	User-defined	User-defined	User-defined
STOP2	OFF	All off	OFF	OFF	User Define	OFF	OFF

5 PCU and GPIO

PCU

The A33M11x MCU's port control unit (PCU) block controls the external input and output (I/O) ports. By setting the PCU block registers, you can configure the pins uses, input/output, pull-up/pull-down, and debouncing, as needed for your application.

Port Control Unit (PCU) configures and controls external I/Os as listed in the followings:

- The MUX registers define the use of each pin.
  - Input/output
  - Push-pull output
  - Open-drain output
  - Logic input
  - Analog input
- The internal pull-up resistor and open-drain mode are configurable for each pin.
- The following interrupts can be set for each pin:
  - Input level interrupt
  - Input rising-edge interrupt
  - Input falling-edge interrupt
- Up to six GPIO interrupts are supported (GPIOA through GPIOG).
- Each pin can be set for debouncing.

GPIO

Pins other than the VDD, GND, and certain specific-purpose pins can be used as general-purpose input/output (GPIO) pins. The GPIO block controls the general I/O ports. Output pins can be configured by setting their bits to generate an "H" or "L" level signal, and logic input pins can be checked for their input state.

GPIO ports are controlled by GPIO block as listed in the followings:

- Output signal level (H/L) selection
- External interrupt interface
- Enables or disables pull-up/pull-down for pins

Six pins in Table 15 are assigned for PCU and GPIO blocks.

Table 15. PCU and GPIO Pins

Pin name	Type	Description
PA	IO	PA0 – PA15
PB	IO	PB0 – PB15
PC	IO	PC0 – PC15
PD	IO	PD0 – PD3
PF	IO	PF0 – PF4, PF6 – PF7
PG	IO	PG10

5.1 PCU and GPIO block diagram

Figure 21 describes PCU in block diagram.

Figure 21. PCU Block Diagram

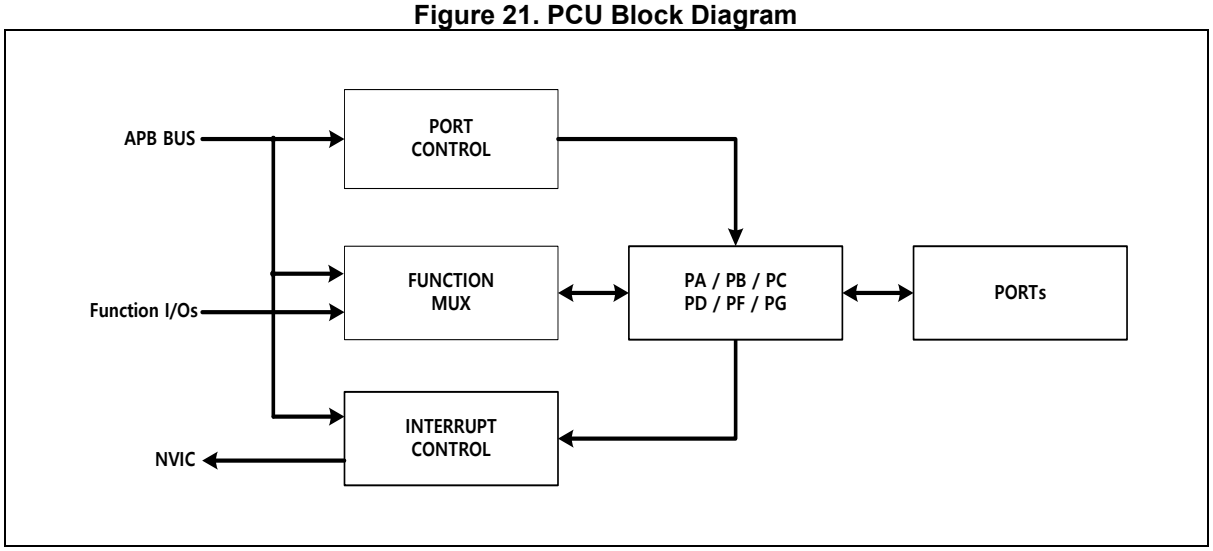


Figure 22 describes GPIO in block diagram, and Figure 23 introduces external interrupt I/O pins.

Figure 22. GPIO Block Diagram

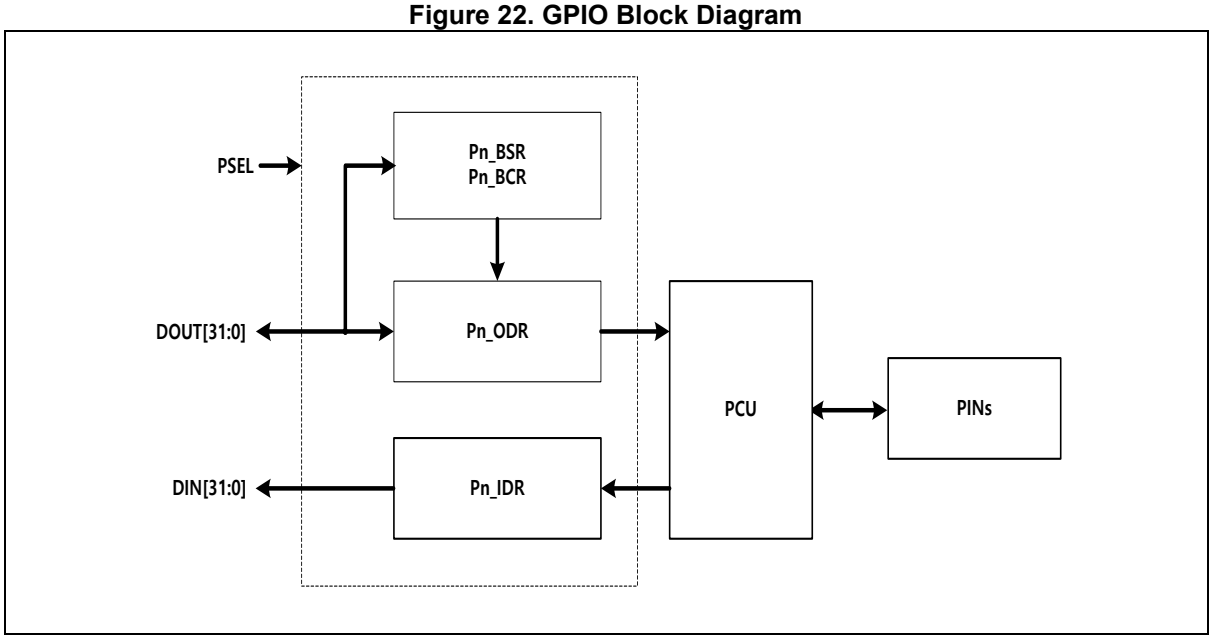


Figure 23. I/O Port Block Diagram (GPIO Pins)

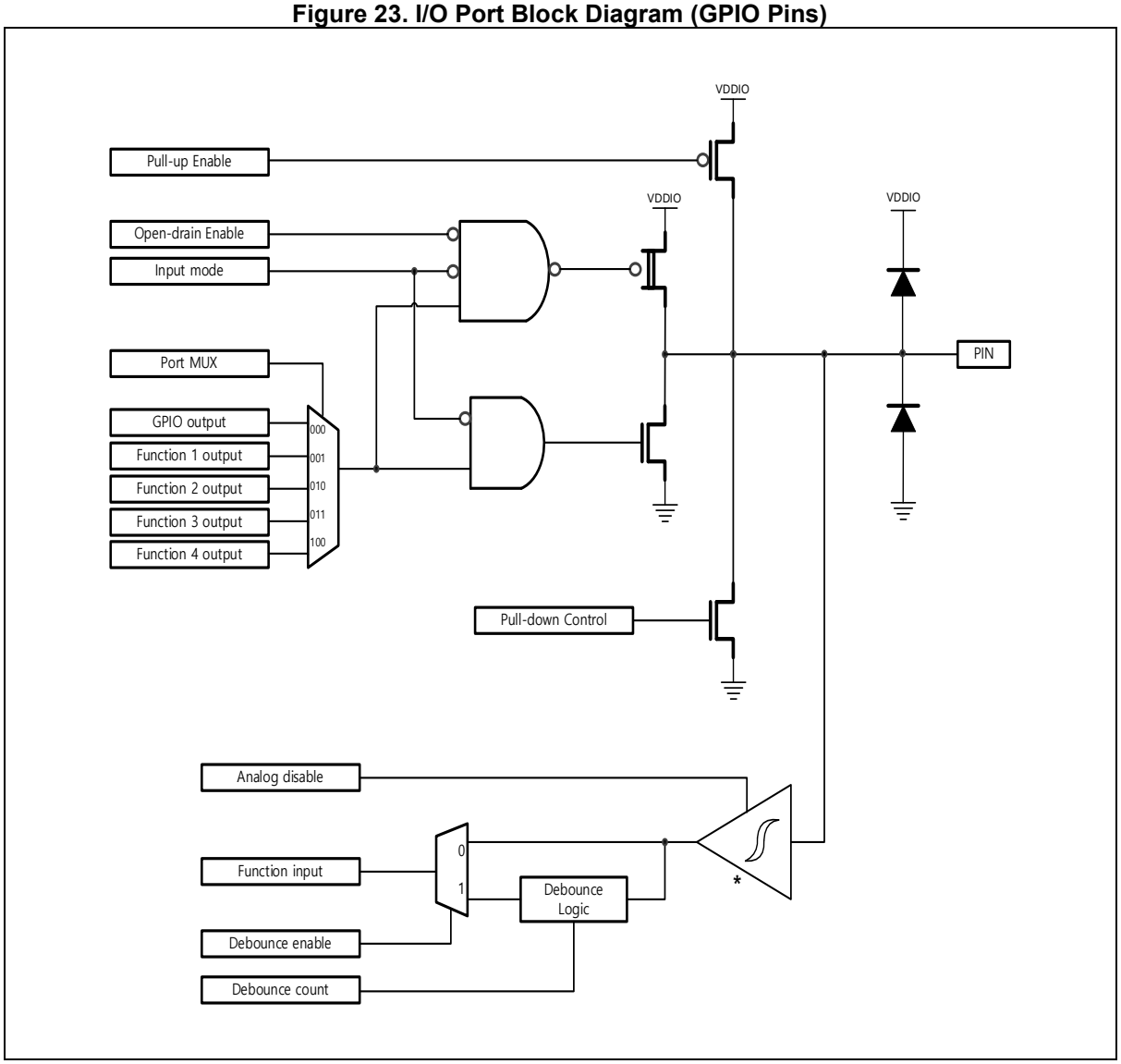
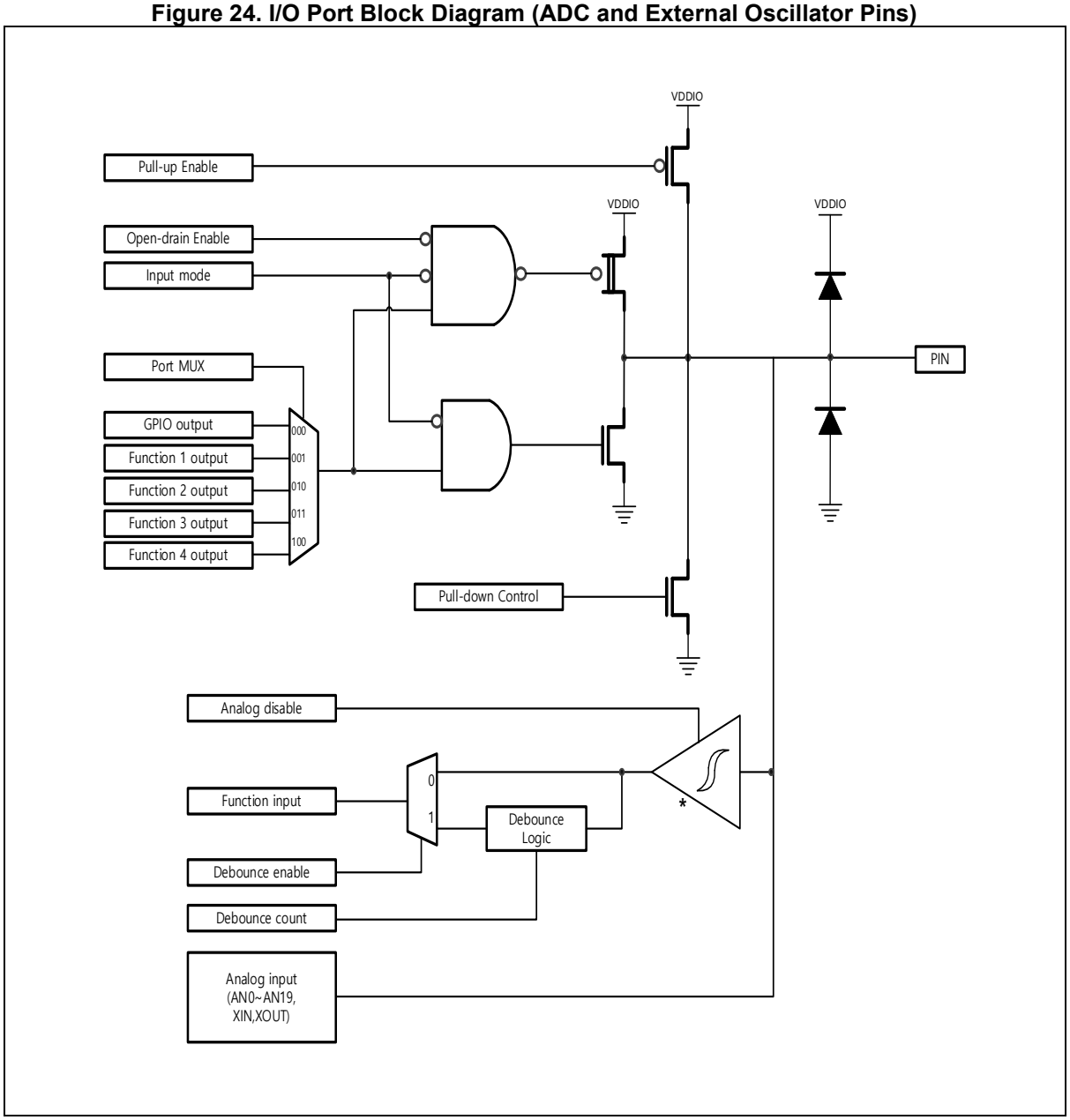


Figure 24. I/O Port Block Diagram (ADC and External Oscillator Pins)



5.2 Pin multiplexing

GPIO pins have alternative function pins. Table 16 shows pin multiplexing information.

Table 16. GPIO Alternative Function

Pin name	Alternative function					
	AF0	AF1	AF2	AF3	AF4	AF7
PA0	PA0*				CO0	AN0/AO0
PA1	PA1*					AN1/AIN0
PA2	PA2*					AN2/AIP0
PA3	PA3*			CAPEU		AN3/AIP1
PA4	PA4*		T0IO			AN4
PA5	PA5*		T1IO			AN5
PA6	PA6*		T2IO	CAPEV		AN6/AIN1
PA7	PA7*		T3IO	CAPEW	CO1	AN7/AO1
PA8	PA8*			SCAPEU	CO2	AN8/AO2
PA9	PA9*			SCAPEV		AN9/AIN2
PA10	PA10*		QEI0_UPDN	SCAPEW		AN10/AIP2
PA11	PA11					AN11
PA12	PA12	SS0				AN12
PA13	PA13*	SCK0	QEI0_A			AN13/AIP3
PA14	PA14*	MOSI0	QEI0_B	PRTINEV		AN14/AIN3
PA15	PA15*	MISO0	QEI0_IDX	OVINEV	CO3	AN15/AO3
PB0	PB0*			MP0UH		
PB1	PB1*			MP0UL		
PB2	PB2*			MP0VH		
PB3	PB3*			MP0VL		
PB4	PB4*		T4IO	MP0WH		
PB5	PB5*		T5IO	MP0WL		
PB6	PB6*			PRTIN0U		
PB7	PB7*			OVIN0U	CLKO	
PB8	PB8*	RXD3		PRTIN1U	SWCLK	
PB9	PB9*	TXD3		OVIN1U	SWDIO	
PB10	PB10*		SS1	MP1UH		
PB11	PB11*		SCK1	MP1UL		
PB12	PB12*	TXD2	MOSI1	MP1VH		
PB13	PB13*	RXD2	MISO1	MP1VL		
PB14	PB14*		PRTINEV	MP1WH		
PB15	PB15*		OVINEV	MP1WL		

Table 16. GPIO Alternative Function (continued)

Pin name	Alternative function					
	AF0	AF1	AF2	AF3	AF4	AF7
PC0	PC0	RXD0		SWCLK*	nBOOT	
PC1	PC1	TXD0		SWDIO*		
PC2	PC2*					
PC3	PC3*					
PC4	PC4*		T0IO			
PC5	PC5*	RXD1	T1IO	QEI1_UPDN		
PC6	PC6*	TXD1	T2IO	QEI1_A		
PC7	PC7*	SCL0	T3IO	QEI1_B		
PC8	PC8*	SDA0	T4IO	QEI1_IDX		
PC9	PC9*		T5IO	CLKO		
PC10	PC10			nRESET*		
PC11	PC11		T6IO	nBOOT*		
PC12	PC12*					XIN
PC13	PC13*					XOUT
PC14	PC14*			RXD0		
PC15	PC15*			TXD0		
PD0	PD0*	SS0	T6IO			AN16
PD1	PD1*	SCK0	T7IO			AN17
PD2	PD2*	MOSI0	SCL1			AN18
PD3	PD3*	MISO0	SDA1			AN19
PF0	PF0*	SCL1				
PF1	PF1*	SDA1				
PF2	PF2*					
PF3	PF3*					
PF4	PF4*					
PF5	PF6*			PRTINEW		
PF6	PF7*			OVINEW		
PG10	PG10*		T7IO			

NOTES:

1. * means ‘selected pin function after reset condition’, which is a 64-pin standard.(The initial value of the pin is different depending on the package type)
2. Unused pins are set to output from Firmware (low output is recommended).

6 Flash memory controller

The flash memory controller (FMC) is an interface controller of internal flash memories:

- Flash code memory with 128-KB, and 256-KB protection bits
- 512-B, and 2-KB erases
- 128-KB, and 256-KB bulk erases
- Max available clock frequency : 28MHz
- Zero wait (less than 28MHz), 1- to 15-wait, and cache (flash acceleration) access

Table 17. Code Flash Memory Controller Features

Item	Description	
Size	128KB	256KB
Start Address	0x0000_0000	0x0000_0000
End Address	0x0002_0000	0x0004_0000
Page Size	512-byte	512-byte
Total Page Count	256 pages	512 pages
PGM Unit	4-byte (1 word)	4-byte (1 word)
Erase Unit	512-byte/ 2KB/ bulk	512-byte/ 2KB/ bulk

Figure 25. Code Flash Memory Map (256 KB Code Flash)

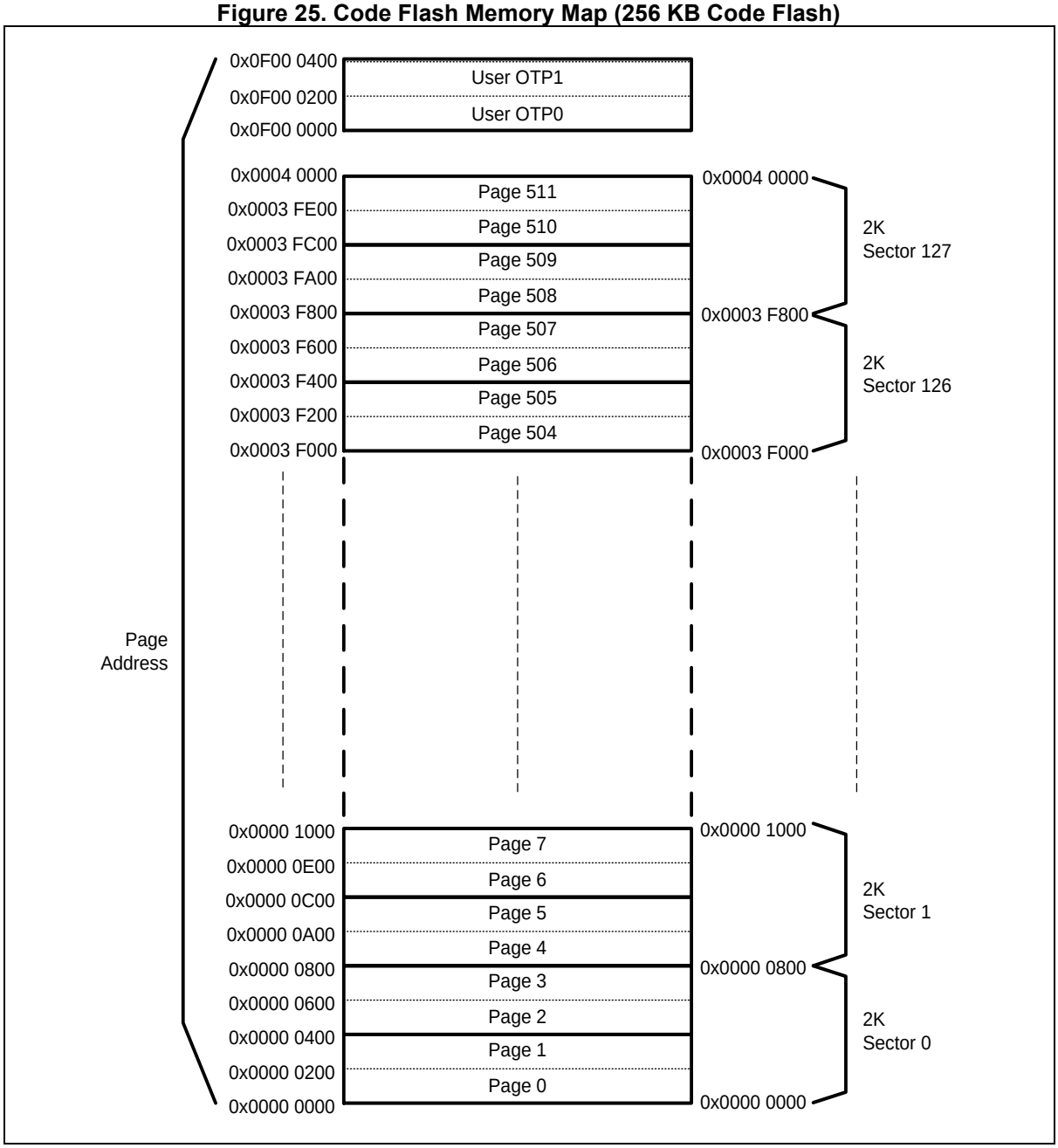
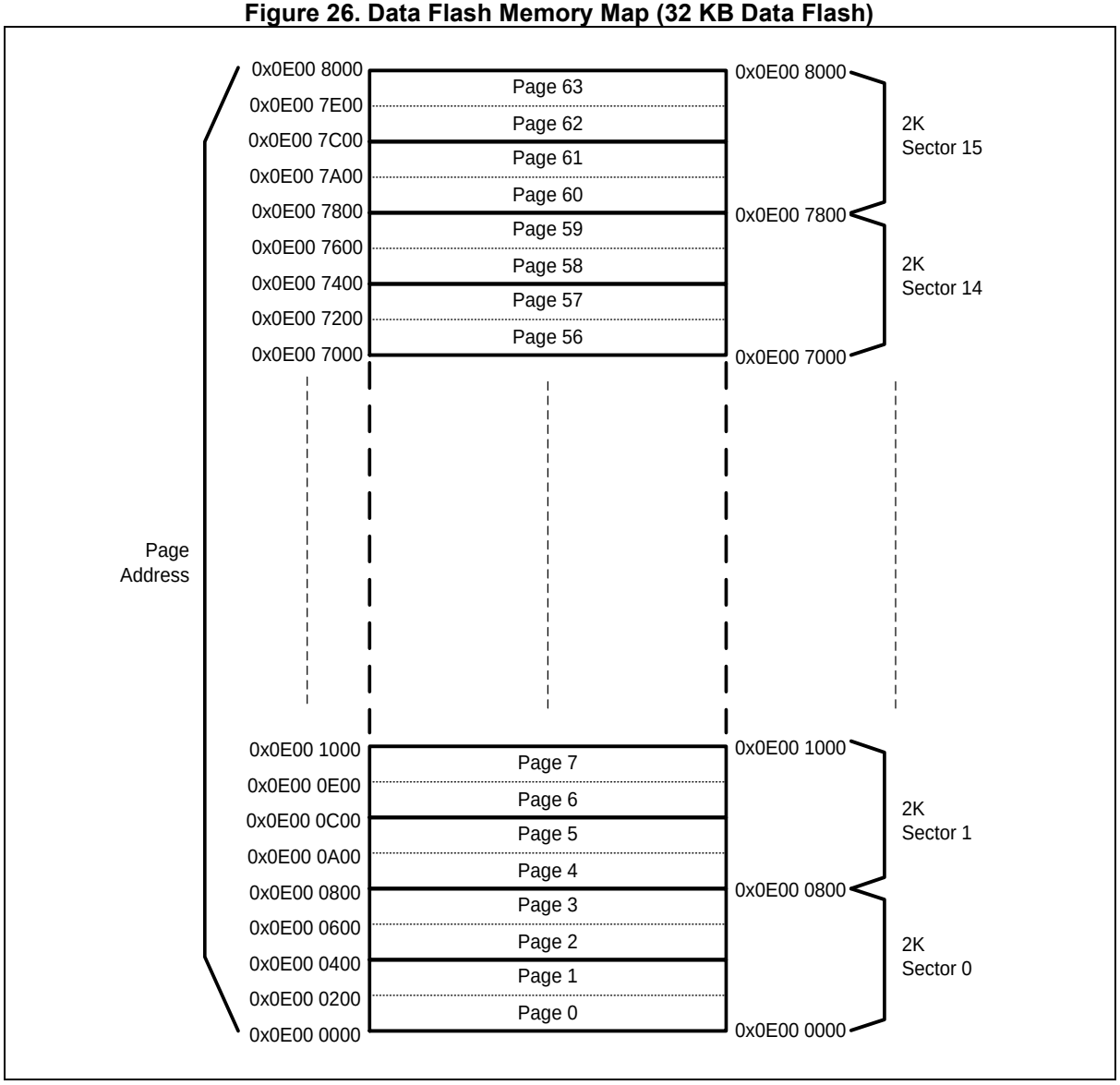


Table 18. Data Flash Memory Controller Features

Item	Description
Size	32KB
Start Address	0x0E00_0000
End Address	0x0E00_8000
Page Size	512-byte
Total Page Count	64 pages
PGM Unit	4-byte (1 word)
Erase Unit	512-byte / 2KB / bulk

Figure 26. Data Flash Memory Map (32 KB Data Flash)



7 Direct Memory Access Controller (DMAC)

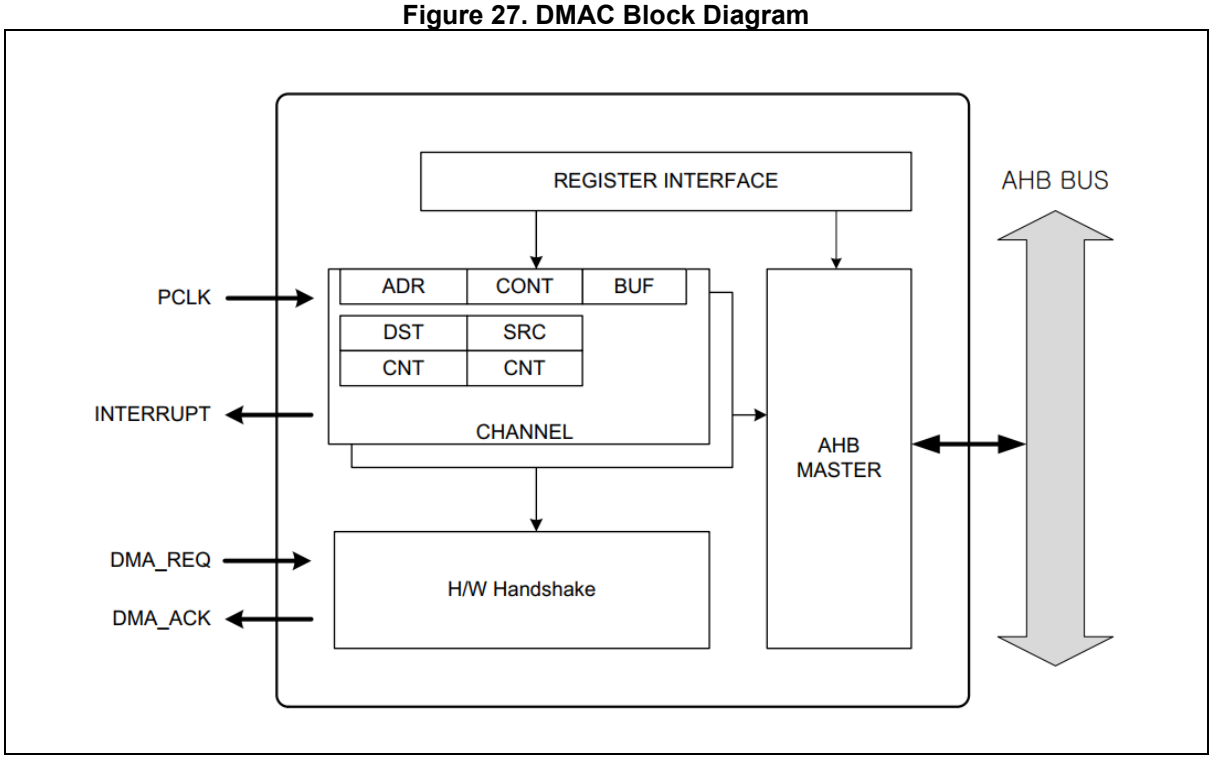
The direct memory access (DMA) controller is used for high-speed data transfers between peripherals and memories. DMA enables quick data transfers having memory to memory copying or moving of data within memory.

- 8 channels
- Only single-ended signaling supported
- 8-/16-/32-bit data transfers supported
- Various buffers with the same size supported
- DMA transfers are triggered through peripheral interrupts

7.1 DMAC block diagram

In this section, DMAC block diagram is introduced in Figure 27.

Figure 27. DMAC Block Diagram



8 Watchdog Timer (WDT)

Watchdog timer (WDT) monitors the operation of the MCU and is typically used to detect software errors. When the MCU becomes uncontrollable due to a malfunction, the WDT resets the MCU to recover it.

The A33M11x series has one WDT module built in, which functions as a 32-bit down-counter. Once the WDT counts down to zero while set as a reset source, the MCU gets reset. When it is not used to monitor the MCU, it can be used as a cycle timer along with an interrupt.

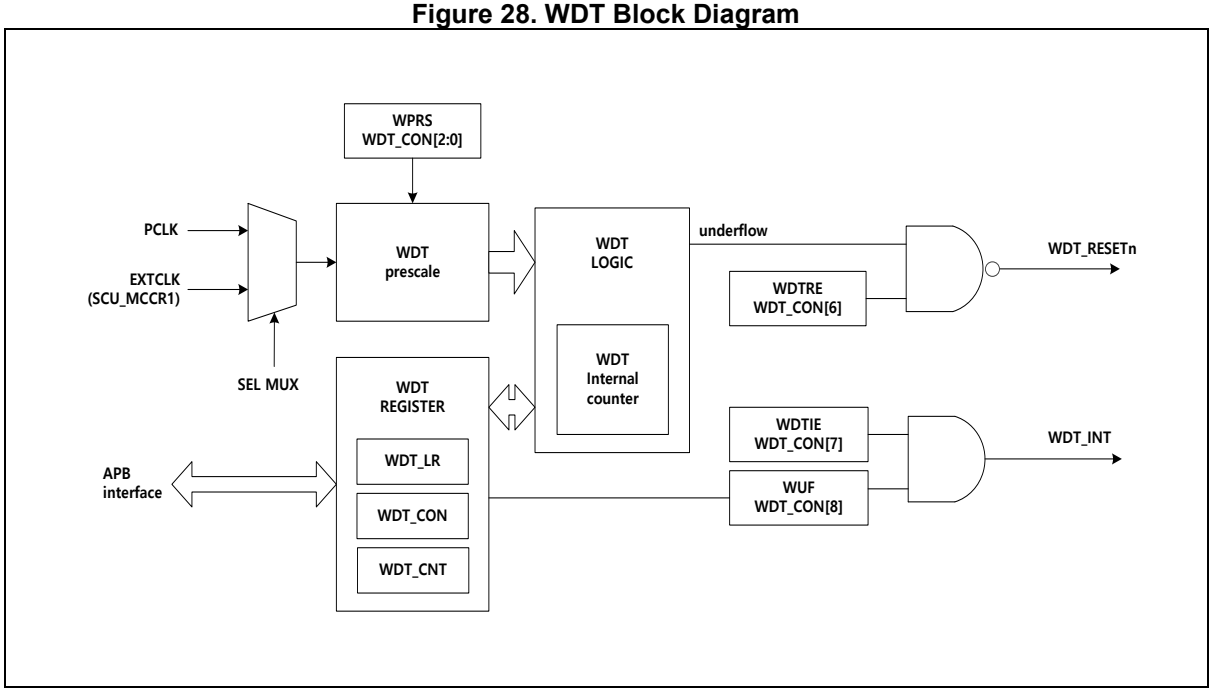
WDT of A33M11x series features followings:

- A 32-bit down-counter
- WDT underflow reset supported
- Cycle timer and underflow interrupt supported
- WDT input clock sources selectable
  - PCLK
  - Clock sources selectable with the setting of SCU_MCCR1[26:24]: LSI, MCLK, HSI, HSE, PLL
- Eight-level prescaler for the WDT clock
- The user can set whether to enable or disable the WDT counter in debug mode

8.1 WDT block diagram

In this section, WDT block diagram is introduced in Figure 28.

Figure 28. WDT Block Diagram



9 16-bit Timer

The A33M11x series has eight channels of 16-bit timers built in. These 16-bit timers support four operating modes: periodic, PWM, one-shot, and capture modes. As the input clock source to the 16-bit timers, either a divided PCLK or an external clock can be used. Additionally, an internal 10-bit prescaler allows the user to generate various timer base clocks.

Interrupts can be triggered at regular intervals when a timer is used in periodic mode. The user can set the period and duty to form a PWM signal to be used in PWM mode. In one-shot and PWM modes, the timer can generate one PWM waveform. In capture mode, the external input signal's pulse intervals can be measured based the preset conditions. Moreover, the timer can export signals to other devices to control them. These timers are primarily used as periodic tick timers or wake-up sources.

16-bit timer of A33M11x series features the followings:

- 16-bit up-counter timers
- Four operating modes:
  - Periodic timer mode
  - One-shot timer mode
  - PWM mode
  - Capture mode
- Various interrupts:
  - Match/overflow interrupts
- Timer input clock sources selectable:
  - Four PCLK prescaler levels (1/2, 1/4, 1/16, 1/64)
  - Clock sources selectable with the setting of SCU_MCCR3: LSI, MCLK, HSI, HSE, and PLL
  - Timer clock source by an input to port TnIO
- 10-bit prescaler built in to support the timer input clock
- PWM synchronization
  - Start delay and clear synchronization

Table 19 introduces pins assigned for 16-bit timer.

Table 19. Pin Assignment of 16-bit Timer: External Pins

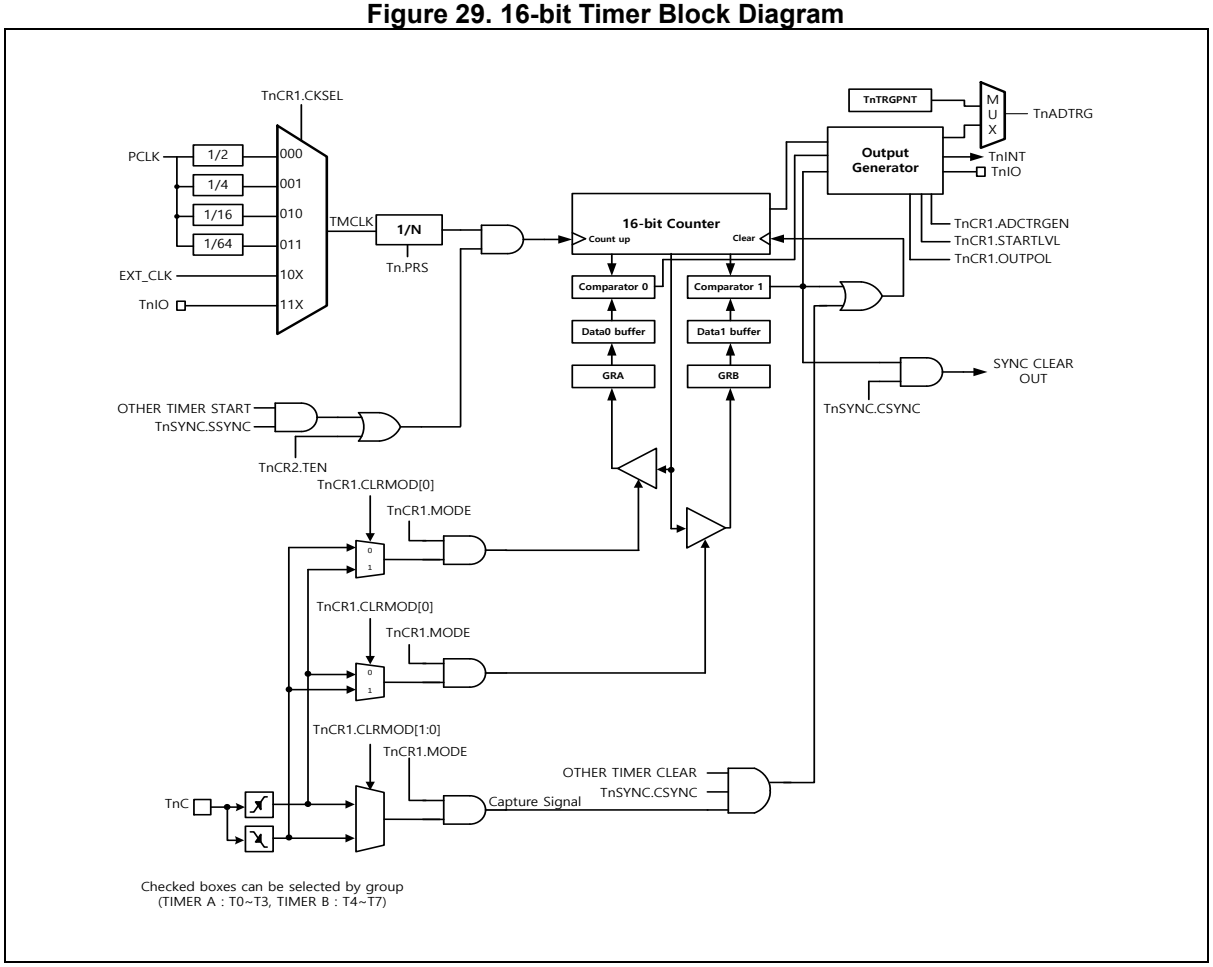
Pin name	Type	Description	Supported Packages	
			A33M116RL A33M116RM A33M114RL (LQFP-64)	**A33M116CL A33M114CL A33M114SN** (LQFP-48, 44)
T0IO	IO	Timer0 capture input signal/external clock input Timer0 timer/PWM/one-shot output	O	O
T1IO	IO	Timer1 capture input signal/external clock input Timer1 timer/PWM/one-shot output	O	O
T2IO	IO	Timer2 capture input signal/external clock input Timer2 timer/PWM/one-shot output	O	O
T3IO	IO	Timer3 capture input signal/external clock input Timer3 timer/PWM/one-shot output	O	O
T4IO	IO	Timer4 capture input signal/external clock input Timer4 timer/PWM/one-shot output	O	O
T5IO	IO	Timer5 capture input signal/external clock input Timer5 timer/PWM/one-shot output	O	O
T6IO	IO	Timer6 capture input signal/external clock input Timer6 timer/PWM/one-shot output	O	O
T7IO	IO	Timer7 capture input signal/external clock input Timer7 timer/PWM/one-shot output	O	O

NOTE: If the package is reduced, the timer function can be used internally, but the external pin cannot be used.

9.1 16-bit timer block diagram

In this section, 16-bit timer is described in a block diagram in Figure 29.

Figure 29. 16-bit Timer Block Diagram



10 Free Run Timer (FRT)

The A33M11x series has one free-run timers (FRTs) built in, which are 32-bit up-count timers. These timers can run with the overflow or match interrupt according to their uses and can remain active in stop mode.

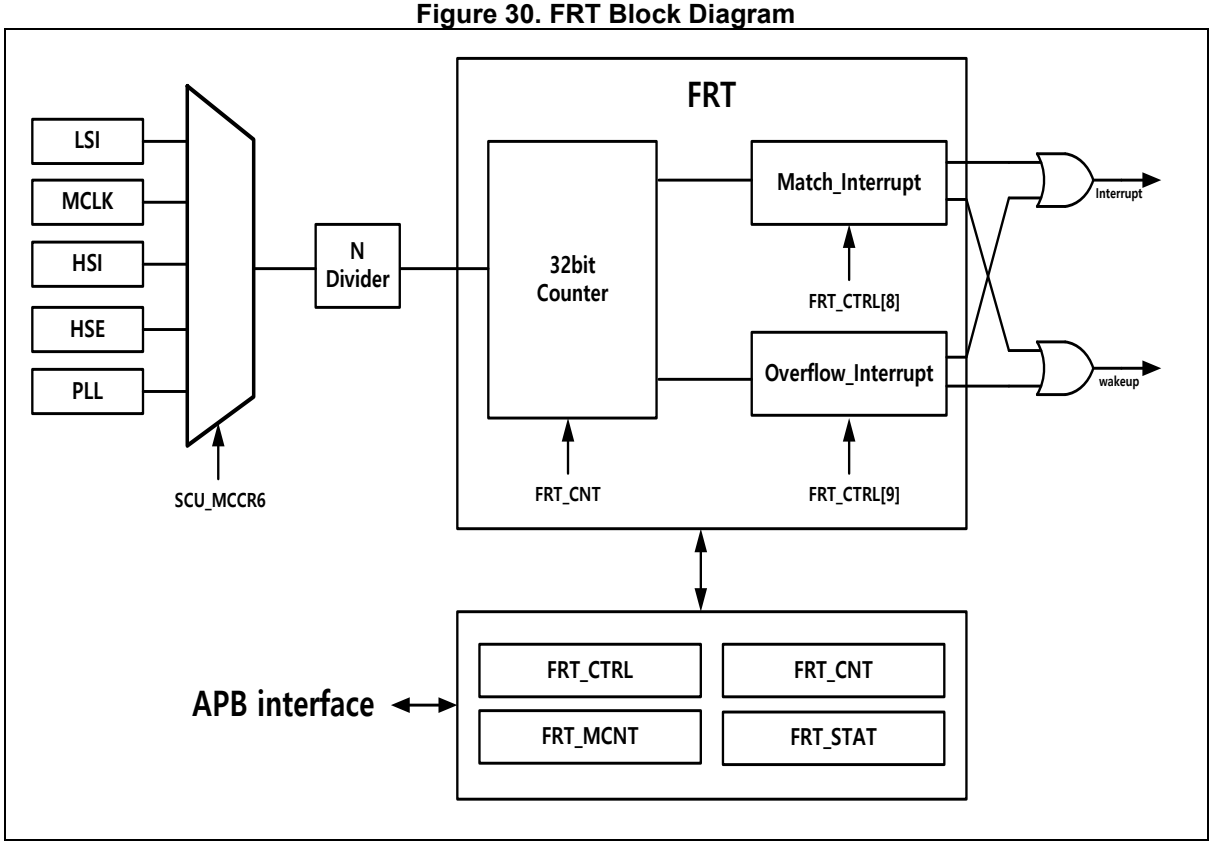
FRT of A33M11x series features the followings:

- 32-bit up-count timers
  - Capable of functioning as periodic timers (Each timer's period is configurable)
  - Free-run timer mode
- FRT overflow and match interrupts supported
- FRT input clock sources selectable
  - Clock sources selectable with the setting of SCU_MCCR6: LSI, MCLK, HSI, HSE, and PLL

10.1 FRT block diagram

In this section, FRT block diagram is introduced in Figure 30.

Figure 30. FRT Block Diagram



11 Universal Asynchronous Receiver/Transmitter (UART)

The A33M11x series is equipped with a four-channel UART module. These built-in UARTs transmit and receive data according to user-specified settings and read the current UART status. UART status information includes the type and conditions of the current UART transmission/reception process and can be used to check for errors (parity, overrun, framing, or break interrupts) that occur during data reception.

Each UART channel has a programmable baud-rate generator, which serves to generate an internal clock for the corresponding UART by dividing the prescaled clock by a baud-rate divisor (ranging from 1 to 65535) and then dividing the result by 16.

Additionally, the user can program interrupts that control UART communication.

UART of A33M11x series features the followings:

- A total of four 16450 asynchronous serial communication ports supported
- Configurable standard asynchronous communication bits (start, stop, and parity)
- User-programmable serial communication
  - 5, 6, 7, or 8 data bits
  - Even, odd, or no parity generation and checking
  - 1-, 1.5-, or 2-stop bit generation and checking
- A 16-bit baud-rate generator and an 8-bit fractional compensator
- Delay between data frames supported
- Transfer status indicated by the interrupt ID and line status registers
  - Stop bit error detection
  - Display of information about the current status
  - Line break generation and checking
  - Receive error diagnosis
- Loop-back control
- A priority-based interrupt system

Table 20 introduces pins assigned for the UART.

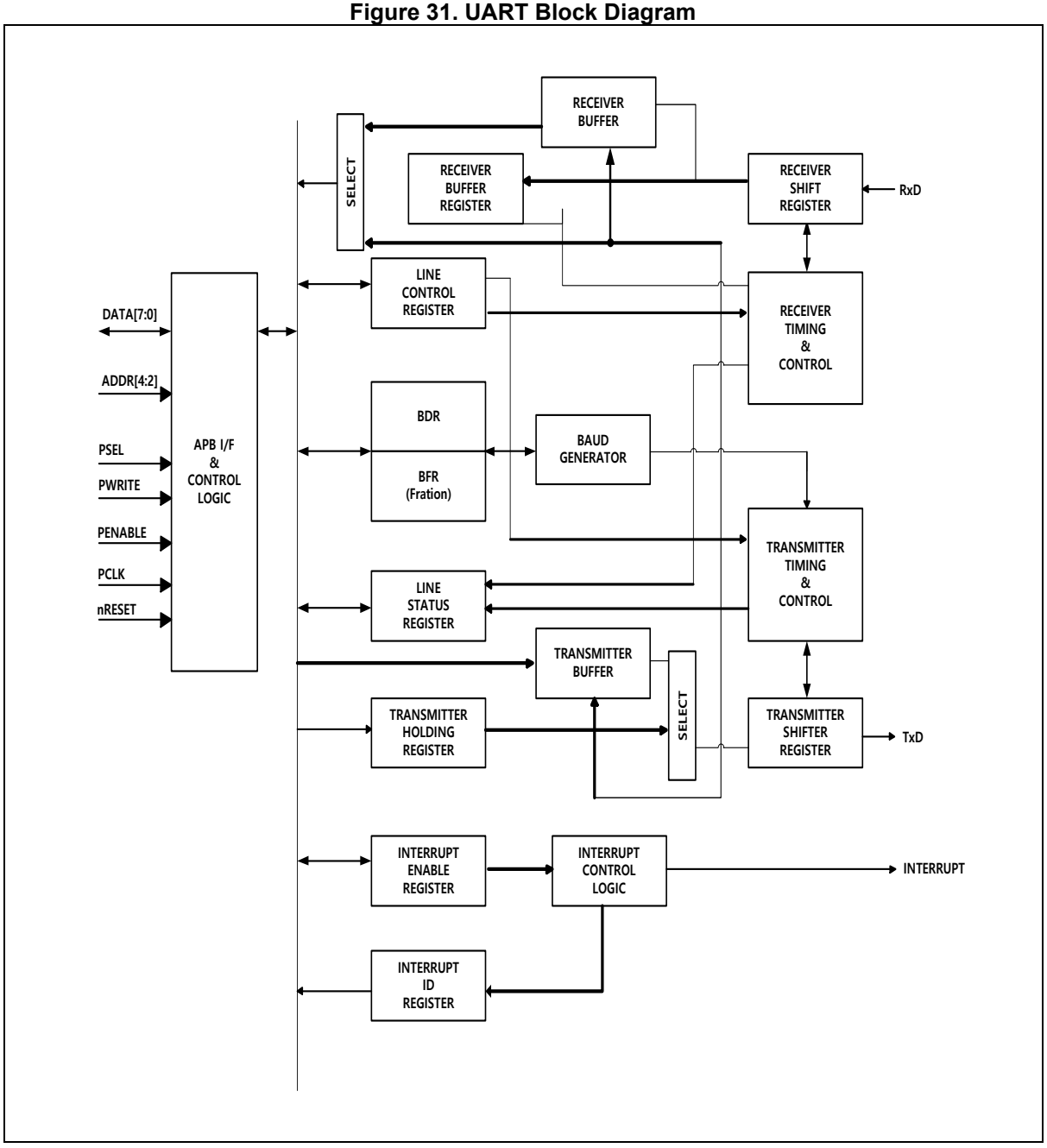
Table 20. Pin Assignment of UART: External Pins

Pin name	Type	Description	Supported Packages	
			A33M116RL **A33M116RM** **A33M114RL** (LQFP-64)	**A33M116CL** **A33M114CL** **A33M114SN** (LQFP-48, 44)
TXD0	O	UART channel 0 transmit output	O	O
RXD0	I	UART channel 0 receive input	O	O
TXD1	O	UART channel 1 transmit output	O	X
RXD1	I	UART channel 1 receive input	O	X
TXD2	O	UART channel 2 transmit output	O	O
RXD2	I	UART channel 2 receive input	O	O
TXD3	O	UART channel 3 transmit output	O	O
RXD3	I	UART channel 3 receive input	O	O

11.1 UART block diagram

In this section, UART is introduced in block diagrams.

Figure 31. UART Block Diagram



12 Serial Peripheral Interface (SPI)

The A33M11x series has two serial peripheral interface (SPI) modules built in. The SPI modules are synchronized by clocks. The specifications of the transmit and receive clocks are adjustable. The SPI supports communications between one master and multiple slaves. Slaves can be selected using slave select (SS).

The SPI performs four-wire synchronous transfers via four signal terminals (SS, SCK, MOSI, and MISO). Its separate transmit and receive buffers enables full-duplex communication, which is capable of reading and writing data simultaneously.

SPI of A33M11x series features the followings:

- Selectable between the master and slave operations
- Full-duplex and four-wire synchronous transfers supported
  - SS: Slave Select
  - SCLK: Serial Clock
  - MOSI: Master Output Slave Input
  - MISO: Master Input Slave Output
- SPI clock speed and polarity adjustable
- Separate transmit and receive data registers with different data transfer sizes
  - Available transmit/receive data sizes: 8, 9, 16, and 17 bits
- Configurable interrupts triggered by the transmit status and SS signal
- Loop-back mode for internal checkups
- User-programmable start, burst, and stop delay times
- DMA transfers

Table 21 introduces pins assigned for SPI.

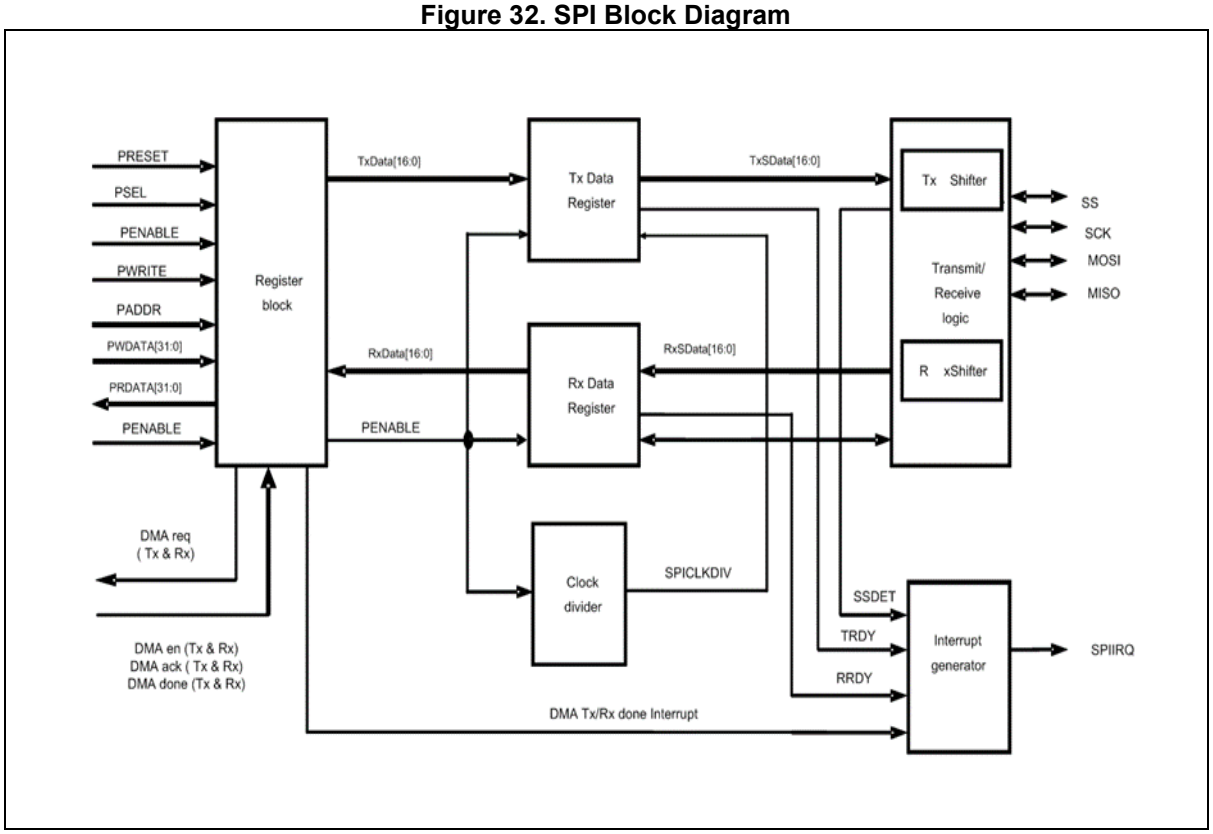
Table 21. Pin Assignment of SPI: External Pins

Pin name	Type	Description	Supported Packages	
			A33M116RL **A33M116RM** **A33M114RL** (LQFP-64)	**A33M116CL** **A33M114CL** **A33M114SN** (LQFP-48, 44)
SS0	I/O	SPI0 serial port I/O signal for slave selection	O	O
SCK0	I/O	SPI0 clock I/O (master: output / slave: input)	O	O
MOSI0	I/O	SPI0 transmit and receive data (master: output / slave: input)	O	O
MISO0	I/O	SPI0 transmit and receive data (master: input / slave: output)	O	O
SS1	I/O	SPI1 serial port I/O signal for slave selection	O	O
SCK1	I/O	SPI1 clock I/O (master: output / slave: input)	O	O
MOSI1	I/O	SPI1 transmit and receive data (master: output / slave: input)	O	O
MISO1	I/O	SPI1 transmit and receive data (master: input / slave: output)	O	O

12.1 SPI block diagram

In this section, SPI is described in a block diagram in Figure 32.

Figure 32. SPI Block Diagram



13 Inter Integrated Circuit (I2C) interface

The I2C (inter-integrated circuit) interface built in the A33M11x series provides serial communications with internal and external devices via the I2C protocol. Equipped with two channels, it supports both master and slave modes and capable of transmitting and receiving data in bytes through interrupts or polling.

The I2C block is used to communicate with various peripherals that have the same bus type. When using the I2C capabilities of the A33M11x series, it is recommended to configure pins SCL and SDA as open-drain and then connect an external pull-up resistor to each of them to render their output signals “high.”

I2C features the followings:

- Compliant with I2C protocol
  - Supports two channels
- Master and slave modes
- Multi-slave mode
  - 1:1 and N:N (up to 1008) slave devices
- Transfer rates configurable
  - Maximum transfer rate: 400KHz
- I2C interrupts
- 7-bit addressing
- Delay time can be set for pin SCL’s high or low waveform
- Hold time can be set for previous data
- Generates and detects STOP, START, and ACK signals

Table 22 introduces pins assigned for I2C interface.

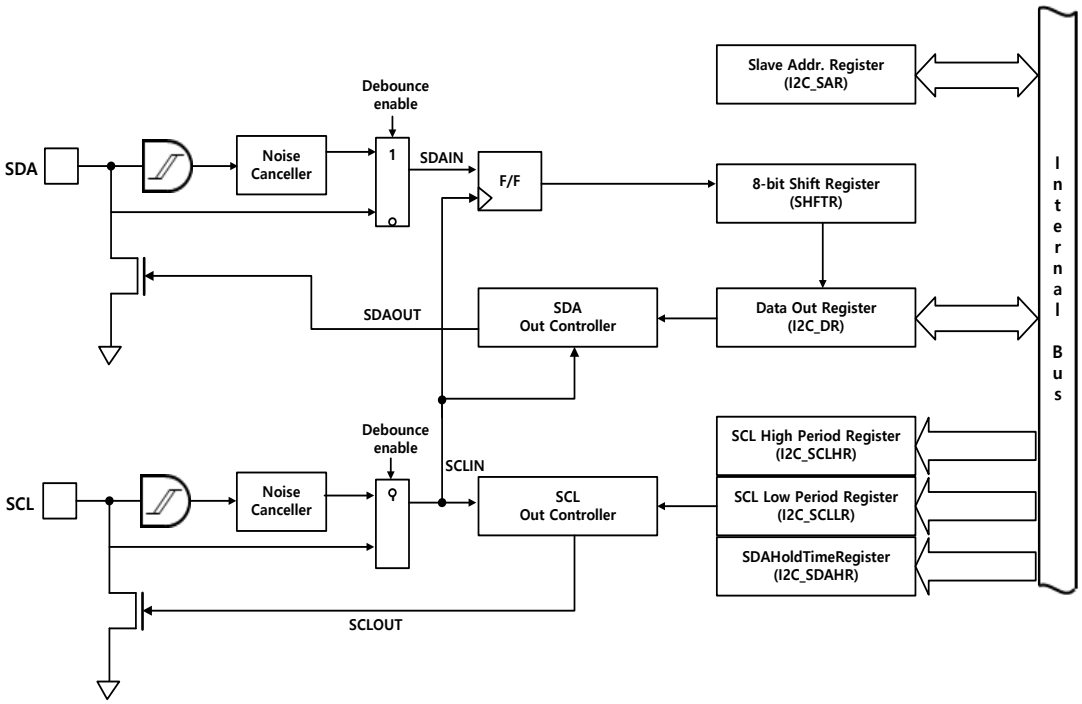
Table 22. Pin Assignment of I2C: External Pins

Pin name	Type	Description	Supported Packages	
			A33M116RL **A33M116RM** **A33M114RL** (LQFP-64)	**A33M116CL** **A33M114CL** **A33M114SN** (LQFP-48, 44)
SCL0	I/O	I2C channel 0 serial clock bus line (open-drain)	O	O
SDA0	I/O	I2C channel 0 serial data bus line (open-drain)	O	O
SCL1	I/O	I2C channel 1 serial clock bus line (open-drain)	O	O
SDA1	I/O	I2C channel 1 serial data bus line (open-drain)	O	O

13.1 I2C block diagram

In this section, I2C interface block is described in a block diagram.

Figure 33. I2C Block Diagram



NOTE: When the corresponding port of I2C is a sub-function for SCL/SDA pin, the SCL/SDA pins are automatically set to the N-channel open-drain outputs and the input latch is read in the case of reading the pins. The corresponding pull-up resistor is determined by the control register.

14 Motor Pulse Width Modulation (MPWM)

The Motor PWM (MPWM) modules are programmable motor controllers optimized for three-phase AC and DC motor control applications. Each MPWM module is equipped with three channels that can generate their respective pairs of outputs. The MPWM counter is clocked from the SCU block. As the clock determines MPWM resolution and period, you must select an appropriate MPWM clock before enabling the MPWM module.

MPWM Normal Mode of A33M11x series features the followings:

- 16-bit counter
- Six output channels for motor control
- Dead-time rising or falling area
- Handling of protection and overvoltage events
- Six ADC trigger sources
- Interval interrupt mode (Only a period interrupt is used)
- Up-count and down-count modes

MPWM Individual Mode of A33M11x series features the followings:

The MPWM module supports an Individual mode to enable various applications, such as IH cookers.

- 16-bit counter
- Different periods and dead times (rising/falling) configurable for phases U, V, and W
- Handling of different protection and overvoltage events for phases U, V, and W
- Different interrupts for phases U, V, and W (except for the protection and overvoltage interrupts)
- Different protection and overvoltage events for phases U, V, and W (e.g., if protection occurs for phase V, only the phase V output becomes inactive while phases U and W remain operational).
- Capture functionality

Table 23 introduces pins assigned for MPWM.

Table 23. Pin Assignment of MPWM: External Pins

Pin name	Type	Description	Supported Packages	
			A33M116RL **A33M116RM** **A33M114RL** (LQFP-64)	**A33M116CL** **A33M114CL** **A33M114SN** (LQFP-48, 44)
MP0UH/L MP0VH/L MP0WH/L	O	MPWM0 H/L side output ports of phases U, V, and W	O	O
MP1UH/L MP1VH/L MP1WH/L	O	MPWM1 H/L side output ports of phases U, V, and W	O	O
PRTIN0U OVIN0U	I	MPWM0 protection and overvoltage input pins dedicated to MPWM0 phase U in Individual mode	O	O
PRTIN1U OVIN1U	I	MPWM1 protection and overvoltage input pins dedicated to MPWM1 phase U in Individual mode	O	O
PRTINEV OVINEV	I	Protection and overvoltage input pins dedicated to MPWM0/1 phase V in Individual mode	O	O
PRTINEW OVINEW	I	Protection and overvoltage input pins dedicated to MPWM0/1 phase W in Individual mode	O	X
CAPEU CAPEV CAPEW	I	Input pins in MPWM0/1 dedicated to capturing in Individual mode	O	O
SCAPEU SCAPEV SCAPEW	I	Input pins in MPWM0/1 dedicated to sub-capturing in Individual mode	O	O
Normal mode	MPWM0 Protection		MPWM1 Protection	
	PRTIN0U, OVIN0U		PRTIN1U, OVIN1U	
Individual mode	U	PRTIN0U, OVIN0U	PRTIN1U, OVIN1U	
	V	PRTINEV	OVINEV	
	W	PRTINEW	OVINEW	

NOTE: In Individual PWM mode, V and W of PRTINE / OVINE operate simultaneously with MPWM0 and MPWM1.

14.1 MPWM block diagram

Figure 34 describes normal mode of MPWM in block diagram.

Figure 34. MPWM Block Diagram (Normal Mode)

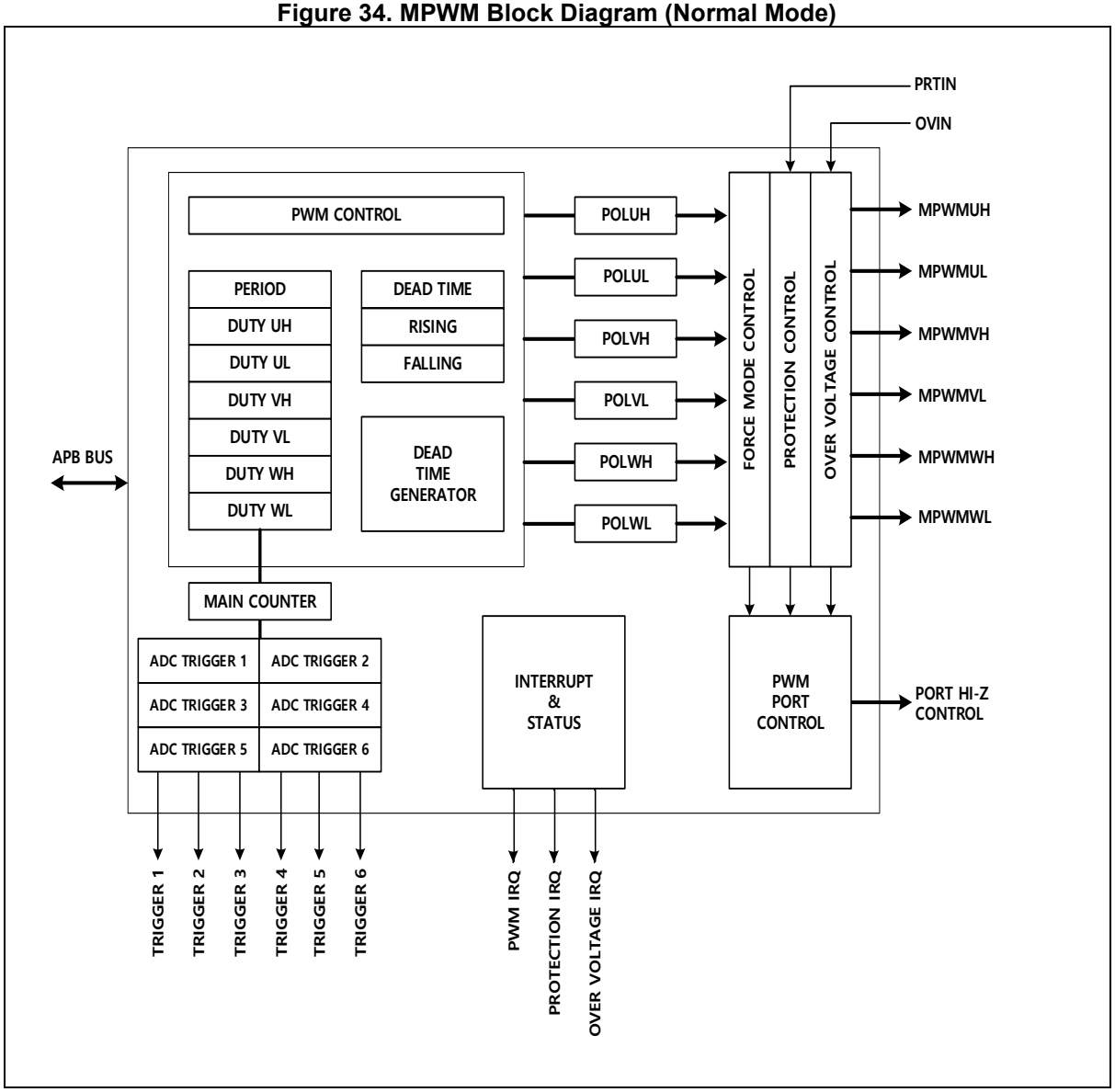


Figure 35 describes individual mode of MPWM in block diagram.

Figure 35. MPWM Block Diagram (Individual Mode)

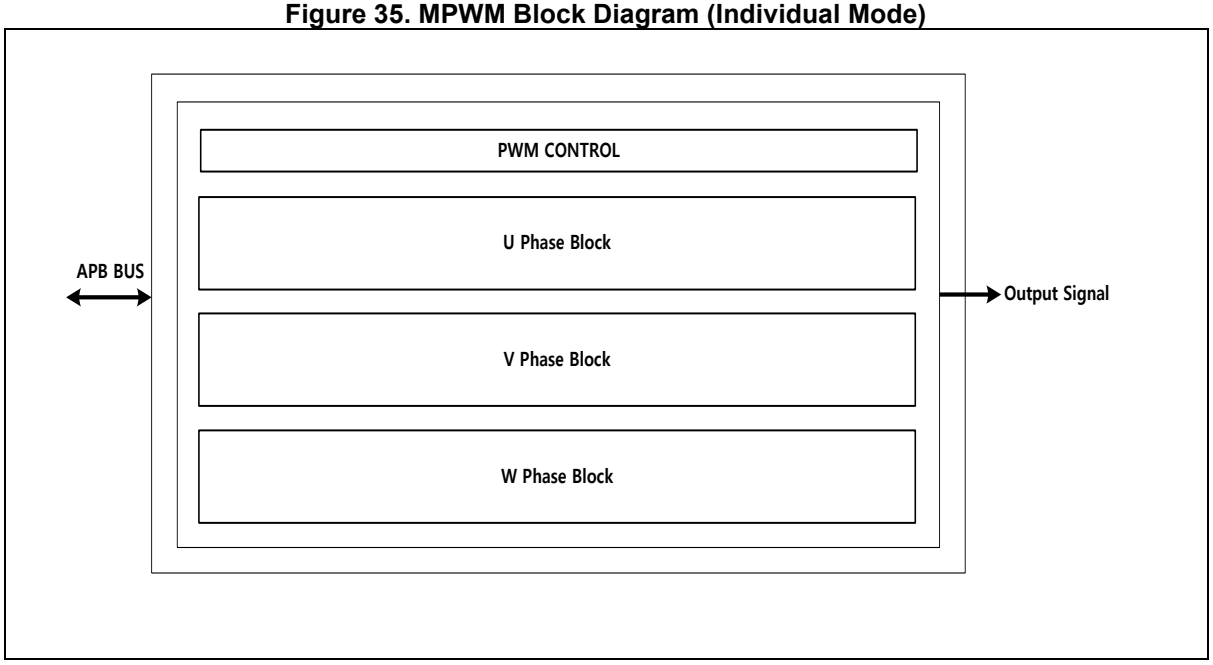
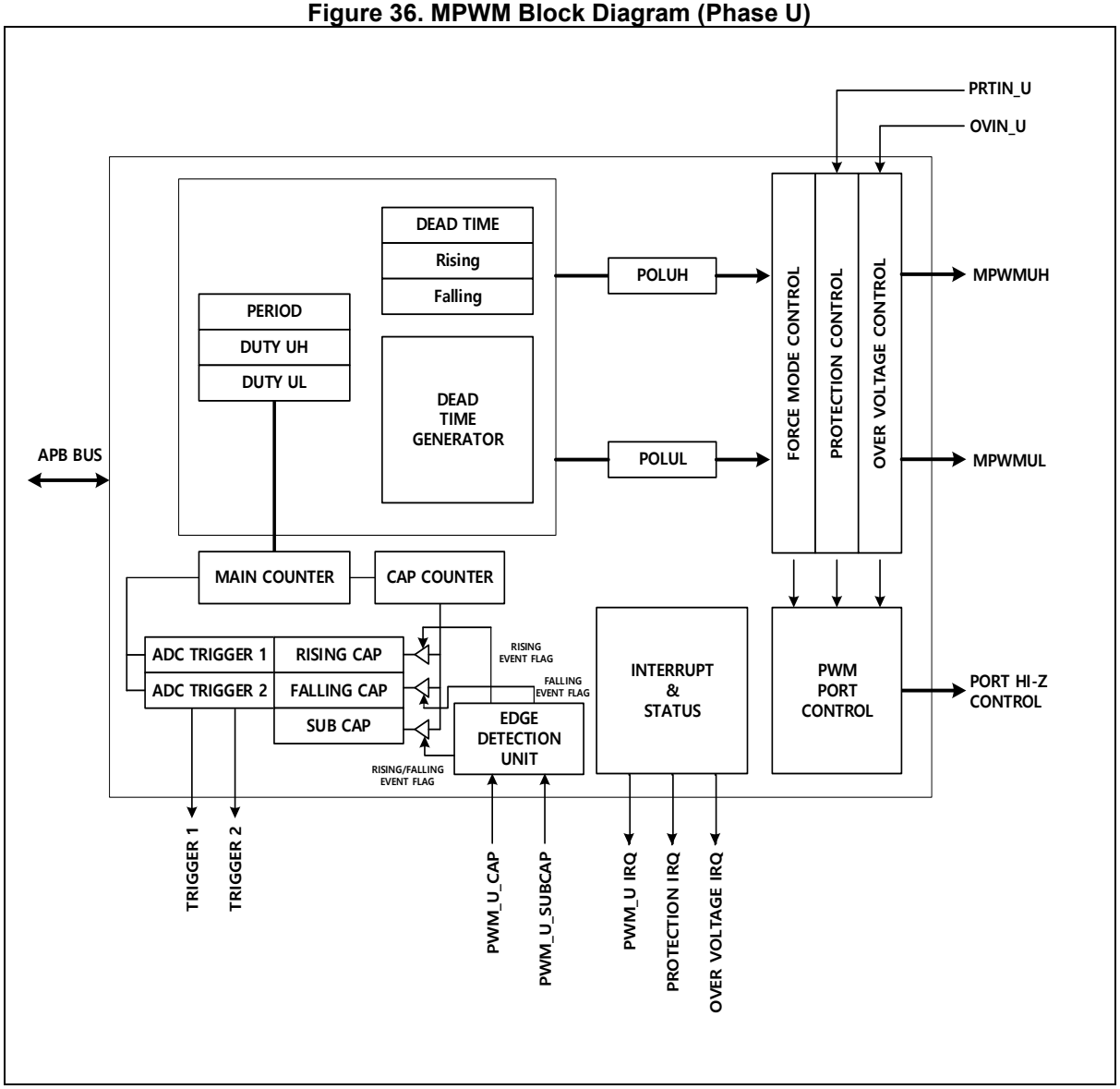


Figure 36 describes MPWM in block diagram (detailed).

Figure 36. MPWM Block Diagram (Phase U)



NOTE: The figure above represents the phase U block only. The phase V and W blocks are identical to the phase U block. Each phase block is independently configurable; however, the protection and overvoltage interrupts are used in common.

15 Quadrature Encoder Interface (QEI)

The two-channel quadrature encoder interface (QEI) uses two pulse signals outputted from an encoder. By counting the number of relative phase pulses between these two signals, the encoder's rotational position, direction, and velocity are tracked. Additionally, an index signal is used to reset the position counter.

Each QEI module consists of a decoder logic interpreting the Ph-A and Ph-B signals and up- and down-counters.

QEI of A33M11x series features the followings:

- Three input pins for two phase signals and index pulse
  - Phases A/B: Input of QEI phases A and B
  - INDEX: Input of QEI index
  - UPDN: Output of phase direction
- 32-bit up-/down-counter counting the number of rotations in each direction
- x2 and x4 count resolution for capture mode
- Position compare register and interrupt
- Index compare register and interrupt
- Velocity capture by a velocity timer
- Signals are selectable
  - Quadrature signals (Ph-A and Ph-B)
  - Clock and direction signals (Clock: Ph-A, direction: Ph-B)

Table 24 introduces pins assigned for QEI interface.

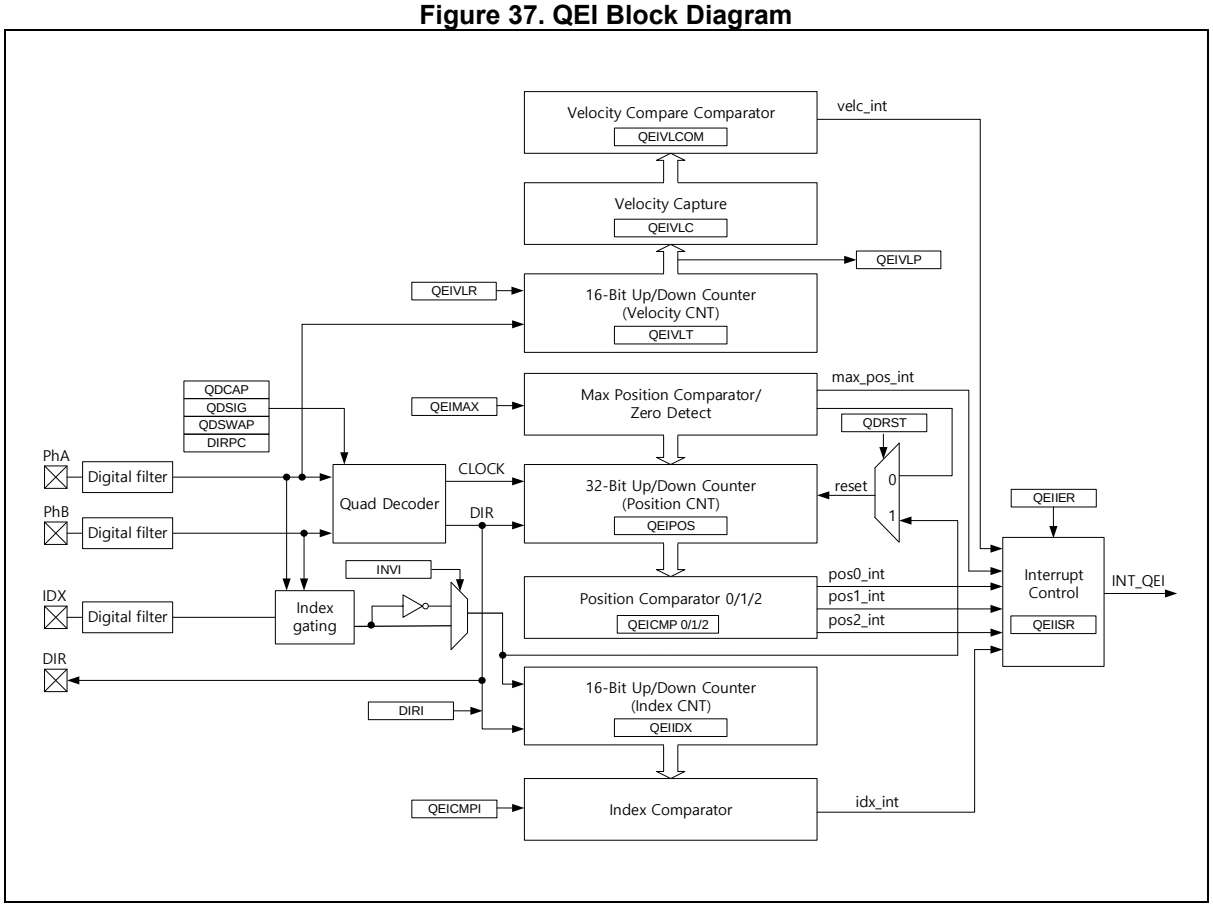
Table 24. Pin Assignment of QEI: External Pins

Pin name	Type	Description	Supported packages	
			A33M116RL **A33M116RM** **A33M114RL** (LQFP-64)	**A33M116CL** **A33M114CL** **A33M114SN** (LQFP-48, 44)
QEI0_UPDN	O	QEI0 phase direction output port	O	O
QEI0_A QEI0_B QEI0_IDX	I	QEI0 phase-A, phase-B, and index input ports	O	O
QEI1_UPDN	O	QEI1 phase direction output port	O	X
QEI1_A QEI1_B QEI1_IDX	I	QEI1 phase-A, phase-B, and index input ports	O	X

15.1 QEI block diagram

Figure 37 describes normal mode of MPWM in block diagram.

Figure 37. QEI Block Diagram



16 12-bit Analog-to-Digital Converter (ADC)

ADC block of A33M11x series consists of an independent ADC unit featuring the followings:

- 22 Channel Analog Input
- Single mode and Continuous conversion mode
- Maximum 8 sequential conversion support
- Software trigger support
- Three internal trigger source (PWM, TIMER) Support
- Adjustable sample and hold time

Table 25 introduces pins assigned for ADC.

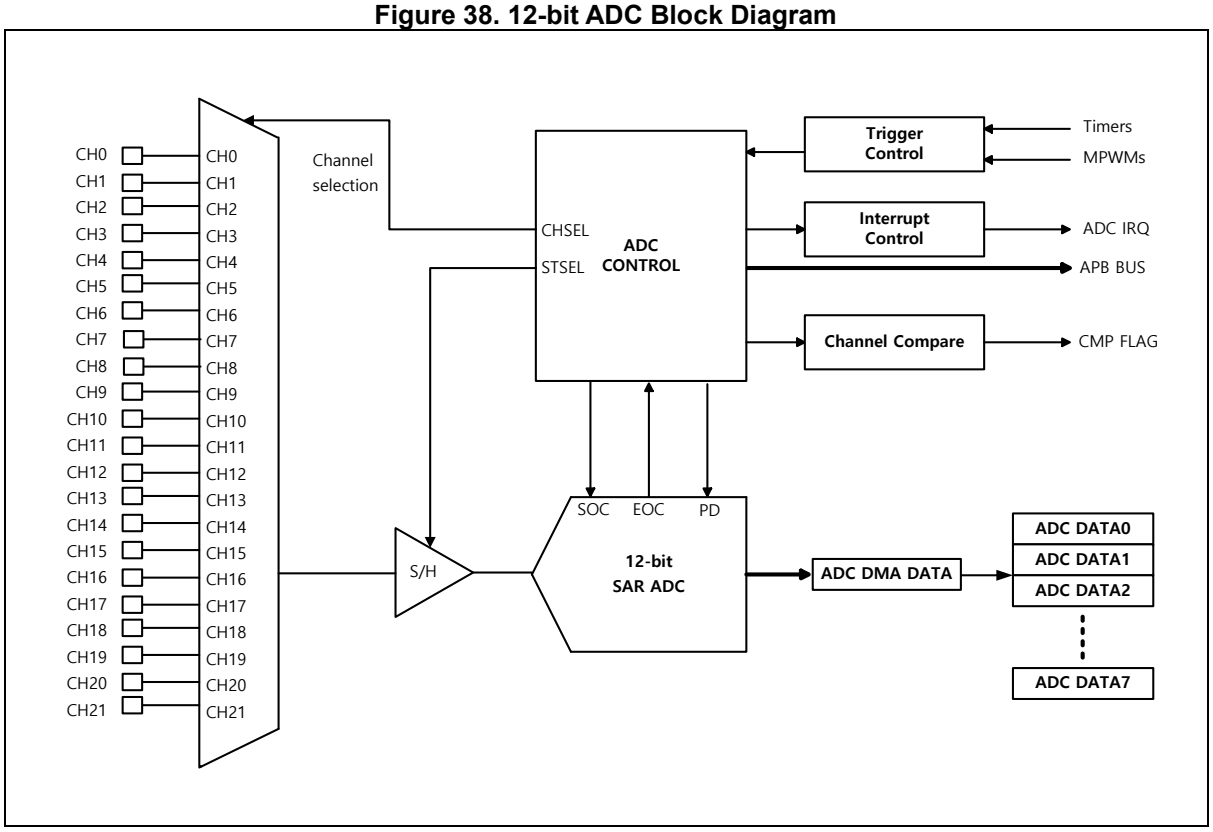
Table 25. Pin Assignment of ADC: External Pins

Pin name	Type	Description	Supported Packages		
			A33M116RL **A33M116RM** **A33M114RL** (LQFP-64)	**A33M116CL** **A33M114CL** **A33M114SN** (LQFP-48)	**A33M114SN** (LQFP-44)
AN0	A	ADC input 0	O	O	O
AN1	A	ADC input 1	O	O	O
AN2	A	ADC input 2	O	O	O
AN3	A	ADC input 3	O	O	O
AN4	A	ADC input 4	O	O	X
AN5	A	ADC input 5	O	O	X
AN6	A	ADC input 6	O	O	O
AN7	A	ADC input 7	O	O	O
AN8	A	ADC input 8	O	O	O
AN9	A	ADC input 9	O	O	O
AN10	A	ADC input 10	O	O	O
AN11	A	ADC input 11	O	O	X
AN12	A	ADC input 12	O	O	X
AN13	A	ADC input 13	O	O	O
AN14	A	ADC input 14	O	O	O
AN15	A	ADC input 15	O	O	O
AN16	A	ADC input 16	X	O	O
AN17	A	ADC input 17	X	O	O
AN18	A	ADC input 18	X	O	O
AN19	A	ADC input 19	X	O	O

16.1 12-bit ADC block diagram

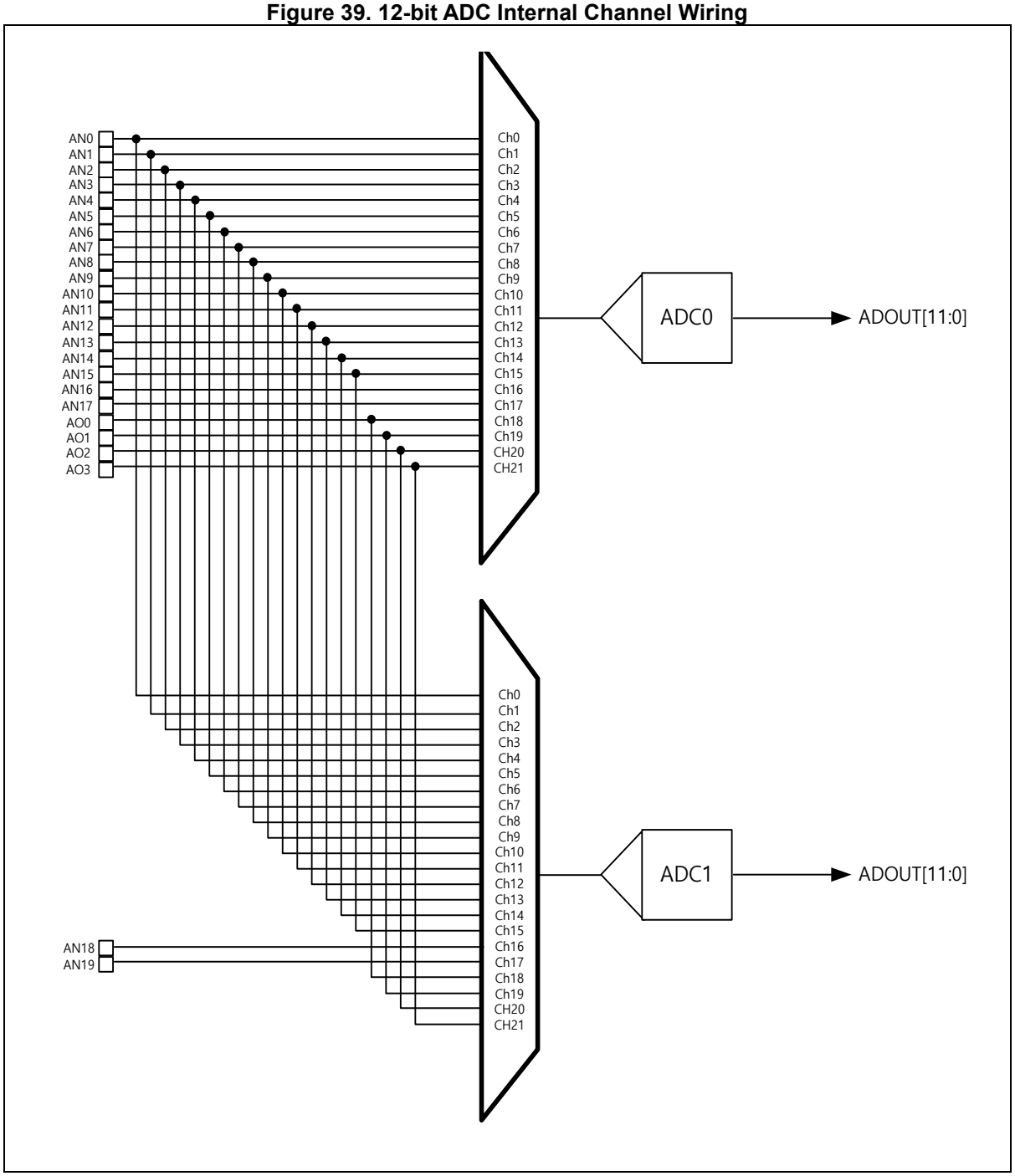
In this section, 12-bit ADC is described in a block diagram in Figure 38.

Figure 38. 12-bit ADC Block Diagram



16.2 Internal channel wiring

Figure 39. 12-bit ADC Internal Channel Wiring



17 Analog Front End (AFE)

The AFE (Analog Front End) is an Op-Amp and a comparator interface controller. The A33M11x series is equipped with four Op-Amps and comparators. The OPAMPs amplify their voltage difference between positive analog input signals and negative analog input signals. A comparator outputs a signal from its I/O pin or triggers an interrupt based on comparison between the voltages of two analog signals.

AFE of A33M11x series features the followings:

- Four op-amps and comparators
- OPAMP outputs are used in connection with ADC channels or AOx Pins
- The comparator output supports the debounce function.
- Level and edge interrupt support

Table 26 introduces pins assigned for AFE.

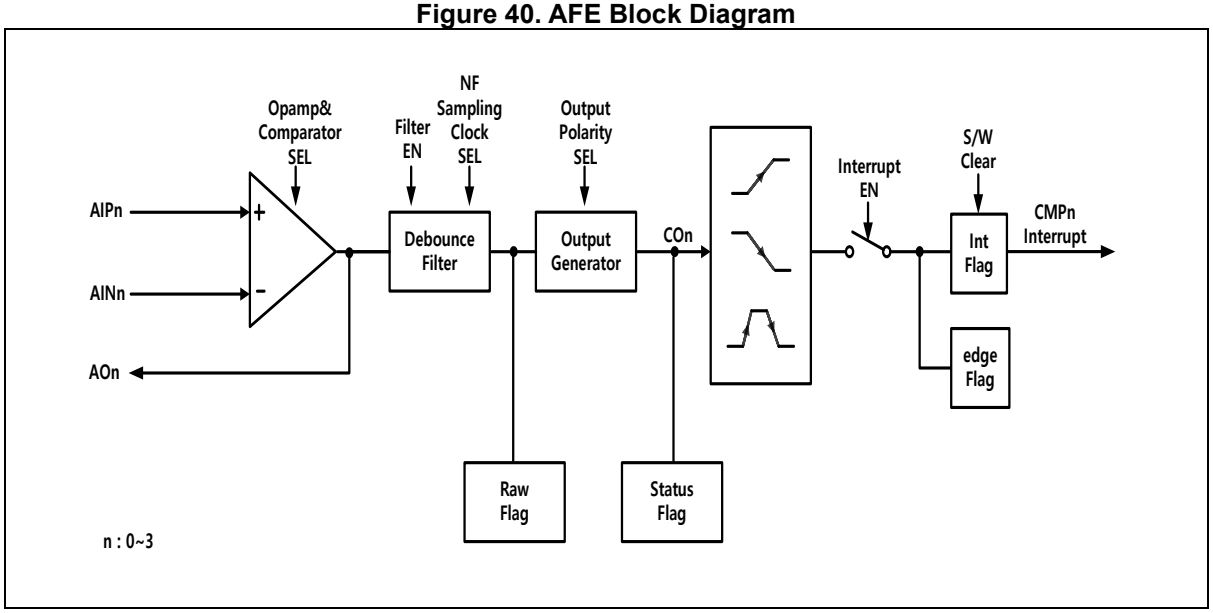
Table 26. Pin Assignment of AFE: External Pins

Pin name	Type	Description	Supported Packages	
			A33M116RL **A33M116RM** **A33M114RL** (LQFP-64)	**A33M116CL** **A33M114CL** **A33M114SN** (LQFP-48, 44)
AIN0	A	Analog Input 0 (-)	O	O
AIP0	A	Analog Input 0 (+)	O	O
AO0/CO0	A	Op-Amp & Comparator Output 0	O	O
AIN1	A	Analog Input 1 (-)	O	O
AIP1	A	Analog Input 1 (+)	O	O
AO1/CO1	A	Op-Amp & Comparator Output 1	O	O
AIN2	A	Analog Input 2 (-)	O	O
AIP2	A	Analog Input 2 (+)	O	O
AO2/CO2	A	Op-Amp & Comparator Output 2	O	O
AIN3	A	Analog Input 3 (-)	O	O
AIP3	A	Analog Input 3 (+)	O	O
AO3/CO3	A	Op-Amp & Comparator Output 3	O	O

17.1 AFE block diagram

In this section, AFE is described in a block diagram in Figure 40.

Figure 40. AFE Block Diagram



18 Cyclic Redundancy Check (CRC)

The cyclic redundancy check (CRC) module is used to load 32/16/8/7-bit CRC codes. Application programs employs CRC-based technologies to examine the integrity of data transfers, storages, and flash memories in conformance with functional safety standards.

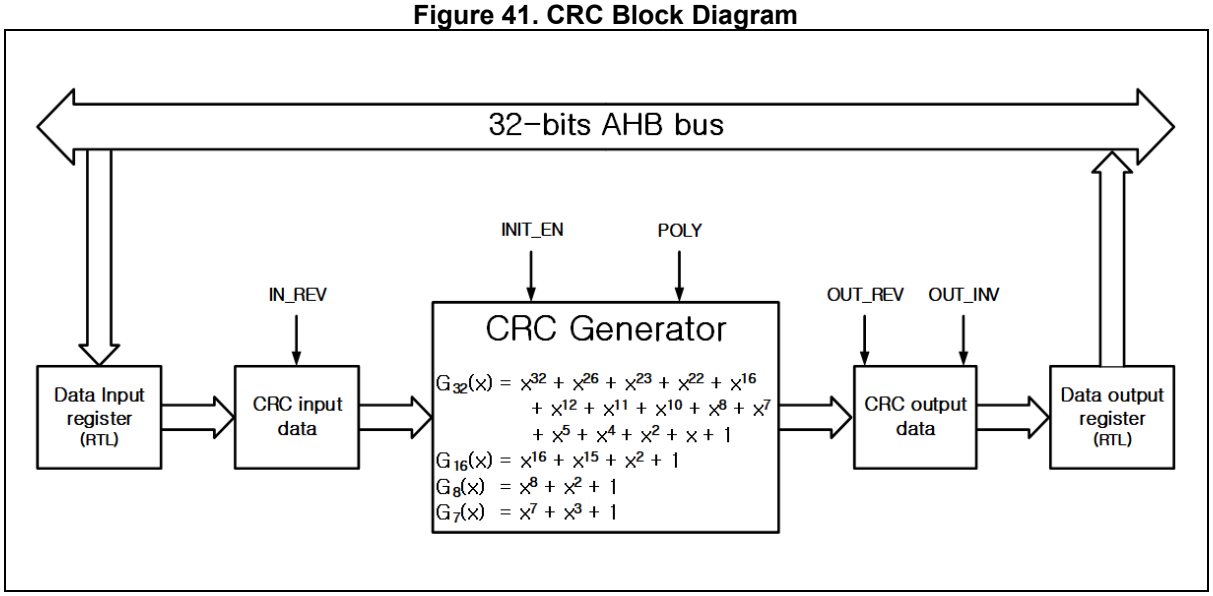
CRC of A33M11x series features the followings:

- Automatic CRC and user CRC modes
- Handles 8-, 32-bit data size
- Input buffer to avoid bus stall during calculation
- CRC computation done in 4 AHB clock cycles (HCLK) for the 32-bit data size
- Reversibility option on I/O data

18.1 CRC block diagram

In this section, CRC is described in a block diagram in Figure 41.

Figure 41. CRC Block Diagram



19 Electrical characteristics

19.1 Absolute maximum ratings

Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions.

Table 27. Absolute Maximum Rating

Parameter	Symbol	Ratings	Unit	Remark
Supply Voltage	VDD	-0.5 – +6	V	—
Normal Pin	V_I	-0.5 – VDD+0.5	V	Voltage on any pin with respect to VSS
	V_O	-0.5 – VDD+0.5	V	
	I_{OH}	10	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	ΣI_{OH}	120	mA	Maximum current (ΣI_{OH})
	I_{OL}	20	mA	Maximum current sunk by (I_{OL} per I/O pin)
	ΣI_{OL}	120	mA	Maximum current (ΣI_{OL})
Input external main clock range	—	4-16	MHz	—
Storage Temperature	T_{STG}	-55 – +125	℃	—
Operating Temperature	Top	-40-+105	℃	—

19.2 Recommended operating conditions

Table 28. Recommended Operating Condition

(Temperature: -40℃ to +105℃)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Supply Voltage	VDD	ADC excluded	2.5	—	5.5	V
		Only ADC	2.7	—	5.5	V
Operating Frequency	FREQ	HSE	4	—	16	MHz
		HSI	31.68	32	32.32	MHz
		LSI500KHz	350	500	650	KHz
		PLL	—	—	96	MHz
Operating Temperature	Top	Top	-40	—	+105	℃

19.3 ADC characteristics

Table 29. ADC Electrical Characteristics

(Temperature: -40℃ to +105℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating voltage	AVDD	—	2.7	5	5.5	V
Resolution		—	—	—	12	Bit
Operating current	IDDA	AVDD = 5.0V Input buffer off	—	3.0	—	mA
		AVDD = 5.0V Input buffer on	—	4.4	—	mA
Analog input range	V_{AN}	—	VSS	—	AVDD	V
Power Down Current	I_{OFF}	-	50	-		nA
Analog Input Capacitance	C_{AIN}	-	14	-		pF
Conversion time	t_{CONV}	—	15*MCLK	-	45*MCLK	us
Conversion rate	F_{CONV}	AVDD > 4.0V (Input buffer on, maxf_{AIN})	—	—	1.3(1.2)	MHz
		AVDD > 3.2V	—	—	1.0	MHz
		AVDD > 2.7V	—	—	0.76	MHz
Operating frequency	ACLK	—	—	—	25	MHz
DC accuracy	INL	—	—	—	±4	LSB
	DNL	—	—	—	±2	LSB
Zero offset error	ZOE	TBD	—	±4	—	LSB
Full scale error	FSE	TBD	—	±4	—	LSB

19.4 Power on reset characteristics

Table 30. POR Electrical Characteristics

(Temperature: -40℃ to +105℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating current	I_{DD}	—	—	0.5	4	uA
POR set level	V_{set}	—	1.05	1.20	1.35	V
VDD Voltage Rising Time	t_R	—	0.05	—	30.0	V/ms
POR reset level	V_{reset}	—	1.00	1.10	1.20	V

19.5 Low voltage reset characteristics

Table 31. Low Voltage Reset Characteristics

(Temperature: -40℃ to +105℃)

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
Detection level	V_{LVR}	T_A = –40˚C to +105˚C, Falling voltage	2.01	2.12	2.23	V
			2.19	2.30	2.42	
			2.35	2.47	2.59	
			2.54	2.67	2.80	
			2.89	3.04	3.19	
			3.02	3.18	3.34	
			3.41	3.59	3.77	
			3.53	3.72	3.91	
			3.83	4.03	4.23	
			3.99	4.20	4.41	
			4.26	4.48	4.70	
Hysteresis	—	—	—	50	150	mV
Noise cancelling time	—	—	—	2	—	us
Operation current	I_{DD}	—	—	4.0	5.0	uA
Operation current(STOP)	$I_{DD, STOP}$	—	—	2.5	250	nA

19.6 Low voltage indicator characteristics

Table 32. Low Voltage Indicator Characteristics

(Temperature: -40℃ to +105℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Detection level	V_{LVI}	T_A = –40˚C to +105˚C, Falling voltage	2.54	2.67	2.80	V
			2.89	3.04	3.19	
			3.02	3.18	3.34	
			3.41	3.59	3.77	
			3.53	3.72	3.91	
			3.83	4.03	4.23	
			3.99	4.20	4.41	
			4.26	4.48	4.70	
Hysteresis	—		—	50	150	mV
Noise cancelling time	—		—	2	—	us
Operation current	I_{DD}		—	4.0	5.0	uA
Operation current(STOP)	$I_{DD, STOP}$		—	2.5	250	nA

19.7 Analog front end characteristics

Table 33. Op-Amp Characteristics

(Temperature: -40℃ to +105℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating voltage	VDD	—	2.5	—	5.5	V
Operating Current	IDD (RMS)	AVDD=5V, 25℃	—	630	800	uA
Input Offset Voltage	VIO	—	—	±1.5	—	mV
Input Voltage Range	VI	—	0		AVDD	V
Slew Rate Rising	Srr	CL=200pF	—	20	—	V/us
Slew Rate Falling	Srf	CL=200pF	—	20	—	V/us
Gain Error	GE	Gain = x20	—	—	3	%
Common Mode Rejection Ratio	CMRR	—	—	90	—	dB
Power Supply Rejection Ratio	PSRR	—	—	90	—	dB
Gain Bandwidth	fGB	CL=200pF	—	5	—	MHz
Open Loop Voltage Gain	AV	CL=20pF	—	100	—	dB
Phase Margin	tON	CL=20pF	—	80	—	Degree

Table 34. Comparator Characteristics

(Temperature: -40℃ to +105℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating voltage	VDD	—	2.5	—	5.5	V
Input Offset Voltage	VIO	—	-5	—	+5	mV
Propagation Delay	TDR	Rising	—	—	150	ns
	TDF	Falling	—	—	150	ns

19.8 High frequency internal RC oscillator characteristics

Table 35. High Frequency Internal RC Oscillator Characteristics

(Temperature: -40℃ to +105℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating voltage	VDD	—	2.5	—	5.5	V
Operating current	I_{HIRC}	—	—	330	400	uA
Operating frequency	f_{32M}	-20℃ ~ 85℃	31.68	32	32.32	MHz
		-40℃ ~ 105℃	31.52	32	32.48	MHz
Frequency error	f_E	@ -20℃ ~ 85℃	-1.0	—	1.0	%
		@ -40℃ ~ 105℃	-1.5	—	1.5	%

19.9 Low frequency internal RC oscillator characteristics

Table 36. Low Frequency (500KHz) Internal RC Oscillator Characteristics

(Temperature: -40℃ to +105℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating voltage	VDD		2.5	—	5.5	V
Operating Current	I_{LSI}	–	-	1.5	4.9	uA
Power Down Current	I_{OFFLSI}	–	-	2.6	682	nA
Operating Frequency	f_{OUT}	–	350	500	650	KHz
Frequency Error	f_E		-30		30	%

19.10 DC electrical characteristics

Table 37. DC Electrical Characteristics

(Temperature: -40℃ to +105℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input high voltage	V_{IH}	PA,PB,PC,PD,PF,PG,nRESET, nBOOT	0.8VDD	—	—	V
Input low voltage	V_{IL}	PA,PB,PC,PD,PF,PG,nRESET, nBOOT	—	—	0.2VDD	V
Output high voltage	V_{OH}	VDD=5V, I_{OH} = – 3mA	VDD-1.0	—	—	V
Output low voltage	V_{OL}	VDD=5V, I_{OL}=3mA	—	—	1.0	V
Output Low Current	I_{OL}	—	—	—	3	mA
Output High Current	I_{OH}	—	-3	—	—	mA
Input high leakage current	I_{IH}	All Input ports	—	—	4	uA
Input low leakage current	I_{IL}	All Input ports	– 4	—	—	uA
Pull-up resistor	R_{PU}	R_{MAX}:V_{DD}=5.0V R_{MIN}:V_{DD}=3.0V	30	—	105	KΩ

19.11 Supply current characteristics

Table 38. Supply Current Characteristics (Normal and Sleep Mode)

Parameter	Symbol	Condition	HCLK	Typ.	Max	unit
Normal operation	IDD_{RUN}	External clock with PLL code running from Flash Low-speed(LSI500K) and High-speed(HSI32M) internal oscillator OFF PCLK = HCLK	96MHz	15.4	30.8	mA
			60MHz	10.4	20.8	
			30MHz	6.2	12.4	
			16MHz	4.2	8.4	
		External clock(PLL not used) code running from Flash Low-speed(LSI500K) and High-Speed(HSI32M) internal oscillator OFF PCLK = HCLK	8MHz	2.9	5.8	
		High-speed(HSI32M) internal oscillator clock code running from Flash Low-speed(LSI500K) internal oscillator and External clock OFF PCLK = HCLK	32MHz	5.8	11.6	
		Low-speed(LSI500K) internal oscillator clock code running from Flash High-speed internal(HSI32M) oscillator and External clock OFF PCLK = HCLK	500KHz	324	648	uA
Sleep mode	IDD_{SLEEP}	External clock with PLL code running from Flash Low-speed(LSI500K) and High-speed(HSI32M) internal oscillator OFF PCLK = HCLK	96MHz	8.6	17.2	mA
			60MHz	6.1	12.2	
			30MHz	4	8	
			16MHz	3	6	
		External clock(PLL not used) code running from Flash Low-speed(LSI500K) and High-Speed(HSI32M) internal oscillator OFF PCLK = HCLK	8MHz	2.1	4.2	
		High-speed(HSI32M) internal oscillator clock code running from Flash Low-speed(LSI500K) internal oscillator and External clock OFF PCLK = HCLK	32MHz	2.5	5	

Table 38. Supply Current Characteristics (Normal and Sleep Mode) (continued)

Parameter	Symbol	Condition	HCLK	Typ.	Max	unit
		Low-speed(LSI500K) internal oscillator clock code running from Flash High-speed internal(HSI32M) oscillator and External clock OFF PCLK = HCLK	500KHz	272	544	uA

NOTES:

1. Typical values are measured at T_A=25℃, and V_{DD}=5V
2. All I/O pins are in output mode and output low status.
3. All peripherals are disabled.
4. The Flash access time is adjusted to HCLK frequency (0 wait state from 0 to 28MHz, 1 wait state from 28 to 56MHz and 2 wait states above)

Table 39. Supply Current Characteristics (Stop Mode)

Parameter	Symbol	Condition	Typ.	Max		unit
				T_A=25℃	T_A=105℃	
Stop mode	IDD_{STOP}	Internal VDC regulator disable mode, Low-speed and high-speed internal RC oscillators and External clock OFF (no independent watchdog and Low voltage reset)	100	350	3000	uA

NOTES:

1. Typical values are measured at T_A=25℃, and V_{DD}=5V
2. All I/O pins are in output mode and output low status.
3. All peripherals are disabled.
4. The Flash access time is adjusted to HCLK frequency (0 wait state from 0 to 28MHz, 1 wait state from 28 to 56MHz and 2 wait states above)

19.12 Internal Flash ROM characteristics

Table 40. Internal Flash ROM Characteristics

(Temperature: -40℃ to +105℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Max available clock frequency	—	0-wait	—	—	28	MHz
Reset cycle time	$t_{RSTBUSY}$	—	8	—	—	us
Fuse program time	$t_{FRDBUSY}$		—	—	6	us
Normal program time	$t_{PGMBUSY}$	—	—	—	25	us
Burst program time	$t_{BMPGMBUSY}$		—	—	15	us
Normal Page erase time	$t_{PERSBUSY}$	—	—	—	2	ms
Sector erase time	$t_{SERSBUSY}$	—	—	—	2	ms
Mat erase time	$t_{MERSBUSY}$	—	—	—	8	ms
Endurance of write/erase	N_{FWE}	T_A=25 ˚C, Page unit	10,000	—	—	Times
Retention time	t_{FRT}	—	10	—	—	Years

19.13 Main oscillator characteristics

Table 41. Main Oscillator Characteristics

(Temperature: -40℃ to +105℃)

Oscillator	Parameter	Conditions	Min	Typ.	Max	Units
Operating voltage	VDD	—	1.8	5.0	5.5	V
Operating current	IDD	VDD≥2.4V NOTE1		0.91	1.5	mA
Power down current	I_{STOP}	—	—	0.2	30	nA
Output frequency	XOUT input frequency	VDD≥2.4V NOTE1	1.0	—	16.0	MHz
Crystal input (low)	V_{IL}	—	—	—	0.2VDD	V
Crystal input (high)	V_{IH}	—	0.8VDD	—	—	V
Crystal out (low)	V_{OL}	—	—	—	0.2VDD	V
Crystal out (high)	V_{OH}	—	0.8VDD	—	—	V
External load cap	C_L	4M≤f_{OUT}≤12M	10	22	30	pF
		12M≤f_{OUT}≤16M	7	18	22	pF
Feedback resistance	R_{FB}	VDD=5V	0.7	1.0	1.3	MΩ

NOTE: EISEL = 0x0, ENFSEL = 0x3

Figure 42. Crystal/Ceramic Oscillator

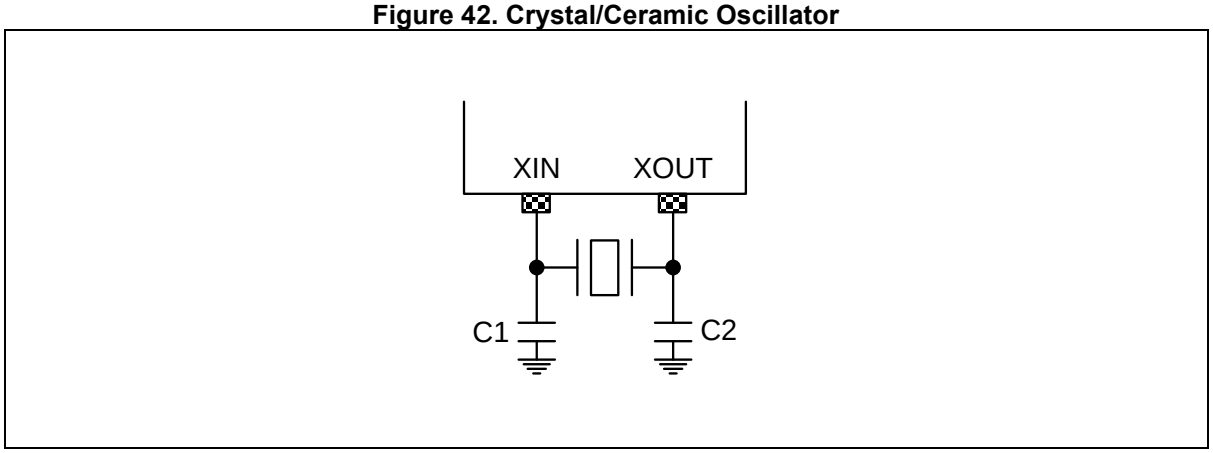


Figure 43. External Clock

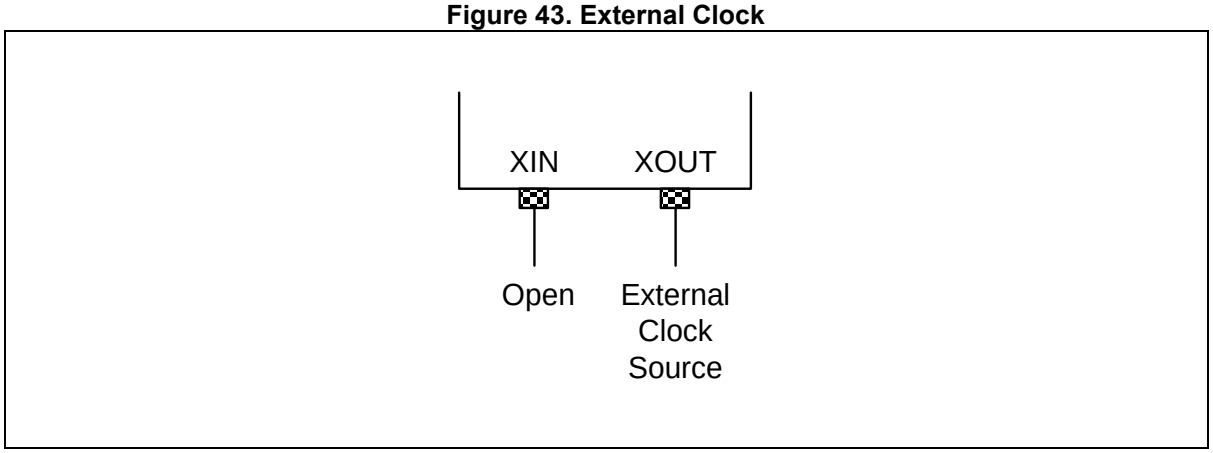
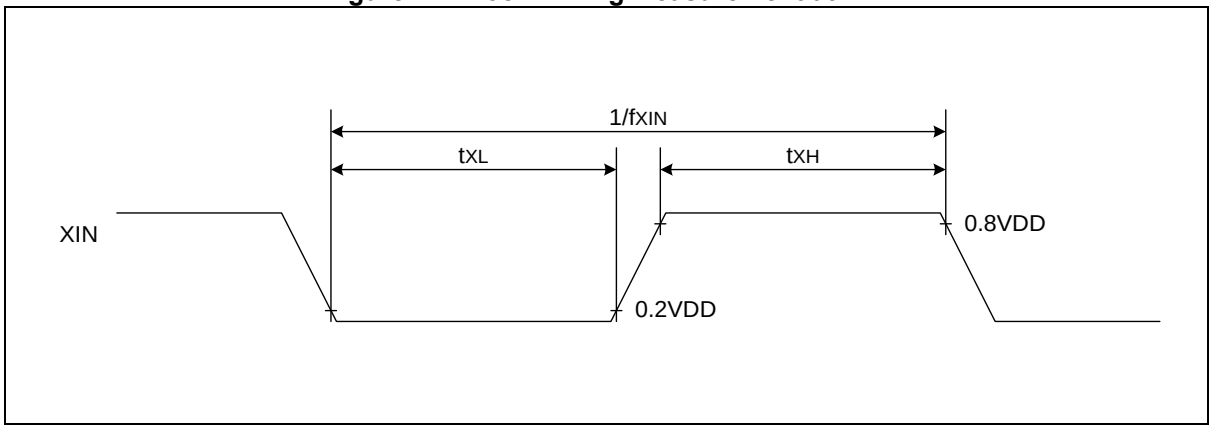


Figure 44. Clock Timing Measurement at XIN



19.14 PLL electrical characteristics

Table 42. PLL Electrical Characteristics

(Temperature: -40℃ to +105℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating voltage	VDD	—	2.5	—	5.5	V
Operating current	I_{DD}	—	—	0.5	1	mA
Output frequency	f_{OUT}	—		—	96	MHz
Duty	f_{DUTY}	—	40	—	60	%
Input frequency	$f_{PLLINCLK}$	—	4	8	16	MHz
FXIN frequency	f_{XIN}	—	1	2	3	MHz
P-P jitter	t_{JITTER}	@Lock State	—	—	500	ps

NOTE: f_{XIN} = $f_{PLLINCLK}$/Pre divider value

20 Package information

This chapter provides A33M11x series package information.

20.1 64 LQFP package information

Figure 45. 64 LQFP (10x10) Package Outline

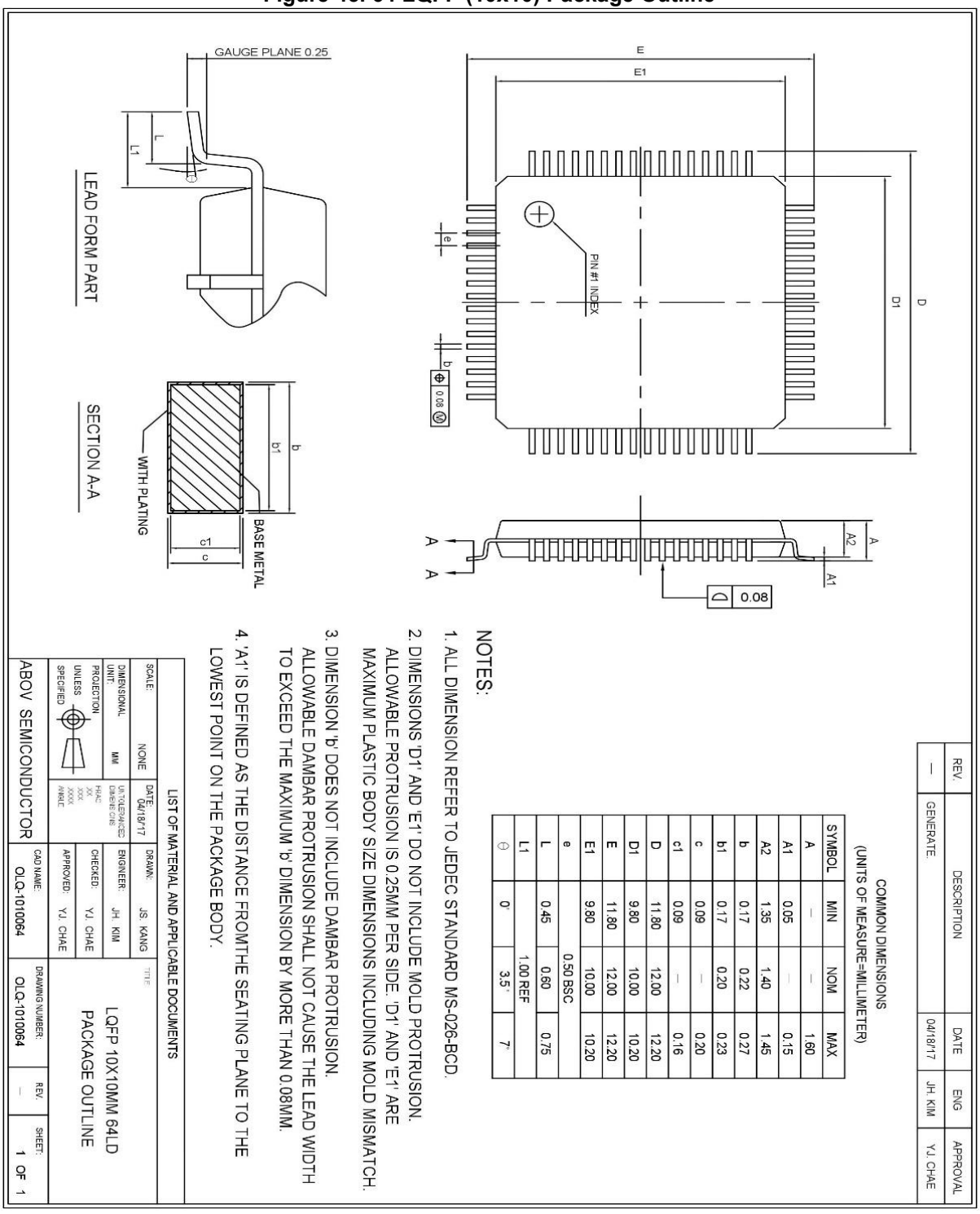
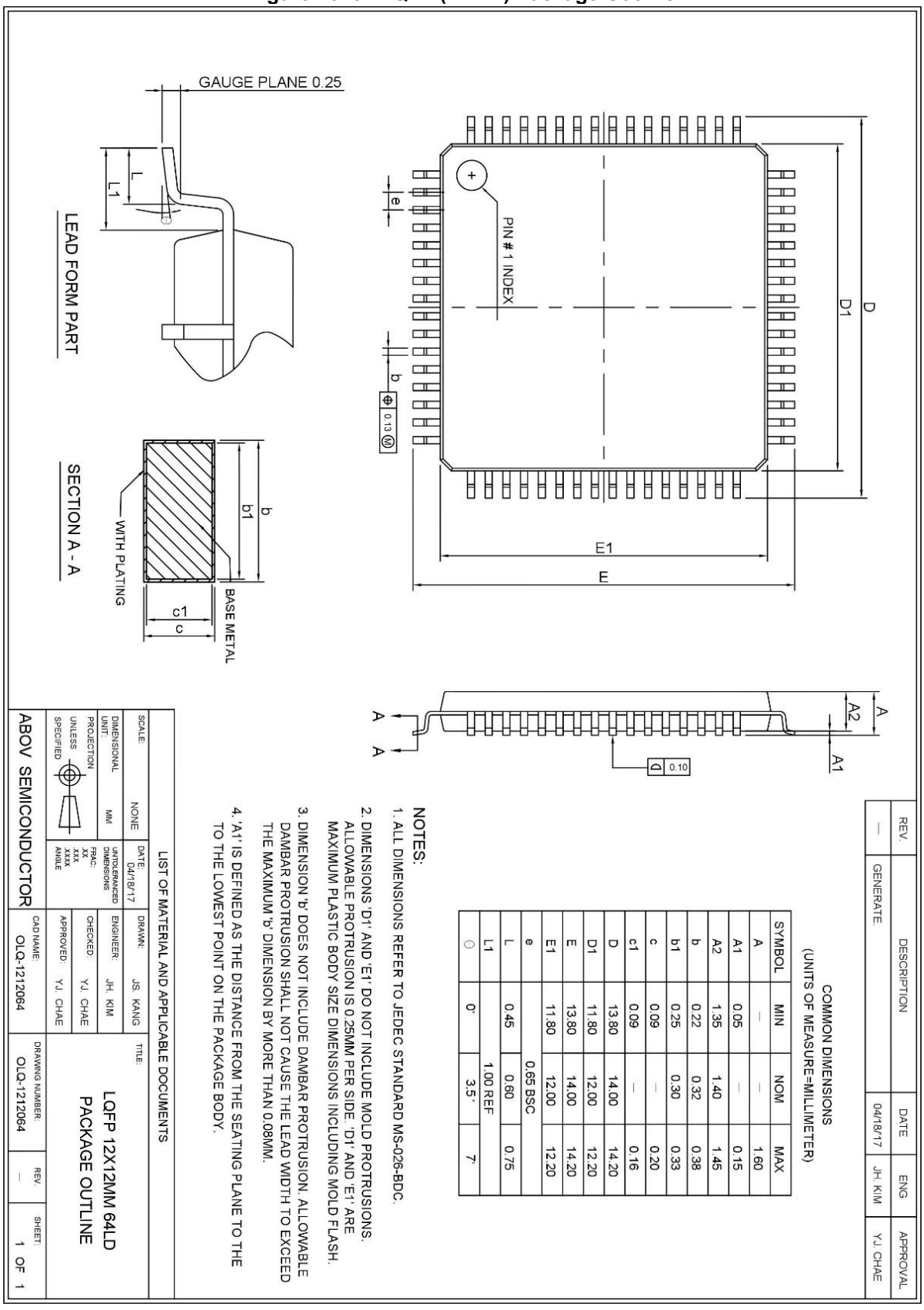
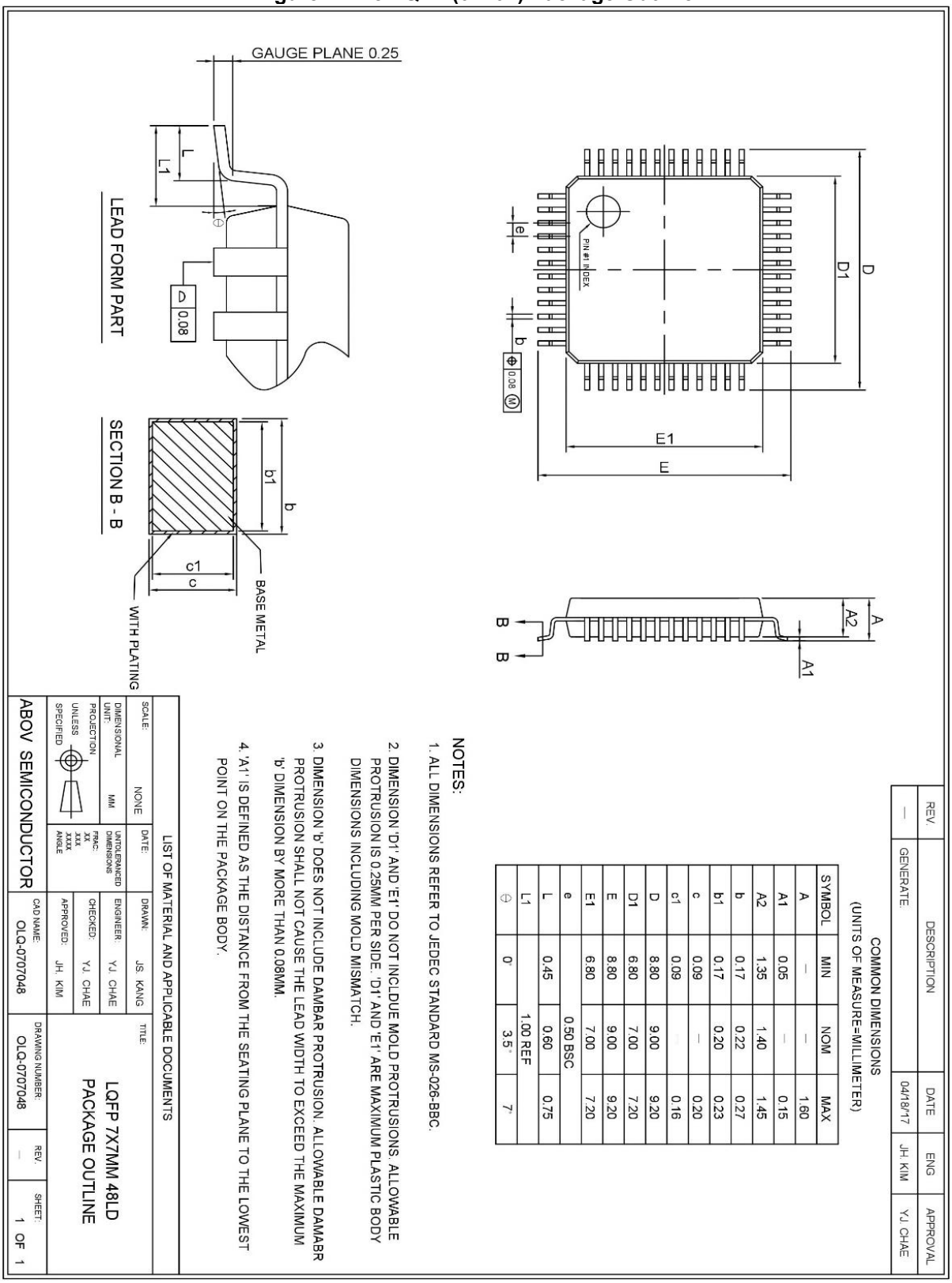


Figure 46. 64 LQFP (12x12) Package Outline



20.2 48 LQFP package information

Figure 47. 48 LQFP (07x07) Package Outline



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09		0.16
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e		0.50 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026-BBC.
2. DIMENSION 'D1' AND 'E1' DO NOT INCLDUE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. 'D1' AND 'E1' ARE MAXIMUM PLASTIC BODY DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMABR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 'b' DIMENSION BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

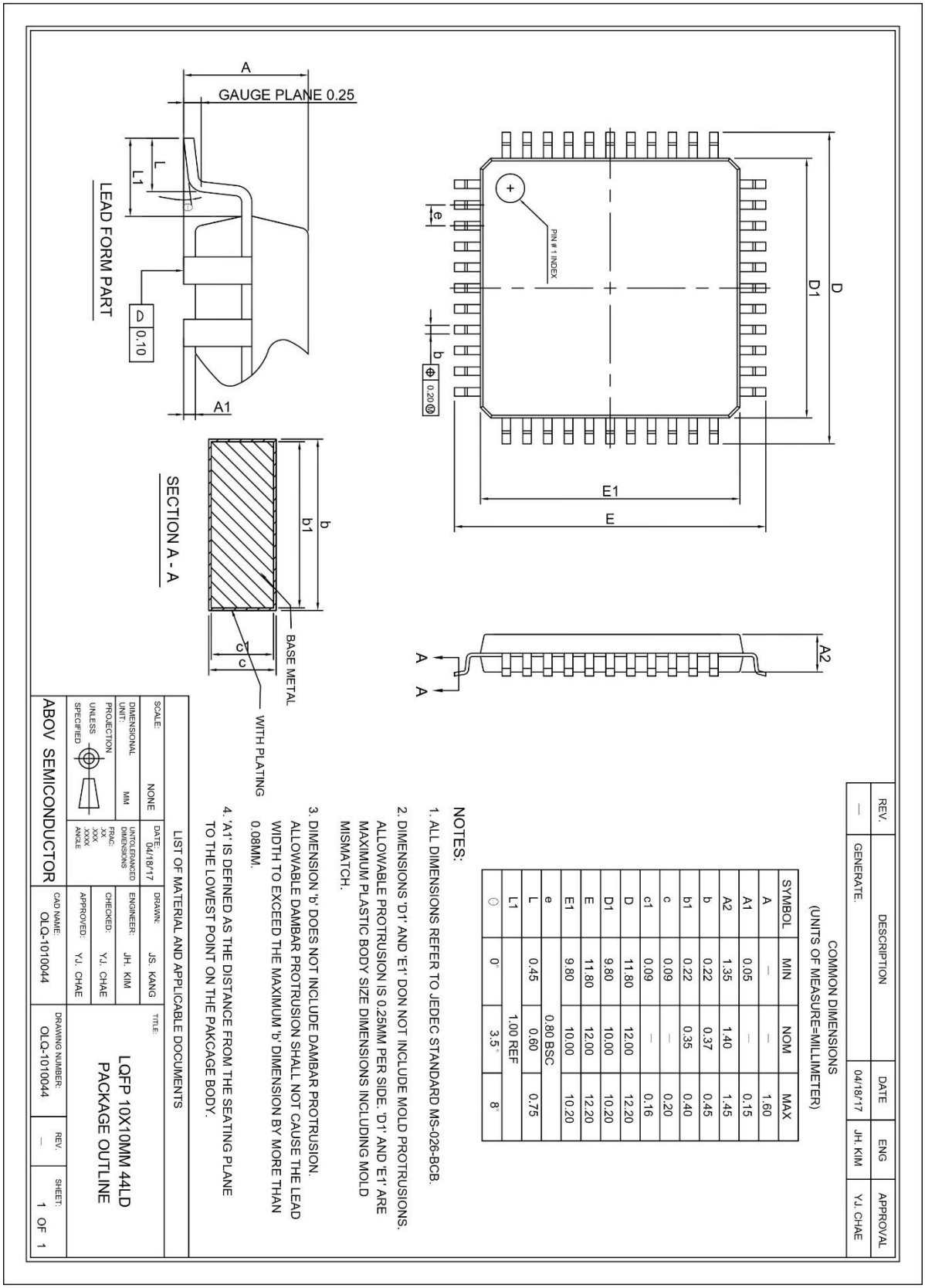
REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE:	04/18/17	JH. KIM	YJ. CHAE

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE:	DRAWN: JS. KANG	TITLE: LQFP 7X7MM 48LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS FRAC: XX .XX .XXX ANGLE	ENGINEER: YJ. CHAE	
PROJECTION UNLESS SPECIFIED		CHECKED: YJ. CHAE	
ABOV SEMICONDUCTOR	CAD NAME: OLQ-070748	APPROVED: JH. KIM	DRAWING NUMBER: OLQ-070748 REV. — SHEET: 1 OF 1

20.3 44 LQFP package information

Figure 48. 44 LQFP (10x10) Package Outline



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.22	0.37	0.45
b1	0.22	0.35	0.40
c	0.09	—	0.20
c1	0.09	—	0.16
D	11.80	12.00	12.20
D1	9.80	10.00	10.20
E	11.80	12.00	12.20
E1	9.80	10.00	10.20
e		0.80 BSC.	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	8°

NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026-BCB.
2. DIMENSIONS 'D1' AND 'E1' DON NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. 'D1' AND 'E1' ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 'b' DIMENSION BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PAKCAGE BODY.

REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE:	04/18/17	JH. KIM	YJ. CHAE

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE: 04/18/17	DRAWN: JS. KANG	TITLE: LQFP 10X10MM 44LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS	ENGINEER: JH. KIM	
PROJECTION	FRAC: XX± XXX± XXXX± ANGLE	CHECKED: YJ. CHAE	
UNLESS SPECIFIED		APPROVED: YJ. CHAE	
ABOV SEMICONDUCTOR	CAD NAME: OLQ-1010044	DRAWING NUMBER: OLQ-1010044	REV: —
			SHEET: 1 OF 1

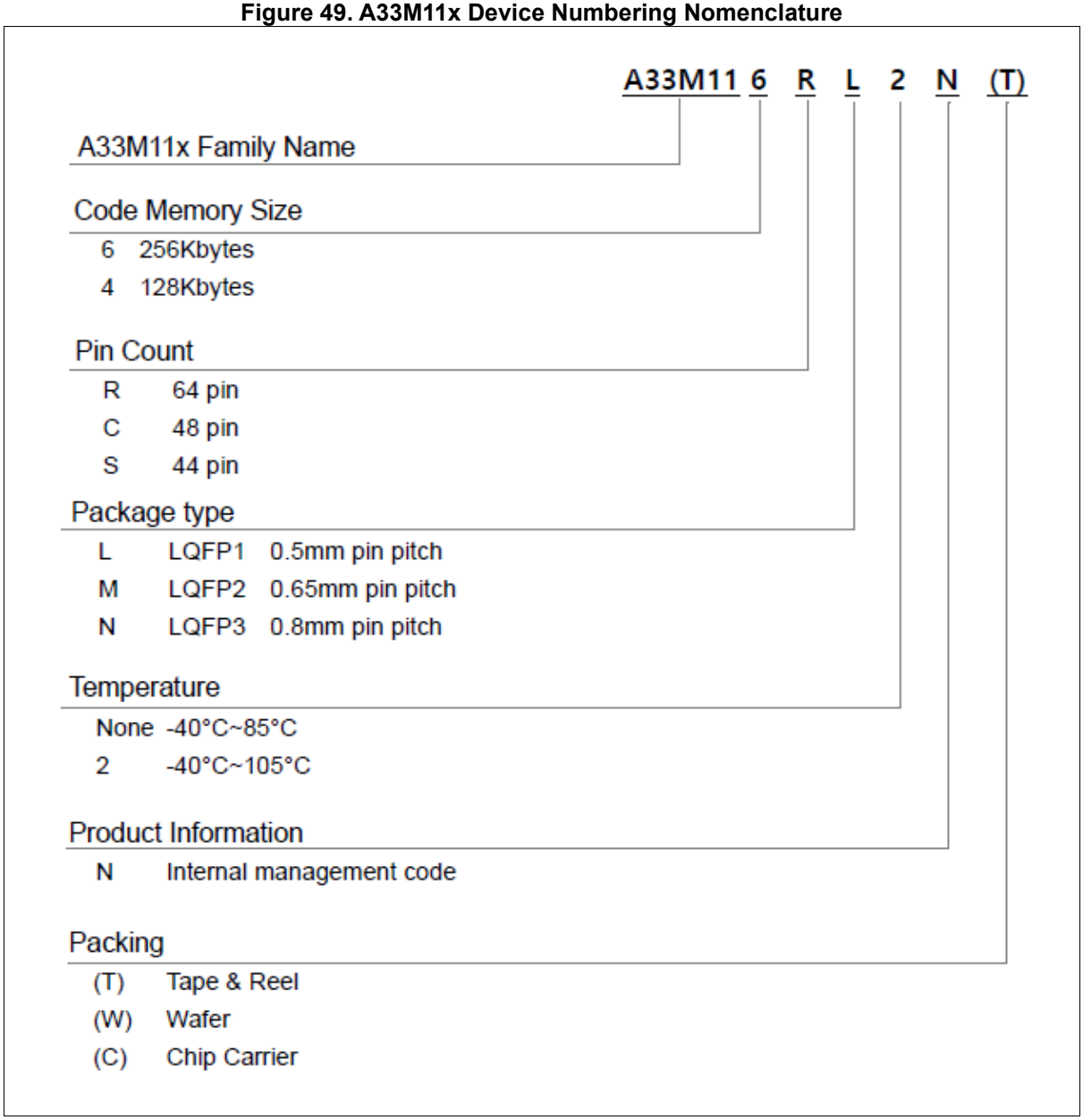
21 Ordering information

Table 43. A33M11x Series Device Ordering Information

Device name	Flash	SRAM	SPI	UART	I2C	OPAMP (COMP)	TIMER	MPWM	ADC	I/O ports	Package
A33M116RL	256KB	16KB	2	4	2	4	8	2	16	56	LQFP-64
A33M116RM*	256KB	16KB	2	4	2	4	8	2	16	56	LQFP-64
A33M114RL*	128KB	16KB	2	4	2	4	8	2	16	56	LQFP-64
A33M116CL*	256KB	16KB	2	3	2	4	8	2	20	45	LQFP-48
A33M114CL*	128KB	16KB	2	3	2	4	8	2	20	45	LQFP-48
A33M114SN*	128KB	16KB	2	3	2	4	8	2	16	41	LQFP-44

* For available options or further information on the devices marked with "*", please contact the ABOV sales offices.

Figure 49. A33M11x Device Numbering Nomenclature



22 Development tools

This chapter introduces wide range of development tools for A33M11x. ABOV offers software tools, debuggers, and programmers to help a user in generating right results to match target applications. ABOV supports entire development ecosystem of the customers.

22.1 Compiler

ABOV semiconductor does not provide any compiler for A33M11x. However, since A33M11x have ARM's high-speed 32-bit Cortex-M3 Cores for their CPU, you can use all kinds of third party's standard compiler such as Keil C Compiler. These compilers' output debug information can be integrated with our A-Link and A-Link Pro. Please visit our website www.abovsemi.com for more information regarding the A-Link and A-Link Pro.

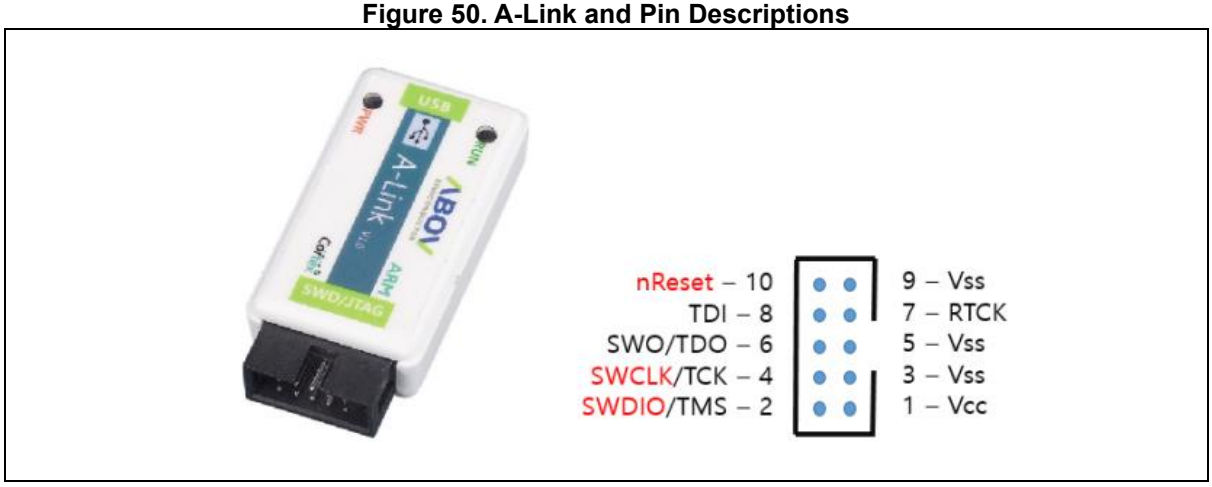
22.2 Debugger

The A-Link and A-Link Pro support ABOV Semiconductor's A33M11x MCU emulation in SWD Interface. The A-Link and A-Link Pro use two wires interfacing between PC and MCU, which is attached to user's system. The A-Link and A-Link Pro can read or change the value of MCU's internal memory and I/O peripherals. In addition, the A-Link and A-Link Pro control MCU's internal debugging logic. This means A-Link and A-Link Pro control emulation, step run, monitoring and many more functions regarding debugging.

The A-Link and A-Link Pro run underneath MS operating system such as MS-Windows NT/ 2000/ XP/ Vista/ 7/ 8/ 8.1/ 10 (32-bit, 64-bit).

Programming information using the A-Link and A-Link Pro are provided in Figure 50. More detailed information about the A-Link and A-Link Pro, please visit our website www.abovsemi.com and download the debugger S/W and documents.

Figure 50. A-Link and Pin Descriptions



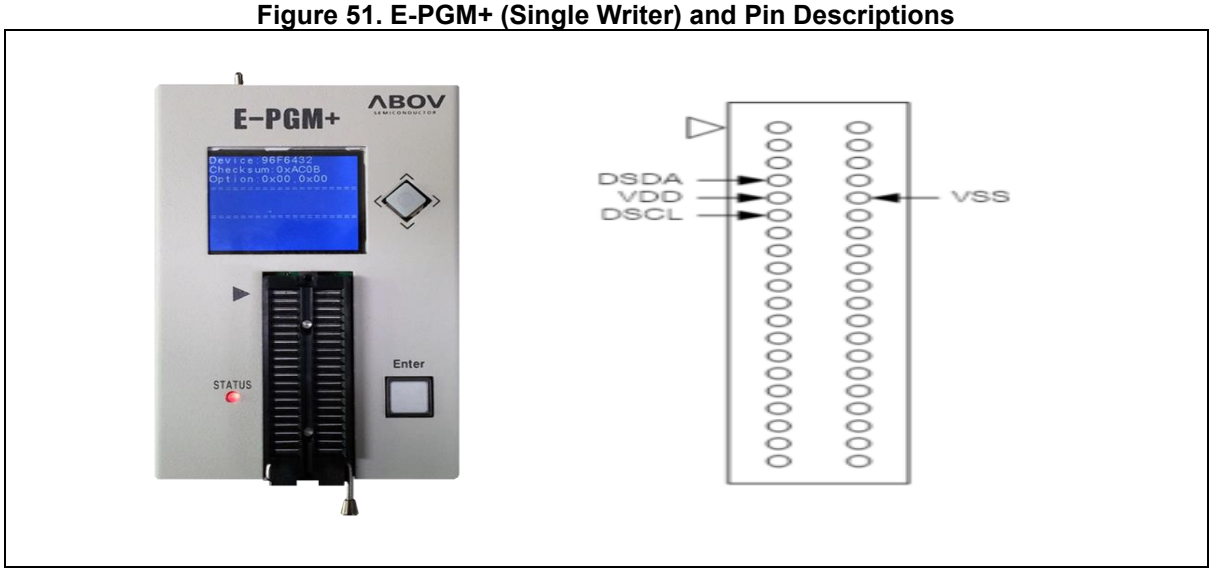
22.3 Programmer

22.3.1 E-PGM+

E-PGM+ is a single programmer, and allows a user to program on the device directly.

- Support ABOV devices
- 2 to 5 times faster than E-PGM+
- Main controller: 32-bit MCU @ 72MHz
- Buffer memory: 1MB

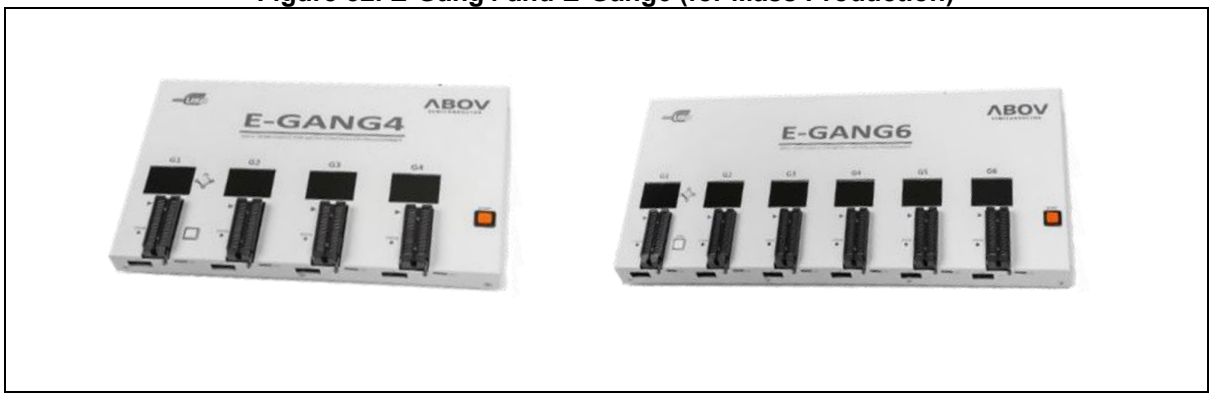
Figure 51. E-PGM+ (Single Writer) and Pin Descriptions



22.3.2 Gang programmer

E-Gang4 and E-Gang6 allows a user to program on multiple devices at a time. They run not only in PC controlled mode but also in standalone mode without PC control. USB interface is available and it is easy to connect to the handler.

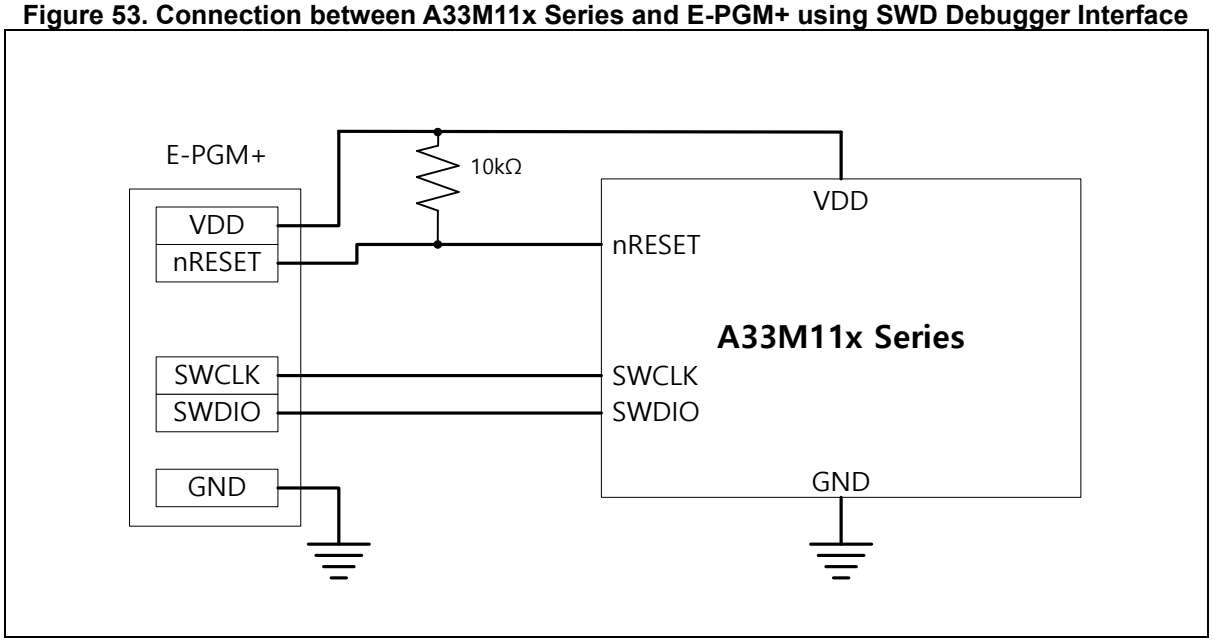
Figure 52. E-Gang4 and E-Gang6 (for Mass Production)



22.4 SWD debug mode and E-PGM+ connection

Connections for SWD debugger interface or E-PGM+ is described in Figure 53.

Figure 53. Connection between A33M11x Series and E-PGM+ using SWD Debugger Interface



Revision history

Revision	Date	Notes
1.00	Jun. 25, 2020	1st creation
1.01	Mar. 3, 2021	Table 3 Pin description note updated 4.2.4 Clock setting guide updated Table 17, Table 18 Code flash and data flash PGM unit updated
1.03A33M116, A33M114 Datasheet	Dec. 2, 2021	Figure 2, Figure 3 Note added Table 11. Reset Sources of Cold Reset and Warm Reset: warm reset updated
1.03	Jan. 13, 2023	Changed style and font
1.04	Mar. 28, 2023	Added 44 LQFP package information

Korea

Regional Office, Seoul
R&D, Marketing & Sales
8th Fl., 330, Yeongdong-daero,
Gangnam-gu, Seoul,
06177, Korea

Tel: +82-2-2193-2200
Fax: +82-2-508-6903
www.abovsemi.com

HQ, Ochang
R&D, QA, and Test Center
93, Gangni 1-gil, Ochang-eup,
Cheongwon-gun,
Chungcheongbuk-do,
28126, Korea

Tel: +82-43-219-5200
Fax: +82-43-217-3534
www.abovsemi.com

Domestic Sales Manager
Tel: +82-2-2193-2206
Fax: +82-2-508-6903
Email: sales_kr@abov.co.kr

Global Sales Manager
Tel: +82-2-2193-2281
Fax: +82-2-508-6903
Email: sales_gl@abov.co.kr

China Sales Manager
Tel: +86-755-8287-2205
Fax: +86-755-8287-2204
Email: sales_cn@abov.co.kr