

## 32-bit Cortex-M0+ based Touch Sensing Microcontroller

Datasheet Version 1.08

### Introduction

This datasheet contains complete information for application developers who use A31T214/216 series for their specific needs. To meet the requirements for the complexity and high performance in consumer electronics, A31T214/216 incorporates the ARM's high-speed 32-bit Cortex-M0+ Core, and flash memory of up to 256KB and SRAM of 16KB. Building on the very successful Cortex-M0+ processor, the ARM® Cortex®-M0+ retains full instruction set and tool compatibility, while further reducing energy consumption and increasing performance.

In addition, A31T214/216 series includes 16-bit/32-bit timers, Watch timer, 12-bit ADC, CRC generator, USART, I2C, SPI, and DMA. It also has a POR, LVR, LVI, and an internal RC oscillator.

A31T214/216 series supports SLEEP/ POWER DOWN mode to reduce power consumption. It supports operation voltage of 1.8V to 5.5V.

Since A31T214/216 series provides highly flexible and cost effective solutions for many embedded control applications, it can be used for various appliances such as home electronics.

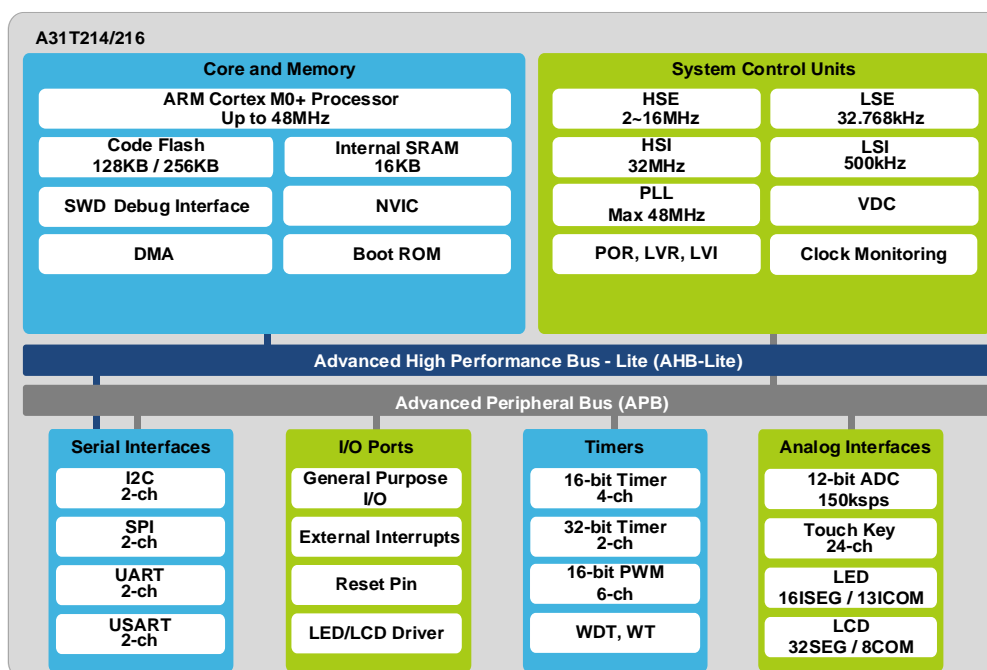


Figure 1. A31T214/216 Block Diagram

### Reference document

- Document 'DDI 0484C' is provided by ARM and contains information of Cortex-M0+.
- A31T214/216 User's manual is provided by ABOV and available at [www.abovsemi.com](http://www.abovsemi.com).

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# 1 Description

A31T214/216 series is a 32-bit touch sensing microcontroller with up to 256Kbytes of flash memory. This powerful microcontroller provides effective solutions to various electrical appliances which require both low power consumption and high performance.

## 1.1 Device overview

In this section, features of A31T214/216 and peripheral counts are introduced.

**Table 1. A31T214/216 Device Features and Peripheral Counts**

Peripherals		Description
Core	CPU	High Performance Low-Power Cortex-M0+ Core 32-bit ARM Cortex-M0+ CPU
	Interrupt	NVIC (Nested-Vectored Interrupt Controller) Up to 32 peripheral interrupts supported.
Memory	Code flash	A31T214: 128Kbytes code flash memory A31T216: 256Kbytes code flash memory
	SRAM	16 Kbytes SRAM
System Control Unit (SCU)	Operating frequency	Up to 48MHz
	Clock	High speed internal oscillator (HSI): 32MHz Low speed internal oscillator (LSI): 500kHz External main oscillator (HSE): 2MHz to 16MHz External sub-oscillator (LSE): 32.768kHz Phase-locked loop (PLL) frequency generator generates a high-speed clock (up to 48MHz)

Table 1. A31T214/216 Device Features and Peripheral Counts (continued)

Peripherals		Description
System Control Unit (SCU)	Clock monitoring	System Fail-Safe function by Clock Monitoring External main oscillator(HSE) External sub oscillator(LSE) Main system clock (MCLK)
	Operating mode	RUN mode SLEEP mode Power-Down mode
	Reset	nRESET pin reset Core reset Software reset POR (Power On Reset) LVR (Low Voltage Reset) WDTR (Watch Dog Timer Reset) Reset due to clock oscillating error
General Purpose I/O (GPIO)		64-Pin: 60-Ports 48-Pin: 44-Ports 44-Pin: 40-Ports 40-Pin: 38-Ports
Direct Memory Access controller (DMA)		4-ch Direct Memory Access (DMA) channels
Watch Timer (WT)		12-bit counter: 1-ch
Watchdog Timer (WDT)		24-bit down counter timer: 1-ch Reset and periodic interrupts are supported
TIMER	Timer1x	16bit: 4-ch Periodic timer mode, One-shot timer mode, PWM pulse mode, Capture mode
	Timer2x	32bit: 2-ch Periodic timer mode, One-shot timer mode, PWM pulse mode, Capture mode
PWM	Timer30	16bit: 6-ch Periodic timer mode, Back-to-Back mode, Capture mode

Table 1. A31T214 and A31T216 Device Features and Peripheral Counts (continued)

Peripherals		Description
Communication function	USART	2-ch
	UART	2-ch
	SPI	2-ch
	I2C	2-ch
ADC		12-bit ADC: 150ksps
Capacitive touch switch		Capacitive Touch Switch 24-ch (64-pin) 24-ch (48-pin) 21-ch (44-pin) 24-ch (40-pin) ESD 4K, CS10V
LED Driver		16SEG / 13COM (64-pin) - T-type Max (13COM X 12SEG), M-type Max (8COM X 8SEG) 16SEG / 13COM (48-pin) - T-type Max (13COM X 12SEG), M-type Max (8COM X 8SEG) 14SEG / 11COM (44-pin) - T-type Max (11COM X 10SEG), M-type Max (7COM X 7SEG) 16SEG / 13COM (40-pin) - T-type Max (13COM X 12SEG), M-type Max (8COM X 8SEG)
LCD Driver		32SEG / 8COM, Max pin [8COM X 27SEG] (64-pin) 20SEG / 6COM, Max pin [6COM X 17SEG] (48-pin) 18SEG / 6COM, Max pin [6COM X 15SEG] (44-pin) 15SEG / 6COM, Max pin [6COM X 12SEG] (40-pin)
CRC calculator (CRC)		CRC-CCITT, CRC-16
Operating voltage		1.8V to 5.5V
Operating temperature		-40°C to +105°C
Package		Four types of package options 64/48/44-LQFP 40-QFN

### 1.2 Block diagram

In Figure 2, A31T214/216 devices with peripherals are described in block diagram.

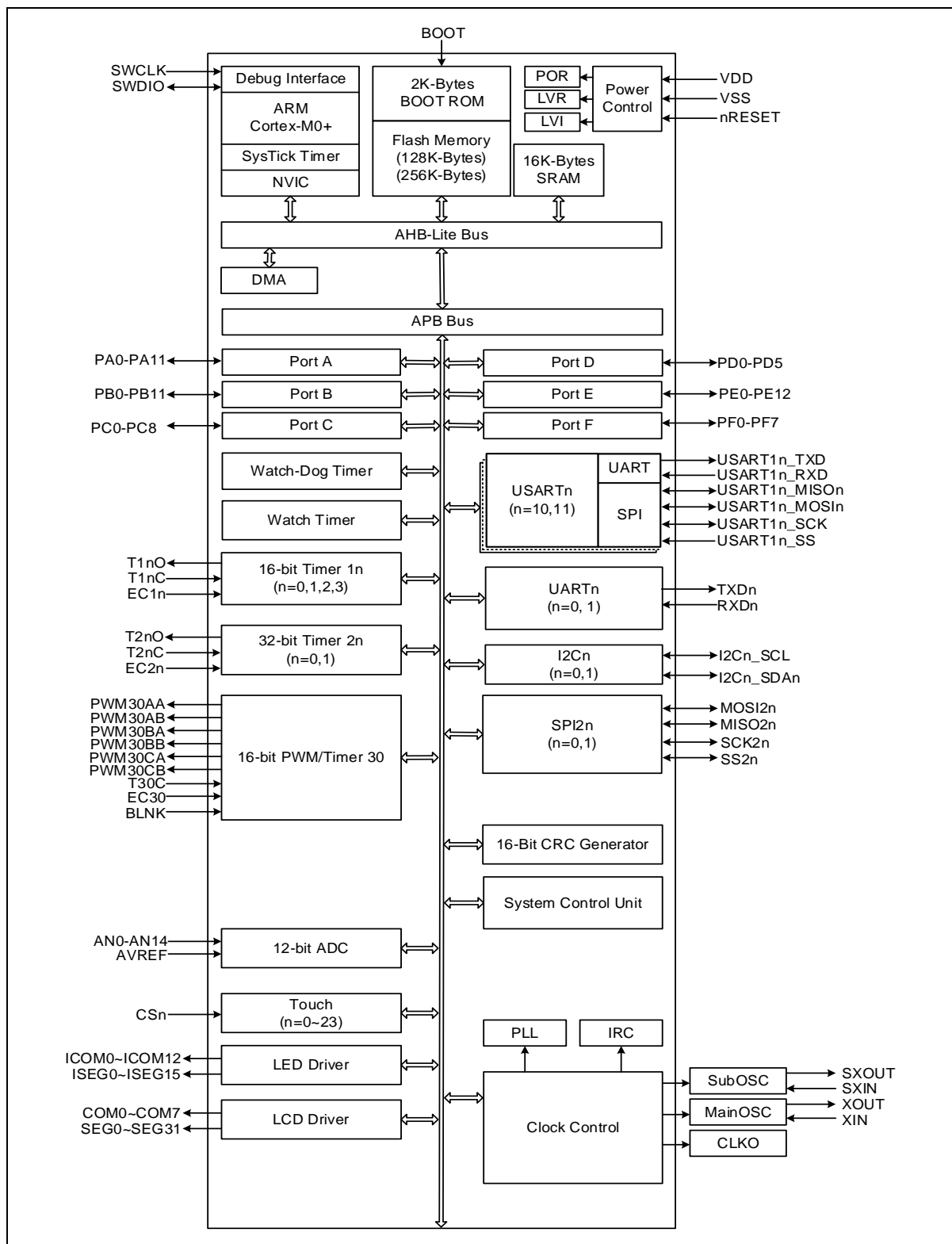


Figure 2. A31T214/216 Block Diagram

## 2 Pinouts and pin descriptions

A31T214/216 devices' pinouts and pin descriptions are introduced in the following sections.

### 2.1 Pinouts

#### 2.1.1 A31T21xRLN (64 LQFP)

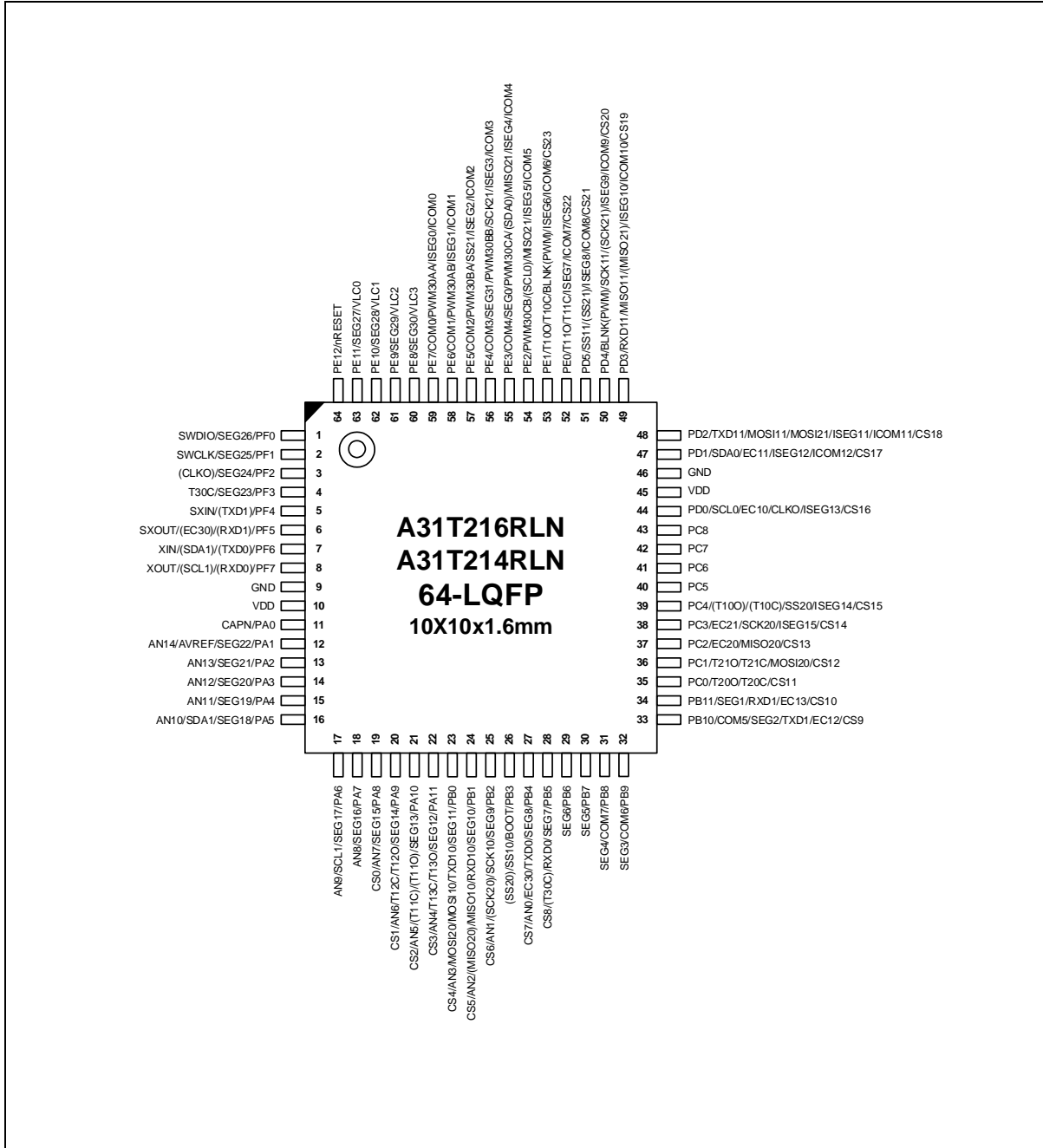


Figure 3. LQFP 64 Pinouts



2.1.3 A31T21xSNN (44 LQFP)

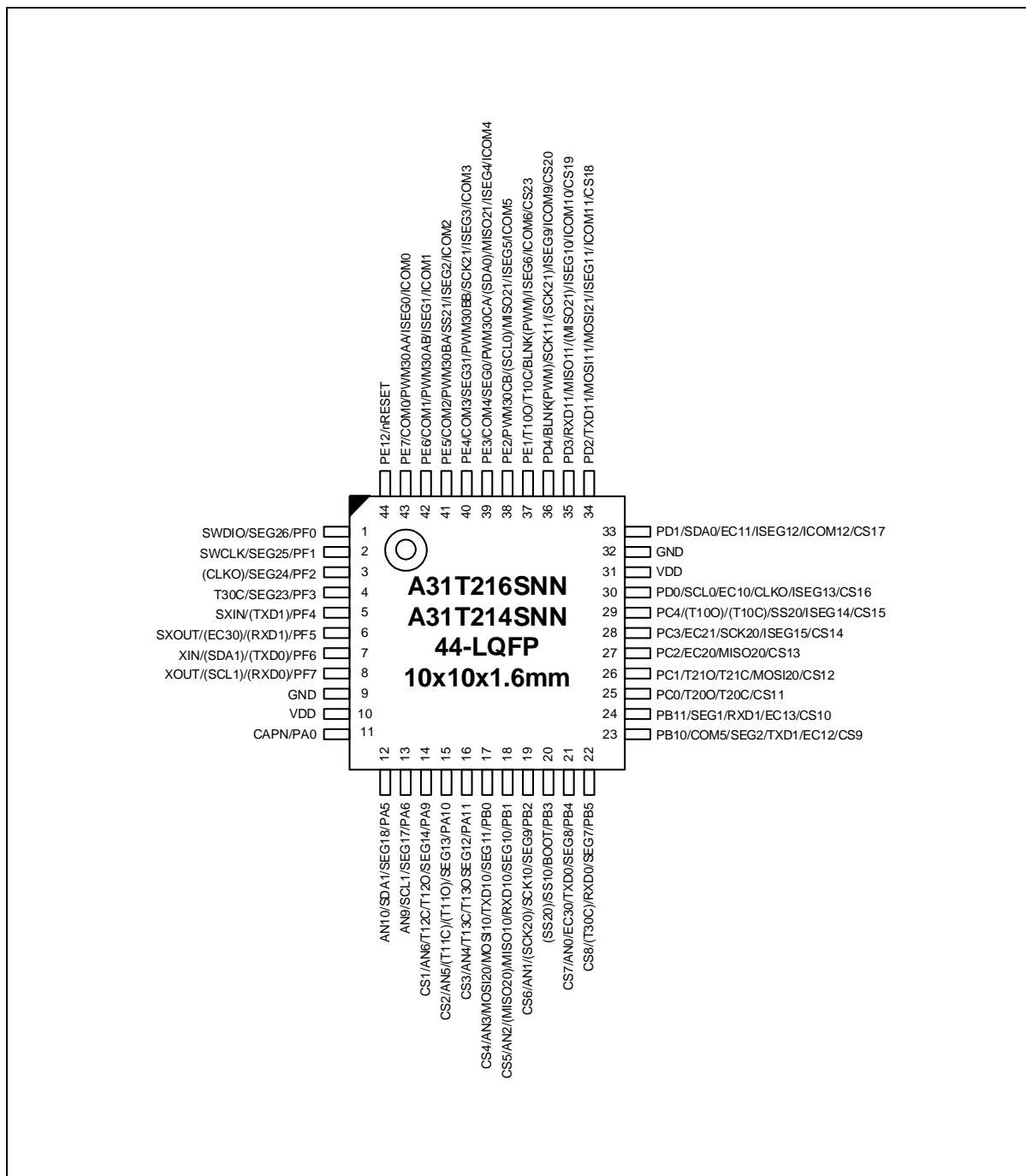


Figure 5. LQFP 44 Pinouts

2.1.4 A31T21xIUN (40 QFN)

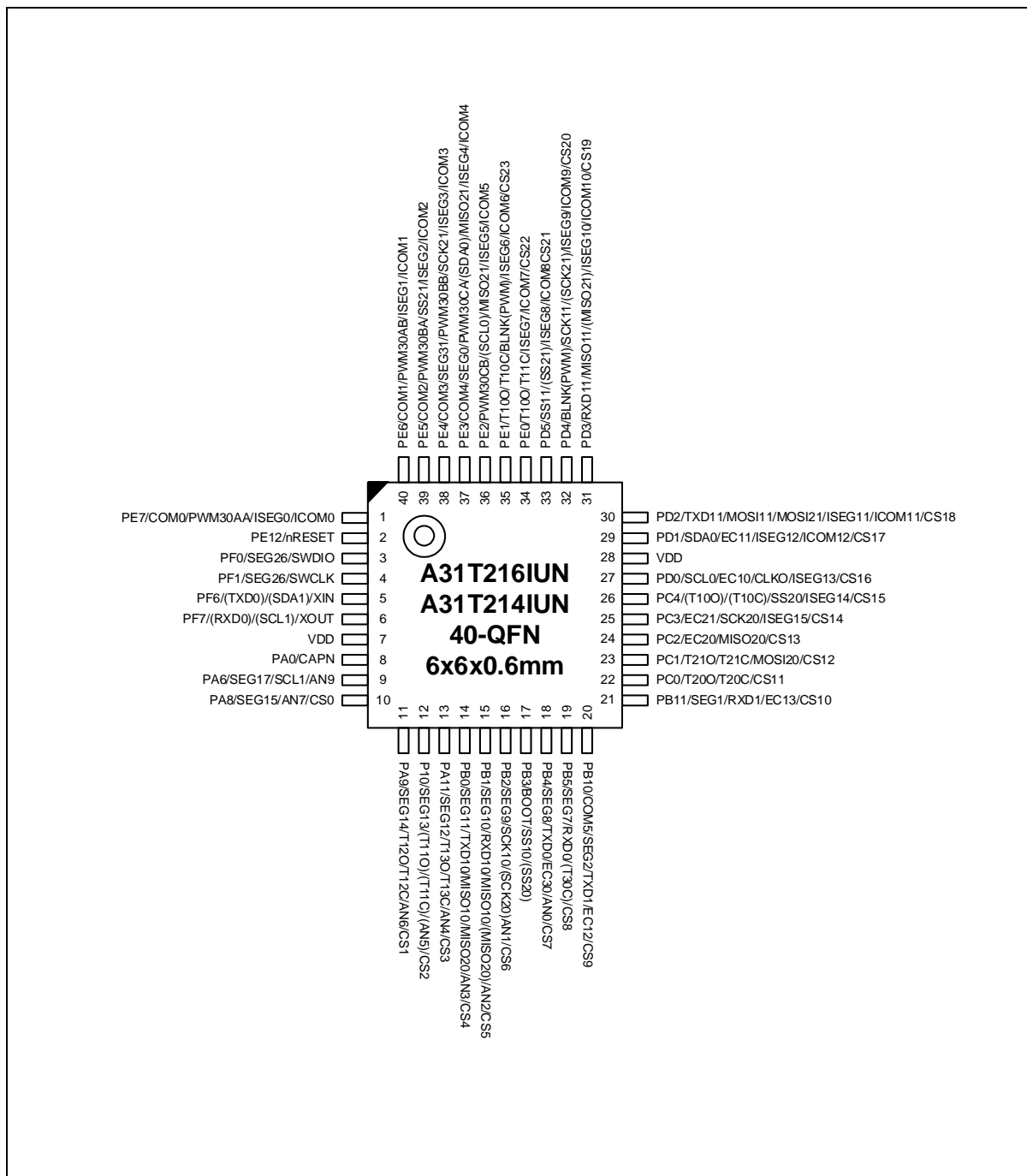


Figure 6. QFN 40 Pinouts



## 2.2 Pin description

Pin configuration information in Table 2 contains two pairs of power/ground and other dedicated pins. These multi-function pins have up to ten selections of functions including GPIO. Configuration including pin ordering can be changed without notice.

**Table 2. Pin Description**

Pin no.				Pin name	Type	Description	Remark
64-pin	48-pin	44-pin	40-pin				
1	1	1	3	PF0	IOUDS	PORT F Bit 0 Input/Output	
				SEG26	O	LCD Segment Signal 26 Output	
				SWDIO*	I/O	SWD Data Input/Output	Pull-Up
2	2	2	4	PF1	IOUDS	PORT F Bit 1 Input/Output	
				SEG25	O	LCD Segment Signal 25 Output	
				SWCLK*	I	SWD Clock Input	Pull-Up
3	3	3	-	PF2*	IOUDS	PORT F Bit 2 Input/Output	
				SEG24	O	LCD Segment Signal 24 Output	
				(CLKO)	O	System Clock Output	
4	4	4	-	PF3*	IOUDS	PORT F Bit 3 Input/Output	
				SEG23	O	LCD Segment Signal 23 Output	
				T30C	I	Timer 30 Clock/Capture Input	
5	5	5	-	PF4*	IOUDS	PORT F Bit 4 Input/Output	
				(TXD1)	O	UART Channel 1 TXD Output	
				SXIN	I	Sub Oscillator Input	
6	6	6	-	PF5*	IOUDS	PORT F Bit 5 Input/Output	
				(RXD1)	I	UART Channel 1 RXD Input	
				(EC30)	I	Timer 30 Event Count Input	
				SXOUT	O	Sub Oscillator Output	
7	7	7	5	PF6*	IOUDS	PORT F Bit 6 Input/Output	
				(TXD0)	O	UART Channel 0 TXD Output	
				(SDA1)	I/O	I2C Channel 1 SDA In/Out	
				XIN	I	Main Oscillator Input	
8	8	8	6	PF7*	IOUDS	PORT F Bit 7 Input/Output	
				(RXD0)	I	UART Channel 0 RXD Input	
				(SCL1)	I/O	I2C Channel 1 SCL In/Out	
				XOUT	O	Main Oscillator Output	
9	9	9	-	GND	P	GND	
10	10	10	7	VDDEXT	P	VDD	
11	11	11	8	PA0*	IOUDS	PORT A Bit 0 Input/Output	
				CAPN	I/O	Modulation Cap	
12	-	-	-	PA1*	IOUDS	PORT A Bit 1 Input/Output	
				SEG22	O	LCD Segment Signal 22 Output	
				AN14/ AVREF	IA	Analog Input 14 A/D Converter Reference Input	

Table 2. Pin Description (continued)

Pin no.				Pin name	Type	Description	Remark
64-pin	48-pin	44-pin	40-pin				
13	-	-	-	PA2*	IOUDS	PORT A Bit 2 Input/Output	
				SEG21	O	LCD Segment Signal 21 Output	
				AN13	IA	Analog Input 13	
14	-	-	-	PA3*	IOUDS	PORT A Bit 3 Input/Output	
				SEG20	O	LCD Segment Signal 20 Output	
				AN12	IA	Analog Input 12	
15	-	-	-	PA4*	IOUDS	PORT A Bit 4 Input/Output	
				SEG19	O	LCD Segment Signal 19 Output	
				AN11	IA	Analog Input 11	
16	12	12	-	PA5*	IOUDS	PORT A Bit 5 Input/Output	
				SEG18	O	LCD Segment Signal 18 Output	
				SDA1	I/O	I2C Channel 1 SDA In/Out	
				AN10	IA	Analog Input 10	
17	13	13	9	PA6*	IOUDS	PORT A Bit 6 Input/Output	
				SEG17	O	LCD Segment Signal 17 Output	
				SCL1	I/O	I2C Channel 1 SCL In/Out	
				AN9	IA	Analog Input 9	
18	14	-	-	PA7*	IOUDS	PORT A Bit 7 Input/Output	
				SEG16	O	LCD Segment Signal 16 Output	
				AN8	IA	Analog Input 8	
19	15	-	10	PA8*	IOUDS	PORT A Bit 8 Input/Output	
				SEG15	O	LCD Segment Signal 15 Output	
				AN7	IA	Analog Input 7	
				CS0	IA	Capacitive Touch Switch Input 0	
20	16	14	11	PA9*	IOUDS	PORT A Bit 9 Input/Output	
				SEG14	O	LCD Segment Signal 14 Output	
				T12O	O	Timer 12 Output	
				T12C	I	Timer 12 Capture Input	
				AN6	IA	Analog Input 6	
				CS1	IA	Capacitive Touch Switch Input 1	
21	17	15	12	PA10*	IOUDS	PORT A Bit 10 Input/Output	
				SEG13	O	LCD Segment Signal 13 Output	
				(T11O)	O	Timer 11 Output	
				(T11C)	I	Timer 11 Capture Input	
				AN5	IA	Analog Input 5	
				CS2	IA	Capacitive Touch Switch Input 2	
22	18	16	13	PA11*	IOUDS	PORT A Bit 11 Input/Output	
				SEG12	O	LCD Segment Signal 12 Output	
				T13O	O	Timer 13 Output	
				T13C	I	Timer 13 Capture Input	
				AN4	IA	Analog Input 4	
				CS3	IA	Capacitive Touch Switch Input 3	

Table 2. Pin Description (continued)

Pin no.				Pin name	Type	Description	Remark
64-pin	48-pin	44-pin	40-pin				
23	19	17	14	PB0*	IOUDS	PORT B Bit 0 Input/Output	
				SEG11	O	LCD Segment Signal 11 Output	
				TXD10	O	UART Channel 10 TXD Output	
				MOSI10	I/O	SPI Channel 10 Master Out/Slave In	
				(MOSI20)	I/O	SPI Channel 20 Master Out/Slave In	
				AN3	IA	Analog Input 3	
24	20	18	15	PB1*	IOUDS	PORT B Bit 1 Input/Output	Input
				SEG10	O	LCD Segment Signal 10 Output	
				RXD10	I	UART Channel 10 RXD Input	
				MISO10	I/O	SPI Channel 10 Master In/Slave Out	
				(MISO20)	I/O	SPI Channel 20 Master In/Slave Out	
				AN2	IA	Analog Input 9	
25	21	19	16	PB2*	IOUDS	PORT B Bit 2 Input/Output	
				SEG9	O	LCD Segment Signal 9 Output	
				SCK10	I/O	SPI10 Data Clock Input/Output	
				(SCK20)	I/O	SPI20 Data Clock Input/Output	
				AN1	IA	Analog Input 1	
				CS6	IA	Capacitive Touch Switch Input 6	
26	22	20	17	PB3	IOUDS	PORT B Bit 3 Input/Output	
				BOOT*	I	Boot mode selection Input	Pull-Up
				SS10	I/O	SPI Channel 10 Slave Select signal	
				(SS20)	I/O	SPI Channel 20 Slave Select signal	
27	23	21	18	PB4*	IOUDS	PORT B Bit 4 Input/Output	
				SEG8	O	LCD Segment Signal 8 Output	
				TXD0	O	UART Channel 0 TXD Output	
				EC30	I	Timer 30 Event Count Input	
				AN0	IA	Analog Input 0	
				CS7	IA	Capacitive Touch Switch Input 7	
28	24	22	19	PB5*	IOUDS	PORT B Bit 5 Input/Output	
				SEG7	O	LCD Segment Signal 7 Output	
				RXD0	I	UART Channel 0 RXD Input	
				(T30C)	I	Timer 30 Capture Input	
				CS8	IA	Capacitive Touch Switch Input 8	
29	-	-	-	PB6*	IOUDS	PORT B Bit 6 Input/Output	
				SEG6	O	LCD Segment Signal 6 Output	
30	-	-	-	PB7*	IOUDS	PORT B Bit 7 Input/Output	
				SEG5	O	LCD Segment Signal 5 Output	
31	-	-	-	PB8*	IOUDS	PORT B Bit 8 Input/Output	
				COM7/	O	LCD Common Signal 7 Output	
				SEG4	O	LCD Segment Signal 4 Output	

Table 2. Pin Description (continued)

Pin no.				Pin name	Type	Description	Remark
64-pin	48-pin	44-pin	40-pin				
32	-	-	-	PB9*	IOUDS	PORT B Bit 9 Input/Output	
				COM6/ SEG3	O	LCD Common Signal 6 Output LCD Segment Signal 3 Output	
33	25	23	20	PB10*	IOUDS	PORT B Bit 10 Input/Output	
				COM5/ SEG2	O	LCD Common Signal 5 Output LCD Segment Signal 2 Output	
				TXD1	O	UART Channel 1 TXD Output	
				EC12	I	Timer 12 Event Count Input	
34	26	24	21	CS9	IA	Capacitive Touch Switch Input 9	
				PB11*	IOUDS	PORT B Bit 11 Input/Output	
				SEG1	O	LCD Segment Signal 1 Output	
				RXD1	I	UART Channel 1 RXD Input	
				EC13	I	Timer 13 Event Count Input	
35	27	25	22	CS10	IA	Capacitive Touch Switch Input 10	
				PC0*	IOUDS	PORT C Bit 0 Input/Output	
				T20O	O	Timer 20 Output	
				T20C	I	Timer 20 Capture Input	
36	28	26	23	CS11	IA	Capacitive Touch Switch Input 11	
				PC1*	IOUDS	PORT C Bit 1 Input/Output	
				T21O	O	Timer 21 Output	
				T21C	I	Timer 21 Capture Input	
				MOSI20	I/O	SPI Channel 20 Master Out/Slave In	
37	29	27	24	CS12	IA	Capacitive Touch Switch Input 12	
				PC2*	IOUDS	PORT C Bit 2 Input/Output	
				EC20	I	Timer 20 Event Count Input	
				MISO20	I/O	SPI Channel 20 Master In/Slave Out	
38	30	28	25	CS13	IA	Capacitive Touch Switch Input 13	
				PC3*	IOUDS	PORT C Bit 3 Input/Output	
				EC21	I	Timer 21 Event Count Input	
				SCK20	I/O	SPI20 Data Clock Input/Output	
39	31	29	26	ISEG15/ CS14	O IA	LED Segment Signal 15 Output Capacitive Touch Switch Input 14	
				PC4*	IOUDS	PORT C Bit 4 Input/Output	
				(T10O)	O	Timer 10 Output	
				(T10C)	I	Timer 10 Capture Input	
				SS20	I/O	SPI Channel 20 Slave Select signal	
40	-	-	-	ISEG14/ CS15	O IA	LED Segment Signal 14 Output Capacitive Touch Switch Input 15	
41	-	-	-	PC5*	IOUDS	PORT C Bit 5 Input/Output	
42	-	-	-	PC6*	IOUDS	PORT C Bit 6 Input/Output	
43	-	-	-	PC7*	IOUDS	PORT C Bit 7 Input/Output	
				PC8*	IOUDS	PORT C Bit 8 Input/Output	

Table 2. Pin Description (continued)

Pin no.				Pin name	Type	Description	Remark
64-pin	48-pin	44-pin	40-pin				
44	32	30	27	PD0*	IOUDS	PORT D Bit 0 Input/Output	Input Pull-Up
				SCL0	I/O	I2C Channel 0 SCL In/Out	
				EC10	I	Timer 10 Event Count Input	
				CLKO	O	System Clock Output	
				ISEG13/ CS16	O IA	LED Segment Signal 13 Output Capacitive Touch Switch Input 16	
45	33	31	28	VDDEXT	P	VDD	
46	34	32	-	GND	P	GND	
47	35	33	29	PD1*	IOUDS	PORT D Bit 1 Input/Output	Input Pull-Up
				SDA0	I/O	I2C Channel 0 SDA In/Out	
				EC11	I	Timer 11 Event Count Input	
				ISEG12/ ICOM12/ CS17	O O IA	LED Segment Signal 12 Output LED Common Signal 12 Output Capacitive Touch Switch Input 17	
				48	36	34	30
48	36	34	30	TXD11	O	UART Channel 11 TXD Output	
				MOSI11	I/O	SPI Channel 11 Master Out/Slave In	
				(MOSI21)	I/O	SPI Channel 21 Master Out/Slave In	
				ISEG11/ ICOM11/ CS18	O O IA	LED Segment Signal 11 Output LED Common Signal 11 Output Capacitive Touch Switch Input 18	
				49	37	35	31
49	37	35	31	RXD11	I	UART Channel 11 RXD Input	
				MISO11	I/O	SPI Channel 11 Master In/Slave Out	
				(MISO21)	I/O	SPI Channel 21 Master In/Slave Out	
				ISEG10/ ICOM10/ CS19	O O IA	LED Segment Signal 10 Output LED Common Signal 10 Output Capacitive Touch Switch Input 19	
				50	38	36	32
50	38	36	32	BLNK(PW M)	I	External Sync Signal Input for T30 PWM	
				SCK11	I/O	SPI11 Data Clock Input/Output	
				(SCK21)	I/O	SPI21 Data Clock Input/Output	
				ISEG9/ ICOM9/ CS20	O O IA	LED Segment Signal 9 Output LED Common Signal 9 Output Capacitive Touch Switch Input 20	
				51	39	-	33
51	39	-	33	SS11	I/O	SPI Channel 11 Slave Select signal	
				(SS21)	I/O	SPI Channel 21 Slave Select signal	
				ISEG8/ CS20	O	LED Segment Signal 8 Output	

Table 2. Pin Description (continued)

Pin no.				Pin name	Type	Description	Remark
64-pin	48-pin	44-pin	40-pin				
				ICOM8/ CS21	O IA	LED Common Signal 8 Output Capacitive Touch Switch Input 21	
52	40	-	34	PE0*	IOUDS	PORT E Bit 0 Input/Output	
				T11O	O	Timer 11 Output	
				T11C	I	Timer 11 Clock/Capture Input	
				ISEG7/ ICOM7/ CS22	O O IA	LED Segment Signal 7 Output LED Common Signal 7 Output Capacitive Touch Switch Input 22	
53	41	37	35	PE1*	IOUDS	PORT E Bit 1 Input/Output	
				T10O	O	Timer 10 Output	
				T10C	I	Timer 10 Capture Input	
				BLNK(PW M)	I	External Sync Signal Input for T30 PWM	
				ISEG6/ ICOM6/ CS23	O O IA	LED Segment Signal 6 Output LED Common Signal 6 Output Capacitive Touch Switch Input 23	
54	42	38	36	PE2*	IOUDS	PORT E Bit 2 Input/Output	
				PWM30CB	O	Timer 30 PWM Output	
				(SCL0)	I/O	I2C Channel 0 SCL In/Out	
				MOSI21	I/O	SPI Channel 21 Master Out/Slave In	
				ISEG5/ ICOM5	O	LED Segment Signal 5 Output LED Common Signal 5 Output	
55	43	39	37	PE3*	IOUDS	PORT E Bit 3 Input/Output	
				COM4/ SEG0	O	LCD Common Signal 4 Output LCD Segment Signal 0 Output	
				PWM30CA	O	Timer 30 PWM Output	
				(SDA0)	I/O	I2C Channel 0 SDA In/Out	
				MISO21	I/O	SPI Channel 21 Master In/Slave Out	
				ISEG4/ ICOM4	O	LED Segment Signal 4 Output LED Common Signal 4 Output	
56	44	40	38	PE4*	IOUDS	PORT E Bit 4 Input/Output	
				COM3/ SEG31	O	LCD Common Signal 3 Output LCD Segment Signal 31 Output	
				PWM30BB	O	Timer 30 PWM Output	
				SCK21	I/O	SPI21 Data Clock Input/Output	
				ISEG3/ ICOM3	O	LED Segment Signal 3 Output LED Common Signal 3 Output	
57	45	41	39	PE5*	IOUDS	PORT E Bit 5 Input/Output	
				COM2	O	LCD Common Signal 2 Output	
				PWM30BA	O	Timer 30 PWM Output	
				SS21	I/O	SPI Channel 21 Slave Select signal	
				ISEG2/ ICOM2	O	LED Segment Signal 2 Output	

Table 2. Pin Description (continued)

Pin no.				Pin name	Type	Description	Remark
64-pin	48-pin	44-pin	40-pin				
				ICOM2		LED Common Signal 2 Output	
58	46	42	40	PE6*	IOUDS	PORT E Bit 6 Input/Output	
				COM1	O	LCD Common Signal 1 Output	
				PWM30AB	O	Timer 30 PWM Output	
				ISEG1/ ICOM1	O	LED Segment Signal 1 Output LED Common Signal 1 Output	
59	47	43	1	PE7*	IOUDS	PORT E Bit 7 Input/Output	
				COM0	O	LCD Common Signal 0 Output	
				PWM30AA	O	Timer 30 PWM Output	
				ISEG0/ ICOM0	O	LED Segment Signal 0 Output LED Common Signal 0 Output	
60	-	-	-	PE8*	IOUDS	PORT E Bit 8 Input/Output	
				SEG30	O	LCD Segment Signal 30 Output	
				VLC3	IA	External LCD Voltage bias 3	
61	-	-	-	PE9*	IOUDS	PORT E Bit 9 Input/Output	
				SEG29	O	LCD Segment Signal 29 Output	
				VLC2	IA	External LCD Voltage bias 2	
62	-	-	-	PE10*	IOUDS	PORT E Bit 10 Input/Output	
				SEG28	O	LCD Segment Signal 28 Output	
				VLC1	IA	External LCD Voltage bias 1	
63	-	-	-	PE11*	IOUDS	PORT E Bit 11 Input/Output	
				SEG27	O	LCD Segment Signal 27 Output	
				VLC0	IA	External LCD Voltage bias 0	
64	48	44	2	PE12	IOUDS	PORT E Bit 12 Input/Output	
				nRESET*	IU	External Reset Input	Pull-Up

**NOTES:**

1. I=Input, O=Output, U=Pull-up, D=Pull-down, S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
2. The \* means 'selected pin function after reset condition'.
3. Pin order may be changed with revision notice.

## 3 System and memory overview

### 3.1 System architecture

Main system of A31T214/216 series consists of the followings:

- ARM<sup>®</sup> Cortex<sup>®</sup>-M0+ core
- General purpose DMA
- Internal SRAM
- Internal Flash memory

#### 3.1.1 Cortex-M0+ core

The ARM<sup>®</sup> Cortex<sup>®</sup>-M0+ processor is the most energy-efficient ARM processor available. It builds on the very successful Cortex-M0+ processor, retaining full instruction set and tool compatibility, while further reducing energy consumption and increasing performance. Document “DDI 0484C” from ARM provides detail information of Cortex-M0+.



## 3.1.2 Interrupt controller

Table 3. Interrupt Vector Map

Priority	Vector address	Interrupt source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Address
-14	0x0000_0008	NMI Handler
-13	0x0000_000C	Hard Fault Handler
-12	0x0000_0010	Reserved
-11	0x0000_0014	
-10	0x0000_0018	
-9	0x0000_001C	
-8	0x0000_0020	
-7	0x0000_0024	
-6	0x0000_0028	
-5	0x0000_002C	
-4	0x0000_0030	Reserved
-3	0x0000_0034	
-2	0x0000_0038	PenSV Handler
-1	0x0000_003C	SysTick Handler
0	0x0000_0040	LVI
1	0x0000_0044	SYSClkFAIL
2	0x0000_0048	WDT
3	0x0000_004C	GPIOA, GPIOB
4	0x0000_0050	GPIOC, GPIOD
5	0x0000_0054	GPIOE
6	0x0000_0058	GPIOF
7	0x0000_005C	TIMER10
8	0x0000_0060	TIMER11
9	0x0000_0064	TIMER12
10	0x0000_0068	I2C0
11	0x0000_006C	USART10
12	0x0000_0070	WT
13	0x0000_0074	TIMER30
14	0x0000_0078	I2C1
15	0x0000_007C	TIMER20
16	0x0000_0080	TIMER21

Table 3. Interrupt Vector Map (continued)

Priority	Vector address	Interrupt source
17	0x0000_0084	USART11
18	0x0000_0088	ADC
19	0x0000_008C	UART0
20	0x0000_0090	UART1
21	0x0000_0094	TIMER13
22	0x0000_0098	Reserved
23	0x0000_009C	Reserved
24	0x0000_00A0	Reserved
25	0x0000_00A4	SPI20
26	0x0000_00A8	SPI21
27	0x0000_00AC	Reserved
28	0x0000_00B0	LED
29	0x0000_00B4	TOUCH
30	0x0000_00B8	Reserved
31	0x0000_00BC	CRC

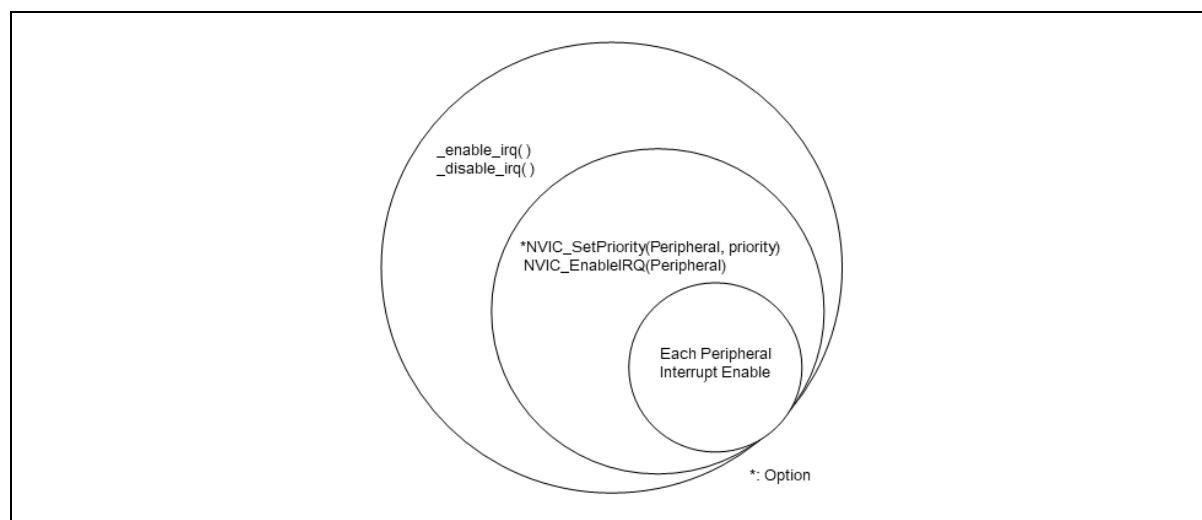
**NOTES:**

- Each interrupt has an associated priority-level register. Each of them is 2 bits wide, occupying the two MSBs of the Interrupt Priority Level Registers. Each Interrupt Priority Level Register occupies 1 byte (8 bits). NVIC registers in the Cortex-M0+ processor can only be accessed using word-size transfers, so for each access, four Interrupt Priority Level Registers are accessed at the same time.

\*\* \_\_NVIC\_PRIO\_BITS = 2

- Figure 7 is a caution when using Peripheral Interrupts. Interrupt don't work if only peripheral interrupts are enabled. Enable the function in core to enable interrupt.

\* \_\_enable\_irq > NVIC\_EnableIRQ(Peripheral) > Each Peripheral Interrupt

**Figure 7. Interrupt Block Diagram**

## 3.2 Memory organization

Program memory, data memory, registers and I/O ports are organized in the same address space.

### 3.2.1 Register boundary address

Table 4 gives the boundary addresses of peripherals in A31T214/216 series.

**Table 4. A31T214/216 Memory Boundary Addresses**

Boundary address	Memory area	Register description
0x4000_0000	SCU	
0x4000_5100	LVI/LVR	
0x4000_1000/1100/1200/1300/1400/1500	PCU A/B/C/D/E/F	
0x4000_0100	Flash controller	
0x2000_0000	Internal SRAM	
0x4000_0400/0410/0420/0430	DMACH0/1/2/3	
0x4000_1A00	WDT	
0x4000_2000	WT	
0x4000_2100/2200/2300/2700	Timer 10/11/12/13	
0x4000_2500/2600	Timer 20/21	
0x4000_2400	Timer 30	
0x4000_3800/3900	USART 10/11	
0x4000_4000/4100	UART 0/1	
0x4000_4800/4900	I2C 0/1	
0x4000_4C00/4D00	SPI 20/21	
0x4000_3000	12-bit ADC	
0x4000_3600	TOUCH	
0x4000_5000	LCD	
0x4000_6000	LED	
0x4000_0300	CRC	

3.2.2 Memory map

Figure 8 shows addressable memory space in memory map.

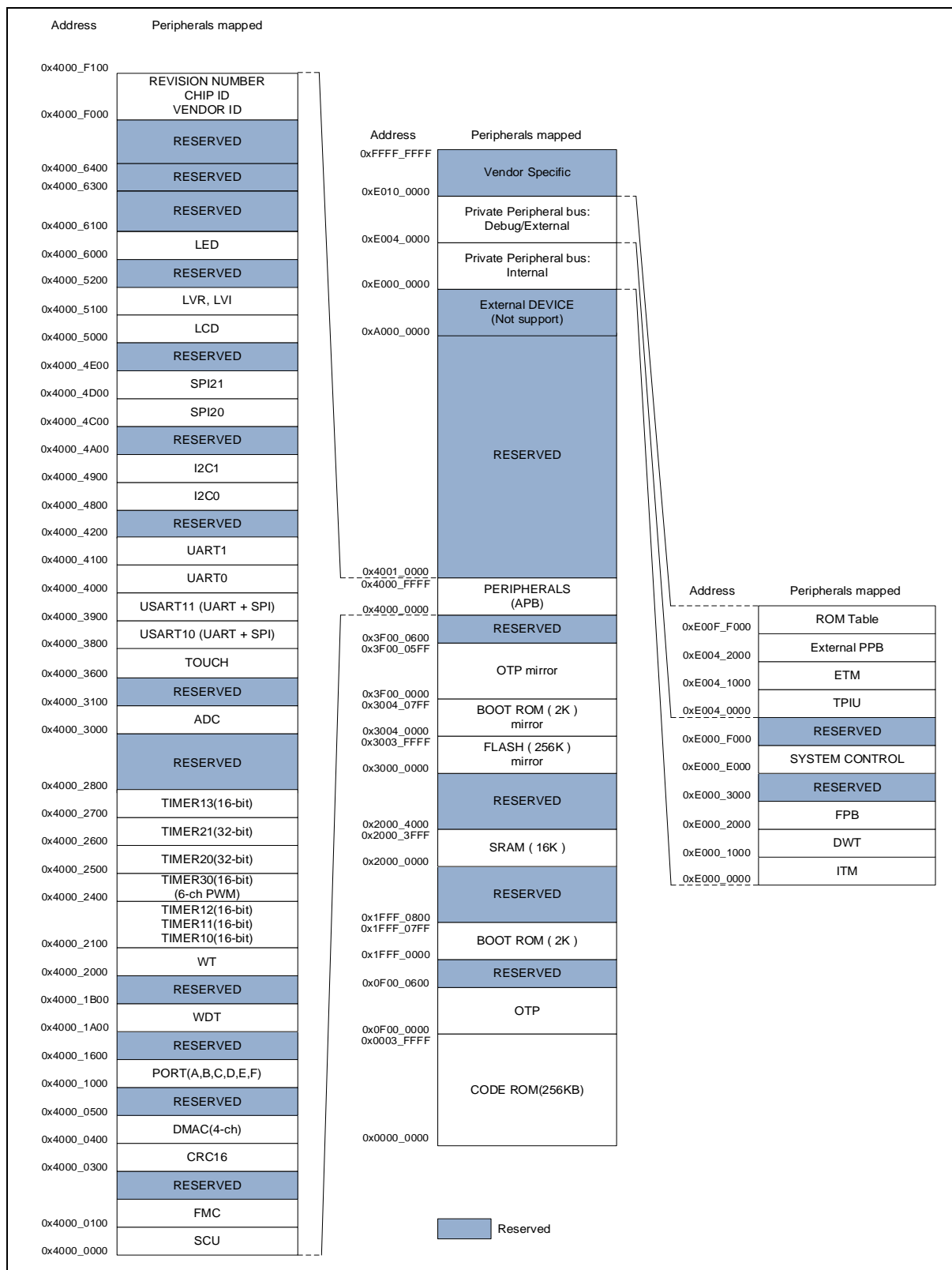


Figure 8. Memory Map (A31T216)

### 3.2.3 Embedded SRAM

A31T214/216 series has a block of 0-wait on-chip SRAM, and 0x2000\_0000 is base address of the 16KB SRAM. SRAM memory area is usually used for data memory and stack memory. Sometimes the code is dumped into the SRAM memory for fast operation or flash erase/programming operation. This device does not support memory remap strategy. So jump and return are required to perform the code in SRAM memory area.

### 3.2.4 Flash memory overview

A31T214/216 series provides internal 128KB/256KB code flash memory and its controller. This is enough to control the general system. Self-programming is available and ISP and SWD programming is also supported in boot or debugging mode.

Instruction and data cache buffer are present and overcome the low bandwidth flash memory. CPU can access flash memory with one wait state up to 20MHz bus frequency.

### 3.2.5 Boot mode

#### Boot mode pins

A31T214/216 series has a boot mode option to program internal flash memory. Boot mode can be entered by setting BOOT pin to 'L' at reset timing (Normal state is 'H').

Boot mode supports UART boot:

- UART boot uses USART10\_TXD/USART10\_RXD port.

The pins for boot mode are listed in Table 5.

**Table 5. Boot Mode Pin List**

Block	Pin name	Dir.	Description
SYSTEM	nRESET	I	Reset Input signal
	nBOOT / PB3	I	'Low' to enter Boot mode
UART mode of USART10	USART10_RXD / PB1	I	USART10 Boot Receive Data
	USART10_TXD / PB0	O	USART10 Boot Transmit Data

**Boot mode connections**

User can design a target board using any of boot mode ports such as UART mode of USART10. Sample connection diagrams of boot mode are introduced in the following figures:

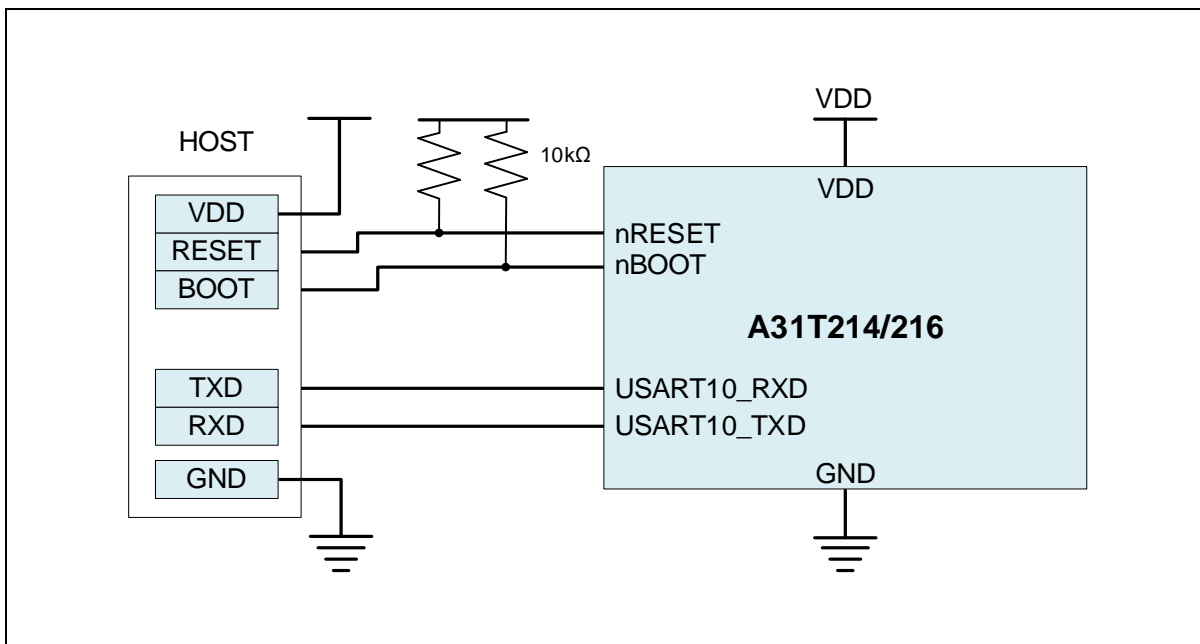


Figure 9. Connection Diagram of UART10 Boot

**SWD mode connections**

A user can use SWD mode for writing with E-PGM+. This mode can be used for writing & debugging.

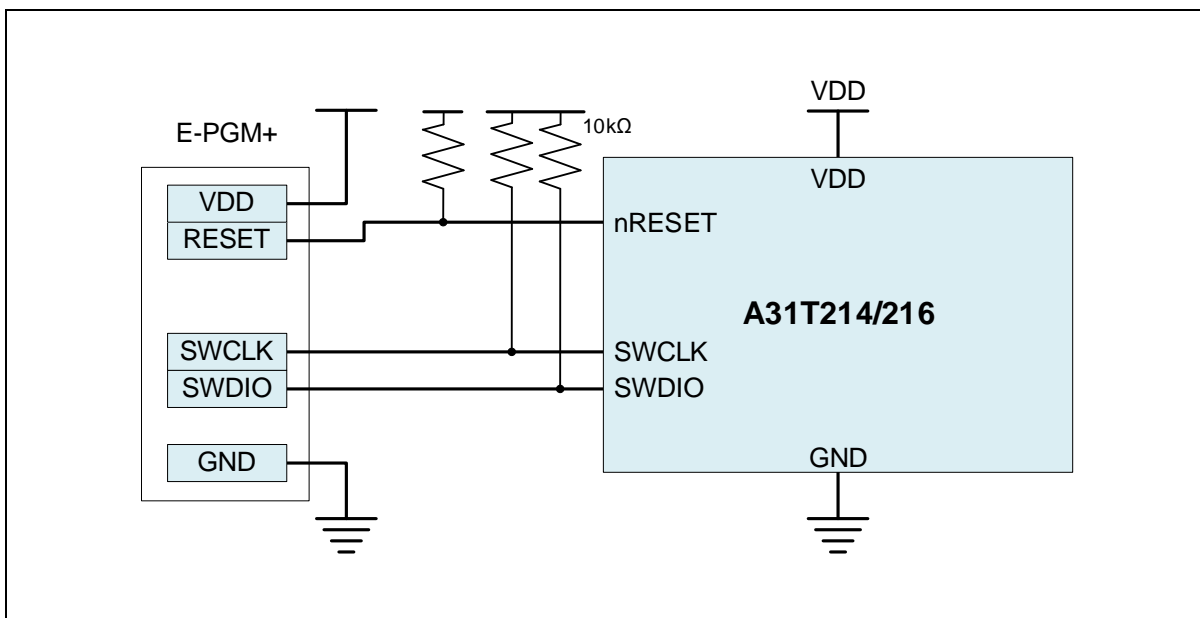


Figure 10. Connection Diagram of E-PGM+ and SWD Port

## 4 System Control Unit (SCU)

A31T214/216 series has a built-in intelligent power control block which manages system analog blocks and operating modes. System Control Unit (SCU) block controls an internal reset and clock signals to maintain optimize system performance and power dissipation.

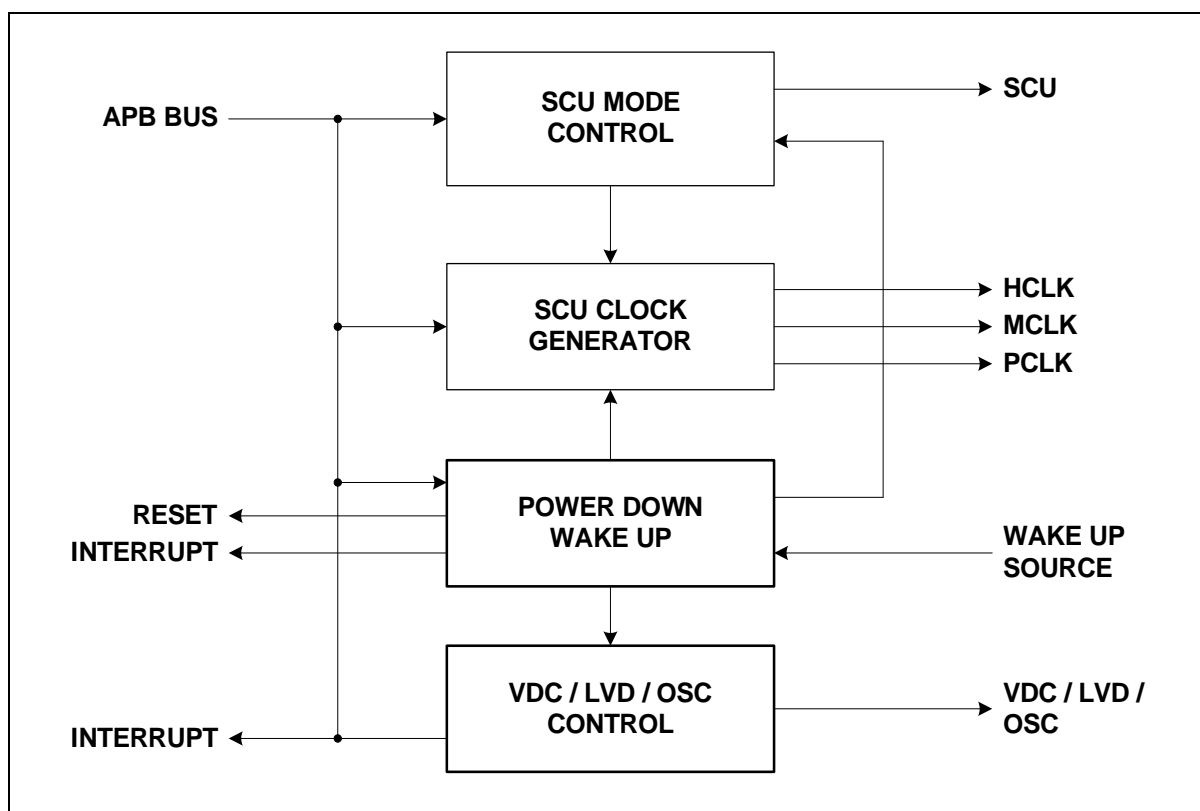
Four pins in Table 6 are assigned for the SCU block.

**Table 6. SCU Pins**

Pin name	Type	Description
nRESET	I	External Reset Input
XIN/XOUT	OSC	External Crystal Oscillator
SXIN/SXOUT	OSC	External sub-Crystal Oscillator
CLKO	O	Clock Output Monitoring Signal

### 4.1 SCU block diagram

In this section, SCU block diagram is introduced in Figure 11.



**Figure 11. SCU Block Diagram**

### 4.2 Clock system

A31T214/216 series has two main operating clocks. One is HCLK which produces a clock signal both for CPU and AHB bus system. The other is PCLK which produces a clock signal for peripheral systems.

A user can keep the clock system variation under software control. Through Figure 12 and Table 7, users learn about the clock system of A31T214/216 devices and clock sources.

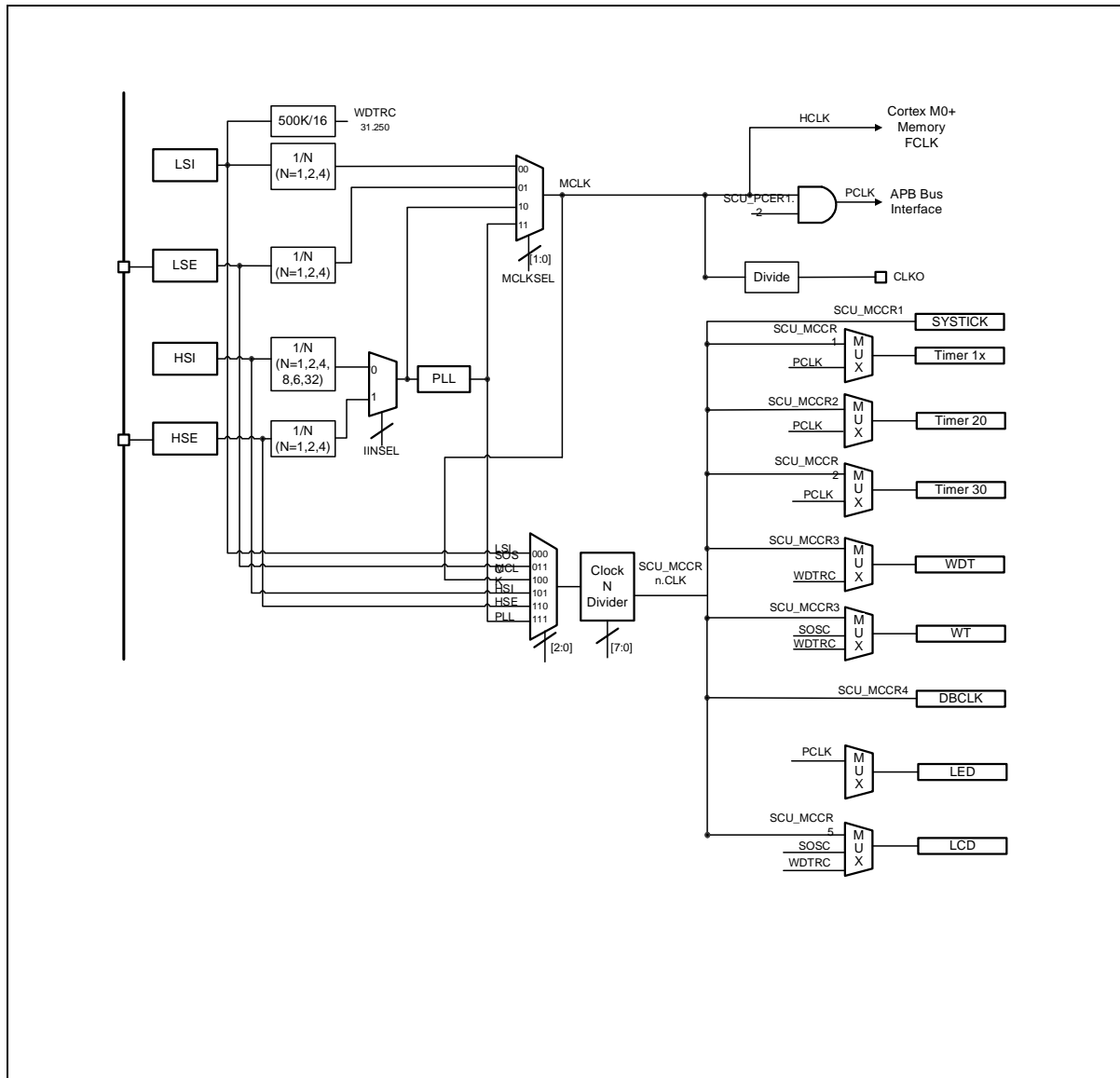


Figure 12. Clock Tree Configuration



All multiplexers switching clock sources have a glitch-free circuit in each. So a clock can be switched without glitch risks. When a user tries to change a clock mux control, both of clock sources must be alive. If one of them is not alive, clock change operation is stopped and system will be halted and not be recovered.

**Table 7. Clock Sources**

<b>Clock name</b>	<b>Frequency</b>	<b>Description</b>
HSE	2-16MHz	High Speed External Oscillator
LSE	32.768kHz	Low Speed External Oscillator
HSI	32MHz	High Speed Internal OSC
LSI	500kHz	Low Speed Internal OSC

#### 4.2.1 HCLK clock domain

HCLK clock feeds the clock to the CPU and the AHB bus. Cortex-M0+ CPU requires 2 clocks related with FCLK and HCLK. FCLK is free running clock and it is always running except in power down mode. HCLK can be stopped in SLEEP mode and power down mode.

BUS system and memory systems are operated by MCLK clock. Maximum bus operating clock speed is 48MHz.

#### 4.2.2 PCLK clock domain

PCLK is the master clock of all peripherals. Each peripheral clock is enabled by SCU\_PCER1, and SCU\_PCER2 registers can be used by each peripheral. Before enabling the PCLK input clock of each block, it can't be accessible even reading its registers. It can be stopped in power down mode.

#### 4.2.3 Clock configuration procedure

After powering up, the default system clock is fed by LSI (500kHz) clock. By default LSI is enabled at power up sequence. The other clock sources will be enabled by user controls with the LSI system clock.

HSI (32MHz) clock can be enabled by SCU\_CSCR register.

HSE (2-16MHz) clock can be enabled by SCU\_CSCR register. Prior to enable the HSE block, the pin mux configuration should be set for XIN, XOUT function. PF6 and PF7 pins are shared with HSE's XIN and XOUT function – PF\_MOD and PF\_AFSR1 registers should be configured properly. After enabling the HSE block, you must wait for more than 5ms time to ensure stable operation of crystal oscillation.

LSE (32.768kHz) clock can be enabled by SCU\_CSCR register. Prior to enable the LSE block, the pin mux configuration should be set for SXIN, SXOUT function. PF4 and PF5 pins are shared with LSE's SXIN and SXOUT function – PF\_MOD and PF\_AFSR1 registers should be configured properly.

After enabling the LSE block, you must wait for more than 10ms time to ensure stable operation of crystal oscillation. You can change an MCLK by using the SCU\_SCCR register.

You can find an example flow chart configuring the system clock in Figure 13.

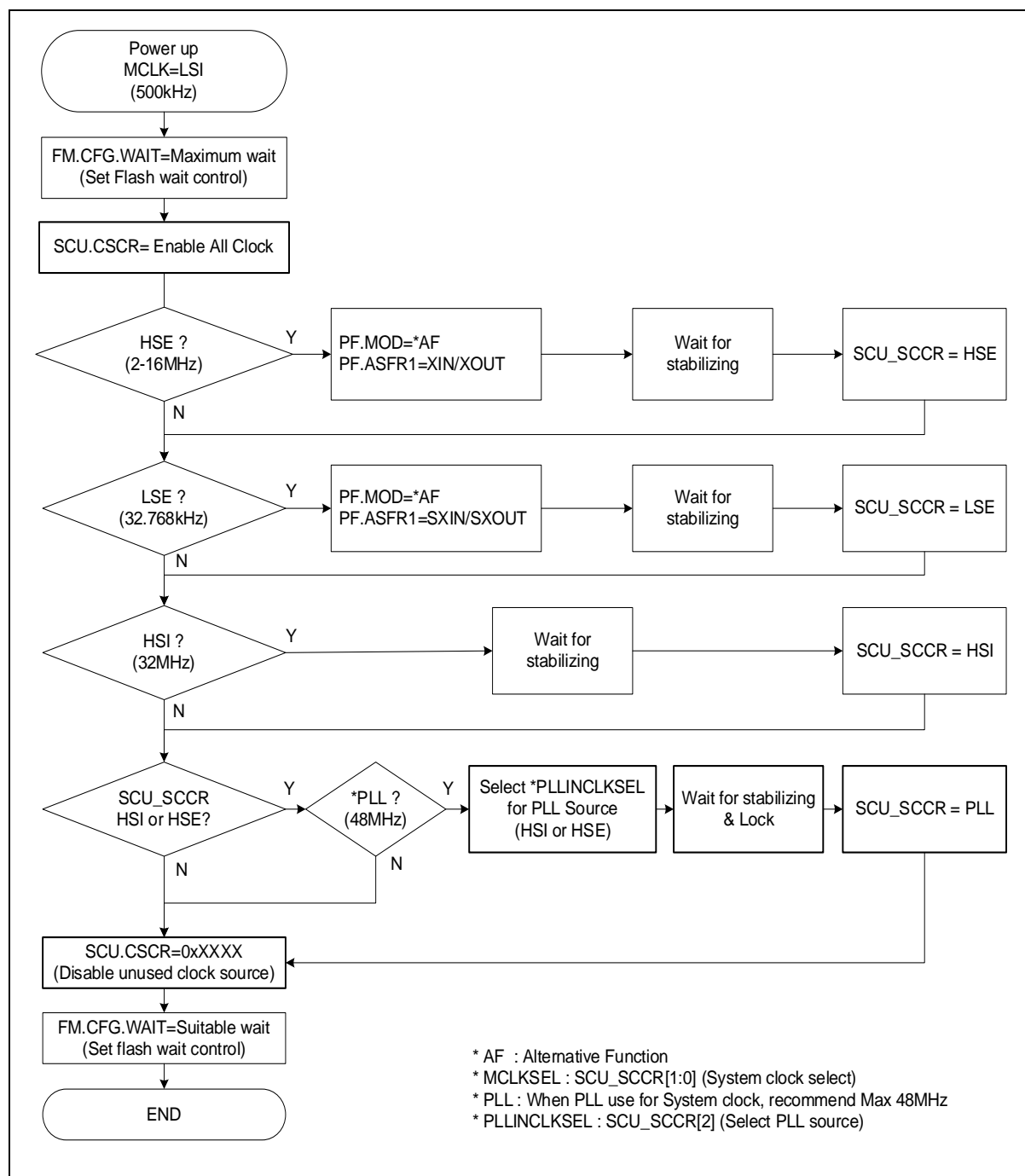


Figure 13. Clock Change Procedure

When you speed up the system clock to the maximum operating frequency, you should check flash wait control configuration. Flash read access time is one of limitation factor for performance. The wait control recommendation is suggested in Table 8.

**Table 8. Flash Wait Control Recommendation**

<b>FM.CFG.WAIT</b>	<b>FLASH Access Wait</b>	<b>Available Max System clock frequency</b>
000	0 clock wait	Up to 20MHz
001	1 clock wait	Up to 40MHz
010	2 clock wait	Up to 48MHz
011	3 clock wait	Up to 48MHz
100	4 clock wait	Up to 48MHz
11x	5 clock wait	Up to 48MHz

### 4.3 Reset

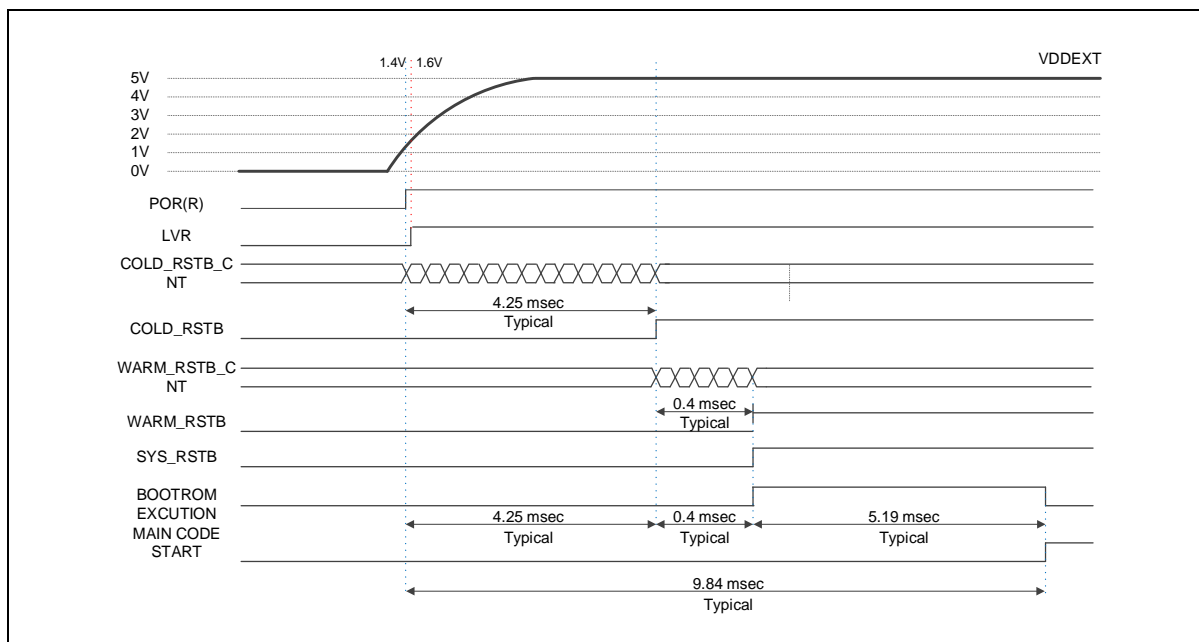
A31T214/216 series has two system reset options. One is cold reset that is effective during power up or down sequence. The other is warm reset which is generated by several reset sources. A reset event makes a chip to turn to an initial state. Reset sources of the cold reset and the warm reset are listed in Table 9.

**Table 9. Reset Sources of Cold Reset and Warm Reset**

	Cold reset	Warm reset
<b>Reset sources</b>	<ul style="list-style-type: none"> <li>• POR</li> </ul>	<ul style="list-style-type: none"> <li>• nRESET Pin</li> <li>• WDT reset</li> <li>• LVD reset</li> <li>• MCLK Fail reset</li> <li>• HSE Fail reset</li> <li>• S/W reset</li> <li>• CPU request reset</li> </ul>

#### 4.3.1 Cold reset

Cold reset is an important feature of a chip when power is up. This characteristic will affect overall system boot. Internal VDC is enabled when VDD power is turn on. Internal POR trigger level is 1.4V of VDD voltage out level, and boot operation is started at this point. The LSI clock is enabled and counts 4.25msec time for internal VDC level stabilizing. In this time, VDD voltage level should be over than initial LVR level (1.6V). After 4.25msec counting, the cold reset is released and counts 0.4msec time for warm reset synchronizing. After releasing both cold and warm reset, BOOTROM and CPU are running. Figure 14 shows power up sequence and internal reset waveforms.



**Figure 14. Power-up Procedure**

### 4.3.2 Warm reset

Warm reset event has several reset sources and some parts of chip returns to an initial state when the warm reset condition is occurred.

The warm reset source is controlled by SCU\_RSER register and the status is appeared in SCU\_RSSR register. The reset for each peripheral blocks is controlled by SCU\_PRER register. The reset can be masked independently.

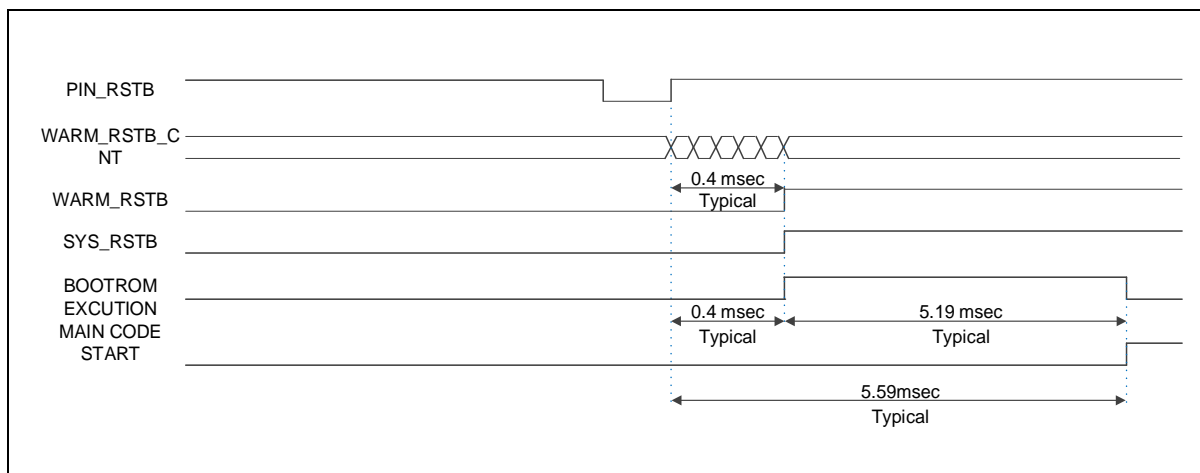


Figure 15. Warm Reset Diagram

### 4.3.3 LVR reset

Voltage level of LVR is set by low voltage reset configuration register (SCULV\_LVRCNFIG). Reset status of the LVR is shown in SCU\_RSSR register. The LVR reset is controlled by SCULV\_LVRCR register, which is cleared to “0x00” by POR reset.

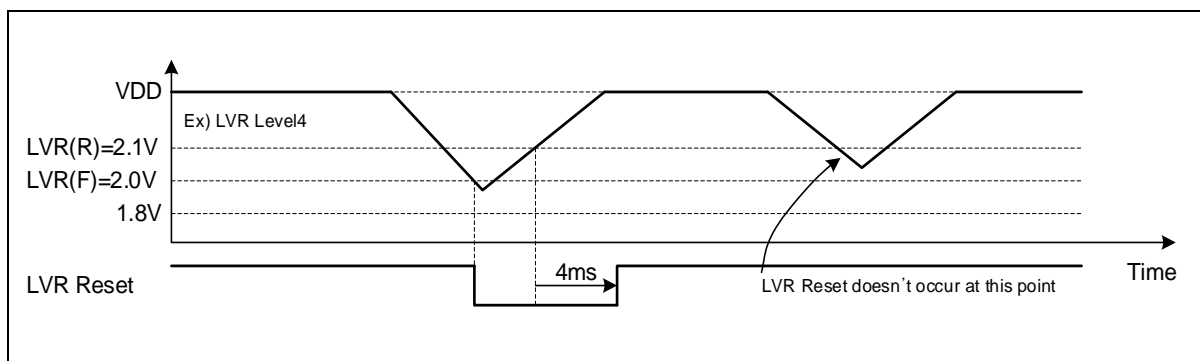


Figure 16. LVR Reset Timing Diagram

4.3.4 Reset tree

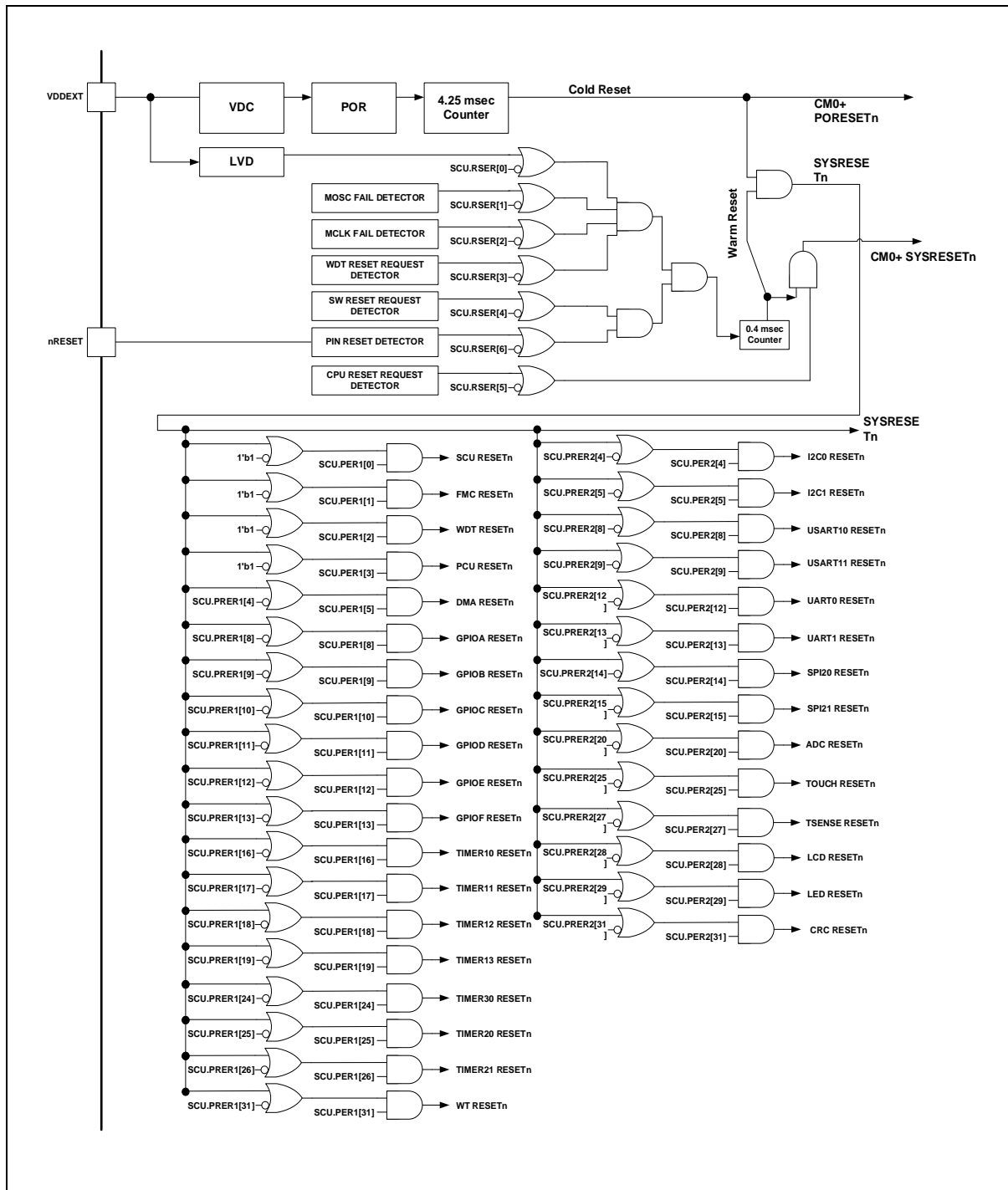


Figure 17. Reset Tree Configuration

### 4.4 Operation mode

INIT mode is an initial state of the chip when a reset is asserted. In RUN mode, CPU shows the maximum performance with high-speed clock system. SLEEP mode and Power Down modes can be used as a low power consumption mode. In the low power consumption mode, power is effectively managed to reduce power consumption by halting processor core and unused peripherals. Figure 18 describes transition between the operation modes.

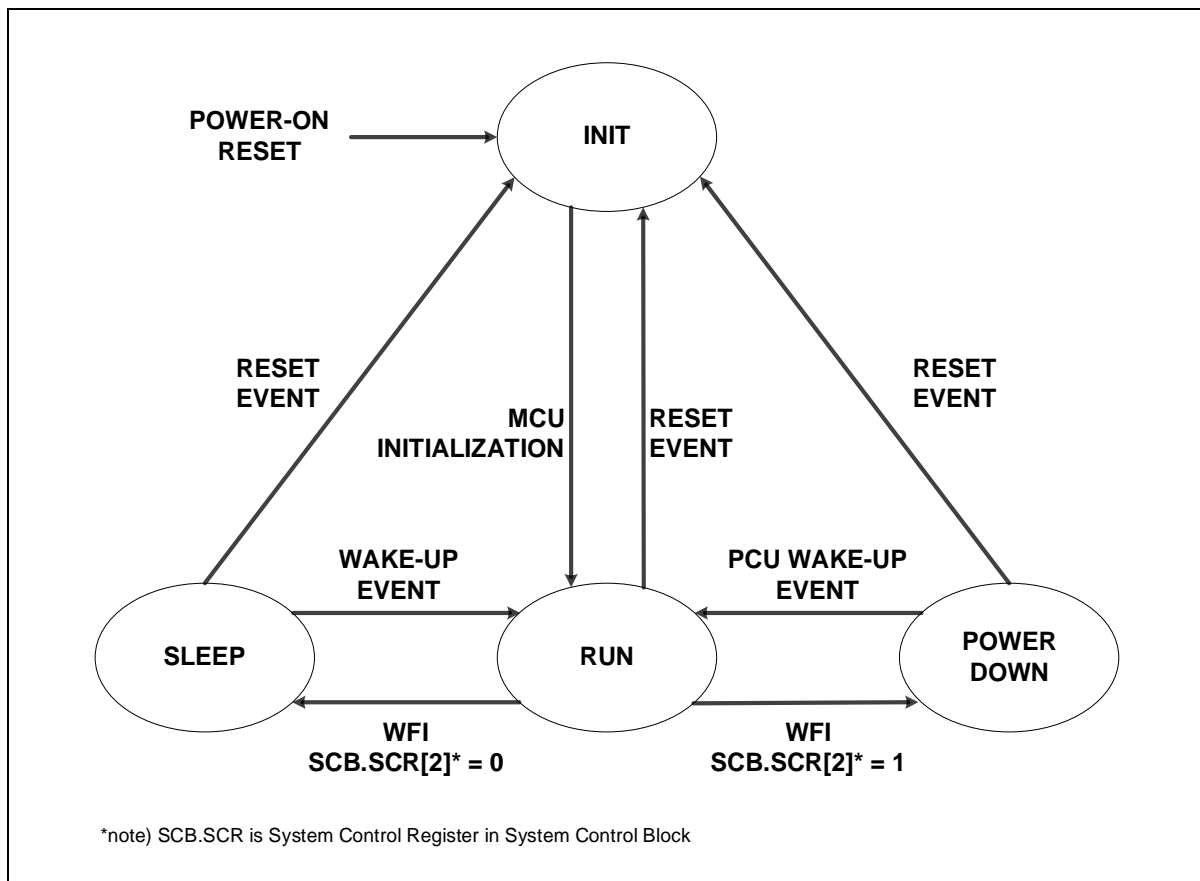


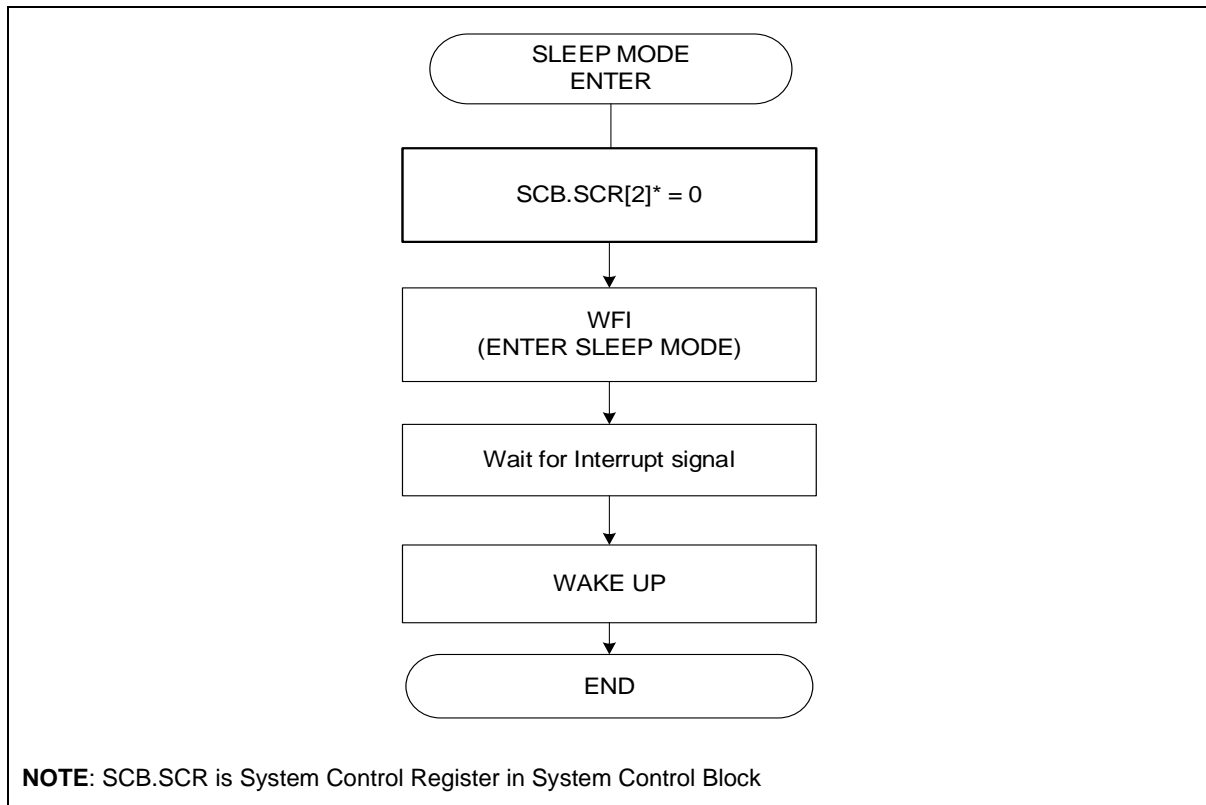
Figure 18. Transition between Operation Modes

#### 4.4.1 RUN mode

In RUM mode, CPU and the peripheral hardware operate with a high-speed clock. After a reset followed by INIT state, the system enters in the RUN mode.

#### 4.4.2 SLEEP mode

Only CPU is stopped in this mode. Each peripheral function can be enabled by the function enable and clock enable bit in the PER and PCER register.



**Figure 19. SLEEP Mode Operation Sequence**



4.4.3 Power-down mode

In STOP mode, all the internal circuits are entered the stop state.

Power down operation has special power off sequence as below picture.

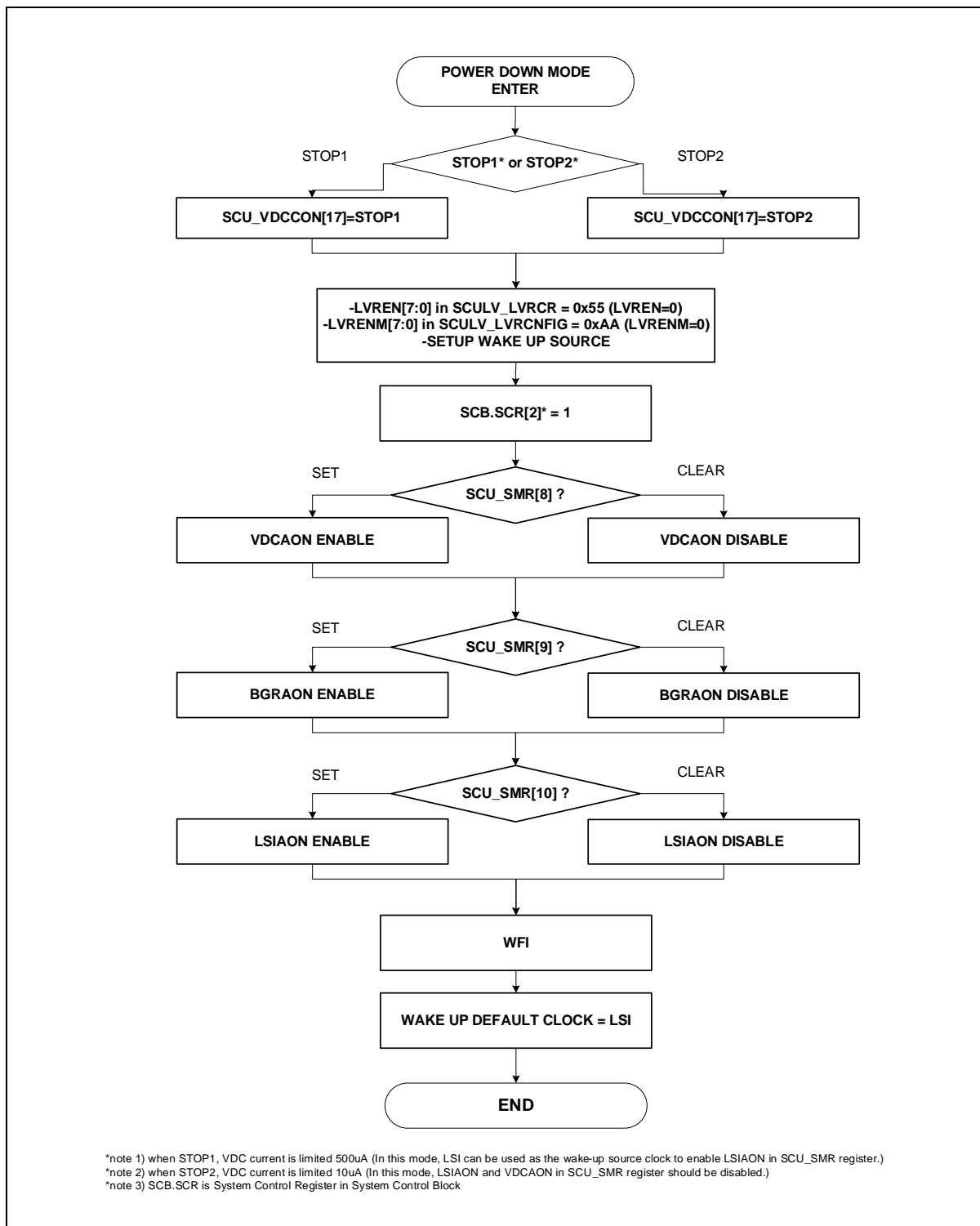


Figure 20. Power-down Mode Sequence

## 5 PCU and GPIO

Port Control Unit (PCU) configures and controls external I/Os as listed in the followings:

- External signal directions of each pins
- Interrupt trigger mode for each pins
- Internal pull-up/down register control and open drain control

General Purpose Input/Output (GPIO) is corresponding to the most pins except dedicated-function pins. GPIO ports are controlled by GPIO block as listed in the followings:

- Output signal level (H/L) select
- External interrupt interface
- Pull up/down enable or disable

Four pins in Table 10 are assigned for PCU and GPIO blocks.

**Table 10. PCU and GPIO Pins**

Pin name	Type	Description
PA	IO	PA0 to PA11
PB	IO	PB0 to PB11
PC	IO	PC0 to PC8
PD	IO	PD0 to PD5
PE	IO	PE0 to PE12
PF	IO	PF0 to PF7

### 5.1 PCU and GPIO block diagram

Figure 21 describes PCU in block diagram.

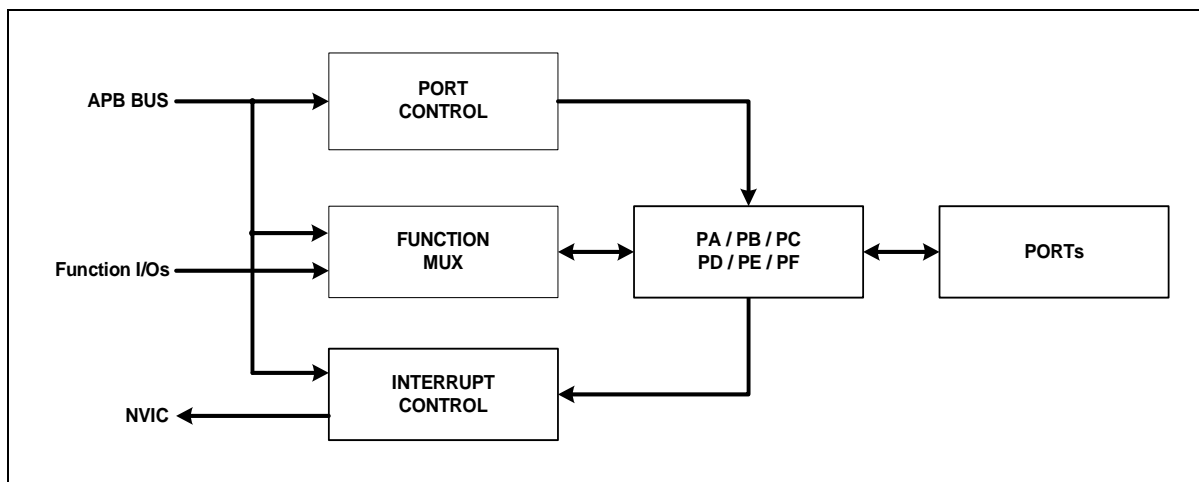


Figure 21. PCU Block Diagram

Figure 22 describes GPIO in block diagram, and Figure 23 introduces GPIO pins for external input / output.

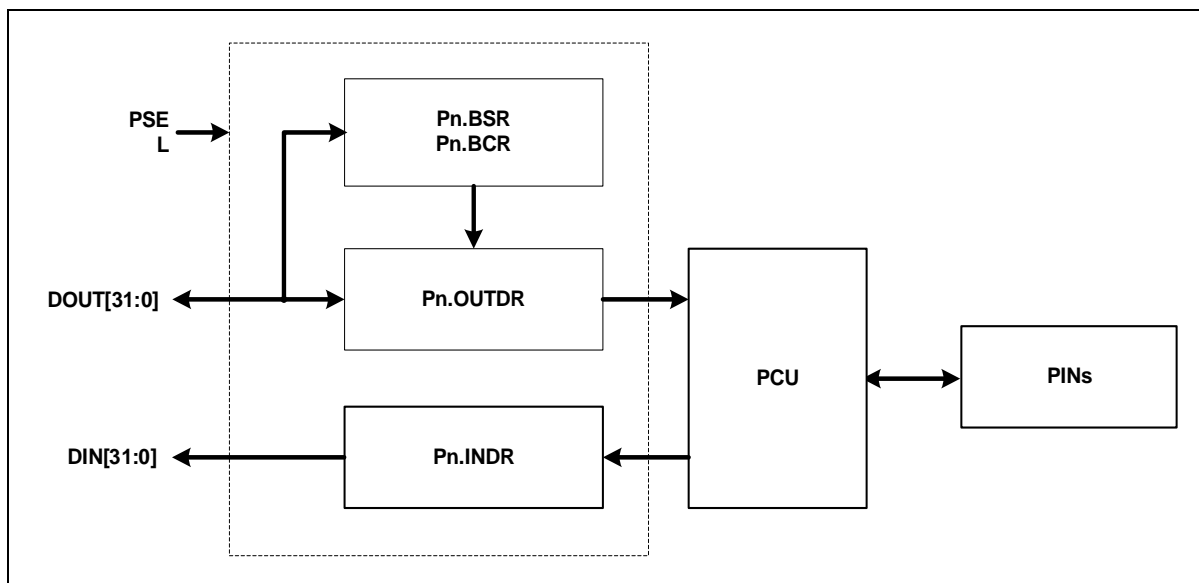


Figure 22. GPIO Block Diagram

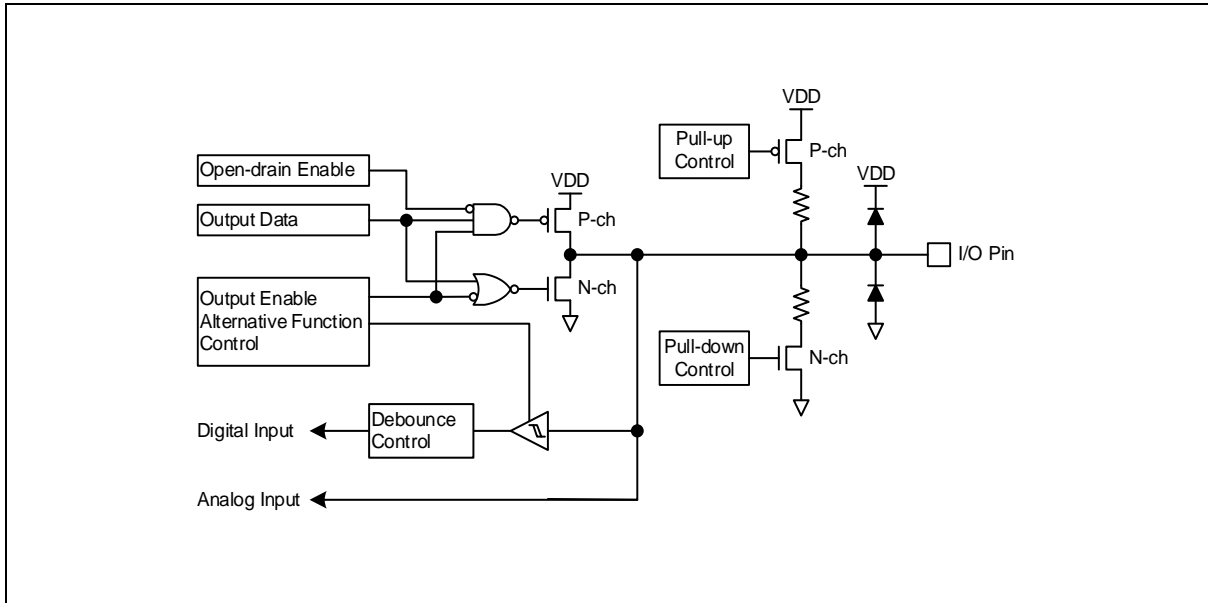


Figure 23. I/O Port Block Diagram (General I/O Pins)

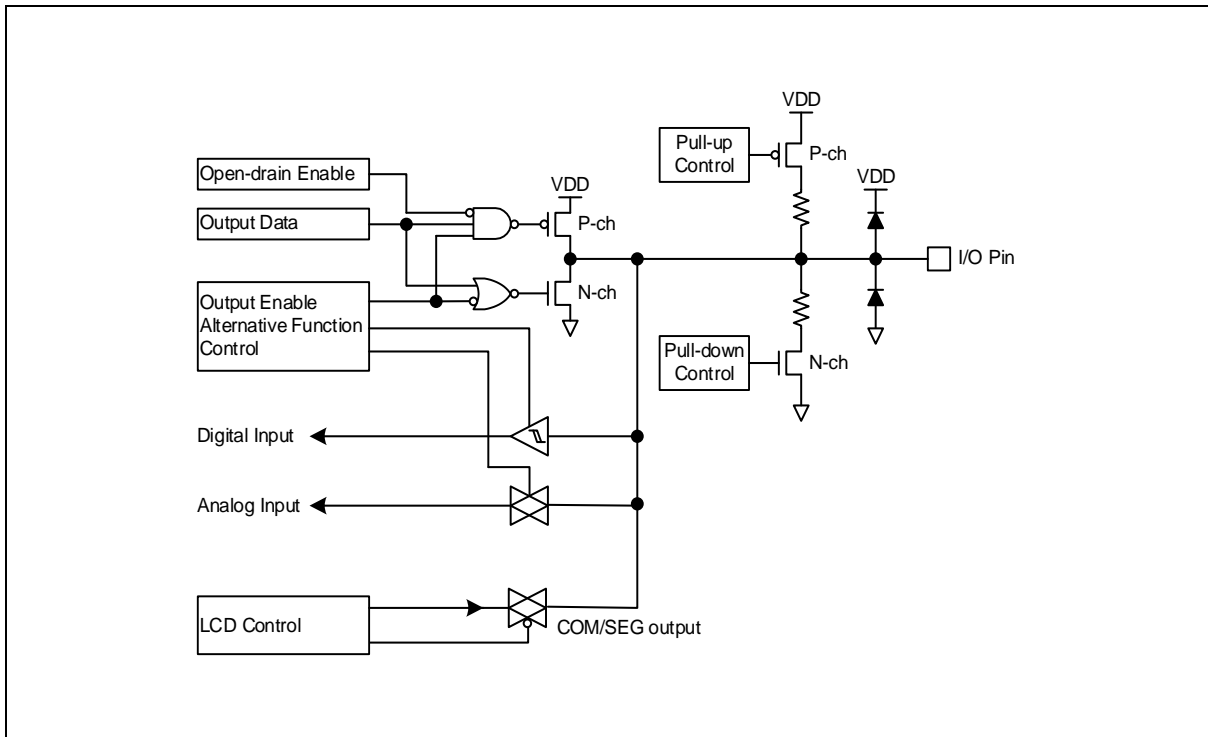


Figure 24. I/O Port Block Diagram (LCD Pins)

## 5.2 Pin multiplexing

GPIO pins have alternative function pins. Table 11 shows pin multiplexing information.

**Table 11. GPIO Alternative Function**

Pin name	Alternative function					
	AF0	AF1	AF2	AF3	AF4	AF5
PA0						CAPN
PA1	SEG22				AN14/AVREF	
PA2	SEG21				AN13	
PA3	SEG20				AN12	
PA4	SEG19				AN11	
PA5	SEG18	SDA1			AN10	
PA6	SEG17	SCL1			AN9	
PA7	SEG16				AN8	
PA8	SEG15				AN7	CS0
PA9	SEG14	T120	T12C		AN6	CS1
PA10	SEG13	(T110)	(T11C)		AN5	CS2
PA11	SEG12	T130	T13C		AN4	CS3
PB0	SEG11	USART10_TXD	USART10_MOSI	(MOSI20)	AN3	CS4
PB1	SEG10	USART10_RXD	USART10_MISO	(MISO20)	AN2	CS5
PB2	SEG9		USART10_SCK	(SCK20)	AN1	CS6
PB3		BOOT	USART10_SS	(SS20)		
PB4	SEG8	TXD0	EC30		AN0	CS7
PB5	SEG7	RXD0	(T30C)			CS8
PB6	SEG6					
PB7	SEG5					
PB8	COM7/SEG4					
PB9	COM6/SEG3					
PB10	COM5/SEG2	TXD1	EC12			CS9
PB11	SEG1	RXD1	EC13			CS10
PC0		T200	T20C			CS11
PC1		T210	T21C	MOSI20		CS12
PC2			EC20	MISO20		CS13
PC3			EC21	SCK20		ISEG15/CS14
PC4		(T100)	(T10C)	SS20		ISEG14/CS15
PC5						
PC6						
PC7						
PC8						

Table 17. GPIO Alternative Function (continued)

Pin name	Alternative function					
	AF0	AF1	AF2	AF3	AF4	AF5
PD0		SCL0	EC10	CLKO		ISEG13/CS16
PD1		SDA0	EC11			ISEG12/ICOM12/CS17
PD2		USART11_TXD	USART11_MOSI	(MOSI21)		ISEG11/ICOM11/CS18
PD3		USART11_RXD	USART11_MISO	(MISO21)		ISEG10/ICOM10/CS19
PD4		BLNK(PWM)	USART11_SCK	(SCK21)		ISEG9/ICOM9/CS20
PD5			USART11_SS	(SS21)		ISEG8/ICOM8/CS21
PE0		T11O	T11C			ISEG7/ICOM7/CS22
PE1		T10O	T10C	BLNK(PWM)		ISEG6/ICOM6/CS23
PE2		PWM30CB	(SCL0)	MOSI21		ISEG5/ICOM5
PE3	COM4/SEG0	PWM30CA	(SDA0)	MISO21		ISEG4/ICOM4
PE4	COM3/SEG31	PWM30BB		SCK21		ISEG3/ICOM3
PE5	COM2	PWM30BA		SS21		ISEG2/ICOM2
PE6	COM1	PWM30AB				ISEG1/ICOM1
PE7	COM0	PWM30AA				ISEG0/ICOM0
PE8	SEG30				VLC3	
PE9	SEG29				VLC2	
PE10	SEG28				VLC1	
PE11	SEG27				VLC0	
PE12	nRESET	nRESET	nRESET	nRESET	nRESET	nRESET
PF0	SEG26			SWDIO		
PF1	SEG25			SWCLK		
PF2	SEG24			(CLKO)		
PF3	SEG23		T30C			
PF4		(TXD1)			SXIN	
PF5		(RXD1)	(EC30)		SXOUT	
PF6		(TXD0)	(SDA1)		XIN	
PF7		(RXD0)	(SCL1)		XOUT	

**NOTE:** Unused pins are set to output from firmware (low output is recommended).

## 6 Flash memory controller

Flash memory controller is an internal flash memory interface controller, and includes following features as shown below:

- 128KB and 256KB Flash code memory
- Programmable wait control (0 to 5)
- Read protection support
- Self-Program support
- User option area : 3-page (each 512 Bytes)
- Erase, Program in user mode

**Table 12. Flash Memory Controller Features**

Item	Description	
Size	128KB	256KB
Start address	0x0000_0000	0x0000_0000
End address	0x0002_0000	0x0004_0000
Page size	512-byte	512-byte
Total page count	256 pages	512 pages
PGM unit	32-bit (1-word)	32-bit (1-word)
Erase unit	512-byte/ 1KB/ 4KB/ bulk	512-byte/ 1KB/ 4KB/ bulk

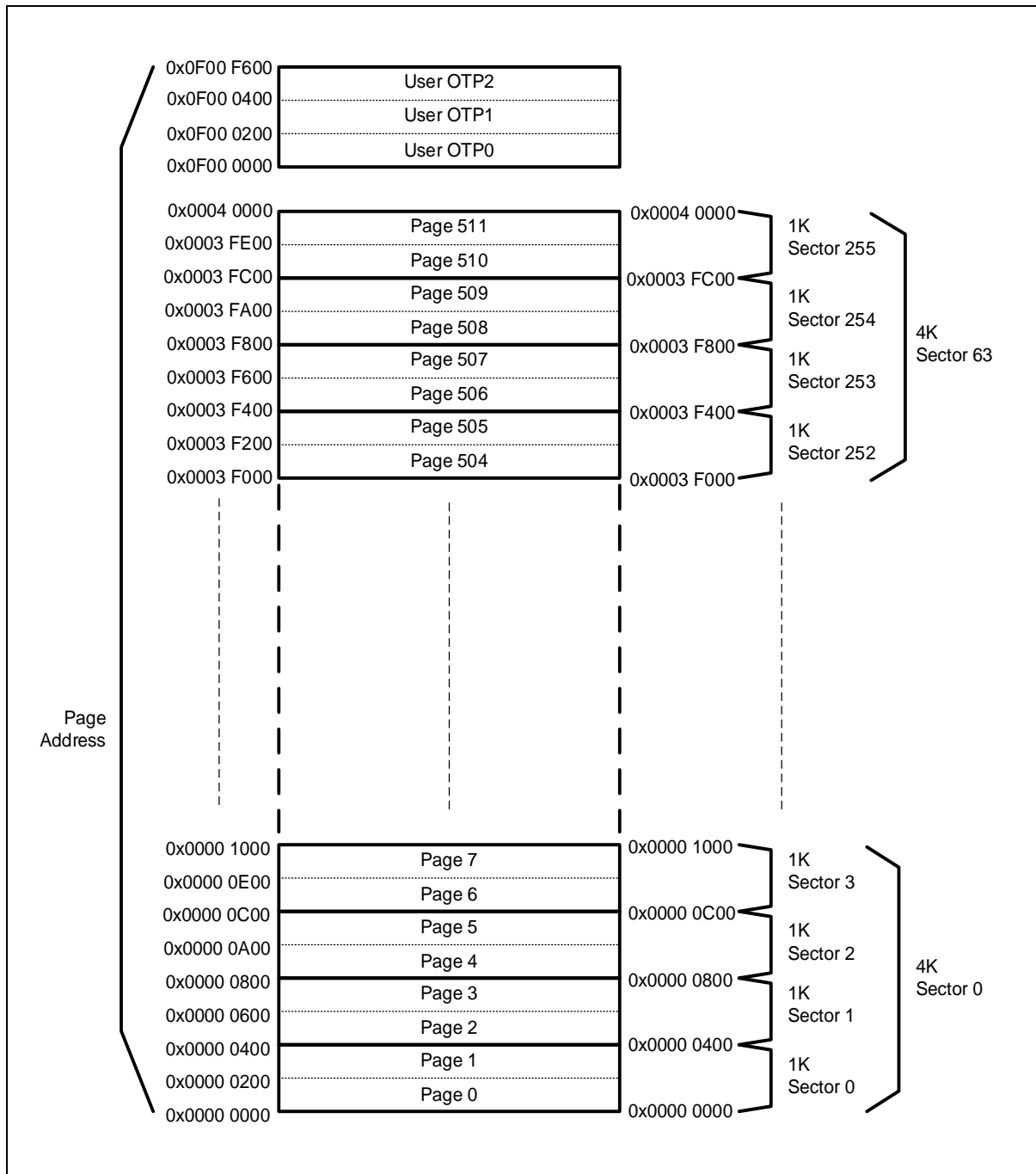


Figure 25. Flash Memory Map (256KB Code Flash)



## 7 Direct Memory Access Controller (DMAC)

The direct memory access (DMA) controller is used for high-speed data transfers between peripherals and memories. DMA enables quick data transfers having memory to memory copying or moving of data within memory.

- 4 channels
- Single transfer only
- Support 8/16/32-bit data size
- Support multiple buffer with same size
- Interrupt condition is transferred through a peripheral interrupt.

### 7.1 Block diagram

In this section, DMAC block diagram is introduced in Figure 26.

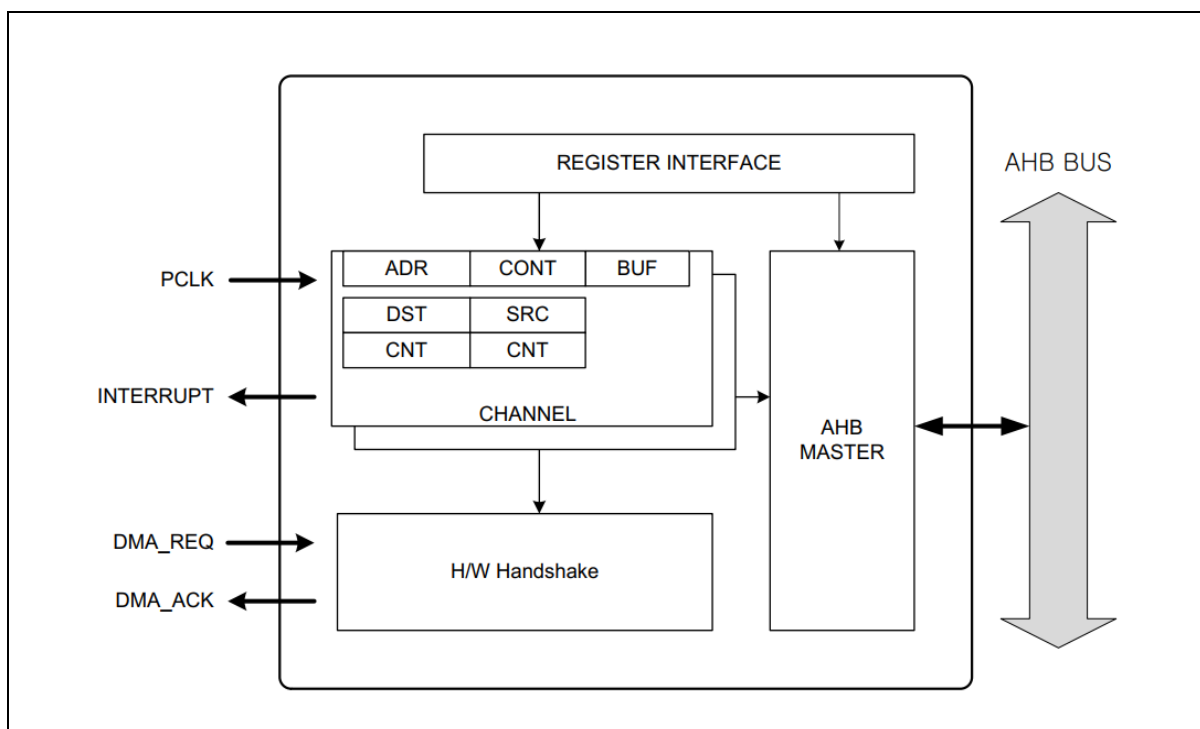


Figure 26. DMAC Block Diagram

## 8 Watchdog Timer (WDT)

Watchdog Timer (WDT) rapidly detects CPU's malfunction such as endless looping caused by noise, and returns the CPU to the normal state. WDT signal for malfunction detection can be used as either a CPU reset or an interrupt request. When WDT is not being used for malfunction detection, it can be used as a timer generating an interrupt at fixed intervals.

When WDT\_CNT value is reached to WDT\_WINDR value, a watchdog interrupt can be generated. The underflow time of WDT can be set by WDT\_DR. If the underflow occurs, an internal reset is generated. WDT operates on the WDTRC embedded RC oscillator clock.

WDT of A31T214/216 series features followings:

- 24-bit down counter (WDT\_CNT)
- Select reset or periodic interrupt
- Count clock selection
- Watchdog overflow output signal
- Counter window function

### 8.1 WDT block diagram

In this section, WDT block diagram is introduced in Figure 27.

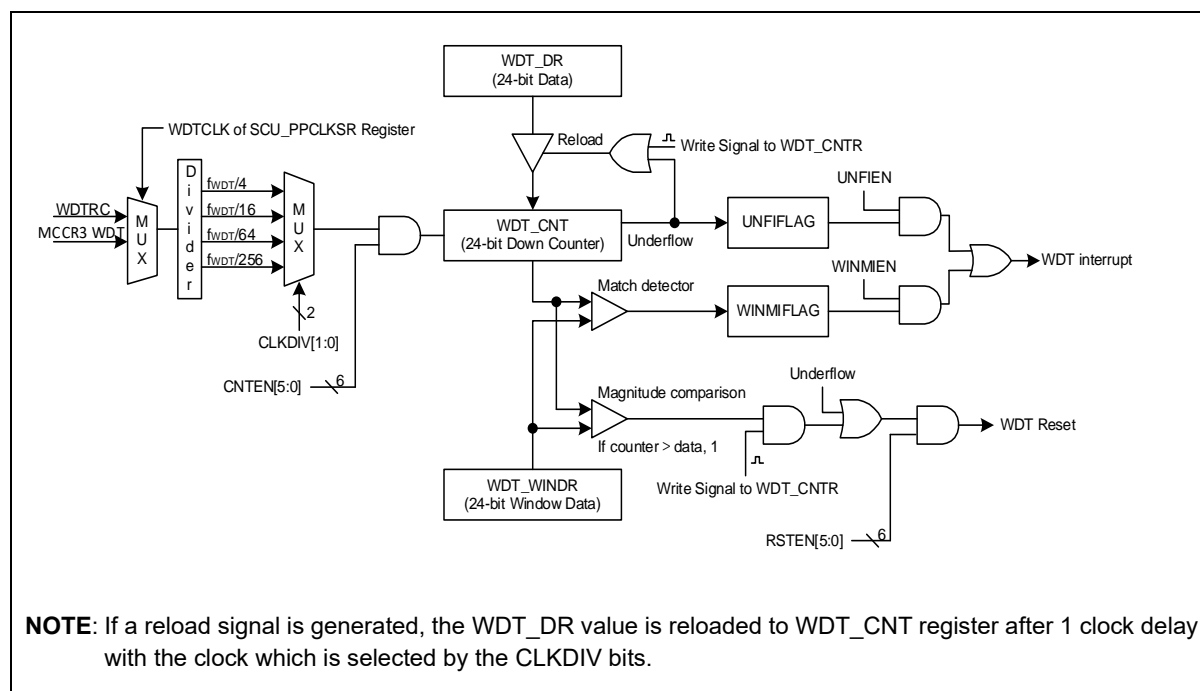


Figure 27. WDT Block Diagram

## 9 Watch Timer (WT)

Watch Timer (WT) has functions for RTC (Real Time Clock) operation. It is generally used for RTC design. WT consists of a clock source select circuit, a timer counter circuit, an output select circuit and watch timer control registers.

Prior to operate WT, a user needs to determine an input clock source and output interval, and to set WTEN as '1' in watch timer control register (WT\_CR). It is able to execute simultaneously or individually. To stop or reset WT, clear the WTEN bit in WT\_CR register.

Watch timer counter circuit incorporates a 26-bit counter. Low 14 bits of the counter form a binary counter and high 12 bits form an auto reload counter in order to raise resolution. In WTCLR, it can control WT clear and set interval value at write time, and it can read 12-bit WT counter value at read time.

### 9.1 WT block diagram

As shown in Figure 28, WT of A31T214/216 series has the following blocks:

- 14-bit divider
- 12-bit up-counter
- RTC function

Figure 28 shows a block diagram of the WT.

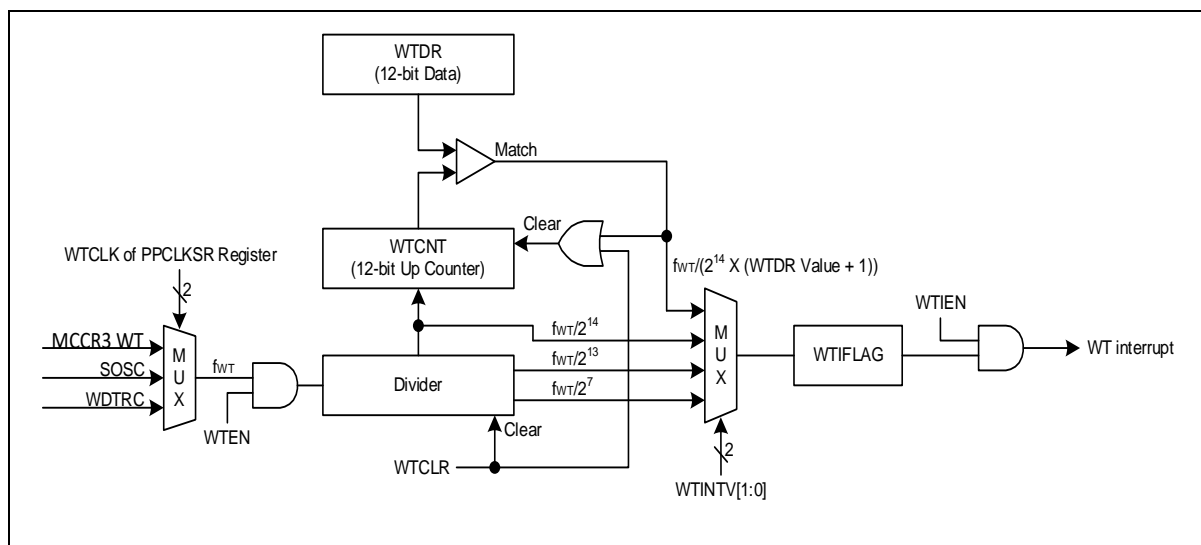


Figure 28. Watch Timer Block Diagram

## 10 16-bit timer

16-bit timer block comprises 4 channels of 16-bit general purpose timers. Each channel has an independent 16-bit counter and a dedicated prescaler that feeds a counting clock. 16-bit timer supports periodic timer, PWM pulse, one-shot and capture mode. In addition, one more optional free-run timer is provided. Main purpose of 16-bit timer is a periodical tick timer.

16-bit timer of A31T214/216 series features the followings:

- 16-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 12-bit prescaler
- Synchronous start and clear function

Table 13 introduces pins assigned for 16-bit timer.

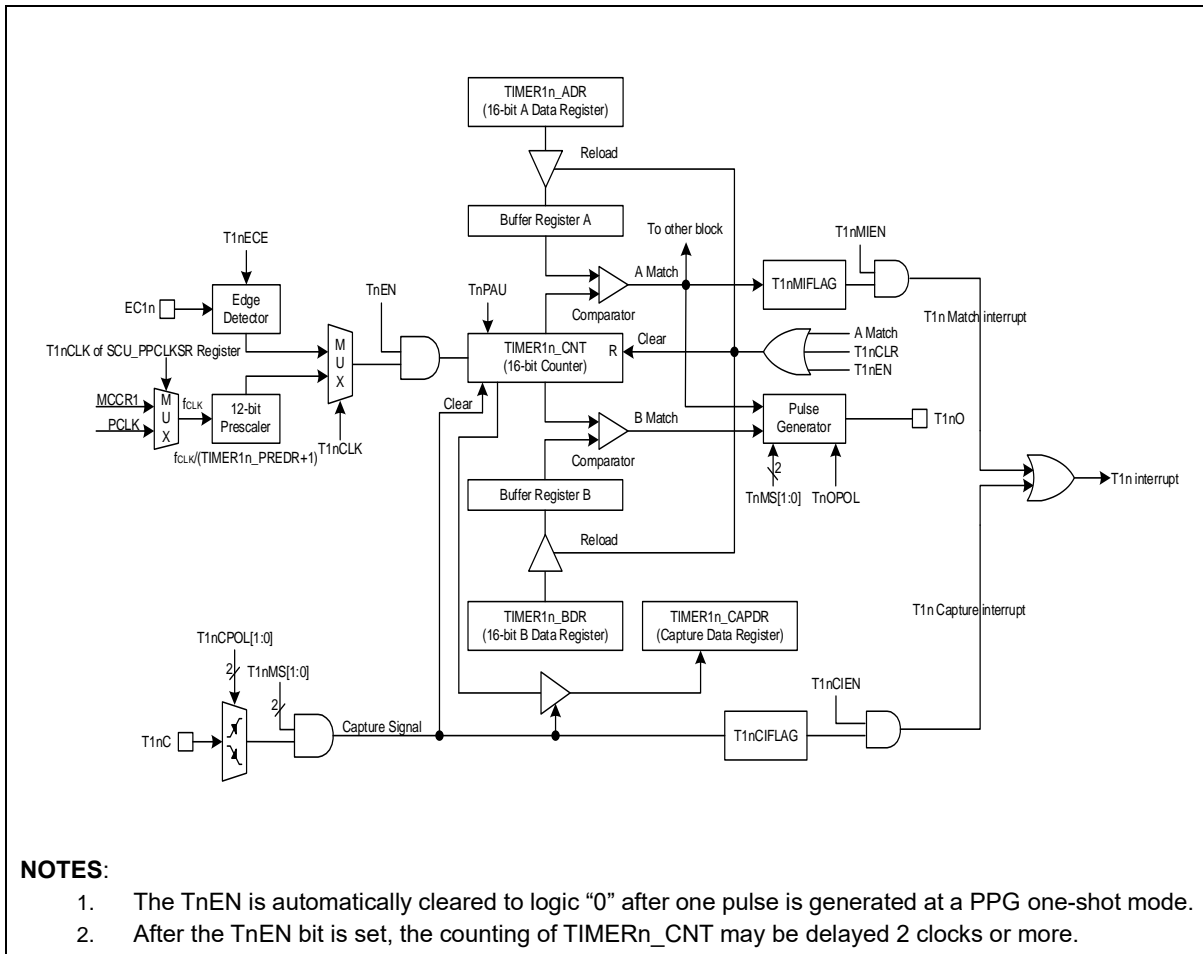
**Table 13. Pin Assignment of 16-bit Timer: External Pins**

Pin name	Type	Description
EC1n	I	Timer 1n External Clock input
T1nCAP	I	Timer 1n Capture input
T1nOUT	O	Timer 1n Output

**NOTE:** n = 0, 1, 2, and 3

### 10.1 16-bit timer block diagram

In this section, 16-bit timer is described in a block diagram in Figure 29.



**Figure 29. 16-bit Timer Block Diagram**

## 11 32-bit timer

32-bit timer block comprises 2 channels of 32-bit general purpose timers. Each channel has an independent 32-bit counter and a dedicated prescaler that feeds a counting clock. 32-bit timer supports periodic timer, PWM pulse, one-shot and capture mode. In addition, one more optional free-run timer is provided. Main purpose of 32-bit timer is a periodical tick timer.

32-bit timer of A31T214/216 series features the followings:

- 32-bit up-counter
- Periodic timer mode
- One-shot timer mode
- PWM pulse mode
- Capture mode
- 12-bit prescaler
- Synchronous start and clear function

Table 14 introduces pins assigned for 32-bit timer.

**Table 14. Pin Assignment of 32-bit Timer: External Pins**

Pin name	Type	Description
EC2n	I	Timer 2n external clock input
T2nCAP	I	Timer 2n capture input
T2nOUT	O	Timer/PWM/one-shot output

**NOTE:** n = 0 or 1

### 11.1 32-bit timer block diagram

In this section, 32-bit timer is described in a block diagram in Figure 30.

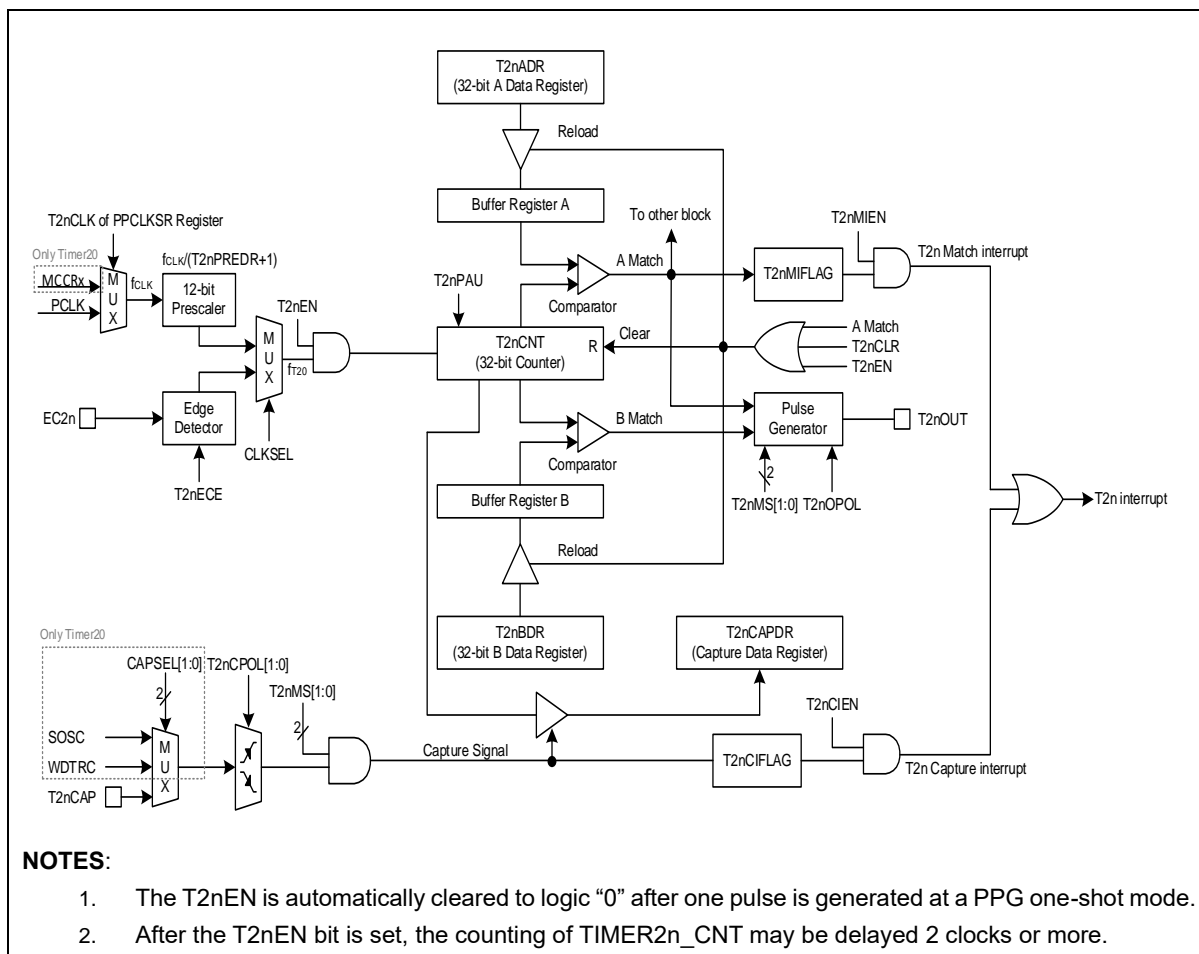


Figure 30. 32-bit Timer Block Diagram

## 12 Timer counter 30

Timer counter 30 of A31T214/216 series consists of a multiplexer, a comparator, 16-bit sized timer data registers A/B/C, and many other registers used for its operation. Main features are listed in the followings:

- 16-bit up/down-counter
- Periodic timer mode
- Back-to-Back mode
- Capture mode
- 12-bit prescaler

Table 15 introduces pins assigned for the timer counter 30.

**Table 15. Pin Assignment of Timer Counter 30: External Pins**

Pin name	Type	Description
EC30	I	External clock input
T30CAP	I	Capture input
BLNK	I	External sync signal input
PWM30AA	O	PWM output
PWM30AB	O	PWM output
PWM30BA	O	PWM output
PWM30BB	O	PWM output
PWM30CA	O	PWM output
PWM30CB	O	PWM output



### 12.1 Timer counter 30 block diagram

In this section, timer counter 30 is introduced in a block diagram.

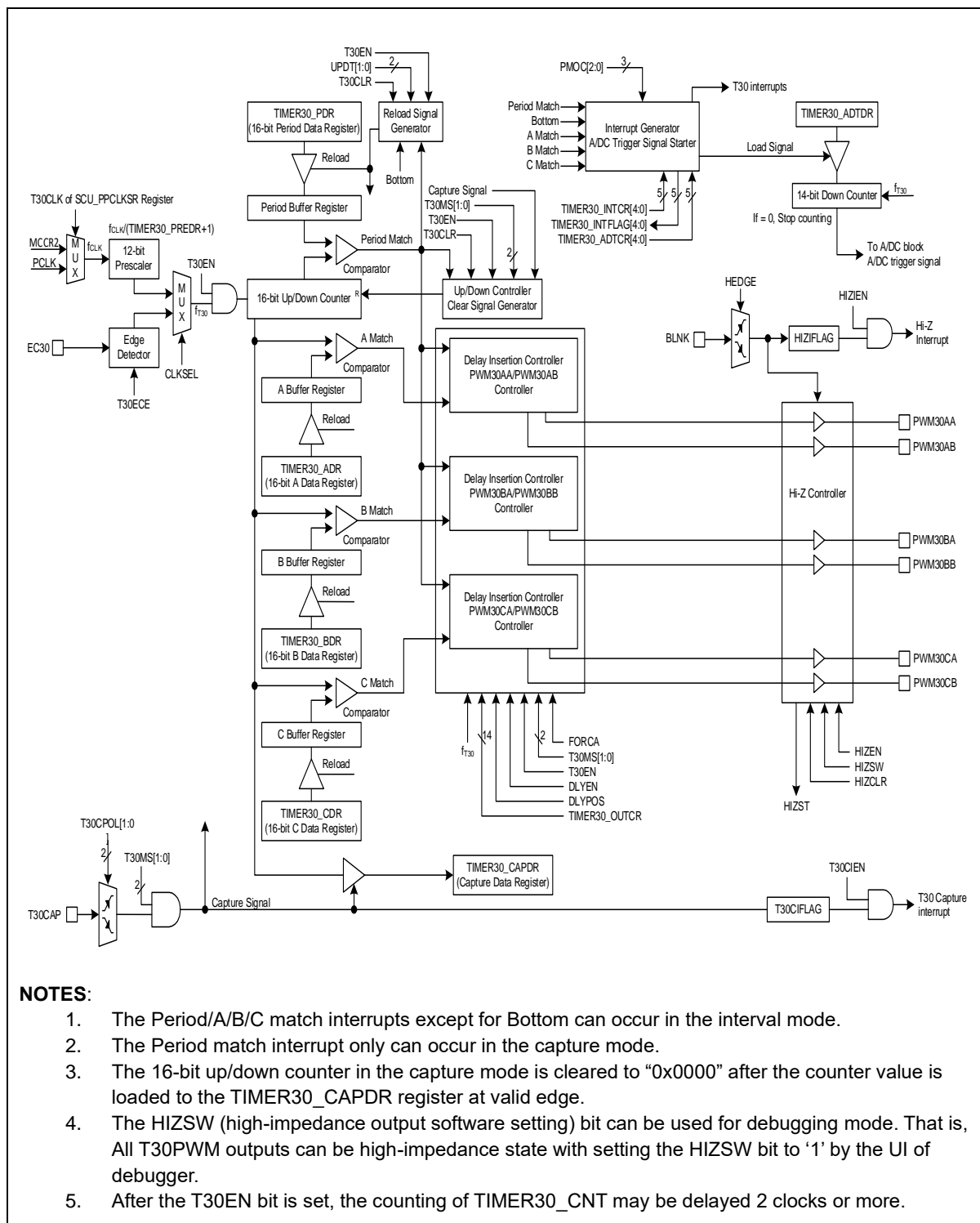


Figure 31. Timer Counter 30 Block Diagram

## 13 USART

Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication device. The main features are listed below:

- Full Duplex Operation. (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation.
- Baud Rate Generator.
- Supports Serial Frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits.
- Odd or Even Parity Generation and Parity Check are Supported by Hardware.
- Data Over Run Detection.
- Framing Error Detection.
- Three Separate Interrupts on TX Completion, TX Data Register Empty and RX Completion.
- Double Speed Asynchronous communication mode.

Additional features are:

- 0% Error Baud Rate by floating point count register.
- Supports receive time out interrupt.
- Supports direct memory access and interrupt.

Table 16 introduces pins assigned for the USART.

**Table 16. Pin Assignment of USART: External Pins**

Pin name	Type	Description
TXDn	O	UART Channel n transmit output
RXDn	I	UART Channel n receive input
SSn	I/O	SPIn Slave select input / output
SCKn	I/O	SPIn Serial clock input / output
MOSIn	I/O	SPIn Serial data ( Master output, Slave input )
MISO n	I/O	SPIn Serial data ( Master input, Slave output )

**NOTE:** n = 10 and 11

### 13.1 USART block diagram

In this section, USART and SPIN are introduced in block diagrams.

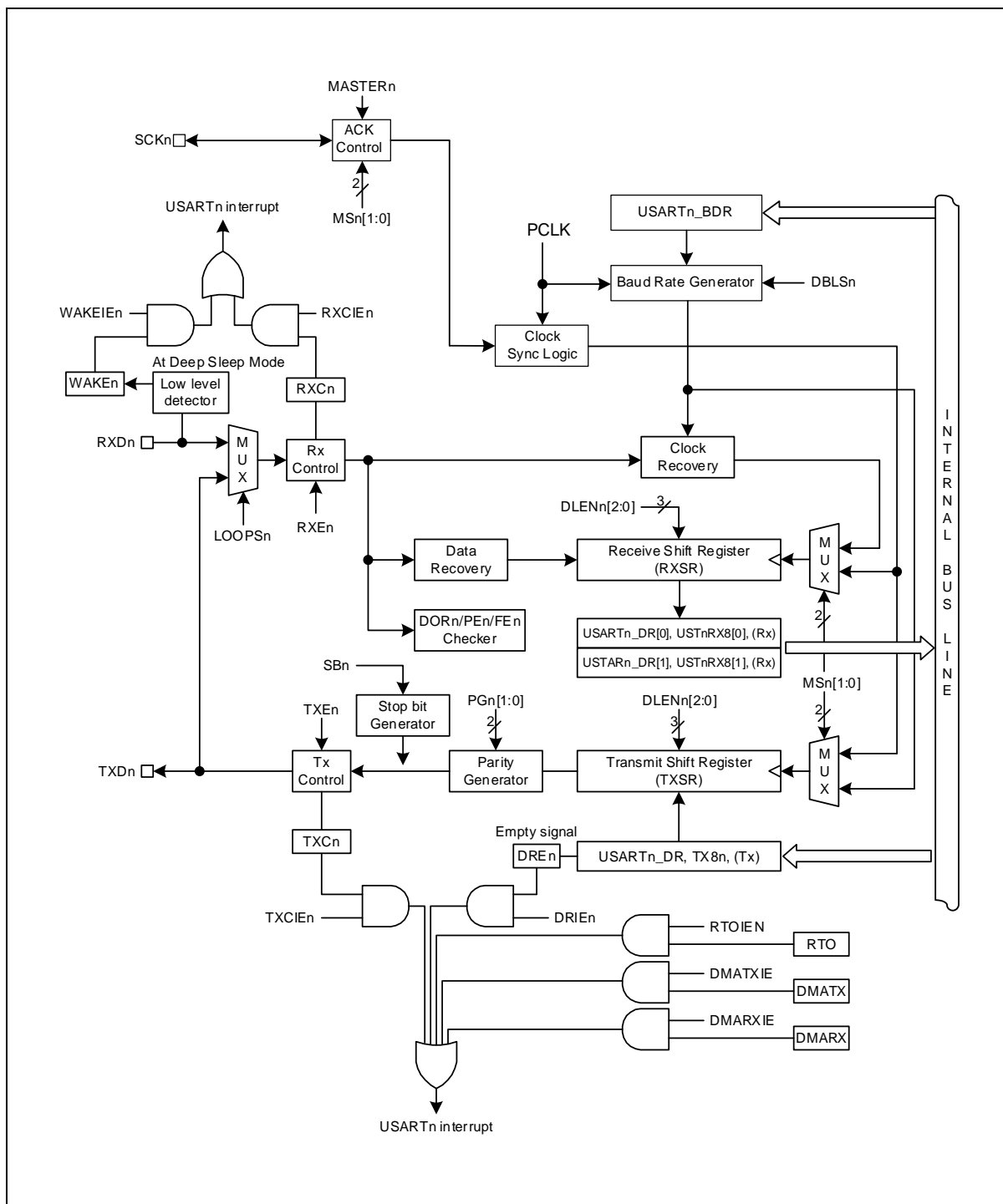


Figure 32. USART Block Diagram (n = 10 and 11)

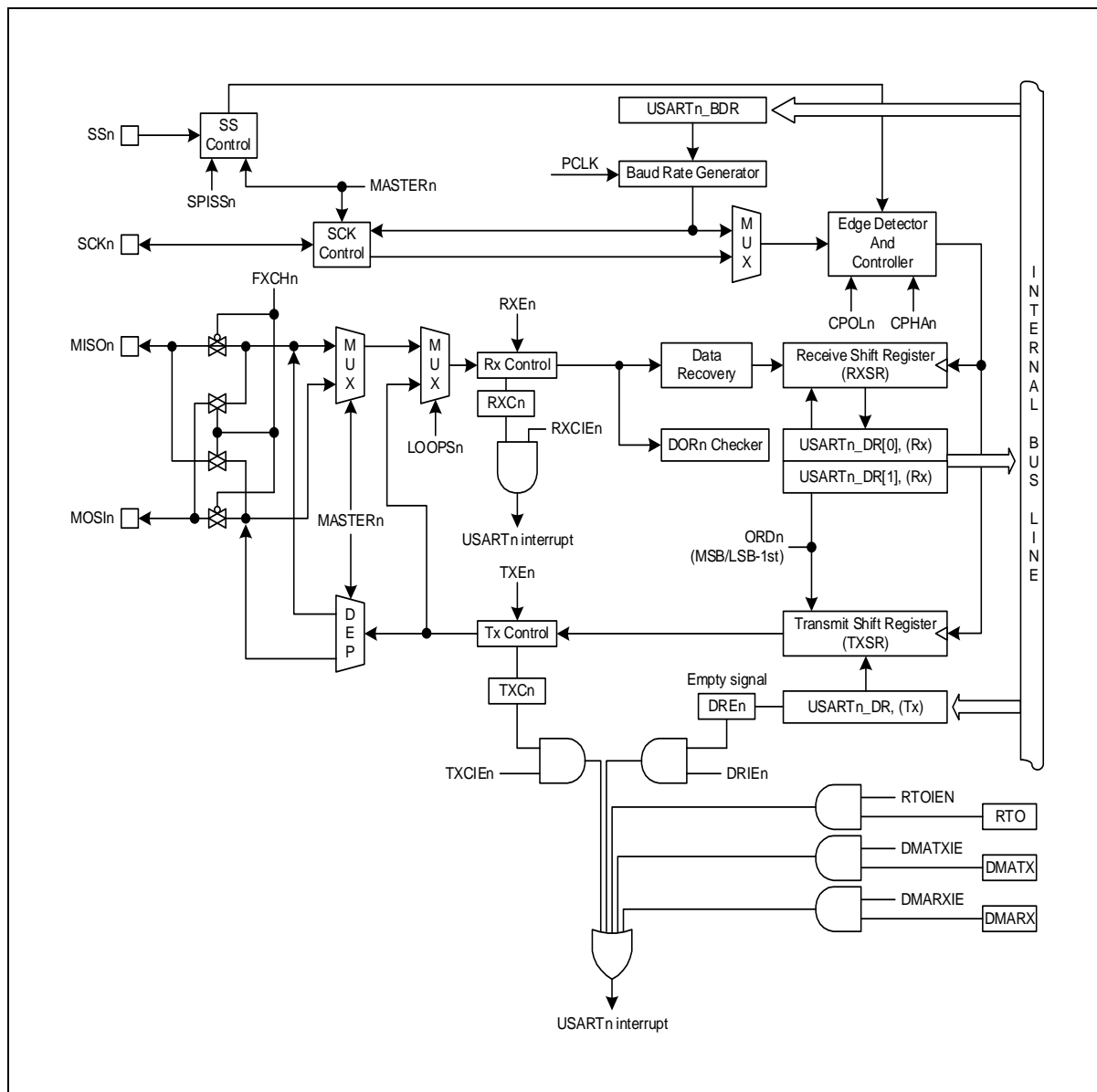


Figure 33. SPIN Block Diagram (n = 10 and 11)

## 14 UART

Universal Asynchronous serial Receiver and Transmitter (UART) is a highly flexible serial communication device. UART operation status including error status can be read from status register. The prescaler which generates proper baud rate, is exist for each UART channel. The prescaler can divide the UART clock source that is PCLK, from 1 to 65535. And baud rate generation is by clock which internally divided by 16 of the prescaled clock and 8-bit precision clock tuning function. Programmable interrupt generation function will help to control the communication via UART channel

The main features are listed below:

- Compatible with 16450
- Standard asynchronous control bit (start, stop, and parity) configurable B
- Programmable 16-bit fractional baud generator
- Programmable serial communication
- 5-, 6-, 7- or 8- bit data transfer
- Even, odd, or no-parity bit insertion and detection
- 1-, 1.5- or 2-stop bit-insertion and detection
- 16-bit baud rate generation with 8-bit fraction control
- Hardware inter-frame delay function
- Stop bit error detection
- Detail status register

Table 17 introduces pins assigned for the UART.

**Table 17. Pin Assignment of UART: External Pins**

Pin name	Type	Description
TXD0	O	UART Channel 0 transmit output
RXD0	I	UART Channel 0 receive input
TXD1	O	UART Channel 1 transmit output
RXD1	I	UART Channel 1 receive input

**NOTE:** n = 0 and 1

### 14.1 UART block diagram

In this section, the UART interface block is described in a block diagram.

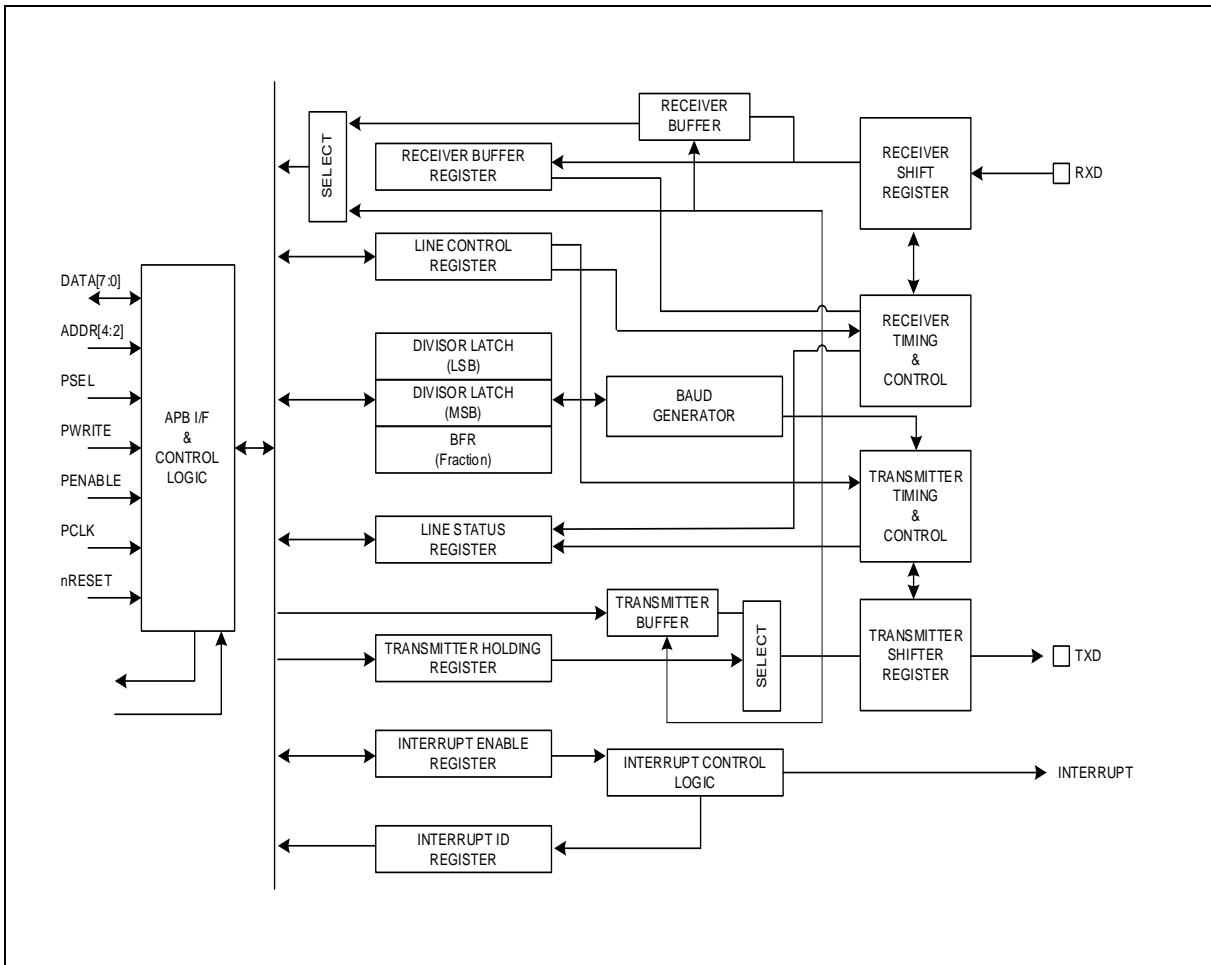


Figure 34. UART Block Diagram

## 15 I2C interface

I2C is one of industrial standard serial communication protocols, and which uses 2 bus lines such as Serial Data Line (SDAn) and Serial Clock Line (SCLn) to exchange data. Because both SDAn and SCLn lines are open-drain output, each line needs pull-up resistor respectively.

I2C features the followings (n = 0 and 1):

- Compatible with I2C bus standard.
- Multi-master operation.
- Up to 1MHz data transfer read speed.
- 7-bit address.
- Support two slave address.
- Both master and slave operation.
- Bus busy detection

Table 18 introduces pins assigned for I2C interface.

**Table 18. Pin Assignment of I2C: External Pins**

Pin name	Type	Description
SCL0	I/O	I2C channel 0 Serial clock bus line (open-drain)
SDA0	I/O	I2C channel 0 Serial data bus line (open-drain)
SCL1	I/O	I2C channel 1 Serial clock bus line (open-drain)
SDA1	I/O	I2C channel 1 Serial data bus line (open-drain)

**NOTE:** n = 0 and 1

### 15.1 I2C block diagram

In this section, I2C interface block is described in a block diagram.

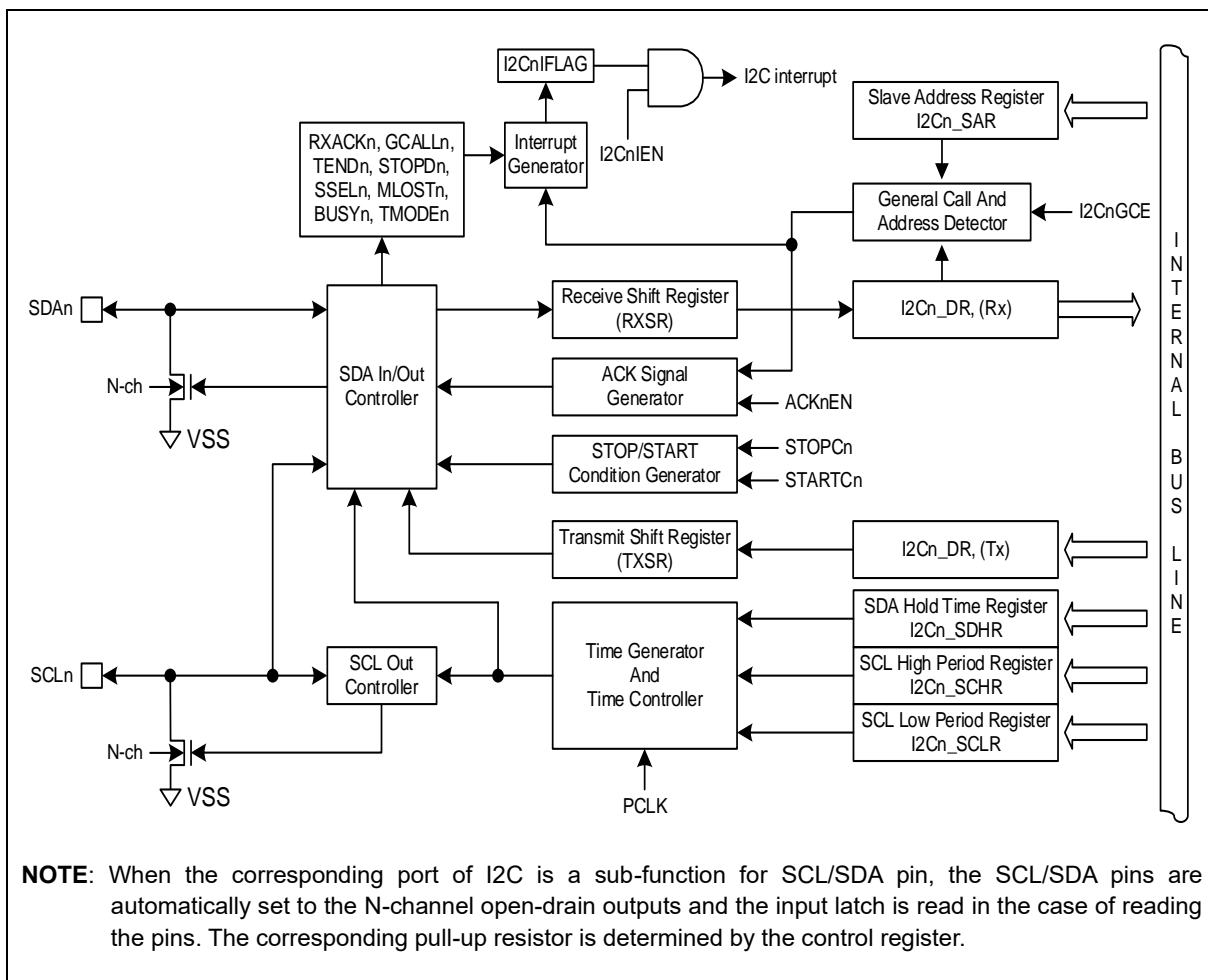


Figure 35. I2C Block Diagram



## 16 Serial Peripheral Interface (SPI)

A channel serial interface is provided for synchronous serial communications with external peripherals. SPI block support both of master and slave mode. Four signals will be used for SPI communication such as SS, SCK, MOSI, and MISO.

SPI of A31T214/216 series features the followings:

- Master or Slave operation.
- Programmable clock polarity and phase.
- 8, 9, 16, 17-bit wide transmit/receive register.
- 8, 9, 16, 17-bit wide data frame.
- Loop-back mode.
- Programmable start, burst, and stop delay time.
- DMA transfer operation.

Table 19 introduces pins assigned for SPI.

**Table 19. Pin Assignment of SPI: External Pins**

Pin name	Type	Description
SSn	I/O	SPIn Slave select input / output
SCKn	I/O	SPIn Serial clock input / output
MOSIn	I/O	SPIn Serial data ( Master output, Slave input )
MISO n	I/O	SPIn Serial data ( Master input, Slave output )

**NOTE:** n = 20 and 21

### 16.1 SPI block diagram

In this section, SPI is described in a block diagram in Figure 36.

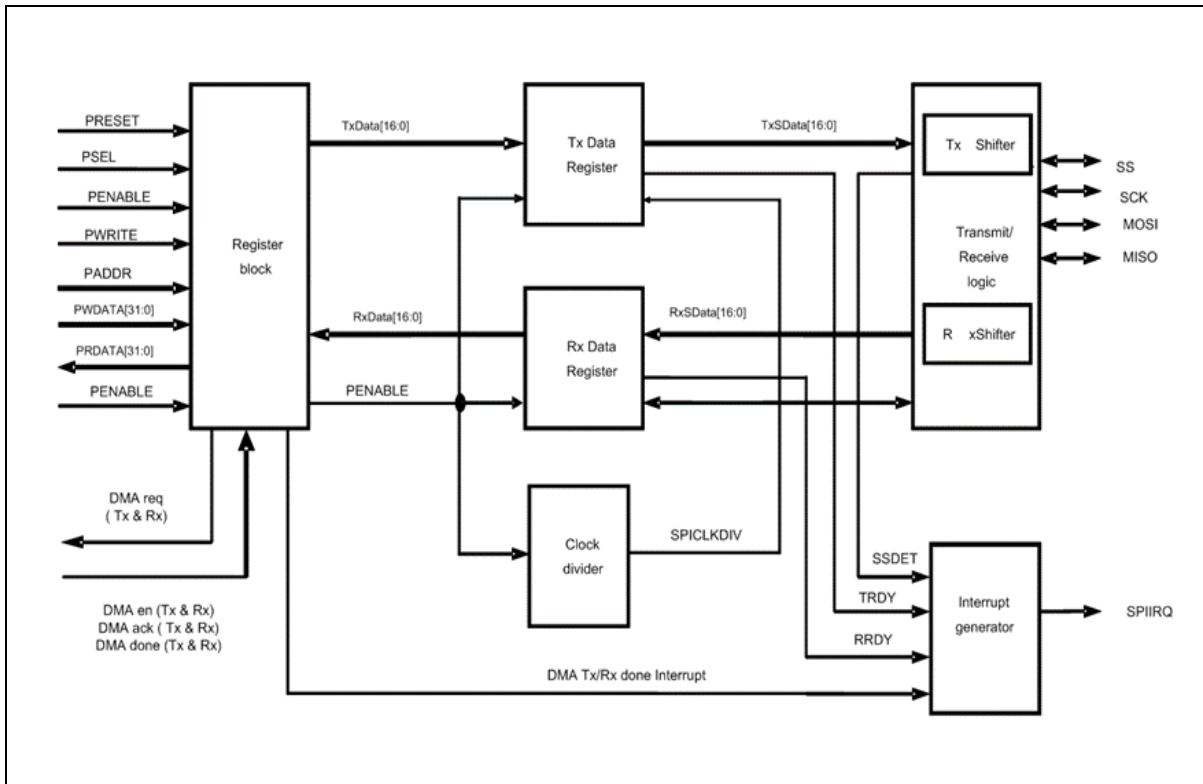


Figure 36. SPI Block Diagram

## 17 12-bit ADC

Analog to Digital Converter (A/D Converter) allows conversion of an analog input signal to corresponding 12-bit digital value. The A/D module has 14 analog inputs. The output of the multiplexer is the input into the converter which generates the result through successive approximation. The A/D module has three registers which are the A/D converter control register (ADC\_CR), A/D converter data register (ADC\_DR) and A/D converter prescaler data register (ADC\_PREDR). The channels to be converted are selected by setting ADSEL[3:0]. The register ADC\_DR contains the results of the A/D conversion. When the conversion is completed, the result is loaded into the ADC\_DR, the A/D conversion status bit AFLAG is set to '1', and the A/D interrupt is set. During A/D conversion, AFLAG bit is read as '0'.

ADC block of A31T214/216 series consists of an independent ADC unit featuring the followings:

- 14 channels of analog inputs
- S/W (ADST) and Timer trigger: TIMER10/11/12 A match and ADC trigger signal from TIMER30 support
- Maximum 4.5MHz conversion rate (Max. 150Ksps)
- Conversion time: 30 clock
- 6-bit Prescaler

Table 20 introduces pins assigned for ADC.

**Table 20. Pin Assignment of ADC: External Signal**

Pin name	Type	Description
AVREF	P	Analog Reference Voltage
AN0	A	ADC Input 0
AN1	A	ADC Input 1
AN2	A	ADC Input 2
AN3	A	ADC Input 3
AN4	A	ADC Input 4
AN5	A	ADC Input 5
AN6	A	ADC Input 6
AN7	A	ADC Input 7
AN8	A	ADC Input 8
AN9	A	ADC Input 9
AN10	A	ADC Input 10
AN11	A	ADC Input 11
AN12	A	ADC Input 12
AN13	A	ADC Input 13
AN14	A	ADC Input 14

### 17.1 12-bit ADC block diagram

In this section, 12-bit ADC is described in a block diagram in Figure 37.

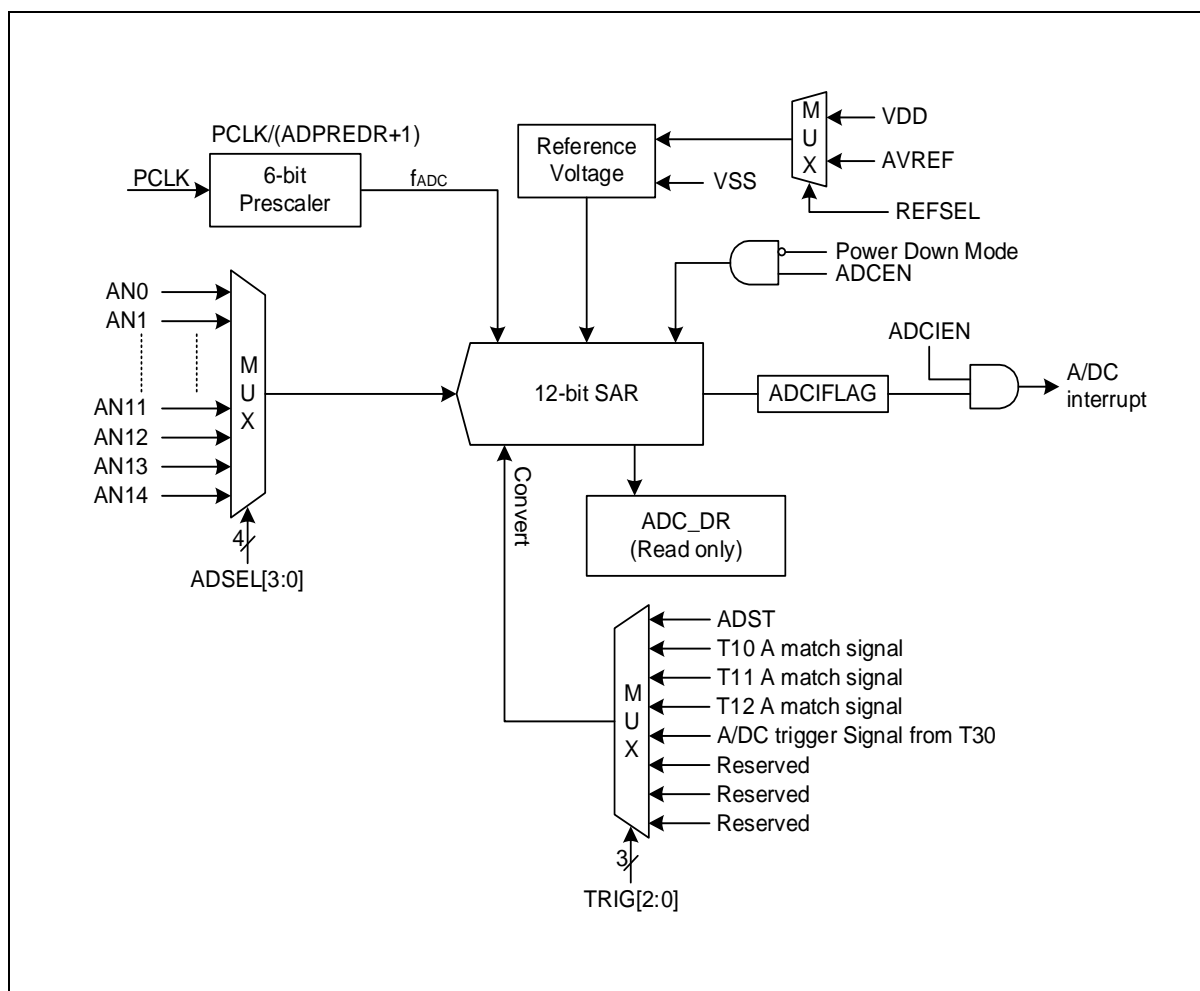


Figure 37. 12-bit ADC Block Diagram

## 18 TOUCH

Capacitive touch sensor systems are typical Human Machine Interfaces (HMI) which operate by detecting changes in electrostatic capacitance produced by the touch of a finger or other conductor.

The use of capacitive touch technology can easily improve reliability in product design, and enhance the end-user experience. It also enables manufacturing costs to be lowered in a wide range of fields such as household appliances (white goods), healthcare devices, and other electric and electronic equipment.

TOUCH of A31T214/216 series features the followings:

- 10V Conducted Susceptibility (CS) Immunity
- Self-capacitive Touch Key Sensor.
- Total 24-channel Touch Key Support.
- 16-bits Sensing Resolutions.
- Fast Initial Self Calibration.
- Key Detection Mode: Single/Multi-Mode.
- Clock Frequency during Sensing Operation: 16MHz.
- The Improvement of the SNR by Bias-Calibration in Analog Sensing Block.
- VDD Operating Voltage: 2.7V to 5.5V.
- Current Consumption: T.B.D.
- Current Consumption @STOPmode: < 1uA.
- Operation Temperature: -40°C to +85°C.

Table 21 introduces pins assigned for TOUCH.

**Table 21. Pin Assignment of TOUCH: External Signal**

Pin name	Type	Description
CS0 to CS23	IA	Capacitive Touch switch input

### 18.1 TOUCH block diagram

Figure 38 shows a block diagram of TOUCH.

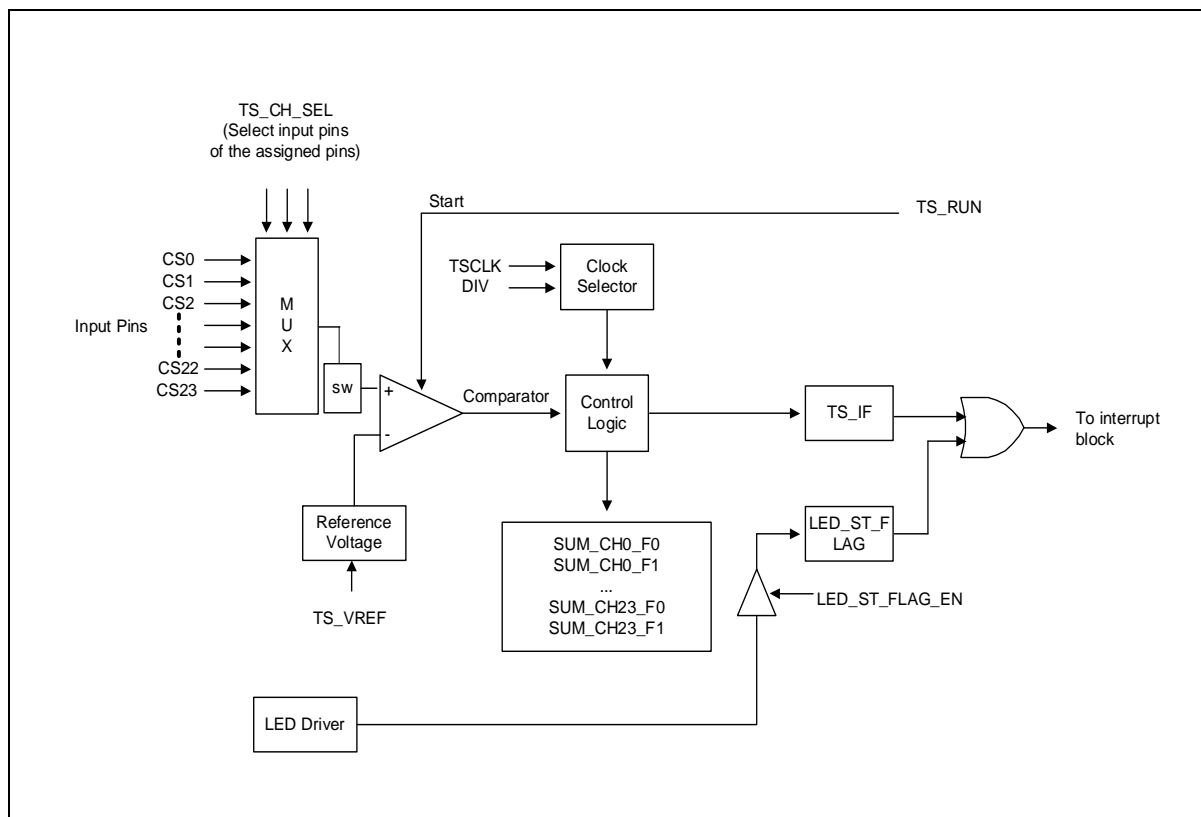


Figure 38. TOUCH Block Diagram

## 19 LCD Driver

LCD Driver is controlled by the LCD control register (LCD\_CR) and the LCD Driver bias and contrast control register (LCD\_BCCR).

The LCD\_CR<LCLK> bits determine the frequency of COM signal scanning of each segment output. A RESET clears the LCD control registers LCD\_CR and LCD\_BCCR values to logic '0'.

The LCD display can continue operating during IDLE and STOP modes.

The clock and duty for LCD Driver are automatically initialized by hardware, whenever the LCD\_CR register data value is re-written. Therefore, it is not recommended that users re-write the LCD\_CR frequently.

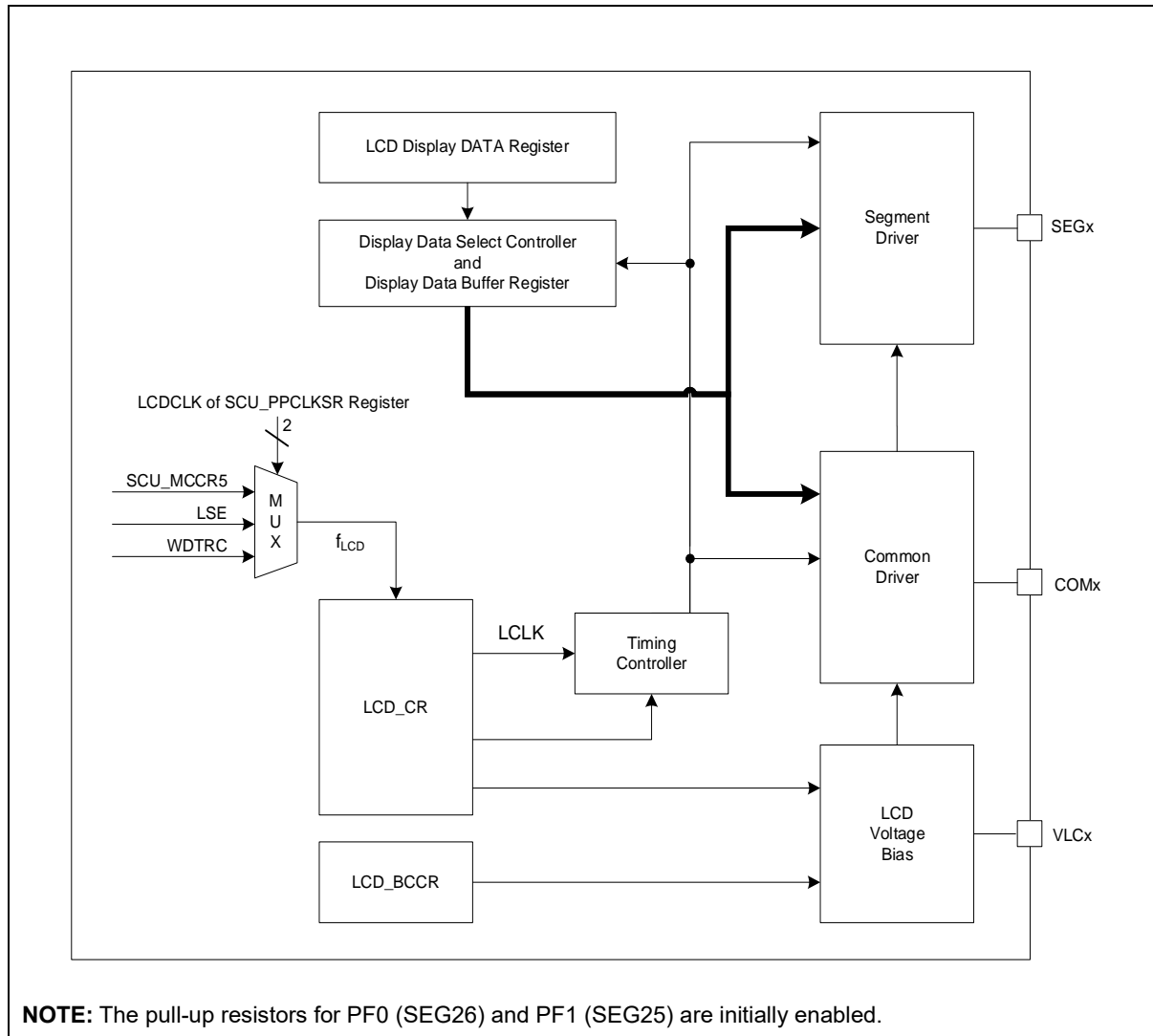
Table 22 introduces pins assigned for LCD Driver.

**Table 22. Pin Assignment of LCD Driver: External Signal**

Pin name	Type	Description
VLC0 to 3	A	LCD External Bias voltage input
COM0 to 7	O	LCD Common signal outputs
SEG0 to SEG31	O	LCD Segment signal outputs

### 19.1 LCD driver block diagram

Figure 39 shows a block diagram of LCD Driver.



**Figure 39. LCD Driver Block Diagram**



## 20 LED Driver

LED Driver has 13 ICOM / 16 ISEG output pins that are shared with Touch sensing pins. By configuring the LED control register 1 (LED\_CON1), users can decide whether to share pins with Touch sensing function.

The LED Driver consists of display data RAM memory, and the COM and SEG generator with the following features:

- ICOM0, ICOM1, ..., ICOM12 are shared with ISEG0, ISEG1, ..., ISEG12. It is selected by configuring the LED\_COMER register.
- ISEG13, ISEG14, and ISEG15 are dedicated only for the SEG function in LED function.
- ICOM and ISEG pins can be used as I/O pins.
- The LED\_COMOE and LED\_SEGOE registers are used to enable or disable each of ISEG0, ISEG1, ..., ISEG15 and ICOM0, ICOM1, ..., ICOM12.
- During the power-on reset, the reset pin, BOD reset or watchdog reset, and LED are turned off.
- The fPCLK is the PERI clock.

Table 23 introduces pins assigned for LED Driver.

**Table 23. Pin Assignment of LED Driver: External Signal**

Pin name	Type	Description
ICOM0 to ICOM12	O	LED Common signal outputs
ISEG0 to ISEG15	O	LED Segment signal outputs

### 20.1 LED Driver block diagram

Figure 40 shows a block diagram of LED Driver.

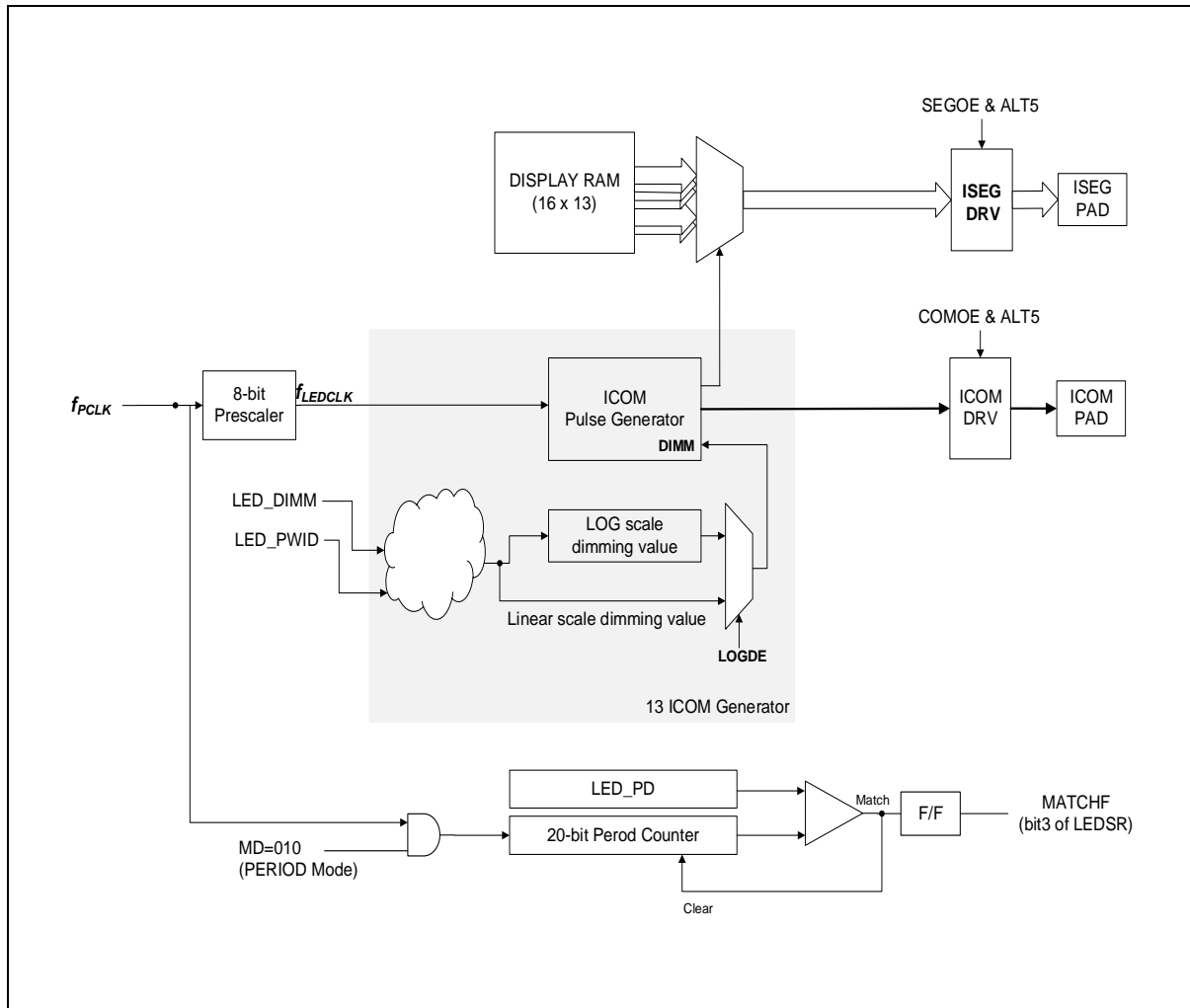


Figure 40. LED Driver Block Diagram

## 21 Cyclic Redundancy Check (CRC) and checksum

Cyclic redundancy check (CRC) generator is used to get a 16-bit CRC code from Flash ROM and a generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the functional safety standards, they offer a means of verifying the Flash memory integrity. CRC generator helps compute a signature of the software during runtime, to be compared with a reference signature.

CRC generator of A31T214/216 series features the followings:

- Auto CRC (DMA) and User CRC Mode.
- Polynomial:
  - CRC-CCITT ( $G_1(x) = x^{16} + x^{12} + x^5 + 1$ )
  - CRC-16 ( $G_2(x) = x^{16} + x^{15} + x^2 + 1$ )
- CRC Mode and Checksum Mode.

### 21.1 CRC and checksum block diagram

Figure 41 describes the CRC and checksum in a block diagram.

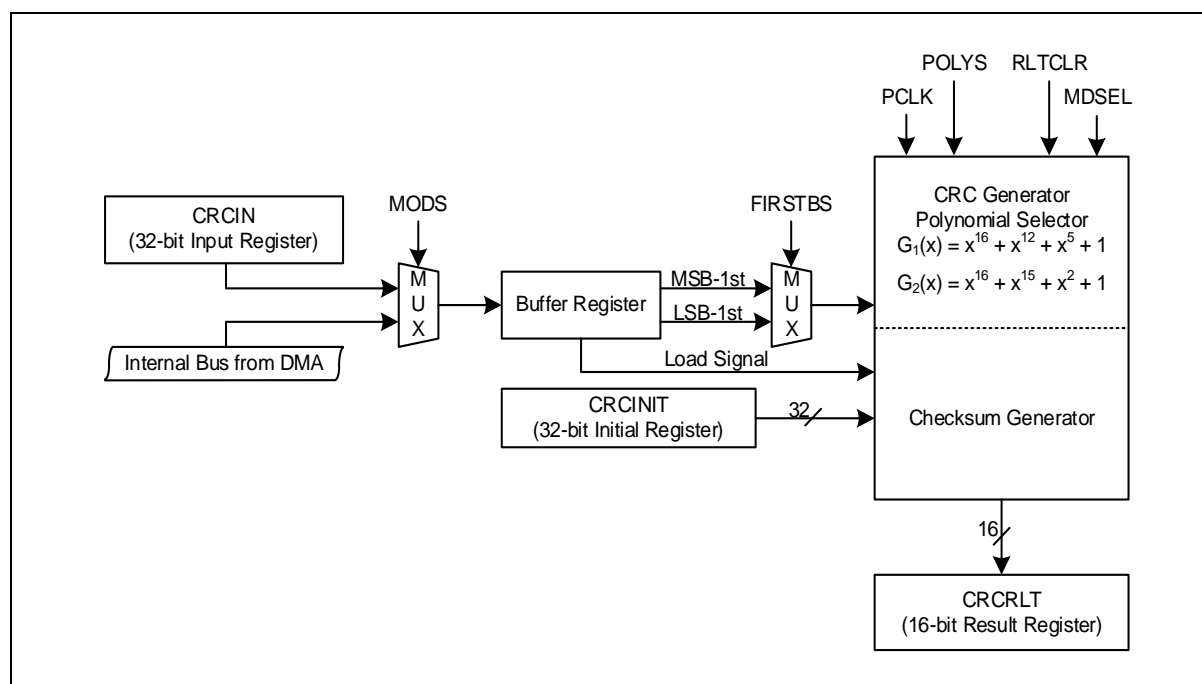


Figure 41. CRC and Checksum Block Diagram

## 22 Electrical characteristics

### 22.1 Absolute maximum ratings

Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions.

**Table 24. Absolute Maximum Rating**

Parameter	Symbol	Ratings	Unit	Remark
Supply voltage	$V_{DD}$	-0.3 – +6.5	V	—
Normal pin	$V_I$	-0.3 – $V_{DD}+0.3$	V	Voltage on any pin with respect to $V_{SS}$
	$V_O$	-0.3 – $V_{DD}+0.3$	V	
	$I_{OH}$	-20	mA	Maximum output current sourced by per I/O pin
	$\Sigma I_{OH}$	-100	mA	Total output current sourced by sum of all I/Os
	$I_{OL1}$	25	mA	Maximum output current sunk by per I/O pin
	$\Sigma I_{OL1}$	210	mA	Total output current sunk by sum of all I/Os
LED COM pin	$I_{OL2}$	250	mA	Maximum output current sunk by per LED COM pin
	$\Sigma I_{OL2}$	250	mA	Total output current sunk by sum of all LED COM
Total power dissipation	$T_P$	300	mW	—
Storage temperature	$T_{STG}$	-55 – +125	°C	—

## 22.2 Recommended operating conditions

**Table 25. Recommended Operating Condition**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V <sub>DD</sub>	Core and Peripherals	1.8	—	5.5	V
		ADC	2.4	—	5.5	V
		LED/LCD/TOUCH	2.7	—	5.5	V
		HSE	1.8	—	5.5	V
		LSE	2.7	—	5.5	V
Operating frequency	f <sub>OP</sub>	PLL	1	—	48	MHz
		HSE	1	—	16	MHz
		LSE	—	32.768	—	kHz
		HSI	31.52	32.00	32.48	MHz
		LSI	400	500	600	kHz
Operating temperature	T <sub>OP</sub>	Top	-40	+25	+105	°C
		TOUCH	-40	+25	+85	°C

## 22.3 POR (Power on Reset) characteristics

**Table 26. Operating Condition of POR**

Parameter	Symbol	Min	Typ.	Max	Units
Analog supply voltage	V <sub>DD</sub>	V <sub>SS</sub>	5.0	5.5	V
Operating Temperature	T <sub>A</sub>	-40	25	105	°C

**Table 27. POR Electrical Characteristics**

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
Operating current	I <sub>DD</sub>	—	-	0.5	4	uA
POR set level	V <sub>SET</sub>	—	1.20	1.40	1.60	V
POR reset level	V <sub>RESET</sub>	—	1.00	1.20	1.40	V
Supply rising rate	T <sub>rVDD</sub>		0.05	-	50	ms/V
Supply falling rate	T <sub>fVDD</sub>		-	-	2.5	ms/V

**NOTE:** The specifications of the parameters are guaranteed by design.

## 22.4 LVI (Low Voltage Indicator) LVR (Low Voltage Reset) characteristics

**Table 28. Operating Condition of Low Voltage Reset**

Parameter	Symbol	Min	Typ.	Max	Units
Operating temperature	T <sub>A</sub>	-40	25	105	°C

**Table 29. Low Voltage Indicator Characteristics**

Parameter	Symbol	Conditions	Min	Typ.	Max	Units	
Operating voltage	VDD		0.8	5.0	5.5	V	
Detection level	V <sub>LVI</sub>	Level0	Rising voltage	1.49	1.60	1.71	V
			Falling voltage	1.45	1.56	1.67	
		Level1	Rising voltage	1.62	1.74	1.86	
			Falling voltage	1.58	1.70	1.82	
		Level2	Rising voltage	1.70	1.83	1.96	
			Falling voltage	1.66	1.79	1.92	
		Level3	Rising voltage	1.83	1.96	2.09	
			Falling voltage	1.78	1.91	2.04	
		Level4	Rising voltage	1.92	2.06	2.20	
			Falling voltage	1.86	2.00	2.14	
		Level5	Rising voltage	2.04	2.19	2.34	
			Falling voltage	1.98	2.13	2.28	
		Level6	Rising voltage	2.21	2.37	2.53	
			Falling voltage	2.15	2.31	2.47	
		Level7	Rising voltage	2.37	2.54	2.71	
			Falling voltage	2.31	2.48	2.65	
		Level8	Rising voltage	2.56	2.75	2.94	
			Falling voltage	2.49	2.68	2.87	
		Level9	Rising voltage	2.91	3.13	3.35	
			Falling voltage	2.83	3.05	3.27	
		Level10	Rising voltage	3.05	3.28	3.51	
			Falling voltage	2.97	3.19	3.41	
		Level11	Rising voltage	3.45	3.70	3.95	
			Falling voltage	3.35	3.60	3.85	
		Level12	Rising voltage	3.58	3.84	4.10	
			Falling voltage	3.48	3.74	4.00	
		Level13	Rising voltage	3.86	4.15	4.44	
			Falling voltage	3.76	4.04	4.32	
		Level14	Rising voltage	4.03	4.33	4.63	
			Falling voltage	3.92	4.22	4.52	
Level15	Rising voltage	4.30	4.62	4.94			
	Falling voltage	4.18	4.50	4.82			

**Table 30. Low Voltage Reset Characteristics**

Parameter	Symbol	Conditions	Min	Typ.	Max	Units	
Operating voltage	VDD		0.8	5.0	5.5	V	
Detection level	V <sub>LVR</sub>	Level0	Rising voltage	1.49	1.60	1.71	V
			Falling voltage	1.45	1.56	1.67	
		Level1	Falling voltage	1.58	1.70	1.82	
		Level2	Falling voltage	1.66	1.79	1.92	
		Level3	Falling voltage	1.78	1.91	2.04	
		Level4	Falling voltage	1.86	2.00	2.14	
		Level5	Falling voltage	1.98	2.13	2.28	
		Level6	Falling voltage	2.15	2.31	2.47	
		Level7	Falling voltage	2.31	2.48	2.65	
		Level8	Falling voltage	2.49	2.68	2.87	
		Level9	Falling voltage	2.83	3.05	3.27	
		Level10	Falling voltage	2.97	3.19	3.41	
		Level11	Falling voltage	3.35	3.60	3.85	
		Level12	Falling voltage	3.48	3.74	4.00	
		Level13	Falling voltage	3.76	4.04	4.32	
		Level14	Falling voltage	3.92	4.22	4.52	
Level15	Falling voltage	4.18	4.50	4.82			

**Table 85. Low Voltage Reset Characteristics (continued)**

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
Noise cancelling time	—		—	2	-	us
Operation current	I <sub>DD</sub>		—	3.5	5	uA
Operation current(STOP)	I <sub>DD, STOP</sub>		—	2.5	3	nA

**NOTES:**

1. The specifications of the parameters are guaranteed by design.
2. To use LVR or LVI function while the system is in STOP mode (DEEP SLEEP mode), set SCU\_SMR <BGRON> to '1' to enable BGR function of VDC.



## 22.5 HSI (High Frequency Internal) RC oscillator characteristics

**Table 31. Operating Condition of HSI**

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	VDD	1.8	5.0	5.5	V
Operating temperature	T <sub>A</sub>	-40	25	105	°C

**Table 32. High Frequency Internal RC Oscillator Characteristics**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f <sub>HSI</sub>	V <sub>DD</sub> = 1.8V to 5.5V T <sub>A</sub> = -20 °C to +85 °C	31.68	32.0	32.32	MHz
Frequency	f <sub>HSI</sub>	V <sub>DD</sub> = 1.8V to 5.5V T <sub>A</sub> = -40 °C to +105 °C	31.52	32.0	32.48	MHz
Tolerance	-	T <sub>A</sub> = -20 °C to +85 °C	-1.0	-	1.0	%
		T <sub>A</sub> = -40 °C to +105 °C	-1.5	-	1.5	%
Clock duty ratio	T <sub>OD</sub>	-	-	50	-	%
Stabilization time	t <sub>HFS</sub>	-	100	-	-	us
IRC current	I <sub>HSI</sub>	Enable	-	300	350-	uA
		Disable	-	1	-	uA

**NOTE:** The specifications of the parameters are guaranteed by design.

## 22.6 LSI (Low Frequency Internal) RC oscillator characteristics

**Table 33. Operating Condition of LSI**

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	VDD	1.8	5.0	5.5	V
Operating temperature	T <sub>A</sub>	-40	25	105	°C

**Table 34. Low Frequency (500KHz) Internal RC Oscillator Characteristics**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating current	I <sub>LIRC</sub>	Enable	-	3.2	4.3	uA
		Disable	-	1	20	nA
Frequency	f <sub>LSI</sub>	V <sub>DD</sub> = 1.8V to 5.5V T <sub>A</sub> = -40 °C to +105 °C	400	500	600	kHz
Tolerance	-	V <sub>DD</sub> = 1.8V to 5.5V T <sub>A</sub> = -40 °C to +105 °C	-20	-	20	%

**NOTE:** The specifications of the parameters are guaranteed by design.

## 22.7 HSE (main oscillator) characteristics

**Table 35. Operating Condition of HSE**

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	VDD	1.8	5.0	5.5	V
Operating temperature	T <sub>A</sub>	-40	25	105	°C

**Table 36. Main Oscillator Characteristics**

Oscillator	Parameter	Conditions	Min	Typ.	Max	Units
Operating current	I <sub>DD</sub>	—	—	—	2.5	mA
Power down current	I <sub>STOP</sub>	—	—	0.2	30	nA
Output frequency	XOUT input frequency	VDDEXT ≥ 1.8V SCU_EOSCR < ISEL[1:0] ≥ 2'b11 SCU_EOSCR < NCOPT[1:0] ≥ 2'b00	1.0	—	4.0	MHz
		VDDEXT ≥ 2.0V SCU_EOSCR < ISEL[1:0] ≥ 2'b10 SCU_EOSCR < NCOPT[1:0] ≥ 2'b01	1.0	—	8.0	MHz
		VDDEXT ≥ 2.2V SCU_EOSCR < ISEL[1:0] ≥ 2'b01 SCU_EOSCR < NCOPT[1:0] ≥ 2'b10	1.0	—	12.0	MHz
		VDDEXT ≥ 2.4V SCU_EOSCR < ISEL[1:0] ≥ 2'b00 SCU_EOSCR < NCOPT[1:0] ≥ 2'b11	1.0	—	16	MHz
Start-up time	T <sub>start</sub>	—	—	2	—	ms
Crystal input (low)	V <sub>IL</sub>	—	—	—	0.2V DD	V
Crystal input (high)	V <sub>IH</sub>	—	—	—	0.8V DD	V
Crystal out (low)	V <sub>OL</sub>	—	—	—	0.2V DD	V
Crystal out (high)	V <sub>OH</sub>	—	—	—	0.8V DD	V
External load cap	C <sub>L</sub>	1M < f <sub>OUT</sub> < 4M	18	30	35	pf
		4M < f <sub>OUT</sub> < 12M	10	22	30	pf
		12M < f <sub>OUT</sub> < 16M	7	18	22	pf
Feedback resistance	R <sub>FB</sub>	VDDEXT = 5V	0.7	1.0	1.3	MΩ

**NOTE:** The specifications of the parameters are guaranteed by design.

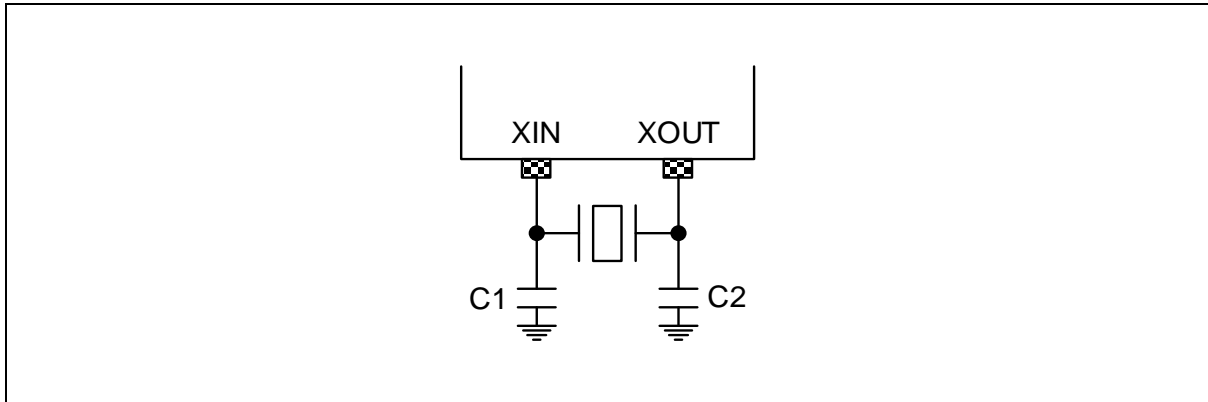


Figure 42. Crystal/Ceramic Oscillator

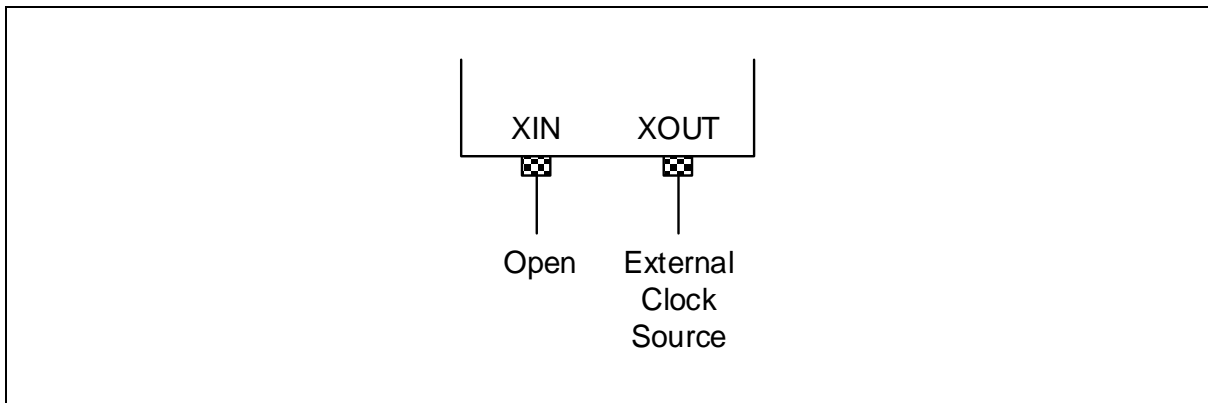


Figure 43. External Clock

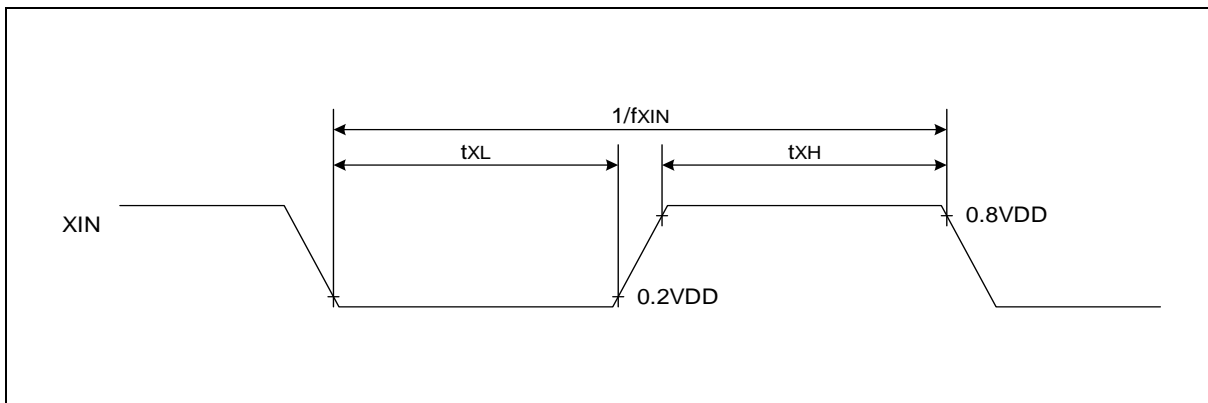


Figure 44. Clock Timing Measurement at XIN

## 22.8 LSE (sub oscillator) characteristics

Table 37. Operating Condition of LSE

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	$V_{DD}$	2.7	5.0	5.5	V
Operating temperature	$T_A$	-40	25	105	°C

Table 38. Sub Oscillator Characteristics

Oscillator	Parameter	Conditions	Min	Typ	Max	Units
Operating current	$I_{DD}$			-	5.0	uA
Power down current	$I_{STOP}$	—	—	0.2	15.0	nA
Output frequency	$f_{SUB}$	—	—	32.768	—	KHz
Start-up time	$T_{start}$	—	—	2	—	s
Crystal input (low)	$V_{IL}$	—	—	—	0.2VDD	V
Crystal input (High)	$V_{IH}$	—	0.8VDD	—	—	V
Crystal out (low)	$V_{OL}$	—	—	—	0.2VDD	V
Crystal out (high)	$V_{OH}$	—	0.8VDD	—	—	V
External load cap	$R_{FB}$	—	5	15	35	pF
Feedback resistance	$C_L$	—	7	12	24	MΩ

**NOTE:** The specifications of the parameters are guaranteed by design.

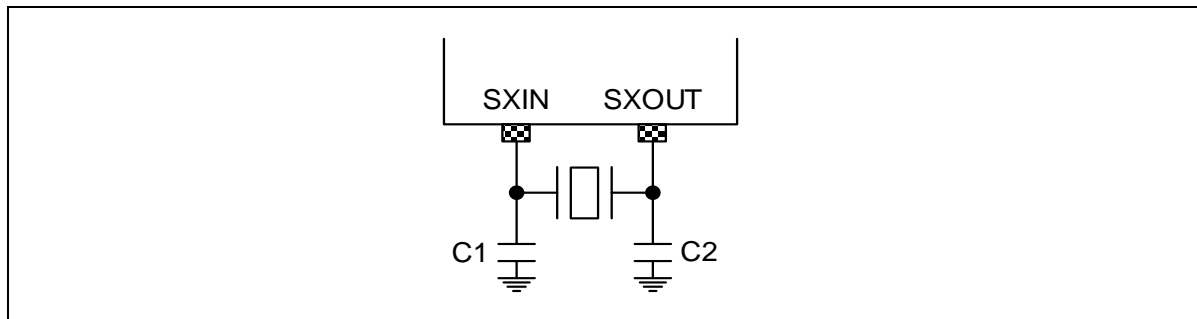


Figure 45. Crystal Oscillator

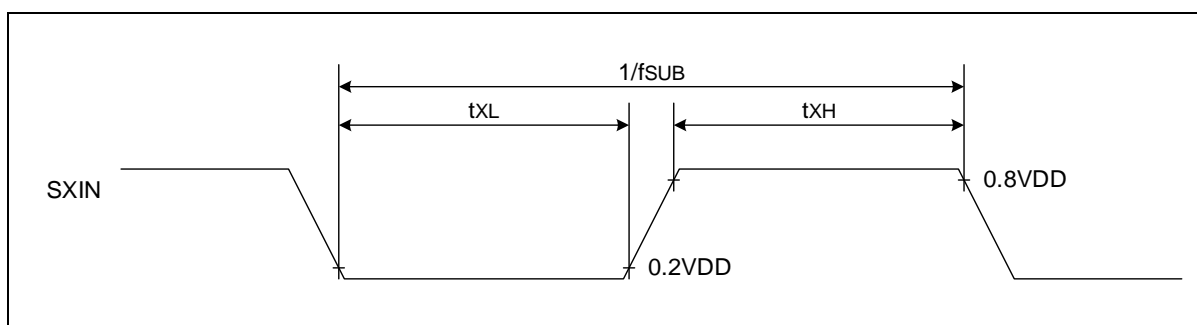


Figure 46. Clock Timing Measurement at SXIN

## 22.9 PLL electrical characteristics

**Table 39. Operating Condition of PLL**

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V <sub>DD</sub>	1.8	5.0	5.5	V
Operating temperature	T <sub>A</sub>	-40	25	105	°C

**Table 40. PLL Electrical Characteristics**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating current	I <sub>DD</sub>	Enable	—	—	1	mA
		Disable	—	5	500	nA
Output frequency	f <sub>OUT</sub>	—	1	—	48	MHz
Duty	f <sub>DUTY</sub>		40	—	60	%
VCO Frequency	f <sub>VCO</sub>		10	—	240	MHz
Frequency Peak-to-Peak Jitter	f <sub>JITTER(P-P)</sub>				500	ps
VCO Linear Range	f <sub>VCO_LIN</sub>		50	—	150	MHz
Input Frequency <sup>NOTE3</sup>	f <sub>PLLINCLK</sub>		4	8	16	MHz
Locking Time <sup>NOTE2</sup>	t <sub>LOCK</sub>		—	60	100	us
Input Bandwidth	f <sub>IN</sub>		—	2	—	MHz

**NOTES:**

1. The specifications of the parameters are guaranteed by design.
2. The tolerance of PLL output frequency is reflected based on PLL input clock source selected by PLLINCLKSEL in the SCU\_SCCR[2] register.
3. It is recommended to use 8MHz for input frequency.

## 22.10 Supply current characteristics

**Table 41. Operating Condition of Supply Current**

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V <sub>DD</sub>	1.8	5.0	5.5	V
Operating temperature	T <sub>A</sub>	-40	25	105	°C

**Table 42. Supply Current Characteristics**

Parameter	Symbol	Conditions	Min	Typ	Max	Units		
Supply current	I <sub>DD1</sub> (Run)	f <sub>PLL</sub> = 48MHz	VDD=5V±10% T <sub>A</sub> =25°C	-	9.0	12.0	mA	
		f <sub>HSI</sub> = 32MHz		-	6.0	8.0		
		f <sub>XIN</sub> = 8MHz		-	3.0	4.0		
		f <sub>LSI</sub> = 500KHz		All peripherals off	-	200	600	uA
		f <sub>LSE</sub> = 32.768KHz			-	140	300	
	I <sub>DD2</sub> (Sleep)	f <sub>PLL</sub> = 48MHz	VDD=5V±10% T <sub>A</sub> =25°C	-	6.0	10.0	mA	
		f <sub>HSI</sub> = 32MHz		-	4.0	7.0		
		f <sub>XIN</sub> = 8MHz		-	2	6		
		f <sub>LSI</sub> = 500KHz		All peripherals off	-	180	500	uA
		f <sub>LSE</sub> = 32.768KHz			-	130	400	
I <sub>DD3</sub> (Deep-Sleep) (STOP1)	WDTRC = ON, (LSIAON=ENABLE) <sup>NOTE4</sup> , LVD=ON	VDD=5V±10% T <sub>A</sub> =25°C	-	50	-	uA		
I <sub>DD4</sub> (Deep-Sleep) (STOP1)	WDTRC = ON, (LSIAON=ENABLE) <sup>NOTE4</sup> , LVD=OFF <sup>NOTE5</sup>	VDD=5V±10% T <sub>A</sub> =25°C	-	30	-	uA		
I <sub>DD5</sub> (Deep-Sleep) (STOP2)	WDTRC = OFF, LVD=ON	VDD=5V±10% T <sub>A</sub> =25°C	-	15	-	uA		
I <sub>DD6</sub> (Deep-Sleep) (STOP2)	WDTRC = OFF, LVD=OFF <sup>NOTE5</sup>	VDD=5V±10% T <sub>A</sub> =25°C	-	2	-	uA		

**NOTES:**

- The specifications of the parameters are guaranteed by design.
- All supply current items do not include the current of a low frequency internal RC oscillator and a peripheral block.
- All supply current items include the current of the power-on reset (POR) block.
- SCU\_SMR<LSIAON> bit must be enabled in order to use the WDT as a wake up source in deep-sleep mode(STOP1).
- 'LVD = OFF' indicates that LVR reset function , LVR block and LVI block are disabled.
  - LVRRST in SCU\_RSER = 0
  - LVREN[7:0] in SCULV\_LVRCR = 0x55 (LVREN=0)
  - LVRENM[7:0] in SCULV\_LVRCNFIG = 0xAA (LVRENM=0)
  - LVIEN in SCULV\_LVICR = 0

## 22.11 I/O port characteristics

**Table 43. Operating Condition of I/O Electrical Characteristics**

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V <sub>DD</sub>	1.8	5.0	5.5	V
Operating temperature	T <sub>A</sub>	-40	25	105	°C

### 22.11.1 General I/O characteristics

Parameters given in Table 44 for I/O static characteristics are derived from tests performed under the ambient temperature, and V<sub>DD</sub> supply voltage conditions summarized in Table 43.

**Table 44. I/O Static Characteristics**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output high voltage	V <sub>OH1</sub>	V <sub>DD</sub> =5V, I <sub>OH</sub> =-2.68mA All output ports <b>NOTE2</b>	0.8V <sub>DD</sub>	-	V <sub>DD</sub>	V
	V <sub>OH2</sub>	V <sub>DD</sub> =5V, I <sub>OH</sub> =-3.80mA All output ports <b>NOTE3</b>				
	V <sub>OH3</sub>	V <sub>DD</sub> =5V, I <sub>OH</sub> =-2.54mA All output ports <b>NOTE4</b>				
Output low voltage	V <sub>OL1</sub>	V <sub>DD</sub> =5V, I <sub>OL</sub> =3.68mA All output ports <b>NOTE2</b>	0	-	0.2V <sub>DD</sub>	V
	V <sub>OL2</sub>	V <sub>DD</sub> =5V, I <sub>OL</sub> =3.74mA All output ports <b>NOTE3</b>				
	V <sub>OL3</sub>	V <sub>DD</sub> =5V, I <sub>OL</sub> =3.74mA All output ports <b>NOTE4</b>				
ISEG output high voltage	V <sub>OHSEG0</sub>	V <sub>DD</sub> =5V, I <sub>OH</sub> = -8.66mA, T <sub>A</sub> =25°C	-	V <sub>DD</sub> - 0.5	-	V
	V <sub>OHSEG1</sub>	V <sub>DD</sub> =5V, I <sub>OH</sub> = -13.22mA, T <sub>A</sub> =25°C	-	V <sub>DD</sub> - 0.5	-	V
	V <sub>OHSEG2</sub>	V <sub>DD</sub> =5V, I <sub>OH</sub> = -19.49mA, T <sub>A</sub> =25°C	-	V <sub>DD</sub> - 0.5	-	V
	V <sub>OHSEG3</sub>	V <sub>DD</sub> =5V, I <sub>OH</sub> = -22.06mA, T <sub>A</sub> =25°C	-	V <sub>DD</sub> - 0.5	-	V
ISEG current matching <b>NOTE1</b>	I <sub>TOSEG</sub>	V <sub>DD</sub> =5V, V <sub>OH</sub> =4.5V, T <sub>A</sub> =25°C, V <sub>OHSEG1</sub>	-5	-	5	%
ICOM output low voltage	V <sub>OLCOM</sub>	V <sub>DD</sub> =5V, I <sub>OL</sub> =250mA, T <sub>A</sub> =25°C LED ICOM High sink current output	-	1.5	-	V
Input high voltage	V <sub>IH1</sub>	All Input ports	0.8*V <sub>DD</sub>	—	V <sub>DD</sub>	V
Input low voltage	V <sub>IL1</sub>	All Input ports	V <sub>GND</sub>	—	0.2*V <sub>DD</sub>	V
Input high leakage current	I <sub>IHLKG</sub>	All Input ports	—	—	1	uA

Input low leakage current	$I_{LLKG}$	All Input ports	-1	—	—	$\mu A$
Pull-up resistor	$R_{PU}$	All Input pins	25	50	100	$K\Omega$
Pull-down resistor	$R_{PD}$	All Input pins	25	50	100	$K\Omega$
I/O pin capacitance	$C_{IO}$	—	—	TBD	—	$pF$

**NOTES:**

1. The specifications of the parameters are guaranteed by design.
2. PA[0], PB[3], PC[8:5, 2:0], PE[12], PF[7:4]
3. PA[11:1], PB[11:4, 2:0], PE[11:8], PF[3:0]
4. PC[4:3], PD[5:0], PE[7:0]



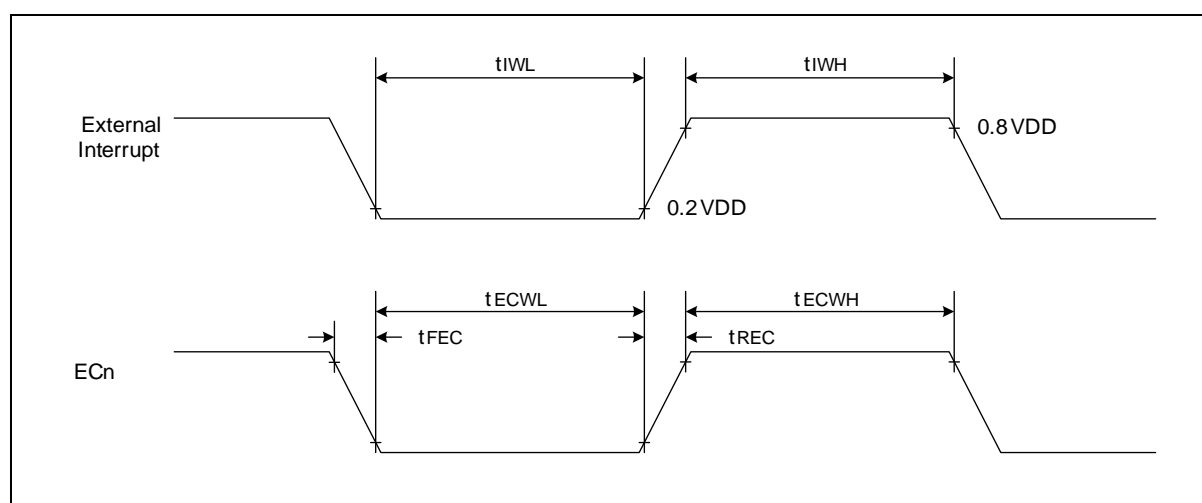
5. In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in **22.1 Absolute maximum ratings**.
  - The sum of the currents sourced by all the I/Os on VDD, plus the maximum run consumption of the MCU sourced on VDD, cannot exceed the absolute maximum rating  $\Sigma IOH$ .
  - The sum of the currents sunk by all the I/Os on VSS plus the maximum run consumption of the MCU sunk on VSS cannot exceed the absolute maximum rating  $\Sigma IOL$ .
6. SEG Current Matching represents  $(ISEGx - ISEGAVR) / ISEGAVR$ 
  - ISEGx: Output high current on each SEG pin ( $x = 0$  to 15)
  - ISEGAVR: Sum of ISEG0 to ISEG15

### 22.11.2 I/O AC characteristics

The definition and values of external input AC characteristics are given in Table 45 and Figure 47.

**Table 45. External Input AC Characteristics**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Interrupt input high low width	$t_{IWH}, t_{IWL}$	All external interrupts $1.8 V \leq V_{DD} \leq 5.5 V$ $-40^\circ C \leq T_A \leq 105^\circ C$	0.2	—	—	ns
External counter input high low pulse width	$t_{ECWH}, t_{ECWL}$	ECn, All external counter input $1.8 V \leq V_{DD} \leq 5.5 V$ $-40^\circ C \leq T_A \leq 105^\circ C$	100	—	—	
External counter transition time	$t_{REC}, t_{FEC}$	ECn, All external counter input $1.8 V \leq V_{DD} \leq 5.5 V$ $-40^\circ C \leq T_A \leq 105^\circ C$	—	—	20	



**Figure 47. Timing Diagram of External Input AC Characteristics Definitions**

## 22.12 UART characteristics

**Table 46. Operating Condition of UART**

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V <sub>DD</sub>	1.8	5.0	5.5	V
Operating temperature	T <sub>A</sub>	-40	25	105	°C

## 22.13 SPI characteristics

Parameters given in for SPI are derived from tests performed under the ambient temperature, and fPCLK frequency and VDD supply voltage conditions summarized in .

**Table 47. Operating Condition of SPIn (n = 20, 21)**

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V <sub>DD</sub>	1.8	5.0	5.5	V
Operating temperature	T <sub>A</sub>	-40	25	105	°C

**Table 48. SPIn Characteristics (n = 20, 21)**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
SPI clock frequency	f <sub>SCK1</sub>	SPI20, SPI21 V <sub>DD</sub> ≤ 1.8 V	—	—	5	MHz
	f <sub>SCK2</sub>	SPI20, SPI21 V <sub>DD</sub> ≤ 3.3 V	—	—	8	MHz
	f <sub>SCK3</sub>	SPI20, SPI21 V <sub>DD</sub> ≤ 5.5 V	—	—	10	MHz
Duty cycle of SPI frequency (SCK)	Duty	Slave mode	30	50	70	%
Capacitance load	C <sub>CL</sub>	—	—	—	TBD	pF

**NOTE:** The specifications of the parameters are guaranteed by design.

### 22.14 USART SPI characteristics

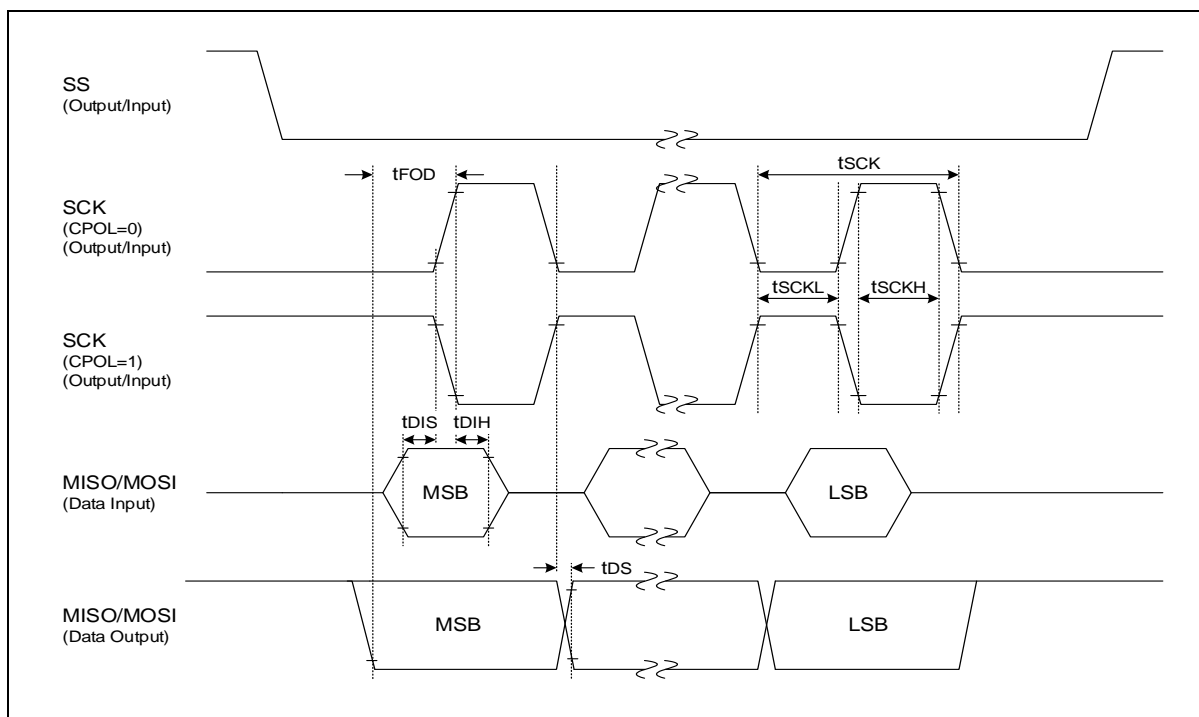
**Table 49. Operating Condition of USART SPI**

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V <sub>DD</sub>	1.8	5.0	5.5	V
Operating temperature	T <sub>A</sub>	-40	25	105	°C

**Table 50. USART SPI Characteristics**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output clock pulse period	tSCK	Internal SCK source	400	—	—	ns
Input clock pulse period		External SCK source	400	—	—	
Output clock high, low pulse width	tSCKH, tSCKL	Internal SCK source	180	—	—	
Input clock high, low pulse width		External SCK source	180	—	—	
First output clock delay time	tFOD	Internal/external SCK source	200	—	—	
Output clock delay time	tDS	—	—	—	100	
Input setup time	tDIS	—	180	—	—	
Input hold time	tDIH	—	180	—	—	

**NOTE:** The specifications of the parameters are guaranteed by design.



**Figure 48. SPI (USART) Timing Diagram**

### 22.15 USART UART timing characteristics

**Table 51. Operating Condition of USART UART**

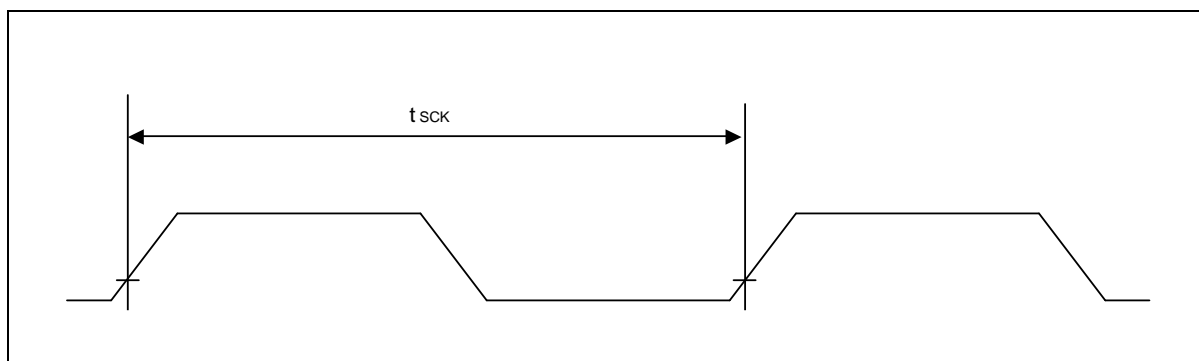
Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V <sub>DD</sub>	1.8	5.0	5.5	V
Operating temperature	T <sub>A</sub>	-40	25	105	°C

**Table 52. USART UART Timing Characteristics**

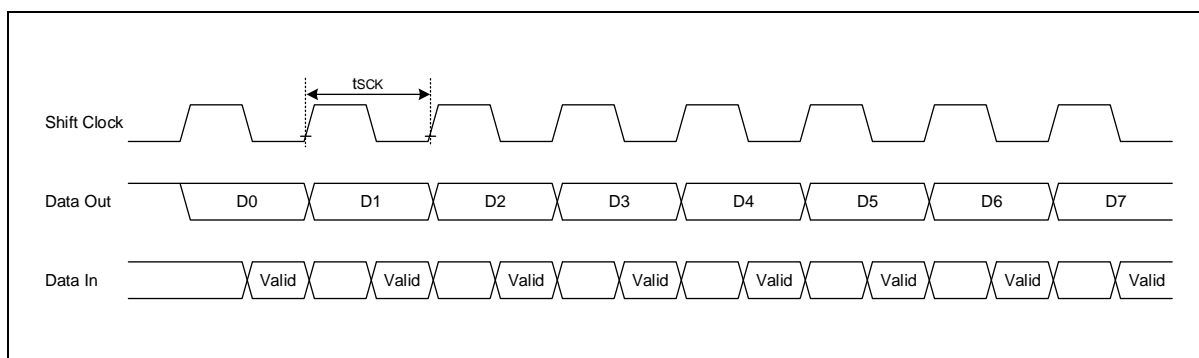
Parameter	Symbol	Typ	Units
Serial port clock cycle time	t <sub>SCK</sub>	t <sub>CPU</sub> x 16	us

**NOTE:** The specifications of the parameters are guaranteed by design.

- t<sub>CPU</sub> : BDR \* 2 \* (1/PCLK)



**Figure 49. Timing Diagram of UART Timing Characteristics**



**Figure 50. Timing Diagram of UART Module**

**NOTES:**

- t<sub>SCK</sub> : Board Rate

### 22.16 I2C characteristics

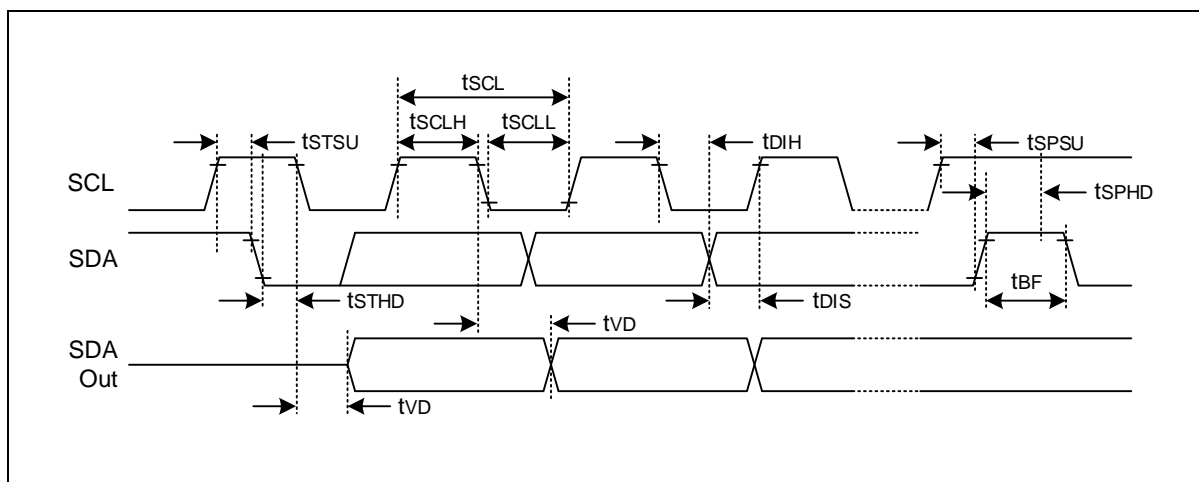
**Table 53. Operating Condition of I2C**

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V <sub>DD</sub>	1.8	5.0	5.5	V
Operating temperature	T <sub>A</sub>	-40	25	105	°C

**Table 54. I2C Characteristics**

Parameter	Symbol	Standard		Fast		Units
		Min	Max	Min	Max	
Clock frequency	t <sub>SCL</sub>	0	100	0	400	kHz
Clock high pulse width	t <sub>SCLH</sub>	4.0	—	0.6	—	
clock low pulse width	t <sub>SCLL</sub>	4.7	—	1.3	—	
Bus free time	t <sub>BF</sub>	4.7	—	1.3	—	
Start condition setup time	t <sub>STSU</sub>	4.7	—	0.6	—	
Start condition hold time	t <sub>STHD</sub>	4.0	—	0.6	—	
Stop condition setup time	t <sub>SPSU</sub>	4.0	—	0.6	—	
Stop condition hold time	t <sub>SPHD</sub>	4.0	—	0.6	—	
Output valid from clock	t <sub>VD</sub>	0	—	0	—	
Data input hold time	t <sub>DIH</sub>	0	—	0	1.0	
Data input setup time	t <sub>DIS</sub>	250	—	100	—	ns

**NOTE:** The specifications of the parameters are guaranteed by design.



**Figure 51. Timing Diagram of I2C Timing Characteristics**

## 22.17 Internal code flash characteristics

**Table 55. Operating Condition of Internal Code Flash**

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V <sub>DD</sub>	1.8	5.0	5.5	V
Operating temperature	T <sub>A</sub>	-40	25	105	°C

**Table 56. Internal Code Flash Characteristics**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Max. available clock frequency	-	0-wait	—	—	32	MHz
Reset Cycle Time	t <sub>RSTBUSY</sub>	—	5.6	8	10.4	us
Fuse Program Cycle Time	t <sub>FRDBUSY</sub>	—	4.2	6	7.8	us
Normal Program Cycle Time	t <sub>PGMBUSY</sub>	—	21	30	42	us
Normal Page Erase Cycle Time	t <sub>PERSBUSY</sub>	—	2.8	4	5.2	ms
Sector Erase Cycle Time	t <sub>SERSBUSY</sub>	—	2.8	4	5.2	ms
Chip Erase Cycle Time	t <sub>MERSBUSY</sub>	—	5.6	8	10.4	ms
Endurance of write/erase	N <sub>FWE</sub>	T <sub>A</sub> =25 °C, Page unit	10,000	—	—	Times
Retention time	t <sub>FRT</sub>	—	10	—	—	Years

**NOTE:** The specifications of the parameters are guaranteed by design.

## 22.18 ADC characteristics

**Table 57. Operating Condition of ADC**

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V <sub>DD</sub>	2.4	5.0	5.5	V
Operating temperature	T <sub>A</sub>	-40	25	105	°C

**NOTE:** If 12-bit ADC uses voltage of less than 2.4V, measurement error may be big. To avoid this, it is recommended to use voltage ranging from 2.4V to 5.5V for the ADC which is used for precision sensing of analog voltage.

**Table 58. ADC Electrical Characteristics**

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Resolution	—	—	—	—	12	Bit
Number of channel	—	—	—	15	—	CH
Analog input range	V <sub>IN</sub>	V <sub>AVREF</sub> =V <sub>DD</sub> V <sub>SS</sub> =V <sub>GND</sub>	V <sub>SS</sub>	—	AVREF	V
Operating current	I <sub>DD</sub>	V <sub>DD</sub> = 5V	—	1	2—	mA
Standby current	I <sub>ST</sub>	—	—	20	1500	nA
Differential nonlinearity	DNL	—	—	±1	±4	LSB
Integral nonlinearity	INL	T <sub>A</sub> = 25 °C	—	±4	±10	LSB
Top offset error (FSE)	TOE	—	—	±6	±12	LSB
Zero offset error	ZOE	—	—	±4	±8	LSB
Operating frequency	ACLK	—	—	—	4.5	MHz
Conversion frequency	f <sub>CONV</sub>	—	—	—	150	Ksps

**NOTE:** The specifications of the parameters are guaranteed by design.

## 22.19 LCD Driver characteristics

**Table 59. Operating Condition of LCD Driver**

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V <sub>DD</sub>	2.7	5.0	5.5	V
Operating temperature	T <sub>A</sub>	-40	25	105	°C

**Table 60. Comparator Characteristics**

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
LCD voltage	VLC0	LCD contrast = DISABLED, 1/4 bias	—	—	—	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 00H	Typ.x0.94	V <sub>DDX16/31</sub>	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 01H	Typ.x0.94	V <sub>DDX16/30</sub>	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 02H	Typ.x0.94	V <sub>DDX16/29</sub>	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 03H	Typ.x0.94	V <sub>DDX16/28</sub>	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 04H	Typ.x0.94	V <sub>DDX16/27</sub>	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 05H	Typ.x0.94	V <sub>DDX16/26</sub>	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 06H	Typ.x0.94	V <sub>DDX16/25</sub>	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 07H	Typ.x0.94	V <sub>DDX16/24</sub>	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 08H	Typ.x0.94	V <sub>DDX16/23</sub>	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 09H	Typ.x0.94	V <sub>DDX16/22</sub>	Typ.x1.06	V



Table 115. Comparator Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
LCD voltage	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0AH	Typ.x0.94	V <sub>DDX16/21</sub>	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0BH	Typ.x0.94	V <sub>DDX16/20</sub>	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0CH	Typ.x0.94	V <sub>DDX16/19</sub>	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0DH	Typ.x0.94	V <sub>DDX16/18</sub>	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0EH	Typ.x0.94	V <sub>DDX16/17</sub>	Typ.x1.06	V
	VLC0	LCD contrast = ENABLED, 1/4 bias, No panel load VLCD[3:0] = 0FH	Typ.x0.94	V <sub>DDX16/16</sub>	Typ.x1.06	V
LCD mid bias voltage <sup>NOTE 2</sup>	VLC1	V <sub>DD</sub> = 2.7V to 5.5V,	Typ-0.2	3/4xVLC0	Typ+0.2	V
	VLC2	LCD clock = 0Hz,	Typ-0.2	2/4xVLC0	Typ+0.2	
	VLC3	1/4 bias, No panel load	Typ-0.2	1/4xVLC0	Typ+0.2	
LCD Driver output impedance	RLO	VLCD=3.0V	–	5	10	kΩ
LCD bias dividing resistor	RLCD1	1/4 bias, T <sub>A</sub> = 25°C	7.5	10	12.5	kΩ
	RLCD2		38	50	62	
	RLCD3		60	80	100	
	RLCD4		180	240	300	

**NOTES:**

1. The specifications of the parameters are guaranteed by design.
2. It is middle output voltage when the VDD and the VLC0 node are connected.

## 22.20 Touch sensing characteristics

**Table 61. Operating Condition of Touch Sensing**

Parameter	Symbol	Min	Typ.	Max	Units
Operating voltage	V <sub>DD</sub>	2.7	5.0	5.5	V
Operating temperature	T <sub>A</sub>	-40	25	85	°C
VDD RIPPLE <sup>NOTE</sup>	V <sub>R_5V</sub>	-	-	±100	mV
	V <sub>R_3.3V</sub>	-	-	±100	mV

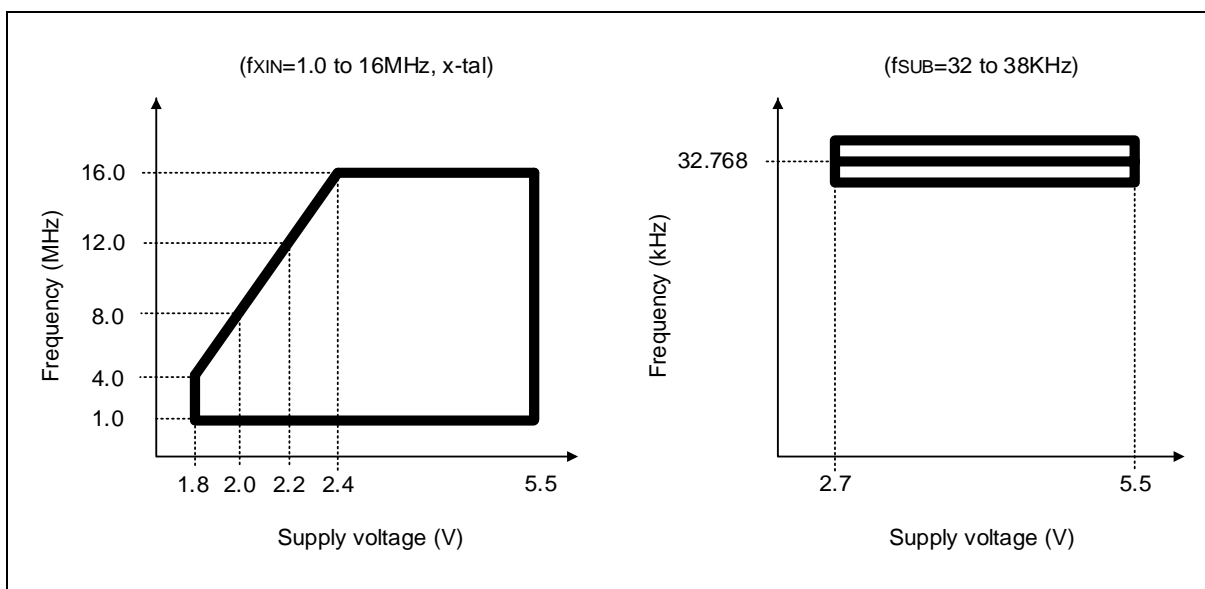
**NOTE:** The above values are experimental data and depend on the test conditions. (sensitivity, cover, board...)  
 - Test with A31T216 Start Kit Shield board. (9pi Touch stick Sensitivity on 2T Acrylic Cover)

**Table 62. Touch Sensing Characteristics**

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
Load capacitance	C <sub>load</sub>	-	—	50	100	pF
Operating frequency	F <sub>op</sub>	C <sub>load</sub> =50pF(@typ.) C <sub>load</sub> =100pF(@min.)	2	4	4	MHz
High-sense voltage	V <sub>HS</sub>	V <sub>DD</sub> =5V	2.6	3.5	5	V
COMP reference voltage	V <sub>COM</sub>	V <sub>DD</sub> =5V	2.6	3	3.5	V

**NOTE:** The specifications of the parameters are guaranteed by design.

## 22.21 Operating voltage range



**Figure 52. Operating Voltage Range**

### 22.22 Circuit design guide

Figure 53 shows a recommended circuit design.

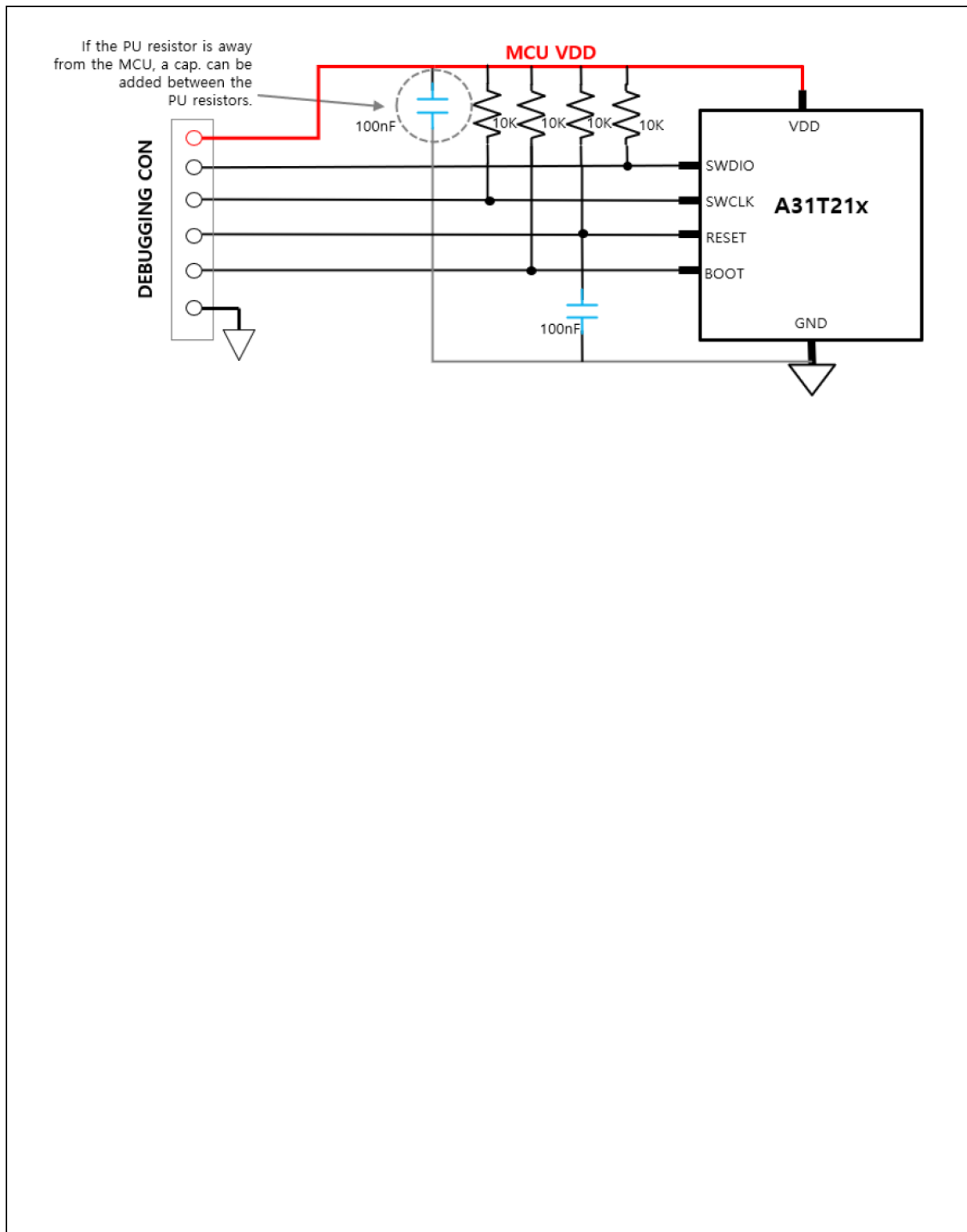


Figure 53. Circuit Design Guide for On-Board Programming

## 23 Package information

This chapter provides A31T214/216 series package information.

### 23.1 64 LQFP package information

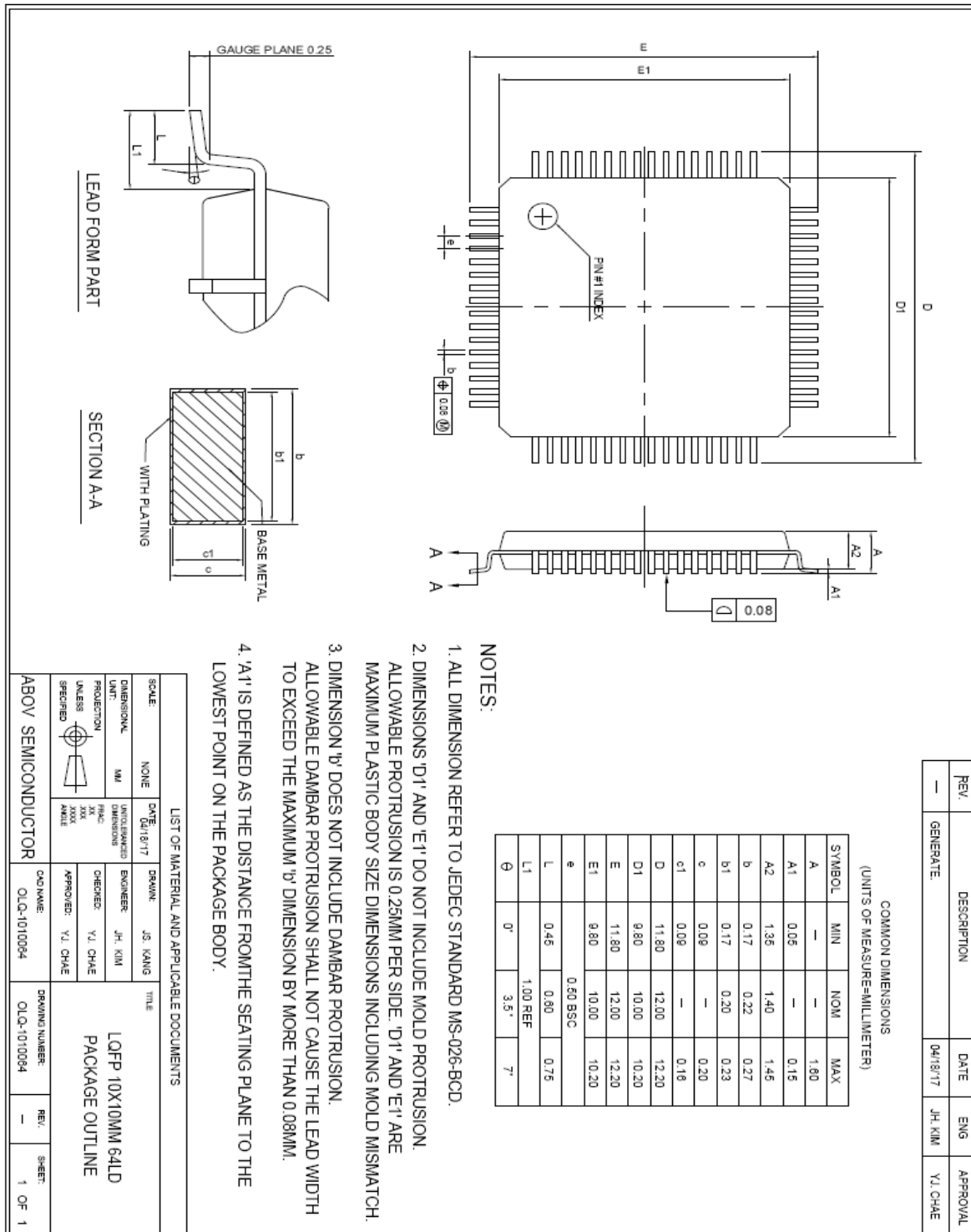


Figure 54. 64 LQFP Package Dimension

23.2 48 LQFP package information

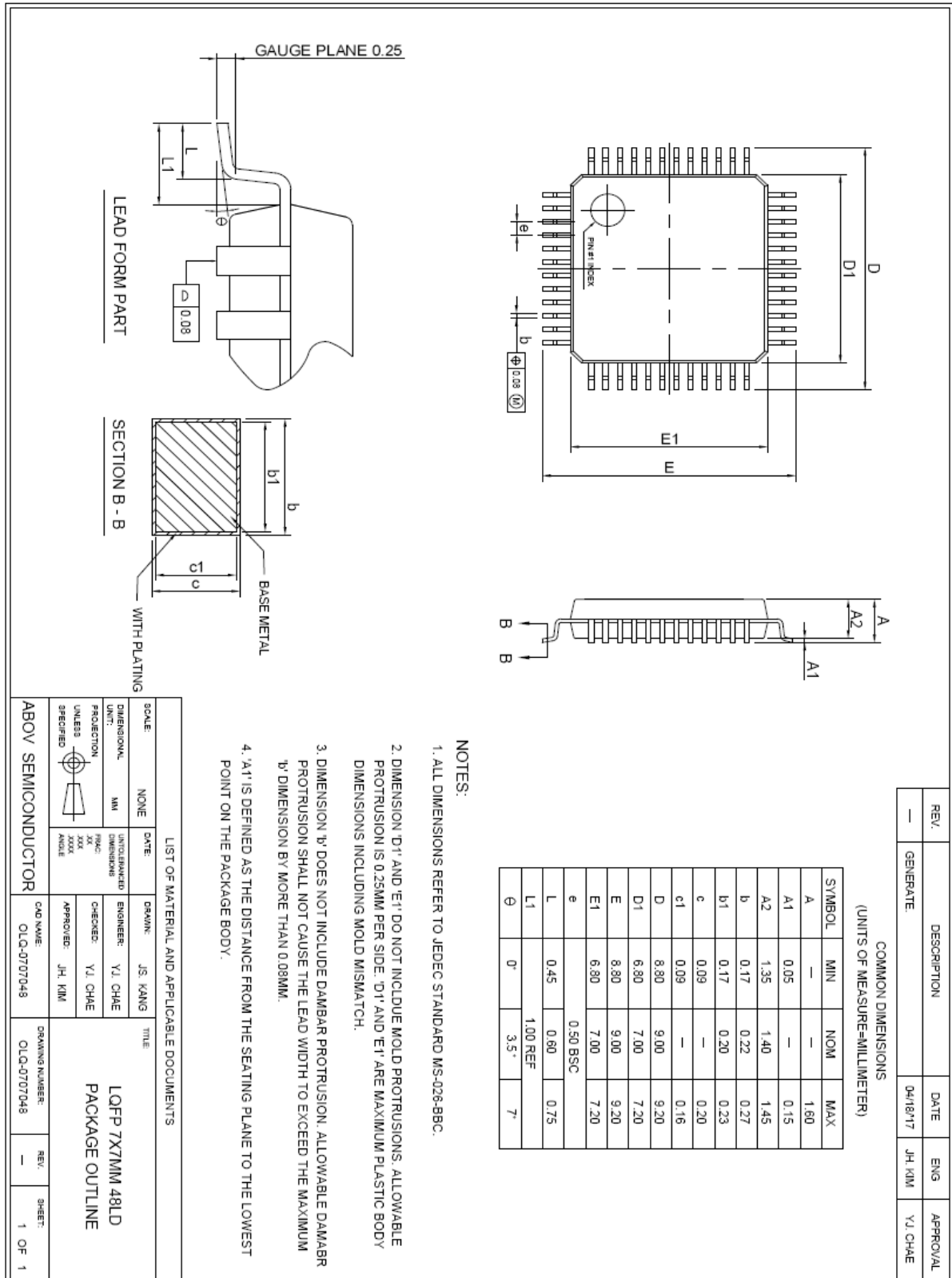


Figure 55. 48 LQFP Package Dimension

23.3 44 LQFP package information

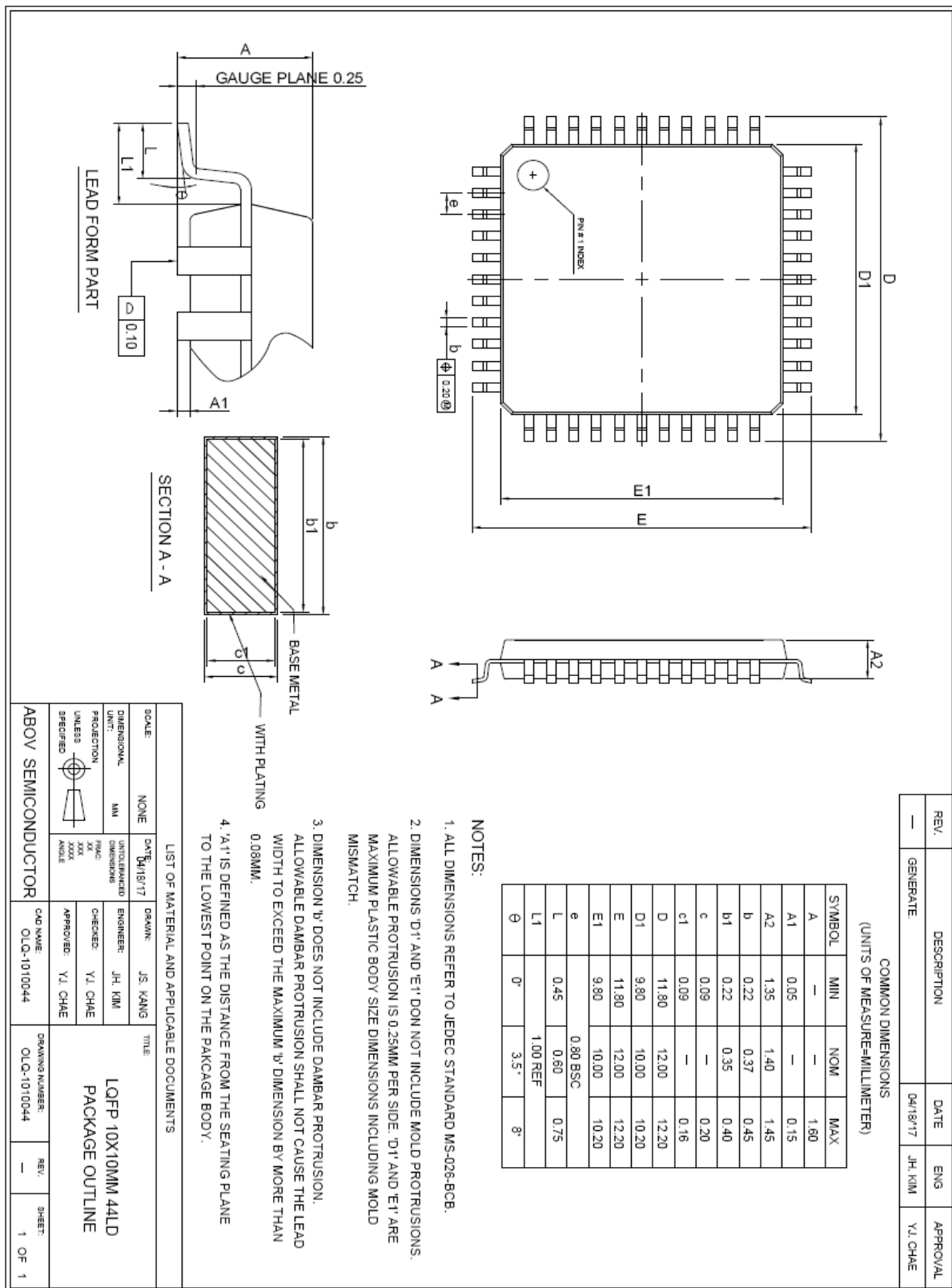


Figure 56. 44 LQFP Package Dimension

### 23.4 40 QFN package information

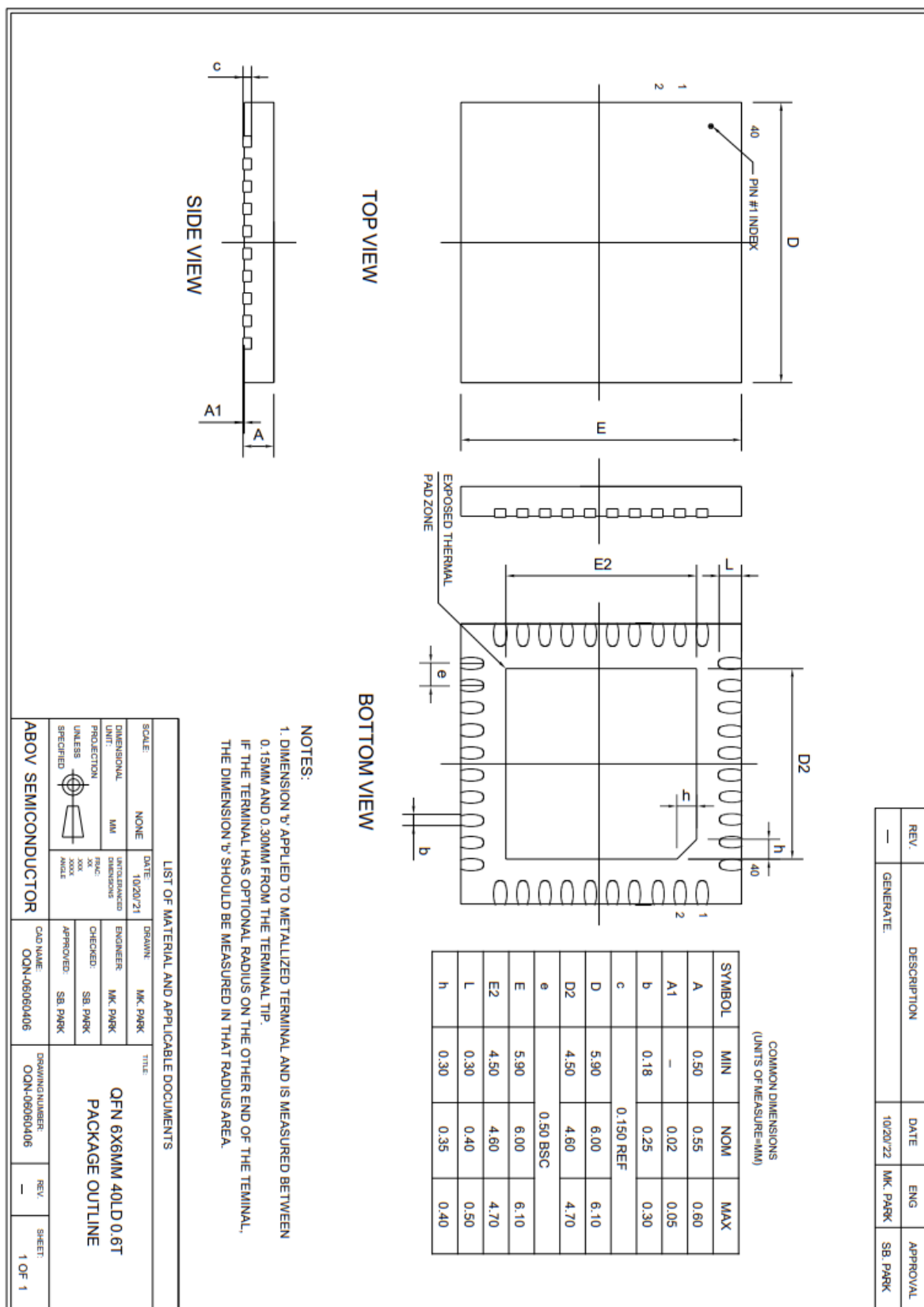


Figure 57. 40 QFN Package Dimension



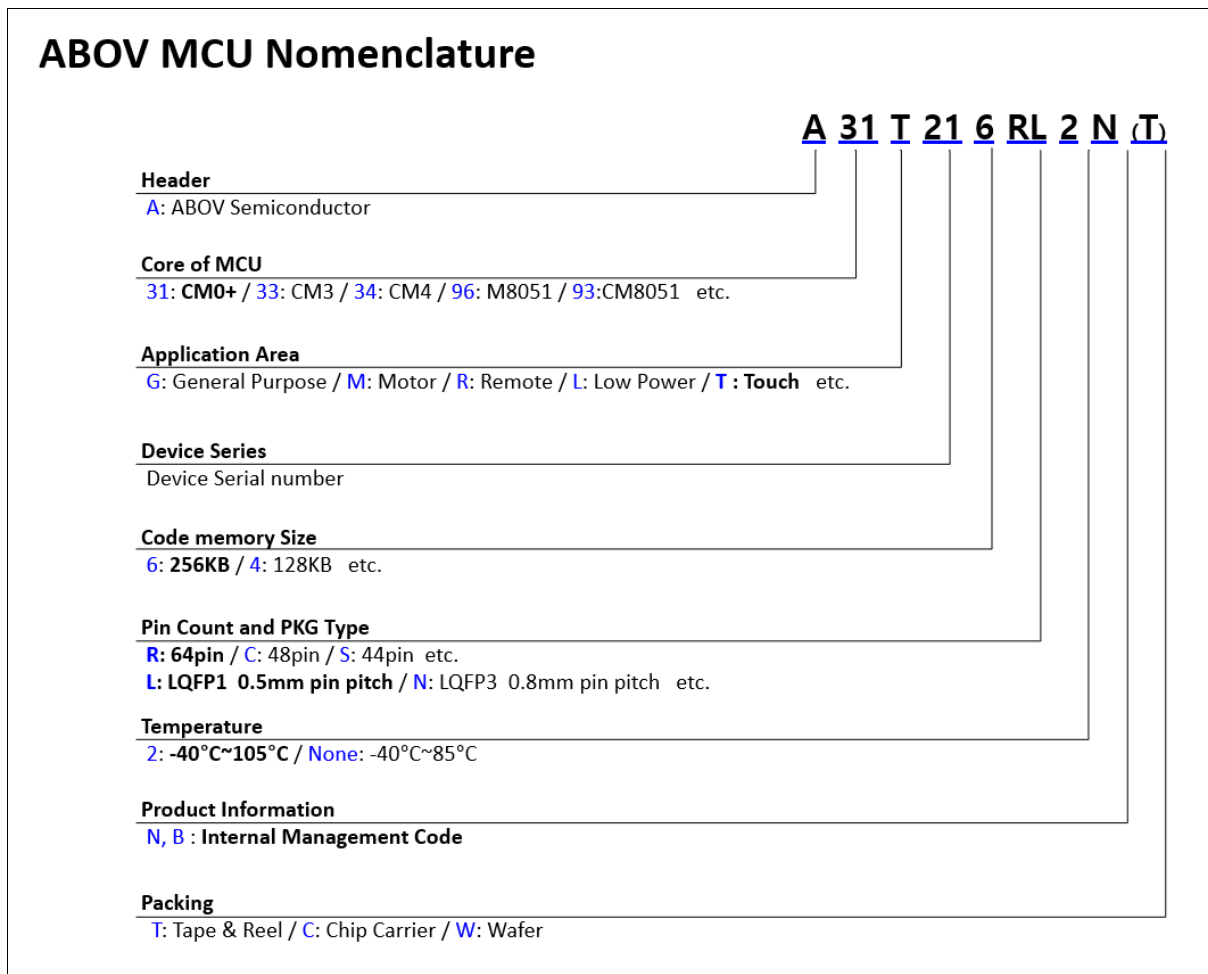


## 24 Ordering information

**Table 63. A31T214/216 Device Ordering Information**

Device name	Flash	SRAM	SPI	USART	I2C	Timer	PWM	ADC	I/O ports	Op. Temp.[°C]	Package
A31T216RLN	256KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	15-ch	60	-40~85	64-LQFP
A31T216CLN	256KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	11-ch	44	-40~85	48-LQFP
A31T216SNN	256KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	9-ch	40	-40~85	44-LQFP
A31T214RLN	128KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	15-ch	60	-40~85	64-LQFP
A31T214CLN	128KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	11-ch	44	-40~85	48-LQFP
A31T214SNN	128KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	9-ch	40	-40~85	44-LQFP
A31T214IUN	128KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	9-ch	38	-40~85	40-QFN
A31T216RL2N*	256KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	15-ch	60	-40~105	64-LQFP
A31T216CL2N*	256KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	11-ch	44	-40~105	48-LQFP
A31T216SN2N*	256KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	9-ch	40	-40~105	44-LQFP
A31T214RL2N*	128KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	15-ch	60	-40~105	64-LQFP
A31T214CL2N*	128KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	11-ch	44	-40~105	48-LQFP
A31T214SN2N*	128KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	9-ch	40	-40~105	44-LQFP
A31T214IU2N	128KB	16KB	2-ch	2-ch	2-ch	16-bit (4-ch) 32-bit (2-ch)	6-ch	9-ch	38	-40~105	40-QFN

\* For available options or further information on the devices with “\*” marks, please contact the ABOV sales offices.



**Figure 58. A31T214/216 Device Numbering Nomenclature**

## 25 Development tools

This chapter introduces wide range of development tools for A31T214/216. ABOV offers software tools, debuggers, and programmers to help a user in generating right results to match target applications. ABOV supports entire development ecosystem of the customers.

### 25.1 Compiler

ABOV semiconductor does not provide any compiler for A31T214/216. However, since A31T214/216 have ARM's high-speed 32-bit Cortex-M0+ Cores for their CPU, you can use all kinds of third party's standard compiler such as Keil C Compiler. These compilers' output debug information can be integrated with our A-Link and A-Link Pro. Please visit our website [www.abovsemi.com](http://www.abovsemi.com) for more information regarding the A-Link and A-Link Pro.

## 25.2 Debugger

The A-Link and A-Link Pro support ABOV Semiconductor's A31T214/216 MCU emulation in SWD Interface. The A-Link and A-Link Pro use two wires interfacing between PC and MCU, which is attached to user's system. The A-Link and A-Link Pro can read or change the value of MCU's internal memory and I/O peripherals. In addition, the A-Link and A-Link Pro control MCU's internal debugging logic. This means A-Link and A-Link Pro control emulation, step run, monitoring and many more functions regarding debugging.

The A-Link and A-Link Pro run underneath MS operating system such as MS-Windows NT/ 2000/ XP/ Vista/ 7/ 8/ 8.1/ 10 (32-bit, 64-bit).

Programming information using the A-Link and A-Link Pro are provided in Figure 59. More detailed information about the A-Link and A-Link Pro, please visit our website [www.abovsemi.com](http://www.abovsemi.com) and download the debugger S/W and documents.

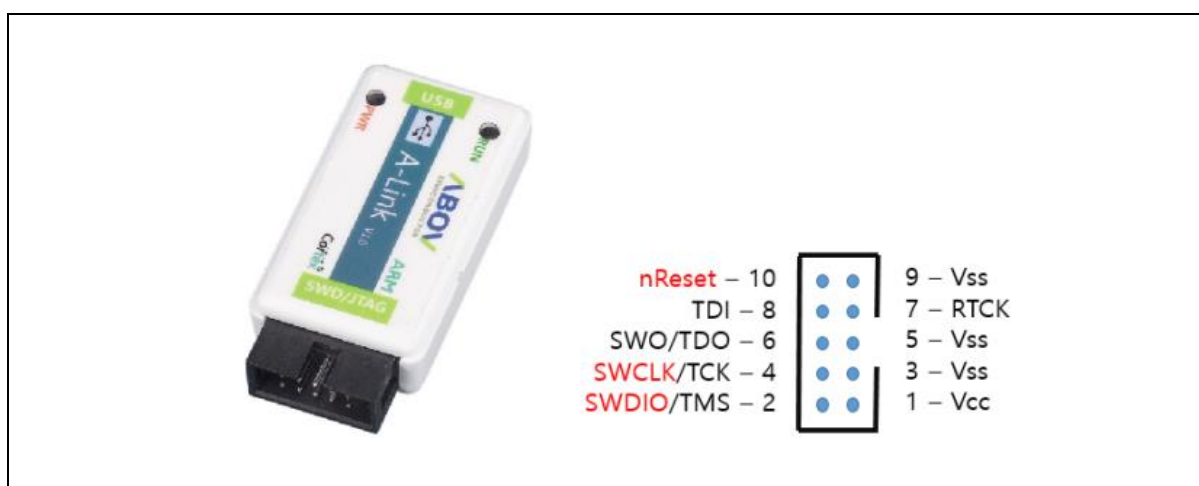


Figure 59. A-Link and Pin Descriptions

## 25.3 Programmer

### 25.3.1 E-PGM+

E-PGM+ is a single programmer, and allows a user to program on the device directly.

- Support ABOV devices
- 2 to 5 times faster than S-PGM+
- Main controller: 32-bit MCU @ 72MHz
- Buffer memory: 1MB

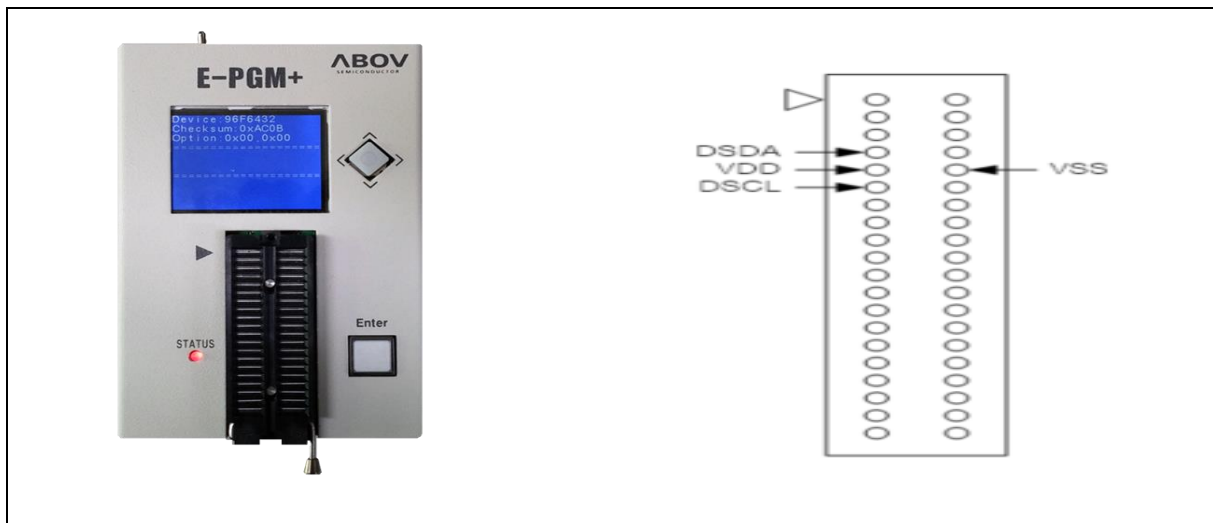


Figure 60. E-PGM+ (Single Writer) and Pin Descriptions

### 25.3.2 Gang programmer

E-Gang4 and E-Gang6 allows a user to program on multiple devices at a time. They run not only in PC controlled mode but also in standalone mode without PC control. USB interface is available and it is easy to connect to the handler.



Figure 61. E-Gang4 and E-Gang6 (for Mass Production)

## Revision history

Revision	Date	Notes
1.00	2021-10-28	Document Created
1.01	2021-11-25	Modify LCD block diagram
1.02	2021-12-20	Modified The start-up time of HSE Characteristics from Typ. 200 ms to Typ. 2 ms. Modified Stabilization time of HSI characteristics from Max. 100 us to Min. 100 us. Added the notifications to Figure 38
1.03	2022-05-30	Modified incorrect device name.
1.04	2022-06-21	Modified $t_{IWH}$ , $t_{IWL}$ specs in Table 45. External Input AC Characteristics.
1.05	2022-07-15	Updated Table <Operating Condition of Touch Sensing>.
1.06	2022-12-12	Updated font style of this document Changed LED COM / SEG notation. (Change to ICOM/ISEG) Added 40-QFN Package information. Changed LCD COM / SEG notation.
1.07	2023-02-15	Change UART Spec
1.08	2023-03-15	Incorrect content has been corrected in the Package Description section.

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