Ultra-Low Power Cortex-M0+ Microcontroller
Flash 32/16KB, SRAM 4KB, ADC, Temperature Sensor

DS Rev. 1.00

Features

- High performance Cortex-M0+ core
- 32/16KB Flash memory
- 4KB SRAM, 32-byte backup register
- Watchdog Timer, Real Time Clock and Calendar
- Five general purpose timers
  - Periodic, one-shot, PWM, capture
- 12-bit ADC, 8-channel, 0.5Msps, down to 1.71V
- Temperature Sensor
- Two comparators, down to 1.71V
- External communication ports
  - 1 x USART, 1 x UART, 1 x LPUART
  - 1 x I2C up to 1Mbps
  - 1 x SPI up to 16Mbps
- Clock monitoring function for system clock
- 8/16/32-bit CRC unit, 128-bit unique ID
- SWD debug interface
- USART (UART) ISP supported
- Ultra-low power tech
  - 1.71V to 3.6V Supply voltage
  - 78uA/MHz in RUN mode
  - 10uA in RUN mode (32.768kHz, 40kHz)
  - 0.99uA DEEP SLEEP + RTCC + retention
  - 0.3uA DEEP SLEEP with power control
  - 36nA SHUT DOWN (DEEP SLEEP mode 3)
  - 5us wakeup time from power modes
- Three types of package options
  - TSSOP 20
  - QFN 20
  - TSSOP 16
- Operating temperature, -40℃ to +105℃
  - Commercial and Industrial grade

Applications

- RF Module – NB-IoT
- Detector – Gas/Alarm
- IoT/Handheld device

Product selection table

Table 1. Device Summary

Part Number	Flash	SRAM	USART	UART	LPUART	I2C	SPI	TIMER	ADC	I/O	Package
A31L222FR	32KB	4KB	1	1	1	1	1	5	8ch	17	20TSSOP
A31L222FU*	32KB	4KB	1	1	1	1	1	5	8ch	17	20QFN
A31L222AR*	32KB	4KB	1	1	1	1	1	4	6ch	13	16TSSOP
A31L221FR*	16KB	4KB	1	1	1	1	1	5	8ch	17	20TSSOP
A31L221FU*	16KB	4KB	1	1	1	1	1	5	8ch	17	20QFN
A31L221AR*	16KB	4KB	1	1	1	1	1	4	6ch	13	16TSSOP

* For available options or further information on the devices with "*" marks, please contact the ABOV sales offices.

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1 Description

The A31L22x series is an ultra-low power microcontroller based on the high-performance ARM Cortex-M0+ core.

It has a Flash memory of up to 32KB, and an SRAM of 4KB. Operation voltage of the device is from 1.71V to 3.6V. It provides a highly flexible and cost-effective solution for many embedded control applications.

This device offers 16-bit timers, Real timer and calendar, 12-bit ADC, Comparator, CRC generator, UART, USART, LPUART, I2C, SPI, etc. The A31L22x series also has a POR, LVR, LVI, and an internal RC oscillator.

The A31L22x series supports SLEEP mode and DEEP SLEEP mode to reduce power consumption, and these power saving modes allow the design of low power applications.

1.1 Device overview

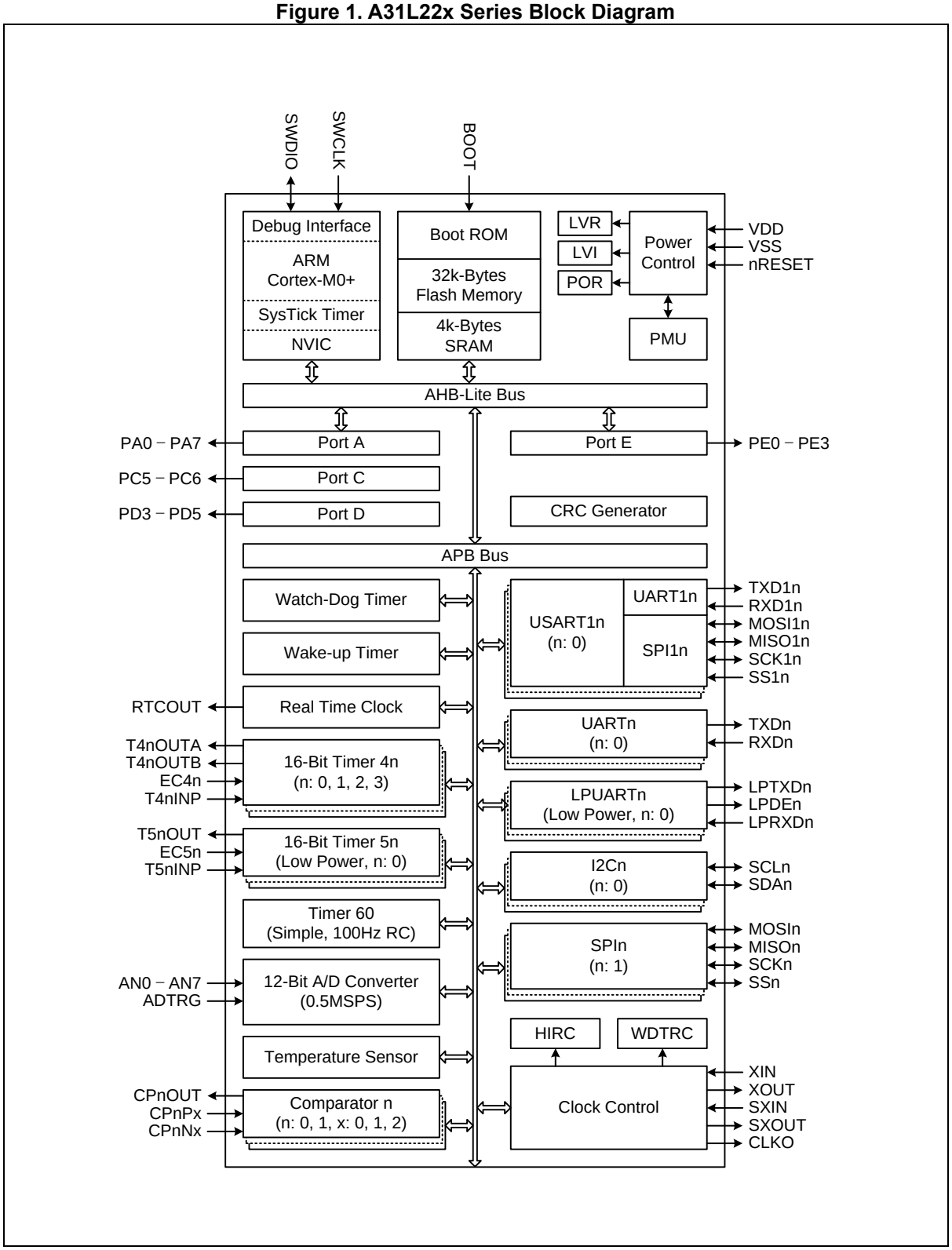
Table 2. A31L22x Series Features and Peripheral Counts

Peripheral	Description
CPU	Cortex-M0+
Memory	• Flash memory: 32/16 Kbytes • SRAM: 4 Kbytes, 32-byte backup register
I/O	17 programmable
Timers	• Watchdog Timer, Real time clock and calendar • Four general purpose timers and one low power timer — Periodic, one-shot, PWM, capture mode
ADC	8-channel input, 12-bit ADC with 0.5Msps, down to 1.71V
Comparator	Two comparators, down to 1.71V
Temperature sensor	Frequency variation: 3.2 kHz/℃
CRC generator	8/16/32-bit CRC generator, CRC-8/16/32, CRC-CCITT
External communication ports	• 1 USART (UART + SPI), 1 UART • 1 LPUART, up to 9600bps with 32.768kHz • 1 I^2C up to 1Mbps, 1 SPI up to 16Mbps
128-bit Unique ID	Supported
System fail-safe function	Clock monitoring
Debug interface	SWD debug interface
Ultra-low power tech	• 1.71V to 3.6V supply voltage • 78uA/MHz in RUN mode, 10uA in RUN mode (32.768kHz, 40kHz) • 0.99uA DEEP SLEEP + RTCC + SRAM retention • 0.3uA DEEP SLEEP with power control • 36nA SHUT DOWN (DEEP SLEEP mode 3) • 5us wakeup time from all power modes
Packages	• TSSOP 20 (0.65mm pitch) • QFN 20 (0.5mm pitch) • TSSOP 16 (0.65mm pitch)
Operating temperature	-40℃ to +85℃ (commercial grade)
	-40℃ to +105℃ (industrial grade)

1.2 Block diagram

Figure 1 shows a block diagram of the A31L22x series.

Figure 1. A31L22x Series Block Diagram



1.3 Functional description

The following sections provide a brief description of the features of the A31L22x series microcontroller.

1.3.1 ARM Cortex-M0+

The Cortex-M0+ processor has a very low gate count. It is a highly energy efficient processor for microcontrollers and deeply embedded applications that require an area-optimized, low-power processor.

In the core, the system timer (SYSTICK) provides a simple 24-bit timer that can be used as a real time operating system (RTOS) or as a simple counter.

The processor implements the ARMv6-M Thumb instruction set including a number of 32-bit instructions, which are introduced with Thumb-2 technology. Hardware single-cycle multiplication is available.

Integrated Nested Vectored Interrupt Controller (NVIC) provides deterministic interrupt handling.

It also supports SWD debugging features.

1.3.2 Nested Vector-Interrupt Controller (NVIC)

External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt.

The NVIC embedded in the Cortex-M0+ processor core achieves low latency interrupts processing and efficient processing of late arriving interrupts.

All NVIC registers can only be accessed through word transfers.

1.3.3 32KB Internal Flash memory

The A31L22x series has built-in 32KB Flash memory.

It supports self-programming feature. In addition, ISP and JTAG programming in boot or debug mode are supported.

1.3.4 4KB Internal SRAM

On-chip 4KB SRAM is used as a working memory space and as a program code area temporarily.

1.3.5 Boot logic

A boot logic supports Flash programming. The boot logic is activated when the external boot pin is set to boot mode.

1.3.6 System Control Unit (SCU)

An SCU block manages internal power, clock, reset and operation mode. It also controls the analog blocks (Oscillator block, VDC and LVR).

1.3.7 Power Management Unit (PMU)

A PMU block manages power of internal core, Code Flash, SRAM, logic, and peripheral blocks in RUN, SLEEP, and DEEP SLEEP modes.

It also controls the wake-up time from SLEEP and DEEP SLEEP modes.

1.3.8 24-bit Watchdog Timer (WDT)

A Watchdog Timer monitors the system. It generates internal resets or interrupts to detect abnormal status of the system.

1.3.9 Multi-purpose 16-bit timer

Four-channel 16-bit timers and one-channel low power general-purposed 16-bit timer support the functions introduced below:

- Periodic timer mode
- Counter mode
- PWM mode
- Capture mode

1.3.10 Real Time Clock and Calendar (RTCC)

A real time clock and a calendar can run in SLEEP and DEEP SLEEP modes. The RTCC is not reset by a system reset except in the event of a power-on reset.

1.3.11 USART (UART and SPI)

USART supports UART and SPI modes. The A31L22x series has 1 channel USART module.

Boot mode uses this USART10 block to download Flash program.

1.3.12 Inter-Integrated Circuit interface (I2C)

The A31L22x series has one channel of I2C block and supports up to 1MHz I2C communication.

Master and slave modes are available.

1.3.13 Serial Peripheral Interface (SPI)

The A31L22x series has one channel of SPI block and supports up to 16MHz communication.

Master and slave modes are available.

1.3.14 Universal Asynchronous Receiver/Transmitter (UART)

The A31L22x series has one channel of UART block.

For accurate baud rate control, a fractional baud-rate generation feature is supported.

1.3.15 Low Power Universal Asynchronous Receiver/Transmitter (LPUART)

The A31L22x series has one channel of Low Power UART block. This LPUART is available at 32.768kHz sub oscillator with up to 9600bps.

1.3.16 General PORT I/Os

8-bit PA port, 2-bit PC port, 3-bit PD port, and 4-bit PE port are available and provide multiple functions.

- General I/O port
- External interrupt input port and on-chip input debounce filter
- Programmable pull-up, pull-down, and open-drain selection

1.3.17 12-bit Analog-to-Digital Converter (ADC)

ADC of the A31L22x series can convert analog signals to digital signals at a conversion rate of up to 0.5Msps. 12-channel analog MUX provides various combinations of data from external and internal analog signals.

1.3.18 Comparator

The A31L22x series has two comparator blocks. The block has an internal reference for channel.

1.3.19 Cyclic Redundancy Check (CRC) generator

The A31L22x series has four polynomials for the CRC generator: CRC-CCITT and CRC-8/-16/-32.

1.3.20 Temperature Sensor (TS)

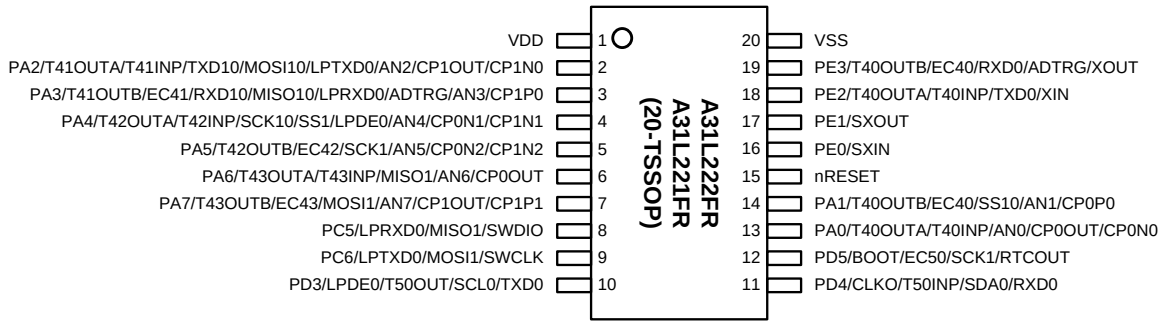
The temperature sensor consists of a ring-oscillator. Its frequency varies with temperature.

2 Pinouts and pin descriptions

In chapter 2, pinouts and pin descriptions of the A31L22x series are introduced.

2.1 Pinouts

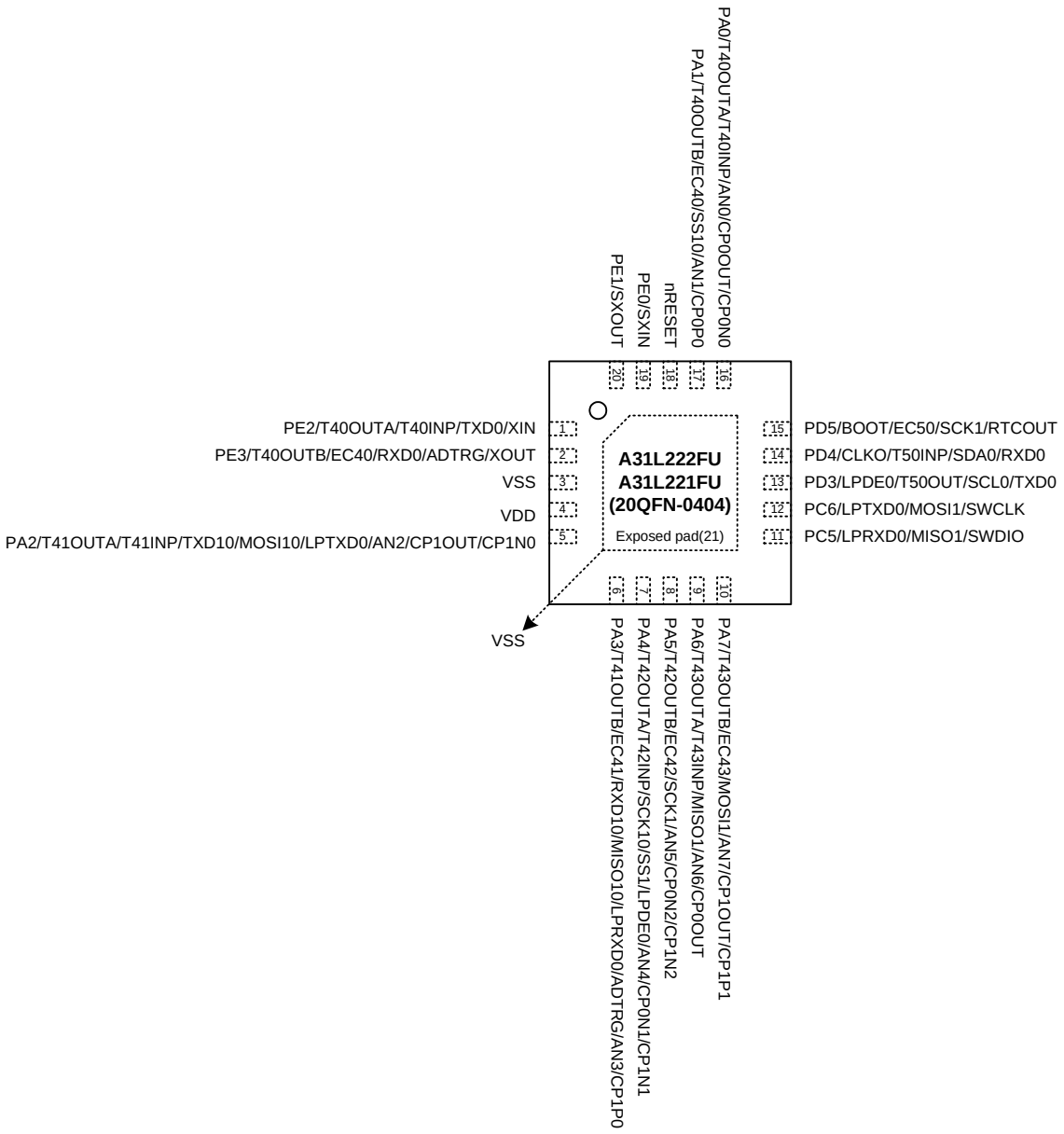
Figure 2. TSSOP-20 Pinouts



NOTES:

1. PD[4:3] pins are 5V tolerant I/O. The corresponding internal resistor must be disabled by s/w to use as 5V I/O. To use as 5V tolerant output, an external pull-up resistor must be used by application and the corresponding pins must be configured with open-drain output by s/w.
2. The PA0 and PA2 pins may be a wakeup source from deep sleep with ALLPWR = 2/3.

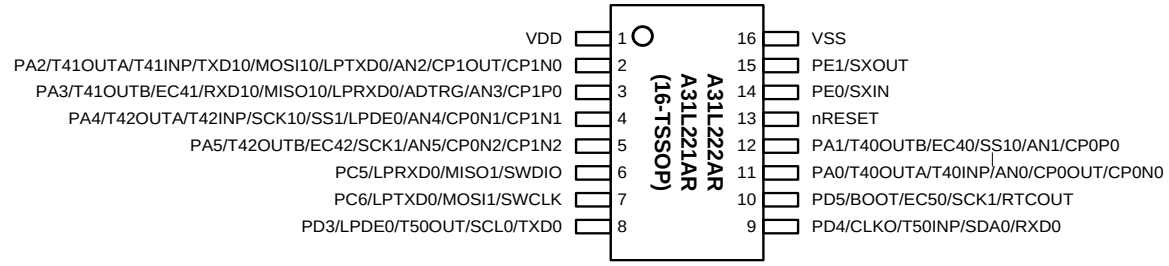
Figure 3. QFN-20 Pinouts



NOTES:

1. PD[4:3] pins are 5V tolerant I/O. The corresponding internal resistor must be disabled by s/w to use as 5V I/O. To use as 5V tolerant output, an external pull-up resistor must be used by application and the corresponding pins must be configured with open-drain output by s/w.
2. The PA0 and PA2 pins may be a wakeup source from deep sleep with ALLPWR = 2/3.

Figure 4. TSSOP-16 Pinouts



NOTES:

1. The PA[7:6] and PE[3:2] pins should be selected as a push-pull output or an input with pullup or pull-down resistor by software control when the 16TSSOP package is used.
2. PD[4:3] pins are 5V tolerant I/O. The corresponding internal resistor must be disabled by s/w to use as 5V I/O. To use as 5V tolerant output, an external pull-up resistor must be used by application and the corresponding pins must be configured with open-drain output by s/w.
3. The PA0 and PA2 pins may be a wakeup source from deep sleep with ALLPWR = 2/3.

2.2 Pin description

Table 3 shows pin configuration containing several pairs of power/ground and other dedicated pins. Multi-function pins have up to nine selections of functions including GPIO.

Table 3. Pin Description

Pin number			Pin name	Type	Description	Remark
TSSOP-20	QFN-20	TSSOP-16				
1	4	1	VDD	P	VDD	
2	5	2	PA2*	IOUDS	PORT A Bit 2 Input/Output	Wake-up possible from deep sleep with ALLPWR=2/3
			T41OUTA	O	Timer 41 pulse output	
			T41INP	I	Timer 41 capture/force input	
			TXD10	O	UART data output	
			MOSI10	I/O	SPI master output, slave input	
			LPTXD0	O	Low power UART data output	
			AN2	IA	A/D converter analog input channel	
			CP1OUT	OA	Comparator 1 output	
			CP1N0	IA	Comparator 1 negative input	
3	6	3	PA3*	IOUDS	PORT A Bit 3 Input/Output	
			T41OUTB	O	Timer 41 pulse output	
			EC41	I	Timer 41 event count input	
			RXD10	I	UART data input	
			MISO10	I/O	SPI master input, slave output	
			LPRXD0	I	Low power UART data input	
			ADTRG	I	ADC trigger input	
			AN3	IA	A/D converter analog input channel	
			CP1P0	IA	Comparator 1 positive input	
4	7	4	PA4*	IOUDS	PORT A Bit 4 Input/Output	
			T42OUTA	O	Timer 42 pulse output	
			T42INP	I	Timer 42 capture/force input	
			SCK10	I/O	SPI clock input/output	
			SS1	I	SPI slave select input	
			LPDE0	O	Low power UART DE signal output	
			AN4	IA	A/D converter analog input channel	
			CP0N1	IA	Comparator 0 negative input	
			CP1N1	IA	Comparator 1 negative input	
5	8	5	PA5*	IOUDS	PORT A Bit 5 Input/Output	
			T42OUTB	O	Timer 42 pulse output	
			EC42	I	Timer 42 event count input	
			SCK1	I/O	SPI clock input/output	
			AN5	IA	A/D converter analog input channel	
			CP0N2	IA	Comparator 0 negative input	
			CP1N2	IA	Comparator 1 negative input	

Table 3. Pin Description (continued)

Pin number			Pin name	Type	Description	Remark
TSSOP-20	QFN-20	TSSOP-16				
6	9	-	PA6*	IOUDS	PORT A Bit 6 Input/Output	
			T43OUTA	O	Timer 43 pulse output	
			T43INP	I	Timer 43 capture/force input	
			MISO1	I/O	SPI master input, slave output	
			AN6	IA	A/D converter analog input channel	
			CP0OUT	OA	Comparator 0 output	
7	10	-	PA7*	IOUDS	PORT A Bit 7 Input/Output	
			T43OUTB	O	Timer 43 pulse output	
			EC43	I	Timer 43 event count input	
			MOSI1	I/O	SPI master output, slave input	
			AN7	IA	A/D converter analog input channel	
			CP1OUT	OA	Comparator 1 output	
			CP1P1	IA	Comparator 1 positive input	
8	11	6	PC5	IOUDS	PORT C Bit 5 Input/Output	
			LPRXD0	Input	Low power UART data input	
			MISO1	I/O	SPI master input, slave output	
			SWDIO*	I/O	SWD data input/output	Pull-up when reset
9	12	7	PC6	IOUDS	PORT C Bit 6 Input/Output	
			LPTXD0	Output	Low power UART data output	
			MOSI1	I/O	SPI master output, slave input	
			SWCLK*	Input	SWD clock input	Pull-down when reset
10	13	8	PD3*	IOUDS	PORT D Bit 3 Input/Output	5V tolerant I/O (The internal pull-up resistor must be disabled to use 5V I/O)
			LPDE0	O	Low power UART DE signal output	
			T50OUT	O	Timer 50 pulse output	
			SCL0	I/O	I2C clock input/output	
			TXD0	O	UART data output	
11	14	9	PD4*	IOUDS	PORT D Bit 4 Input/Output	5V tolerant I/O (The internal pull-up resistor must be disabled to use 5V I/O)
			CLKO	O	System clock output	
			T50INP	I	Timer 50 capture/clear input	
			SDA0	I/O	I2C data input/output	
			RXD0	I	UART data input	
12	15	10	PD5	IOUDS	PORT D Bit 5 Input/Output	
			BOOT*	I	Boot mode input	Pull-up when reset
			EC50	I	Timer 50 event count input	
			SCK1	I/O	SPI clock input/output	
			RTCOUT	O	Real time clock output	

Table 3. Pin Description (continued)

Pin number			Pin name	Type	Description	Remark
TSSOP-20	QFN-20	TSSOP-16				
13	16	11	PA0*	IOUDS	PORT A Bit 0 Input/Output	Wake-up possible from deep sleep with ALLPWR=2/3
			T40OUTA	O	Timer 40 pulse output	
			T40INP	I	Timer 40 capture/force input	
			AN0	IA	A/D converter analog input channel	
			CP0OUT	OA	Comparator 0 output	
			CP0N0	IA	Comparator 0 negative input	
14	17	12	PA1*	IOUDS	PORT A Bit 1 Input/Output	
			T40OUTB	O	Timer 40 pulse output	
			EC40	I	Timer 40 event count input	
			SS10	I	SPI slave select input	
			AN1	IA	A/D converter analog input channel	
			CP0P0	IA	Comparator 0 positive input	
15	18	13	nRESET	Input	External Reset Input	Always pull-up
16	19	14	PE0*	IOUDS	PORT E Bit 0 Input/Output	
			SXIN	IA	Sub Oscillator Input	
17	20	15	PE1*	IOUDS	PORT E Bit 1 Input/Output	
			SXOUT	OA	Sub Oscillator Output	
18	1	-	PE2*	IOUDS	PORT E Bit 2 Input/Output	
			T40OUTA	O	Timer 40 pulse output	
			T40INP	I	Timer 40 capture/force input	
			TXD0	O	UART data output	
			XIN	IA	Main oscillator input	
19	2	-	PE3*	IOUDS	PORT E Bit 3 Input/Output	
			T40OUTB	O	Timer 40 pulse output	
			EC40	I	Timer 40 event count input	
			RXD0	I	UART data input	
			ADTRG	I	ADC trigger input	
			XOUT	OA	Main oscillator output	
20	3	16	VSS	P	Ground	
-	21	-	VSS	P	Ground (Exposed pad)	

NOTES:

1. Notation: I=Input, O=Output, U=Pull-up, D=Pull-down, S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
2. (*) Selected pin function after reset condition
3. Pin order may be changed with revision notice.

3 System and memory overview

Main system and memory of A31L22x series consist of the followings:

- ARM® Cortex® -M0+ core
- Internal SRAM
- Internal Code Flash memory
- AHB (Advanced High Performance Bus) and APB (Advanced Peripheral Bus)

3.1 Cortex®-M0+ core

The Cortex-M0+ processor is the most energy-efficient ARM processor available. It builds on the very successful Cortex-M0+ processor, retaining full instruction set and tool compatibility, while further reducing energy consumption and increasing performance.

ARM's technical reference manual "DDI 0484C" provides detailed information on Cortex-M0+.

3.2 Interrupt controller

The Cortex-M0+ processor has an embedded interrupt controller named NVIC (Nested Vector Interrupt Controller). The A31L22x series has an additional interrupt control block for controlling 32 interrupt sources generated by internal peripherals.

To use interrupts from internal peripherals, both the NVIC and the interrupt control block must be configured properly.

This document only describes the peripheral interrupt controller, therefore for more information on NVIC inside the Cortex-M0+ processor, please refer to the technical reference manual “ARM DDI 0484C” on the ARM technical document site.

Table 4. Interrupt Vector Map

Priority	Vector Address	Interrupt Source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Address
-14	0x0000_0008	NMI Exception
-13	0x0000_000C	Hard Fault Exception
-12	0x0000_0010	Reserved
-11	0x0000_0014	
-10	0x0000_0018	
-9	0x0000_001C	
-8	0x0000_0020	
-7	0x0000_0024	
-6	0x0000_0028	

Table 4. Interrupt Vector Map (continued)

Priority	Vector Address	Interrupt Source
-5	0x0000_002C	SVCall Exception
-4	0x0000_0030	Reserved
-3	0x0000_0034	
-2	0x0000_0038	PenSV Exception
-1	0x0000_003C	SysTick Exception
0	0x0000_0040	LVI Interrupt
1	0x0000_0044	WUT Interrupt
2	0x0000_0048	WDT Interrupt
3	0x0000_004C	EINT0 Interrupt
4	0x0000_0050	EINT1 Interrupt
5	0x0000_0054	EINT2 Interrupt
6	0x0000_0058	EINT3 Interrupt
7	0x0000_005C	TIMER40 Interrupt
8	0x0000_0060	TIMER41 Interrupt
9	0x0000_0064	TIMER42 Interrupt
10	0x0000_0068	I2C0 Interrupt
11	0x0000_006C	USART10 Interrupt
12	0x0000_0070	SPI1 Interrupt
13	0x0000_0074	Reserved
14	0x0000_0078	
15	0x0000_007C	TIMER50 Interrupt
16	0x0000_0080	Reserved
17	0x0000_0084	
18	0x0000_0088	ADC Interrupt
19	0x0000_008C	UART0 Interrupt
20	0x0000_0090	Temperature Sensor Interrupt

Table 4. Interrupt Vector Map (continued)

Priority	Vector Address	Interrupt Source
21	0x0000_0094	TIMER43 Interrupt
22	0x0000_0098	CMP[1:0] Interrupt
23	0x0000_009C	Reserved
24	0x0000_00A0	
25	0x0000_00A4	LPUART0 Interrupt
26	0x0000_00A8	Reserved
27	0x0000_00AC	
28	0x0000_00B0	RTCC Interrupt TIMER60 Interrupt
29	0x0000_00B4	Reserved
30	0x0000_00B8	
31	0x0000_00BC	

3.3 Boot mode

3.3.1 Boot mode pin

The A31L22x series has Boot mode to program the internal Flash memory. Boot mode is activated when the BOOT pin is set to “Low” level at reset timing. (For normal operation mode, the BOOT pin is set to “High” level.)

Boot mode supports the UART boot using the TXD10/RXD10 ports.

Table 5 introduces pins used in Boot mode.

Table 5. Pin Description used in Boot Mode

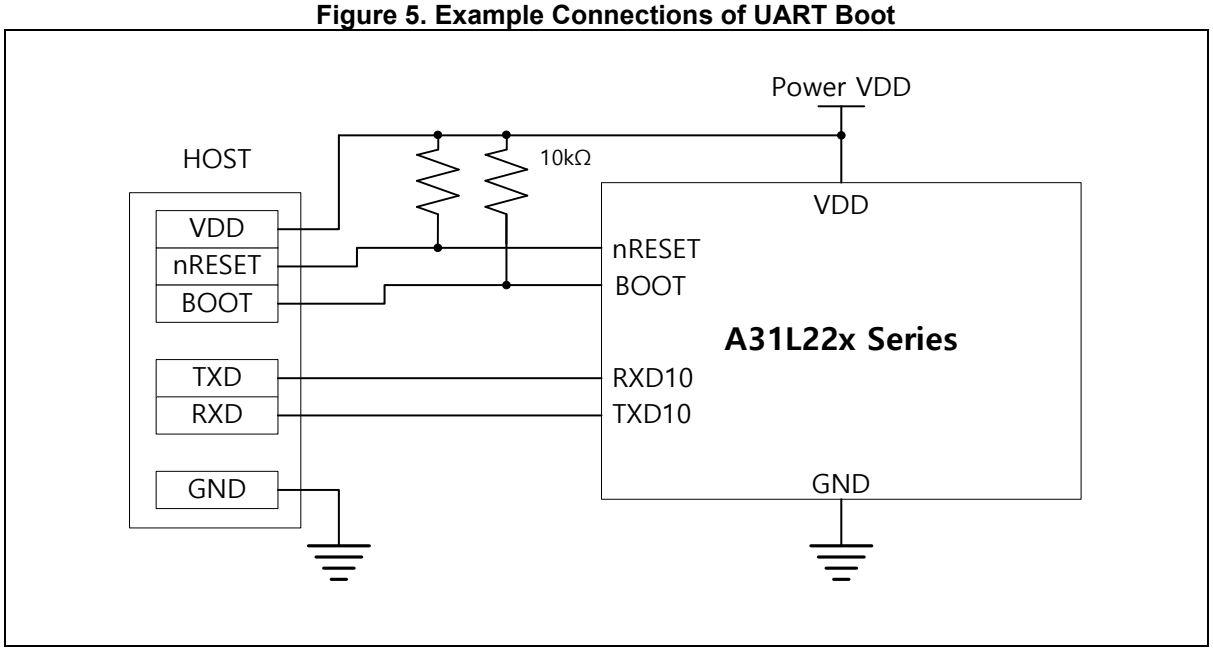
Block	Pin Name	Direction	Description
SYSTEM	nRESET	I	Reset Input signal
	BOOT/PD5	I	‘0’ to enter Boot mode
UART mode of USART10	RXD10/PA3	I	UART Boot Receive Data
	TXD10/PA2	O	UART Boot Transmit Data

3.3.2 Boot mode connections

Users can design the target board using Boot mode ports – UART mode of USART10.

Figure 5 shows an example diagram of connections in Boot mode.

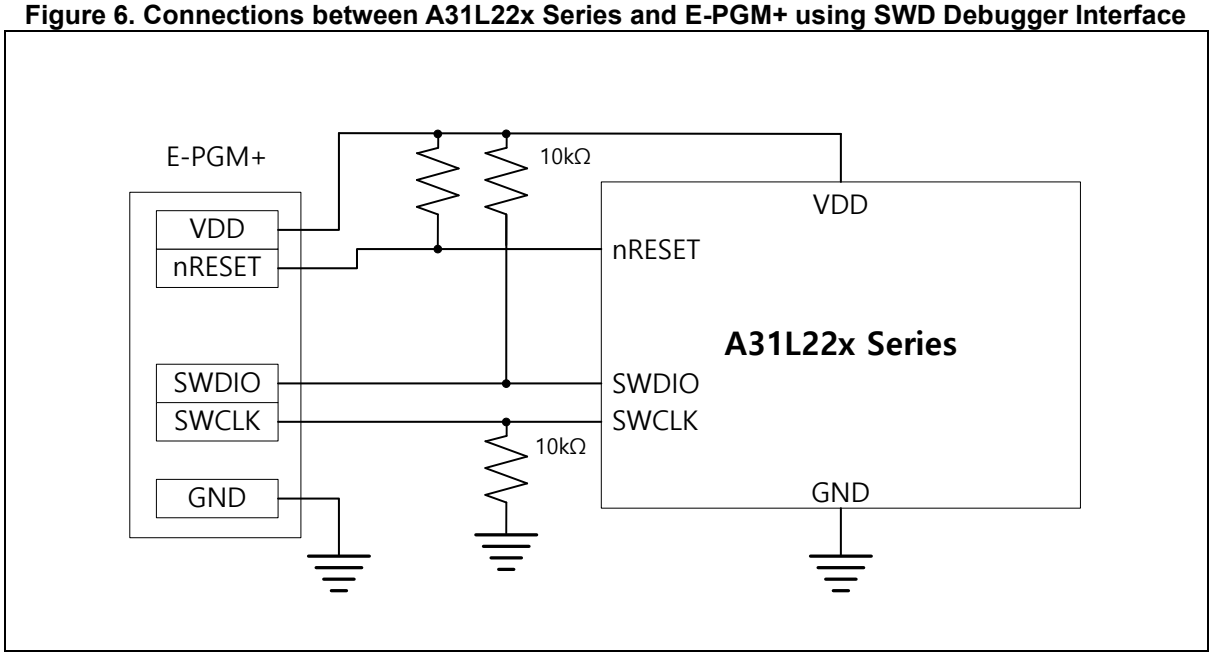
Figure 5. Example Connections of UART Boot



3.4 SWD debug mode and E-PGM+ connections

Figure 6 shows a diagram of connections for SWD debugger interface or E-PGM+.

Figure 6. Connections between A31L22x Series and E-PGM+ using SWD Debugger Interface

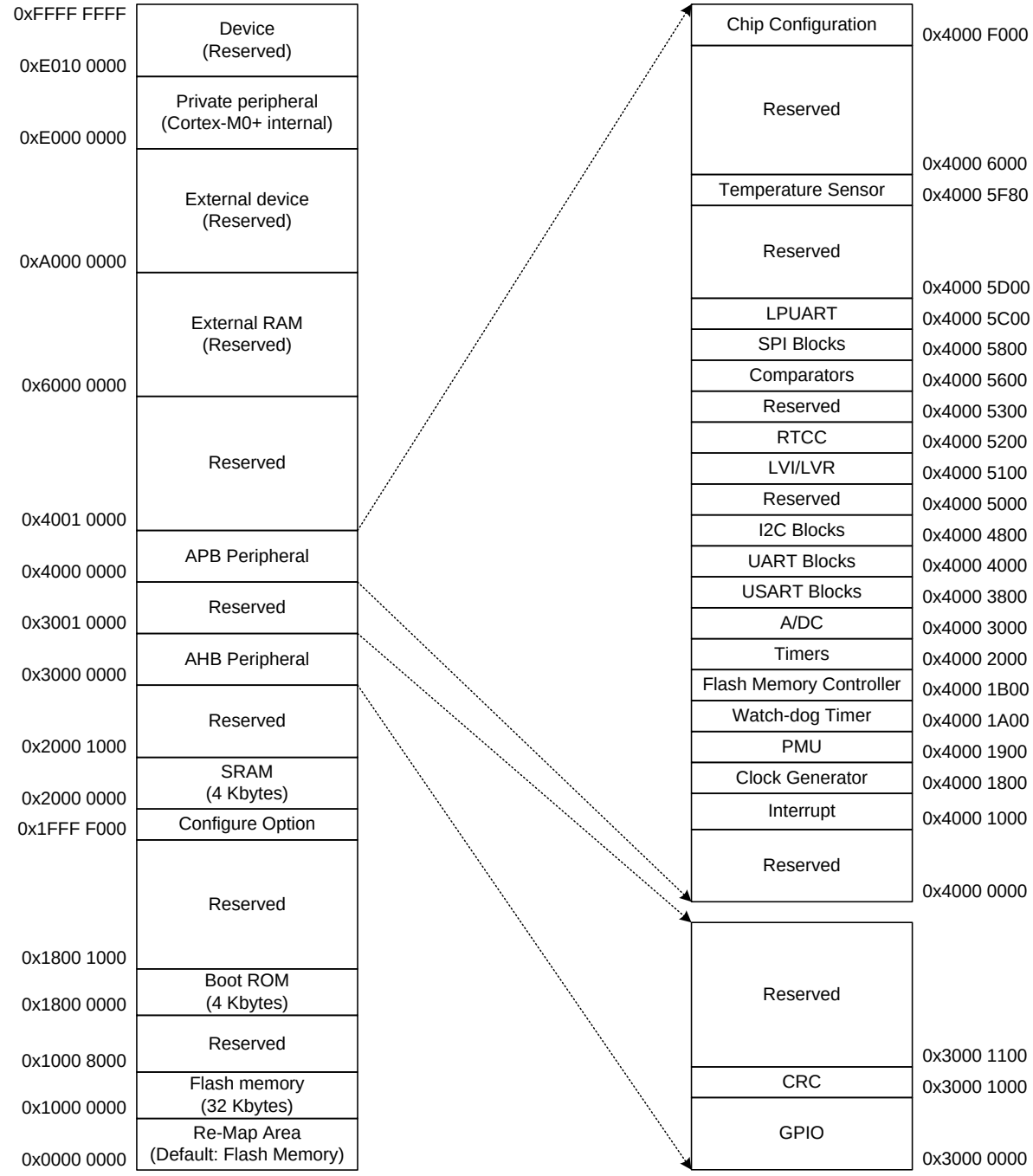


3.5 Memory organization

3.5.1 Memory map

Figure 7 shows addressable memory space in memory map.

Figure 7. Main Memory Map



NOTE: Access to the reserved area may cause a malfunction.

3.5.2 Internal SRAM

The A31L22x series has a block of 0-wait on-chip SRAM. Its size is 4KB, and its base address is 0x2000_0000. The SRAM's memory area is mainly used for data memory and stack memory. It is possible to locate code area in the SRAM memory for fast operation or for Flash erase or program operation for self-program.

This device does not support memory remapping. Therefore, the jump and return are required to process the code in SRAM memory area.

3.5.3 Flash memory

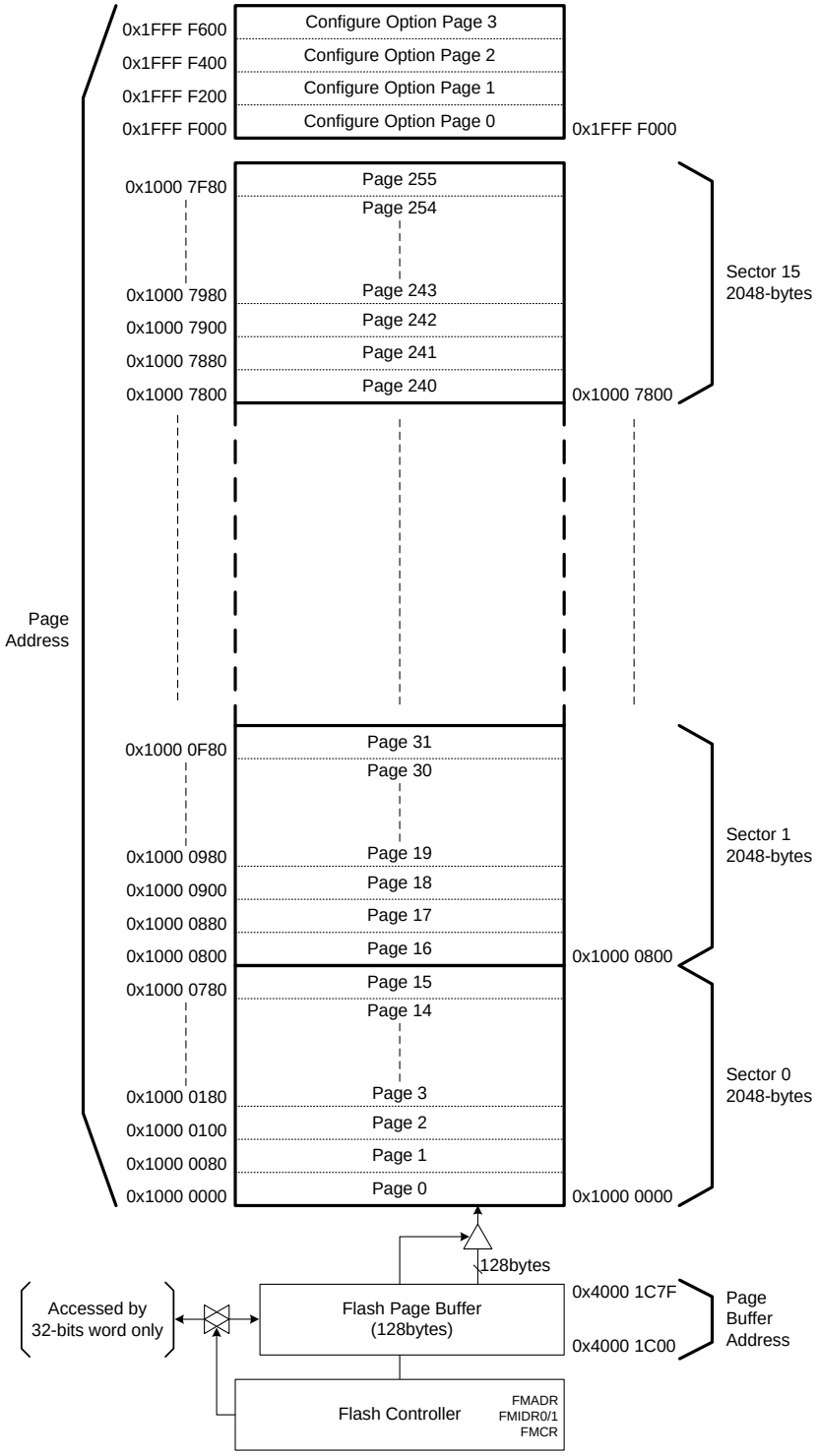
The A31L22x series has built-in Flash memory with the following features:

- 32 or 16KB Flash memory
- 32-bit wide read data bus
- 128-byte sized page
- Page erase and bulk erase
- programming in 128-byte units

Table 6. Built-in Flash Memory Specification

Item	Description
Size	32KB
Start address	0x1000_0000
End address	0x1000_7FFF
Page size	128-byte
Total page count	256 pages
PGM unit	128-byte
Erase unit	128-byte or bulk

Figure 8. Built-in Flash Memory Block Diagram



NOTES:

1. If an instruction of a size other than the 32-bit size is used to write data to the buffer, incorrect data is written.
2. Each of configure option pages (page0/1/2/3) is 128-byte size, respectively.

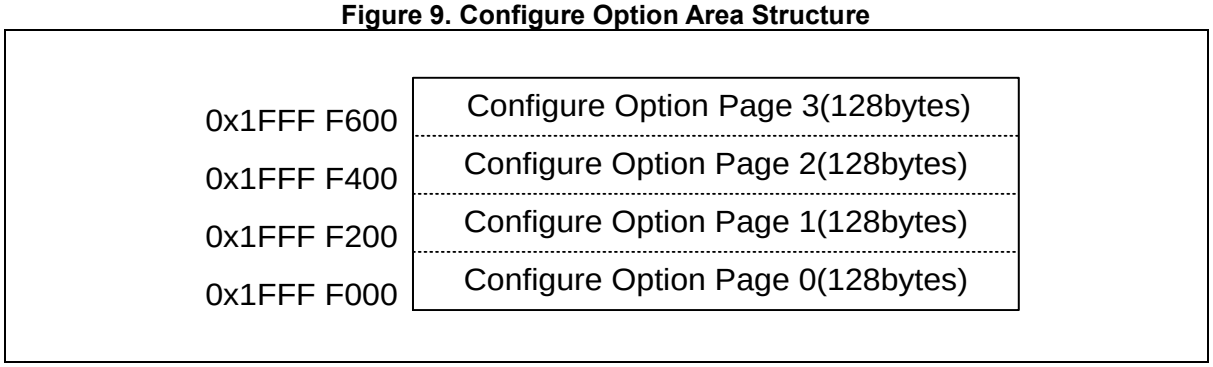
3.5.4 Configure option area

Configure option area of the A31L22x series is used for system related trimming values, user option, and user data. The configure option area consists of four pages in the Flash memory, which can be erased and written by the Flash memory controller. This area can be read by any instruction.

Four pages of the configure option area are listed below:

- Page 0: System related trimming values and 128-bit unique device ID registers
- Page 1: User option for Read Protection, Watchdog Timer, and LVR voltage level configurations
- Page 2: User data 0 area
- Page 3: User data 1 area

Figure 9. Configure Option Area Structure



3.5.4.1 Configure option pages

Base address of the configure option area ranges from 0x1FFF_F000 to 0x1FFF_F600.

The area map is shown in Table 7.

Table 7. Configure Option Area Map

Page	NAME	ADDRESS	DESCRIPTION
0	-	0x1FFF_F000 to 0x1FFF_F047 0x1FFF_F060 to 0x1FFF_F07F	System Trimming Values
	TS_FREQ_T30	0x1FFF_F048	Temperature Sensor Output Frequency acquired at 30℃ [Hz]
	TS_FREQ_T85	0x1FFF_F04C	Temperature Sensor Output Frequency acquired at 85℃ [Hz]
	TS_FREQ_T105	0x1FFF_F06C	Temperature Sensor Output Frequency acquired at 105℃ [Hz]
	CONF_MF1CNFIG	0x1FFF_F050	Manufacture Information 1 for 128-bit unique ID
	CONF_MF2CNFIG	0x1FFF_F054	Manufacture Information 2 for 128-bit unique ID
	CONF_MF3CNFIG	0x1FFF_F058	Manufacture Information 3 for 128-bit unique ID
	CONF_MF4CNFIG	0x1FFF_F05C	Manufacture Information 4 for 128-bit unique ID
1	CONF_RPCNFIG	0x1FFF_F200	Configuration for Read Protection
	CONF_WDTCNFIG	0x1FFF_F20C	Configuration for Watch-Dog Timer
	CONF_LVRCNFIG	0x1FFF_F210	Configuration for Low Voltage Reset
	CONF_CNFIGWTP1	0x1FFF_F214	Erase/Write Protection for configure option page 1/2/3
	CONF_FMWTP1	0x1FFF_F240	Erase/Write Protection 1 for Flash Memory
2	-	0x1FFF_F400 to 0x1FFF_F47F	User Data Area 0
3	-	0x1FFF_F600 to 0x1FFF_F67F	User Data Area 1

4 System Control Unit (SCU)

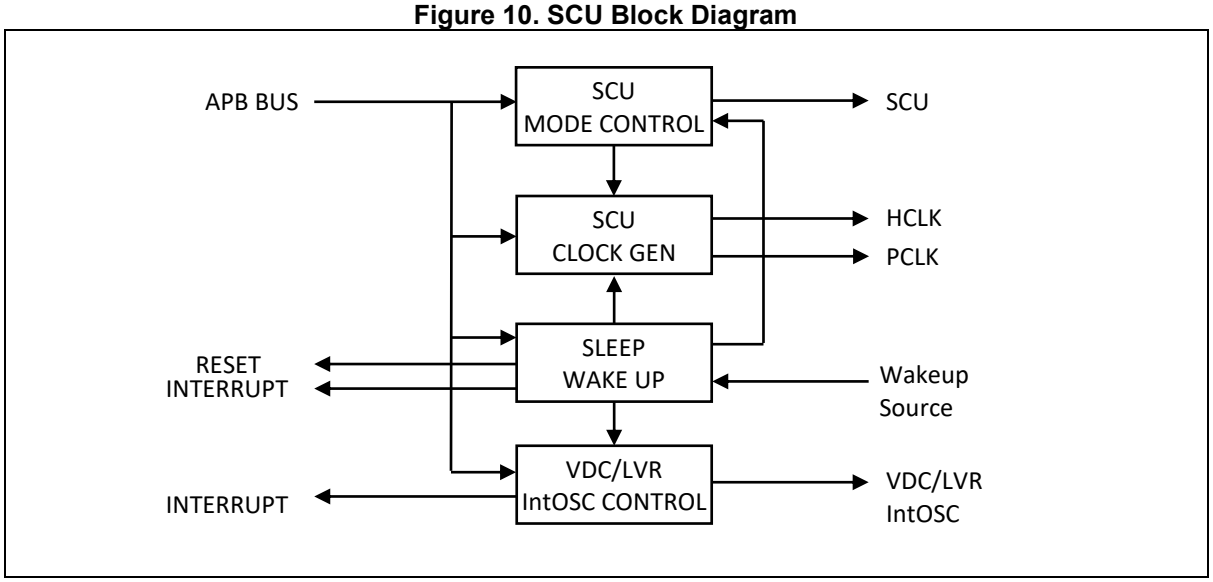
The A31L22x series has a built-in intelligent power control block, which manages analog blocks and operating modes.

This SCU block also controls internal reset and clock signals to maintain optimized system performance and power dissipation.

4.1 SCU block diagram

Figure 10 shows the SCU block diagram.

Figure 10. SCU Block Diagram

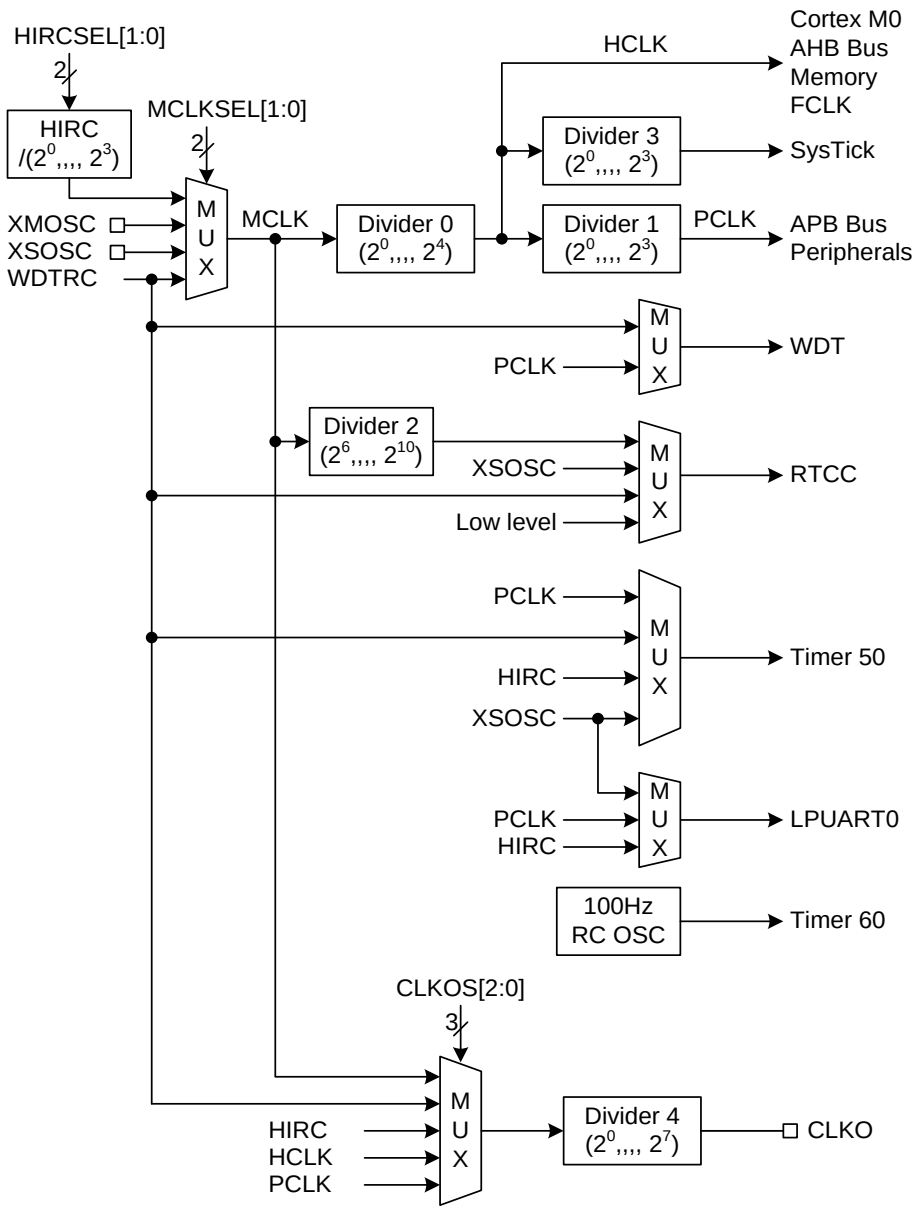


4.2 Clock system

The A31L22x series has two main operating clocks. One is the HCLK, which supplies clocks to the CPU and AHB bus system, and the other is the PCLK, which supplies clocks to the peripheral systems.

Users can control the clock system variation using software. Figure 11 shows the clock system of the A31L22x series and Table 8 shows the description for clock sources.

Figure 11. Clock Source Configuration



NOTE: If the WRCMF[11:0] bits of configuration are not equal to 0x96D, the WDTRC oscillation can't be disabled by the WDTRCEN bit of SCU_CLKSRCR register.

Each mux that switches the clock source has a glitch-free circuit. So a clock can be switched without glitch risks. When users change the clock mux control, be sure that both clock sources are alive. If either is not alive, the clock change operation stops and the system shuts down (and won't recover).

Table 8. Clock Sources

Clock name	Mnemonic	Frequency	Description
Main OSC	XMOSC	• X-TAL (2MHz to 16MHz) • External Clock (2MHz to 32MHz)	• External Main Crystal OSC • External Main Clock
Sub OSC	XSOSC	X-TAL (32.768kHz)	External Sub Crystal OSC
Internal RC OSC	HIRC	2MHz to 32MHz	High Frequency Internal RC OSC
WDT RC OSC	WDTRC	40kHz	Watchdog Timer RC OSC

4.2.1 HCLK clock domain

The HCLK clock feeds the clock to the CPU and AHB bus. Cortex-M0+ CPU requires 2 clocks, FCLK and HCLK. The FCLK is a free running clock and is always running except during power down mode. The HCLK can be stopped during SLEEP mode.

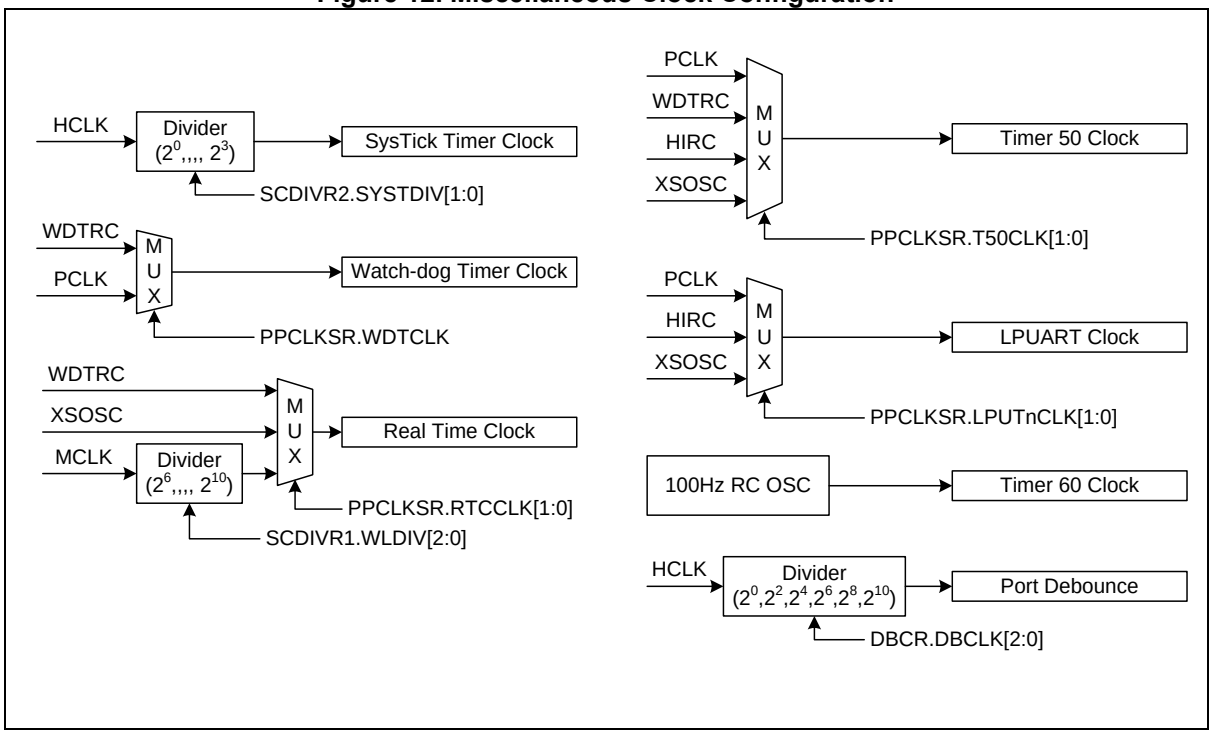
The HCLK clock operates the BUS system and memory systems. The maximum clock speed of the BUS operation is 32MHz. The HCLK frequency should be limited to 32MHz or lower.

4.2.2 Miscellaneous clock domain

Various clock sources are required for each functional block. The SCU provides clock source selectivity with dedicated pre-scaler for each functional block. The clock selection mux does not support glitch-free function, so the clock is unpredictable during clock selection.

Figure 12 shows the configurations of miscellaneous clocks.

Figure 12. Miscellaneous Clock Configuration



4.2.3 PCLK clock domain

The PCLK is the master clock for all peripherals except for the CRC generator and ports. It can shut down during power down modes. Each peripheral clock is generated by the SCU_PPCLKEN1 and SCU_PPCLKEN2 register set.

Figure 11 illustrates the PCLK clock distributions. Peripherals are not accessible until the PCLK clock of each block is enabled, and even by reading its registers.

4.2.4 Clock configuration procedure

When the device is powered on, a default system clock is generated by the HIRC (2MHz) clock. The HIRC is enabled by default during the power up sequence. Other clock sources are enabled by user controls and configuration options with a system clock.

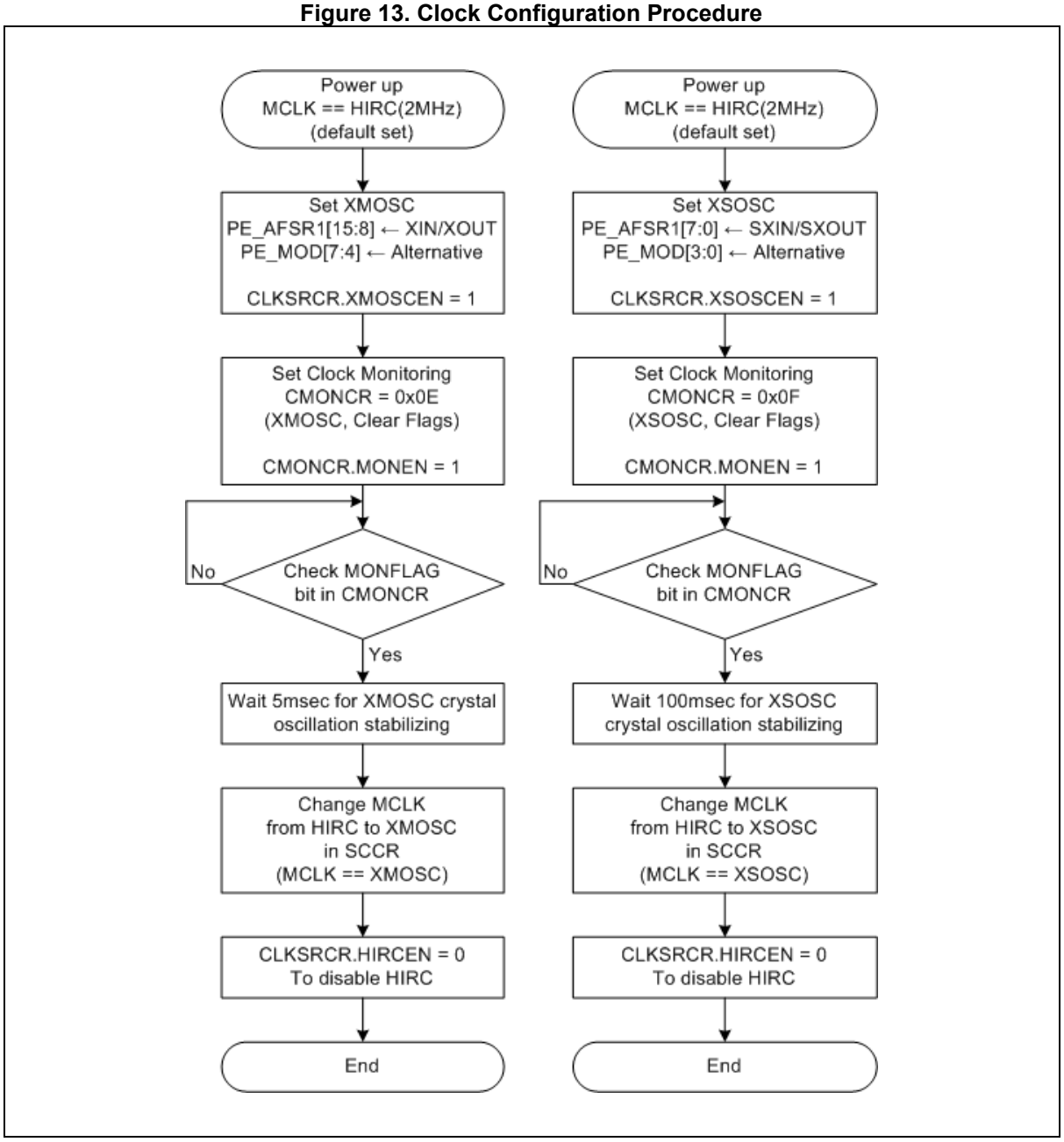
The XMOSC and XSOSC clocks are enabled by the XMOSCEN and XSOSCEN bits of the SCU_CLKSRCR register, respectively. Before enabling XMOSC and XSOSC blocks, the pin mux configuration should be set for XIN/XOUT and SXIN/SXOUT functions.

The PE2/PE3 and PE0/PE1 pins are shared by the XMOSC's XIN/XOUT function and XSOSC's SXIN/SXOUT function – The PE_MOD and PE_AFSR1 registers should be configured properly.

After enabling the XMOSC and XSOSC blocks, a user can check stability of crystal oscillation through the clock monitoring control register, SCU_CMONCR. It takes more than 1ms to ensure stable crystal oscillation before changing the system clock.

Figure 13 shows an example of a flow chart configuring the system clock as the XMOSC and XSOSC clocks.

Figure 13. Clock Configuration Procedure



4.3 Reset

The A31L22x series has two system resets. One is the cold reset by POR, which is effective during power up or down sequence, and the other is the warm reset, which is generated by several reset sources. The reset event makes the device to turn back to its initial state.

The cold reset has a single reset source (POR), and the warm reset has several reset sources listed below:

- nRESET pin
- WDT reset
- LVR reset
- MON reset
- S/W reset
- CPU request reset
- WAKUP3 reset

4.3.1 Cold reset

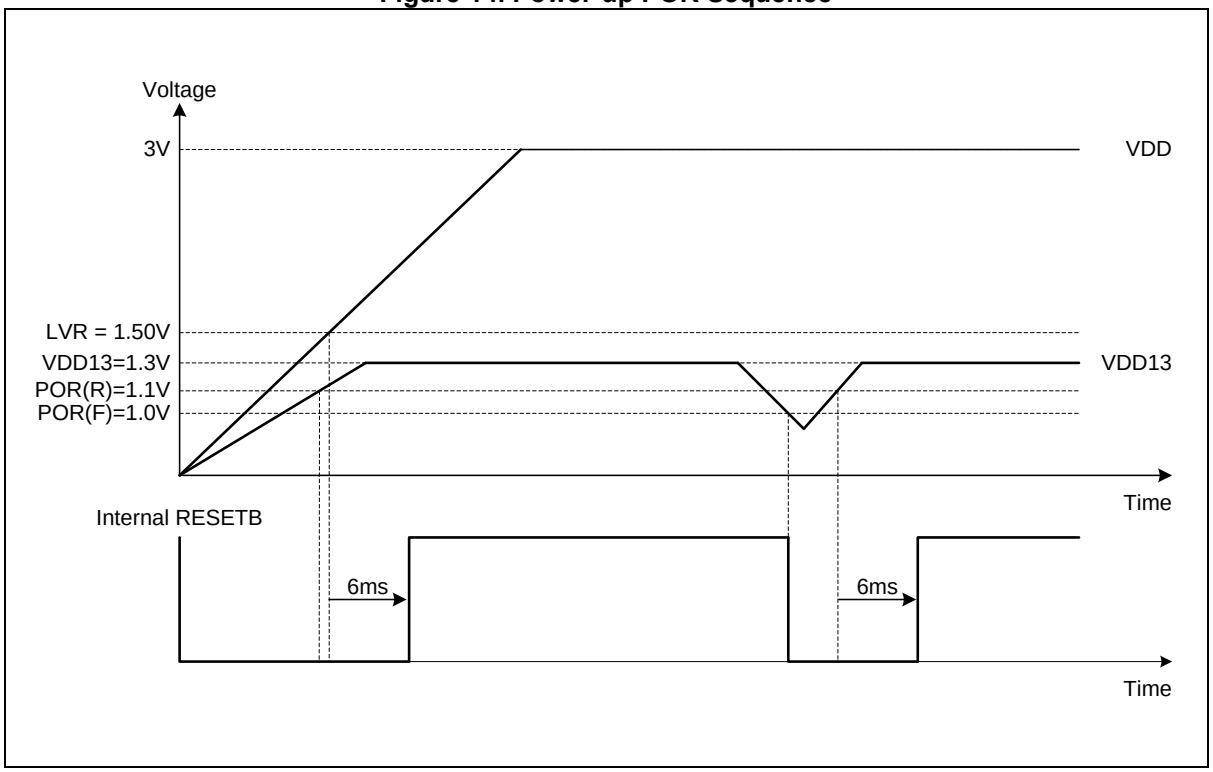
The cold reset is one of the important features of the A31L22x series when powered on. This characteristic globally affects the system boot.

The internal VDC is enabled when the VDD power is supplied. The internal VDD level slope follows the external VDD power slope.

The internal POR trigger level is at 1.1V of the internal VDC voltage. At this time, boot operation begins. The internal RC clock turns on and counts 6ms for the internal VDC level to stabilize. At this time, the external VDD voltage level should be bigger than the initial LVR level (1.50V). After 6ms of counting, the CPU reset is released and operation begins.

Figure 14 shows waveform of the power up sequence and internal reset.

Figure 14. Power-up POR Sequence



The register SCU_RSTSSR shows the POR reset status. The last reset comes from the POR.

The PORSTA bit in the SCU_RSTSSR register is set to ‘1’. After power on, this bit is always set to ‘1’ unless it is cleared by S/W. If abnormal internal voltage drop is detected during normal operation, the system is reset and this bit is set to ‘1’.

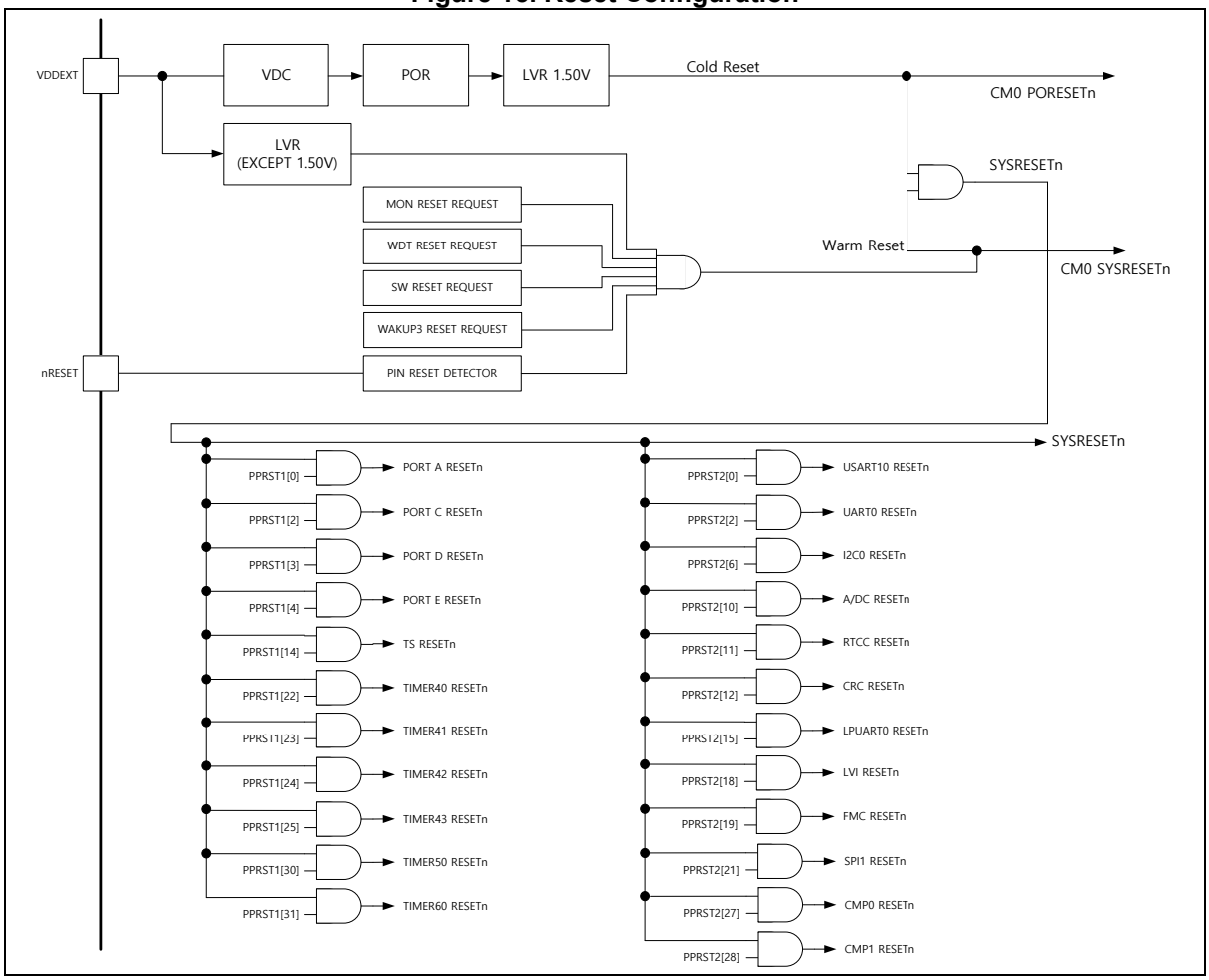
When the cold reset is applied, the entire device returns to its initial state.

4.3.2 Warm reset

The warm reset event has several reset sources and some parts of the device return to their initial states when the warm reset takes place.

The warm reset status appears in the register SCU_RSTSSR. A reset for each peripheral block is controlled by the register SCU_PPRST. The reset can be masked independently.

Figure 15. Reset Configuration

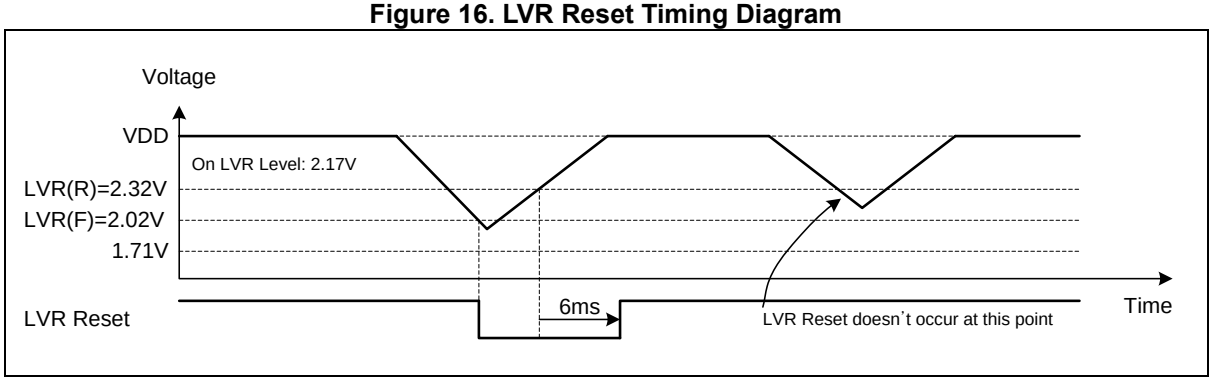


4.3.3 LVR reset

The LVR voltage level is set by a low voltage reset configuration register (CONF_LVRCNFIG) in the configure option page 1. The LVR reset status appears in the register SCU_RSTSSR.

The LVR reset is controlled by the register SCU_LVRCR. This register is cleared to “0x00” when the POR/WAKUP3 reset occurs.

Figure 16. LVR Reset Timing Diagram

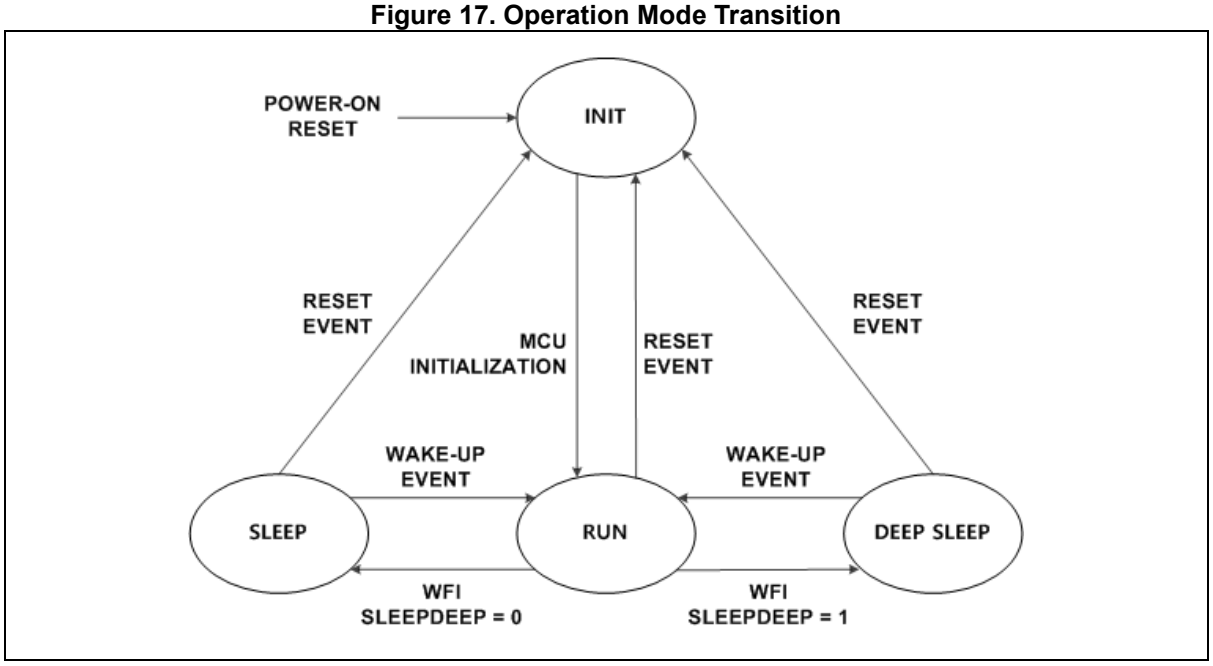


4.4 Operation mode

INIT mode is the initial state of the device when resetting. At RUN mode, the chip runs at its max CPU performance with a high-speed clock system. At SLEEP and DEEP SLEEP mode, the chip runs at a low power consumption mode. The system saves power by halting the processor core and unused peripherals.

Figure 17 shows a diagram of the operation mode transition.

Figure 17. Operation Mode Transition



4.4.1 RUN mode

This mode is to operate CPU core and peripheral hardware with a high-speed clock. The device enters the INIT state after resetting, and then enters the RUN mode.

4.4.2 SLEEP mode

In this mode, only the CPU is stopped. Each peripheral function is turned on by the function enable bit and the clock enable bit of the register SCU_PPCLKEN.

4.4.3 DEEP SLEEP mode

In this mode, not only the CPU but also a selected system clock (MCLK) are stopped. The RTCC with a sub clock, T60, and the Watchdog Timer with WDTRC still operate in DEEP SLEEP mode 0/2.

4.4.4 SHUT DOWN mode

In this mode (DEEP SLEEP mode 3), the CPU, a selected system clock (MCLK), and most of the peripherals are stopped. Only the T60 can operate in this mode.

4.5 Pins for SCU

Table 9. Pins and External Signals for SCU

Pin name	Type	Description
nRESET	I	External Reset Input
XIN/XOUT	OSC	External Crystal Oscillator for Main Clock
SXIN/SXOUT	OSC	External Crystal Oscillator for Sub Clock
CLKO	O	Clock Output Monitoring Signal

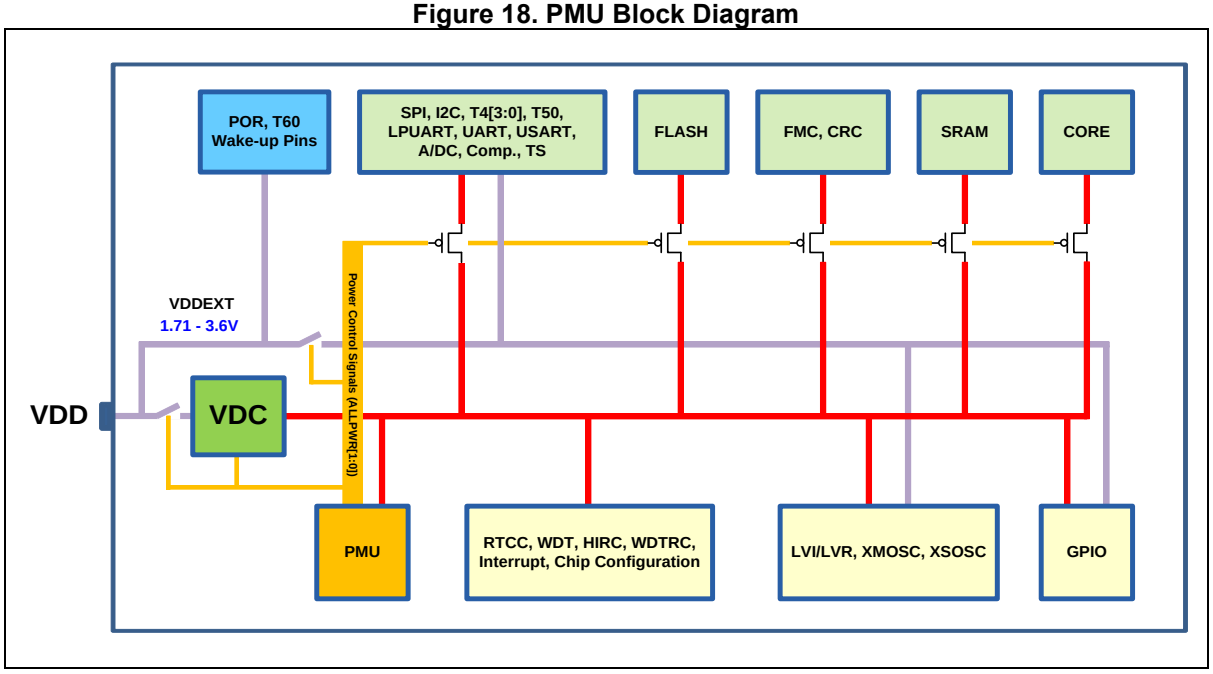
5 Power Management Unit (PMU)

The A31L22x series has a built-in Power Management Unit (PMU), which manages the internal power supply of the system control and peripheral parts and a wake-up time from SLEEP and DEEP SLEEP modes.

This PMU has 32-byte sized backup registers to retain data during DEEP SLEEP modes except DEEP SLEEP mode 3 (SHUT DOWN mode).

5.1 PMU block diagram

Figure 18. PMU Block Diagram



6 Port Control Unit (PCU) and GPIO

The Port Control Unit (PCU) of the A31L22x series configures and controls external I/Os as shown below:

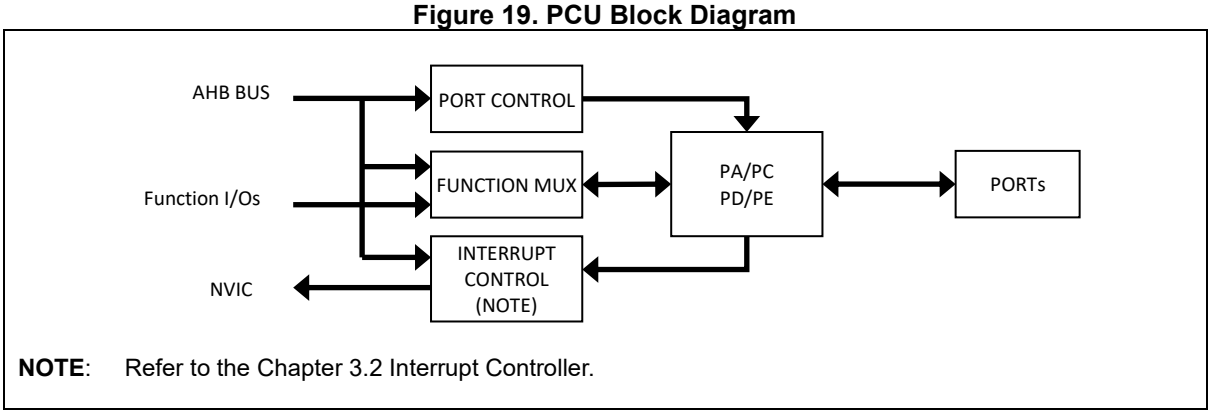
- Direction settings of the external signal on each pin
- Interrupt trigger mode settings for each pin
- Internal pull-up/down register control and open drain control settings

Most pins, except for dedicated function pins, can be used as GPIO (General Purpose I/O) ports. The GPIO block controls the GPIOs as shown below:

- Output signal level (H/L) selection
- External interrupt interface
- Pull-up/down enabling or disabling settings

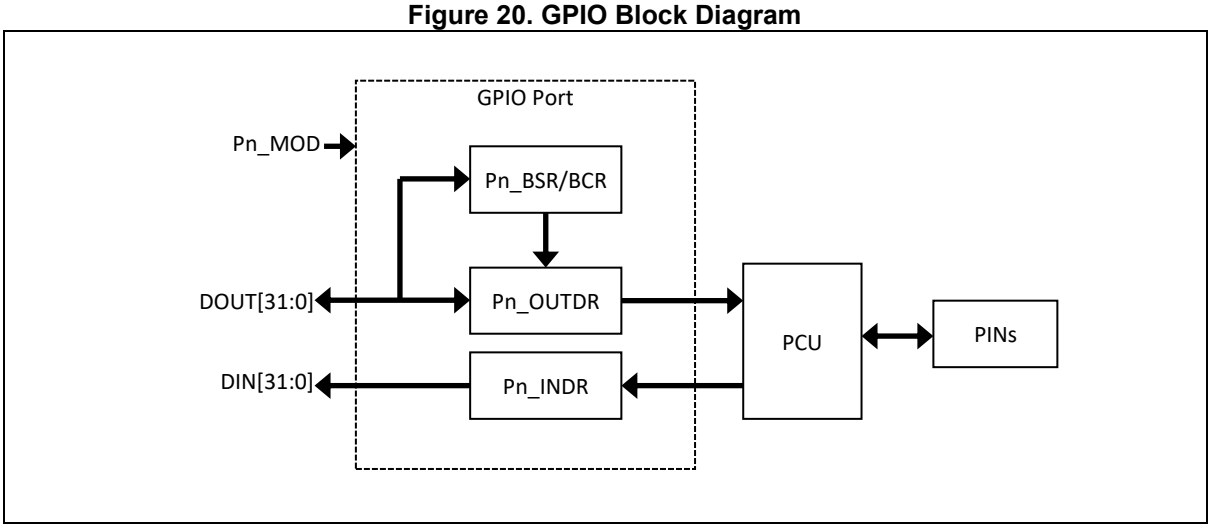
6.1 PCU and GPIO block diagrams

Figure 19. PCU Block Diagram



NOTE: Refer to the Chapter 3.2 Interrupt Controller.

Figure 20. GPIO Block Diagram



6.2 I/O port block diagram

Figure 21. I/O Port Block Diagram (General Purpose I/O Pins)

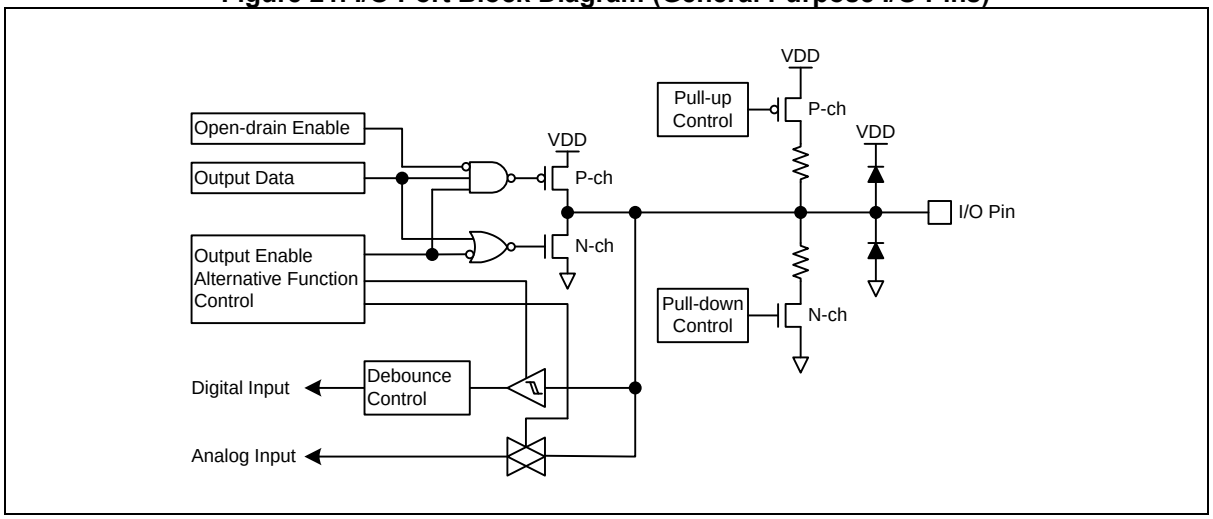
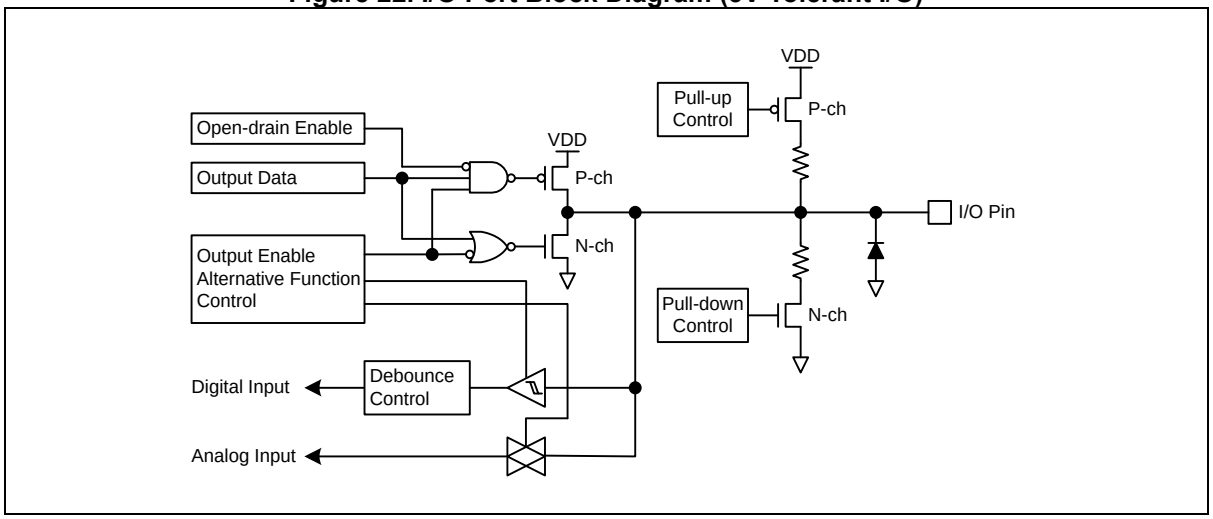


Figure 22. I/O Port Block Diagram (5V Tolerant I/O)



6.3 Pin multiplexing

The GPIO pins support alternative functions. Table 10 shows pin multiplexing information.

Table 10. GPIO Alternative Functions

PORT	PIN	FUNCTION							
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA	0	T40OUTA	T40INP	–	–	AN0	CP0N0	CP0OUT	–
	1	T40OUTB	EC40	–	SS10	AN1	CP0P0	–	–
	2	T41OUTA	T41INP	TXD10	MOSI10	AN2	CP1N0	CP1OUT	LPTXD0
	3	T41OUTB	EC41	RXD10	MISO10	AN3	CP1P0	ADTRG	LPRXD0
	4	T42OUTA	T42INP	SS1	SCK10	AN4	CP0N1	CP1N1	LPDE0
	5	T42OUTB	EC42	–	SCK1	AN5	CP0N2	CP1N2	–
	6	T43OUTA	T43INP	–	MISO1	AN6	–	CP0OUT	–
	7	T43OUTB	EC43	–	MOSI1	AN7	CP1P1	CP1OUT	–
PC	5	SWDIO	–	LPRXD0	MISO1	–	–	–	–
	6	SWCLK	–	LPTXD0	MOSI1	–	–	–	–
PD	3	T50OUT	–	TXD0	–	LPDE0	SCL0	–	–
	4	CLKO	T50INP	RXD0	–	–	SDA0	–	–
	5	BOOT	EC50	RTCOUT	SCK1	–	–	–	–
PE	0	SXIN	–	–	–	–	–	–	–
	1	SXOUT	–	–	–	–	–	–	–
	2	XIN	–	TXD0	–	T40OUTA	T40INP	–	–
	3	XOUT	–	RXD0	–	T40OUTB	EC40	ADTRG	–

NOTE:

1. The SWCLK and SWDIO pins shouldn't be changed as other alternative functions by software during the pins are connected with debugger host.

7 Watchdog Timer (WDT)

The Watchdog Timer (WDT) quickly detects the CPU malfunctions such as endless loops caused by noise, and recovers the CPU to the normal state. The WDT signal for detecting the malfunction can be used as either a CPU reset or an interrupt request.

When the WDT is not used for detecting malfunction, it can be used as a timer to generate interrupts at fixed time intervals. When the WDT_CNT value reaches the WDT_WINDR value, a watchdog interrupt can be generated.

The underflow time of the WDT can be set by configuring the WDT_DR register. If the underflow occurs, an internal reset may be generated.

The WDT operates at a 40kHz clock of the embedded RC oscillator.

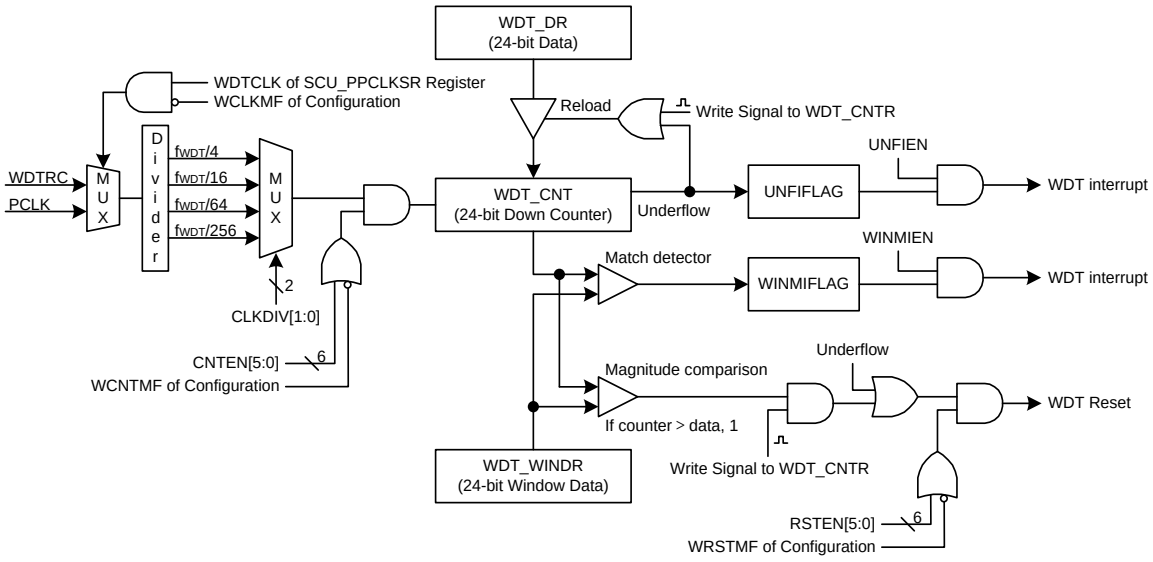
The WDT operations are listed below:

- 24-bit down counter (WDT_CNT)
- Reset or periodic interrupt selection
- Count clock selection
- Watchdog overflow output signal generation
- Counter window function

7.1 WDT block diagram

Figure 23 shows a block diagram of the WDT.

Figure 23. WDT Block Diagram



NOTE: When a reload signal is generated, the WDT_DR value is reloaded to WDT_CNT register, after 1-clock delay, with the clock selected by the CLKDIV bits.

8 Real Timer Clock and Calendar (RTCC)

The Real Timer Clock and Calendar (RTCC) has a function for RTC (Real Time Clock) and calendar operations.

The internal structure of the RTCC is implemented with the clock source select circuit, second/minute/hour/day/week/month/year counter circuits, alarm circuit, output select circuit, and error correction circuit.

The RTCC is an independent BCD counter. The RTCC circuitry and the related control bits are not reset by the system reset other than the POR/WAKUP3.

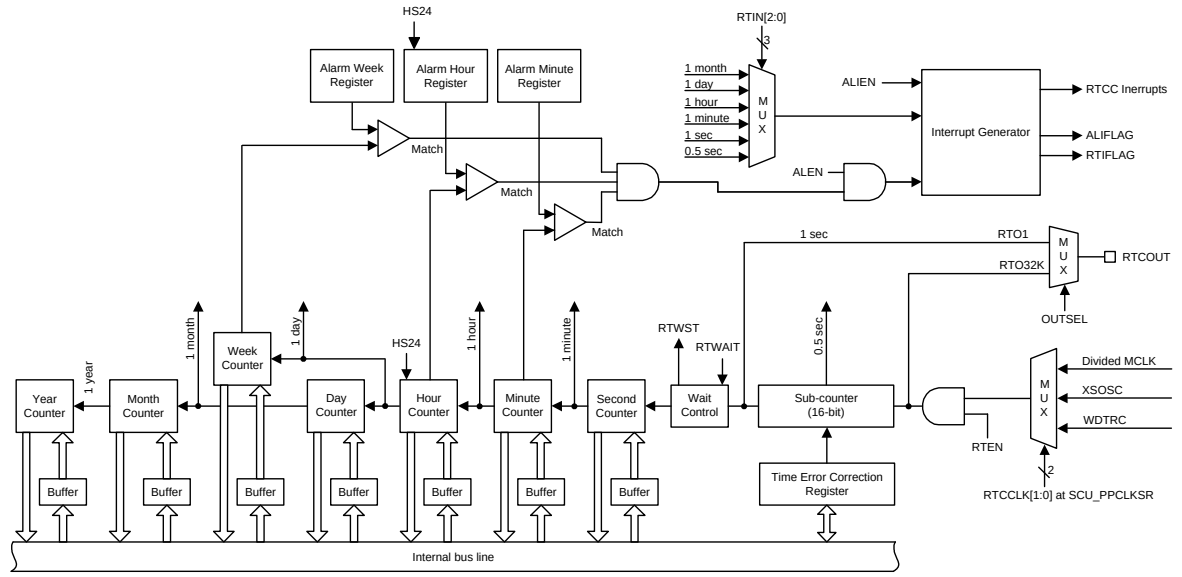
The main operations of the RTCC include the followings:

- Calendar counting 0.5 seconds, seconds, minutes, hours, days, weeks, months, and years up to the year 2099
- Time error correction function
- Alarm function with interrupt
- Wake-up possibility from DEEP SLEEP mode

8.1 RTCC block diagram

Figure 24 shows a block diagram of the RTCC.

Figure 24. RTCC Block Diagram



NOTE: Time in the block diagram is based on 32.768 kHz.

9 Timer counters

9.1 Timer counter 40/41/42/43

Each of the Timer counters 40/41/42/43 is a 16-bit general purpose timer with two outputs. It has an independent 16-bit counter and a dedicated prescaler that feeds a counting clock. It supports periodic timers, PWM pulses, one-shot and capture modes.

The main purpose of this timer is to work as a periodical tick timer or to provide a wake-up source.

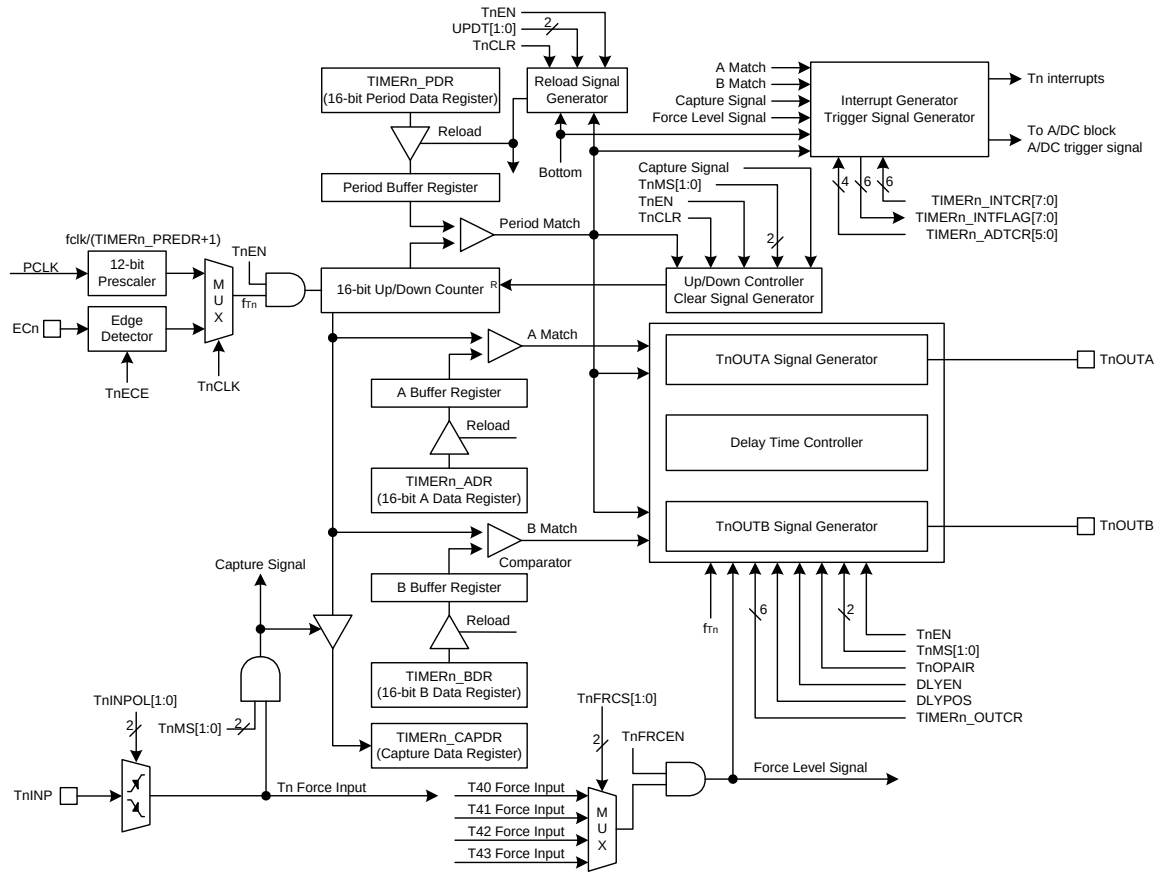
The operations of the timer counters 40/41/42/43 include the followings:

- 12-bit prescaler and 16-bit up-counter
- Interval timer, One-shot timer, Back-to-back, and Capture modes
- Counter sharing function to connect each other
- Synchronous start and clear function

9.1.1 Timer counter 40/41/42/43 block diagram

Figure 25 shows a block diagram of the timer block unit.

Figure 25. Timer Counter n Block Diagram (n = 40, 41, 42, and 43)



NOTES:

1. Period/A/B match interrupts except for bottom can occur in interval mode.
2. Period match interrupt only can occur in capture mode.
3. 16-bit up/down counter in capture mode is cleared to “0000H” after the counter value is loaded to the TIMERn_CAPDR register at a valid edge.
4. The TnEN bit is automatically cleared to logic “0b” after one pulse is generated at one-shot interval mode.
5. After the TnEN bit is set, the counting of the TIMERn_CNT may be delayed by 2 clocks or more.
6. The high/low level width of the ECn clock should be longer than the PCLK clock period.

9.1.2 Pins for timer counter 40/41/42/43

Table 11. Pins and External Signals for Timer Counter n (n = 40, 41, 42, and 43)

Pin name	Type	Description
ECn	I	External clock input
TnINP	I	Capture or force input
TnOUTA	O	Timer A output
TnOUTB	O	Timer B output

9.2 Timer counter 50

A timer block includes a single channel 16-bit general purpose timer. This timer has an independent 16-bit counter and a dedicated prescaler that feeds a counting clock. It supports periodic timer, PWM pulse, one-shot timer and capture mode. Additional free-run timer is optionally provided.

Main purpose of this timer is to work as a periodical tick timer or to provide a wake-up source.

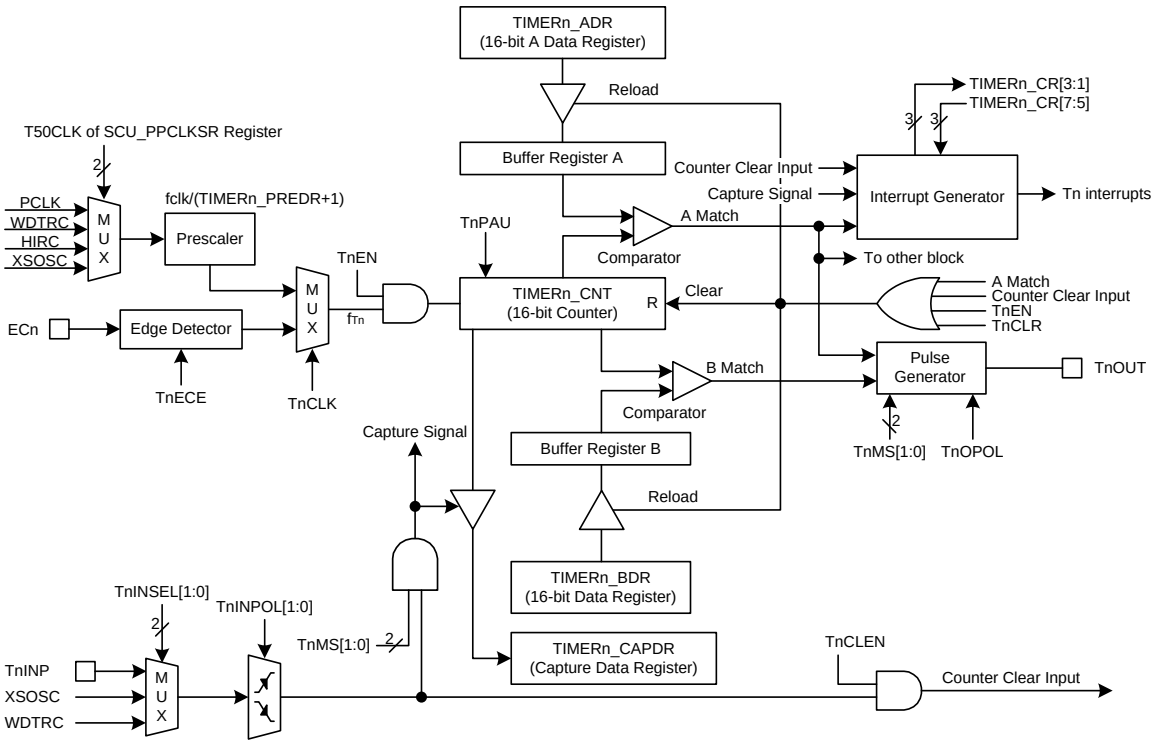
The timer counter 50 features the followings:

- 16-bit up-counter and 8-bit prescaler
- Interval timer, One-shot timer, PWM pulse, and Capture mode
- Synchronous start and clear function
- Low power operation with WDTRC or XSOSC

9.2.1 Timer counter 50 block diagram

Figure 26 shows a block diagram of the timer block unit.

Figure 26. Timer Counter n Block Diagram (n = 50)



NOTES:

1. TnEN is automatically cleared to logic '0' after one pulse is generated in PPG one-shot interval mode.
2. After the TnEN bit is set, the counting of the TIMERn_CNT may be delayed by 2 clocks or more.
3. The counter clear input can control the wake-up operation in SLEEP mode by suppressing A-match interrupt.
4. The high/low level width of the ECn clock should be longer than the PCLK clock period.
5. The capture and counter clear input interrupts cannot be used as a wake-up source in DEEP SLEEP mode. That is, these interrupts will not be generated in DEEP SLEEP mode.

9.2.2 Pins for timer counter 50

Table 12. Pins and External Signals for Timer Counter 50 (n = 50)

Pin name	Type	Description
ECn	I	External clock input
TnINP	I	Capture/Clear input
TnOUT	O	PWM/one-shot output

9.3 Timer counter 60

A timer block includes a single channel 16-bit general purpose timer. This timer has an independent 16-bit counter and 100Hz RC oscillator that feeds a counting clock. It supports only a periodic timer.

Main purpose of this timer is to provide a wake-up source in DEEP SLEEP mode 3 (SHUT DOWN).

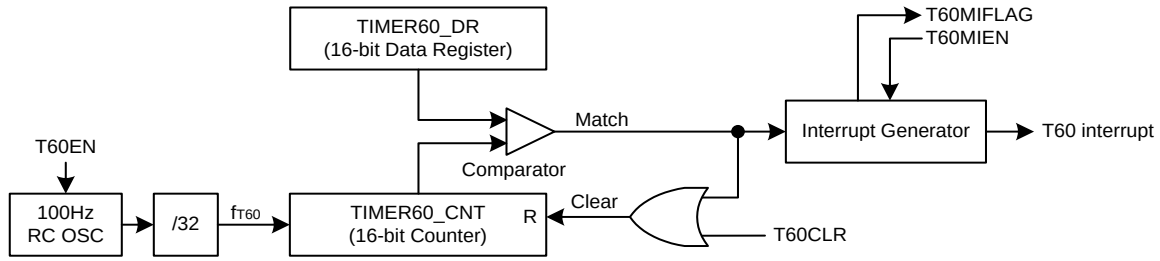
The timer counter 60 features the followings:

- 16-bit up-counter and interval timer mode
- Synchronous start and clear function
- Low power operation with an internal 100Hz RC oscillator

9.3.1 Timer counter 60 block diagram

Figure 27 shows a block diagram of the timer counter 60.

Figure 27. Timer Counter 60 Block Diagram



NOTES:

1. The TIMER60_DR register must be written while the timer counter 60 is disabled.
2. This timer is primarily intended to be used as a wake-up source in DEEP SLEEP mode 3 (SHUT DOWN).
3. When this timer is used in RUN mode, pay attention to the frequency deviation of 100Hz RC oscillator.

10 High speed 12-bit ADC

Analog-to-Digital Converter (ADC) of the A31L22x series allows conversion of an analog input signal to a corresponding 12-bit digital value. Its A/D module has eight analog inputs as shown in Figure 28.

Output of the multiplexer is the input into the converter, which generates the result through successive approximation.

The A/D module includes seven registers: control register (ADC_CR), data register (ADC_DR), prescaler data register (ADC_PREDR), oversampling control register (ADC_OVSCR), interrupt enable and status register (ADC_IESR), sampling time register (ADC_SAMR), and channel selection register (ADC_CHSELR).

The A/D module supports single, sequential, and continuous conversion modes.

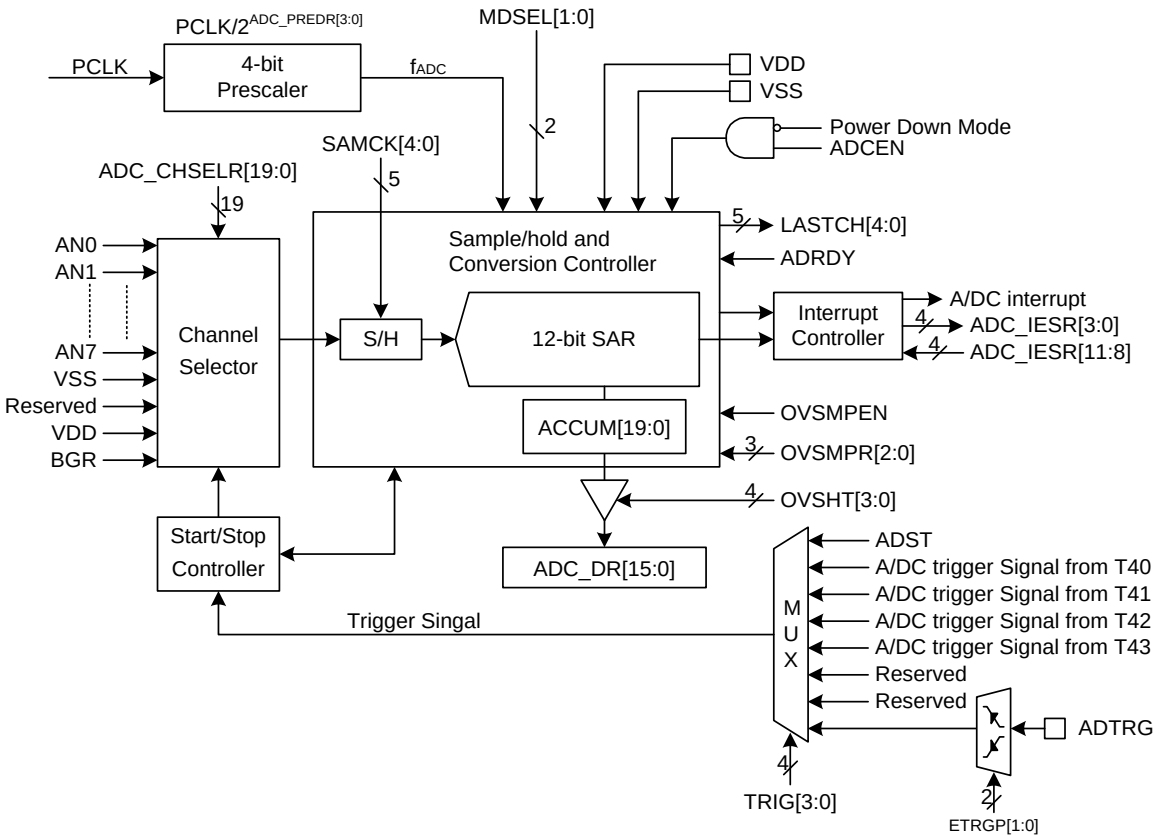
Main features of the ADC are listed in the followings:

- 8-channel of analog inputs
- S/W (ADST), timer trigger (T40/41/42/43 ADC trigger signal), and external trigger supported
- Conversion time: Up to 2us with 12 clocks + at least 4 sample/hold clocks
- 4-bit Prescaler and 16-bit data registers
- Up to 256 over sampling
- Single, sequential, and continuous conversion modes

10.1 12-bit ADC block diagram

Figure 28 shows a block diagram of the ADC block.

Figure 28. 12-bit ADC Block Diagram



NOTE: The external trigger input signal, ADTRG, should be slower than a system clock frequency.

10.2 Pins for 12-bit ADC

Table 13. Pins and External Signals for 12-bit ADC

Pin name	Type	Description
AN0	A	ADC Input 0
AN1	A	ADC Input 1
AN2	A	ADC Input 2
AN3	A	ADC Input 3
AN4	A	ADC Input 4
AN5	A	ADC Input 5
AN6	A	ADC Input 6
AN7	A	ADC Input 7

NOTE: A=Analog

11 Comparator 0/1

The A31L22x series includes two comparator modules.

Each comparator module has three registers: control register (CMP_CR), status register (CMP_SR), and reference control register (CMP_RCR). This comparator module has an internal reference circuit too.

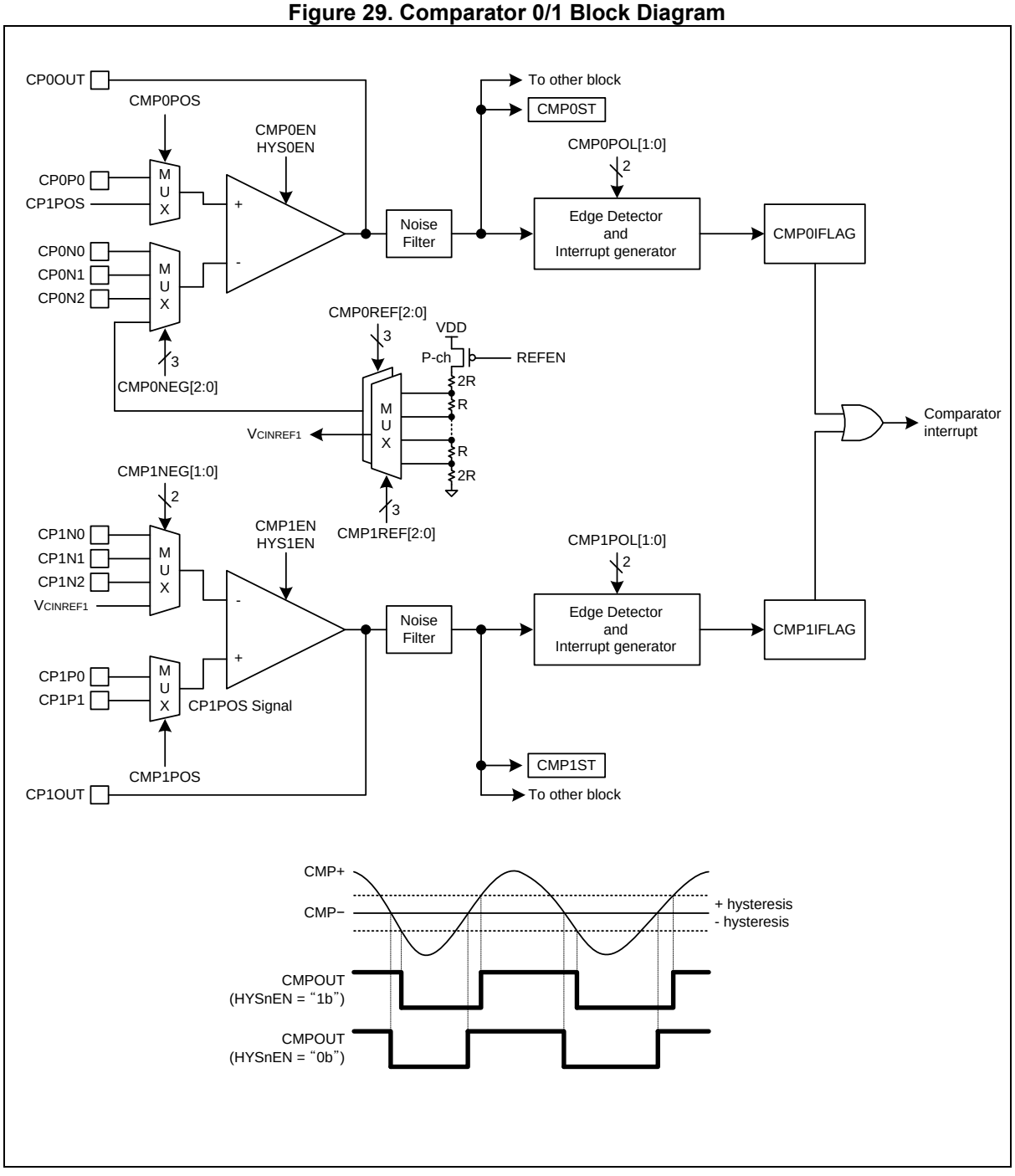
The comparator module features the followings:

- External analog inputs
- Hysteresis function
- Low and fast speed selectable
- Wake-up possible from DEEP SLEEP mode

11.1 Comparator 0/1 block diagram

Figure 29 shows a block diagram of the comparator block.

Figure 29. Comparator 0/1 Block Diagram



11.2 Pins for comparator 0/1

Table 14. Pins and External Signals for Comparator 0/1

Pin name	Type	Description
CP0P0	A	Comparator 0 positive input
CP0N0	A	Comparator 0 negative input
CP0N1	A	Comparator 0 negative input
CP0N2	A	Comparator 0 negative input
CP0OUT	A	Comparator 0 output
CP1P0	A	Comparator 1 positive input
CP1P1	A	Comparator 1 positive input
CP1N0	A	Comparator 1 negative input
CP1N1	A	Comparator 1 negative input
CP1N2	A	Comparator 1 negative input
CP1OUT	A	Comparator 1 output

12 USART 10, UART 0, and LPUART 0

12.1 USART 10

Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) is a highly flexible serial communication device.

The USART 10 of the A31L22x series features the followings:

- Full duplex operation. (independent serial receive and transmit registers)
- Asynchronous or synchronous operation
- Baud rate generator
- Supports serial frames with 5,6,7,8, or 9 Data bits and 1 or 2 Stop bits
- Odd or even parity generation, and parity check supported by hardware.
- Supports receive character detection and receive time out function
- Supports Local Interconnection Network (LIN)
- Data OverRun Detection
- Framing Error Detection
- Three separate interrupts on TX completion, TX data register empty and RX completion
- Double Speed Asynchronous communication mode
- Up to 16MHz data transfer for SPI

12.1.1 USART 10 block diagram

Figure 30 shows a block diagram of the UART block.

Figure 30. UART Block Diagram of USART and LIN (n = 10)

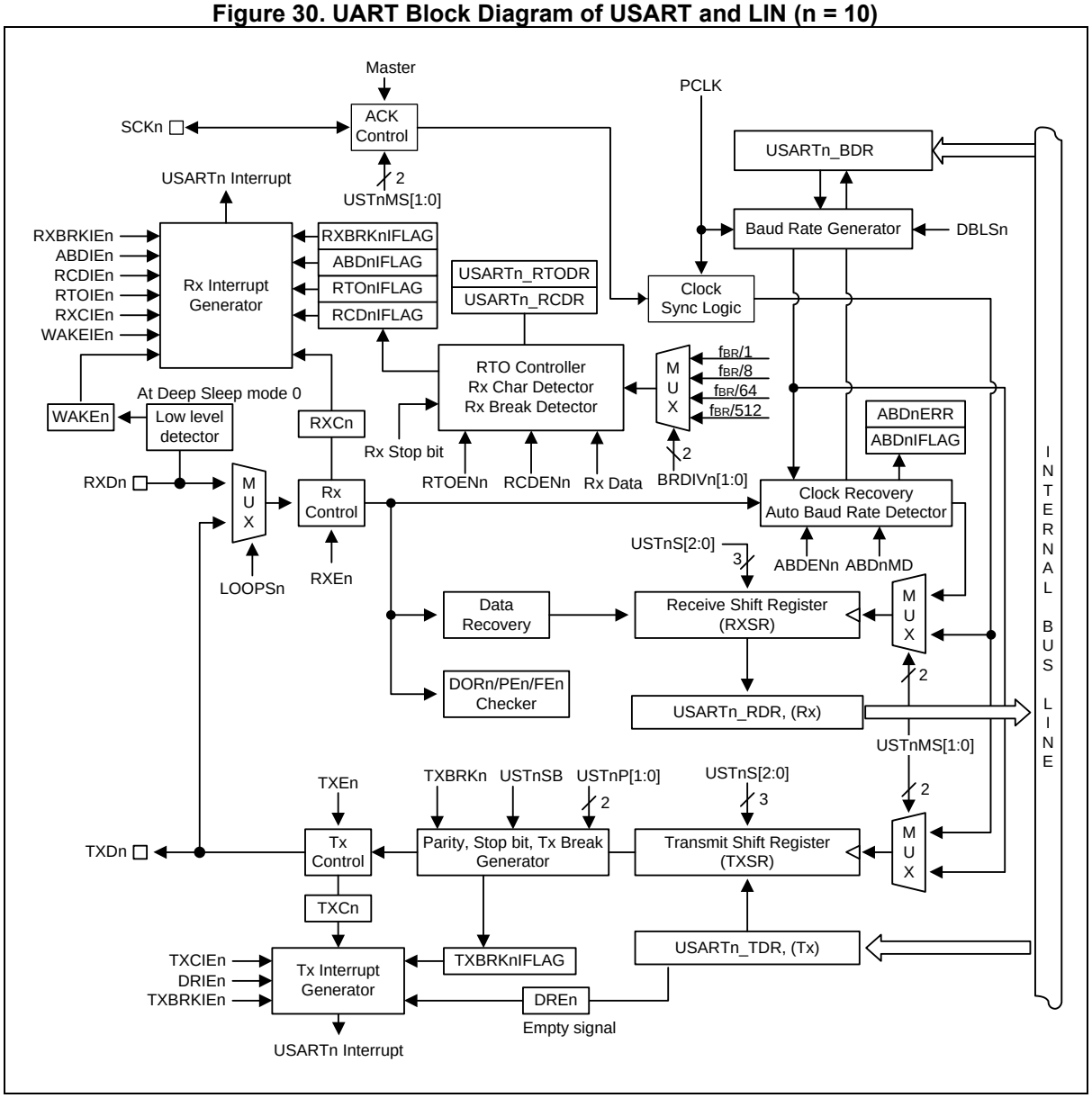
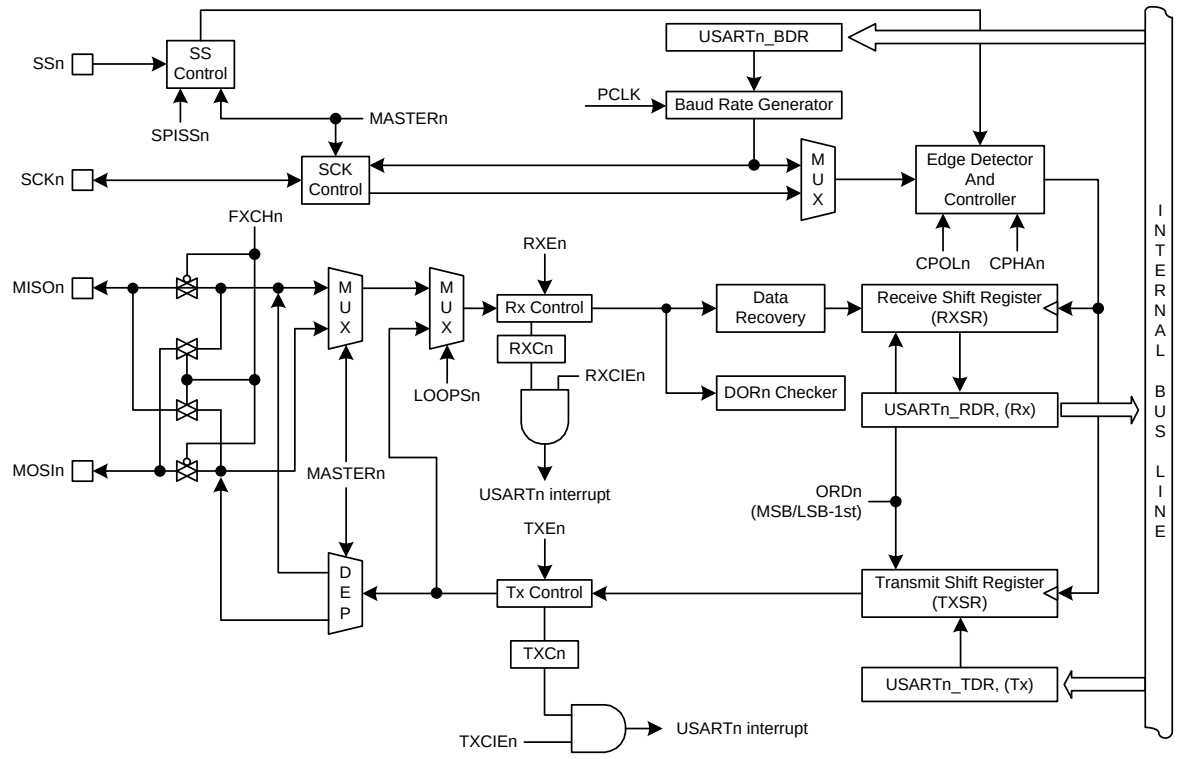


Figure 31 shows a block diagram of the SPI block.

Figure 31. SPIn Block Diagram of USART (n = 10)



NOTES:

1. The clock frequency of SCKn should be less than or equal to PCLK/2.

12.1.2 Pins for USART 10

Table 15. Pins and External Signals for USART 10

Pin name	Type	Description
TXDn	O	UART Channel n transmit output
RXDn	I	UART Channel n receive input
SSn	I/O	SPIn Slave select input / output
SCKn	I/O	SPIn Serial clock input / output
MOSIn	I/O	SPIn Serial data (Master output, Slave input)
MISOn	I/O	SPIn Serial data (Master input, Slave output)

12.2 UART 0

The A31L22x series has built-in 1-channel of UART module (Universal Asynchronous Receiver/Transmitter).

Users can read the UART operation status including the error status from the status register.

A baud rate generator, which generates proper baud rate, exists for each UART channel. This baud rate generator divides down the PCLK to the frequency ranging from 1 to 65536. Then, the baud rate is generated using a 1:16 clock and an 8-bit precision clock tuning function.

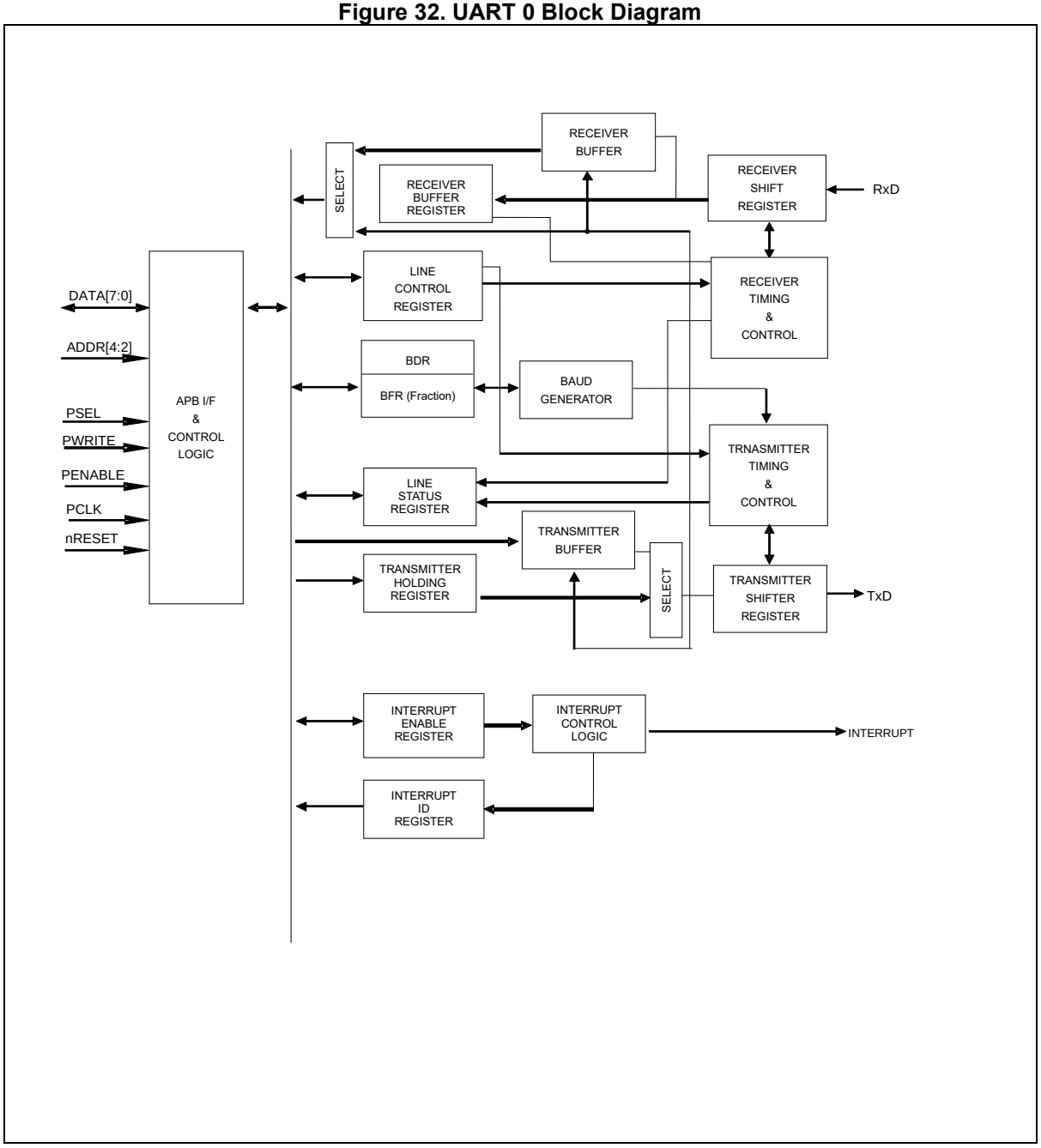
The UART 0 of the A31L22x series features the followings:

- Compatible with 16450 UART
- Configurable standard asynchronous control bit (Start, Stop, and Parity)
- Programmable 16-bit fractional baud rate generator
- Programmable serial communication
- 5-, 6-, 7- or 8- bit data transfer
- Even, odd, or no-parity bit insertion and detection
- 1-, 1.5- or 2-Stop bit-insertion and detection
- 16-bit baud rate generation with 8-bit fraction control
- Hardware inter-frame delay function
- Stop bit error detection
- Detail status register

12.2.1 UART 0 block diagram

Figure 32 shows a block diagram of the UART block.

Figure 32. UART 0 Block Diagram



12.2.2 Pins for UART 0

Table 16. Pins and External Signals for UART 0 (n = 0)

Pin name	Type	Description
TXDn	O	UART Channel n transmit output
RXDn	I	UART Channel n receive input

12.3 LPUART 0

The A31L22x series has built-in 1-channel of low power UART module (Universal Asynchronous Receiver/Transmitter).

This LPUART (Low Power UART) supports asynchronous serial communication up to 9600bps in DEEP SLEEP mode when using a 32.768kHz sub-oscillator. It also supports 1-wire half-duplex communication.

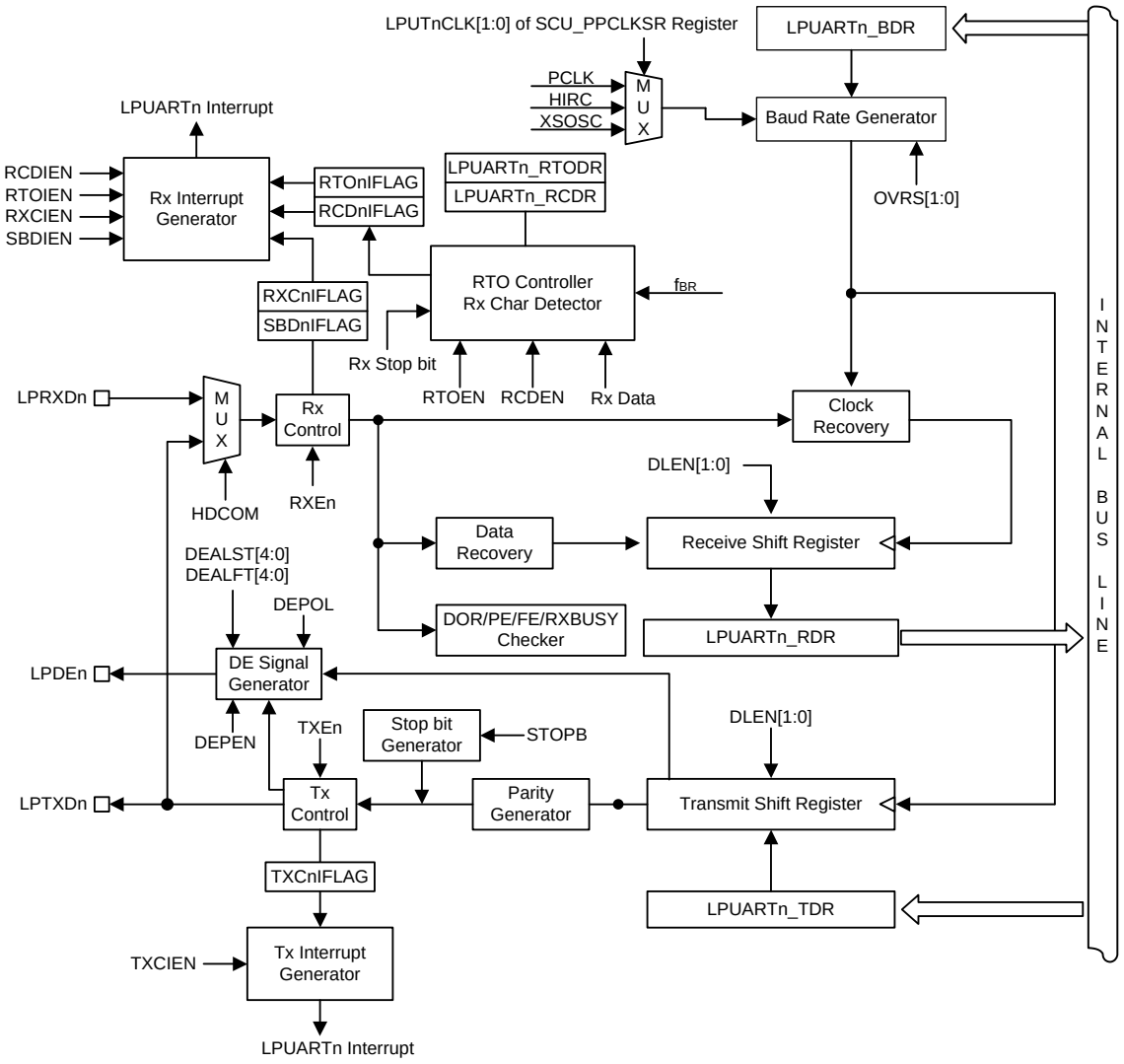
The LPUART 0 of the A31L22x series features the followings:

- Full-duplex and half-duplex operations
- Baud rate generator
- Supports serial frames with 5,6,7, or 8 Data bits and 1 or 2 Stop bits
- Odd or even parity generation, and parity check supported by hardware
- Supports receive character detection and receive time out function
- Baud rate compensation function
- Supports up to 9600pbs with 32.768kHz sub-oscillator
- Data OverRun Detection
- Framing Error Detection
- Double speed asynchronous communication mode

12.3.1 LPUART 0 block diagram

Figure 33 shows a block diagram of the LPUART block.

Figure 33. LPUART Block Diagram (n = 0)



NOTES:

1. If the XSOSC (32.768kHz) is used for a clock of the LPUARTn, the maximum baud rate can be up to 9600bps.
2. A clock of PCLK should be faster than or equal to a clock of the LPUARTn.
3. Data to be transmitted should be written to the LPUARTn_TDR register after checking if the TXCIFLAG bit is set to “1b”.

12.3.2 Pins for LPUART

Table 17. Pins and External Signals for LPUART 0

Pin name	Type	Description
LPTXDn	O	Low Power UART n transmit output
LPRXDn	I	Low Power UART n receive input
LPDEn	O	Low Power UART n DE signal output

13 I2C 0, SPI 1

13.1 I2C 0 interface

I2C is one of industrial standard serial communication protocols, which uses 2 bus lines, Serial Data Line (SDAn) and Serial Clock Line (SCLn). These are used to exchange data.

Because both of the SDAn and SCLn lines are open-drain outputs, each line needs a pull-up resistor (n = 0).

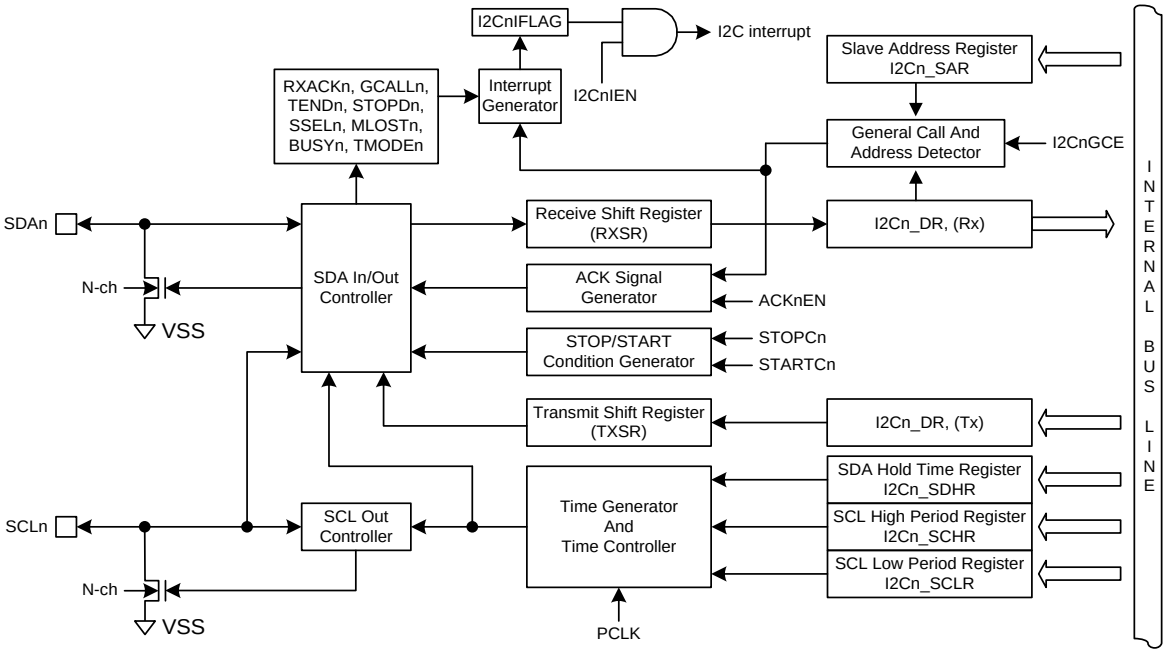
The I2C interface 0 of A31L22x series features the followings:

- Compatible with I2C bus standard
- Multi-master operation
- Up to 1MHz data transfer read speed
- 7-bit address
- Two slave addresses supported
- Master and slave operations
- Bus busy detection

13.1.1 I2C 0 block diagram

Figure 34 shows a block diagram of the I2C block.

Figure 34. I2C Block Diagram (n = 0)



NOTE: When the corresponding port of I2C is a sub-function for the SCLn/SDAn pin, the SCLn/SDAn pins are automatically set as N-channel open-drain outputs and the input latch is read when reading the pins. The corresponding pull-up resistor is determined by the control register.

13.1.2 Pins for I2C 0

Table 18. Pins and External Signals for I2C (n = 0)

Pin name	Type	Description
SCLn	I/O	I2C Channel n Serial clock bus line (open-drain)
SDAn	I/O	I2C Channel n Serial data bus line (open-drain)

13.2 SPI 1 interface

The SPI interface enables synchronous serial data transfer between external serial devices. It allows full-duplex communication using 4-wires (MOSIn, MISOn, SCKn, SSn).

It supports master and slave modes, and selects serial clock (SCKn) polarity. In addition, for the data transmission, it selects whether to transfer LSB first or MSB first.

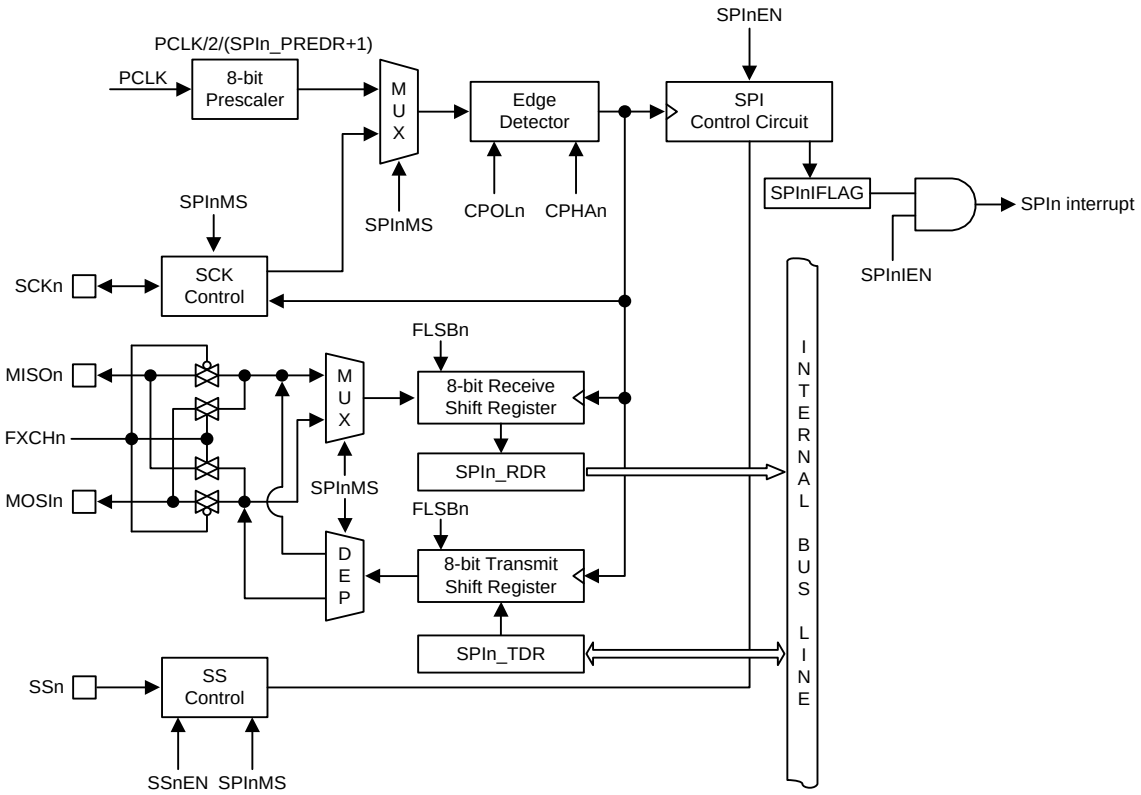
The SPI 1 of the A31L22x series features the followings:

- Master and slave modes supported
- Clock polarity selection
- Up to 16MHz data transmission
- Exchangeable MOSIn and MISOn functions

13.2.1 SPI 1 block diagram

Figure 35 shows a block diagram of the SPI block.

Figure 35. SPI Block Diagram (n = 1)



NOTES:

1. The clock frequency of the SCKn should be less than or equal to the PCLK/2.
2. Interrupts of the SPIn occur only when one byte transmission/reception finishes. So, the status (SPInMS and SSnHIGH) bits should be checked by S/W.

13.2.2 Pins for SPI 1

Table 19. Pins and External Signals for SPI (n = 1)

Pin name	Type	Description
SSn	I/O	SPIn Slave select input / output
SCKn	I/O	SPIn Serial clock input / output
MOSIn	I/O	SPIn Serial data (Master output, Slave input)
MISOn	I/O	SPIn Serial data (Master input, Slave output)

14 CRC and checksum

A CRC (Cyclic Redundancy Check) generator is used to obtain 8/16/32-bit CRC code of Flash ROM and any data stream.

Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of functional safety standards, they offer means of verifying Flash memory's integrity.

The CRC generator helps computing the signature of the software during runtime, comparing with a reference signature.

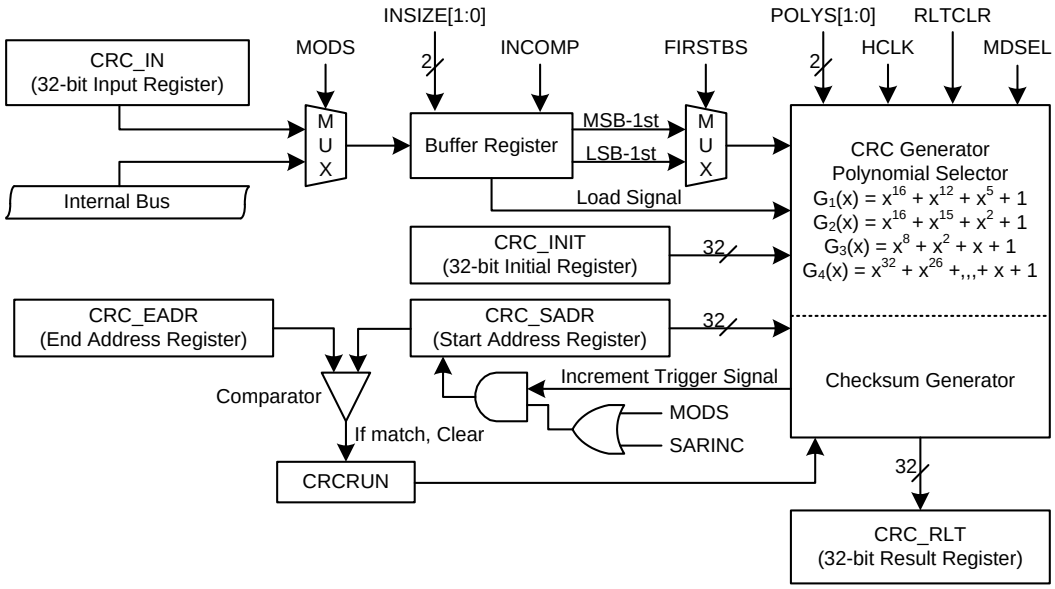
The CRC generator of the A31L22x series has following features:

- Auto CRC and user CRC mode
- CRC-CCITT ($G_1(x) = x^{16} + x^{12} + x^5 + 1$) supported
- CRC-16 ($G_2(x) = x^{16} + x^{15} + x^2 + 1$) supported
- CRC-8 ($G_3(x) = x^8 + x^2 + x + 1$) supported
- CRC-32 ($G_4(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$) supported
- CRC and checksum mode
- CRC/checksum start address auto increment (User mode only)

14.1 CRC and checksum block diagram

Figure 36 shows a block diagram of the CRC and checksum interface block.

Figure 36. CRC and Checksum Block Diagram



NOTES:

1. The operation is finished after calculating from the address specified by the CRC_SADR to the address specified by the CRC_EADR, in auto mode or when SARINC=1.
2. The CRC_SADR and CRC_EADR have the same value after finishing the operation.
3. The end address in the CRC_EADR must be greater than the start address in CRC_SADR.
4. The end address must be at least 0x7C from the start address in “Auto mode”.
5. The CRC_SADR/CRC_EADR in “Auto mode” should have any value in Flash memory area (0x10000000 to 0x10007FFF).
6. The CPU will be held at “Auto mode” if the CPU is in the Flash memory, and global interrupts should be disabled by software.
7. Users must set the HCLK frequency to be less than or equal to 20MHz in “Auto mode” by configuring the MODS bit of the CRC_CR register.
8. In Auto mode, the CRC_CR can’t be written and the CRC_RLT can’t be read.

15 Temperature Sensor (TS)

The temperature sensor (TS) is a ring-oscillator type and can be used to measure the junction temperature of the device. The nominal frequency at 30℃ is about 1.1MHz and it varies from 0.7 to 1.45 [MHz] as the temperature changes from -20℃ to +105℃.

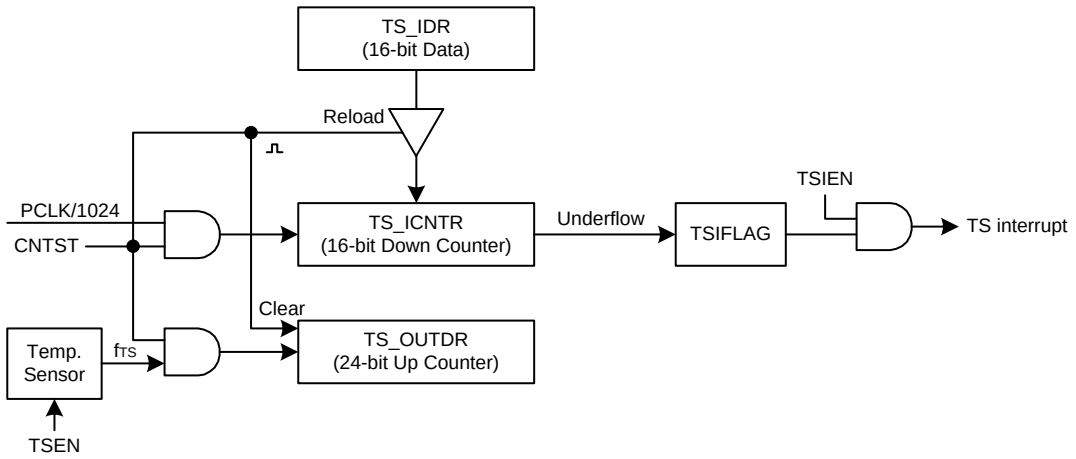
The TS of the A31L22x series has the following features:

- -20℃ to 105℃, wide range of operating temperature
- 16-bit interval down counter (to count the frequency of temperature sensor)
- 24-bit data register (to save the counted value of temperature sensor frequency)

15.1 TS block diagram

Figure 37 shows a block diagram of the temperature sensor block.

Figure 37. Temperature Sensor Block Diagram



NOTE: The CNTST bit will be cleared to “0b” after the underflow of TS_ICNTR.

16 Electrical characteristics

Unless otherwise specified, test conditions for DC characteristics are as follows:

- T_A = - 40 °C to +85°C (Commercial grade) or T_A = - 40 °C to + 105°C (Industrial grade)
- VDD = 1.71V to 3.6V

NOTE: Refer to **Figure 58. A31L22x Series Numbering Nomenclature** for device part number by Commercial and Industrial grade.

16.1 Absolute maximum ratings

Absolute maximum ratings are limiting values of operating and environmental conditions, which should not be exceeded under the worst possible conditions.

Table 20. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Remark
Supply voltage	VDD	-0.3 to +4.0	V	–
Normal pin	V_I	-0.3 to VDD +0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3 to VDD +0.3	V	
	I_{OH}	-15	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	ΣI_{OH}	-60	mA	Maximum current (ΣI_{OH})
	I_{OL}	20	mA	Maximum current sunk by (I_{OL} per I/O pin)
	ΣI_{OL}	160	mA	Maximum current (ΣI_{OL})
5V tolerant pin	VI	-0.3 to +6.0	V	Voltage on any pin with respect to VSS
Total power dissipation	P_T	600	mW	–
Storage temperature	T_{STG}	-65 to +150	°C	–

16.2 Recommended operating conditions

Table 21. Recommended Operating Conditions

Parameter	Symbol	Conditions			Min	Max	Units
Operating voltage	VDD	fx = 32 to 38kHz	Sub clock		1.71	3.6	V
		fx = 2.0 to 4.2MHz	Main clock	Ceramic	1.8	3.6	
		fx = 2.0 to 16MHz		Crystal	2.7	3.6	
		fx = 2.0 to 32MHz	External clock		3.0	3.6	
		fx = 40kHz	Internal RC		1.71	3.6	
		fx = 2.5 to 32MHz			1.71	3.6	
Input voltage	V_{IN}	Normal Pin			-0.3	VDD+0.3	V
		5V tolerance Pins, PD[4:3]	2.0V ≤ VDD ≤ 3.6V		-0.3	5.5	
			1.71V ≤ VDD < 2.0V		-0.3	5.0	
Operating temperature	T_{OPR}	VDD = 1.71 to 3.6V (Commercial grade)			-40	85	°C
		VDD = 1.71 to 3.6V (Industrial grade)			-40	105	

16.3 ADC characteristics

Table 22. ADC Characteristics

(TA = 25℃)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Resolution	–	–		–	12	–	bit
Integral non-linearity	INL	VDD=1.71V – 3.6V		–	–	±6	LSB
Differential non-linearity	DNL			–	±1	±2	
Zero offset error	ZOE			–	–	±5	
Full scale error	FSE			–	–	±5	
Conversion time	t_{CONV}	VDD=1.71V – 3.6V		2	–	–	µs
Analog input voltage	V_{AN}	–		VSS	–	VDD	V
ADC stabilization time	t_{STAB}	–		–	–	16	$1/f_{ADC}$
Band gap reference buffer voltage	V_{ADCBUF}	Conversion time: 8us		890	940	990	mV
ADC input leakage current	I_{AN}	VDD=3.0V		–	–	2	µA
ADC current	I_{ADC}	Enable	VDD=3.0V, f_{ADC}=8MHz	–	400	800	µA
		Disable		–	–	10	nA

NOTES:

1. Zero offset error is a difference between 0x000 and the converted output for zero input voltage (VSS).
2. Full scale error is a difference between 0xFFF and the converted output for top input voltage (VDD).

16.4 Power-on Reset characteristics

Table 23. Power-on Reset Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Reset release level	V_{POR}	–	–	1.2	–	V
Hysteresis	△V	–	–	0.1	–	V
VDD voltage rising time	t_R	0.2V to 2.0V	0.05	–	100	V/ms
POR current	I_{POR}	–	–	21	40	nA

16.5 Comparator characteristics

Table 24. Comparator Characteristics

(TA = 25℃)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Input offset voltage	VOF	VDD=3.0V, VIN=1/2VDD		–	±4	±20	mV
Operating voltage	VDD	All comparator pins		1.71	–	3.6	V
Startup time	t_{START}	Fast speed		–	15	20	µs
		Slow speed		–	20	25	
Propagation delay	t_{DELAY}	1.71V ≤ VDD ≤ 2.7V	Fast Speed	–	1.2	4	µs
		2.7V ≤ VDD ≤ 3.6V		–	0.8	2	
		1.71V ≤ VDD ≤ 2.7V	Slow Speed	–	2.5	6	
		2.7V ≤ VDD ≤ 3.6V		–	1.8	3.5	
Hysteresis	△V+	VDD=3.0V, VIN- = 1/2VDD, HYSnEN=1		5	10	20	mV
	△V-			-20	-10	-5	
Minimum input level	V_{INMIN}	HYSnEN=1		50	–	–	mVp-p
Reference resistors	R_{REF}	VDD=3.0V		21	30	39	kΩ
Comparator current	ICMP	Enable, fast speed	VDD=3.0V	–	3.5	5	µA
		Enable, slow speed		–	1.0	2	
		Disable		–	–	0.02	

16.6 Temperature Sensor characteristics

Table 25. Temperature Sensor Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Temp. linearity	T_{LIN}	Down to -20℃		–	±4	–	℃
Frequency variation	△F	(F(T2) – F(T1)) ÷ (T2 – T1)		1.8	3.2	5.7	kHz/℃
Frequency deviation	–	△F ÷ F(30)		0.25	0.35	0.45	%
Sensor current	I_{TS}	Enable	VDD = 3.0V	–	10	20	uA
		Disable		–	–	10	nA
Startup time	t_{START}	–		–	–	500	µs

NOTES:

1. Temperature = {(F(T) – F(30)) ÷ △F} + 30 [℃], Where: T1 = 30℃, T2 = 85℃(Commercial grade) or 105℃(Industrial grade)
2. F(T1) [kHz] is the temperature sensor output frequency acquired at 30℃.
3. F(T2) [kHz] is the temperature sensor output frequency acquired at 85℃(Commercial grade) or 105℃(Industrial grade).
4. F(T) [kHz] is the temperature sensor output frequency acquired at an arbitrary temperature.

16.7 Low Voltage Reset/Indicator characteristics

Table 26. Low Voltage Reset/Indicator Characteristics

(TA = 25℃)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Detection level	V_{LVR} V_{LVI}	• LVR: All levels, • LVI: Other levels except 1.50V, • 1.50V level: Rising edge voltage, • Other levels: Falling edge voltage		–	1.50	1.70	V
				1.72	1.87	2.02	
				1.87	2.02	2.17	
				2.02	2.17	2.32	
				2.17	2.32	2.47	
				2.27	2.47	2.67	
				2.44	2.64	2.84	
				2.58	2.78	2.98	
Hysteresis	△V	–		–	40	150	mV
Minimum pulse width	t_{LVRW} t_{LVIW}	–		100	–	–	µs
LVR/LVI current	$I_{LVR/LVI}$	Enable, one of two	VDD = 3V	–	200	400	nA
		Enable, both		–	250	500	
		Disable		–	–	10	

16.8 High frequency internal RC oscillator characteristics

Table 27. High Frequency Internal RC Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{HIRC}	VDD = 1.71V to 3.6V	–	32	–	MHz
Accuracy	–	T_A = -40 °C to +85 °C (commercial grade)	–	–	±2.0	%
		T_A = -40 °C to +105 °C (industrial grade)	–	–	±3.0	
Clock duty ratio	T_{OD}	–	40	50	60	%
Stabilization time	t_{HFS}	–	–	–	2	µs
IRC current	I_{HIRC}	Enable	–	300	450	µA
		Disable	–	–	10	nA

16.9 Internal Watchdog Timer RC oscillator characteristics

Table 28. Internal Watchdog Timer RC Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{WDTRC}	–	34	40	46	kHz
Stabilization time	t_{WDTS}	–	–	–	100	µs
WDTRC current	I_{WDTRC}	Enable	–	450	650	nA
		Disable	–	–	10	

16.10 Timer 60 RC oscillator characteristics

Table 29. Timer 60 RC Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Frequency	f_{T60RC}	–	50	100	200	Hz
Stabilization time	t_{T60S}	–	–	–	100	µs
T60 current	I_{T60RC}	Enable	–	200	350	nA
		Disable	–	–	10	

16.11 DC electrical characteristics

Table 30. DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH}	All input pins, nRESET	0.8VDD	–	VDD	V
Input Low Voltage	V_{IL}	All input pins, nRESET	–	–	0.2VDD	V
Input hysteresis	△V	All input pins, nRESET, VDD=3V	100	200	–	mV
Output High Voltage	V_{OH}	VDD=3V, I_{OH} = – 10mA, T_A=25˚C	VDD-1.0	–	–	V
Output Low Voltage	V_{OL}	VDD=3V, I_{OL1} = 10mA, T_A=25˚C	–	–	1.0	V
Input high leakage current	I_{IH}	All Input ports	–	–	1	µA
Input low leakage current	I_{IL}	All Input ports	– 1	–	–	µA
Pull-up resistor	R_{PU}	V_I=0V, T_A=25˚C, VDD=3V All Input ports	25	50	100	kΩ
		V_I=0V, T_A=25˚C, VDD=3V RESETB	150	250	400	
Pull-down resistor	R_{PD}	V_I=VDD, T_A=25˚C, VDD=3V All Input ports	25	50	100	kΩ
OSC feedback resistor	R_{X1}	XIN=VDD, XOUT=VSS, T_A=25˚C, VDD=3V	0.6	1.2	2.0	MΩ
	R_{X2}	T_A=25˚C, VDD=3V	4.0	7.0	14.0	MΩ

16.12 Supply current characteristics

Table 31. Supply Current Characteristics

Parameter	Symbol	Conditions			Typ	Max	Units
Supply current	I_{DD1} (main run)	f_{HIRC} = 32MHz		VDD=3V, Code executed from Flash	2.5	3.5	mA
		f_{HIRC} = 16MHz			1.5	2.1	
		f_{XIN} = 16MHz			1.4	2.0	
		f_{HIRC} = 32MHz		VDD=3V, Code executed from RAM, Flash power off	2.3	3.2	mA
		f_{HIRC} = 16MHz			1.6	2.2	
		f_{XIN} = 16MHz			1.5	2.1	
	I_{DD2} (main sleep)	f_{HIRC} = 32MHz		VDD=3V, SLEEP in Flash	1.1	1.5	mA
		f_{HIRC} = 16MHz			0.7	1.0	
		f_{XIN} = 16MHz			0.7	1.0	
		f_{HIRC} = 32MHz		VDD=3V, SLEEP in RAM, Flash power off	1.0	1.4	mA
		f_{HIRC} = 16MHz			0.6	0.8	
		f_{XIN} = 16MHz			0.6	0.8	
	I_{DD3} (sub run)	f_{SUB} = 32.768kHz (C_L: 7pF), or f_{WDTRC} = 40kHz	T_A=25°C	VDD=3V Code executed from Flash	10.0	18.0	uA
			T_A=85°C		15.0	22.9	
			T_A=105°C		20.0	30.0	
			T_A=25°C	VDD=3V, Code executed from RAM, Flash power off	9.0	17.1	uA
			T_A=85°C		14.0	25.8	
			T_A=105°C		18.0	28.9	
	I_{DD4} (sub sleep)	f_{SUB} = 32.768kHz (C_L: 7pF), or f_{WDTRC} = 40kHz	T_A=25°C	VDD=3V, SLEEP in Flash	1.9	4.8	uA
			T_A=85°C		4.5	15.8	
			T_A=105°C		9.0	21.0	
	I_{DD5}	VDD=3V DEEP SLEEP mode 0	T_A=25°C	RTCC/f_{SUB} Off	0.39	0.99	uA
			T_A=85°C		1.7	6.0	
			T_A=105°C		3.5	13.2	
			T_A=25°C	RTCC/f_{SUB} On	0.99	1.6	uA
			T_A=85°C		2.4	8.2	
			T_A=105°C		4.9	18.4	
	I_{DD7}	VDD=3V DEEP SLEEP mode 2	T_A=25°C	RTCC/f_{SUB} Off	0.29	0.7	uA
			T_A=85°C		0.7	2.5	
			T_A=105°C		1.3	5.2	
	I_{DD8}	VDD=3V DEEP SLEEP mode 3 (Shutdown)	T_A=25°C	All Off	36	72	nA
			T_A=85°C		0.2	1.2	uA
			T_A=105°C		0.7	2.3	

NOTES:

1. Where the f_{XIN} is an external main oscillator, the f_{SUB} is an external sub oscillator (ISET_I[2:0] = 0x5), and the f_{HIRC} is a high frequency internal RC oscillator.
2. All supply current items don't include the current of WDTRC oscillator and a peripheral block except when explicitly mentioned. However, it does include the current of the power-on reset (POR) block.

Figure 38. IDD4 (SLEEP mode, fSUB = 32.768 kHz) at VDD = 3V

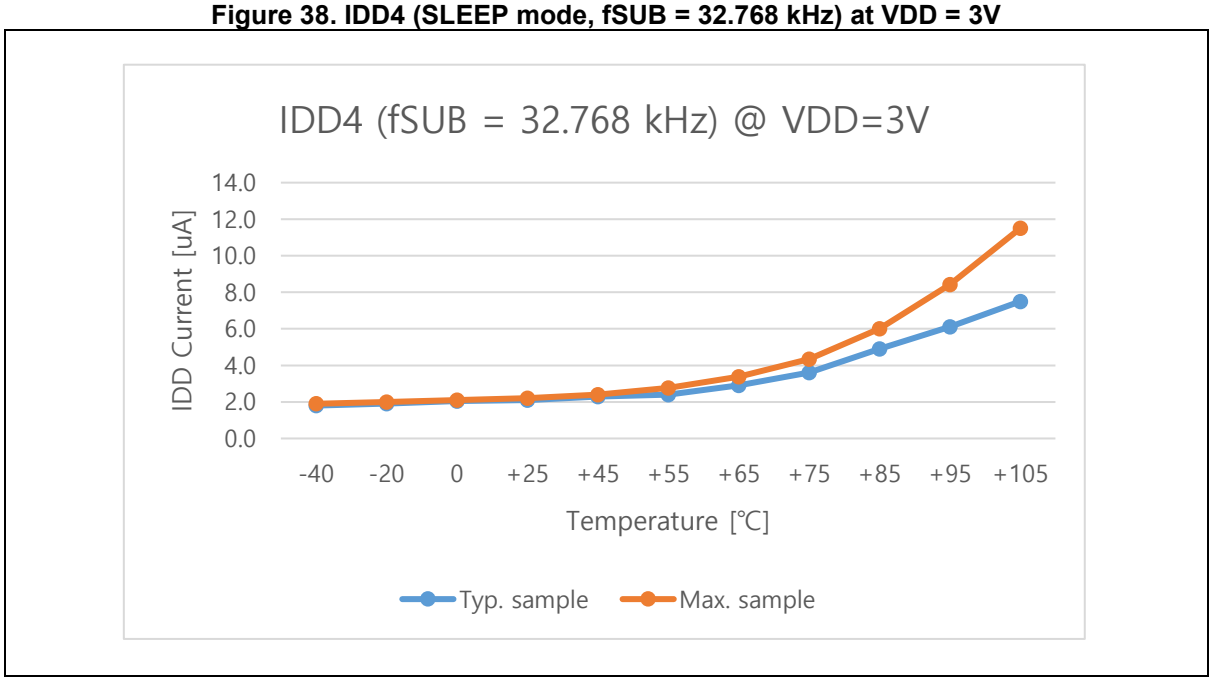


Figure 39. IDD4 (SLEEP mode, fWDTRC = 40 kHz) at VDD = 3V

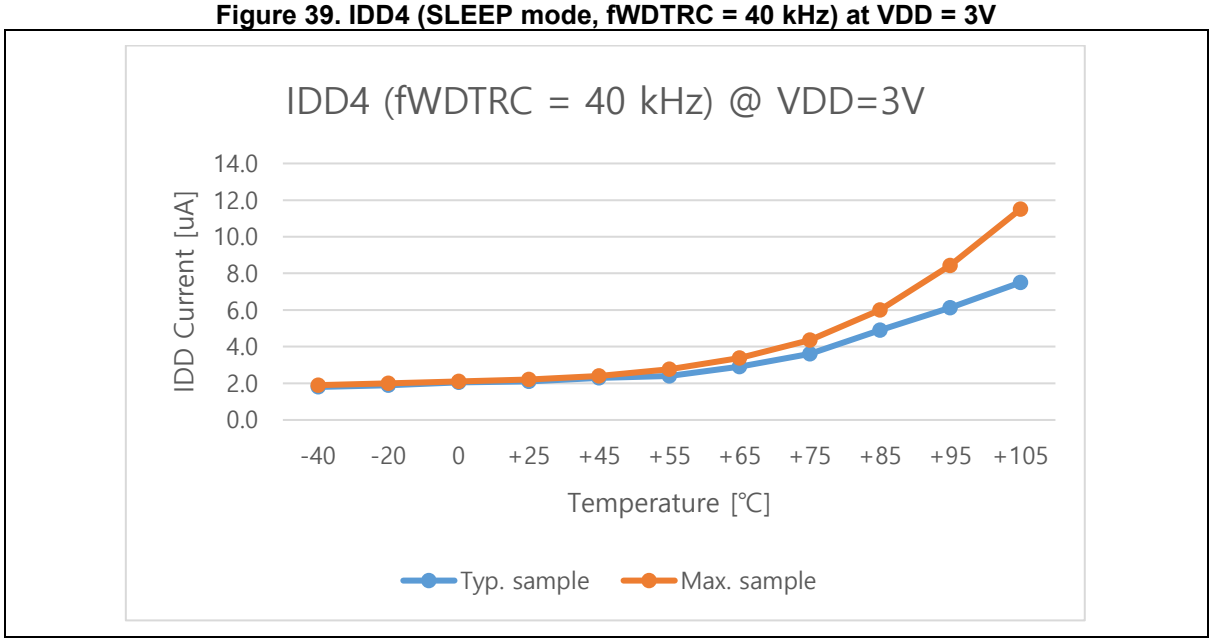


Figure 40. IDD5 (DEEP SLEEP mode 0, RTCC/fSUB Off) at VDD = 3V

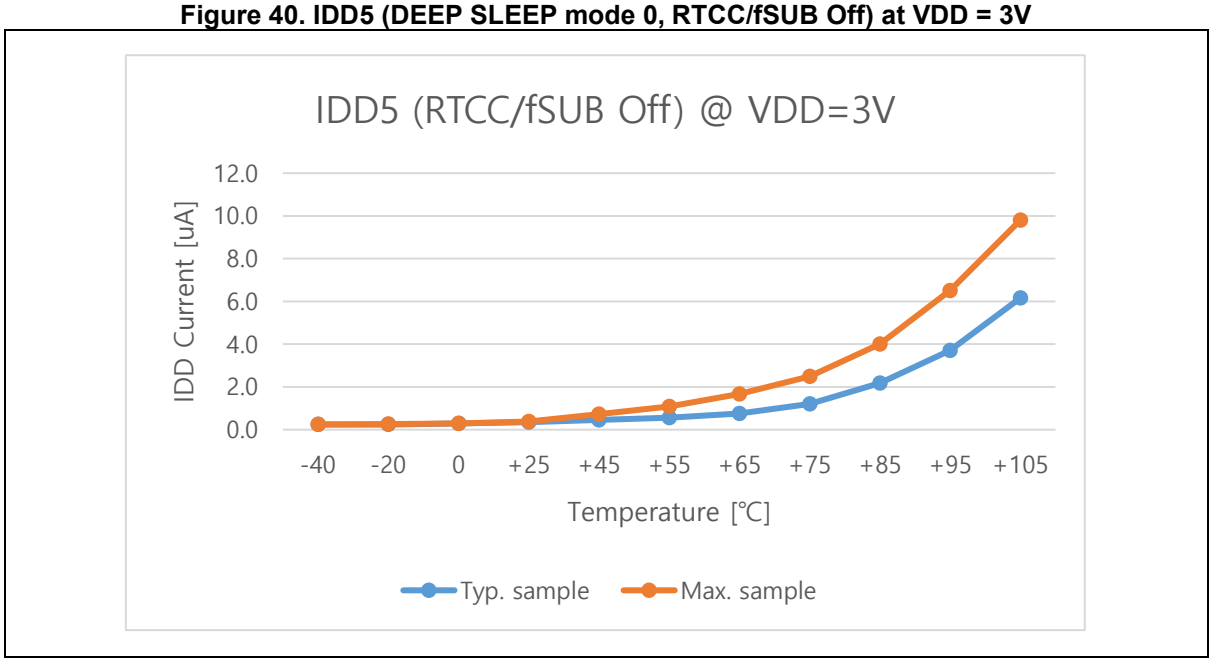


Figure 41. IDD5 (DEEP SLEEP mode 0, RTCC/fSUB On) at VDD = 3V

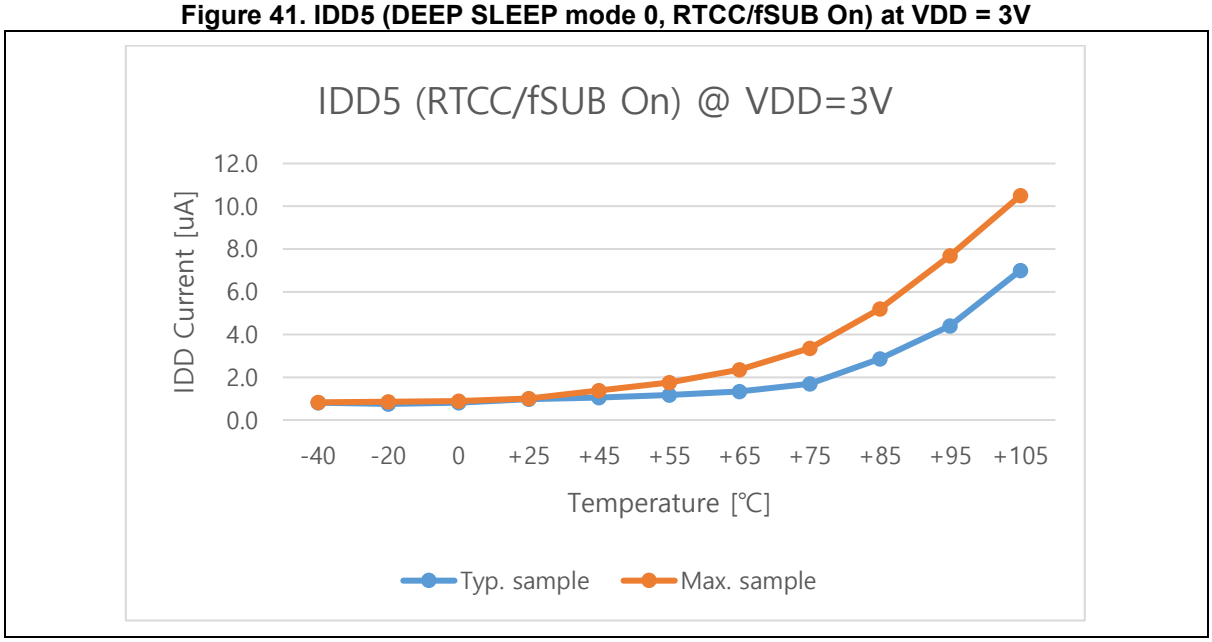
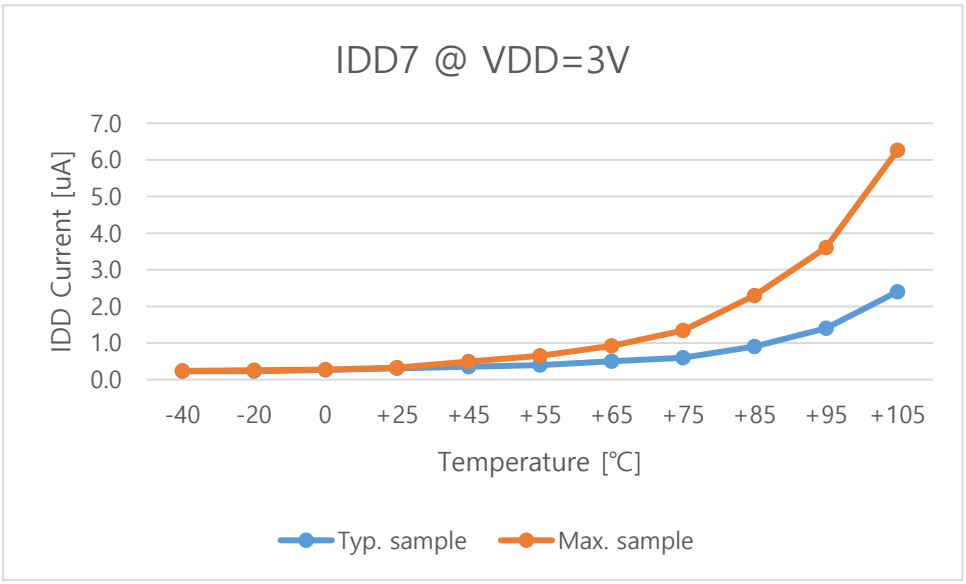


Figure 42. IDD7 (DEEP SLEEP mode 2) at VDD = 3V

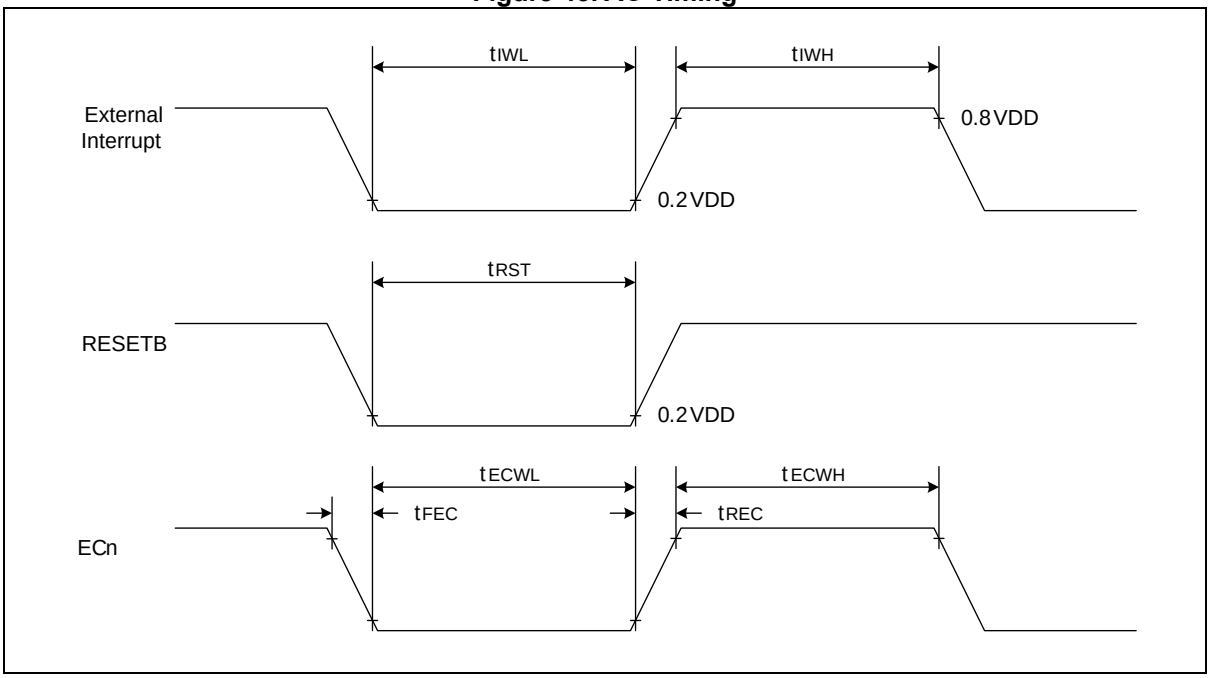


16.13 AC characteristics

Table 32. AC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RESETB input low width	t_{RST}	VDD = 3 V	20	–	–	µs
Interrupt input high, low width	t_{IWH}, t_{IWL}	All interrupts, VDD = 3 V	50	–	–	ns
External counter input high, low pulse width	t_{ECWH}, t_{ECWL}	VDD = 3 V All external counter input	1	–	–	$1/f_{PCLK}$
External counter transition time	t_{REC}, t_{FEC}	ECn, VDD = 3 V All external counter input	–	–	10	ns
I/O frequency	f_{IO1}	VDD = 3.0V, C_L = 30pF, All except f_{IO2}	–	–	10	MHz
	f_{IO2}	VDD = 2.7V, C_L = 30pF, SPI pins	–	–	16	

Figure 43. AC Timing

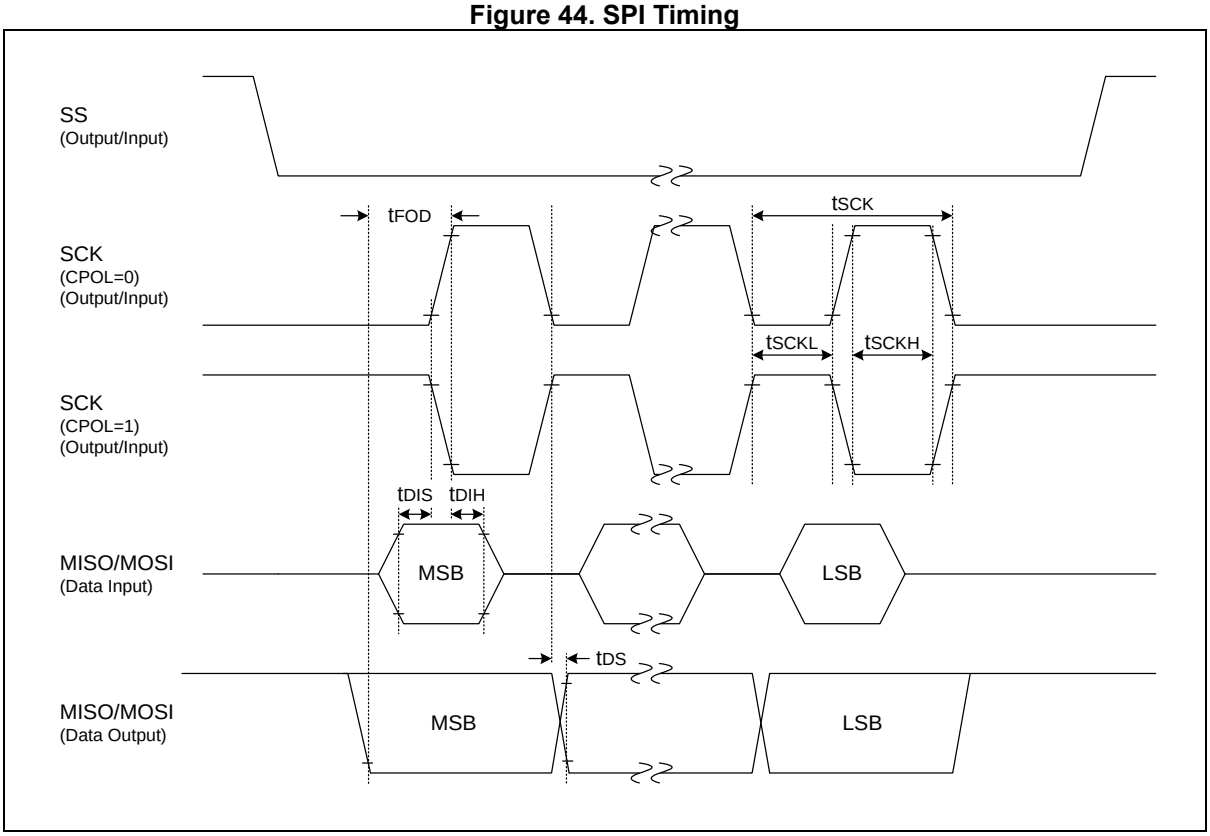


16.14 SPI characteristics

Table 33. SPI Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
SPI clock frequency	f_{SCK}	VDD ≥ 2.7V	Internal SCK source	–	–	16	MHz
			External SCK source				
	f_{SCK}	VDD ≥ 1.71V	Internal SCK source	–	–	12	
			External SCK source				
Input/output clock high, low pulse width	t_{SCKH}, t_{SCKL}	Internal/External SCK source		0.8*Typ	t_{SCK}/2	1.2*Typ	ns
First output clock delay time	t_{FOD}	Internal/External SCK source, CPHA = 0		0.4*t_{SCK}	–	–	
Output clock delay time	t_{DS}	–		–	–	18	
Input setup time	t_{DIS}			13	–	–	
Input hold time	t_{DIH}			15	–	–	

Figure 44. SPI Timing

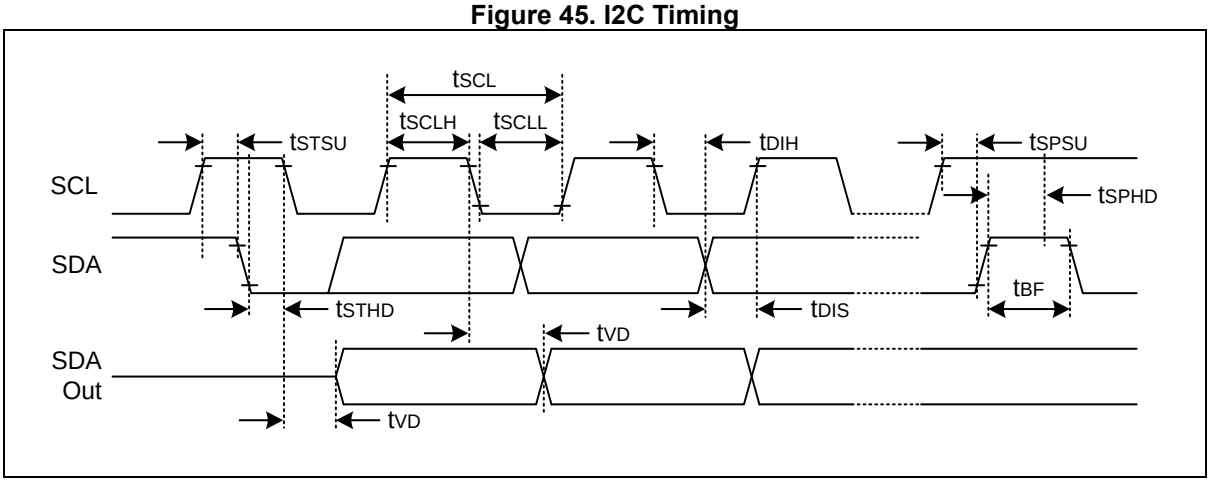


16.15 I2C characteristics

Table 34. I2C Characteristics

Parameter	Symbol	Standard		Fast		Fast Plus		Units
		Min	Max	Min	Max	Min	Max	
I2C operating voltage	–	VDD ≥ 1.71V		VDD ≥ 2V		VDD ≥ 2.7V		–
Clock frequency	t_{SCL}	0	100	0	400	0	1000	kHz
Clock high pulse width	t_{SCLH}	4.0	–	0.6	–	0.26	–	µs
Clock low pulse width	t_{SCLL}	4.7	–	1.3	–	0.5	–	
Bus free time	t_{BF}	4.7	–	1.3	–	0.5	–	
Start condition setup time	t_{STSU}	4.7	–	0.6	–	0.26	–	
Start condition hold time	t_{STHD}	4.0	–	0.6	–	0.26	–	
Stop condition setup time	t_{SPSU}	4.0	–	0.6	–	0.26	–	
Stop condition hold time	t_{SPHD}	4.0	–	0.6	–	0.26	–	
Output Valid from Clock	t_{VD}	0	–	0	–	0	–	
Data input hold time	t_{DIH}	0	–	0	1.0	0	0.45	
Data input setup time	t_{DIS}	250	–	100	–	50	–	ns

Figure 45. I2C Timing



16.16 UART timing characteristics

Table 35. UART Timing Characteristics (PCLK=32MHz)

Parameter	Symbol	Min	Typ	Max	Units
Serial port clock cycle time	t_{SCK}	–	–	2000	kHz
Output data setup to clock rising edge	t_{S1}	t_{SCK} x 12/16	–	–	ns
Clock rising edge to input data valid	t_{S2}	–	–	t_{SCK} x 13/16	
Output data hold after clock rising edge	t_{H1}	–	–	50	
Input data hold after clock rising edge	t_{H2}	0	–	–	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	t_{SCK} x 6/16	t_{SCK} x 8/16	t_{SCK} x 10/16	

Figure 46. UART Timing Characteristics

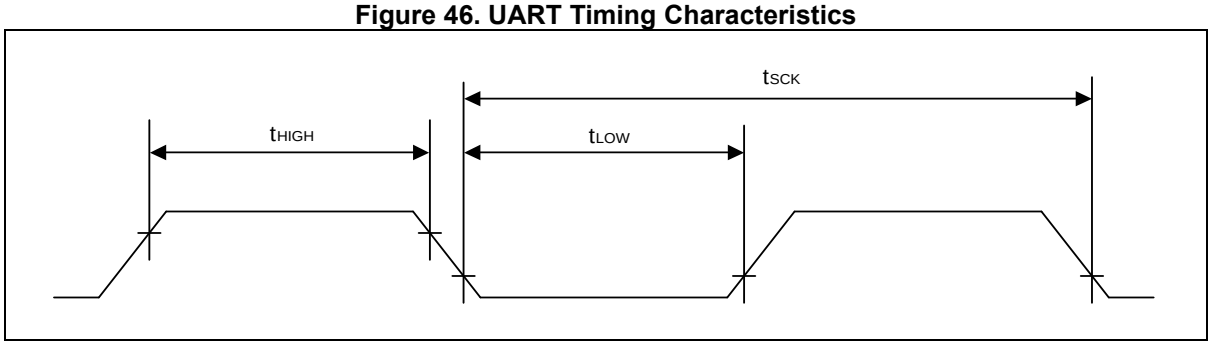
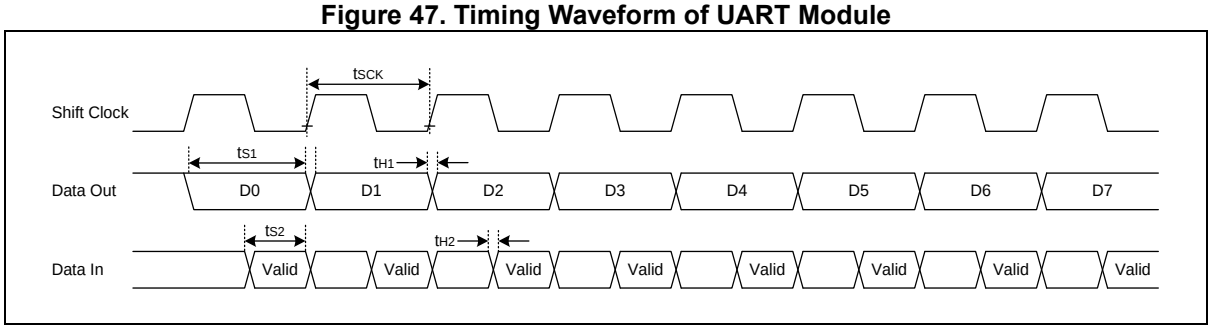


Figure 47. Timing Waveform of UART Module



16.17 Data retention voltage in DEEP SLEEP mode 0

Table 36. Data Retention Voltage in DEEP SLEEP mode 0

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data retention supply voltage	V_{DDDR}	–	1.71	–	3.6	V
Data retention supply current	I_{DDDR}	• V_{DDDR} = 1.71V (T_A=25°C) • DEEP SLEEP mode 0	–	–	1	µA

16.18 Internal Flash memory characteristics

Table 37. Internal Flash Memory Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Page write time	t_{FSW}	–		–	3.0	3.5	ms
Page erase time	t_{FSE}	–		–	3.0	3.5	
Chip erase time	t_{FCE}	–		–	3.0	3.5	
Program voltage	V_{PGM}	On erase/write		2.0	–	3.6	V
System clock frequency	f_{HCLK}	–		2.0	–	–	MHz
Flash Memory Endurance of Write/Erase	NF_{FWE}	• Page 0 to 255 • Configure Option Page 1	T_A=25 °C, Page unit	10,000	–	–	Cycles
		Configure Option Page 2/3		100,000			
Retention time	t_{FRT}			10	–	–	Years

16.19 Input/output capacitance

Table 38. Input/Output Capacitance

(VDD = 0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input capacitance	C_{IN}	• f=1MHz • Unmeasured pins are connected VSS	–	–	10	pF
Output capacitance	C_{OUT}					
I/O capacitance	C_{IO}					

16.20 Main oscillator characteristics

Table 39. Main Oscillator Characteristics

(VDD = 1.8V to 3.6V)

Oscillator	Parameter	Conditions	Min	Typ	Max	Units
Crystal	Main oscillation frequency	2.7 V to 3.6 V	2.0	–	16.0	MHz
Ceramic Oscillator	Main oscillation frequency	1.8 V to 3.6 V	2.0	–	4.2	
		2.7 V to 3.6 V	2.0	–	16.0	
External Clock	XIN input frequency	3.0 V to 3.6 V	2.0	–	32.0	MHz
	External Clock Duty Ratio	–	45	50	55	%

Figure 48. Crystal/Ceramic Oscillator

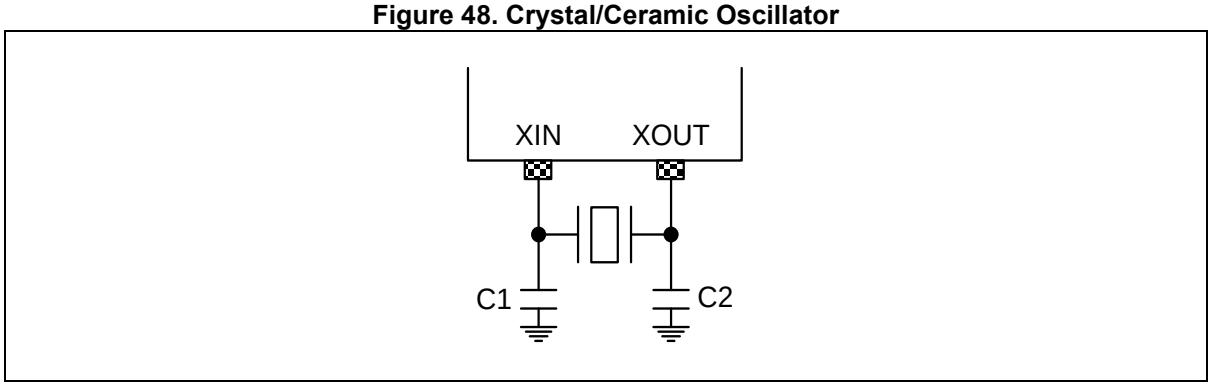
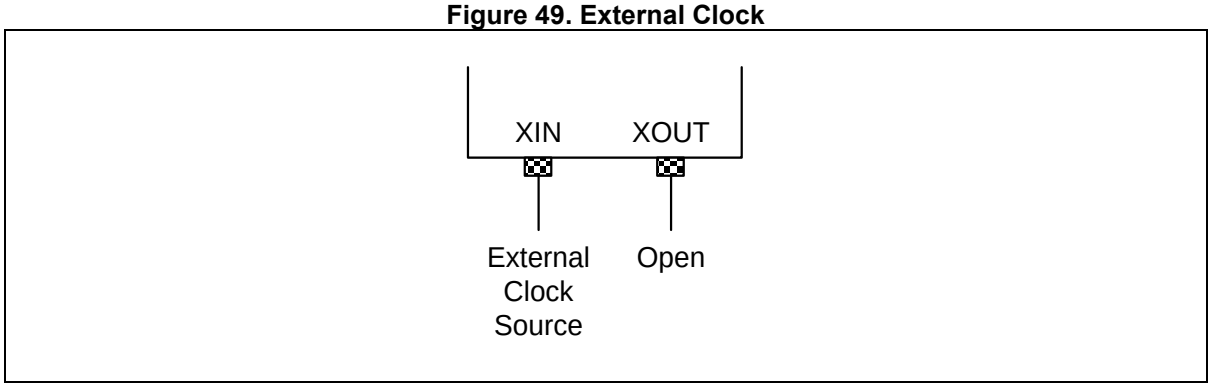


Figure 49. External Clock

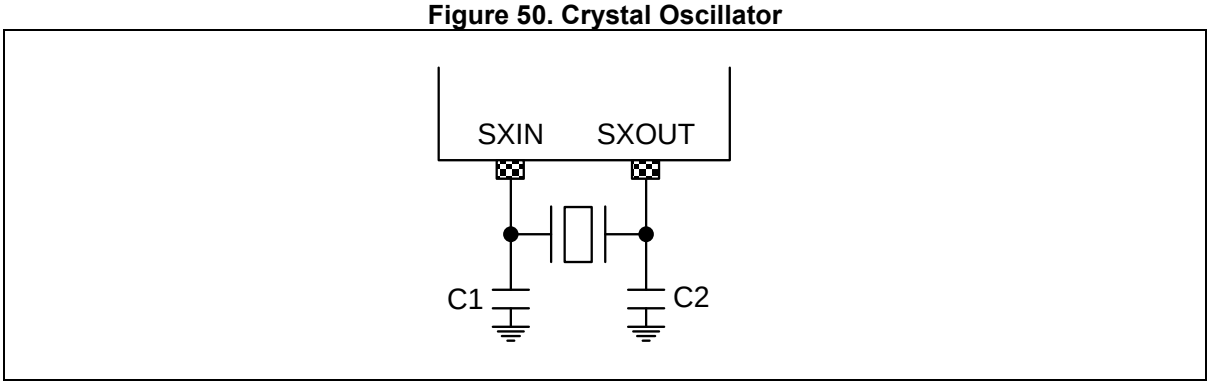


16.21 Sub-oscillator characteristics

Table 40. Sub-oscillator Characteristics

Oscillator	Parameter	Conditions	Min	Typ	Max	Units
Crystal	Sub oscillation frequency	1.71 V to 3.6 V	32	32.768	38	kHz

Figure 50. Crystal Oscillator



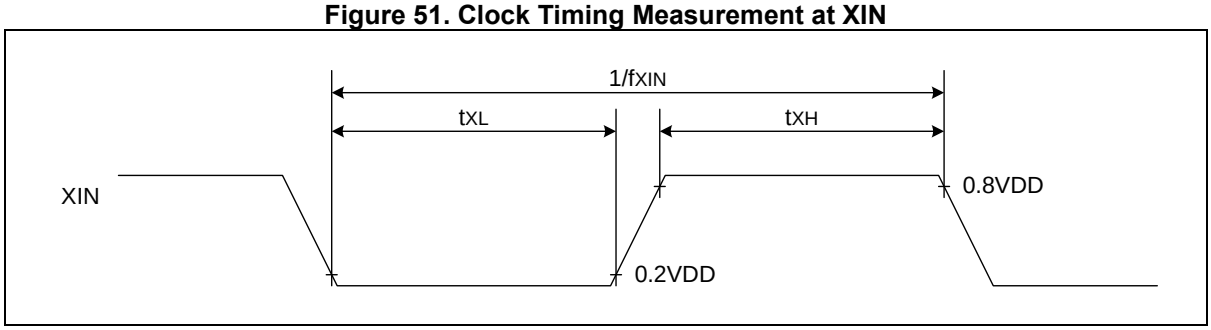
16.22 Main oscillation stabilization time

Table 41. Main Oscillation Stabilization Time

(VDD = 1.8V to 3.6V)

Oscillator	Conditions		Min	Typ	Max	Unit
Crystal	• f_{XIN} ≥ 2MHz • Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	VDD = 2.7V to 3.6V	–	–	60	ms
Ceramic		VDD = 1.8V to 3.6V	–	–	10	
External clock	• f_{XIN} = 2.0 to 32MHz • XIN input high and low width (t_{XL}, t_{XH})		15.6	–	250	ns

Figure 51. Clock Timing Measurement at XIN



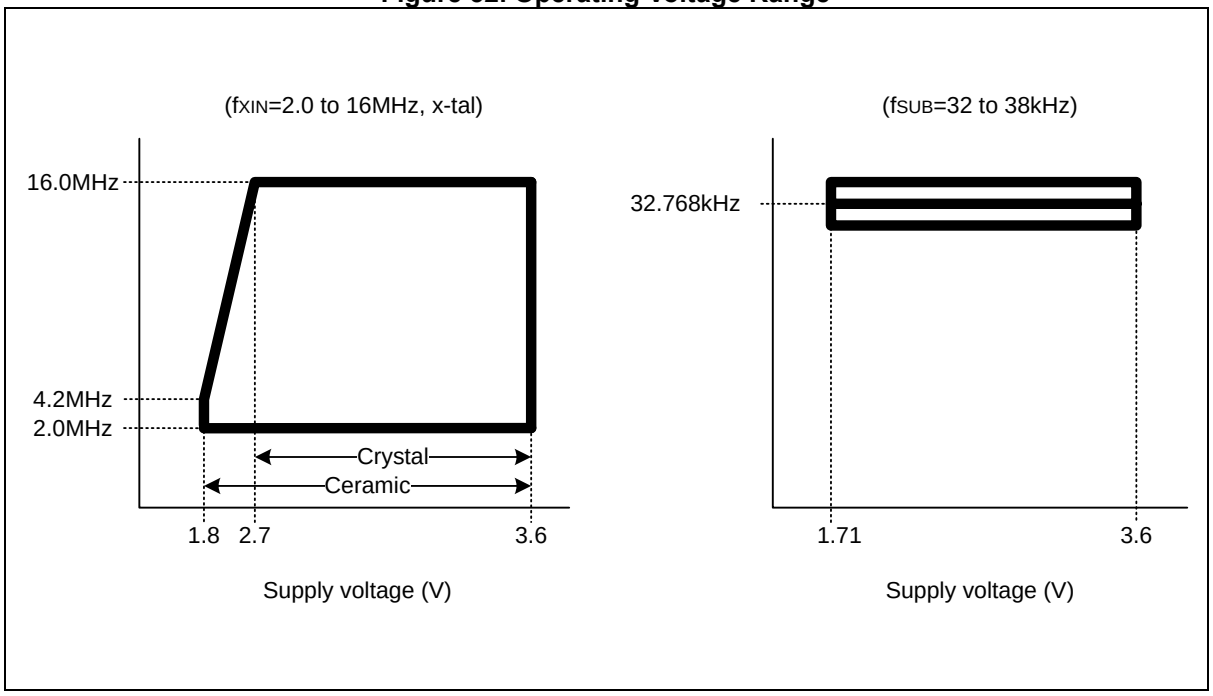
16.23 Sub-oscillation stabilization time

Table 42. Sub-oscillation Stabilization Time

Oscillator	Conditions	Min	Typ	Max	Units
Crystal	–	–	–	10	sec
	VDD=3V, T_A=25 °C, ISET_I[2:0] = 0x7	–	0.7	1.5	

16.24 Operating voltage range

Figure 52. Operating Voltage Range



16.25 Recommended circuit and layout

Figure 53. Recommended Circuit and Layout

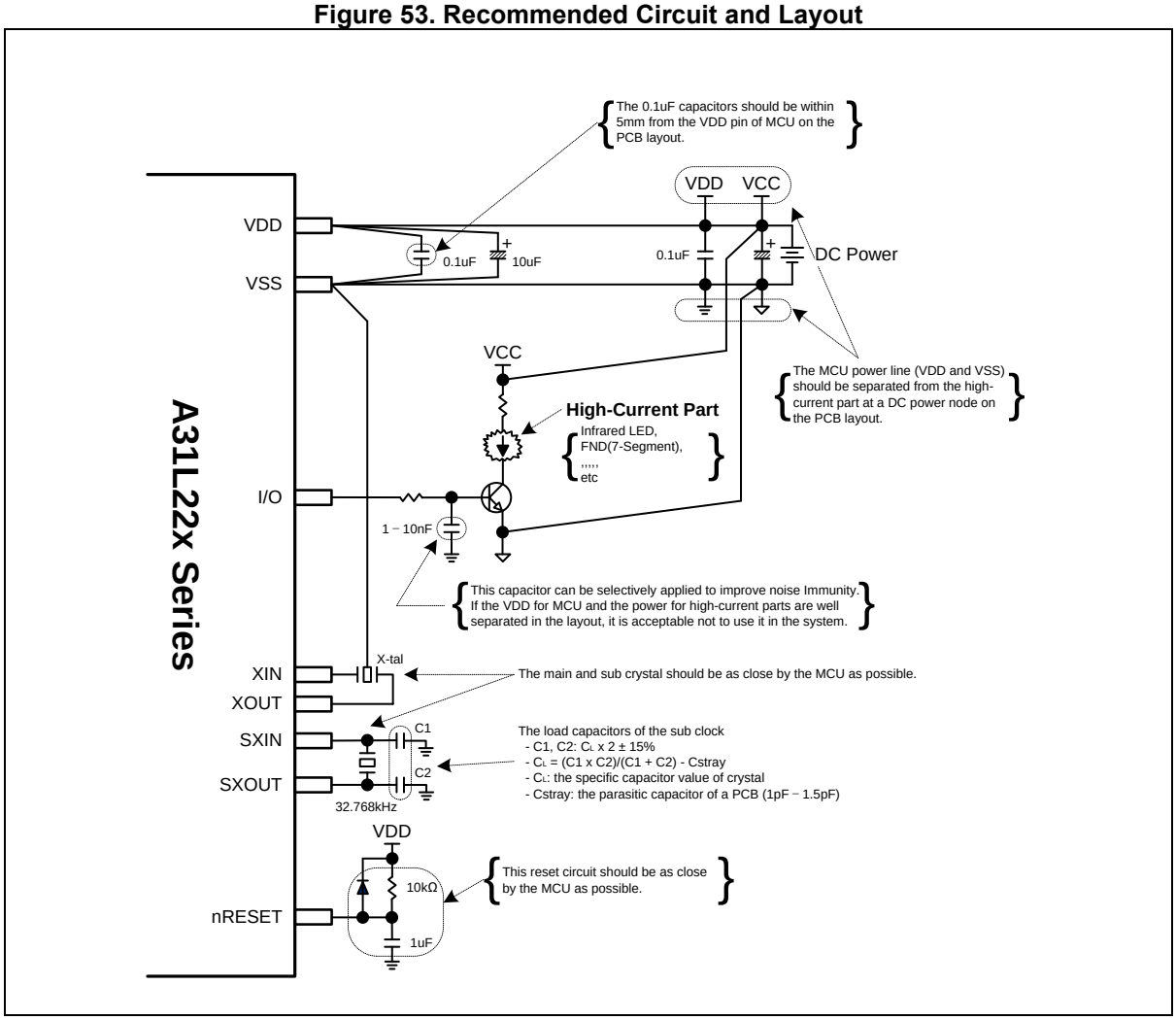
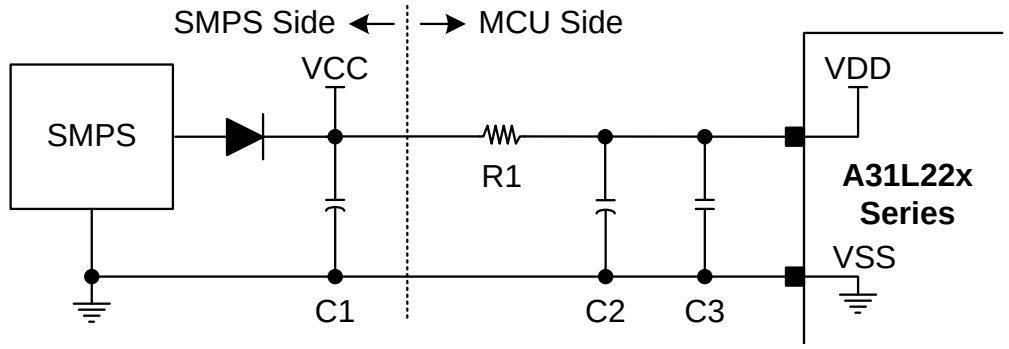


Figure 54. Recommended Circuit and Layout with SMPS Power



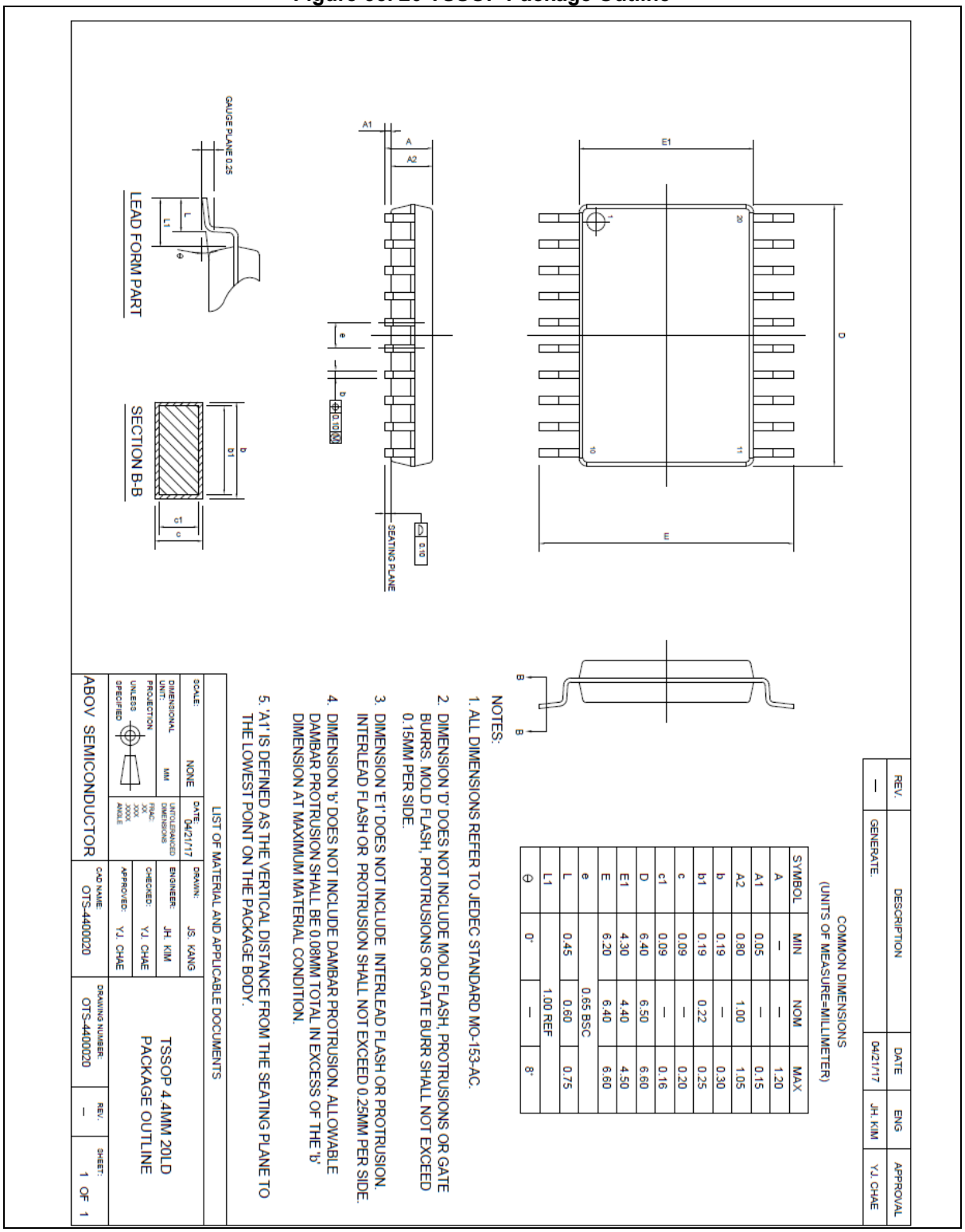
NOTES:

1. Capacitor C1 is to flatten out the voltage of the SMPS power, VCC.
   - Recommended C1: 470uF/25V more
2. Resistor R1 and capacitor C2 are the RC filter for VDD and suppress the ripple of VCC.
   - Recommended R1: 10Ω - 20Ω
   - Recommended C2: 47uF/25V more
   - The R1 and C2 should be as close by the C3 as possible.
3. Capacitor C3 is used for temperature compensation because an electrolytic capacitor becomes worse characteristics at low temperature.
   - Recommended C3: ceramic capacitor 2.2uF more.
   - C3 should be within 1cm from VDD pin of MCU on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc.) when the SMPS supplies the VDD of MCU.

17 Package information

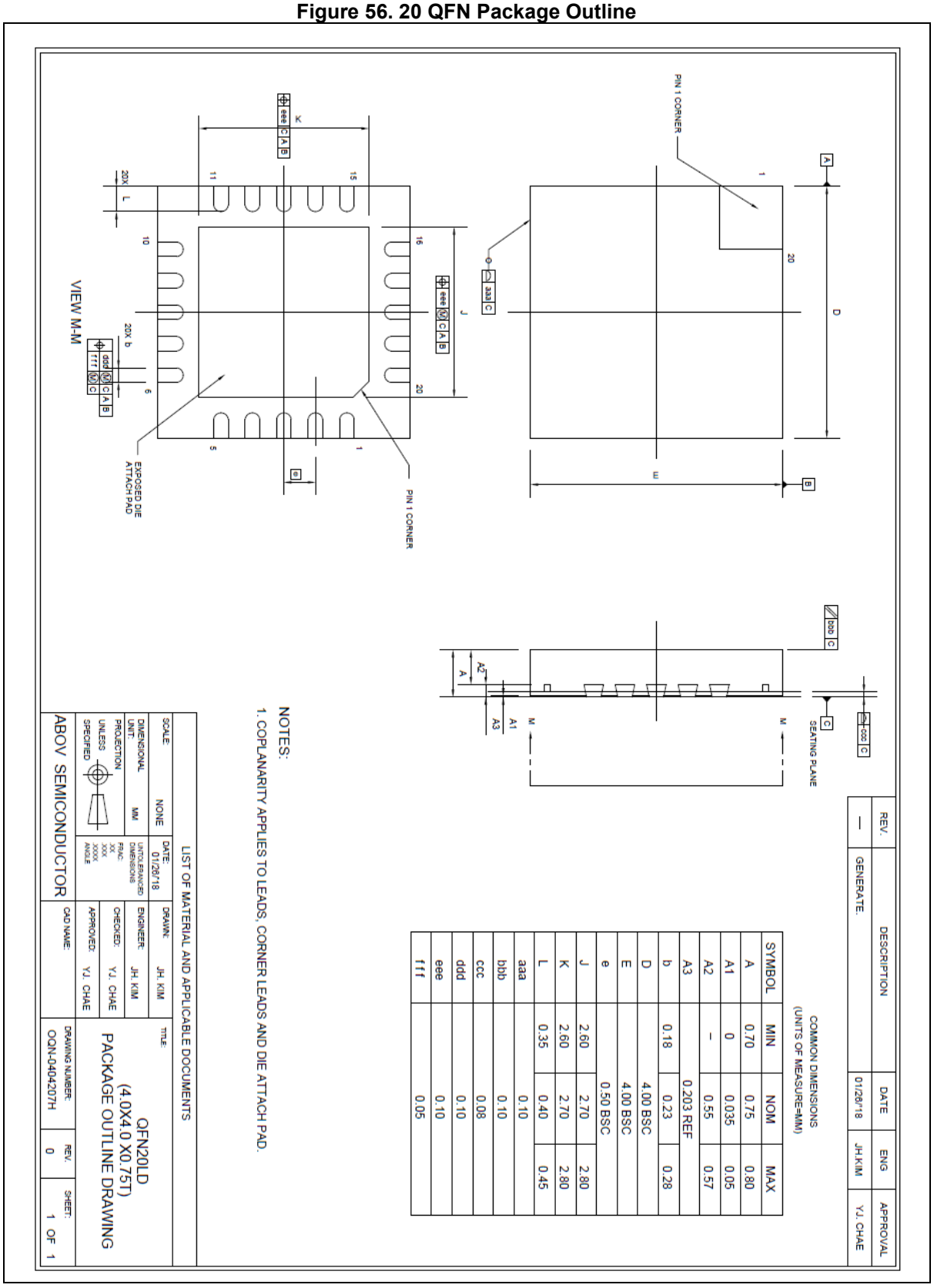
17.1 20 TSSOP package information

Figure 55. 20 TSSOP Package Outline



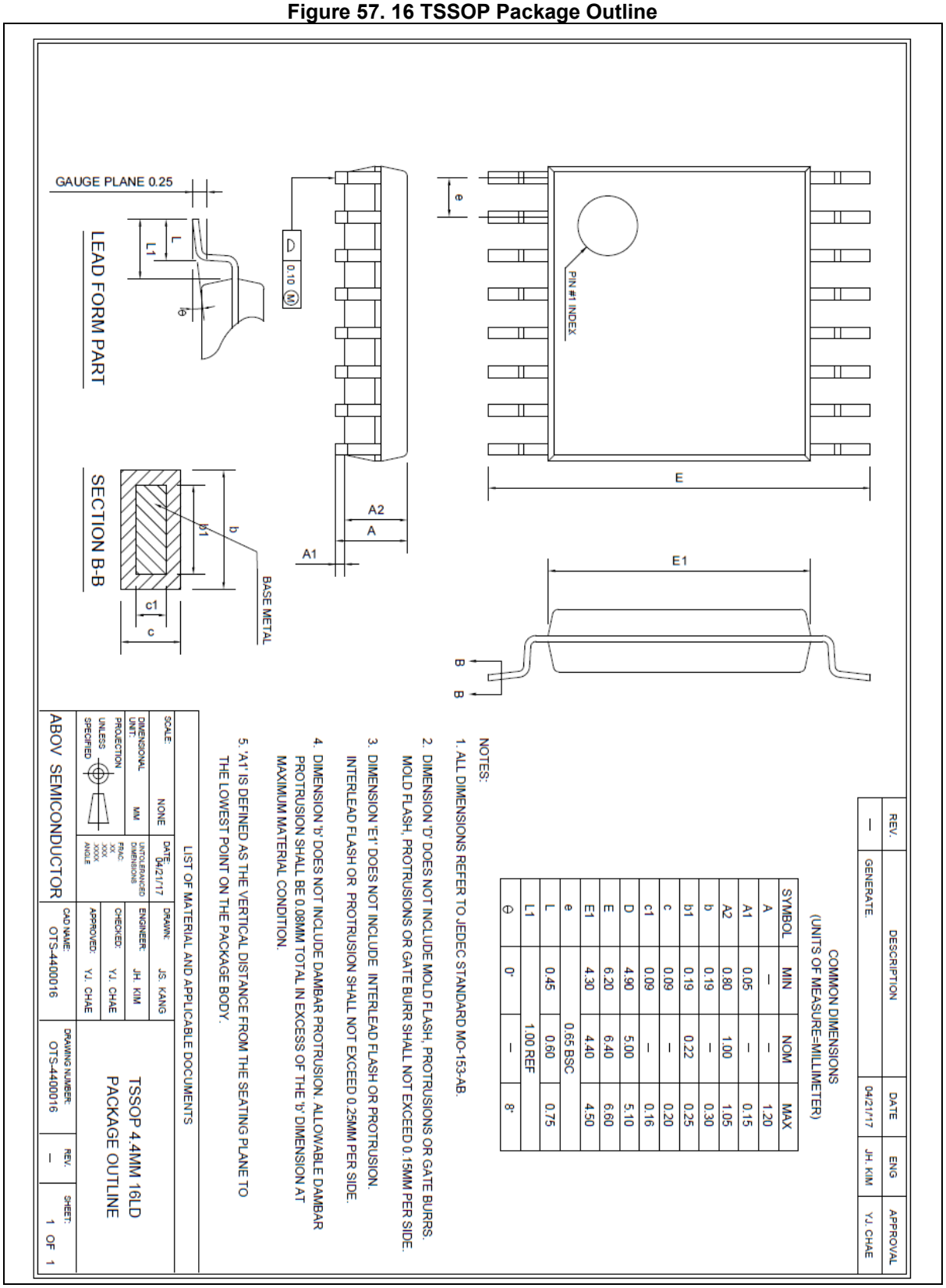
17.2 20 QFN package information

Figure 56. 20 QFN Package Outline



17.3 16 TSSOP package information

Figure 57. 16 TSSOP Package Outline



18 Ordering information

Table 43. A31L22x Series Ordering Information

Part Number	Flash	SRAM	USART	UART	LPUART	I2C	SPI	TIMER	ADC	I/O	Package
A31L222FR	32KB	4KB	1	1	1	1	1	5	8ch	17	20TSSOP
A31L222FU*	32KB	4KB	1	1	1	1	1	5	8ch	17	20QFN
A31L222AR*	32KB	4KB	1	1	1	1	1	4	6ch	13	16TSSOP
A31L221FR*	16KB	4KB	1	1	1	1	1	5	8ch	17	20TSSOP
A31L221FU*	16KB	4KB	1	1	1	1	1	5	8ch	17	20QFN
A31L221AR*	16KB	4KB	1	1	1	1	1	4	6ch	13	16TSSOP

* For available options or further information on the devices with "*" marks, please contact the ABOV sales offices.

Figure 58. A31L22x Series Numbering Nomenclature

A31L22 2 F R 2 N (T)

A31L22 Family Name

Code memory size

2 32Kbytes
1 16Kbytes

Pin count

F 20 pins
A 16 pins

Package type

R TSSOP
U QFN1

Temperature

None -40 to +85℃ (commercial grade)
2 -40 to +105℃ (industrial grade)

Bonding wire

none Au wire
N Pd-Cu wire

Packing

(T) Tape & reel
(W) Wafer
(C) Chip carrier

NOTE: For more information on any aspect of this device, please contact your nearest distributor or the ABOV sales office.

Revision history

Revision	Date	Notes
1.00	Feb. 27, 2023	1st creation

Korea

Regional Office, Seoul
R&D, Marketing & Sales
8th Fl., 330, Yeongdong-daero,
Gangnam-gu, Seoul,
06177, Korea

Tel: +82-2-2193-2200
Fax: +82-2-508-6903
www.abovsemi.com

HQ, Ochang
R&D, QA, and Test Center
93, Gangni 1-gil, Ochang-eup,
Cheongwon-gun,
Chungcheongbuk-do,
28126, Korea

Tel: +82-43-219-5200
Fax: +82-43-217-3534
www.abovsemi.com

Domestic Sales Manager
Tel: +82-2-2193-2206
Fax: +82-2-508-6903
Email: sales_kr@abov.co.kr

Global Sales Manager
Tel: +82-2-2193-2281
Fax: +82-2-508-6903
Email: sales_gl@abov.co.kr

China Sales Manager
Tel: +86-755-8287-2205
Fax: +86-755-8287-2204
Email: sales_cn@abov.co.kr