CMOS single-chip 8-bit MCU with EEPROM and 12-bit A/D converter

Main features

- **8-bit Microcontroller with high speed 8051 CPU**
- **Basic MCU Function**
  - 8Kbytes Flash Code Memory
  - 512bytes EEPROM Backup Memory
  - 512bytes SRAM Data Memory
- **Built-in Analog Function**
  - Power-On Reset and Brown Out Detect Reset
  - Internal 8MHz RC Oscillator (±3%, T_A = -40 ~ +85°C)
  - Internal 1MHz RING Oscillator
- **Peripheral features**
  - 12-bit Analog to Digital Converter (15inputs)
  - Serial Interface (USART + SPI + I2C)
  - 6-channel 10-bit PWM for Motor Control
- **I/O and packages**
  - Up to 30 programmable I/O lines with 32SOP
  - 32/28/20/16 SOP
- **Operating conditions**
  - 1.8V to 5.5V wide voltage range
  - -40°C to 85°C temperature range
- **Application**
  - Small Home Appliance
  - BLDC Motor Controller
  - LED Lighting with High speed PWM
  - (7-bit duty 500kHz period ~ 10-bit duty 62.5kHz period)

MC95FG308
MC95FG208

Data Sheet

V 3.4

Revised 12 May, 2015

Revision history

Version	Date	Revision list
0.0	2010.01.15	Initial version
0.1	2010.02.25	Update 15.7 Security and 16.1 Configuration
0.2	2010.03.29	Update Figure 1.3 gang 4→gang 8
1.0	2010.06.18	Release version
1.1	2010.07.02	Update endurance spec
1.2	2010.10.30	Update 11.1.5 register description for clock generator
1.3	2010.11.23	TxDR register increment range modification
1.4	2010.11.30	ADCM2 and Figure 11-67 modification
1.5	2011.01.22	Electrical Characteristics description modification
1.6	2011.02.10	Correct Interrupt, Port selection register
1.7	2011.03.03	Correct A/D Converter Characteristics and OCD emulator description
1.8	2011.03.10	Add package diagram(28TSSOP)
1.9	2011.03.21	Add Internal RC Oscillator Range, Figure1.1 8MHz Internal OSC Freq. (SOC_HOT: 85℃)
2.0	2011.03.24	Correct register T1ISR
2.1	2011.05.05	Add PWM description
2.2	2011.06.10	Correct Analog Comparator Block Diagram
2.3	2011.06.28	Add Port RESET N/C
2.4	2011.08.17	Add DC Characteristics
2.5	2011.11.24	Add Appendix B (Instructions on how to use the input port)
2.6	2011.11.28	Correct 28SOP package diagram
2.7	2011.12.21	Correct TMISR, ACCSR address
2.8	2012.01.31	Correct 32QFN Package Diagram
2.9	2012.05.21	Correct Ordering Information
3.0	2012.10.04	Add Main and sub clock oscillator characteristics
3.1	2012.12.14	Correct Figure 3.2, Figure 3.3
3.2	2013.06.05	Renewal version
3.3	2015.04.30	Change Configure Option naming. Bit test & branch instruction caution
3.4	2015.05.12	Added 28TSSOP package MC95FG308H

Version 3.4

Published by FAE team

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1 Overview

1.1. Description

The MC95FG308 is an advanced CMOS 8-bit microcontroller with 8Kbytes of FLASH. This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This provides the following features: 8Kbytes of FLASH, 256bytes of internal SRAM, 256bytes of external SRAM, 512bytes of Data EEPROM, general purpose I/O, 8/16-bit timer/counter, watchdog timer, watch timer, SPI, USART, I2C, on-chip POR, BOD, 12-bit A/D converter, analog comparator, buzzer driving port, 10-bit high speed PWM output, on-chip oscillator and clock circuitry. The MC95FG308 also supports power saving modes to reduce power consumption.

Device Name	FLASH	IRAM	XRAM	EEPROM	ADC	I/O PORT	Package
MC95FG308D	8Kbytes	256bytes	256bytes	512bytes	15inputs	30	32SOP
MC95FG308U							32QFN
MC95FG308L							32LQFP
MC95FG308M					12inputs	26	28SOP
MC95FG308H							28TSSOP
MC95FG208D					10inputs	18	20SOP
MC95FG208R							20TSSOP
MC95FG208M					8inputs	14	16SOP
MC95FG208H							16TSSOP

Table 1.1 Ordering Information of MC95FG308

1.2 Features

- **CPU**
  - 8-bit CISC core (8051 Compatible, 2 clock per cycle)
- **8Kbytes On-Chip FLASH**
  - Optional boot code section with protection
  - Endurance : 10,000 times at room temperature
  - Retention : 10 years
- **256bytes SRAM**
- **256bytes XRAM**
- **512bytes Data EEPROM**
  - Endurance : 300,000 times at room temperature
  - Retention : 10 years
- **General Purpose I/O (GPIO)**
  - 30Ports (P0[7:0], P1[6:0], P2[6:0], P3[7:0]): 32-Pin
  - 26Ports (P0[7:0], P1[6:0], P2[2:0], P3[7:0]): 28-Pin
  - 18Ports (P0[7:0], P1[6:0], P2[2:0]): 20-Pin
  - 14Ports (P0[7:0], P1[2:0], P2[2:0]): 16-Pin
- **One Basic Interval Timer**
- **Timer/Counter**
  - 8-bit × 4-ch (16-bit × 2-ch) + 16-bit × 1-ch
- **3 High Frequency 10-bit PWM (Using Timer1)**
- **10-bit PWM (Using Timer3)**
- **Watch Dog Timer**
- **Watch Timer**
- **SPI**
- **USART (2-ch)**
- **I2C**
- **Buzzer Driving Port**
- **12-bit A/D Converter**
  - 15-Input channels : 32-Pin
- **Analog Comparator**
  - On Chip Analog Comparator
- **Interrupt Sources**
  - External Interrupts (8)
  - Pin Change Interrupt(P0) (1)
  - USART0,1 (4)
  - SPI (1)
  - Timer (5)
  - I2C (1)
  - Data EEPROM (1)
  - ADC (1)
  - Analog Comparator (1)
  - WDT (1)
  - WT (1)
  - BIT (1)
- **On-Chip RC-Oscillator**
  - 8MHz(±3%)
- **Power On Reset**
- **Programmable Brown-Out Detector**
- **Minimum Instruction Execution Time**
  - 200ns (@10MHz, NOP Instruction)
- **Power Down Mode**
  - IDLE, STOP1, STOP2 mode
- **Sub-Active mode**
  - System used external 32.768kHz crystal or system used internal 125kHz Ring oscillator
- **Operating Frequency**
  - 1MHz ~ 12MHz
- **Operating Voltage**
  - 1.8V ~ 5.5V
- **Operating Temperature : –40 ~ +85℃**
- **Package Type**
  - 32SOP/QFN/LQFP
  - 28SOP
  - 20SOP/TSSOP
  - 16SOP/TSSOP
  - Pb free package

1.3 Development tools

1.3.1 Compiler

ABOV Semiconductor does not provide compiler. It is recommended that you consult a compiler provider.
The MC95FG308 core is Mentor 8051, and the ROM size is smaller than 64Kbytes.Therefore, developer can use the standard 8051 compiler from other providers.

1.3.2 OCD(On-chip debugger) emulator and debugger

The OCD (On Chip Debug) emulator supports ABOV Semiconductor's 8051 series MCU emulation.The OCD interface uses two-wire connection between PC and MCU which is attached to user's system. The OCD can read or change the value of MCU internal memory and I/O peripherals. And the OCD also controls MCU internal debugging logic, it means OCD controls emulation, step run, monitoring, etc.
The OCD debugger program works on Microsoft-Windows NT, 2000, XP, Vista (32-bit) operating system.If you want to see more details, please refer to OCD debugger manual. You can download debugger S/W and manual from our web-site (http://www.abov.co.kr).

Connection:

- DSCL (MC95FG308 P06 port)
- DSDA (MC95FG308 P07 port)

OCD connector diagram: Connect OCD with user system

Figure 1.1 debugger and pin description

OCD emulator:
It can write code to MCU device too, because OCD debugger supports ISP (In System Programming). It does not require additional H/W, except developer's target system.

1.3.3 Programmer

Single programmer:

PGMplus USB: It programs MCU device directly.

Figure 1.2 PGMplusUSB(Single writer)

Standalone PGMplus:

It programs MCU device directly.

Figure 1.3 Standalone PGMplus(Single writer)

Gang programmer:

It programs 8 MCU devices at once.So, it is mainly used in mass production factory.

Gang programmer is standalone type, it means it does not require host PC, after a program is downloaded from host PC to Gang programmer.

Figure 1.4 StandAlone Gang8 (for Mass Production)

On-Board programming :

The program memory of MC95FG308 is FLASH Memory Type. This flash is accessed by serial data format. There are four pins (DSCL, DSDA, VDD, and VSS) for programming/reading the flash. The MC95FG308 needs only four signal lines including VDD and VSS pins for programming FLASH with serial protocol. Therefore the on-board programming is possible if the programming signal lines are considered when the PCB of application board is designed.

Pin name	Main chip pin name	During programming	
		I/O	Description
DSCL	P06	I	Serial clock pin. Input only pin.
DSDA	P07	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	-	Logic power supply pin.

Table 1.2 Descriptions of pins used to programming/reading the Flash

2 Block diagram

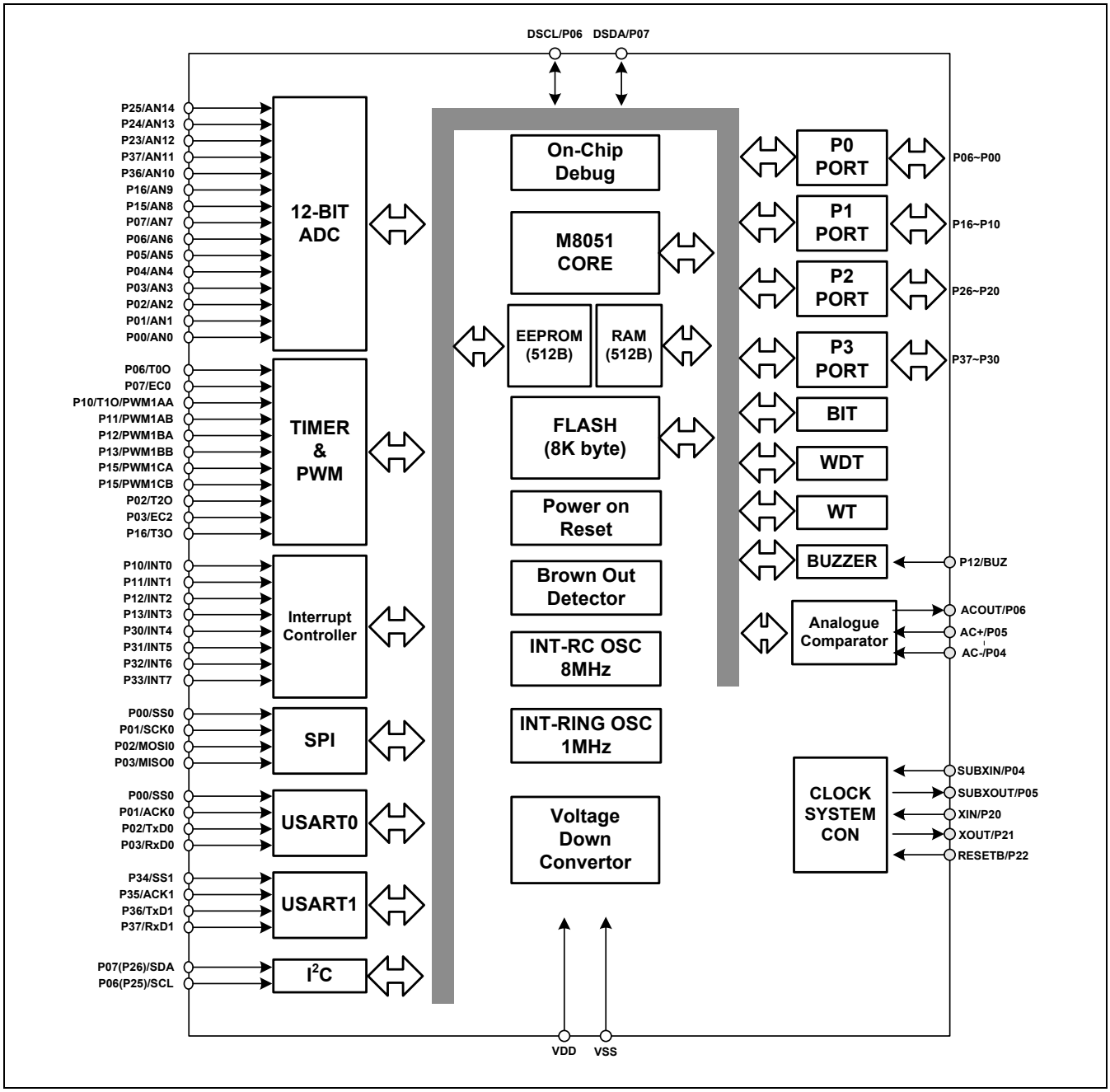
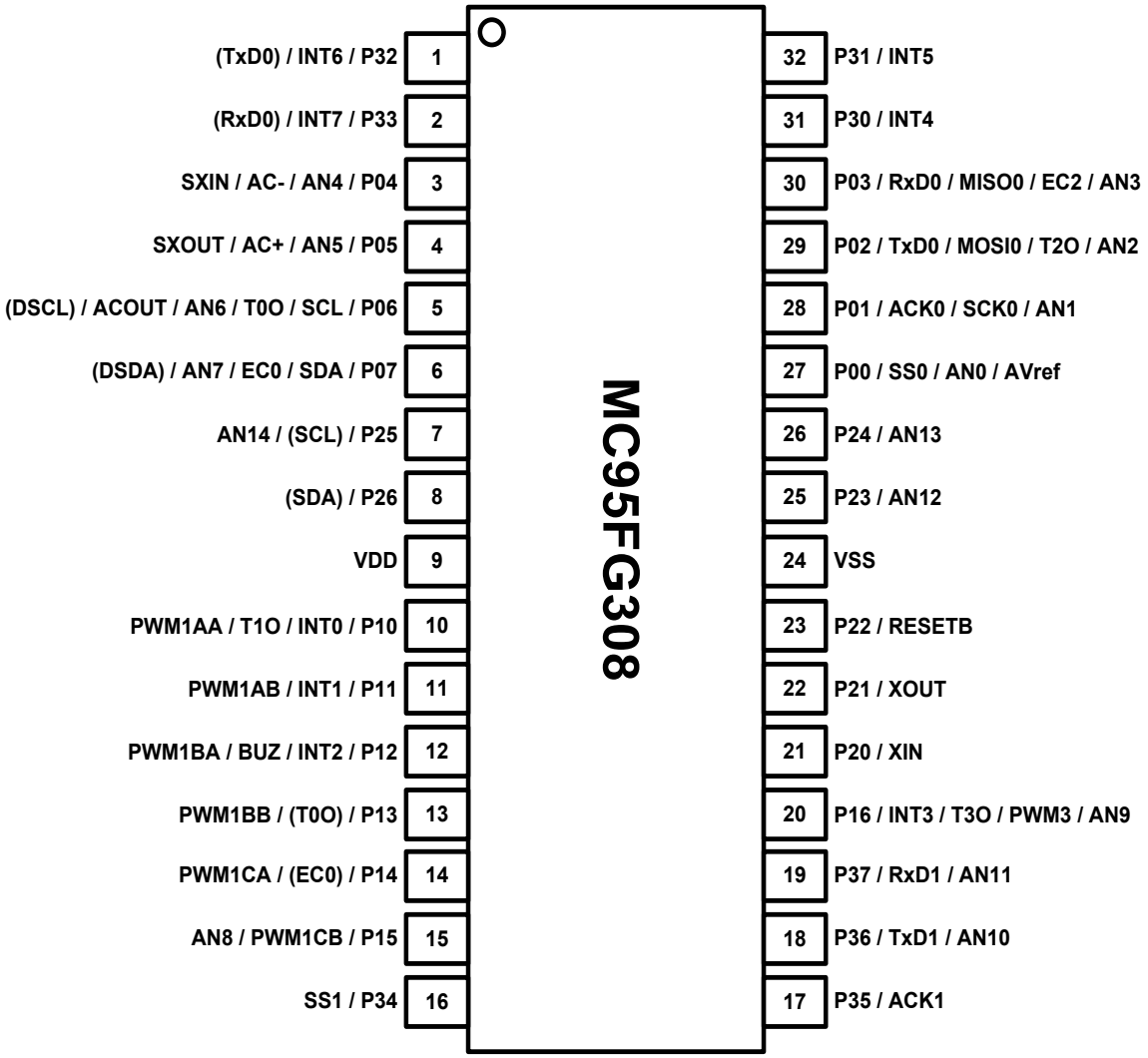


Figure 2.1 Block diagram of MC95FG308

3 Pin assignment



NOTE)

1. If 28PKG, Pin 7, 8, 25 and 26 in 32-pin package are removed and their function can't operate.
2. If 20PKG, Pin 1, 2, 31, 32, 15, 16, 17, 18, 7, 8, 25 and 26 in 32-pin package are removed and their function can't operate.
3. If 16PKG, Pin 13, 14, 19, 20, 1, 2, 31, 32, 15, 16, 17, 18, 7, 8, 25 and 26 in 32-pin package are removed and their function can't operate.
4. On On-Chip Debugging, ISP uses P0[7:6] pin as DSCL, DSDA.
5. The outside pin operation has higher priority than the inside pin operation. Ex) In pin32, if P03, RxD0, MISO0, EC2 and AN3 are set, AN3 will be operated.

Figure 3.1 MC95FG308 32SOP pin assignment

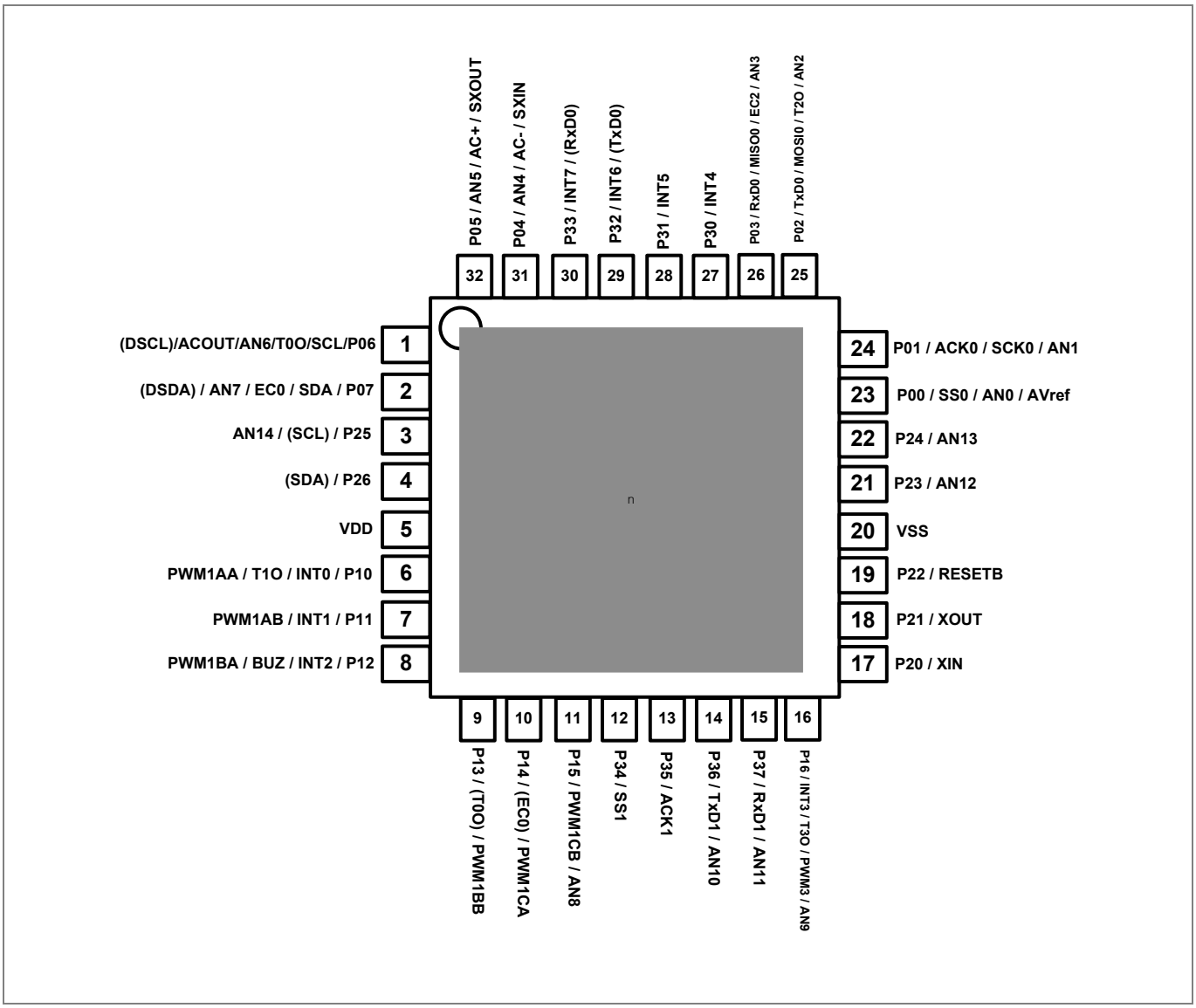


Figure 3.2 MC95FG308 32QFN pin assignment

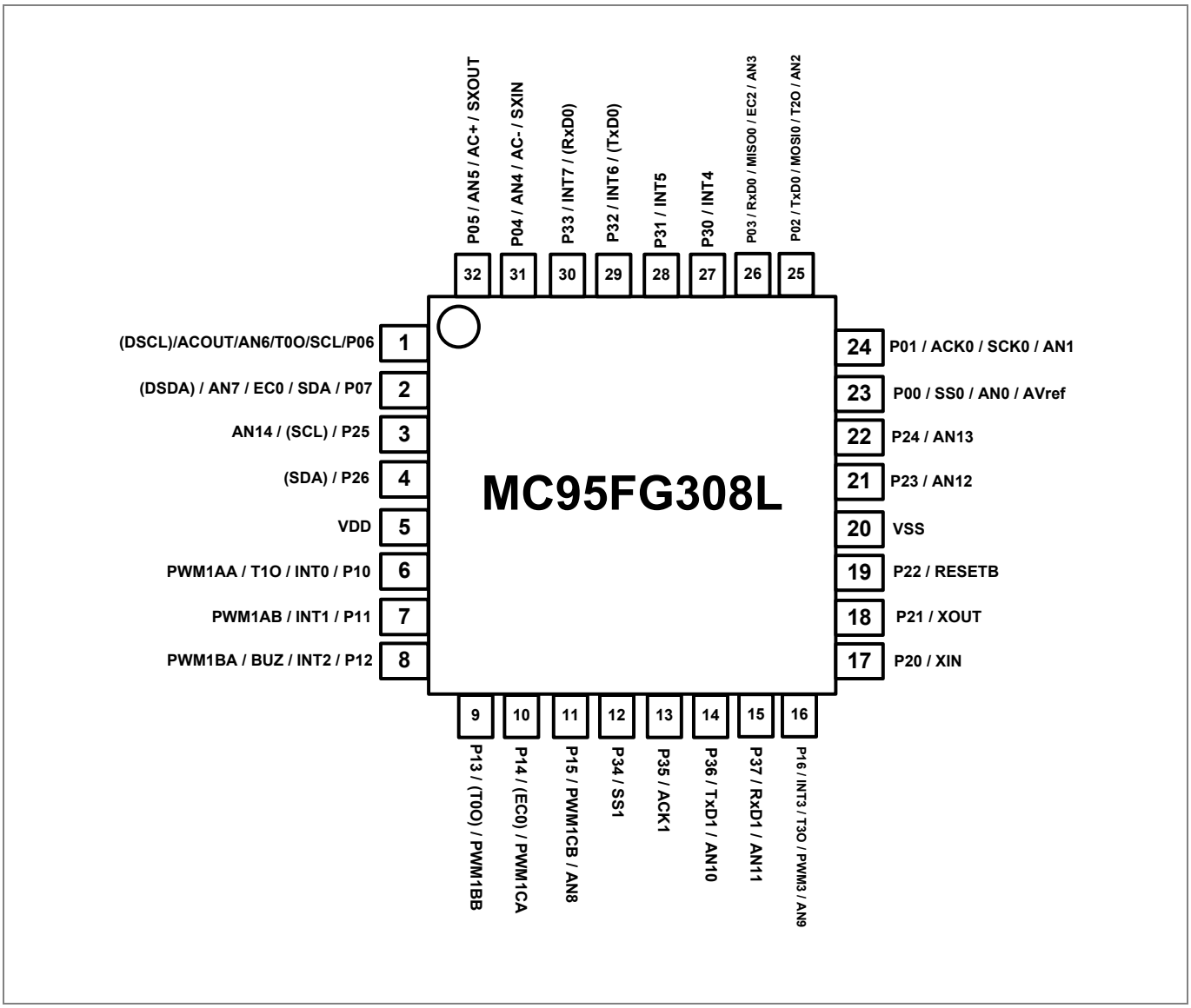


Figure 3.3 MC95FG308 32LQFP pin assignment

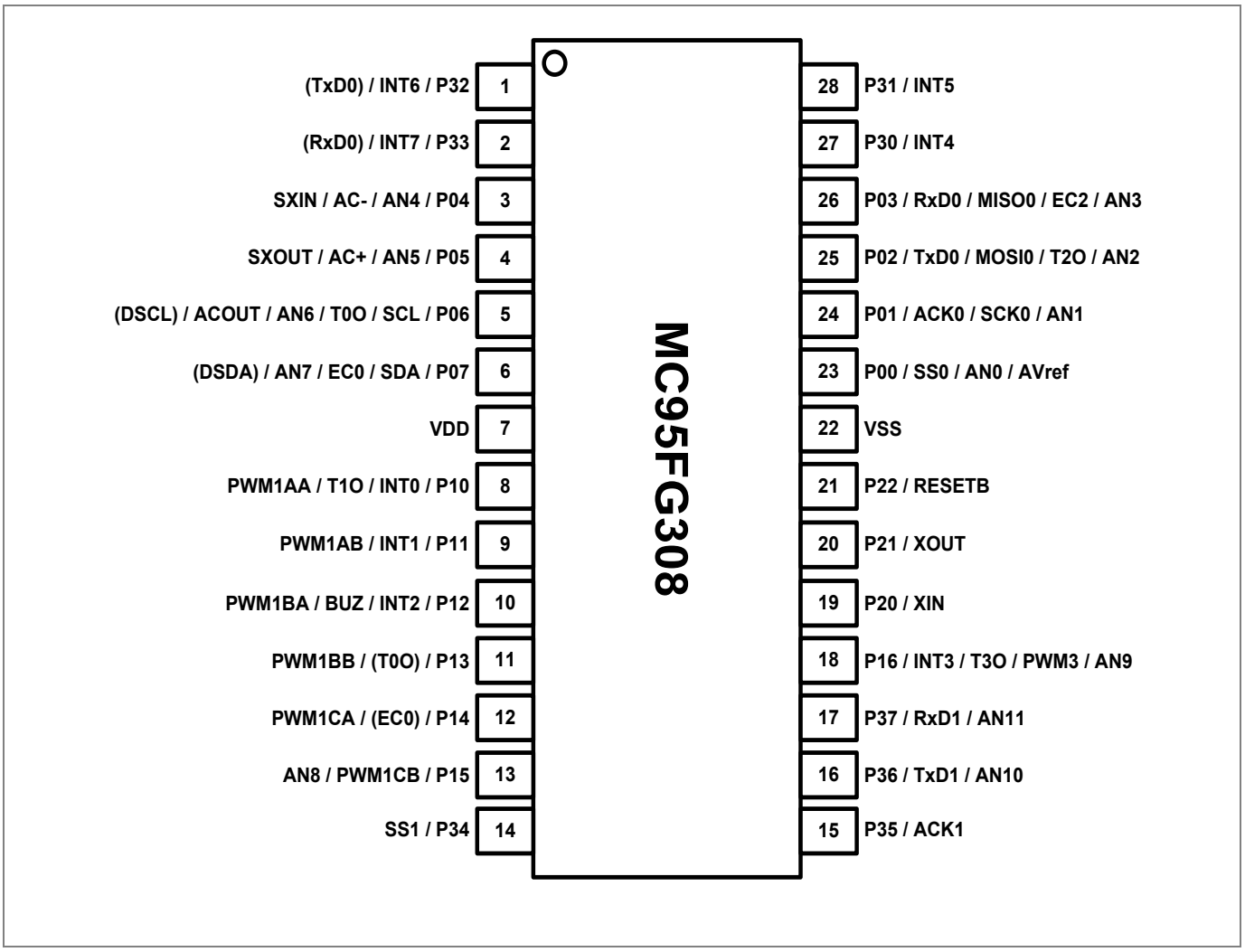


Figure 3.4 MC95FG308 28SOP/TSSOP pin assignmemt

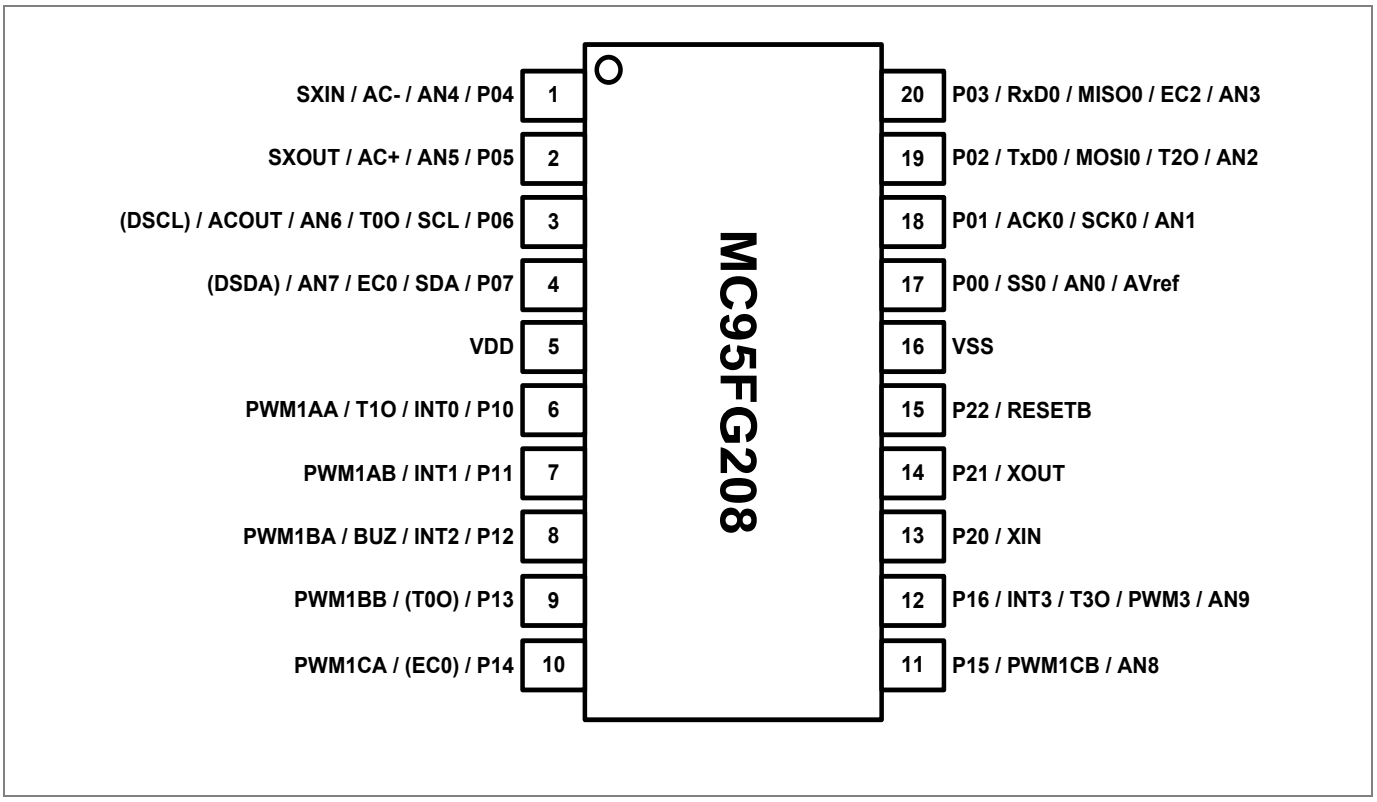


Figure 3.5 MC95FG208 20SOP/TSSOP pin assignmemt

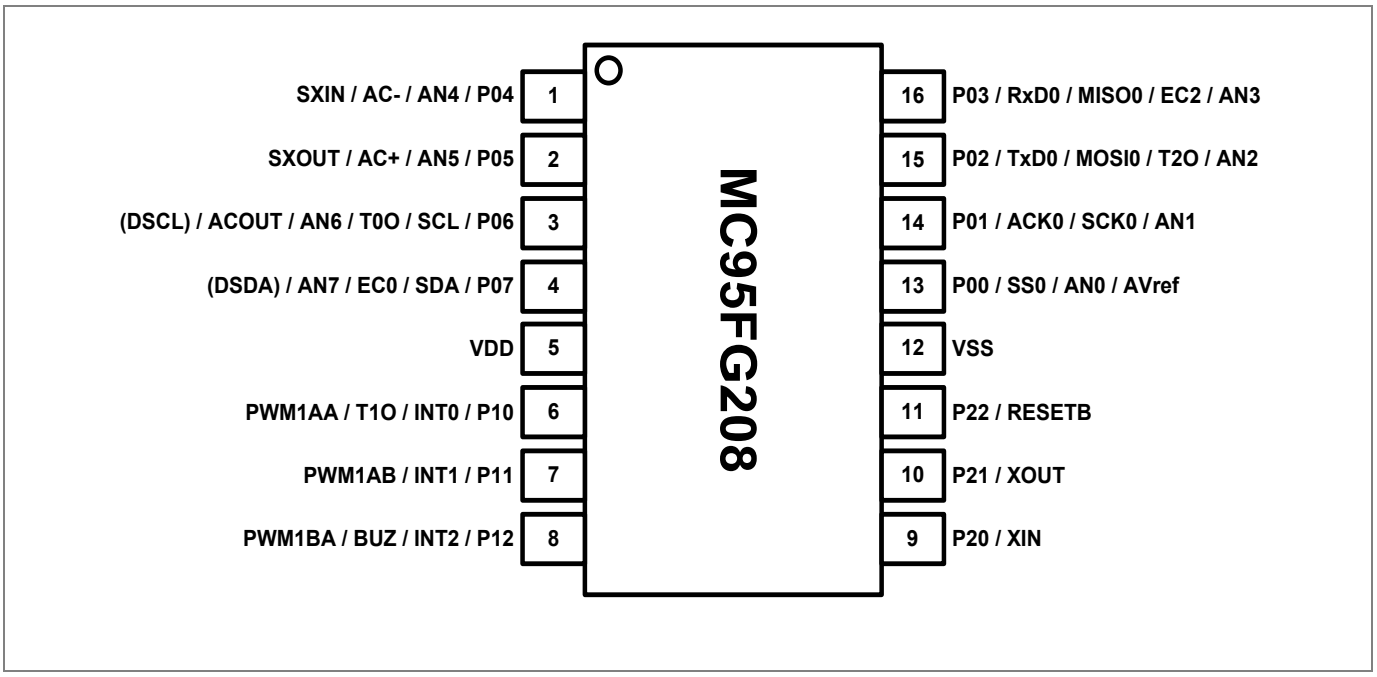


Figure 3.6 MC95FG208 16SOP/TSSOP pin assignmemt

4 Package Diagram

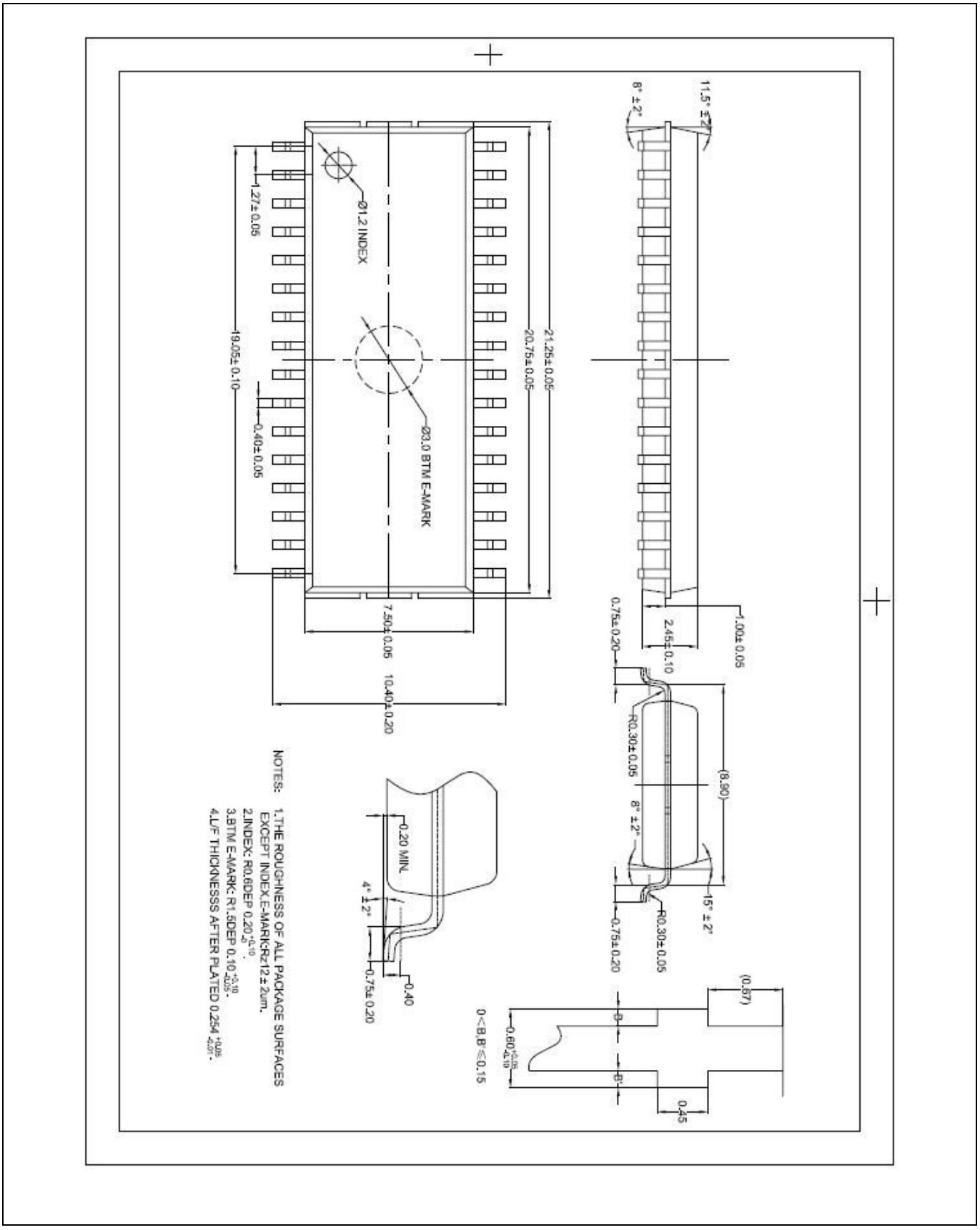


Figure 4.1 32-Pin SOP Package

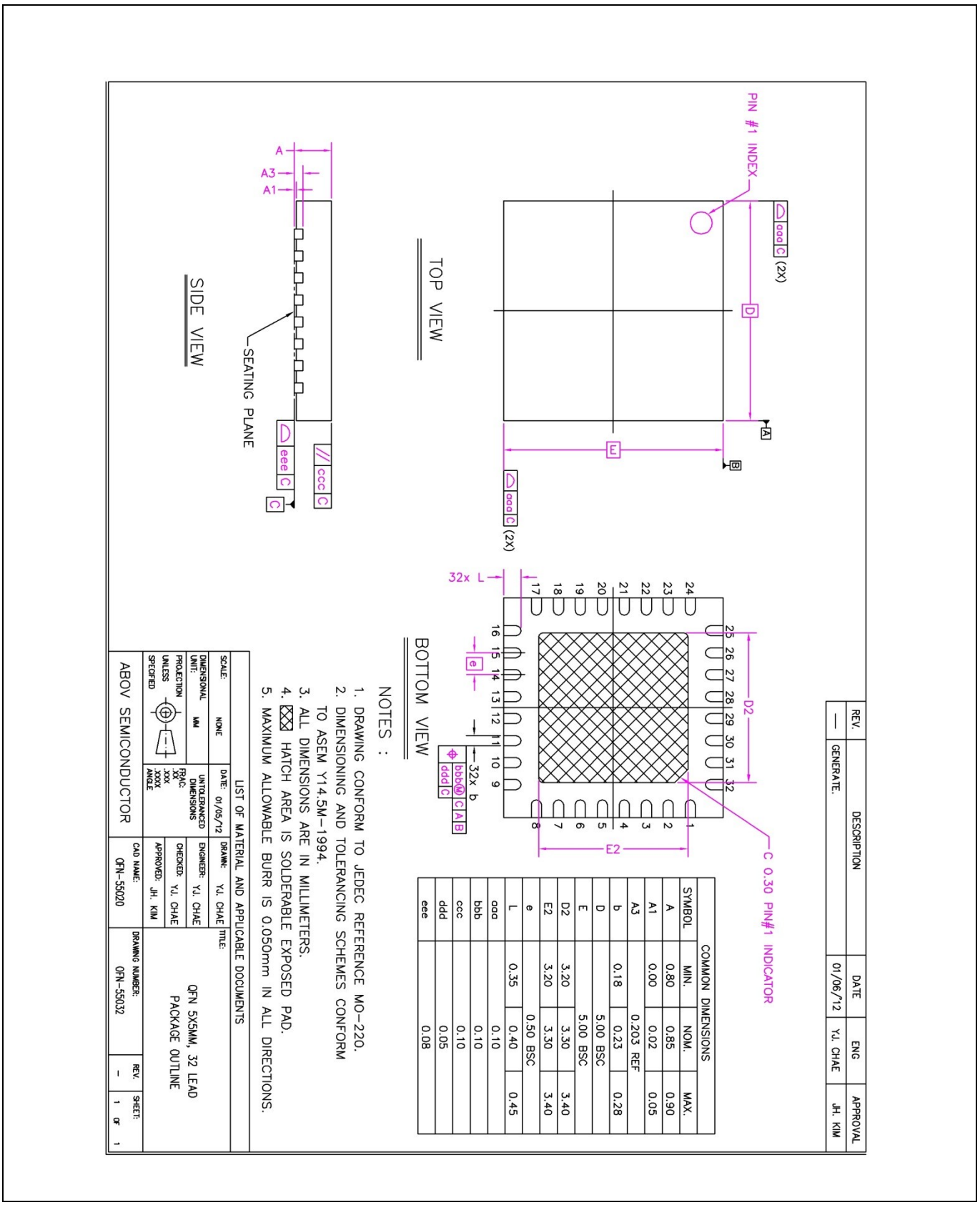
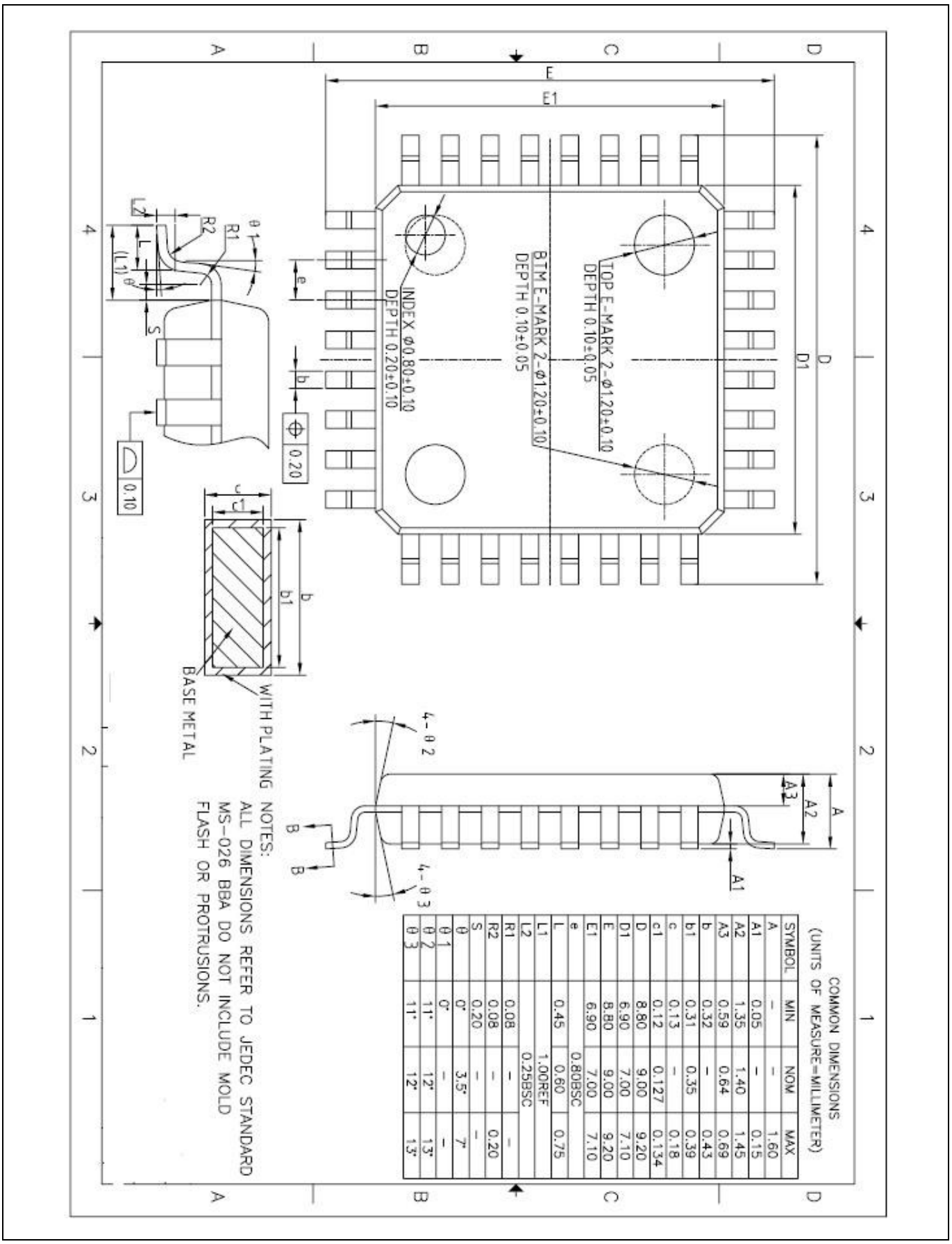


Figure 4.2 32-Pin QFN Package



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32	–	0.43
b1	0.31	0.35	0.39
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e		0.80BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

Figure 4.3 32-Pin LQFP Package

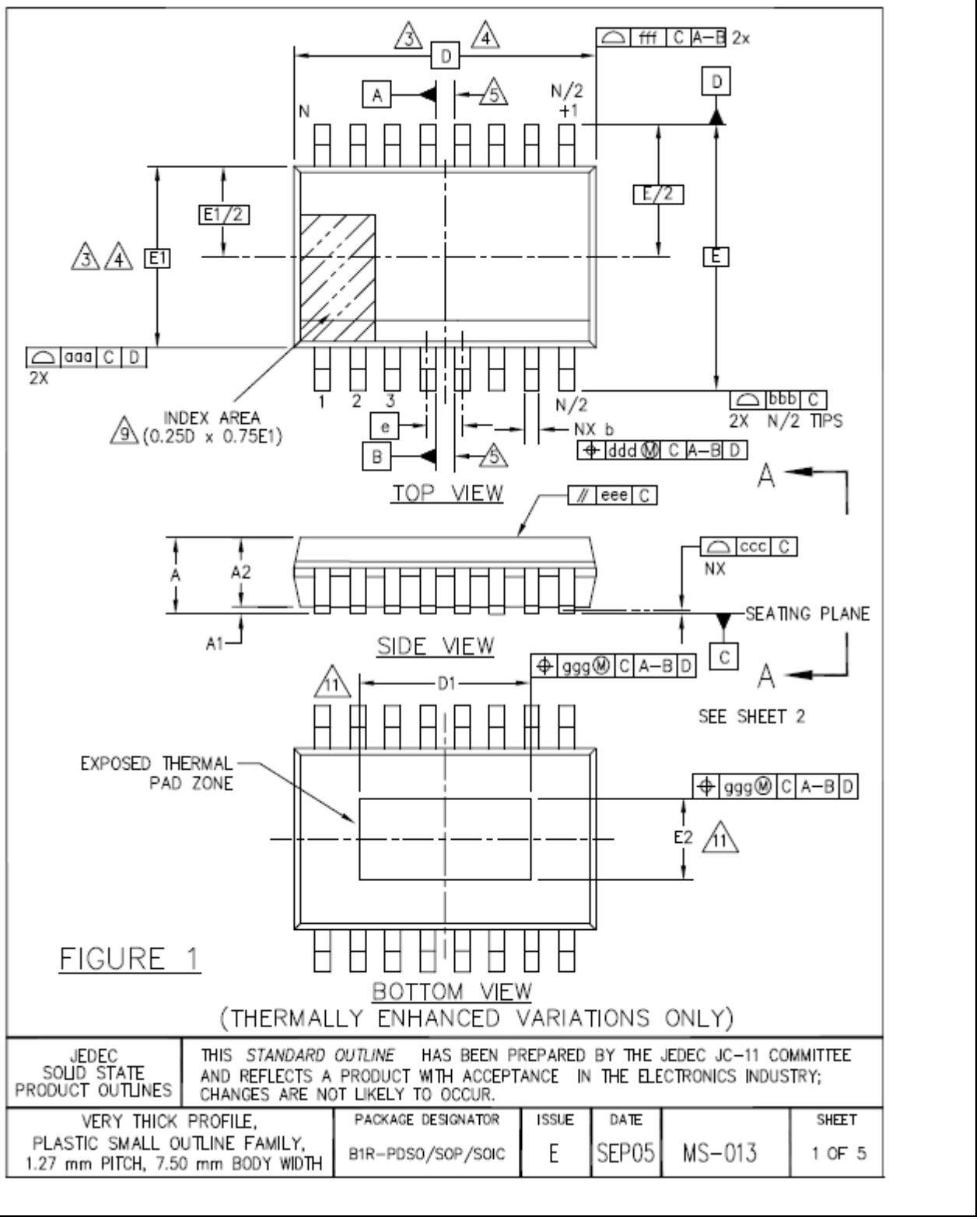


FIGURE 1

Figure 4.4 28-Pin SOP Package

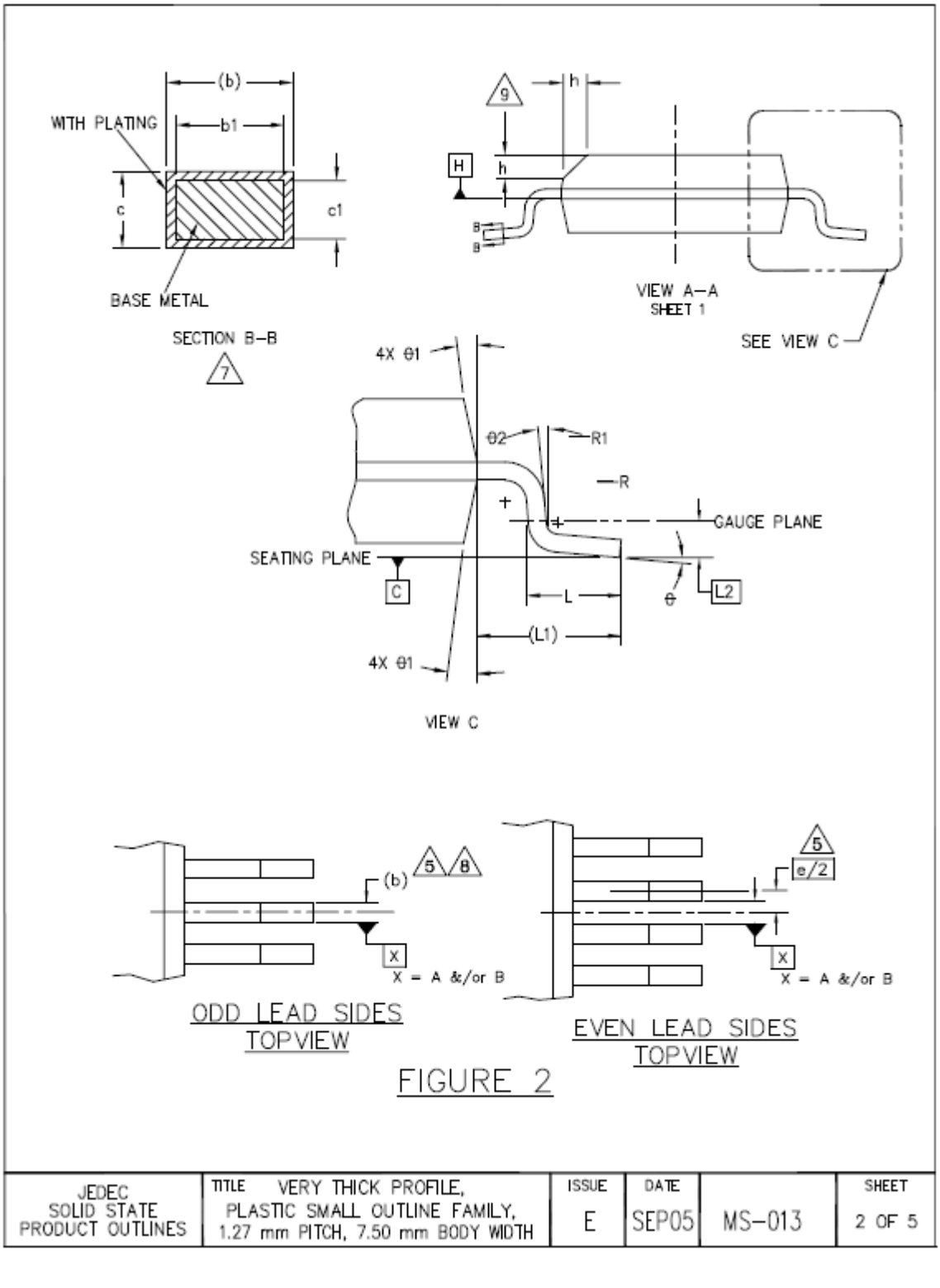


Figure 4.5 28-Pin SOP Package (continue)

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN	NOM	MAX	
A2	2.05	–	–	
b	0.31	–	0.51	7,8
b1	0.27	–	0.48	7,8
c	0.20	–	0.33	7
c1	0.20	–	0.30	7
E	10.30 BSC			
E1	7.50 BSC			3,4
e	1.27 BSC			
L	0.40	–	1.27	
L1	1.40 REF			
L2	0.25 BSC			
R	0.07	–	–	
R1	0.07	–	–	
h	0.25	–	0.75	9
θ	0°	–	8°	
θ1	5°	–	15°	
θ2	0°	–	–	
NOTE	1,2			
REF	11–720S			
ISSUE	E			

SYMBOL	TOLERANCES OF FORM AND POSITION	NOTE
aaa	0.10	
bbb	0.33	
ccc	0.10	
ddd	0.25	
eee	0.10	
fff	0.20	
ggg	0.15	
NOTE	1,2	
REF	11–720S	
ISSUE	E	

VARIATION TABLES

STANDARD

VARIATION ► / SYMBOL ▼		AA	AB	AC	AD	AE	AF	NOTE
A	MIN	---						
	NOM	---						
	MAX	2.65						
A1	MIN	0.10						
	NOM	---						10
	MAX	0.30						
D BSC		10.30	11.55	12.80	15.40	17.90	9.00	3,4
N		16	18	20	24	28	14	6
NOTE								
REF		11–720S						
ISSUE		E						

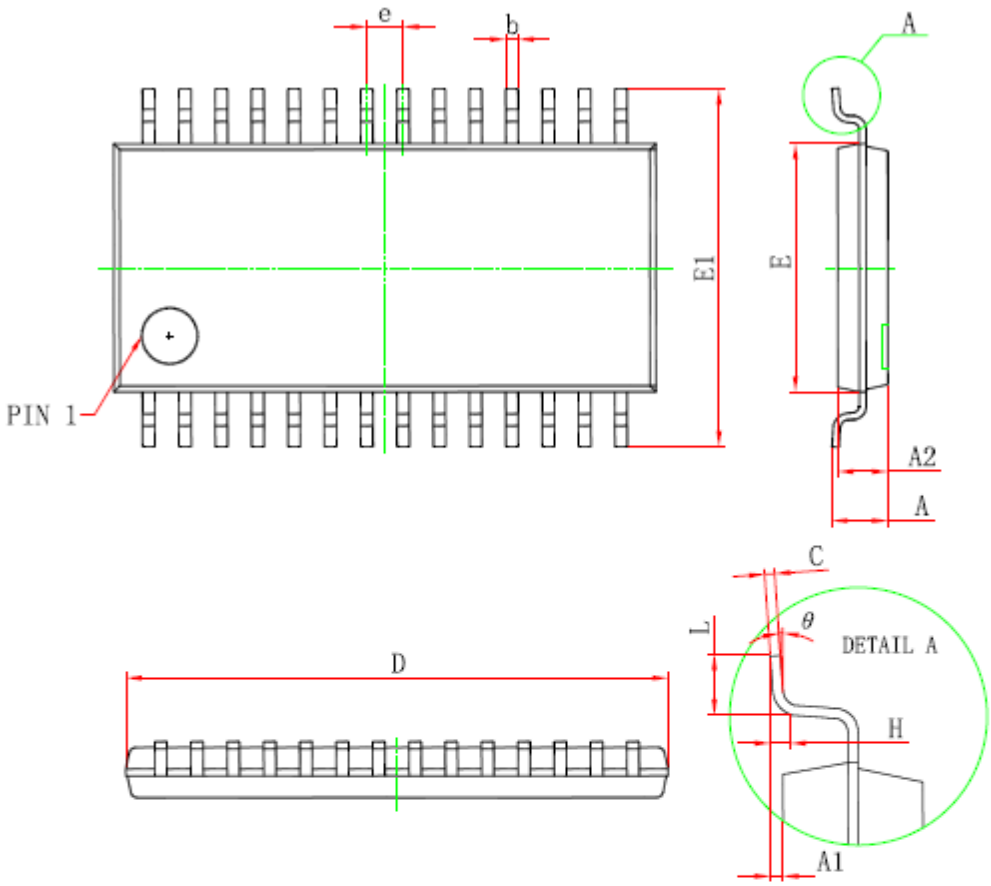
THERMAL

VARIATION ► / SYMBOL ▼		BA	BB	BC	BD	BE	BF	NOTE
A	MIN	---						
	NOM	---						
	MAX	2.50						
A1	MIN	0.00						
	NOM	---						10
	MAX	0.15						
D BSC		10.30	11.55	12.80	15.40	17.90	9.00	3,4
D1	MIN	3.00	3.00	3.00	3.00	3.00	3.00	
	NOM	---	---	---	---	---	---	11
	MAX	---	---	---	---	---	---	
E2	MIN	2.00	2.00	2.00	2.00	2.00	2.00	
	NOM	---	---	---	---	---	---	11
	MAX	---	---	---	---	---	---	
N		16	18	20	24	28	14	6
NOTE								
REF		11–720S						
ISSUE		E						

JEDEC SOLID STATE PRODUCT OUTLINES	TITLE VERY THICK PROFILE, PLASTIC SMALL OUTLINE FAMILY, 1.27 mm PITCH, 7.50 mm BODY WIDTH	ISSUE	DATE		SHEET
		E	SEP05	MS-013	3 OF 5

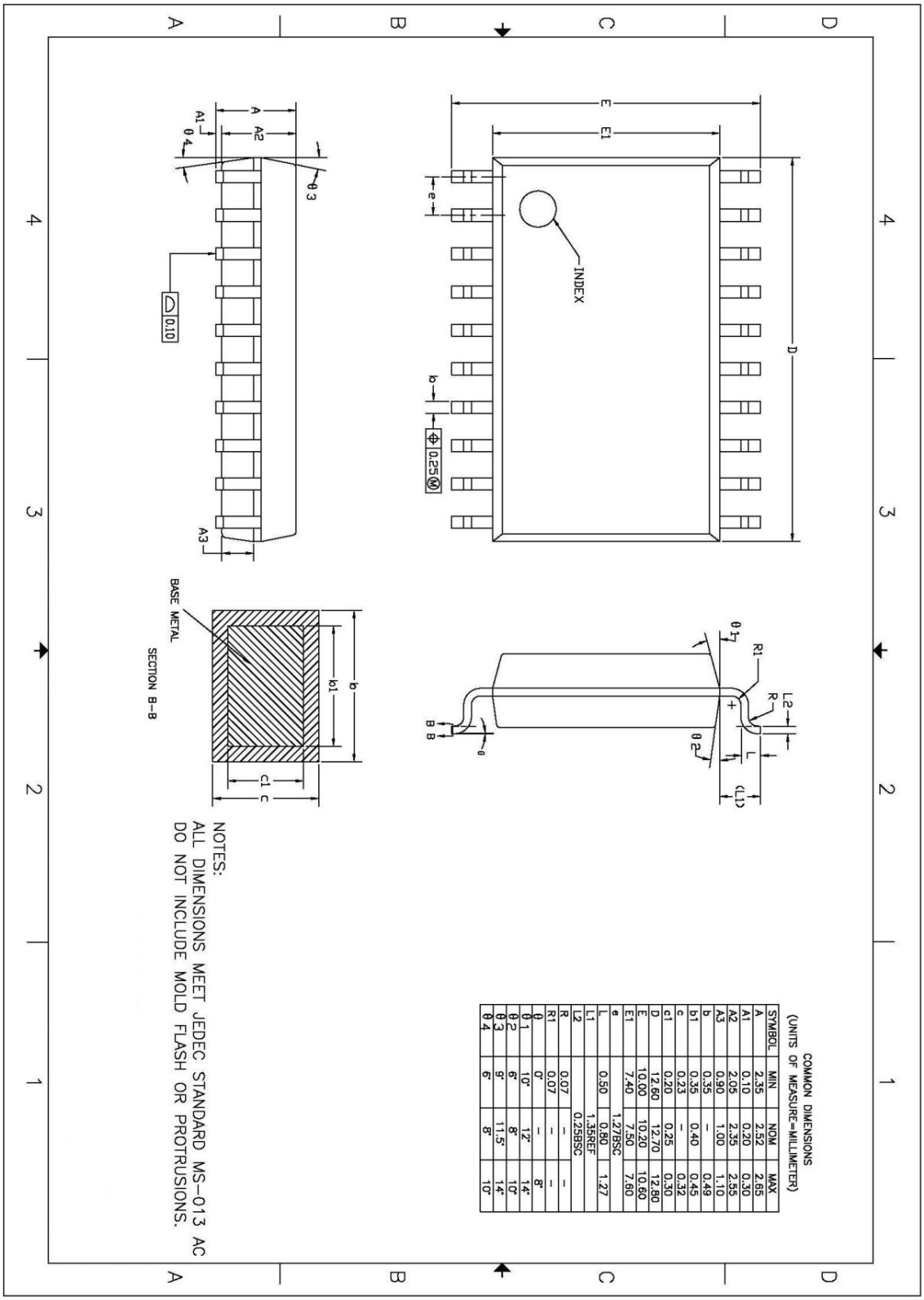
Figure 4.6 28-Pin SOP Package

TSSOP28 PACKAGE OUTLINE DIMENSIONS



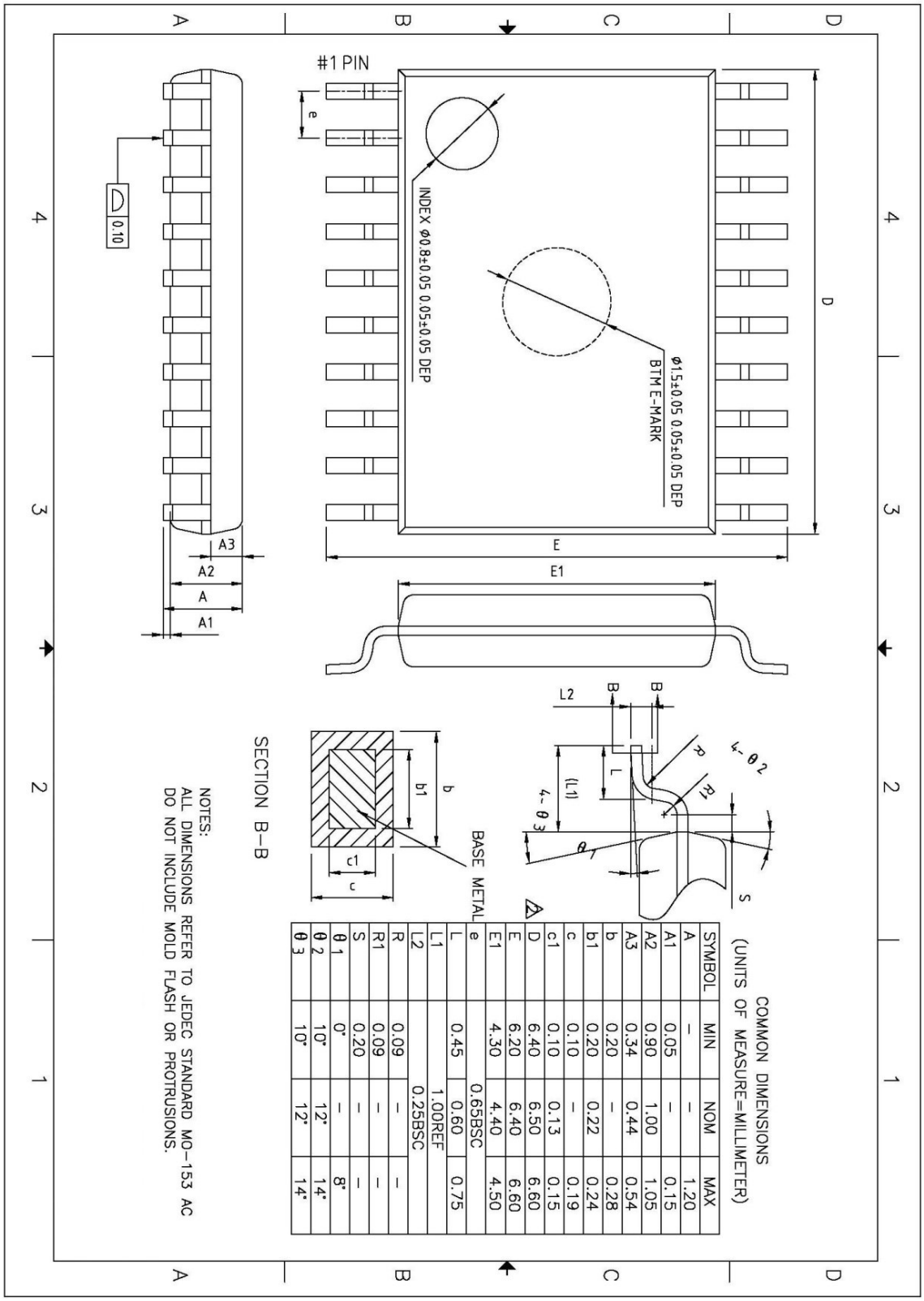
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	9.600	9.800	0.378	0.386
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

Figure 4.7 28-Pin TSSOP Package



SYMBOL	MIN	NOM	MAX
A	2.35	2.52	2.65
A1	0.10	0.20	0.30
A2	2.05	2.35	2.55
A3	0.90	1.00	1.10
b	0.35	–	0.49
b1	0.35	0.40	0.45
c	0.23	–	0.32
c1	0.20	0.25	0.30
D	12.60	12.70	12.80
E	10.00	10.20	10.60
E1	7.40	7.50	7.60
e		1.27BSC	
L	0.50	0.80	1.27
L1		1.35REF	
L2		0.25BSC	
R	0.07	–	–
R1	0.07	–	–
θ	0°	–	8°
θ1	10°	12°	14°
θ2	6°	8°	10°
θ3	9°	11.5°	14°
θ4	6°	8°	10°

Figure 4.8 20-Pin SOP Package



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	–	0.28
b1	0.20	0.22	0.24
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e		0.65BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ1	0°	–	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

Figure 4.9 20-Pin TSSOP Package

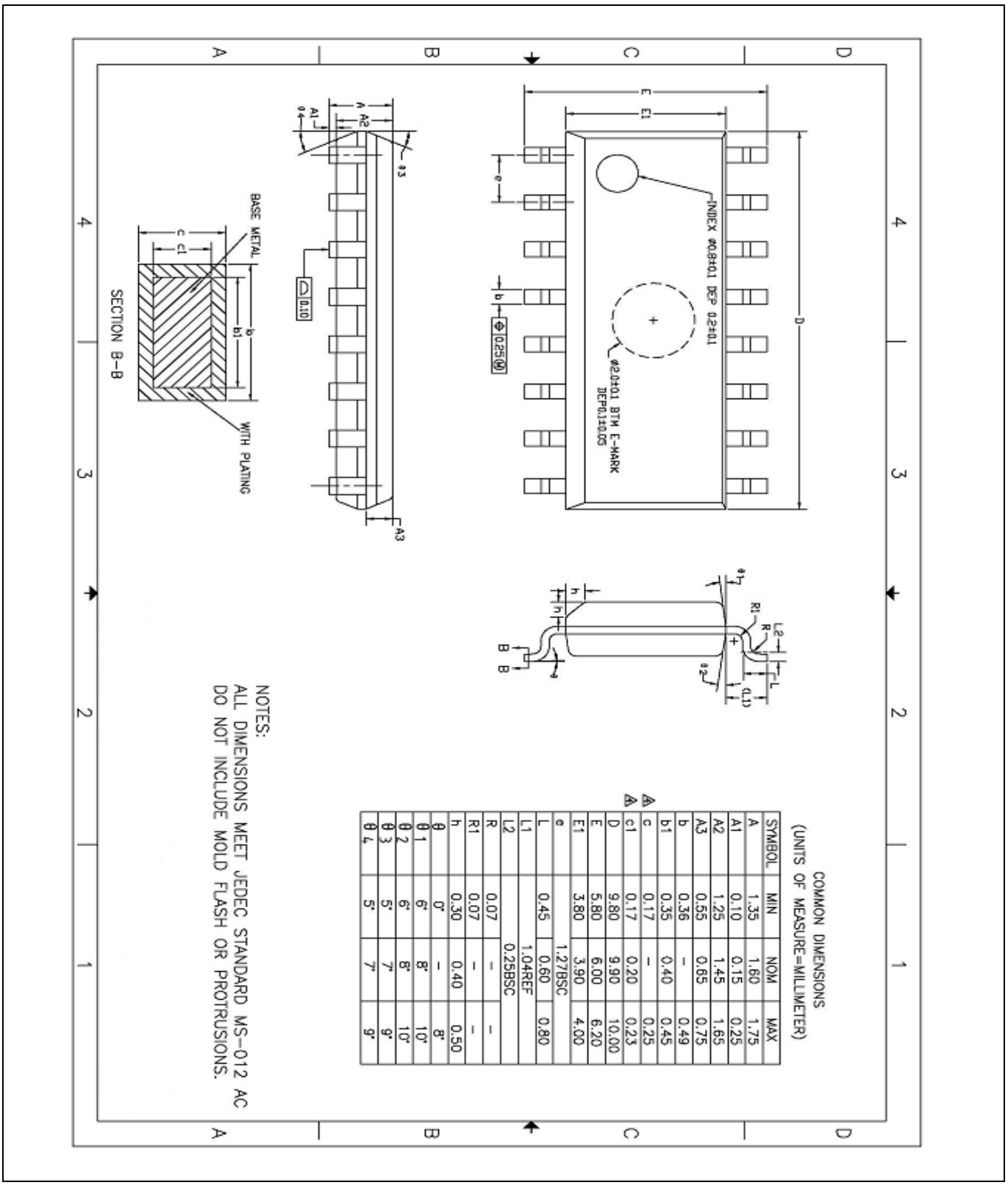
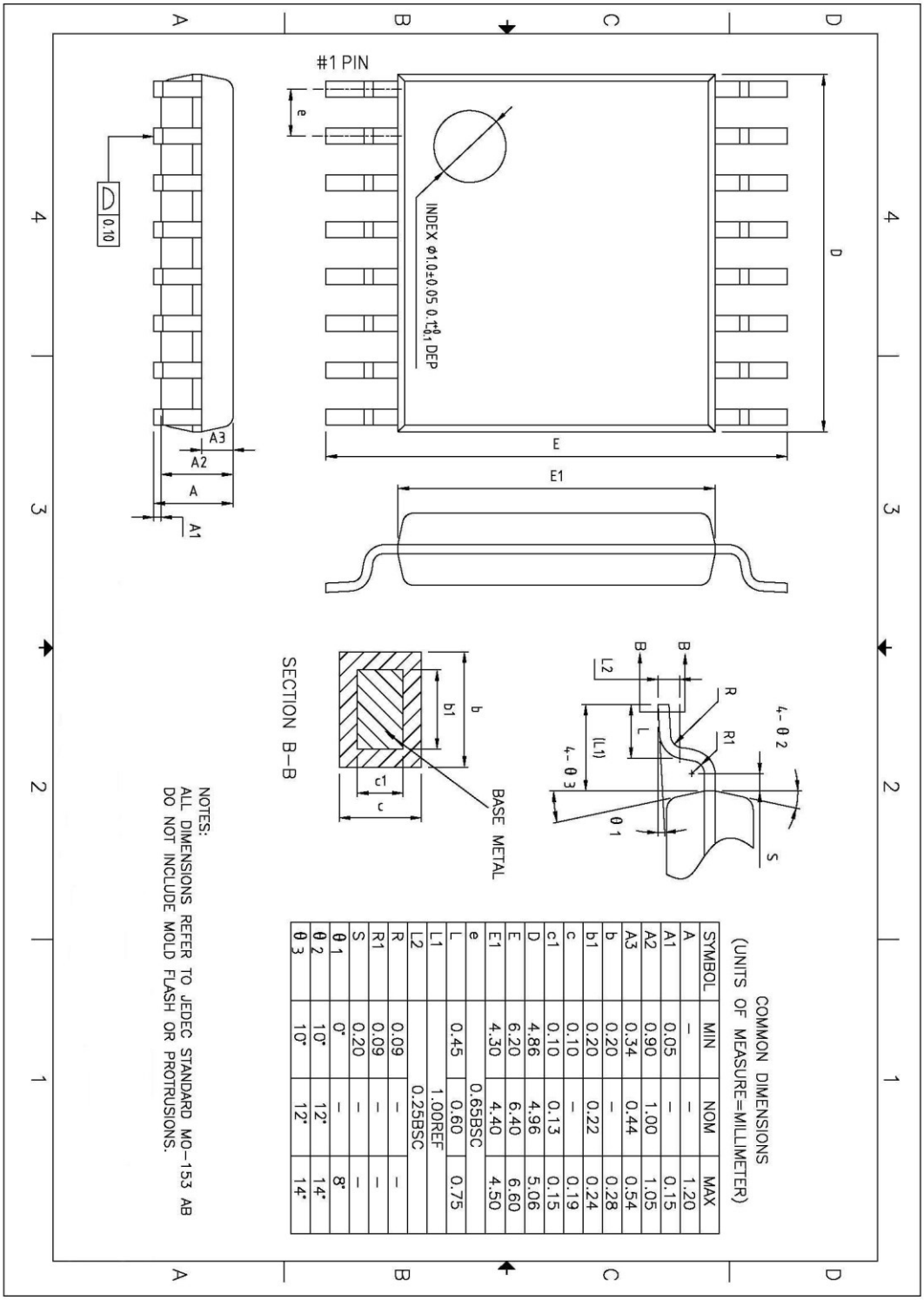


Figure 4.10 16-Pin SOP Package



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	–	0.28
b1	0.20	0.22	0.24
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e		0.65BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ 1	0°	–	8°
θ 2	10°	12°	14°
θ 3	10°	12°	14°

Figure 4.11 16-Pin TSSOP Package

5 Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	Port P0 8-bit I/O Port Can be set in input or output mode in 1-bit units Internal pull-up register can be used via software when this port is used as input port Open Drain enable register can be used via software when this port is used as output port AN0~AN7 can be selected by ADCM register	Input	Avref / AN0 / SS0
P01				AN1 / SCK0 / ACK0
P02				AN2 / T2O / MOSI0 / TxD0
P03				AN3 / EC2 / MISO0 / RxD0
P04				SXIN / AC- / AN4
P05				SXOUT / AC+ / AN5
P06				DSCL / ACOUT/ AN6/ T0O / SCL
P07				DSDA / AN7/ EC0 / SDA
P10	I/O	Port P1 7-bit I/O Port Can be set in input or output mode in 1-bit units Internal pull-up register can be used via software when this port is used as input port Open Drain enable register can be used via software when this port is used as output port AN8, AN9 can be selected by ADCM register	Input	PWM1AA / T1O / INT0
P11				PWM1AB / INT1
P12				PWM1BA / BUZ / INT2
P13				PWM1BB
P14				PWM1CA
P15				AN8 / PWM1CB
P16				AN9 / PWM3 / T3O / INT3
P20	I/O	Port P2 7-bit I/O Port Can be set in input or output mode in 1-bit units Internal pull-up register can be used via software when this port is used as input port Open Drain enable register can be used via software when this port is used as output port AN12, AN13, AN14 can be selected by ADCM register	Input	XIN
P21				XOUT
P22				RESETB
P23				AN12
P24				AN13
P25				AN14 / (SCL)
P26				(SDA)
P30	I/O	Port P3 8-bit I/O Port Can be set in input or output mode in 1-bit units Internal pull-up register can be used via software when this port is used as input port Open Drain enable register can be used via software when this port is used as output port AN10, AN11 can be selected by ADCM register	Input	INT4
P31				INT5
P32				INT6
P33				INT7
P34				SS1
P35				ACK1
P36				AN10 / TxD1
P37				AN11 / RxD1

Table 5.1 Normal Pin Description

6 Port Structures

6.1 General Purpose I/O Port

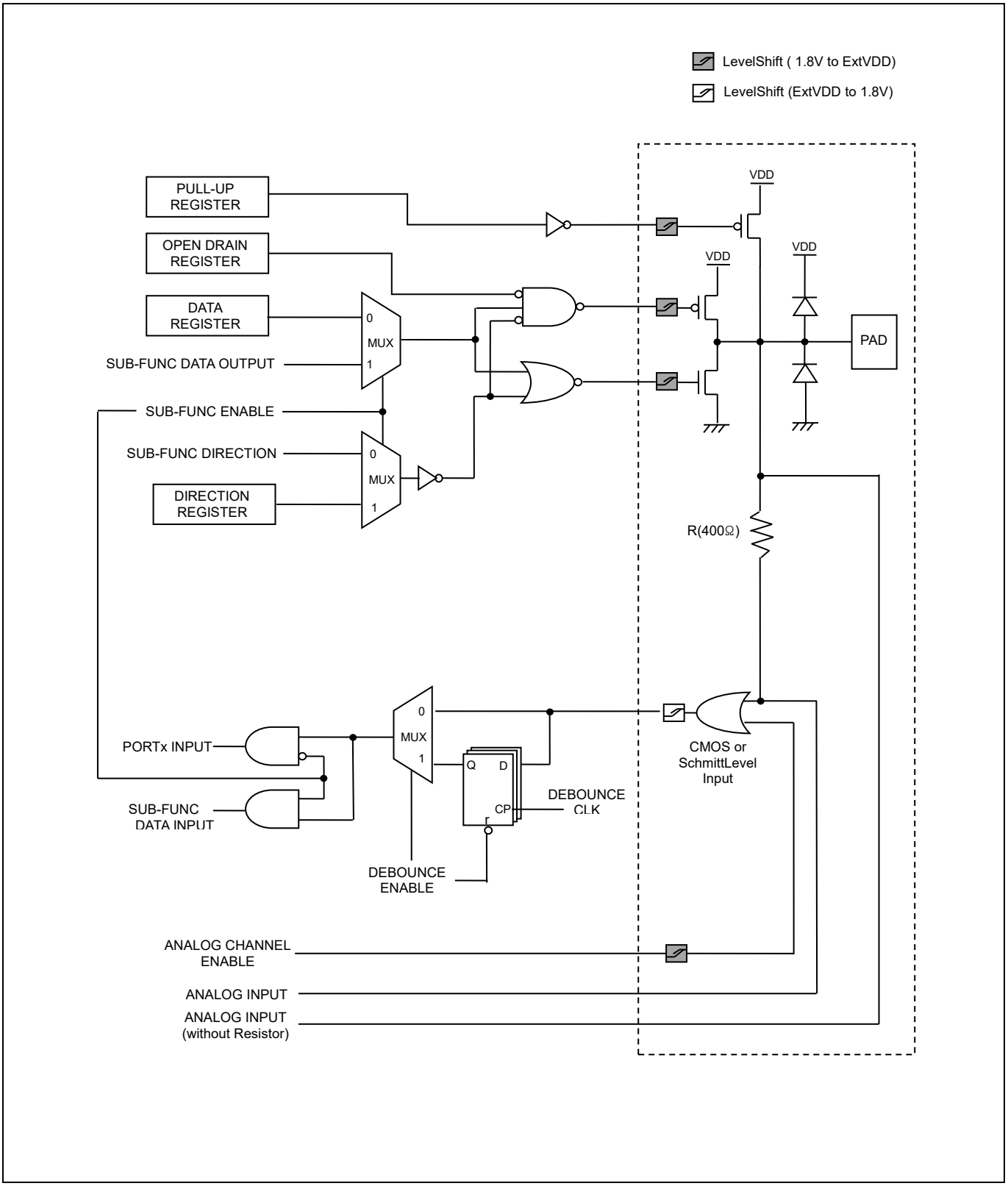


Figure 6.1 General Purpose I/O Port

6.2 External Interrupt I/O Port

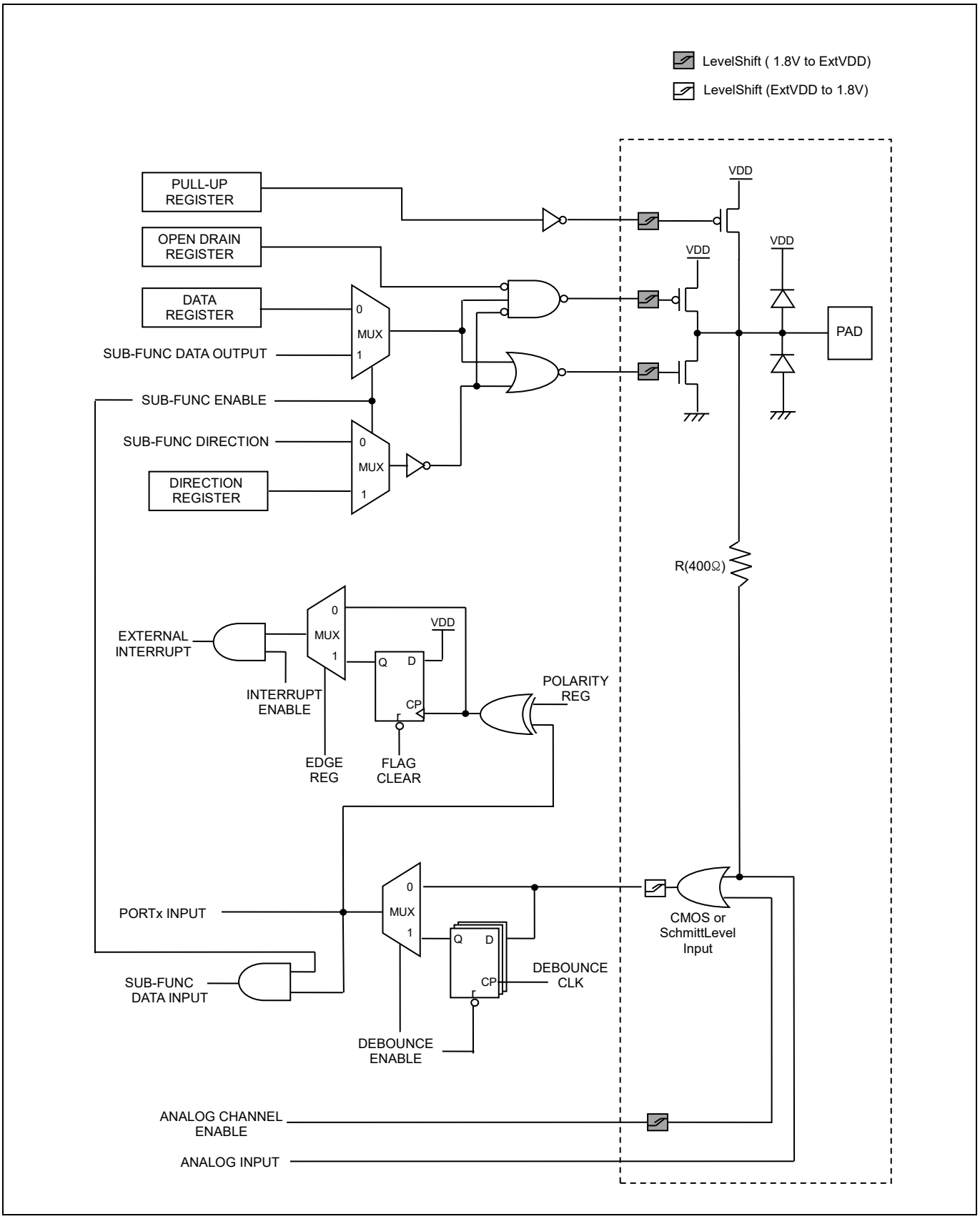


Figure 6.2 External Interrupt I/O Port

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	VDD	-0.3~+6.5	V
	VSS	-0.3~+0.3	V
Normal Voltage Pin	VI	-0.3~VDD+0.3	V
	VO	-0.3~VDD+0.3	V
	IOH	10	mA
	∑IOH	80	mA
	IOL	20	mA
	∑IOL	160	mA
Total Power Dissipation	PT	600	mW
Storage Temperature	TSTG	-65~+150	℃

Table 7.1 Absolute Maximum Ratings

NOTE)

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Supply Voltage	VDD	fXIN=1~12MHz	4.5	-	5.5	V
		fXIN=1~8MHz	1.8			
		fSUB=32.768kHz				
Operating Temperature	TOPR	VDD=1.8~5.5V	-40	-	85	℃
Operating Frequency	FOPR	fXIN	1	-	12	MHz
		fSUB	-	32.768	-	kHz
		Internal RC-OSC	7.76	8	8.24	MHz
		Internal Ring-OSC	-	1		MHz

Table 7.2 Recommended Operating Conditions

7.3 A/D Converter Characteristics

(TA=-40℃ ~ +85℃, VDD=AVDD=2.7V ~ 5.5V, VSS=0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
A/D converting Resolution	-	-	-	12	-	bits
Integral Linearity Error	ILE	Vref=5.12V, Vss=0V, TA=+25℃	-	-	±3	LSB
Differential Linearity Error	DLE		-	-	±2	
Offset Error of Top	EOT		-	-±1	±3	
Zero Offset Error	EOB		-	±1	±3	
Overall Accuracy	-		-	±3	-	
Conversion Time	tCONV	-	-	60	-	Cycle
Analog Input Voltage	VAIN	-	VSS	-	Vref	V
Analog Reference Voltage	Vref	(note)	1.8	-	5.5	V
Analog Input Current	IAIN	VDD=Vref=5V	-	-	10	uA
Analog Block Current	IAVDD	VDD=Vref=5V VDD=Vref=3V	-	1 0.5	3 1.5	mA
		VDD=Vref=5V Power down mode	-	100	500	nA
BGR	-	VDD=5V, TA=+25℃	-	1.67	-	V
		VDD=4V, TA=+25℃	-	1.63	-	
		VDD=3V, TA=+25℃	-	1.62	-	

Table 7.3 A/D Converter Characteristics

(note) When AVREF is lower than 2,7V, the ADC resolution is worse

7.4 Analog Comparator Characteristics

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Leakage Current	I_L	VDDEXT=5V, Vin=1/2VDDEXT	-50	-	50	nA
Input Offset Voltage	V_{offset}	VDDEXT=5V, Vin=1/2VDD	10	-	40	±mV
Operating Current	IOP	COMP_EN=H	-	1	-	mA
Power Down Current	IPD	COMP_EN=L	-	1	-	uA
Response Time	V_{RT}	CL= 50pF, VDDEXT=5V	-	-	500	ns

Table 7.4 Analog Comparator Characteristics

7.5 Voltage Dropout Converter Characteristics

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Operating Voltage		-	1.8	-	5.5	V
Operating Temperature		-	-40	-	+85	℃
Regulation Voltage		-	1.62	1.8	1.98	V
Drop-out Voltage		-	-	-	0.02	V
Current Drivability		RUN/IDLE	-	20	-	mA
		SUB-ACTIVE	-	1	-	mA
		STOP1	-	50	-	uA
		STOP2	-	10	-	uA
Operating Current	IDD1	RUN/IDLE	-	-	1	mA
	IDD2	SUB-ACTIVE	-	-	0.1	mA
	SIDD1	STOP1	-	-	5	uA
	SIDD2	STOP2	-	-	0.1	uA
Drivability Transition Time	TRAN1	SUB to RUN	-	-	1	us
	TRAN2	STOP to RUN	-	-	200	us

Table 7.5 Voltage Dropout Converter Characteristics

NOTE)

1. -STOP1: WDT running - STOP2: WDT disable

7.6 Power-On Reset Characteristics

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Operating Voltage		-	VSS	-	5.5	V
Operating Temperature		-	-40	-	+85	℃
RESET Release Level		-	1.3	1.4	1.5	V
Operating Current	IDD	-	-	-	10	uA
	SIDD	-	-	-	1	uA

Table 7.6 Power-On Reset Characteristics

7.7 Brown Out Detector Characteristics

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Operating Voltage		-	VSS	-	5.5	V
Operating Temperature		-	-40	-	+85	℃
Detection Level	4.2V	-	4.0	-	4.4	V
	3.6V	-	3.4	-	3.8	V
	2.5V	-	2.3	-	2.7	V
	1.6V	-	1.4	-	1.8	V
Hysteresis		-	-	-	-	mV
Operating Current	IDD	-	-	-	50	uA
	SIDD	-	-	-	1	uA

Table 7.7 Brown Out Detector Characteristics

7.8 Internal RC Oscillator Characteristics

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Operating Voltage		-	1.8	-	5.5	V
Operating Temperature		-	-40	-	+85	℃
Frequency		-	7.76		8.24	MHz
Stabilization Time		-	-	-	10	ms
Operating Current	IDD	-	-	-	-	uA
	SIDD	-	-	-	1	uA

Table 7.8 Internal RC Oscillator Characteristics

7.9 Ring-Oscillator Characteristics

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Operating Voltage		-	1.8	-	5.5	V
Operating Temperature		-	-40	-	+85	℃
Frequency		-	-	1	-	MHz
Stabilization Time		-	-	-	-	ms
Operating Current	IDD	-	-	-	-	uA
	SIDD	-	-	-	1	uA

Table 7.9 Ring-Oscillator Characteristics

7.10 PLL Characteristics

(TA = 0℃ ~ +70℃, VDD18 = 1.6V ~ 2.0V, VSS = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
PLL current	IPLL	-	-	1.5	TBD	mA
Input clock frequency	fxin	-	2	-	16	MHz
Output clock frequency	fout	-	6.25	-	128	MHz
Output clock duty	-	-	40	-	60	%
Setting time	tD	-	-	1	-	ms
Accuracy	-	-	-	2	-	%

Table 7.10 PLL Characteristics

7.11 DC Characteristics

(VDD =2.7~5.5V, VSS =0V, fXIN=10.0MHz, TA=-40~+85℃)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Low Voltage	VIL1	P2[2]	-0.5	-	0.2VDD	V
	VIL2	All others PAD	-0.5	-	0.2VDD	V
Input High Voltage	VIH1	P2[2]	0.8VDD	-	VDD	V
	VIH2	All others PAD	0.7VDD	-	VDD	V
Output Low Voltage	VOL1	ALL I/O (IOL=20mA, VDD=4.5V)	-	-	1	V
Output High Voltage	VOH1	ALL I/O (IOH=-8.57mA, VDD=4.5V)	3.5	-	-	V
Input High Leakage Current	IIH	ALL PAD	-	-	1	uA
Input Low Leakage Current	IIL	ALL PAD	-1	-	-	uA
Pull-Up Resister	RPU	ALL PAD	20	-	50	kΩ
Power Supply Current	IDD1	Run Mode, fXIN=12MHz @5V	-	*2.6	10	mA
	IDD2	Sleep Mode, fXIN=12MHz @5V	-	*1.5	5	mA
	IDD3	Sub Active Mode, fSUBXIN=32.768kHz @5V	-	*71	500	uA
	IDD4	STOP1 Mode, WDT Active @5V (BOD enable)	-	*45	200	uA
	IDD5	STOP1 Mode, WDT Active @5V (BOD disable)	-	*20	100	uA
	IDD6	STOP2 Mode, WDT Disable @5V (BOD enable)	-	*27	100	uA
	IDD7	STOP2 Mode, WDT Disable @5V (BOD disable)	-	*1	7 (room temp)	uA

Table 7.11 DC Characteristics

NOTE)

1. STOP1: WDT running, STOP2: WDT disable.
2. (*) typical test condition : VDD=5V, Internal RC-OSC=8MHz, ROOM TEMP, all PORT output LOW, Timer0 Active, 1PORT toggling

7.12 AC Characteristics

(VDD=5.0V±10%, VSS=0V, TA=-40~+85℃)

Parameter	Symbol	PIN	MIN	TYP	MAX	Unit
Operating Frequency	fMCP	XIN	1	-	10	MHz
System Clock Cycle Time	tSYS	-	100	-	1000	ns
Oscillation Stabilization Time (8MHz)	tMST1	XIN, XOUT	-	-	10	ms
External Clock “H” or “L” Pulse Width	tCPW	XIN	90	-	-	ns
External Clock Transition Time	tRCP,tFCP	XIN	-	-	10	ns
External Interrupt Input Width	tIW	INT0~INTx	2	-	-	tSYS
External Interrupt Transition Time	tFI,tRI	INT0~INTx			1	us
nRESET Input Pulse “L” Width	tRST	nRESET	8	-	-	tSYS
External Counter Input “H” or “L” Pulse Width	tECW	EC0~ECx	2	-	-	tSYS
Event Counter Transition Time	tREC,tFEC	EC0~ECx	-	-	20	ns

Table 7.12 AC Characteristics

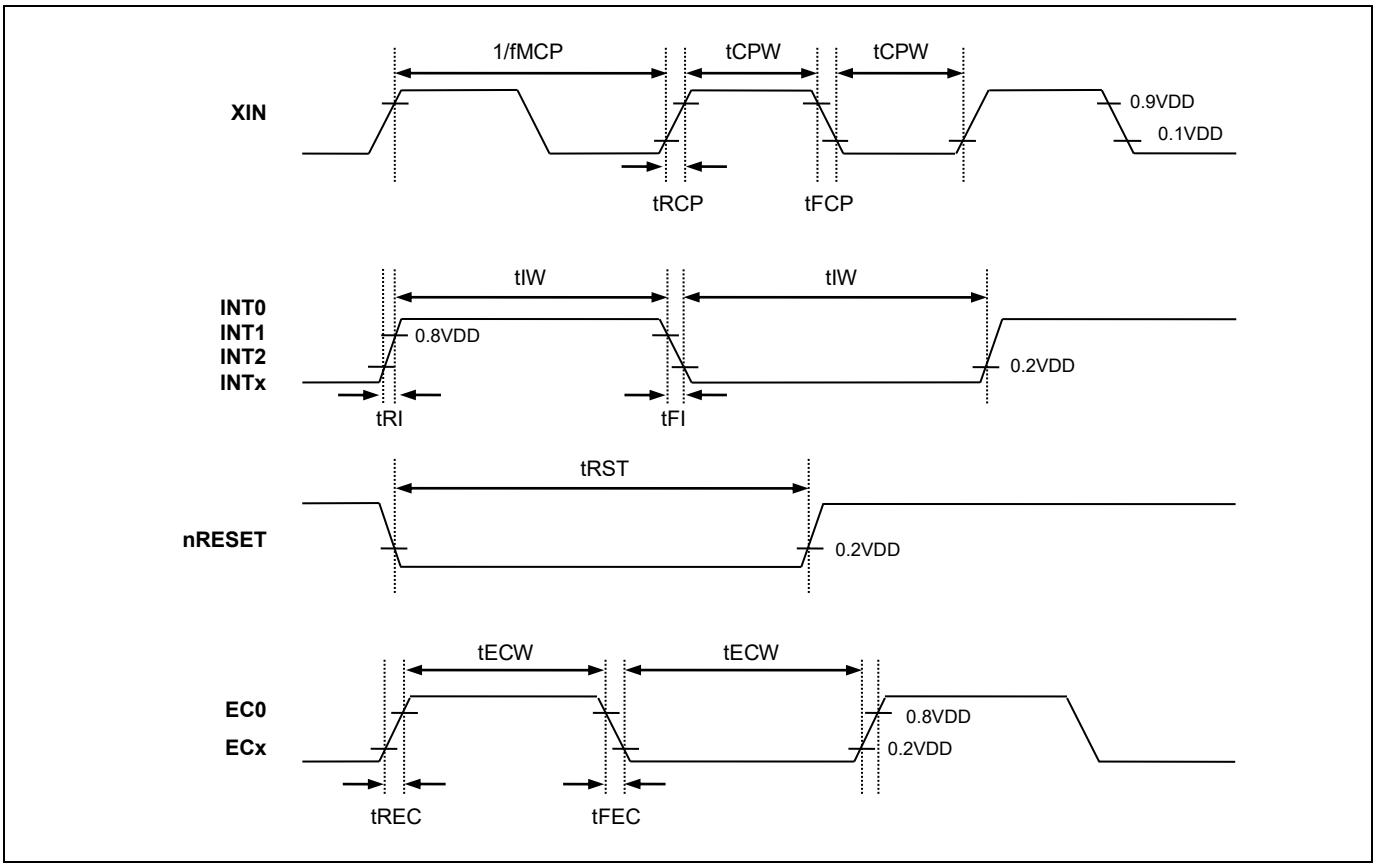


Figure 7.1 AC Timing

7.13 SPI Characteristics

(VDD=5.0V±10%, VSS=0V, TA=-40~+85℃)

Parameter	Symbol	PIN	MIN	TYP	MAX	Unit
Output Clock Pulse Period	tSCK	SCK	-	SPI clock mode	-	ns
Input Clock Pulse Period	tSCK	SCK	2• tSYS	-	-	ns
Input Clock “H” or “L” Pulse Width	tSCKL, tSCKH	SCK		50% duty	-	ns
Input Clock Pulse Transition Time	tFSCK,tRSCK	SCK	-	-	30	ns
Output Clock “H” or “L” Pulse Width	tSCKL, tSCKH	SCK	tSYS-30	-	-	ns
Output Clock Pulse Transition Time	tFSCK,tRSCK	SCK	-	-	30	ns
First Output Clock Delays Time	tFOD	OUTPUT				
Output Clock Delay Time	tDS	OUTPUT	-	-	100	ns
Input Pulse Transition Time	tFSIN,tRSIN	INPUT	-	-	30	ns
Input Setup Time	tDIS	INPUT	100		-	ns
Input Hold Time	tDIH	INPUT	tSYS+70	-	-	ns

Table 7.13 SPI Characteristics

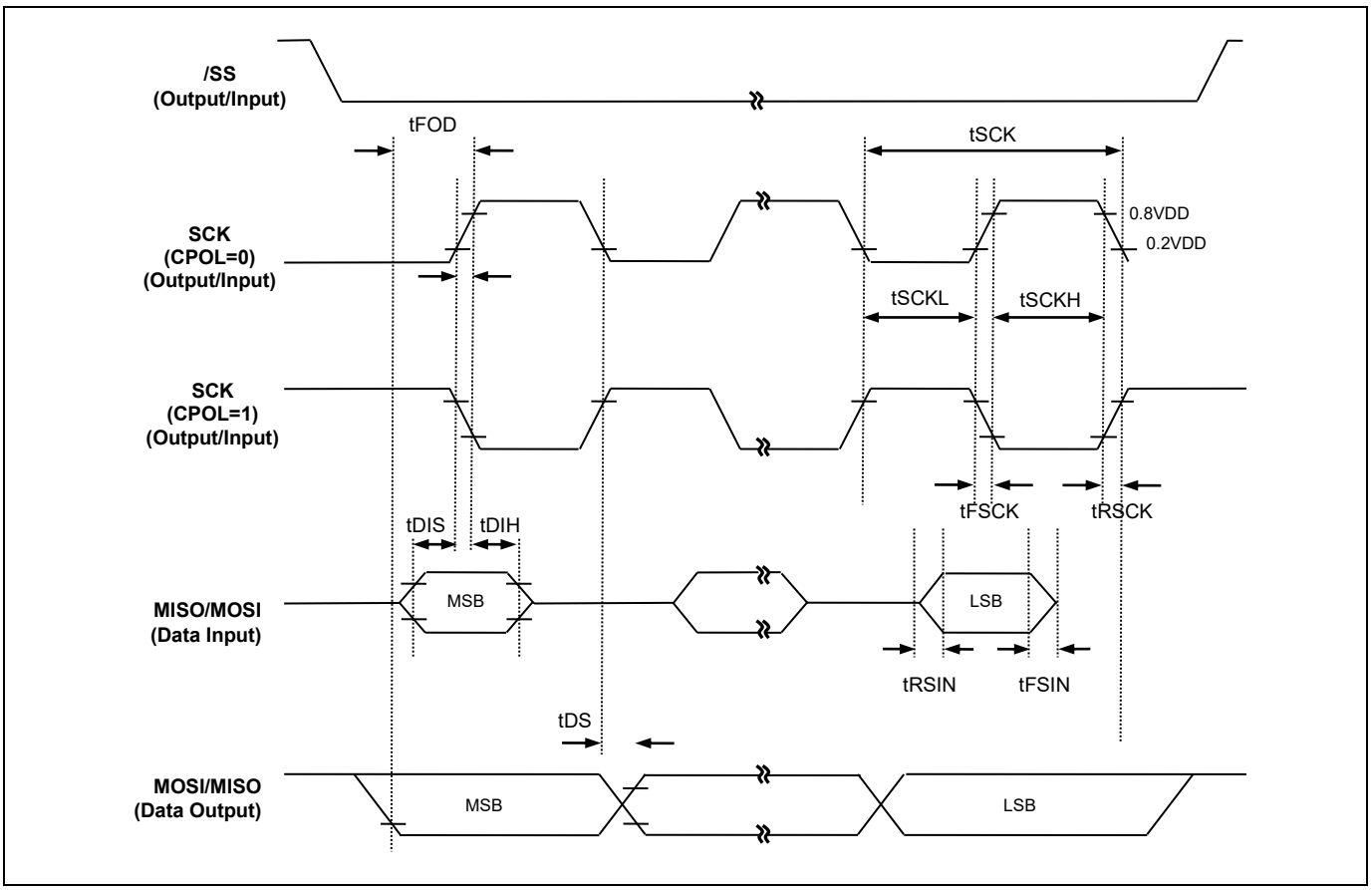


Figure 7.2 SPI Timing

7.14 Main Clock Oscillator Characteristics

(VDD=5.0V±10%, VSS=0V, TA=-40~+85℃)

Parameter	MIN	TYP	MAX	ETC
Operating Voltage (VDDEXT)	1.5V		5.5V	
TEMP	-40℃		85℃	
IDD	-	660uA	-	@4Mhz, VDDEXT(+5V)
Operating Frequency	-		12Mhz	
Ext. Load Cap	5pF	22pF	35pF	C1,C2

Table 7.14 Main Clock Oscillator Characteristics

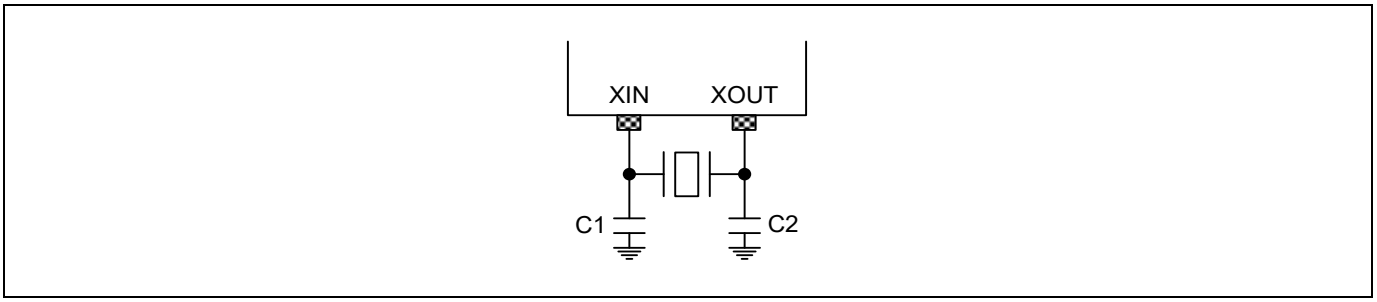


Figure 7.3 Crystal Oscillator

7.15 Sub Clock Oscillator Characteristics

(VDD=5.0V±10%, VSS=0V, TA=-40~+85℃)

Parameter	MIN	TYP	MAX	ETC
Operating Voltage	-	1.8V	-	
TEMP	-40℃	-	85℃	
IDD	-	3uA	-	
Operating Frequency	-	32.768kHz	-	
Ext. Load Cap	5pF	15pF	20pF	C1,C2

Table 7.15 Sub Clock Oscillator Characteristics

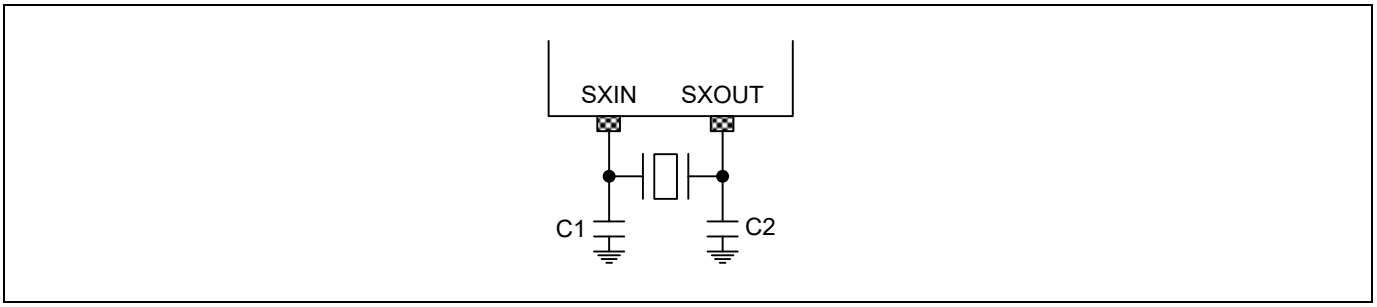


Figure 7.4 Sub-Crystal Oscillator

7.16 Typical Characteristics

These graphs and tables provided in this section are for design guidance only and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

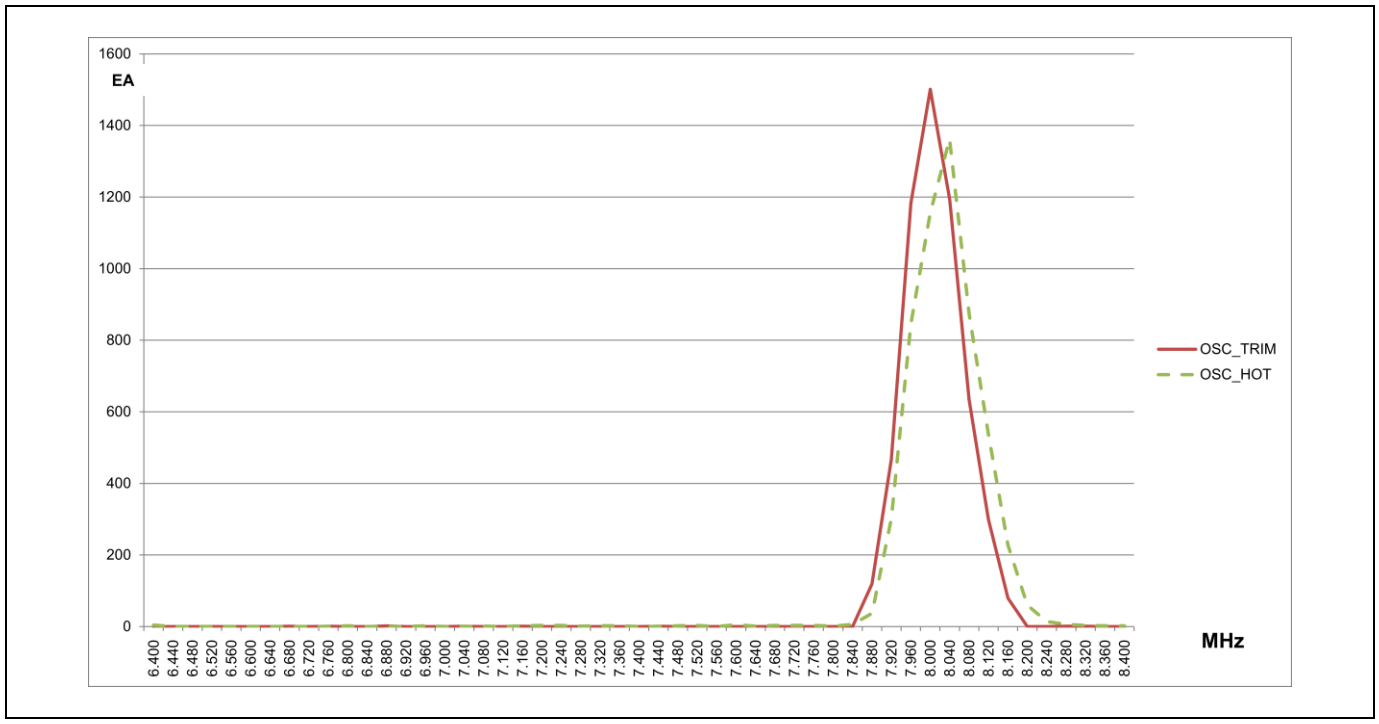


Figure 7.5 8MHz Internal OSC Freq.(OSC_HOT: 85℃)

8 APPENDIX

A. Instruction Table

Instructions are either 1, 2 or 3 bytes long as listed in the 'Bytes' column below.

Each instruction takes either 1, 2 or 4 machine cycles to execute as listed in the following table. 1 machine cycle comprises 2 system clock cycles.

ARITHMETIC				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ADD A,Rn	Add register to A	1	1	28-2F
ADD A,dir	Add direct byte to A	2	1	25
ADD A,@Ri	Add indirect memory to A	1	1	26-27
ADD A,#data	Add immediate to A	2	1	24
ADDC A,Rn	Add register to A with carry	1	1	38-3F
ADDC A,dir	Add direct byte to A with carry	2	1	35
ADDC A,@Ri	Add indirect memory to A with carry	1	1	36-37
ADDC A,#data	Add immediate to A with carry	2	1	34
SUBB A,Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	1	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	1	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC dir	Increment direct byte	2	1	05
INC @Ri	Increment indirect memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC dir	Decrement direct byte	2	1	15
DEC @Ri	Decrement indirect memory	1	1	16-17
INC DPTR	Increment data pointer	1	2	A3
MUL AB	Multiply A by B	1	4	A4
DIV AB	Divide A by B	1	4	84
DA A	Decimal Adjust A	1	1	D4

LOGICAL				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ANL A,Rn	AND register to A	1	1	58-5F
ANL A,dir	AND direct byte to A	2	1	55
ANL A,@Ri	AND indirect memory to A	1	1	56-57
ANL A,#data	AND immediate to A	2	1	54
ANL dir,A	AND A to direct byte	2	1	52
ANL dir,#data	AND immediate to direct byte	3	2	53
ORL A,Rn	OR register to A	1	1	48-4F
ORL A,dir	OR direct byte to A	2	1	45
ORL A,@Ri	OR indirect memory to A	1	1	46-47
ORL A,#data	OR immediate to A	2	1	44
ORL dir,A	OR A to direct byte	2	1	42
ORL dir,#data	OR immediate to direct byte	3	2	43
XRL A,Rn	Exclusive-OR register to A	1	1	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	1	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	1	66-67
XRL A,#data	Exclusive-OR immediate to A	2	1	64
XRL dir,A	Exclusive-OR A to direct byte	2	1	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	2	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13

DATA TRANSFER				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOV A,Rn	Move register to A	1	1	E8-EF
MOV A,dir	Move direct byte to A	2	1	E5
MOV A,@Ri	Move indirect memory to A	1	1	E6-E7
MOV A,#data	Move immediate to A	2	1	74
MOV Rn,A	Move A to register	1	1	F8-FF
MOV Rn,dir	Move direct byte to register	2	2	A8-AF
MOV Rn,#data	Move immediate to register	2	1	78-7F
MOV dir,A	Move A to direct byte	2	1	F5
MOV dir,Rn	Move register to direct byte	2	2	88-8F
MOV dir,dir	Move direct byte to direct byte	3	2	85
MOV dir,@Ri	Move indirect memory to direct byte	2	2	86-87
MOV dir,#data	Move immediate to direct byte	3	2	75
MOV @Ri,A	Move A to indirect memory	1	1	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	2	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	1	76-77
MOV DPTR,#data	Move immediate to data pointer	3	2	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative PC to A	1	2	83
MOVX A,@Ri	Move external data(A8) to A	1	2	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	2	E0
MOVX @Ri,A	Move A to external data(A8)	1	2	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	2	F0
PUSH dir	Push direct byte onto stack	2	2	C0
POP dir	Pop direct byte from stack	2	2	D0
XCH A,Rn	Exchange A and register	1	1	C8-CF
XCH A,dir	Exchange A and direct byte	2	1	C5
XCH A,@Ri	Exchange A and indirect memory	1	1	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	1	D6-D7

BOOLEAN				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	1	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	1	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	1	B2
ANL C,bit	AND direct bit to carry	2	2	82
ANL C,/bit	AND direct bit inverse to carry	2	2	B0
ORL C,bit	OR direct bit to carry	2	2	72
ORL C,/bit	OR direct bit inverse to carry	2	2	A0
MOV C,bit	Move direct bit to carry	2	1	A2
MOV bit,C	Move carry to direct bit	2	2	92

BRANCHING				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ACALL addr 11	Absolute jump to subroutine	2	2	11→F1
LCALL addr 16	Long jump to subroutine	3	2	12
RET	Return from subroutine	1	2	22
RETI	Return from interrupt	1	2	32
AJMP addr 11	Absolute jump unconditional	2	2	01→E1
LJMP addr 16	Long jump unconditional	3	2	02
SJMP rel	Short jump (relative address)	2	2	80
JC rel	Jump on carry = 1	2	2	40
JNC rel	Jump on carry = 0	2	2	50
JB bit,rel	Jump on direct bit = 1	3	2	20
JNB bit,rel	Jump on direct bit = 0	3	2	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	2	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	2	60
JNZ rel	Jump on accumulator ≠0	2	2	70
CJNE A,dir,rel	Compare A,direct jne relative	3	2	B5
CJNE A,#d,rel	Compare A,immediate jne relative	3	2	B4
CJNE Rn,#d,rel	Compare register, immediate jne relative	3	2	B8-BF
CJNE @Ri,#d,rel	Compare indirect, immediate jne relative	3	2	B6-B7
DJNZ Rn,rel	Decrement register, jnz relative	2	2	D8-DF
DJNZ dir,rel	Decrement direct byte, jnz relative	3	2	D5

MISCELLANEOUS				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
NOP	No operation	1	1	00

ADDITIONAL INSTRUCTIONS (selected through EO[7:4])				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOVC @(DPTR++),A	M8051W/M8051EW-specific instruction supporting software download into program memory	1	2	A5
TRAP	Software break command	1	1	A5

In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11→F1 (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the destination address.

The CJNE instructions use the abbreviation #d for immediate data; other instructions use #data.

B. Instructions on how to use the input port

- Error occur status
  - Using compare jump instructions with input port, it could cause error due to the timing conflict inside the MCU.
  - Compare jump Instructions which cause potential error used with input port condition:

```
JB      bit, rel     ; jump on direct bit=1
JNB     bit, rel     ; jump on direct bit=0
JBC     bit, rel     ; jump on direct bit=1 and clear
CJNE    A, dir, rel  ; compare A, direct jne relative
DJNZ    dir, rel     ; decrement direct byte, jnz relative
```

  - It is only related with Input port. Internal parameters, SFRs and output bit ports don't cause any error by using compare jump instructions.
  - If input signal is fixed, there is no error in using compare jump instructions.

- Error status example

```
while(1){
    if (P00==1){ P10=1; }
    else { P10=0; }
    P11^=1;
}
```

```
zzz:    JNB     080.0, xxx  ; it possible to be error
        SETB    088.0
        SJMP    yyy
xxx:    CLR     088.0
yyy:    MOV     C,088.1
        CPL     C
        MOV     088.1,C
        SJMP    zzz
```

```
unsigned char ret_bit_err(void)
{
    return !P00;
}
```

```
        MOV     R7, #000
        JB      080.0, xxx  ; it possible to be error
        MOV     R7, #001
xxx:    RET
```

- Preventative measures (2 cases)
  - Do not use input bit port for bit operation but for byte operation. Using byte operation instead of bit operation will not cause any error in using compare jump instructions for input port.

```
while(1){
  if ((P0&0x01)==0x01){ P10=1; }
  else { P10=0; }
    P11^=1;
}
```

```
zzz:    MOV     A, 080      ; read as byte
        JNB     0E0.0, xxx  ; compare
        SETB    088.0
        SJMP    yyy
xxx:    CLR     088.0
yyy:    MOV     C,088.1
        CPL     C
        MOV     088.1,C
        SJMP    zzz
```

```
bit tt;
while(1){
    tt=P00;
    if (tt==0){ P10=1;}
    else {  P10=0;}
    P11^=1;
}
```

```
zzz:    MOV     C,080.0   ; input port use internal parameter
        MOV     020.0, C      ; move
        JB      020.0, xxx    ; compare
        SETB    088.0
        SJMP    yyy
xxx:    CLR     088.0
yyy:    MOV     C,088.1
        CPL     C
        MOV     088.1,C
        SJMP    zzz
```

- If you use input bit port for compare jump instruction, you have to copy the input port as internal parameter or carry bit and then use compare jump instruction.

Table of contents