
JULY 05, 2012 Ver 0.3

4-BIT SINGLE CHIP MICROCOMPUTERS

ADAM45P52XX

USER`S MANUAL

- ADAM45P5216
- ADAM45P5216T
- ADAM45P5208
- ADAM45P5208T



0. Revision History

Version	Date	Description
VER 0.0	2010.02.16	- . 1'st Release.
VER 0.1	2010.04.22	- . correct some errata. (page-72)
VER 0.2	2012.05.02	- . Add the manual for the Development system. (page-88~91) - . Change the Operating Voltage Spec (page-2, 17) Ver 0.1 : ● 2.0 ~ 5.5 V @ 1MHz ~ 4MHz ● 2.7 ~ 5.5 V @ 8MHz ~ 16MHz Ver 0.2 : ● 2.0 ~ 5.5 V @ 1MHz ~ 4MHz ● 2.7 ~ 5.5 V @ 8MHz ● 4.5 ~ 5.5 V @ 16MHz
VER 0.3	2012.07.05	- . Change the Input Common Mode Voltage (VCM) Spec of Comparator (page-20) ● VCM(min.) : 0.10V → 0.05V

1. Overview

The ADAM45P5216/08 is the High Speed and Low Voltage operating 4-bit single chip microcomputer. This chip contains ADAM45 CPU, EPROM, RAM, Timer/PWM, Interrupt, Watch Dog Timer, 12-bit ADC, Two Analog Comparator, 8-bit DAC, Input/Output Ports and Oscillation Circuit.

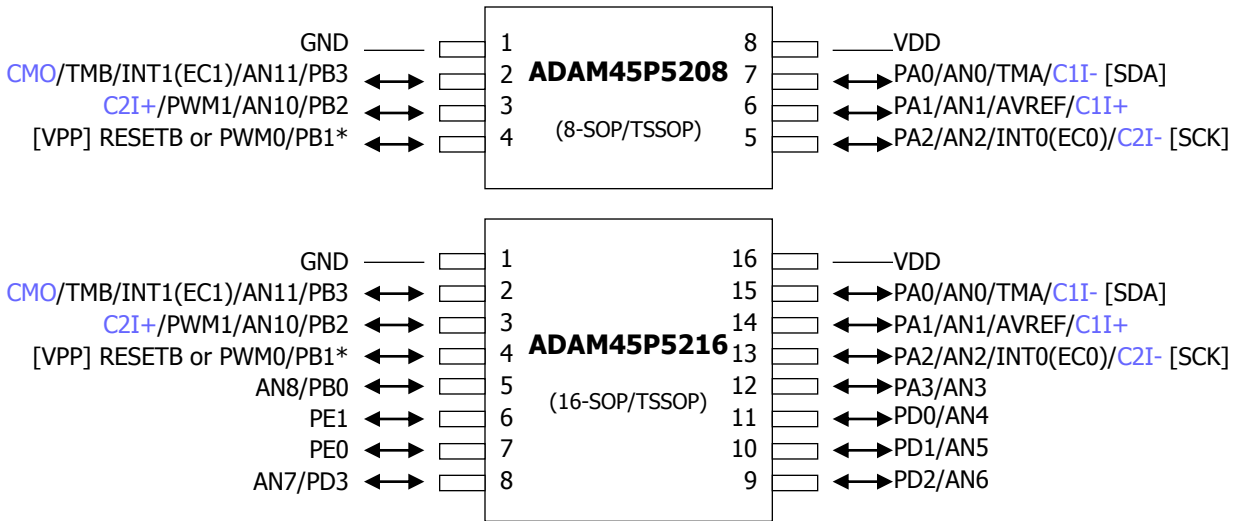
1.1. Features

- ◆ Instruction Execution Time
 - 500ns @ $f_{osc}=8\text{MHz}$
- ◆ Program Memory Area (MTP)
 - 8K Bytes (4,096 x 16bit)
 - Multi-programmable by 4K Bytes (2,048 x 16bit)
 - Multi-programmable by 2K Bytes (1,024 x 16bit)
- ◆ Data memory (RAM)
 - 256 nibble (256 x 4bit)
- ◆ 16-Bit Table read Instruction.
- ◆ A/D Converter
 - 12Bit x 11ch for ADAM45P5216
 - 12Bit x 5ch for ADAM45P5208
- ◆ Timer (Timer/Counter/Capture/PWM)
 - 12Bit x 1ch [PWM0 : (8+4)bit x 1ch]
 - 8Bit x 1ch [PWM1 : (6+2)bit x 1ch]
- ◆ Watch-Dog Timer
 - 19Bit x 1ch
- ◆ Oscillator Type
 - Calibrated Internal RCOSC only
: typ. 16/8/4/1MHz($\pm 2\%$) selectable
- ◆ Power On Reset
- ◆ Power Saving Operation Modes
 - STOP
 - SLEEP
- ◆ Interrupt Sources
 - External : 2ch (INT0, INT1)
 - Internal : 5ch (T0, T1, ADC, WDT, VDI)
- ◆ Low Voltage Detection Reset Circuit
- ◆ 3-level Voltage Detection Indicator (4.0V/3.0V/2.5V)
- ◆ Analog Comparator module with:
 - Two analog comparator with one ORed output
 - Programmable on-chip voltage reference with one 8-bit DAC
- ◆ Operating Voltage Range
 - 2.0 ~ 5.5 V @ 1MHz ~ 4MHz
 - 2.7 ~ 5.5 V @ 8MHz
 - 4.5 ~ 5.5 V @ 16MHz
- ◆ Operating Temperature Range
 - -40 ~ 85 °C
- ADAM45P52XX Device Summary

Series	ADAM45P5216	ADAM45P5208
Program memory	4,096 x 16	4,096 x 16
Data memory	256 x 4	256 x 4
I/O ports	14	6
Package	16-SOP/TSSOP	8-SOP/TSSOP

1. Overview

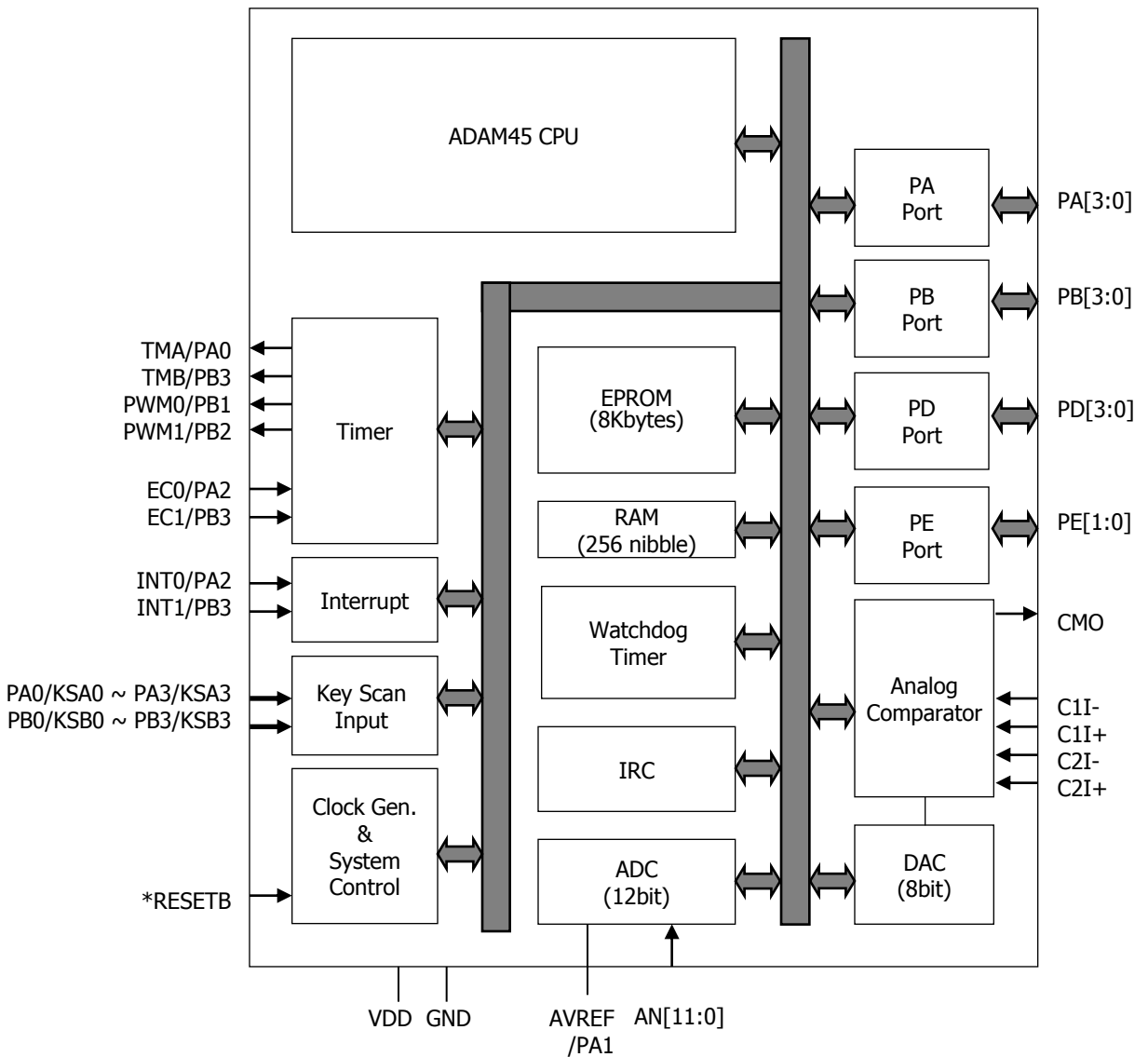
1.2. Pin Assignments



** RESETB is selected by setting the OTP Configuration Bit.*

1. Overview

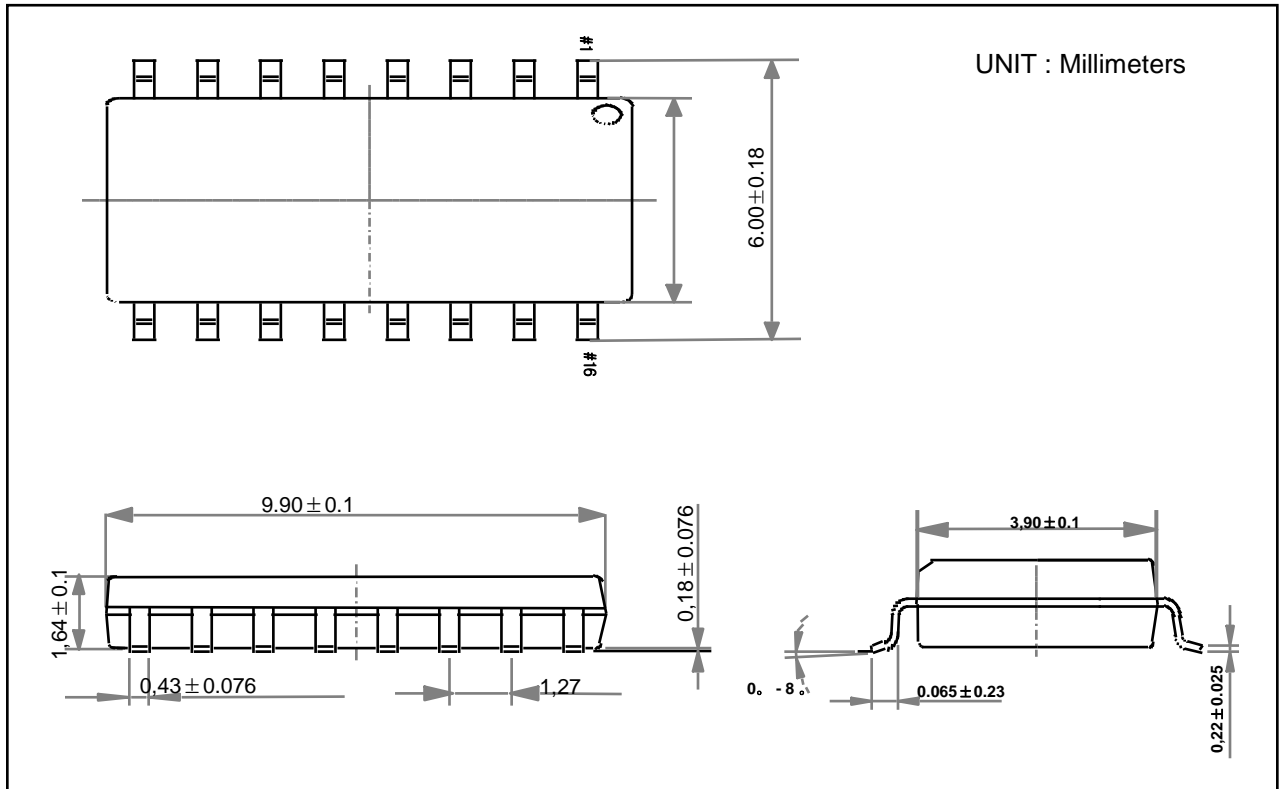
1.3. Block Diagram



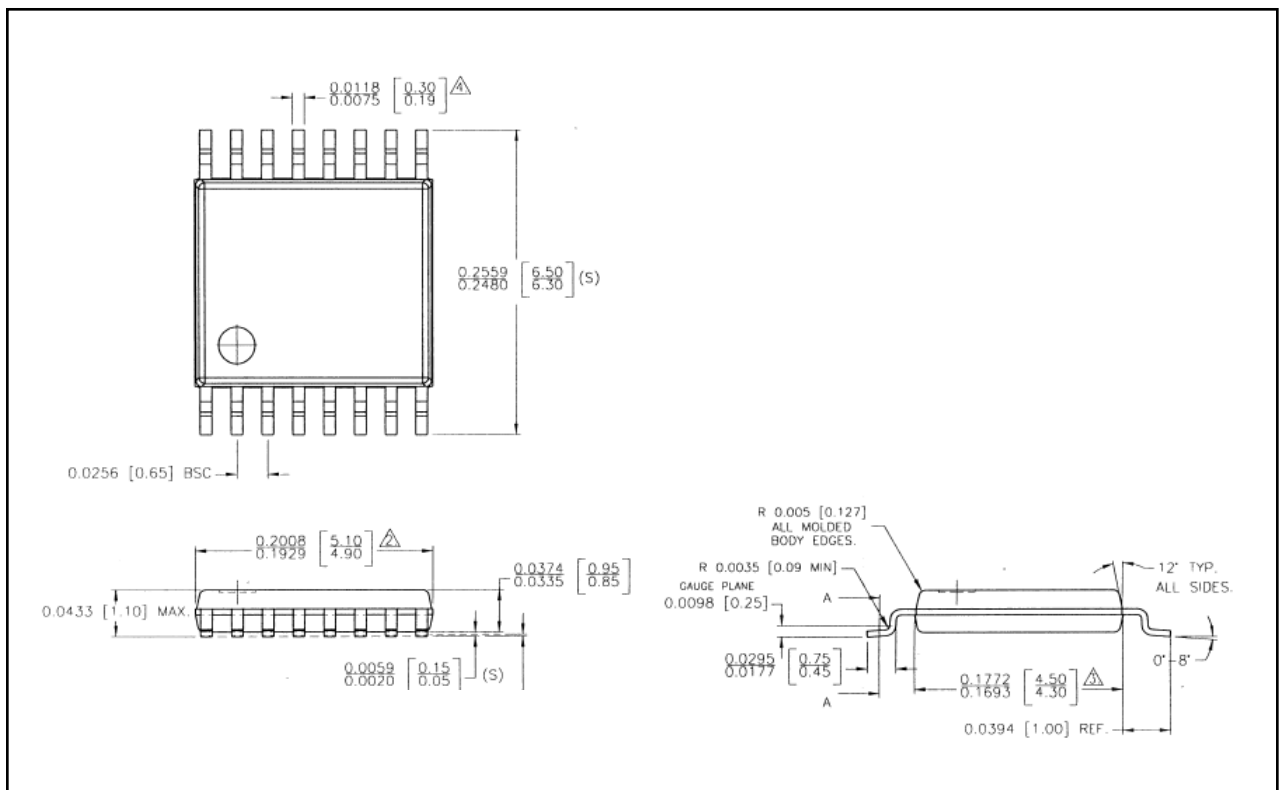
** RESETB is selected by setting the OTP Configuration Bit.*

1. Overview

1.4. Package Dimension



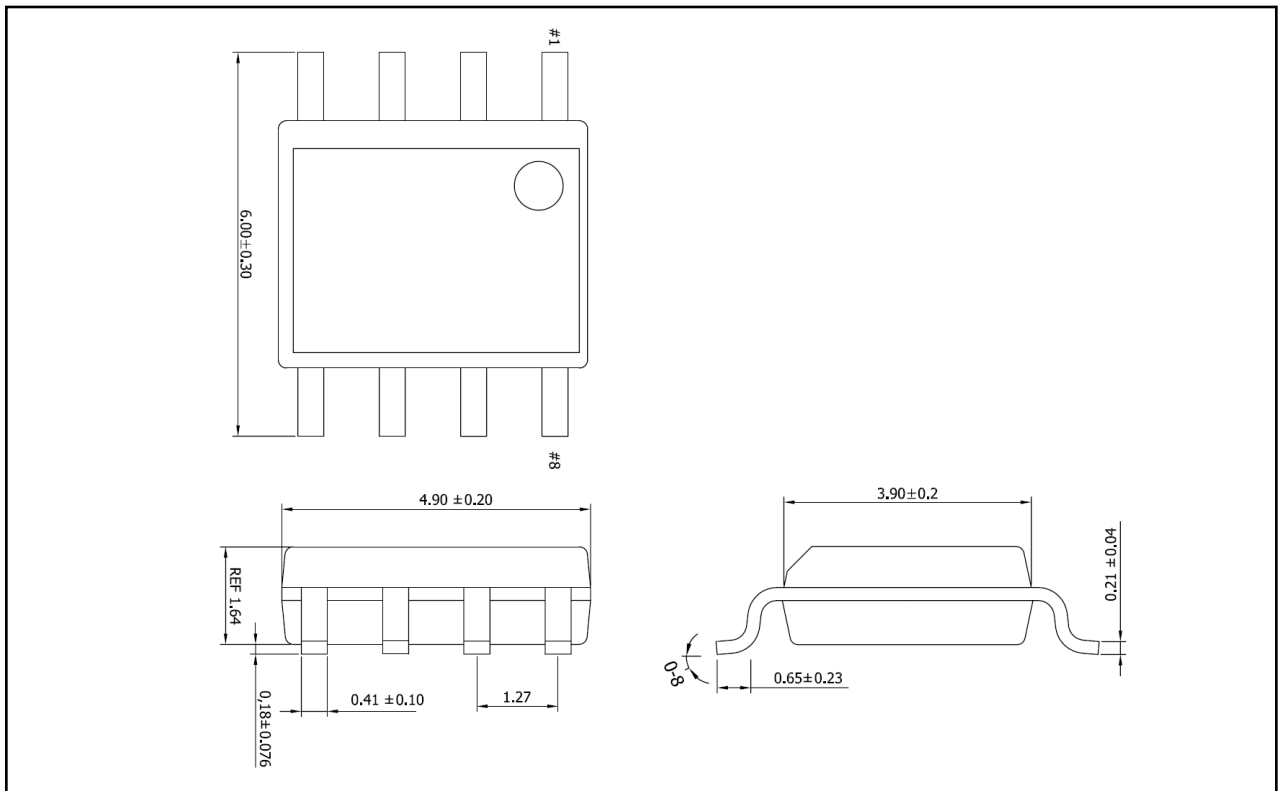
16 SOP (150Mil) Pin Dimension (dimensions in millimeters)



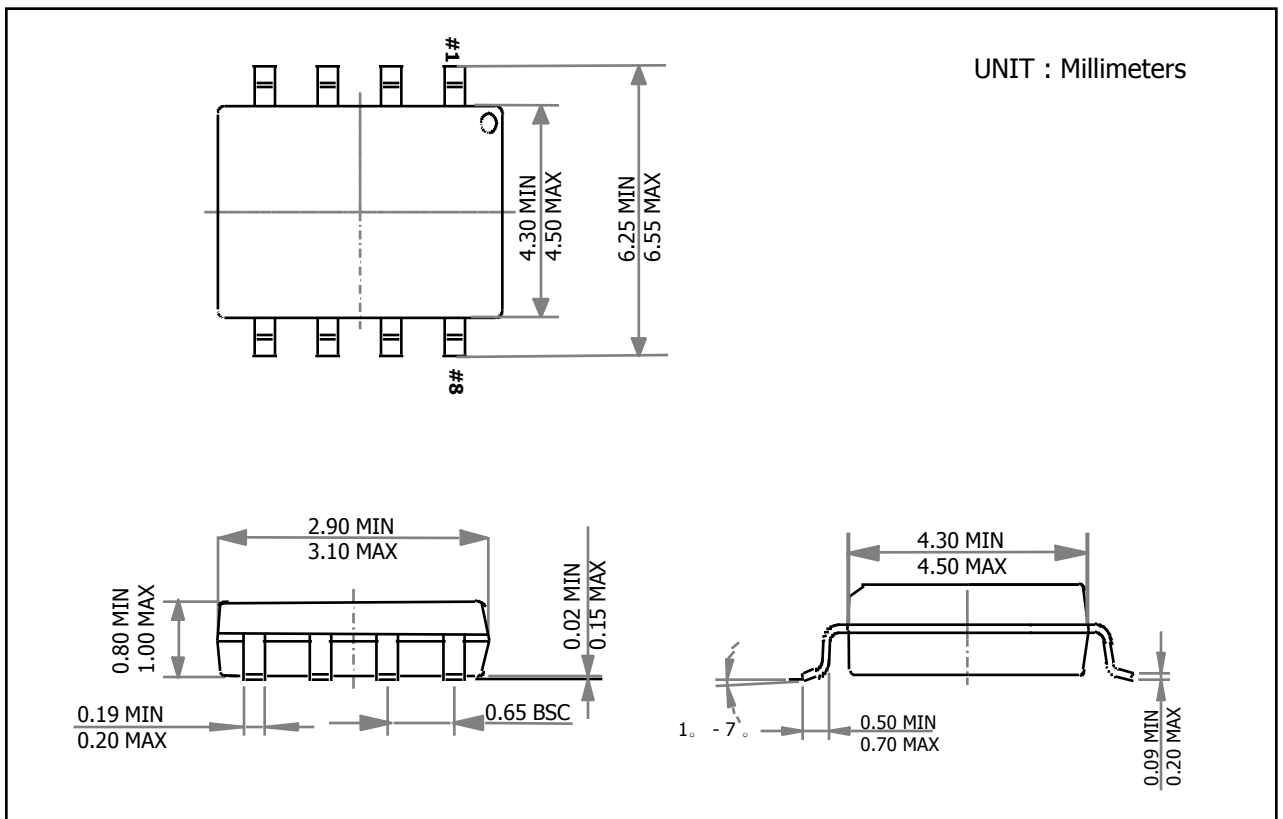
16 TSSOP (4.4 mm) Pin Dimension (dimensions in inch [millimeters])

1. Overview

1.4. Package Dimension



8 SOP (150mil) Pin Dimension (dimensions in millimeters)



8 TSSOP (4.4 mm) Pin Dimension (dimensions in inch [millimeters])

1. Overview

1.5. Pin Function

1.5.1. Port Pins

Pin Name	I/O	Function	@RESET	@STOP	Shared Pins
PA0	I/O	<ul style="list-style-type: none"> - 4-bit I/O Port. - CMOS input. - Push-pull output. - Each pin can be set and reset by Data register value. - Can be programmable as Pull-up/N-ch open drain/KSCN/AN/INT(EC)/TIMER output/AVREF/Comparator input individually. - Direct driving of LED (N-TR). 	C1I-	State of before STOP	C1I-/TMA/AN0/KSA0
PA1			C1I+		AVREF/C1I+/AN1/KSA1
PA2			C2I-		C2I-/INT0(EC0)/AN2/KSA2
PA3			Input (without Pull-up)		AN3/KSA3
PB0	I/O	<ul style="list-style-type: none"> - 4-bit I/O Port. - CMOS input. - Push-pull output. - Each pin can be set and reset by Data register value. - Can be programmable as Pull-up/N-ch open drain/KSCN/AN/INT(EC)/TIMER output/Comparator input /Comparator output individually. - Direct driving of LED (N-TR). - PB1 is N-ch Open drain output only at output mode. - PB2 and PB3 can be selected Pull-down individually. 	Input (without Pull-up)	State of before STOP	AN8/KSB0
PB1					RESETB/PWM0/KSB1
PB2			C2I+		C2I+/PWM1/AN10/KSB2
PB3			CMO		CMO/TMB/AN11/INT1(EC1)/KSB3
PD0	I/O	<ul style="list-style-type: none"> - 4-bit I/O Port. - CMOS input. - Push-pull output. - Each pin can be set and reset by Data register value. - Can be programmable as Pull-up/N-ch open drain /AN individually. - Direct driving of LED (N-TR). 	Input (without Pull-up)	State of before STOP	AN4
PD1					AN5
PD2					AN6
PD3					AN7
PE0	I/O	<ul style="list-style-type: none"> - 2-bit I/O Port. - CMOS input. - Push-pull output. - Each pin can be set and reset by Data register value. - Can be programmable as Pull-up/N-ch open drain individually. - Direct driving of LED (N-TR). 	Input (without Pull-up)	State of before STOP	-
PE1					-

1. Overview

1.5. Pin Function

1.5.2. Non-port Pins

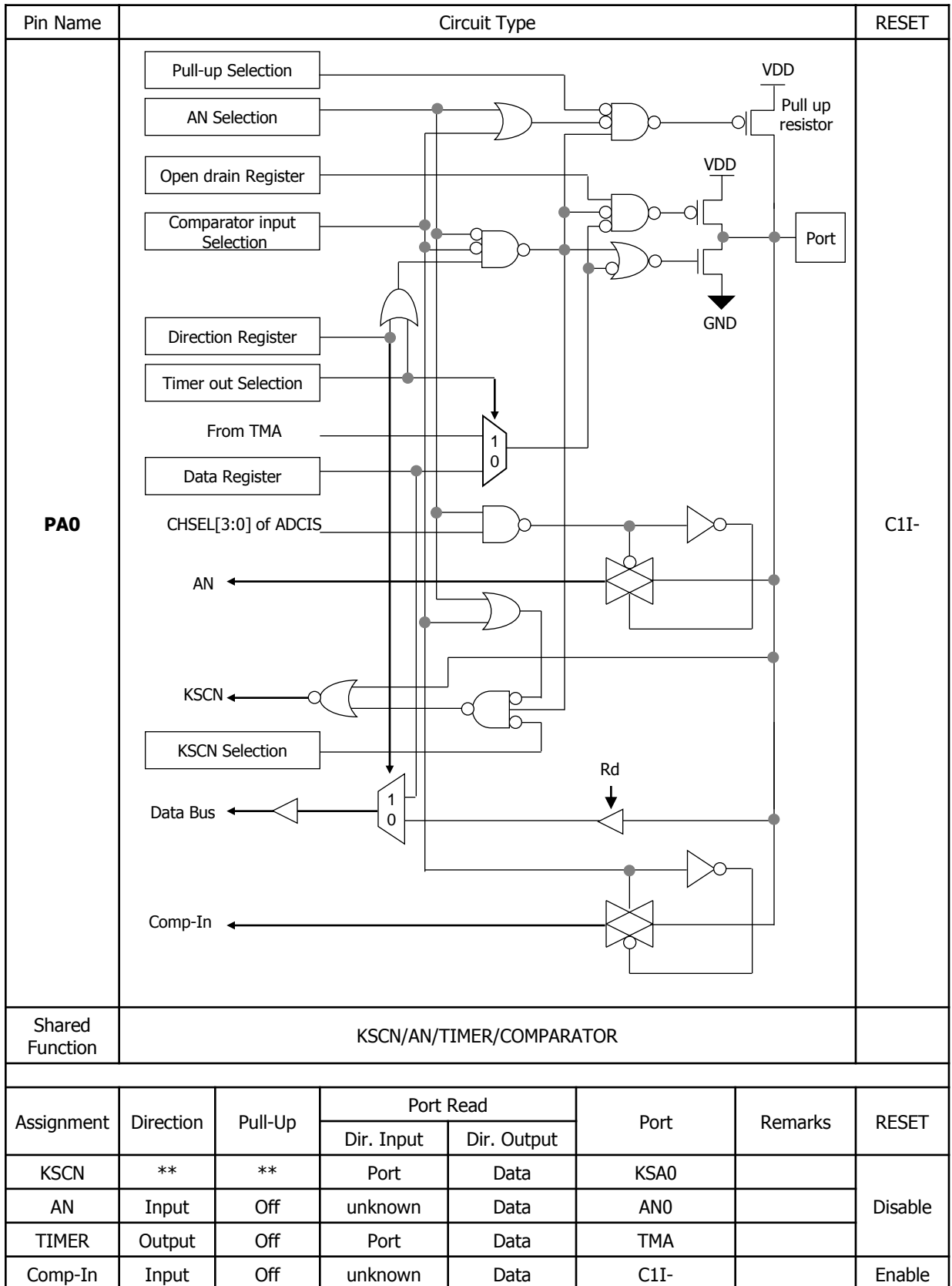
Pin Name	I/O	Function	@RESET	Shared Pins
INT0	I	- External Interrupt input for which the valid edges (rising edge, falling edge, both rising and falling edge) can be specified. - Timer0, Timer1 capture input.	Input (Pull-up off)	PA2
INT1				PB3
EC0	I	- Timer0, Timer1 event counter input.	Input (Pull-up off)	PA2
EC1				PB3
TMA	O	- Timer0, Timer1 logic output.	Input (Pull-up off)	PA0
TMB				PB3
PWM0	O	- Timer0 output.	Input (Pull-up off)	PB1/RESETB
PWM1	O	- Timer1 output.	Input (Pull-up off)	PB2
KSA0 ~ KSA3	I	- STOP mode release input which can be selected individually by user program. - It is released by "L" input at STOP mode.	Input (Pull-up off)	PA0 ~ PA3
KSB0 ~ KSB3				PB0 ~ PB3
AN0 ~ AN3	I	- Analog input for A/D Converter. - Each port's pull-up resistor is disabled at A/D input mode.	Input (Pull-up off)	PA0 ~ PA3
AN4 ~ AN7				PD0 ~ PD3
AN8				PB0
AN10~AN11				PB2 ~ PB3
C1I-	I	- Analog Comparator-1 negative input	Input (C1I-)	PA0
C1I+	I	- Analog Comparator-1 positive input	Input (C1I+)	PA1
C2I-	I	- Analog Comparator-2 negative input	Input (C2I-)	PA2
C2I+	I	- Analog Comparator-2 positive input	Input (C2I+)	PB2
CMO	O	- Analog Comparator-1, Comparator-2 Logic output	Output (CMO)	PB3
AVREF	P	- Analog power for A/D converter.	Input (Pull-up off)	PA1
RESETB	I	- External RESETB Input by Code/Register Option.	Input (Pull-up off)	PB1
VDD	P	- Positive power supply.	-	-
GND	P	- Ground.	-	-

1.5.3. OTP Programming Pin Description (OTP Program Mode)

Pin No.		Pin Name	I/O	Function	Shared Pins
8Pin	16Pin				
#8	#16	VDD	P	- Programming Power supply (+ 5.0V)	VDD
#1	#1	GND	P	- Ground	GND
#4	#4	VPP	P	- Programming high voltage Power supply (+ 11.5V)	RESETB/PB1/PWM0
#5	#13	SCK	I	- Programming Clock input pin	PA2/AN2/INT0(EC0)/CI2-
#7	#15	SDA	I/O	- Programming Data Input/Output pin	PA0/AN0/TMA/C1I-

1. Overview

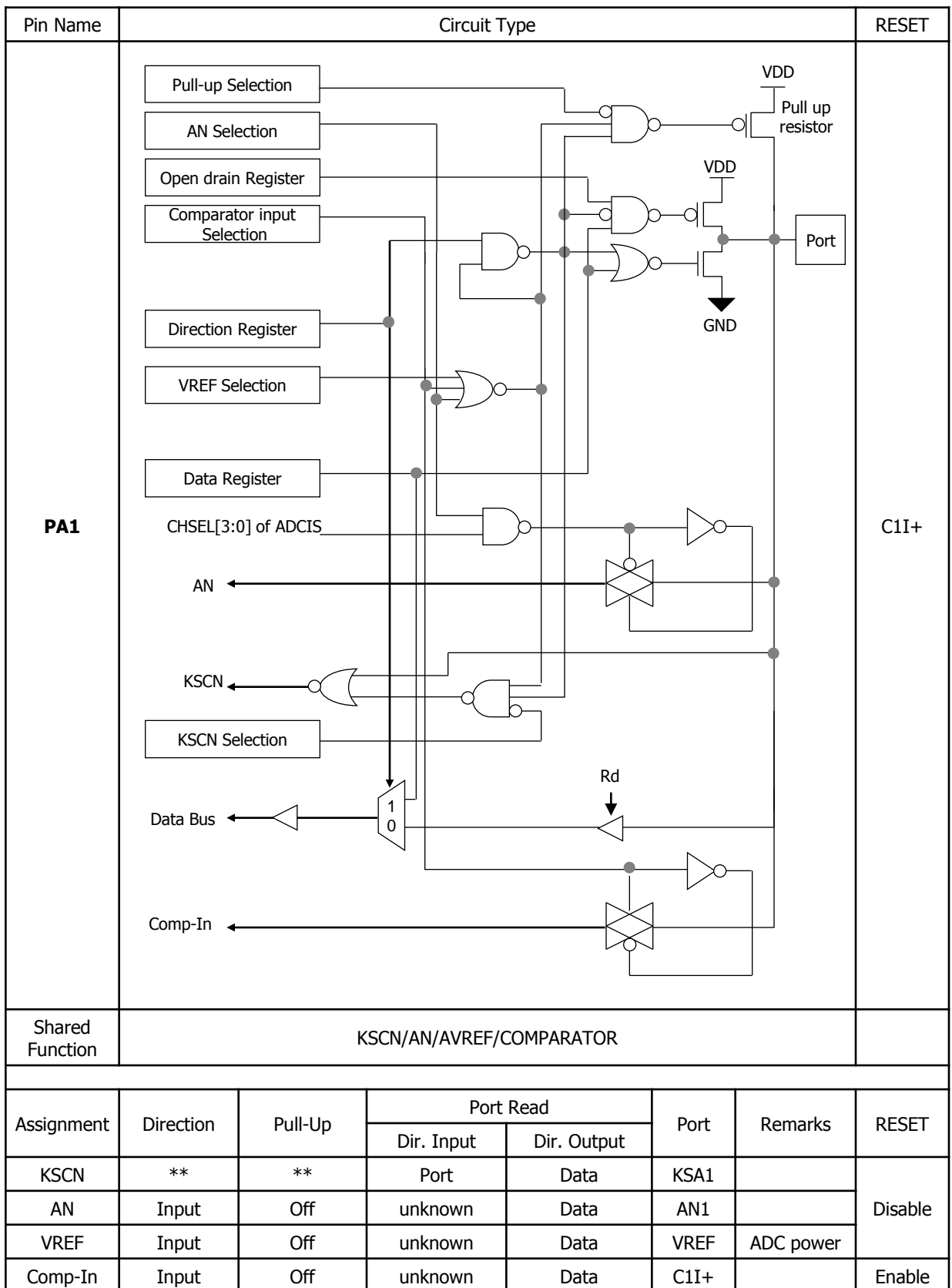
1.6. Port Structure



** : It is depend on user definition.

1. Overview

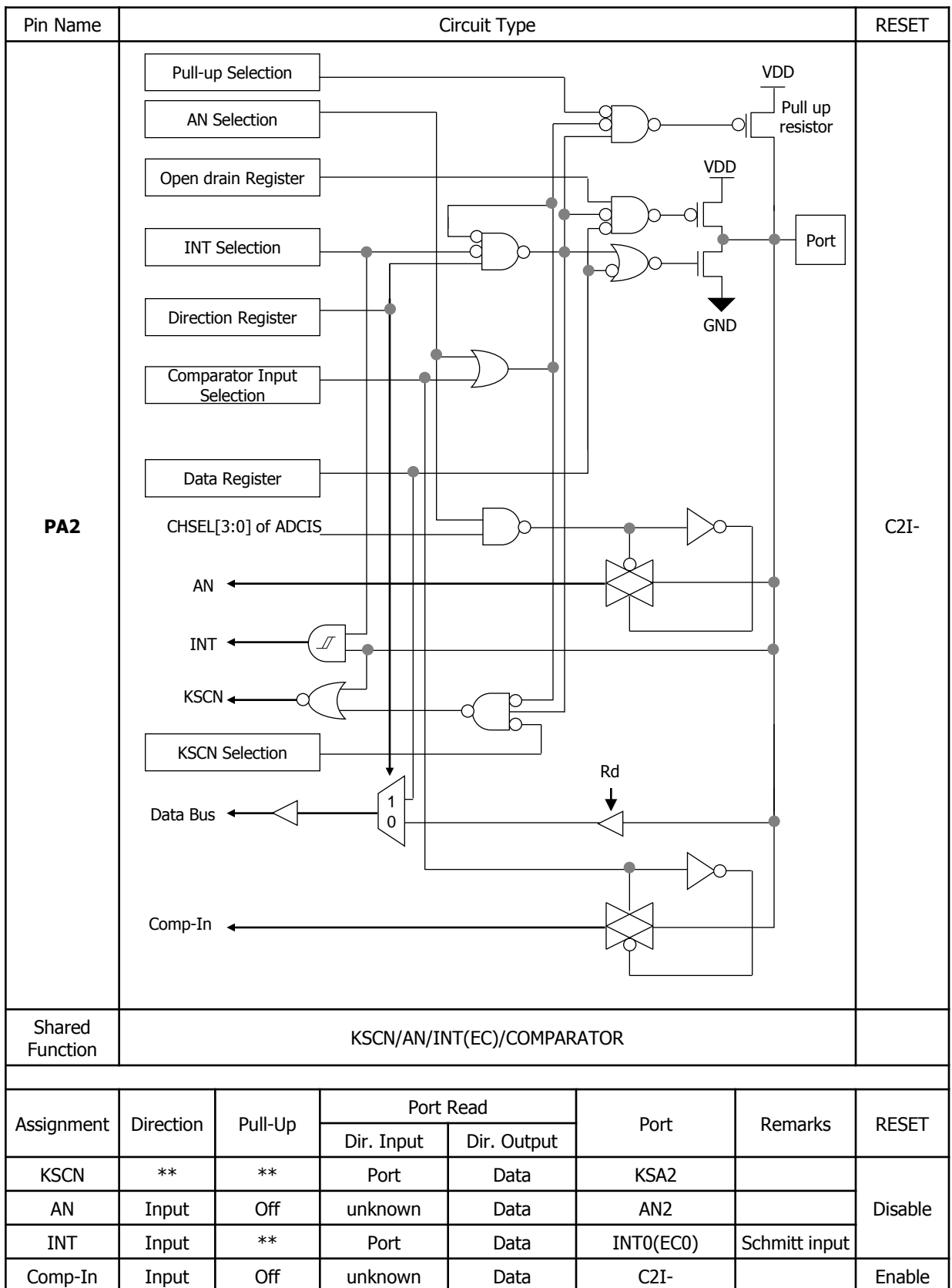
1.6. Port Structure



** : It is depend on user definition.

1. Overview

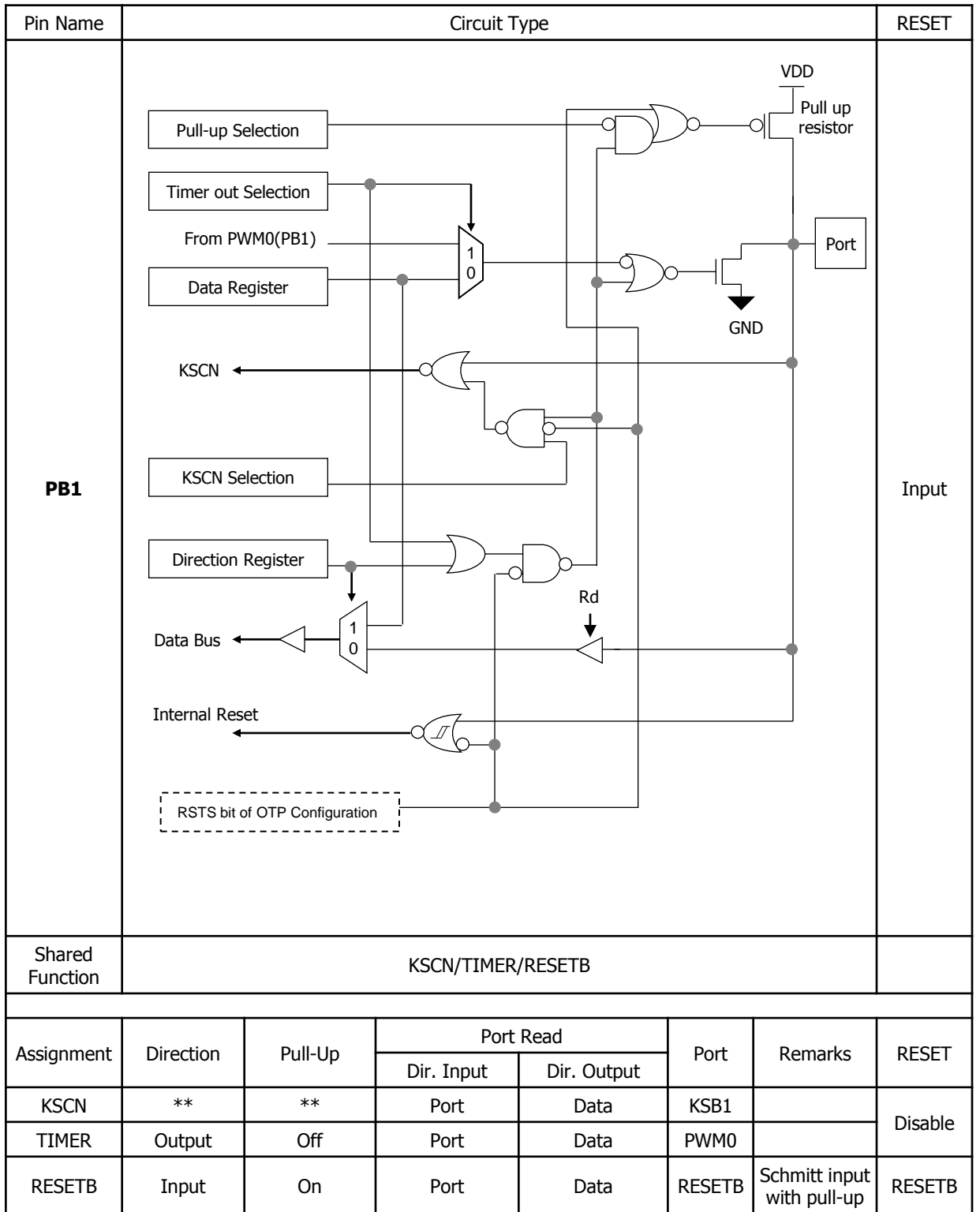
1.6. Port Structure



** : It is depend on user definition.

1. Overview

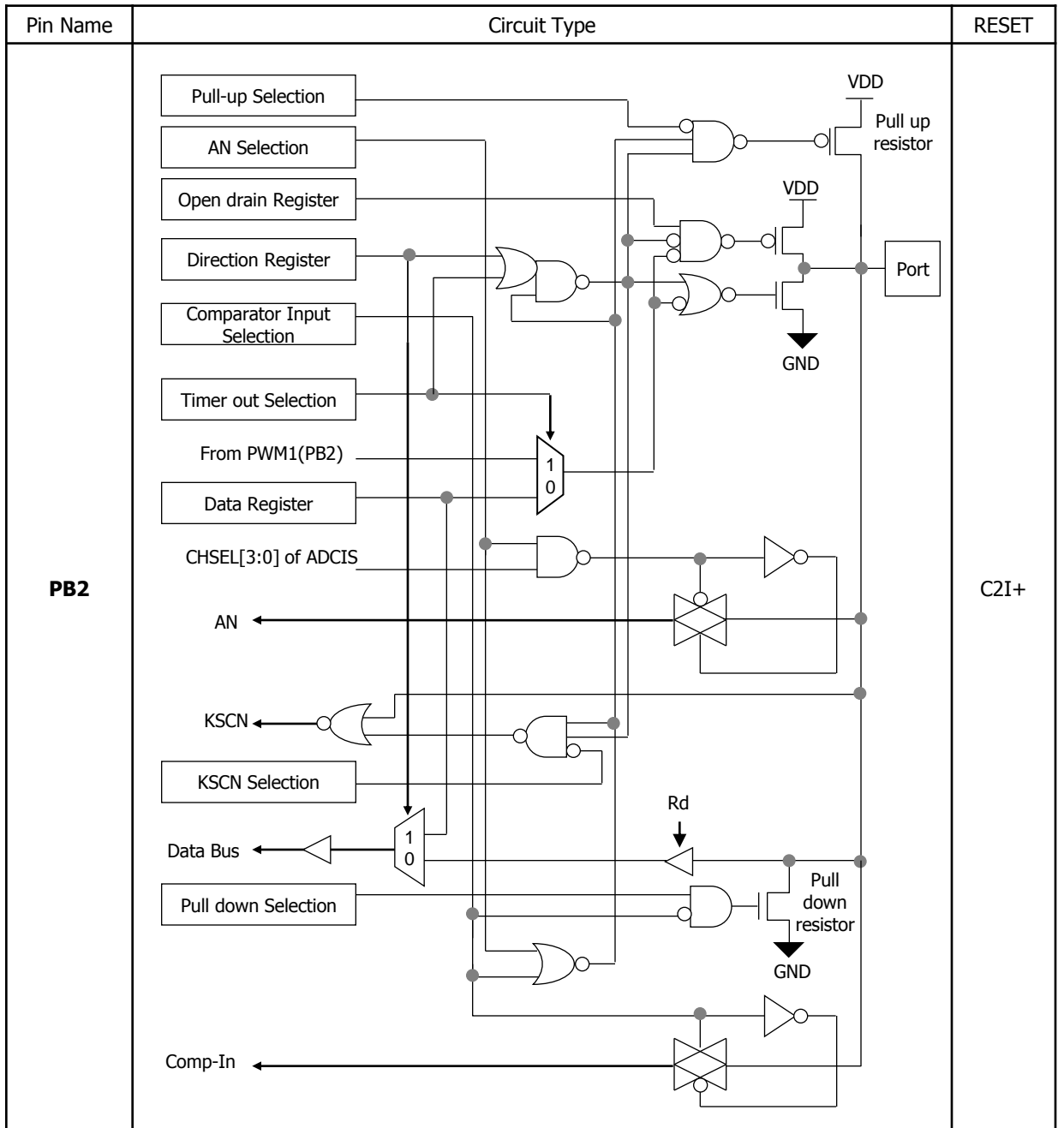
1.6. Port Structure



** : It is depend on user definition.

1. Overview

1.6. Port Structure



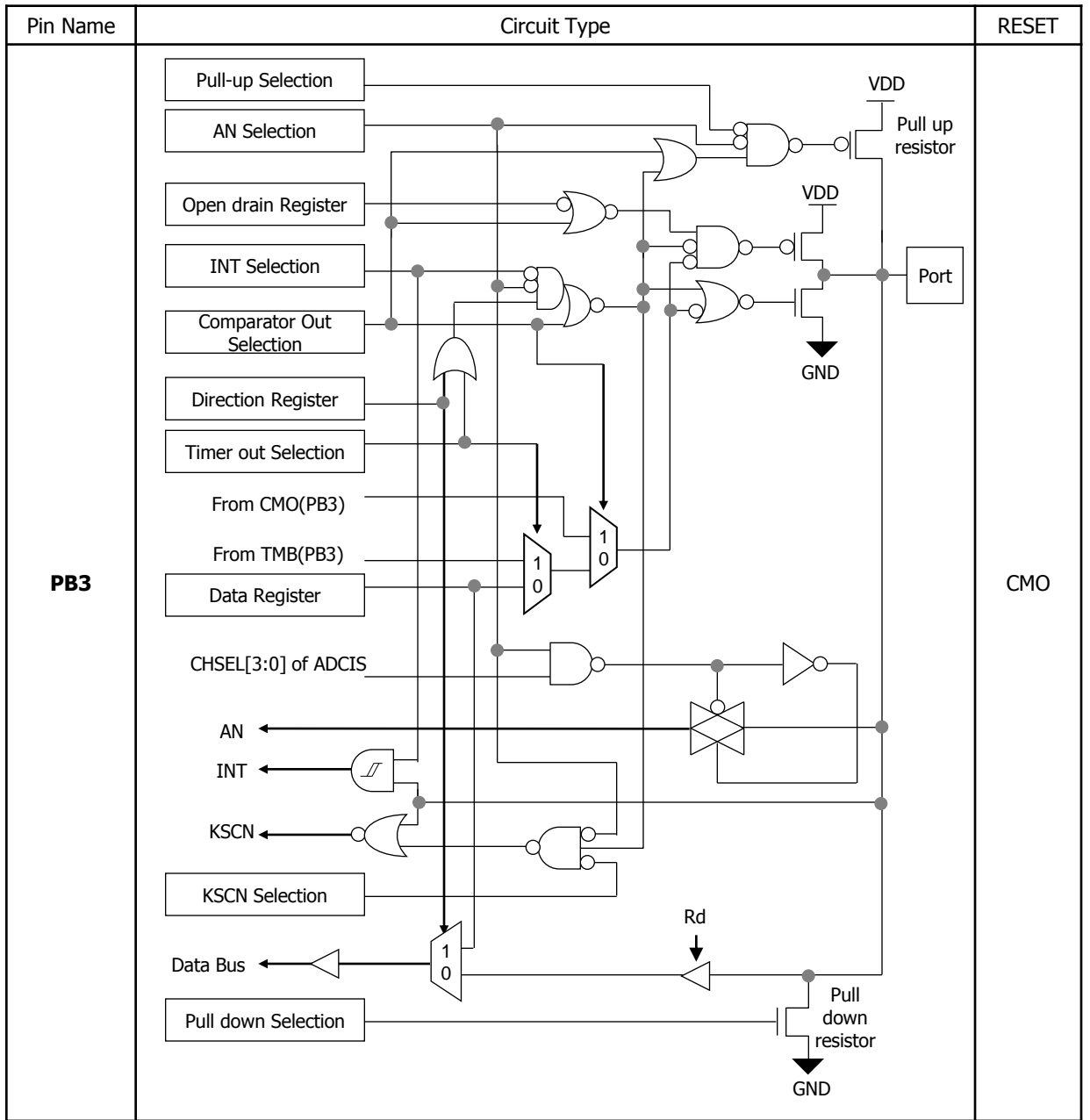
Shared Function	KSCN/AN/TIMER/Pull-Down/COMPARATOR						RESET
-----------------	------------------------------------	--	--	--	--	--	-------

Assignment	Direction	Pull-Up	Pull-Down	Port Read		Port	Remarks	RESET
				Dir. Input	Dir. Output			
KSCN	**	**	**	Port	Data	KSB2	Disable	
AN	Input	Off	**	unknown	Data	AN10		
TIMER	Output	Off	**	Port	Data	PWM1		
Pull-Down	**	**	On	Port	Data	**		
Comp-In	Input	Off	Off	unknown	Data	C2I+		Enable

** : It is depend on user definition.

1. Overview

1.6. Port Structure



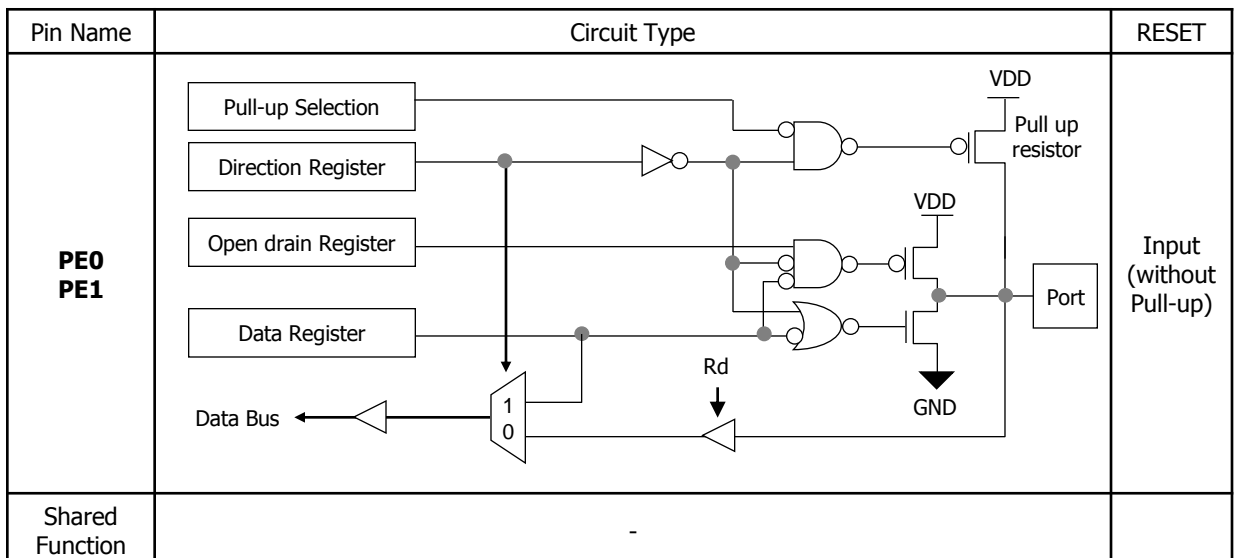
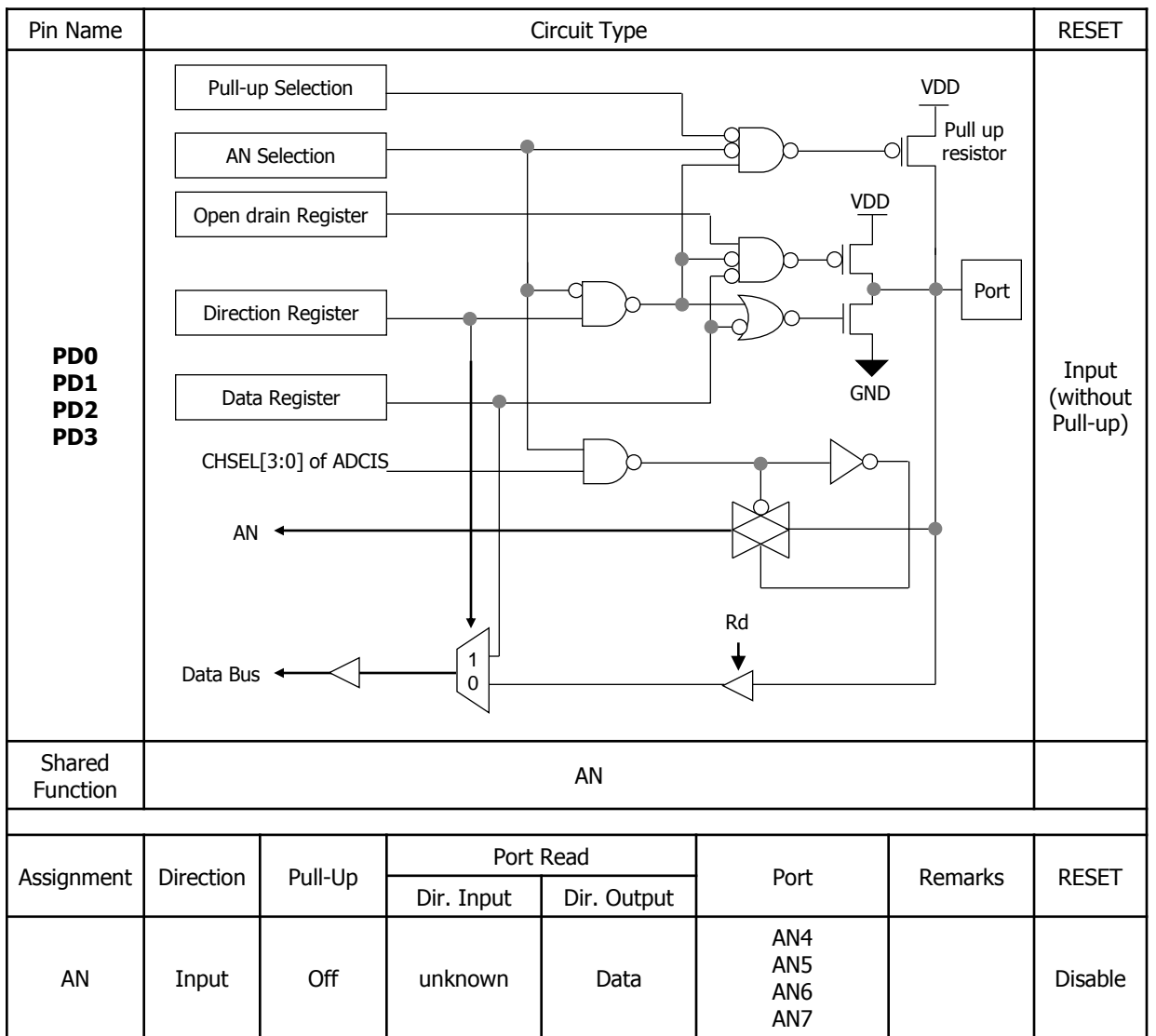
Shared Function	KSCN/AN/INT(EC)/TIMER/Pull-Down/COMPARATOR						RESET
-----------------	--	--	--	--	--	--	-------

Assignment	Direction	Pull-Up	Pull -Down	Port Read		Port	Remarks	RESET
				Dir. Input	Dir. Output			
KSCN	**	**	**	Port	Data	KSB3		Disable
AN	Input	Off	Off	unknown	Data	AN11		
INT	Input	**	**	Port	Data	INT1(EC1)	Schmitt Input	
TIMER	Output	Off	Off	Port	Data	TMB		
Pull-Down	**	**	On	Port	Data	**	Pull-down	
Comp-Out	Output	**	**	unknown	Data	CMO		Enable

** : It is depend on user definition.

1. Overview

1.6. Port Structure



1. Overview

1.7. Electrical Characteristics

1.7.1. Absolute Maximum Ratings (Ta = 25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V _{DD}	-0.3 ~ +6.0	V
Input Voltage	V _I	-0.3 ~ VDD + 0.3	V
Output Voltage	V _O	-0.3 ~ VDD + 0.3	V
Storage Temperature	T _{STG}	-65 ~ 150	°C
Power Dissipation	P _D	700	mW

1.7.2. Recommended Operating Ranges

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD	f _{OSC} = 4MHz	2.0	-	5.5	V
		f _{OSC} = 8MHz	2.7	-	5.5	V
		f _{OSC} = 16MHz	4.5	-	5.5	V
Oscillation Frequency	f _{OSC}	Calibrated Internal RC Oscillator (VDD=2.0 ~ 5.5V) (Temp=-20 ~ 70°C)	15.68	16	16.32	MHz
			7.84	8	8.16	
			3.92	4	4.08	
			0.98 (-2%)	1	1.02 (+2%)	
		Calibrated Internal RC Oscillator (VDD=2.0 ~ 5.5V) (Temp=-40 ~ 85°C)	15.52	16	16.48	MHz
			7.76	8	8.24	
			3.88	4	4.12	
			0.97 (-3%)	1	1.03 (+3%)	
Operating Temperature	T _{OPR}		-40		85	°C

1. Overview

1.7.3. DC Characteristics (Ta = 25 °C)

PARAMETER	Symbol	Condition			Specification			UNIT
					MIN.	TYP.	MAX.	
High level input voltage	V _{IH1}	RESETB, INT0/EC0, INT1/EC1			0.8VDD		VDD	V
	V _{IH2}	PA, PB, PD, PE			0.7VDD		VDD	V
Low level input voltage	V _{IL1}	RESETB, INT0/EC0, INT1/EC1			0		0.2VDD	V
	V _{IL2}	PA, PB, PD, PE			0		0.3VDD	V
High level input leakage current	I _{IH}	PA, PB, PD, PE		V _{IH} = VDD			1	uA
Low level input leakage current	I _{IL}	PA, PB, PD, PE		V _{IL} = 0V			-1	uA
High level output voltage	V _{OH1}	PA, PB, PD, PE (Except PB1)	VDD = 5V	I _{OH} = -10mA	VDD-1.0			V
	V _{OH2}	PB2, PB3 (Reg. selectable)	VDD = 5V	I _{OH} = -15mA	VDD-1.0			V
	V _{OH3}	PB2, PB3 (Reg. selectable)	VDD = 5V	I _{OH} = -2mA	VDD-1.0			V
Low level output voltage	V _{OL1}	PA, PB, PD, PE	VDD = 5V	I _{OL} = 15mA			1.0	V
	V _{OL2}	PB2, PB3 (Reg. selectable)	VDD = 5V	I _{OL} = 25mA			1.0	V
	V _{OL3}	PB2, PB3 (Reg. selectable)	VDD = 5V	I _{OL} = 5mA			1.0	V
High level output leakage current	I _{OHL}	PA, PB, PD, PE		V _{OH} = VDD			1	uA
Low level output leakage current	I _{OLL}	PA, PB, PD, PE		V _{OL} = 0V			-1	uA
Input Pull-up current	I _{PU}	PA, PB, PD, PE	VDD = 5V		-25	-50	-100	uA
Input Pull-down current	I _{PD}	PB2, PB3	VDD = 5V		25	50	100	uA
Power supply current	I _{DD}	Operating current	VDD = 5V	f _{XIN} = 16MHz		2	3	mA
			VDD = 5V	f _{XIN} = 4MHz		1	1.5	mA
	I _{SLEEP}	Sleep mode current	VDD = 5V	f _{XIN} = 16MHz			1	mA
			VDD = 5V	f _{XIN} = 4MHz			0.5	mA
	I _{STOP}	Stop mode current (Oscillator Stop)	VDD = 5V	LVD On		2	5	uA
			VDD = 5V	LVD Off		-	1	uA
RAM retention supply voltage	V _{RET}				0.7			V

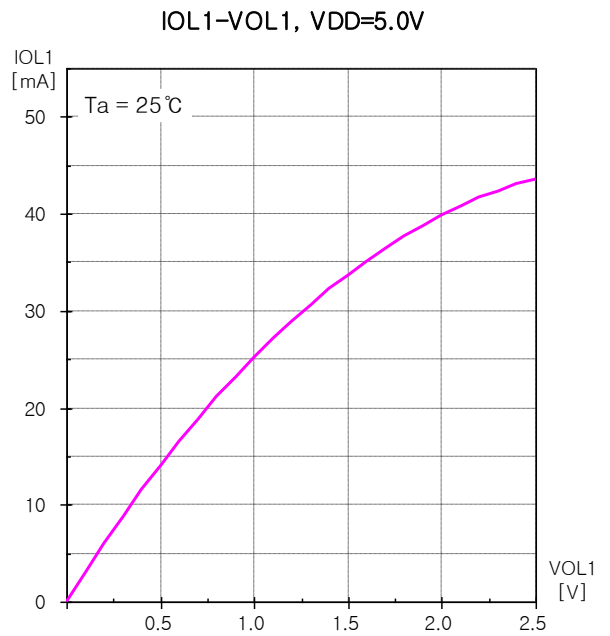
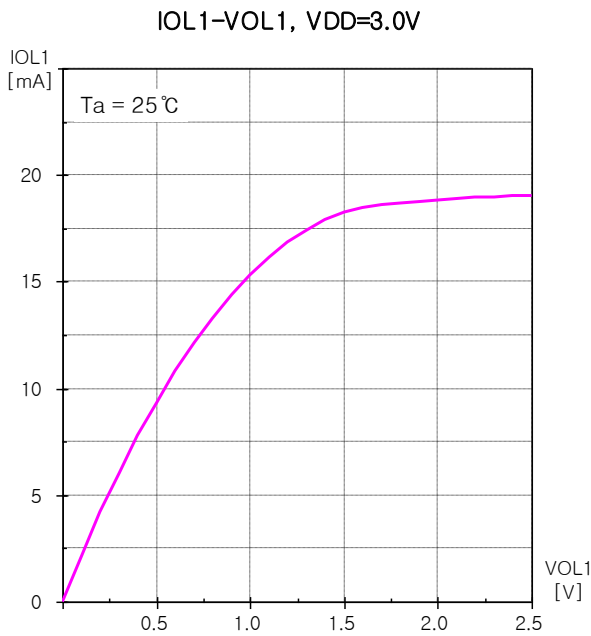
1. Overview

※ Typical Characteristics

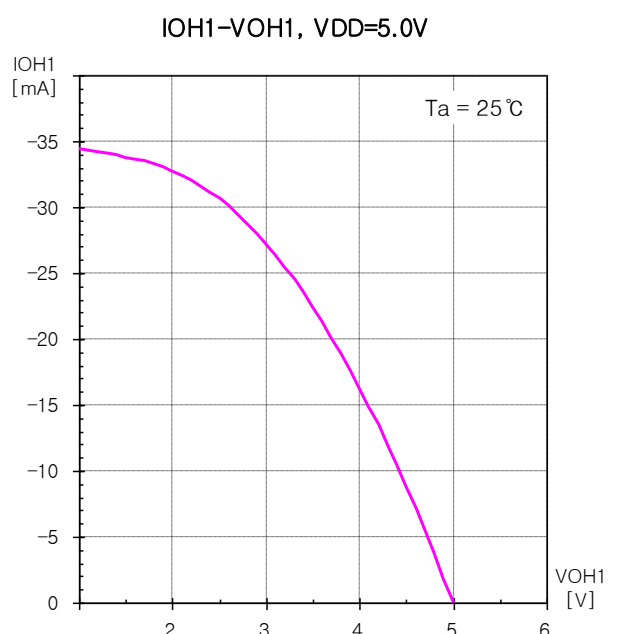
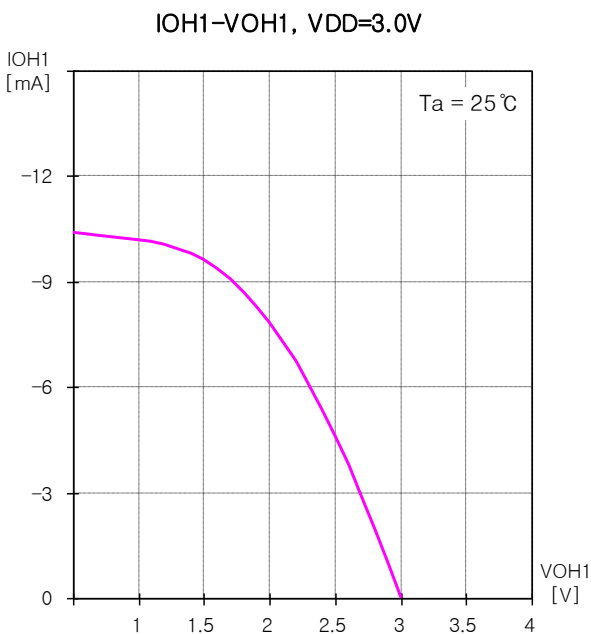
This graphs provided in this section are for design guidance only and are not tested or guaranteed.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

► IOL1 vs. VOL1 (at T=25°C)



► IOH1 vs. VOH1 (at T=25°C)



1. Overview

1.7.4. 12Bit A/D Conversion Characteristics (VDD=5.5 ~ 2.7V, Ta=25°C)

Parameter	Symbol	Condition	Specification			Unit
			MIN	TYP	MAX	
Resolution	RADC			12		Bits
Analog Input Voltage Range	VAIN	AVREFS = 0	VSS	-	VDD	V
		AVREFS = 1	VSS	-	AVREF	V
Analog Input Power Supply Voltage Range	AVREF	VDD = 5.0V	2.4	-	VDD	V
		VDD = 3.0V	2.4	-	VDD	V
Overall Accuracy	EACC	VDD=4.096V f _{XIN} = 4MHz	-	-	±4.0	LSB
Non-Linearity Error	ENE		-	-	±4.0	LSB
Differential Non-Linearity Error	EDE		-	±1.0	±2.0	LSB
Zero Offset Error	EOFF		-	±1.0	±3.0	LSB
Full Scale Error	EFE		-	±1.0	±3.0	LSB
Conversion Time	TCONV		VDD = 5.5V ~ 2.7V	29	-	-
AVREF Input Current	IREF	AVREFS = 1	-	0.8	2.0	mA

1.7.5. Analog Comparator Characteristics (VDD=5.5 ~ 2.7V, Ta=25°C)

Parameter	Symbol	Condition	Specification			Unit
			MIN	TYP	MAX	
Input Voltage Offset	VOS		- 5	-	+ 5	mV
Input Common Mode Voltage	VCM		0.05		VDD-0.1	V
Response Time	TRP*			250	400	ns
Comparator Mode Change to Output Valid	TCMCOV				10	us

*) TRP is measured with one input at ± 5mV, 1MHz triangular waveform while the other input at VDD/2.

1.7.6. 8–Bit DAC Characteristics (VDD=5.5 ~ 2.7V, Ta=25°C)

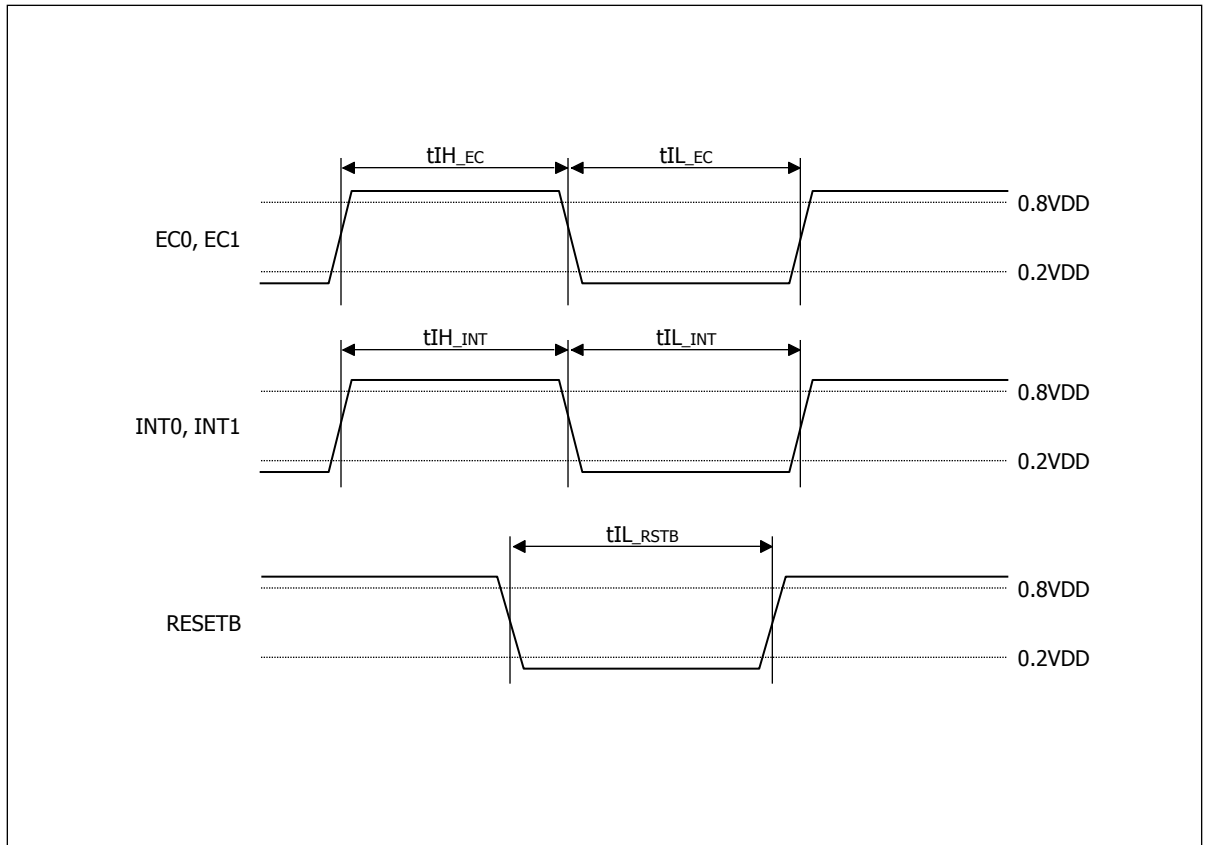
Parameter	Symbol	Condition	Specification			Unit
			MIN	TYP	MAX	
Resolution	RDAC			8		bits
Integral Linearity Error	INL	f _{XIN} =4MHz	-1		+1	LSB
Differential Linearity Error	DNL		-1		+1	LSB
Settling Time	TSET				20	us

1. Overview

1.7.7. AC Characteristics (Ta = 25°C)

Parameter	Symbol	Pin	Specification			Unit
			min.	typ.	max.	
Internal clock cycle time	tCP	–	62.5	250	1000	ns
System clock cycle time	tSYS	–		4		tCP
External pulse width High	tIH_EC	EC0, EC1	1			tCP
External pulse width Low	tIL_EC	EC0, EC1	1			tCP
RESETB pulse width Low	tIL_RSTB	RESETB	8			tSYS
Interrupt pulse width High	tIH_INT	INT0, INT1	2			tSYS
Interrupt pulse width Low	tIL_INT	INT0, INT1	2			tSYS

Minimum pulse width



2. Function Description

2.1. Program Memory

The ADAM45P52XX can address maximum 8Kbytes (4K words × 16bits) for program memory. Program counter PC (A0~A11) is used to address the whole area of program memory having an instruction (16bits) to be next executed.

The program memory consists of 4K words.

The program memory is composed as shown below.

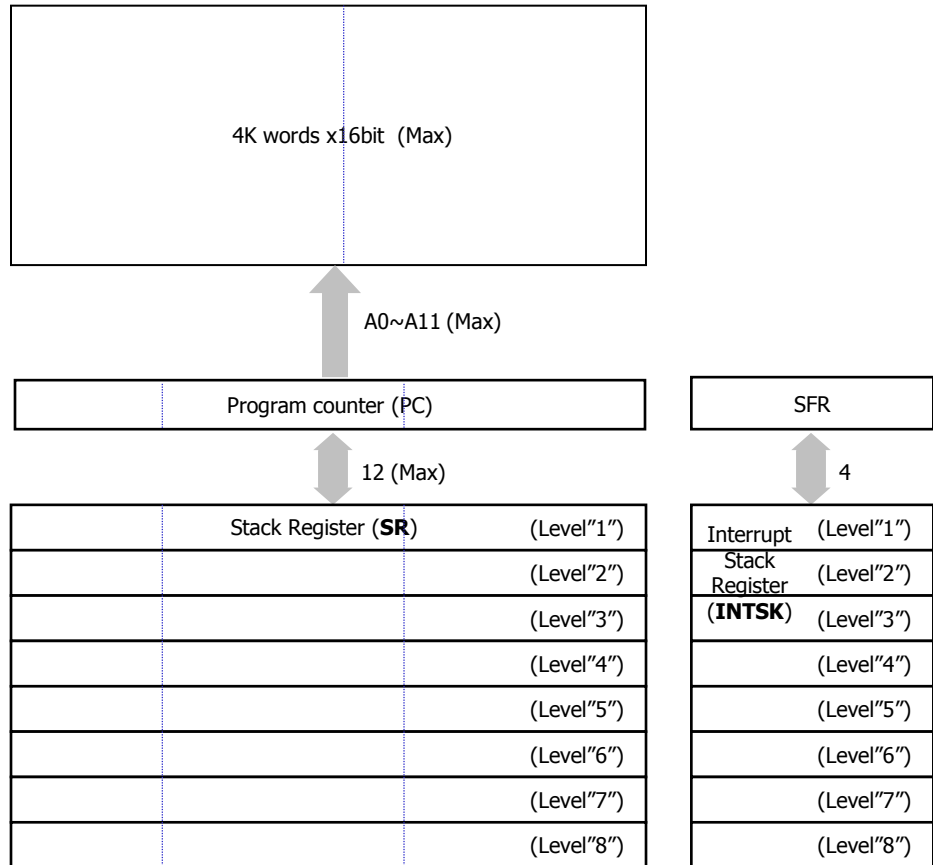


Fig.2.1 Configuration of Program Memory

2. Function Description

2.2. Address Register

The following registers are used to address the ROM.

- **Program counter (PC) :**
Available for addressing word on each page.
- **Stack register (SR) :**
Stores returned-word address in the subroutine call mode.

2.2.1 Program counter :

This 12-bit binary counter increments for fetching a word to be addressed in the currently addressed page having an instruction to be next executed.

For easier programming, at turning on the power, the program counter is reset to the zero location(0000H). Then the program counter specifies the next address.

When BR, CAL or RET instructions are decoded, the switches on each step are turned off not to update the address. Then, for BR or CAL, address data are taken in from the instruction operands (A0 to A11), or for RET, and address including page address is fetched from stack register No. 1.

2.2.2. Stack register (SR)

The address stack register (ADS) stores a return address when the subroutine call instruction is executed or interrupt is acknowledged.

If subroutine or interrupts are nested to more than 8 levels, internal reset is occurred.

The interrupt stack register(INTSK) saves the contents of Status Flag Register (SFR) when an interrupt is acknowledged.

The saved contents are restored when an interrupt return(RETI) instruction is executed. INTSK saves data each time an interrupt is acknowledged.

The programmer must keep in mind that the level of INTSK is 8. So, if more over 8 levels of interrupt occur, the first stored data is lost. There is different result between Stack overflow and interrupt stack overflow.

When clearing SP (Stack Pointer) with using "SPC" instruction, interrupt processing must be inhibited before "SPC".

2. Function Description

2.3. Data Memory (RAM)

256 nibbles (256 words × 4bits) is incorporated for storing data.

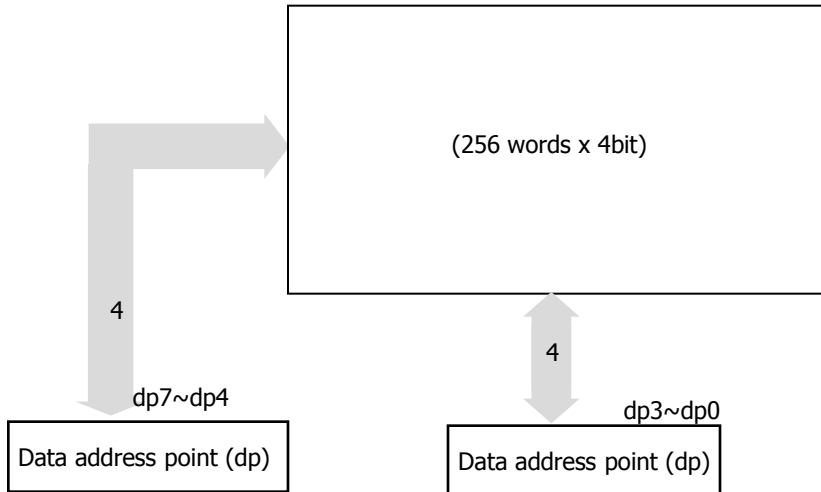
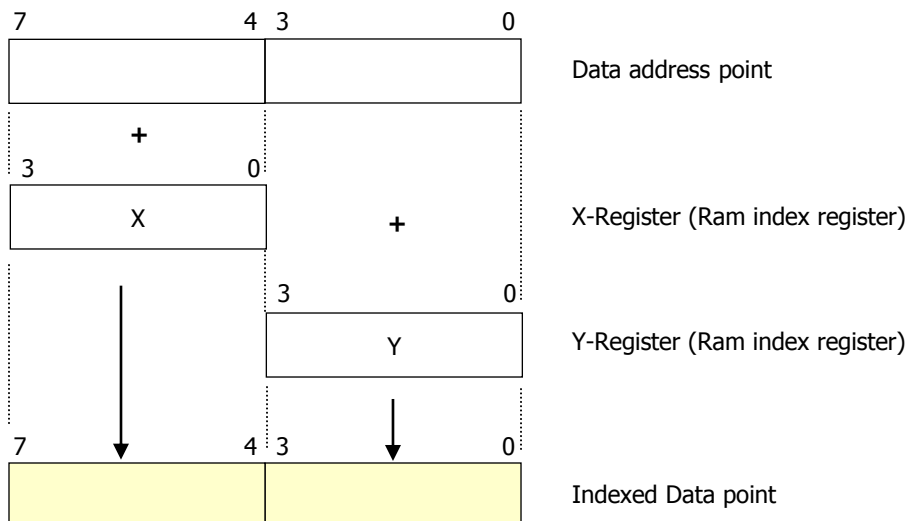


Fig.2.2 Data Memory

2.3.1. Data memory(RAM) addressing method

The whole data memory area is directly addressed by 8-bit ram data address point (dp).

Index data memory addressing is available using X-register and Y-register. In this case, X-register is added upper 4bit of data point and Y-register is added lower 4bit of data point.



2. Function Description

2.3.2. Data memory(RAM) data addressing example Program

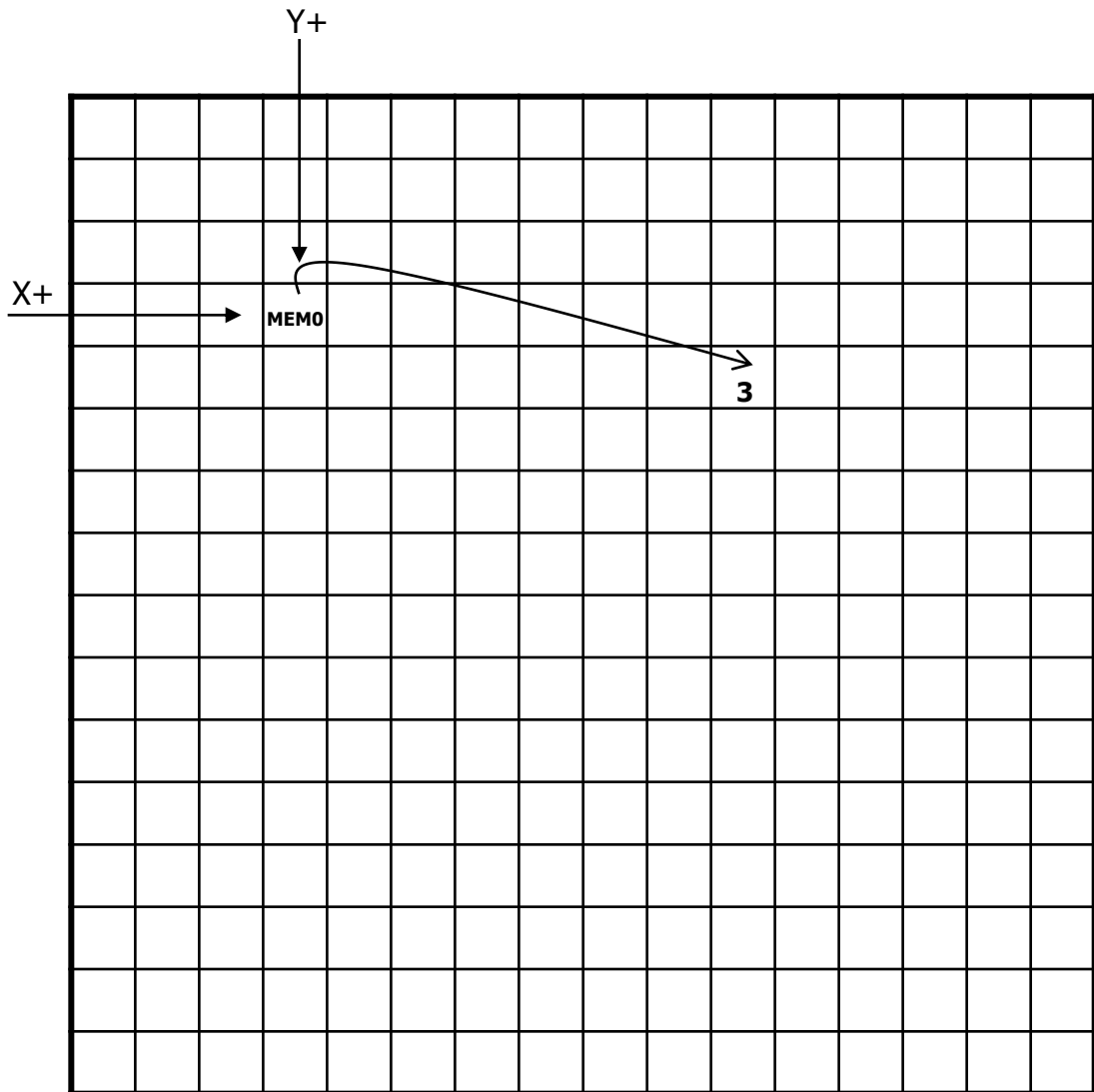


Fig.2.3 Data Memory Map

Below program example is guidance for understanding the flow of index data memory addressing.

```
MEM0 EQU 033h           ; Defining RAM Address

LDM MEM0,#03h          ; [33h] = #03h
LDY #7                 ; Setting Y register as #07h
LDX #1                 ; Setting X register as #01h
LDA MEM0               ; A = #03h == [MEM0]
EIX                   ; Index Enable
LDM MEM0,A             ; [4Ah] == [Indexed Addressed Ram] = A
DIX                   ; Index Disable
```

Result after executing is

MEM0 = #03h

[MEM0 + X + Y] == [4Ah] = #03h

2. Function Description

2.4. General Function Registers

2.4.1. X-register (X)

X-register is consist of 4bit, X-register is used for data memory indexing register.

2.4.2. Y-register (Y)

Y-register is consist of 4 bits. It can used for a general-purpose register.
Y-register also used for data memory indexing register.

2.4.3. Accumulator (ACC)

The 4-bit register for holding data and calculation results.

2.4.4. Peripheral Address Register(PAR)

The 6-bit address register for addressing peripheral registers including address buff register(ABR) , data buff register (DBR).

2.4.5. Address Buff Register (ABR)

The 16-bit register for address buffer.

The address of Address Buffer Register (ABR) is 38h ~ 3Bh on the peripheral register.
It is composed by 4 registers (ABR0, ABR1, ABR2, ABR3) and each register is 4 bit.

2.5. Buffer Registers (DBR, ABR)

Buffer registers are two types of 16 bit registers composed of 4-ninbble registers.

One is Data Buffer Register (DBR) and the other is Address Buffer Register (ABR).

The address of Data Buffer Register (DBR) is 3Ch ~ 3Fh and the address of Address Buffer Register (ABR) is 38h ~ 3Bh on the peripheral register.

These buffers are mainly used for Data transferring between ROM and buffer or peripheral registers and buffer. They are also used for general purpose register for data manipulation, data storage and intermediate buffer.

2.5.1. Function of Address Buff Register (ABR)

The most important function of ABR is ROM address pointer.

ABR must be used for reading data from ROM. The data pointed by ABR is read to DBR.

ABR value is varied through peripheral control instruction and "INC ABR".

2. Function Description

2.5.2. Function of Data Buff Register(DBR)

The most important function of DBR is intermediate (window) buffer for transferring data between peripheral registers and reading data from ROM.

When the data of ROM is read by "LDW @ABR", one word of ROM is fetched to DBR.

The MSB of ROM data is written to DBR3 and LSB to DBR0.

If the data of pointed ROM is 1234h, each DBR has the data as DBR0 = 4h, DBR1 = 3h, DBR2 = 2h and DBR3 = 1h.

DBR is also used for reading some peripheral register data by 12bit unit or 8bit unit.

The peripheral registers are T0CR and T1CR.

Note) HEX. File maps the data as big endian type. Be careful to read the ROM data.

When the programmer assigns the data like below, the ROM data is mapped as below.

DB 12h, 34h → ROM data = 1234h

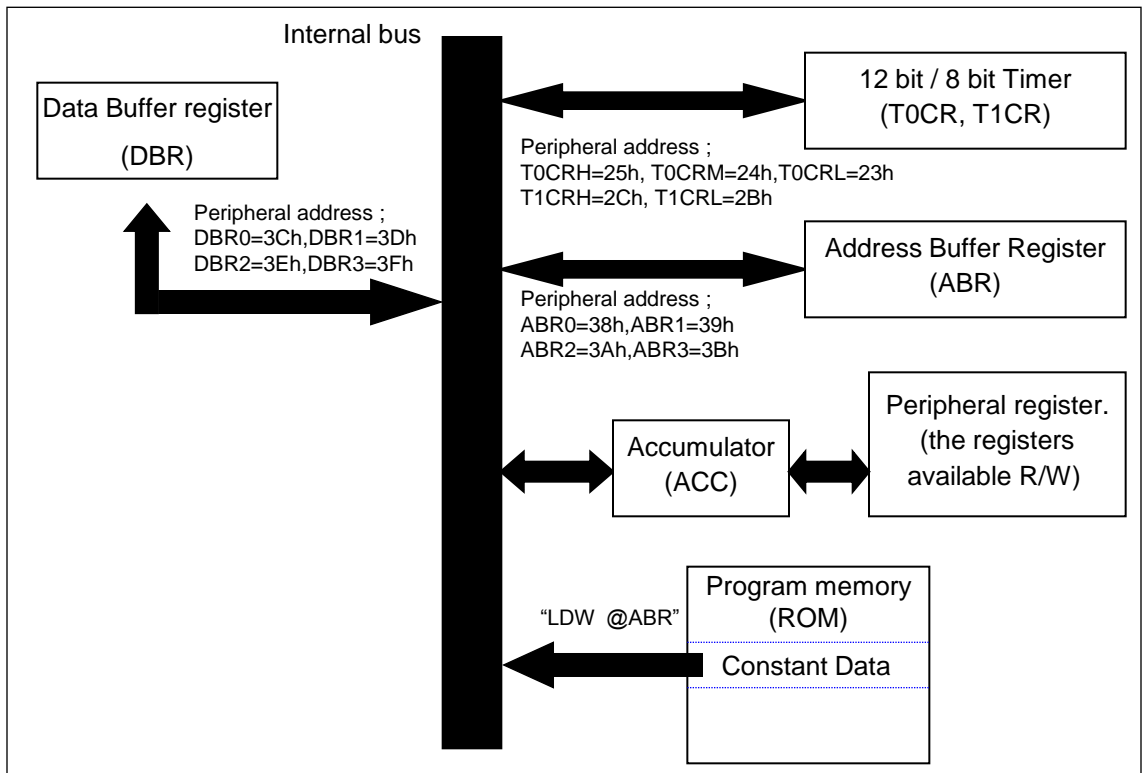


Fig.2.4 The internal Data flow among DBR, ABR, registers and ROM

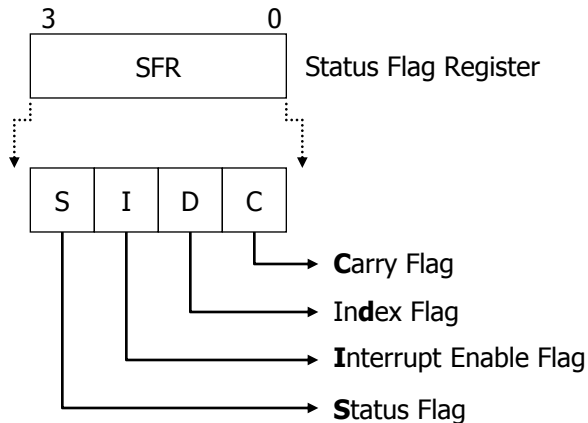
2. Function Description

2.6. Status Flag Registers (SFR)

Status Flag Register (SFR) consists of 4-bit register.

Each of the flags show the post state of operation and the flags determining the CPU operation, initialized as 0h in reset state.

When an interrupt is occurred, the value of SFR keep the value of pre-interrupt except for I flag. So, be careful to initialize the SFR status for getting reliable result in Interrupt sub-routine.



2.6.1 Carry flag (C)

- Carry flag bit is set when there is carry or borrow After executing ADDC / SUBC / ARRC/ARLC instructions.
- Set by SETC and clear by CLRC.
- Load from the assigned bit of Peripheral Registers by LDC
- Transfer to the assigned bit of Peripheral Registers by STC

2.6.2 Index flag (D)

- The control bit of ram data address point indexed or not.
- X-register and Y-register is used for index addressing.
- Set and cleared by EIX, DIX.

2.6.3 Interrupt enable flag (I)

- Master enable flag of interrupt.
- Set and cleared by EI, DI
- This Flag immediately becomes "0" when an interrupt is served.

2.6.4 Status flag (S)

- According to the condition after executing an instruction , set or clear.
- Can not be set or clear by any instruction.
- This Flag decides whether operation of BR and CALL would be done or not.

2. Function Description

2.7. Peripheral Registers

Peripheral Address	Function Registers	Read Write	Symbol	RESET Value
				3 2 1 0
00 h	PORT PA DATA REG.	R/W	*PADR	F
01 h	PORT PA PULL-UP SELECTION REG.	W	PAPU	F
02 h	PORT PA OPEN DRAIN SELECTION REG.	W	PAOD	F
03 h	PORT PA DIRECTION REG.	R/W	PADD	0
04 h	PORT PA STOP RELEASE SELECTION REG.	W	PAST	F
05 h	PORT PA FUNCTION SELECTION REG. LOW	R/W	PAFL	0
06 h	PORT PA FUNCTION SELECTION REG. HIGH	R/W	PAFH	0
07 h	PORT PB PULL-DOWN SELECTION REG.	W	PBPD	0 0 - -
08 h	PORT PB DATA REG.	R/W	*PBDR	F
09 h	PORT PB PULL-UP SELECTION REG.	W	PBPU	F
0A h	PORT PB OPEN DRAIN SELECTION REG.	W	PBOD	F
0B h	PORT PB DIRECTION REG.	R/W	PBDD	0
0C h	PORT PB STOP RELEASE SELECTION REG.	W	PBST	F
0D h	PORT PB FUNCTION SELECTION REG. LOW	R/W	PBFL	0
0E h	PORT PB FUNCTION SELECTION REG. HIGH	R/W	PBFH	0
0F h	PORT PB CURRENT DRIVING CONTROL REG.	W	PBCD	0 0 - -
10 h	PORT PD DATA REG.	R/W	*PDDR	F
11 h	PORT PD DIRECTION REG.	R/W	PDDD	0
12 h	<i>Reserved</i>			
13 h	PORT PE DATA REG.	R/W	*PEDR	F
14 h	PORT PE DIRECTION REG.	R/W	PEDD	0
15 h	PORT PE FUNCTION SELECTION REG. LOW	R/W	PEFL	0
16 h	ANALOG COMPARATOR MODE REG. 1	R/W	ACMR1	F
17 h	ANALOG COMPARATOR MODE REG. 2	R/W	ACMR2	0
18 h	D/A CONVERTER DATA REG.0	W	DACR0	0
19 h	D/A CONVERTER DATA REG.1	W	DACR1	0
1A h	EXT. INTERRUPT EDGE SELECTION REG.	W	IEDS0	0
1B h	SYSTEM CONTROL REG.	W	SCTLR	0
1C h	INTERRUPT REQUEST FLAG REG. 0	R/W	IRQR0	0
1D h	INTERRUPT REQUEST FLAG REG. 1	R/W	IRQR1	0
1E h	INTERRUPT ENABLE REG. 0	R/W	IENR0	0
1F h	INTERRUPT ENABLE REG. 1	R/W	IENR1	0

Note1> '-' is reserved bit , it must be read to "0".

Note2> * Using the bit access Instruction, bit is read-modified operation (SETR1/CLRR1/STC Instructions)

2. Function Description

Peripheral Address	Function Registers	Read Write	Symbol	RESET Value			
				3	2	1	0
20 h	TIMER 0 MODE REG. 0	R/W	T0MR0	0			
21 h	TIMER 0 MODE REG. 1	R/W	T0MR1	0			
22 h	TIMER 0 MODE REG. 2	R/W	T0MR2	0			
23 h	TIMER 0 DATA 0 LOW REG.(PWM0 DUTY LSB)	W	T0D0L	undefined			
	TIMER 0 COUNT REG. LOW	R	T0CRL	undefined			
24 h	TIMER 0 DATA 0 MIDDLE REG.(PWM0 DUTY MSB)	W	T0D0M	undefined			
	TIMER 0 COUNT REG. MIDDLE	R	T0CRM	undefined			
25 h	TIMER 0 DATA 0 HIGH REG.(PWM0 DUTY EXTENSION)	W	T0D0H	undefined			
	TIMER 0 COUNT REG. HIGH	R	T0CRH	undefined			
26 h	TIMER 0 DATA 1 LOW REG.(PWM0 PERIOD LSB)	W	T0D1L	undefined			
27 h	TIMER 0 DATA 1 MIDDLE REG.(PWM0 PERIOD MSB)	W	T0D1M	undefined			
28 h	TIMER 0 DATA 1 HIGH REG.(PWM0 CYCLE)	W	T0D1H	undefined			
29 h	TIMER 1 MODE REG. 0	R/W	T1MR0	0			
2A h	TIMER 1 MODE REG. 1	R/W	T1MR1	0			
2B h	TIMER 1 DATA 0 LOW REG.(PWM1 DUTY)	W	T1D0L	undefined			
	TIMER 1 COUNT REG. LOW	R	T1CRL	undefined			
2C h	TIMER 1 DATA 0 HIGH REG.(PWM1 DUTY EXTENSION)	W	T1D0H	undefined			
	TIMER 1 COUNT REG. HIGH	R	T1CRH	undefined			
2D h	TIMER 1 DATA 1 LOW REG.(PWM1 PERIOD)	W	T1D1L	undefined			
2E h	TIMER 1 DATA 1 HIGH REG.(PWM1 CYCLE)	W	T1D1H	undefined			
2F h	TIMER MODULATION CONTROL REG.	W	TMCR	F			
30 h	PORT PD FUNCTION SELECTION REG. LOW	R/W	PDFL	0			
31 h	PORT PD FUNCTION SELECTION REG. HIGH	R/W	PDFH	0			
32 h	WATCH-DOG TIMER CONTROL REG.	W	WDTCR	1 0 0 0			
33 h	VTG. DETECTION INDICATOR ENABLE REG.	W	VDIER	0			
	VTG DETECTION INDICATOR FLAG REG.	R	VDIR	- 0 0 0			
34 h	A/D CONVERTER MODE REG. 0	R/W	ADCM0	0 0 0 1			
35 h	A/D CONVERTER MODE REG. 1	W	ADCM1	0			
	A/D CONVERTER DATA REG. 0	R	ADCR0	undefined			
36 h	A/D CONVERTER INPUT SELECTION REG.	W	ADCIS	0			
	A/D CONVERTER DATA REG. 1	R	ADCR1	undefined			
37 h	A/D CONVERTER DATA REG. 2	R	ADCR2	undefined			
38 h	ADDRESS BUFF REGISTER 0	R/W	ABR0	undefined			
39 h	ADDRESS BUFF REGISTER 1	R/W	ABR1	undefined			
3A h	ADDRESS BUFF REGISTER 2	R/W	ABR2	undefined			
3B h	ADDRESS BUFF REGISTER 3	R/W	ABR3	undefined			
3C h	DATA BUFF REGISTER 0	R/W	DBR0	undefined			
3D h	DATA BUFF REGISTER 1	R/W	DBR1	undefined			
3E h	DATA BUFF REGISTER 2	R/W	DBR2	undefined			
3F h	DATA BUFF REGISTER 3	R/W	DBR3	undefined			

Note1> '-' is reserved bit , it must be read to "0".

3. I/O Ports

The ADAM45 has 14 I/O ports which are PA (4 I/O), PB (4 I/O), PD (4 I/O) and PE (2 I/O).

PA and PB Port have Stop Release selection register.

Pull-up resistor of PA, PB, PD and PE ports can be selectable by program.

Pull-down resistor of PB2 and PB3 ports can be selectable by program.

PA, PB, PD and PE ports contains data direction register which controls I/O and data register which stores port data.

PA, PB (except PB1), PD and PE Ports have Open Drain selection register and Data register.

*PB1 is Open Drain output only.

I/O Ports Registers

Port	Data Reg.	Direction Reg.	Function Reg.
port PA	PA	PADD	PAFH/PAFL
port PB	PB	PBDD	PBFH/PBFL
port PD	PD	PDDD	PDFH/PDFL
port PE	PE	PEDD	PEFL

R/W	R/W	R/W	R/W
Initial value	1111	0000	0000
default	fh	input	I/O ports

Port	Pull-up Reg.	Open-Drain Reg.	Stop Release Reg.	Current Driving Reg.	Pull-down Reg.
port PA	PAPU	PAOD	PAST	-	-
port PB	PBPU	PBOD	PBST	PBCD	PBPD

R/W	W	W	W	W	W
Initial value	1111	1111	1111	00--	00--
default	disable	disable	disable	disable	disable

3. I/O Ports

3.1. Port PA

Pin Name	Port Selection	Function Selection
PA0/AN0/TMA/C1I-/KSA0	PA0 (I/O)	AN0 Input / Timer0,1 Logic Output /Comparator-1 Negative Input / KSA0 Input
PA1/AN1/C1I+/AVREF/KSA1	PA1 (I/O)	AN1 Input / Comparator-1 Positive Input / AVREF Input / KSA1 Input
PA2/AN2/ECO/INT0/C2I-/KSA2	PA2 (I/O)	AN2 Input / Event Count-0 Input / INT0 Input / Comparator-2 Negative Input / KSA2 Input
PA3/AN3/KSA3	PA3 (I/O)	AN3 Input / KSA3 Input

3.1.1. PA Data Register (PA)

bit	3	2	1	0	
PA	PA3	PA2	PA1	PA0	00h
Initial value	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	

PA data register (PA) is 4-bit register to store data of port PA.

When set as the output state by PA, and data is written in PA, data is outputted into PA pin.

When set as the input state, input state of pin is read. The initial value of PA is "Fh" in reset state.

At output state, if port PA is read, PA Data Register is read instead of port PA.

3.1.2. PA Pull-up Resistor Control Register (PAPU)

bit	3	2	1	0	
PAPU	PAPU3	PAPU2	PAPU1	PAPU0	01h
Initial value	1	1	1	1	
R/W	W	W	W	W	

PA pull-up resistor control register (PAPU) is 4-bit register and can control pull-up on or off each bit, if corresponding port is selected as input. If PAPU is selected as "0", pull-up is enabled and if selected as "1", it is disabled. PAPU is write-only register and initialized as "Fh" in reset state. The pull-up is automatically disabled, if corresponding port is selected as output.

3.1.3. PA Open Drain Assign Register (PAOD)

bit	3	2	1	0	
PAOD	PAOD3	PAOD2	PAOD1	PAOD0	02h
Initial value	1	1	1	1	
R/W	W	W	W	W	

PA Open Drain Assign Register (PAOD) is 4-bit register, and can assign PA port as open drain output port each bit. If PAOD is selected as "0", port PA is open drain output, and if selected as "1", it is push-pull output. PAOD is write-only register and initialized as "Fh" in reset state.

3.1.4. PA I/O Data Direction Register (PADD)

bit	3	2	1	0	
PADD	PADD3	PADD2	PADD1	PADD0	03h
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

PA I/O Data Direction Register (PADD) is 4-bit register, and can assign input state or output state to each bit. If PADD is "0", port PA is in the input state, and if "1", it is in the output state. Since PADD is initialized as "0h" in reset state, the whole port PA becomes input state.

3. I/O Ports

3.1.5. PA Stop Release Selection Register (PAST)

bit	3	2	1	0	
PAST	PAST3	PAST2	PAST1	PAST0	04h
Initial value	1	1	1	1	
R/W	W	W	W	W	

PA Stop Release Selection Register (PAST) is 4-bit register, and can assign stop release pin or not. If PAST is selected as "0", stop release function is enabled and if selected as "1", it is disabled. PAST is write-only register and initialized as "Fh" in reset state.

3.1.6. PA Function Selection Register (PAFL)

bit	3	2	1	0	
PAFL	PA1		PA0		05h
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

3.1.7. PA Function Selection Register (PAFH)

bit	3	2	1	0	
PAFH	PA3		PA2		06h
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of PAFL

Bit Name	Selection Mode	Remarks
PA1	00 I/O	
	01 ADC selection	AN1
	10 I/O	
	11 AVREF selection	AVREF
PA0	00 I/O	
	01 ADC selection	AN0
	10 I/O	
	11 Tout selection	TMA

Selection Mode of PAFH

Bit Name	Selection Mode	Remarks
PA3	00 I/O	
	01 ADC selection	AN3
	10 I/O	
	11 I/O	
PA2	00 I/O	
	01 ADC selection	AN2
	10 Interrupt selection	INT0(EC0)
	11 I/O	

3.2. Port PB

Pin Name	Port Selection	Function Selection
PB0/AN8/KSB0	PB0 (I/O)	AN8 Input / KSB0 Input
PB1/PWM0/RESETB/KSB1	PB1 (I/O)	PWM0 Output / RESETB Input / KSB1 Input
PB2/AN10/PWM1/C2I+/KSB2	PB2 (I/O)	AN10 Input / PWM1 Output / Comparator-2 Positive Input / KSB2 Input
PB3/AN11/EC1/INT1/TMB/CMO/KSB3	PB3 (I/O)	AN11 Input / Event Count-1 Input / INT1 Input / Timer0,1 Logic Output / Comparator Output / KSB3 Input

3. I/O Ports

3.2.1. PB Data Register (PB)

bit	3	2	1	0	
PB	PB3	PB2	PB1	PB0	08h
Initial value	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	

PB data register (PB) is 4-bit register to store data of port PB.

When set as the output state by PB, and data is written in PB, data is outputted into PB pin.

When set as the input state, input state of pin is read. The initial value of PB is "Fh" in reset state.

At output state, if port PB is read, PB Data Register is read instead of port PB.

3.2.2. PB Pull-up Resistor Control Register (PBPU)

bit	3	2	1	0	
PBPU	PBPU3	PBPU2	PBPU1	PBPU0	09h
Initial value	1	1	1	1	
R/W	W	W	W	W	

PB pull-up resistor control register (PBPU) is 4-bit register and can control pull-up on or off each bit, if corresponding port is selected as input. If PBPU is selected as "0", pull-up is enabled and if selected as "1", it is disabled. PBPU is write-only register and initialized as "Fh" in reset state. The pull-up is automatically disabled, if corresponding port is selected as output.

3.2.3. PB Open Drain Assign Register (PBOD)

bit	3	2	1	0	
PBOD	PBOD3	PBOD2	PBOD1	PBOD0	0Ah
Initial value	1	1	1	1	
R/W	W	W	W	W	

PB Open Drain Assign Register (PBOD) is 4-bit register, and can assign PB port as open drain output port each bit. If PBOD is selected as "0", port PB is open drain output, and if selected as "1", it is push-pull output. PBOD is write-only register and initialized as "Fh" in reset state.

3.2.4. PB I/O Data Direction Register (PBDD)

bit	3	2	1	0	
PBDD	PBDD3	PBDD2	PBDD1	PBDD0	0Bh
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

PB I/O Data Direction Register (PBDD) is 4-bit register, and can assign input state or output state to each bit. If PBDD is "0", port PB is in the input state, and if "1", it is in the output state. Since PBDD is initialized as "0h" in reset state, the whole port PB becomes input state.

3.2.5. PB Pull-down Resistor Selection Register (PBPD)

bit	3	2	1	0	
PBPD	PBPD3	PBPD2	-	-	07h
Initial value	0	0	-	-	
R/W	W	W	W	W	

PB Pull-down resistor Selection Register (PBPD) is 2-bit register, and can control pull-down on or off each bit. If PBPD is selected as "1", pull-down is enabled and if selected as "0", it is disabled. PBPD is write-only register and initialized as "0h" in reset state.

3. I/O Ports

3.2.6. PB Stop Release Selection Register (PBST)

bit	3	2	1	0	
PBST	PBST3	PBST2	PBST1	PBST0	0Ch
Initial value	1	1	1	1	
R/W	W	W	W	W	

PB Stop Release Selection Register (PBST) is 4-bit register, and can assign stop release pin or not. If PBST is selected as "0", stop release function is enabled and if selected as "1", it is disabled. PBST is write-only register and initialized as "Fh" in reset state.

3.2.7. PB Function Selection Register (PBFL)

bit	3	2	1	0	
PBFL	PB1		PB0		0Dh
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

3.2.8. PB Function Selection Register (PBFH)

bit	3	2	1	0	
PBFH	PB3		PB2		0Eh
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of PBFL

Bit Name	Selection Mode	Remarks	
PB1	00		
	01	I/O	
	10		
	11	Tout selection	PWM0
PB0	00	I/O	
	01	ADC selection	AN8
	10	I/O	
	11	I/O	

Selection Mode of PBFH

Bit Name	Selection Mode	Remarks	
PB3	00	I/O	
	01	ADC selection	AN11
	10	Interrupt selection	INT1(EC1)
	11	Tout selection	TMB
PB2	00	I/O	
	01	ADC selection	AN10
	10	I/O	
	11	Tout selection	PWM1

3.2.9. PB Current Driving Control Register (PBCD)

bit	3	2	1	0	
PBCD	PBCD3	PBCD2	-	-	0Fh
Initial value	0	0	-	-	
R/W	W	W	W	W	

PB Current Driving Control Register (PBCD) is 2-bit register, and can enhance current drive capacity. If PBCD is selected as "1", current driving control function is enabled and if selected as "0", it is disabled. PBCD is write-only register and initialized as "0h" in reset state.

3. I/O Ports

3.3. Port PD

Pin Name	Port Selection	Function Selection
PD0/AN4	PD0 (I/O)	AN4 Input
PD1/AN5	PD1 (I/O)	AN5 Input
PD2/AN6	PD2 (I/O)	AN6 Input
PD3/AN7	PD3 (I/O)	AN7 Input

3.3.1. PD Data Register (PD)

bit	3	2	1	0	
PD	PD3	PD2	PD1	PD0	10h
Initial value	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	

PD data register (PD) is 4-bit register to store data of port PD.

When set as the output state by PD, and data is written in PD, data is outputted into PD pin.

When set as the input state, input state of pin is read. The initial value of PD is "Fh" in reset state.

At output state, if port PD is read, PD Data Register is read instead of port PD.

3.3.2. PD I/O Data Direction Register (PDDD)

bit	3	2	1	0	
PDDD	PDDD3	PDDD2	PDDD1	PDDD0	11h
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

PD I/O Data Direction Register (PDDD) is 4-bit register, and can assign input state or output state to each bit. If PDDD is "0", port PD is in the input state, and if "1", it is in the output state. Since PDDD is initialized as "0h" in reset state, the whole port PD becomes input state.

3.3.3. PD Function Selection Register (PDFL)

bit	3	2	1	0	
PDFL	PD1		PD0		30h
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

3.3.4. PD Function Selection Register (PDFH)

bit	3	2	1	0	
PDFH	PD3		PD2		31h
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of PDFL

Bit Name	Selection Mode		Remarks
PD1	00	I/O	
	01	ADC selection	AN5
	10	Open-Drain selection	
	11	Pull-up selection	
PD0	00	I/O	
	01	ADC selection	AN4
	10	Open-Drain selection	
	11	Pull-up selection	

Selection Mode of PDFH

Bit Name	Selection Mode		Remarks
PD3	00	I/O	
	01	ADC selection	AN7
	10	Open-Drain selection	
	11	Pull-up selection	
PD2	00	I/O	
	01	ADC selection	AN6
	10	Open-Drain selection	
	11	Pull-up selection	

3. I/O Ports

3.4. Port PE

Pin Name	Port Selection	Function Selection
PE0	PE0 (I/O)	-
PE1	PE1 (I/O)	-
-	-	-
-	-	-

3.4.1. PE Data Register (PE)

bit	3	2	1	0	
PE	-	-	PE1	PE0	13h
Initial value	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	

PE data register (PE) is 4-bit register to store data of port PE. When set as the output state by PE, and data is written in PE, data is outputted into PE pin. When set as the input state, input state of pin is read. The initial value of PE is "Fh" in reset state. At output state, if port PE is read, PE Data Register is read instead of port PE.

3.4.2. PE I/O Data Direction Register (PEDD)

bit	3	2	1	0	
PEDD	-	-	PEDD1	PEDD0	14h
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

PE I/O Data Direction Register (PEDD) is 4-bit register, and can assign input state or output state to each bit. If PEDD is "0", port PE is in the input state, and if "1", it is in the output state. Since PEDD is initialized as "0h" in reset state, the whole port PE becomes input state.

3.4.3. PE Function Selection Register (PEFL)

bit	3	2	1	0	
PEFL	PE1		PE0		15h
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of PEFL

Bit Name	Selection Mode		Remarks
PE1	00	I/O	
	01	<i>Prohibit</i>	
	10	Open-Drain selection	
	11	Pull-up selection	
PE0	00	I/O	
	01	<i>Prohibit</i>	
	10	Open-Drain selection	
	11	Pull-up selection	

4. Oscillation Circuit

4.1. Oscillation Circuit

Clock from oscillation circuit makes CPU clock via clock pulse generator, and then provide peripheral hardware clock.

There is 1 types of Oscillation circuit and it can be divided in 4 different oscillator option modes. The user can use OTP Configuration Option Bits (OSCS1 through OSCS0) to select one of these 4 types. Refer to Table 4.1.

- IRC : Internal RC Oscillator (4 modes)

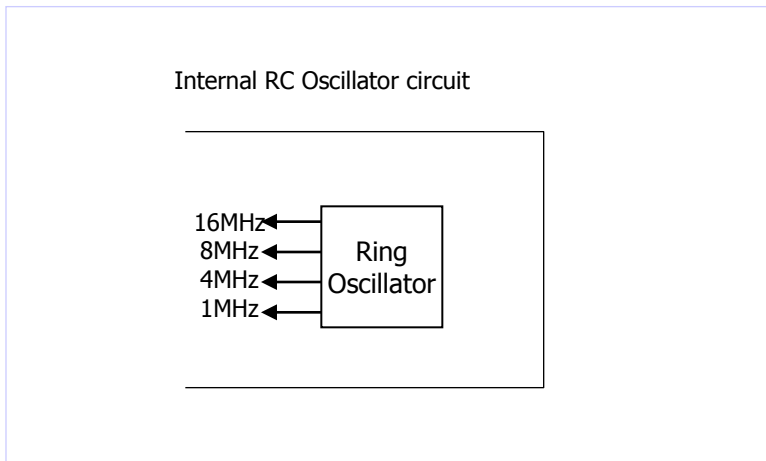


Fig.4.1 Oscillator configurations

It is Internal RC Oscillator circuit. The Internal Oscillator is calibrated in Factory. In STOP mode, Internal RC oscillator is stopped.

Below table shows the selection of the oscillator type by OTP Configuration Option Bits (Address 8000h, OSCS1 ~ OSCS0). (Refer to 15.2. Configuration Option Bit Description)

Table. 4.1 Oscillator Type and Modes Selection

OSCS[1:0]		Oscillator Modes
OSCS[1]	OSCS[0]	
1	1	Internal RC 4MHz
1	0	Internal RC 8MHz
0	1	Internal RC 16MHz
0	0	Internal RC 1MHz

5. Watch Dog Timer

5.1. Watch Dog Timer (WDT)

Watch dog timer is organized binary of 19 steps. The signal of $f_{OSC}/4$ cycle comes in the first step of WDT after WDT reset. If this counter was overflowed, reset signal automatically come out so that internal circuit is initialized. The overflow time is initially $2^{18} \times 4/f_{OSC}$ (262.144ms at $f_{OSC} = 4.0\text{MHz}$), it is selectable by WDT Control Register (WDTCR). Normally, the binary counter must be reset before the overflow by using reset instruction (WDTC), Power-on reset pulse or Low VDD detection pulse. It is constantly reset in STOP and SLEEP mode. When STOP and SLEEP are released, counting is restarted.

5.1.1. WDT Control Register

bit	3	2	1	0	
WDTCR	WDTRST	-	WDTCK1	WDTCK0	32h
Initial value	1	-	0	0	
R/W	W	W	W	W	

WDTRST	0	WDT interrupt enable, when WDT Overflow is occurred.
	1	System Reset enable, when WDT Overflow is occurred. (default)
-	-	-
WDTCK1 & WDTCK0	00	WDT Overflow Time is $2^{18} \times T_{ck}$
	01	WDT Overflow Time is $2^{17} \times T_{ck}$
	10	WDT Overflow Time is $2^{16} \times T_{ck}$
	11	WDT Overflow Time is $2^{15} \times T_{ck}$

Reset or Interrupt Wakeup Time (Example)

	$T_{ck} * 2^{18}$	$T_{ck} * 2^{17}$	$T_{ck} * 2^{16}$	$T_{ck} * 2^{15}$	Unit
if $T_{ck} = 1\mu\text{s}$	262.144	131.072	65.536	32.768	ms

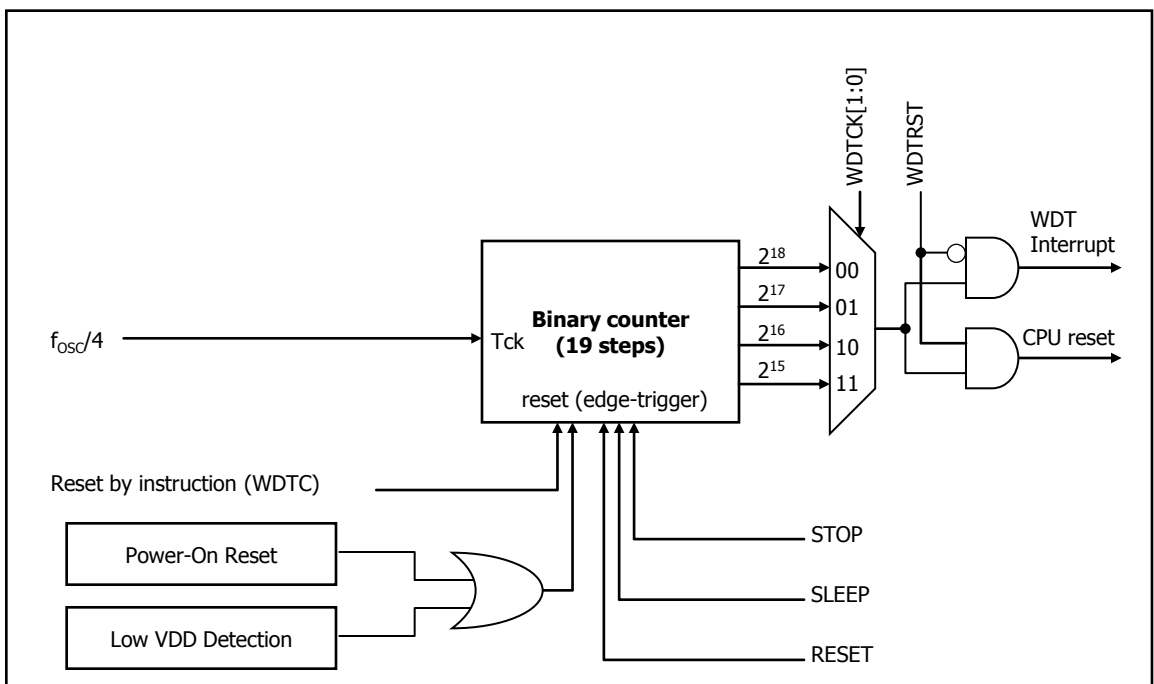


Fig.5.1 Block Diagram of Watch-dog Timer

6. Timer

6.1. Timer

6.1.1. Timer operation mode

Timer is basically made of Timer Data Register, Timer Mode Register and control circuit. The types of Timer are 12-bit binary counter Timer0 (T0), 8-bit binary counter Timer1 (T1).

Timer0 Data Register consists of Timer0 Data 0 High Register (TOD0H), Timer0 Data 0 Middle Register (TOD0M), Timer0 Data 0 Low Register (TOD0L), Timer0 Data 1 High Register (TOD1H), Timer0 Data 1 Middle Register (TOD1M) and Timer0 Data 1 Low Register (TOD1L).

Timer1 Data Register consists of Timer1 Data 0 High Register (T1D0H), Timer1 Data 0 Low Register (T1D0L), Timer1 Data 1 High Register (T1D1H) and Timer1 Data 1 Low Register (T1D1L).

Timer0	<ul style="list-style-type: none"> - . 12-bit Interval Timer - . 12-bit Event Counter - . 12-bit Capture Timer - . 12-bit rectangular-wave output - . (8 + 4) Pulse Width Modulation output
Timer1	<ul style="list-style-type: none"> - . 8-bit Interval Timer - . 8-bit Event Counter - . 8-bit Capture Timer - . 8-bit rectangular-wave output - . (6 + 2) Pulse Width Modulation output

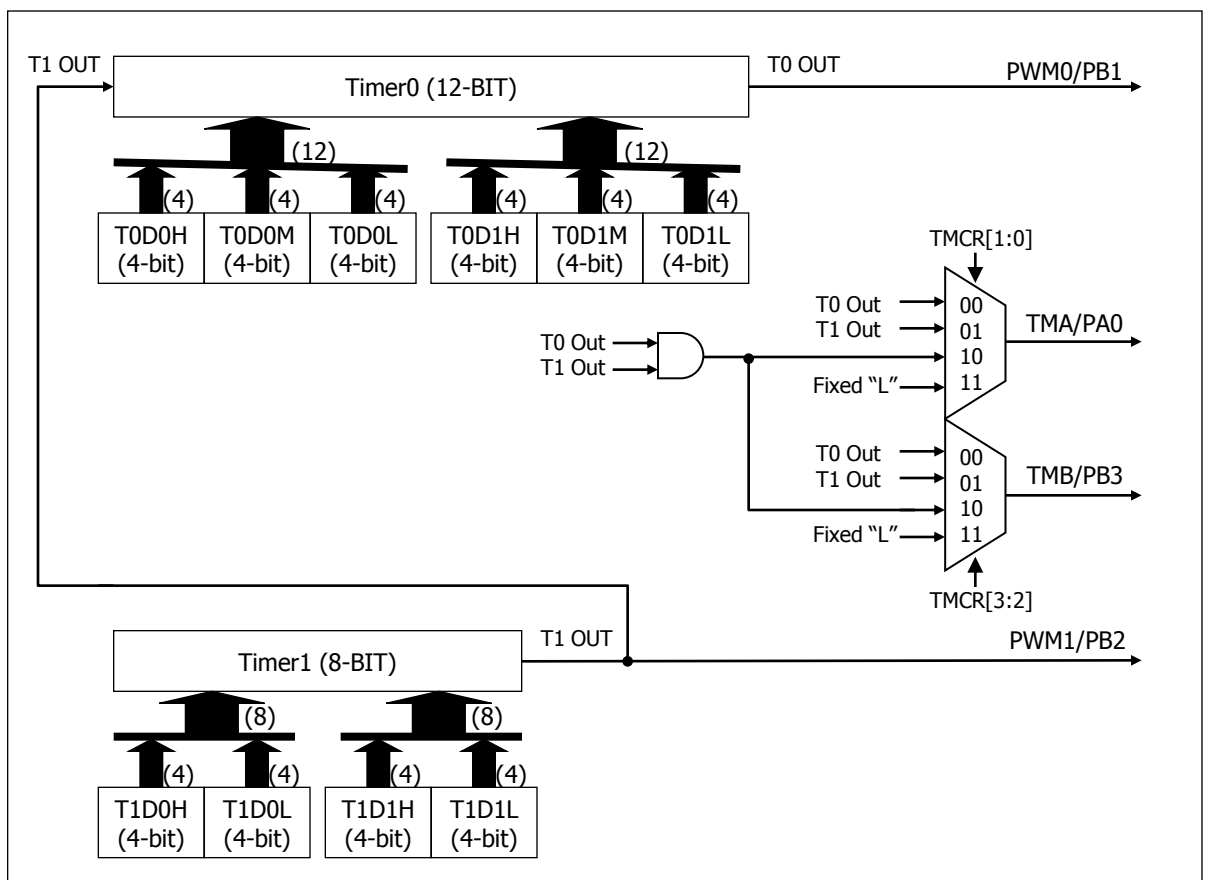
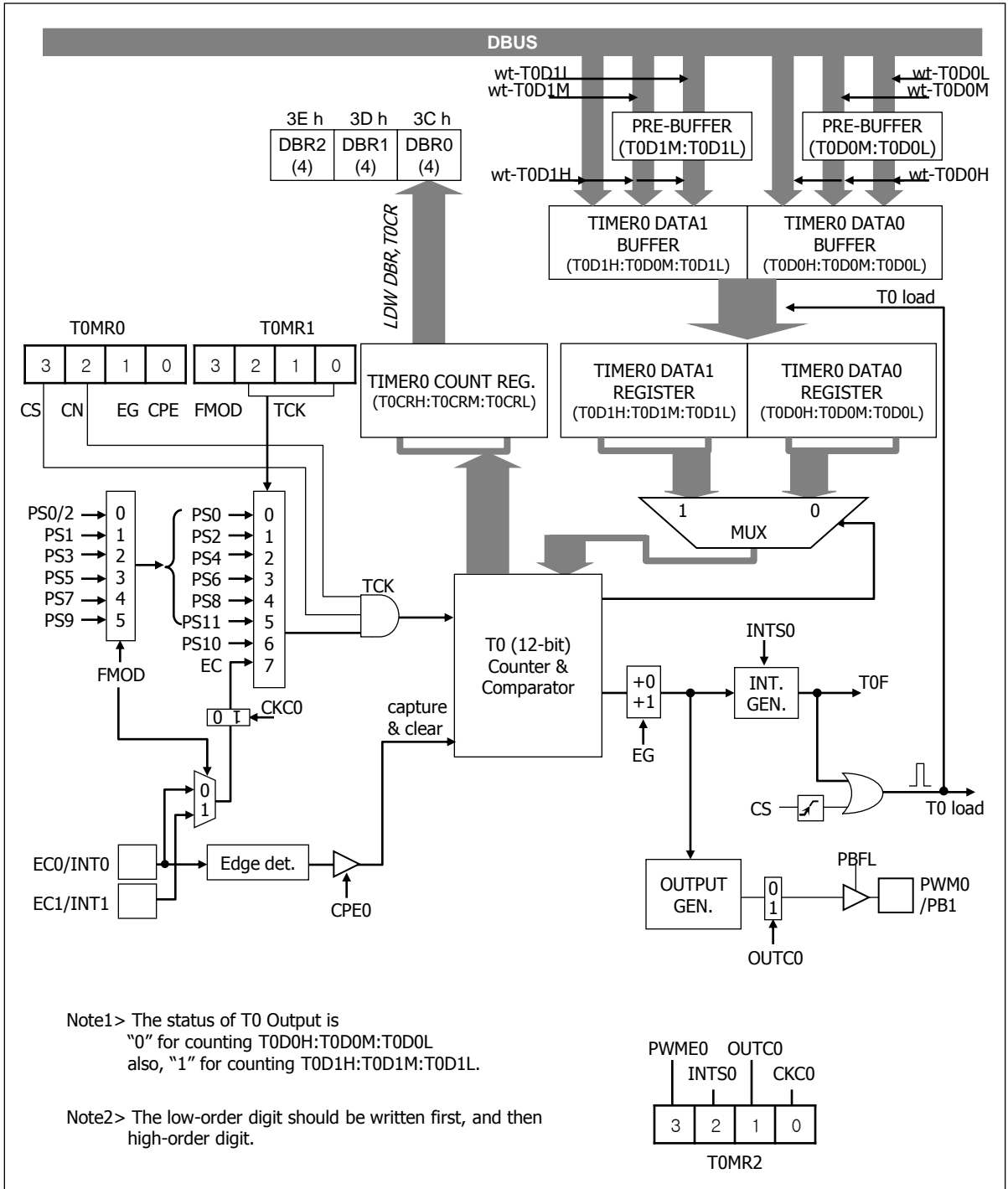


Fig.6.1 Timer/Counter Block diagram

6. Timer

6.2. Timer0

6.2.1. Timer0(T0) Block Diagram



6. Timer

6.2.2. Timer0 Control Register

- Timer0 Mode Register 0 (T0MR0)

	3	2	1	0	
T0MR0	T0CS	T0CN	T0EG	T0CPE	20h
initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of T0MR0

Bit Name			Selection Mode	Remarks
T0CS	Timer0 Clear / start Control	0	Timer0 Stop	
		1	Timer0 Clear and Start	
T0CN	Timer0 Pause / Continue Control	0	Timer0 Pause	
		1	Timer0 continue	
T0EG	Timer0 Count Control	0	Timer0 Count	
		1	Timer0 Count + 1	
T0CPE	Input capture Mode selection	0	Timer/Counter Mode	
		1	Capture Mode	

- Timer0 Mode Register 1 (T0MR1)

	3	2	1	0	
T0MR1	FMODE	T0CK2	T0CK1	T0CK0	21h
initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of T0MR1

Bit Name		Selection Mode		Remarks
FMODE	Input clock selection master bit	0	1	
T0CK2 T0CK1 T0CK0	Input clock selection	000	PS0	*PS0/2
		001	PS2	PS1
		010	PS4	PS3
		011	PS6	PS5
		100	PS8	PS7
		101	PS11	PS9
		110	PS10	
		111	EC0	EC1

Caution : PS0/2 must be used only in the case of $f_{osc} \leq 4.0\text{MHz}$

6. Timer

• Timer0 Mode Register 2 (TOMR2)

	3	2	1	0	
TOMR2	PWME0	INTS0	OUTC0	CKC0	22h
initial value	0	0	0	0	
	R/W	R/W	R/W	R/W	

Selection Mode of TOMR2

Bit Name			Selection Mode	Remarks
PWME0	Timer/PWM Mode Selection	0	Timer0 Normal Mode	
		1	Timer0 PWM Mode	
INTS0	Timer0 Interrupt Overflow Control	0	Timer0 Interrupt Every 2 nd Overflow	
		1	Timer0 Interrupt Every Overflow	
OUTC0	Timer0 Output Control	0	Timer0 Output Normal	
		1	Timer0 Output Reverse	
CKC0	Timer0 Event Counter Input Control	0	Timer0 Event counter Input Clock Normal	
		1	Timer0 Event counter Input Clock Reverse	

• Timer0 Data0 Register Low (TOD0L) = PWM0 DUTY LSB

	3	2	1	0	
TOD0L	TOD0L3	TOD0L2	TOD0L1	TOD0L0	23h
initial value	-	-	-	-	
	R/W	W	W	W	

• Timer0 Count Register Low (T0CRL)

	3	2	1	0	
T0CRL	T0CRL3	T0CRL2	T0CRL1	T0CRL0	23h
initial value	-	-	-	-	
	R/W	R	R	R	

• Timer0 Data0 Register Middle (TOD0M) = PWM0 DUTY MSB

	3	2	1	0	
TOD0M	TOD0M3	TOD0M2	TOD0M1	TOD0M0	24h
initial value	-	-	-	-	
	R/W	W	W	W	

• Timer0 Count Register Middle (T0CRM)

	3	2	1	0	
T0CRM	T0CRM3	T0CRM2	T0CRM1	T0CRM0	24h
initial value	-	-	-	-	
	R/W	R	R	R	

• Timer0 Data0 Register High (TOD0H) = PWM0 DUTY EXTENSION

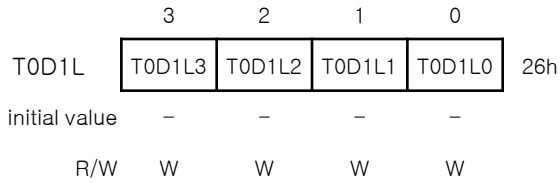
	3	2	1	0	
TOD0H	TOD0H3	TOD0H2	TOD0H1	TOD0H0	25h
initial value	-	-	-	-	
	R/W	W	W	W	

• Timer0 Count Register High (T0CRH)

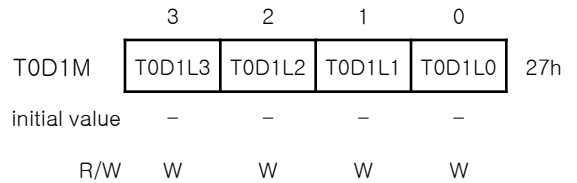
	3	2	1	0	
T0CRH	T0CRH3	T0CRH2	T0CRH1	T0CRH0	25h
initial value	-	-	-	-	
	R/W	R	R	R	

6. Timer

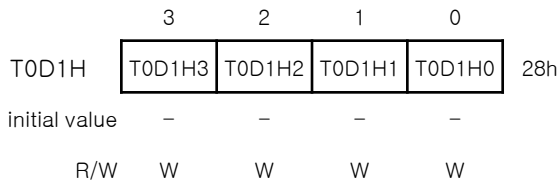
- Timer0 Data1 Register Low (TOD1L)
= PWM0 PERIOD LSB



- Timer0 Data1 Register Middle (TOD1M)
= PWM0 PERIOD MSB

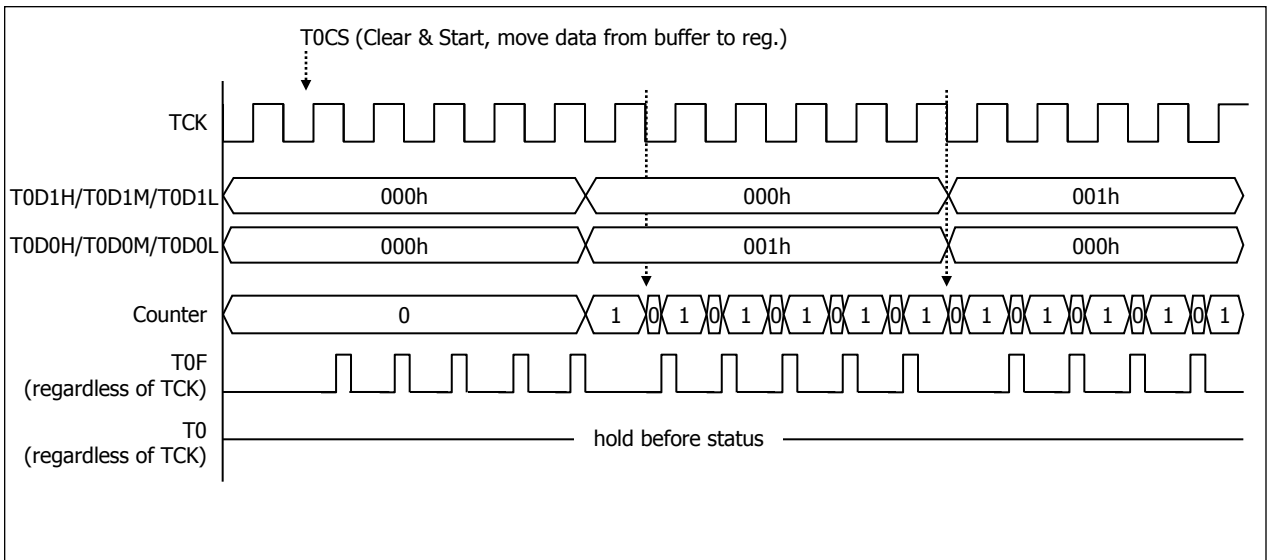


- Timer0 Data1 Register High (TOD1H)
= PWM0 CYCLE



6.2.3. Timer0 Caution

Caution : In the case of T0EG is "0",

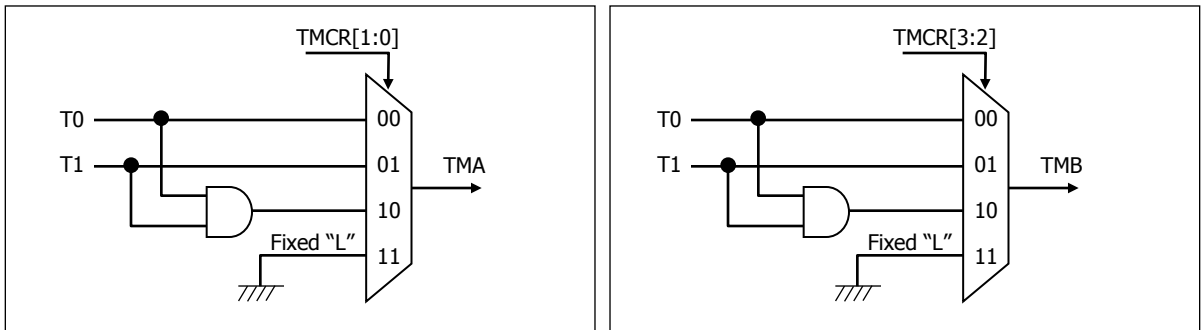


Want to count "0", set T0EG=1

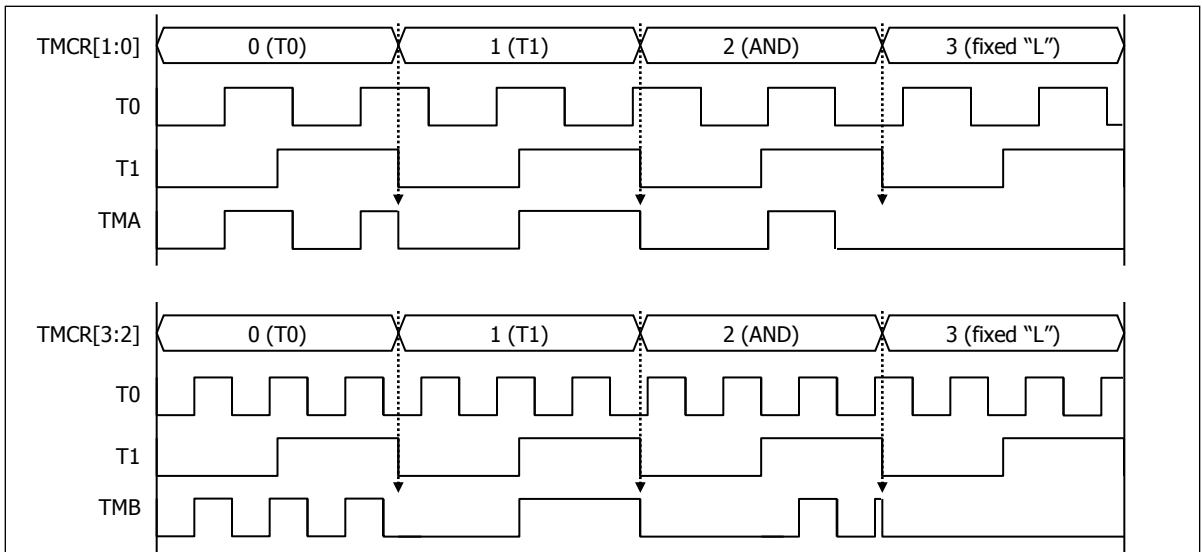
6. Timer

6.2.4. TMA/TMB OUTPUT CONTROL

* TMA/TMB Logical Output Control



* TMA/TMB Output Timing Diagram



• TMA/TMB Output Control Register (TMCR)

	3	2	1	0	
TMCR	TMCR3	TMCR2	TMCR1	TMCR0	2Fh
initial value	1	1	1	1	
R/W	W	W	W	W	

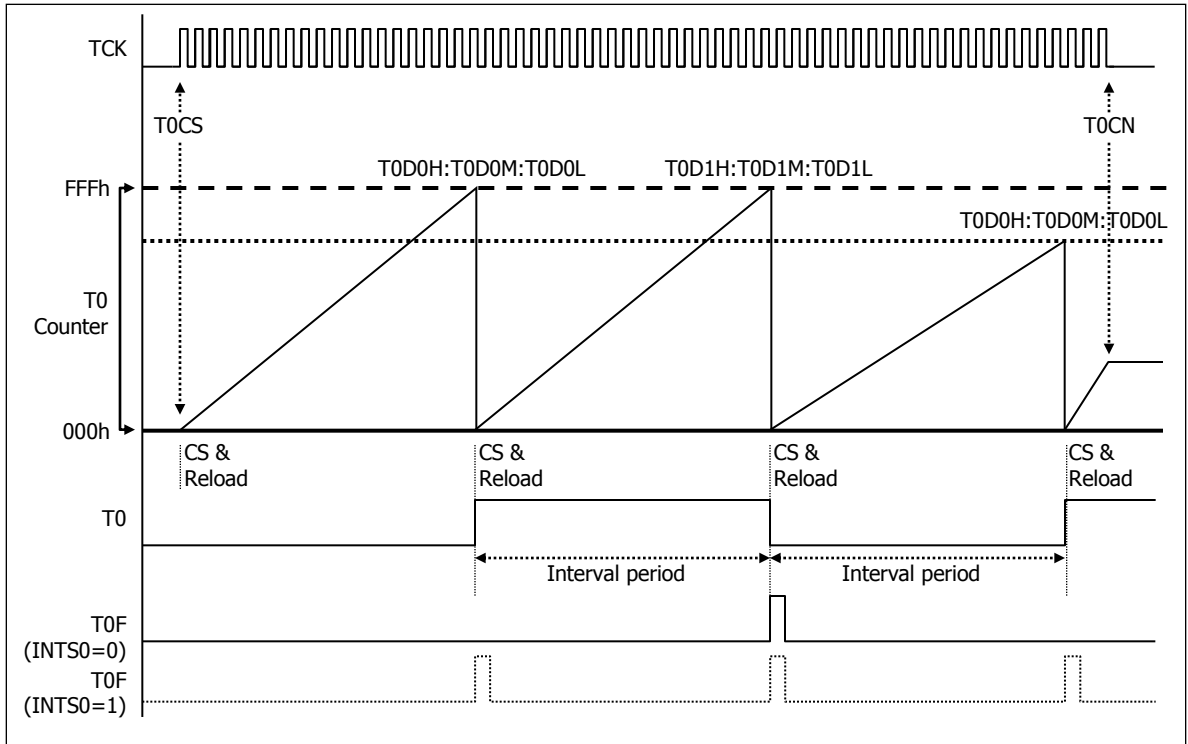
Selection Mode of TMCR

Bit Name		Selection Mode	Remarks
TMCR3	TMB Output Selection	00	T0 (Timer0 Output)
		01	T1 (Timer1 Output)
		10	T0 and T1
		11	fixed "L" (default)
TMCR1	TMA Output Selection	00	T0 (Timer0 Output)
		01	T1 (Timer1 Output)
		10	T0 and T1
		11	fixed "L" (default)

6. Timer

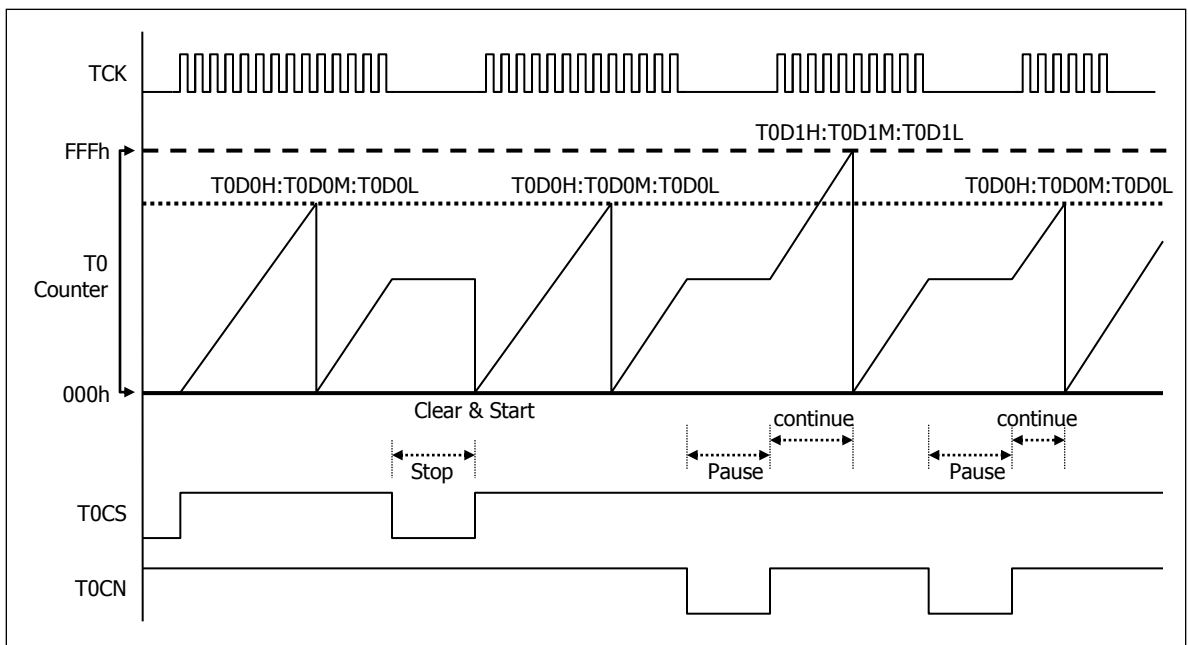
6.2.5. Timer0 Timing Diagram

* 12-bit Timer/Counter mode Timing Diagram



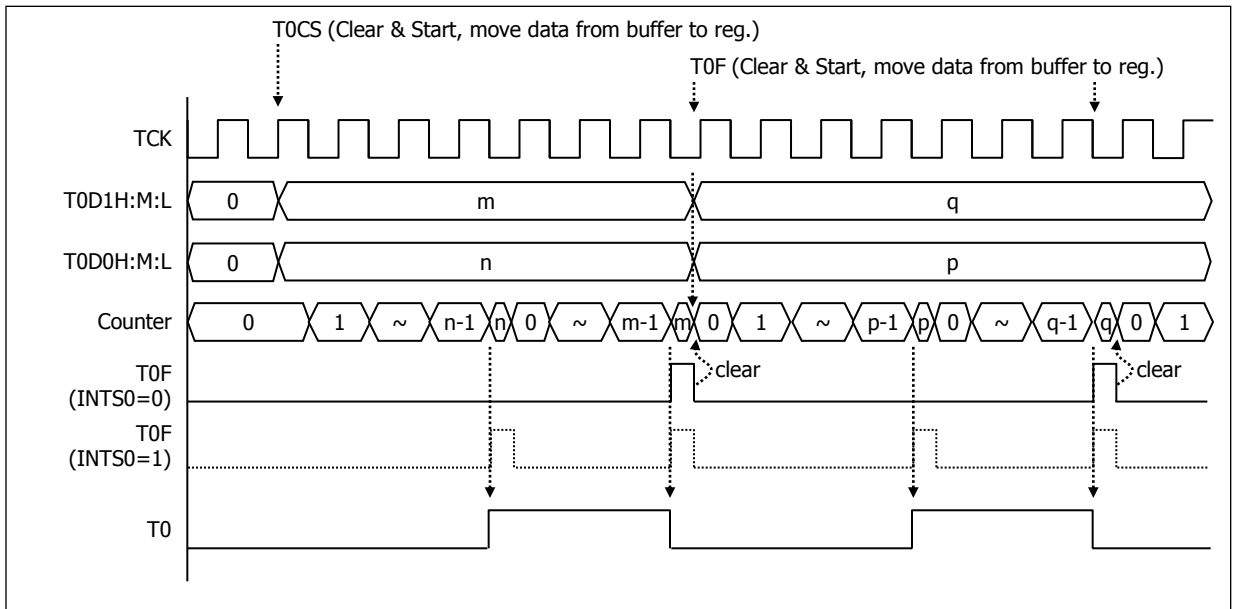
Note > CS : Timer0 Counter Clear & Start.
 Reload : Timer0 Data move from Data buffer to Data register.

* Start / Stop operation

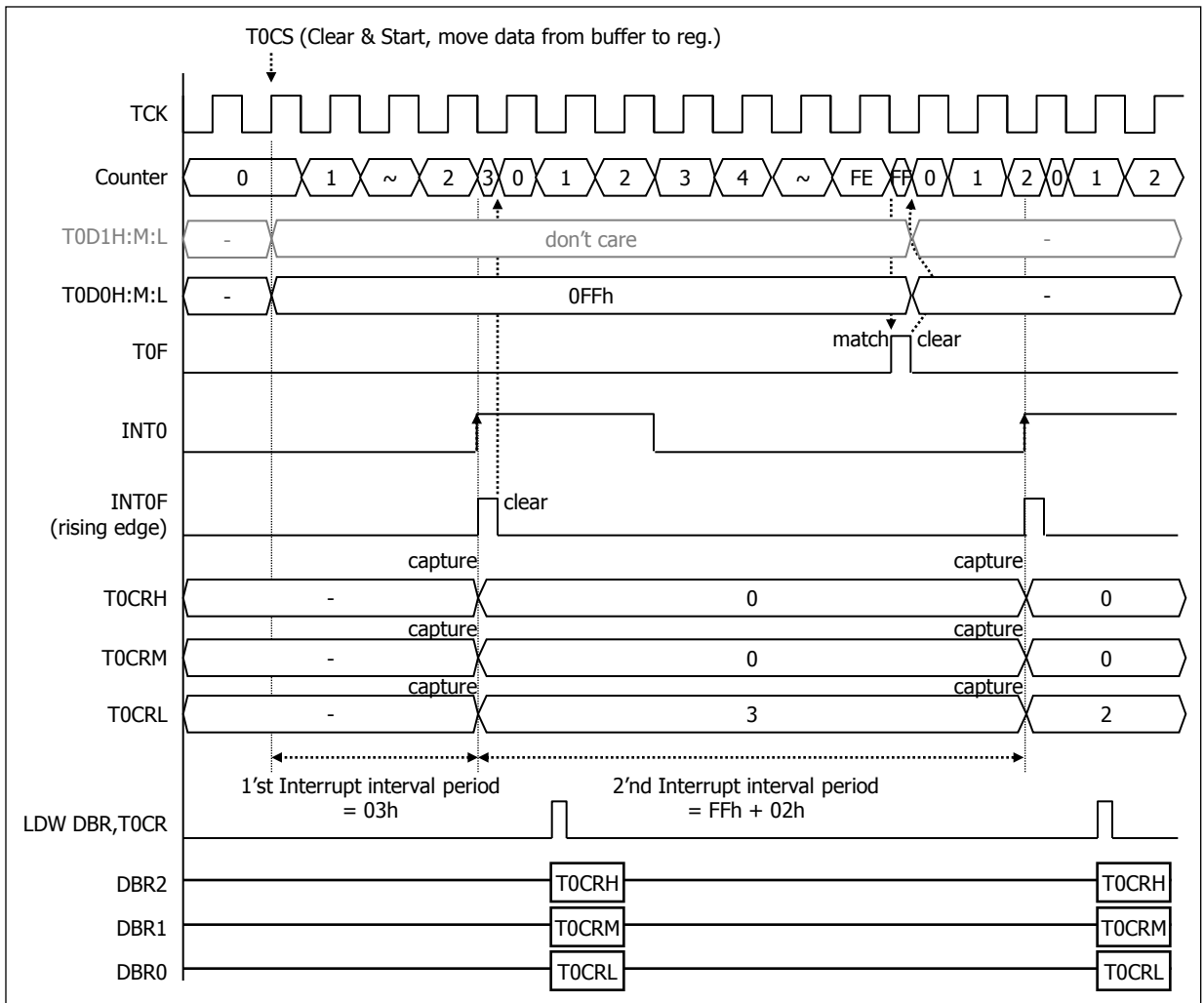


6. Timer

* 12-bit Timer/Counter mode Timing Diagram

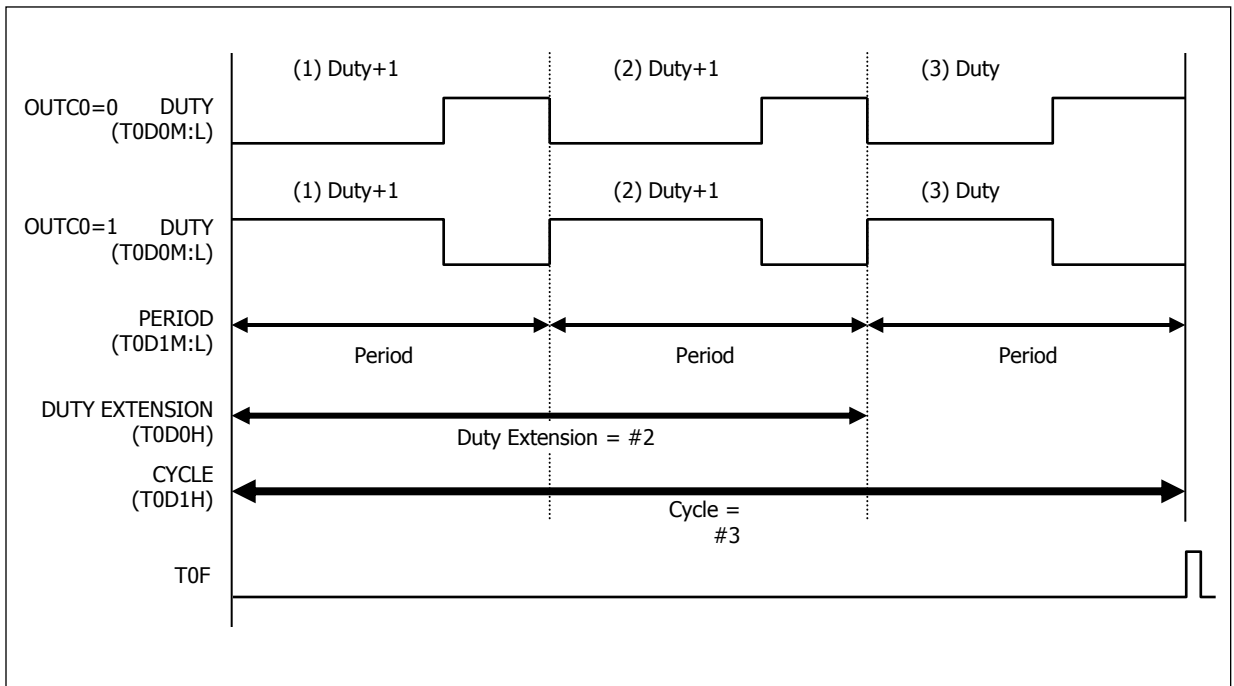


* 12-bit Capture mode Timing Diagram

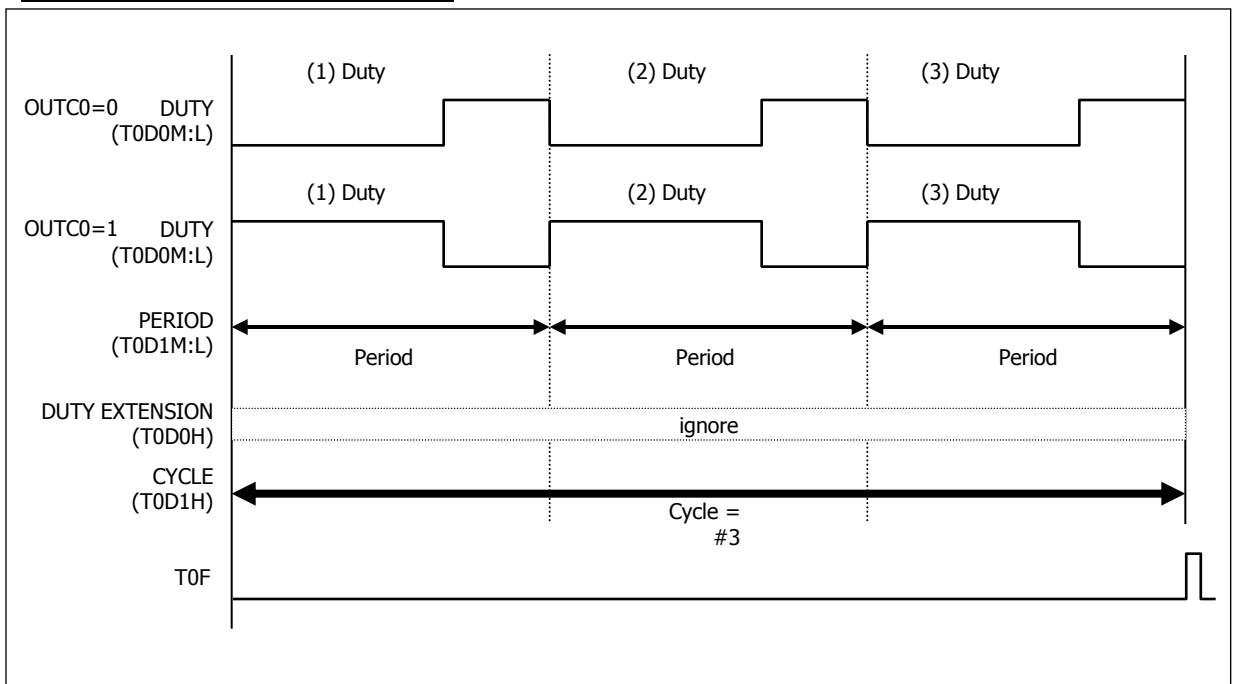


6. Timer

• PWM mode Timing Diagram : (TOEG=0)



• PWM mode Timing Diagram : (TOEG=1)

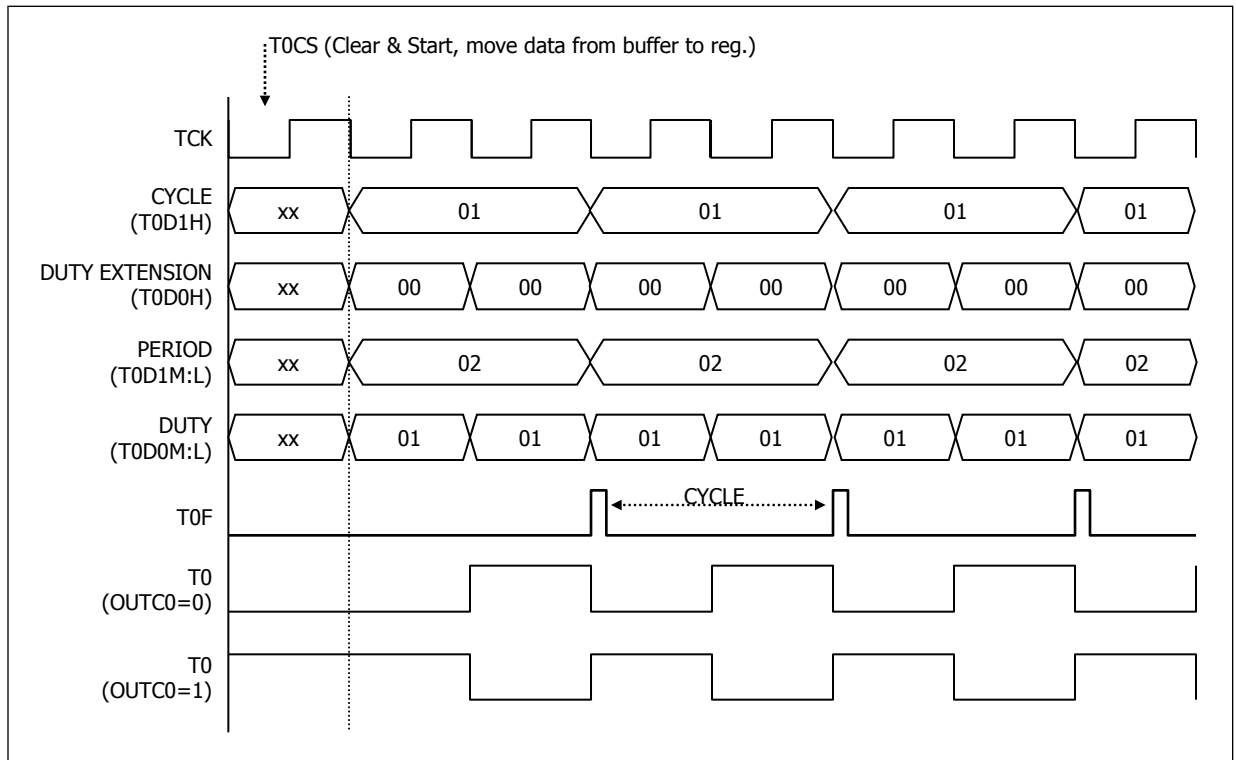


• PWM mode Condition :

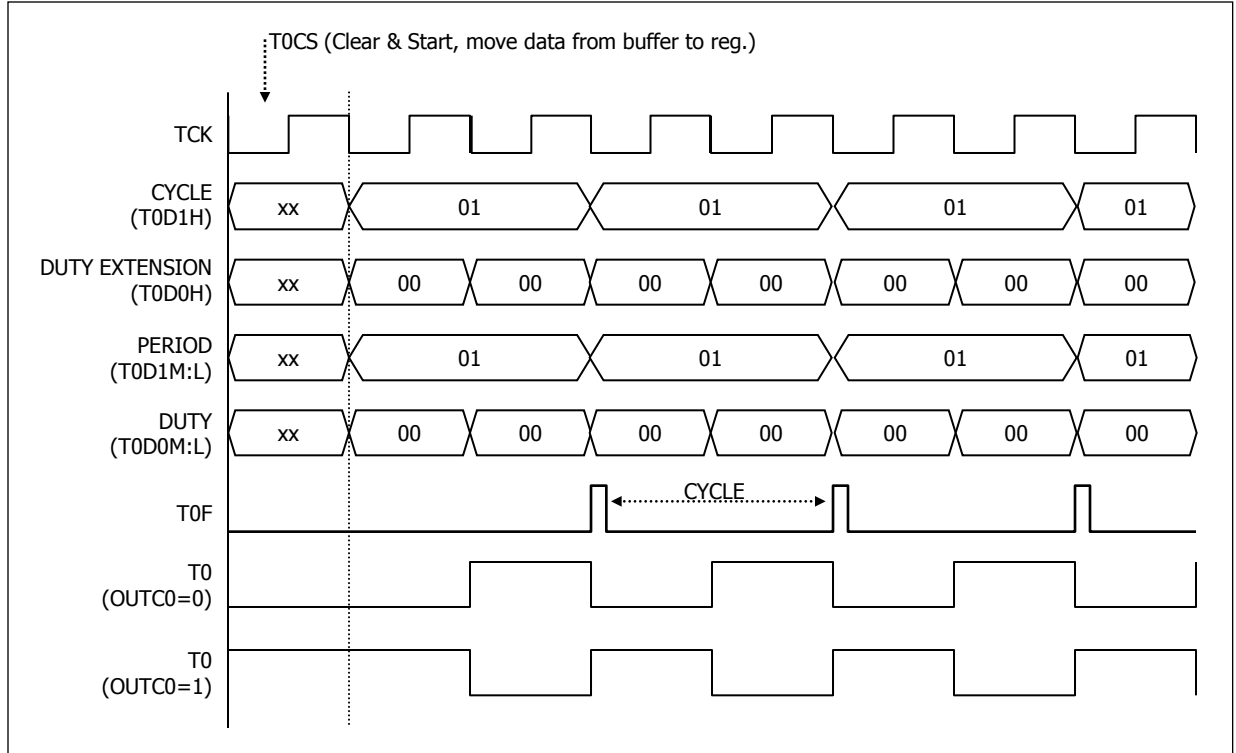
- Cycle \neq #0
- Period \neq #1
- Duty < Period
- Duty Extension < Cycle

6. Timer

• PWM mode Timing Diagram : (TOEG=0, DUTY EXTENSION=0)



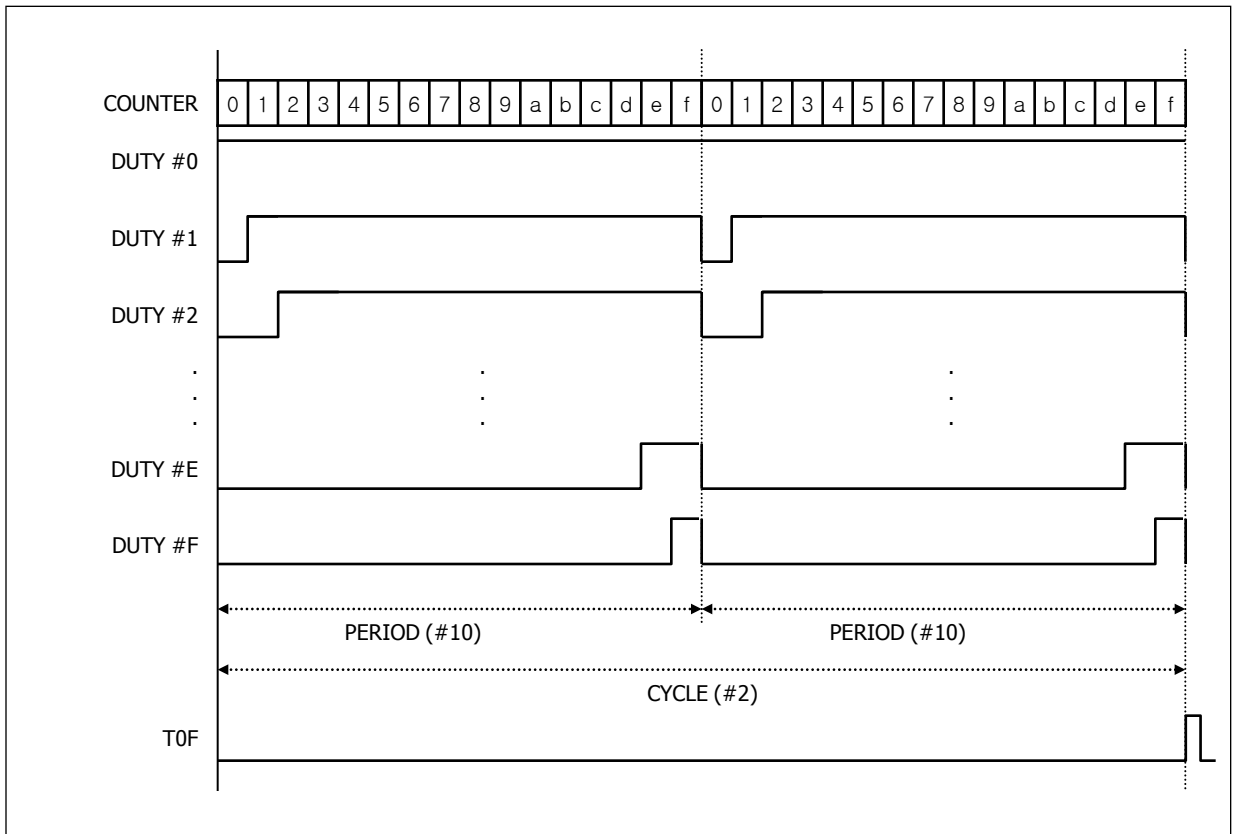
• PWM mode Timing Diagram : (TOEG=1, DUTY EXTENSION=0)



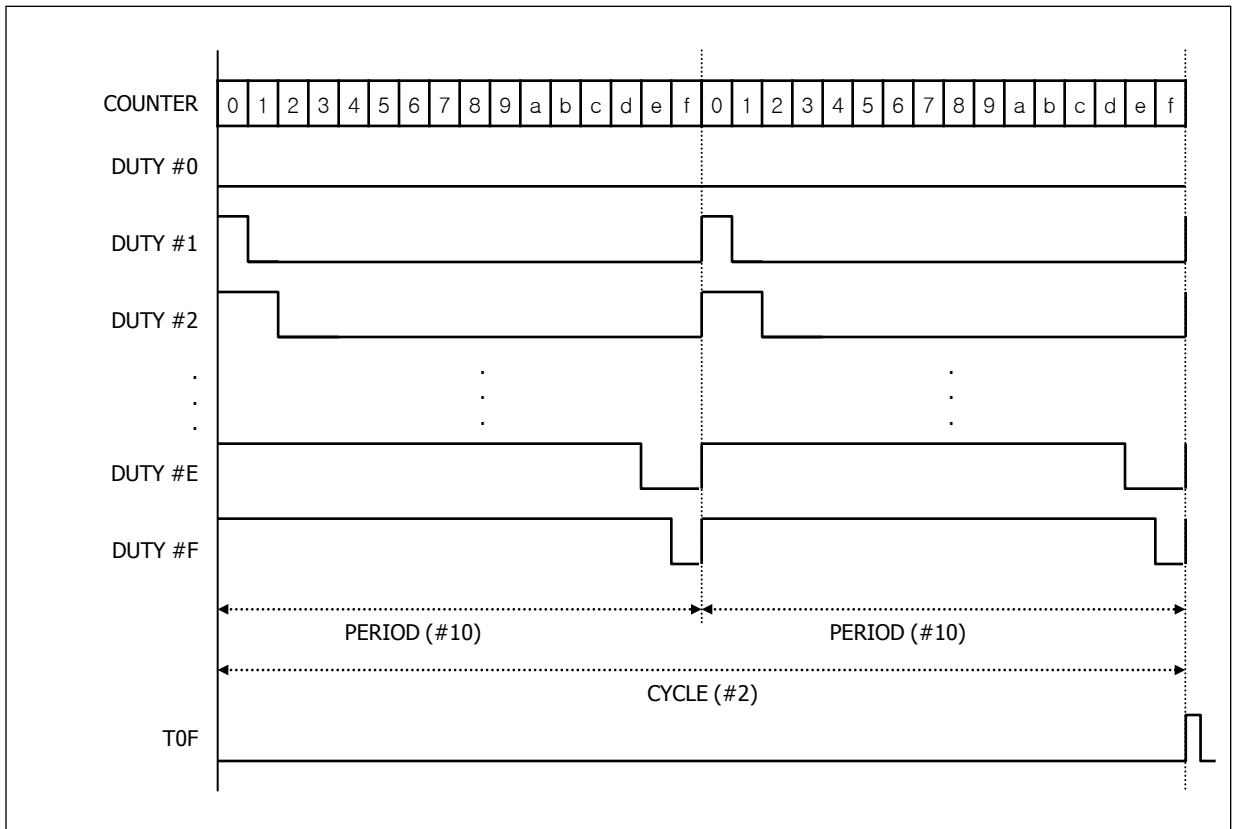
- PWM mode Condition :
 - Cycle \neq #0
 - Period \neq #1
 - Duty < Period
 - Duty Extension < Cycle

6. Timer

- T0 OUTPUT (PWM mode) Timing Diagram : (OUTC0=0, T0EG=0, DUTY EXTENSION=0)

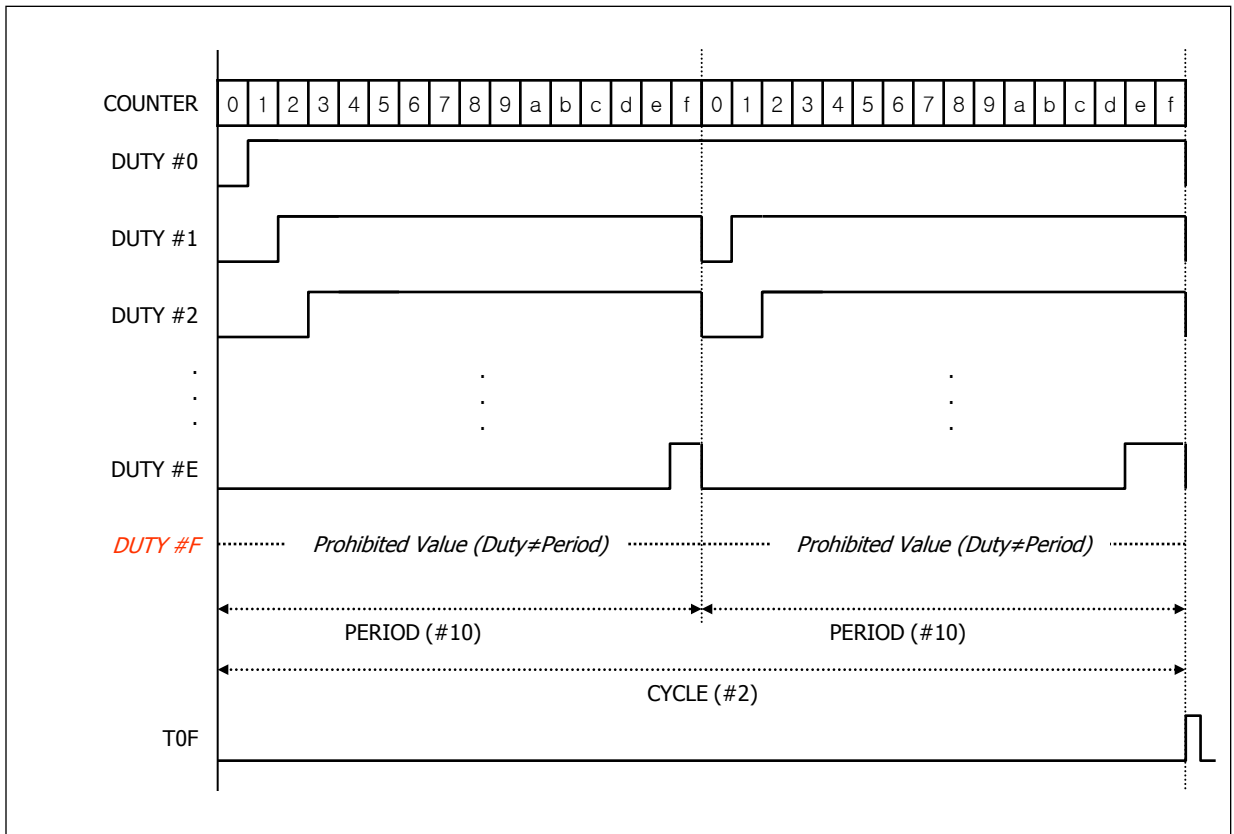


- T0 OUTPUT (PWM mode) Timing Diagram : (OUTC0=1, T0EG=0, DUTY EXTENSION=0)

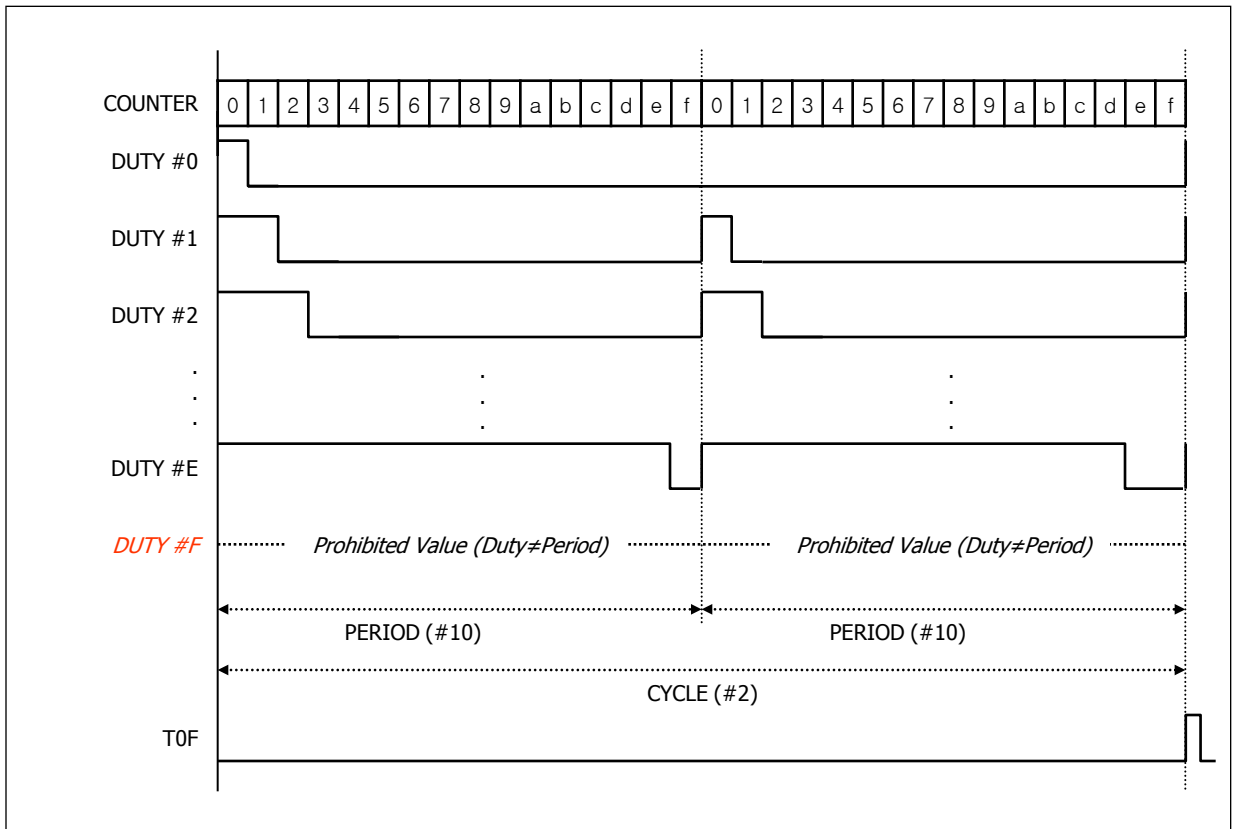


6. Timer

- T0 OUTPUT (PWM mode) Timing Diagram : (OUTC0=0, T0EG=0, DUTY EXTENSION=1)



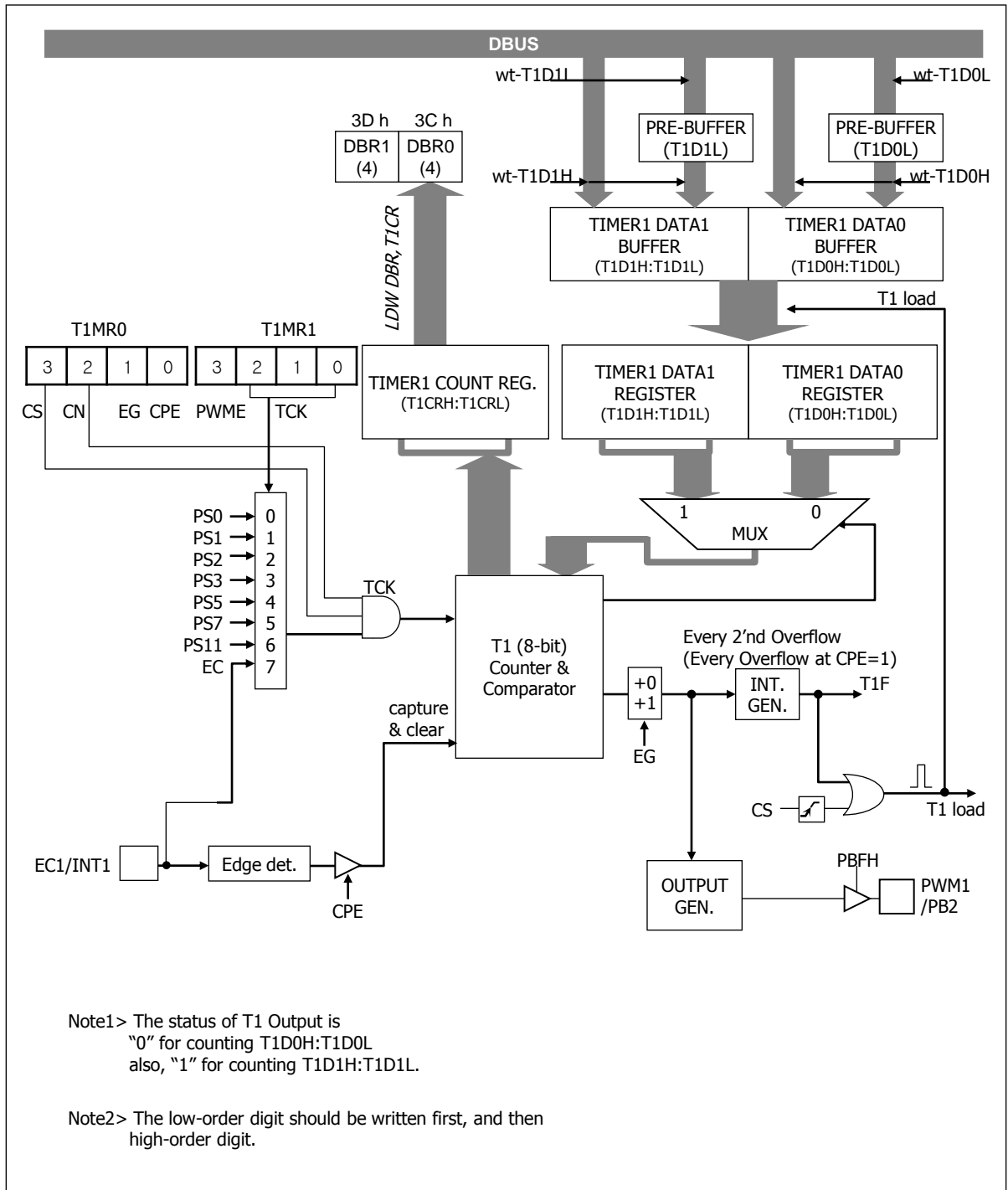
- T0 OUTPUT (PWM mode) Timing Diagram : (OUTC0=1, T0EG=0, DUTY EXTENSION=1)



6. Timer

6.3. Timer1

6.3.1. Timer1(T1) Block Diagram



6. Timer

6.3.2. Timer1 Control Register

- Timer1 Mode Register 0 (T1MR0)

	3	2	1	0	
T1MR0	T1CS	T1CN	T1EG	T1CPE	29h
initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of T1MR0

Bit Name			Selection Mode	Remarks
T1CS	Timer0 Clear / start Control	0	Timer1 Stop	
		1	Timer1 Clear and Start	
T1CN	Timer0 Pause / Continue Control	0	Timer1 Pause	
		1	Timer1 continue	
T1EG	Timer0 Count Control	0	Timer1 Count	
		1	Timer1 Count + 1	
T1CPE	Input capture Mode selection	0	Timer/Counter Mode	
		1	Capture Mode	

- Timer1 Mode Register 1 (T1MR1)

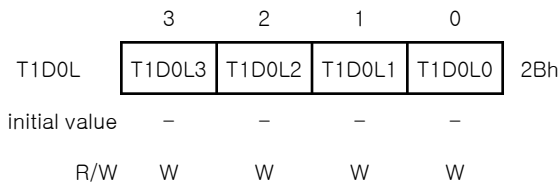
	3	2	1	0	
T1MR1	PWME1	T1CK2	T1CK1	T1CK0	2Ah
initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of T1MR1

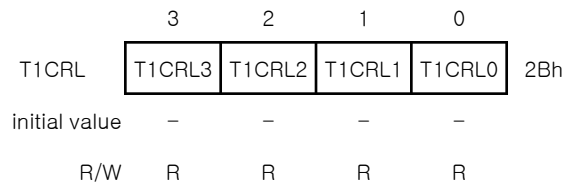
Bit Name			Selection Mode	Remarks
PWME1	Timer/PWM Mode Selection	0	Timer1 Normal Mode	
		1	Timer1 PWM Mode	
T1CK2 T1CK1 T1CK0	Input clock selection	000	PS0	
		001	PS1	
		010	PS2	
		011	PS3	
		100	PS5	
		101	PS7	
		110	PS11	
		111	EC1	

6. Timer

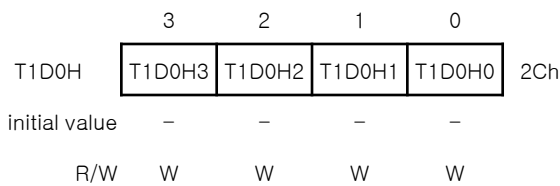
- Timer1 Data0 Register Low (T1D0L)



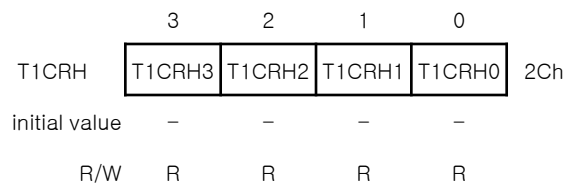
- Timer1 Count Register Low (T1CRL)



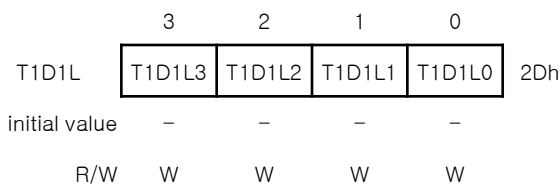
- Timer1 Data0 Register High (T1D0H)



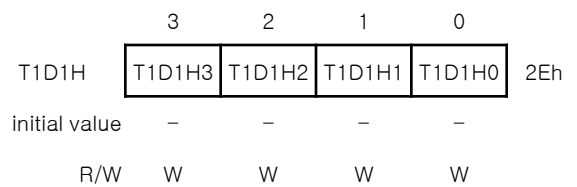
- Timer1 Count Register High (T1CRH)



- Timer1 Data1 Register Low (T1D1L)



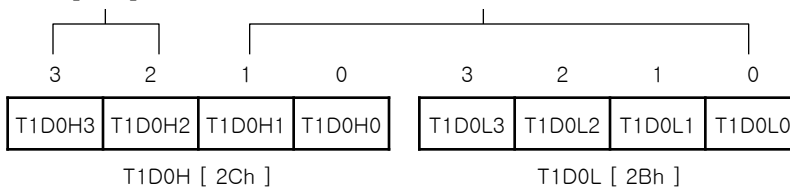
- Timer1 Data1 Register High (T1D1H)



※ PWM1 Data Registers

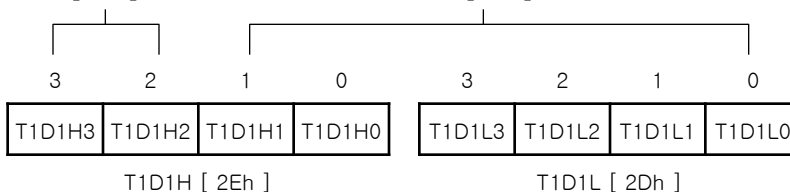
PWM1 Duty Extension (PWM1DE)
[2-bit]

PWM1 Duty (PWM1DY)
[6-bit]



PWM1 Cycle (PWM1CY)
[2-bit]

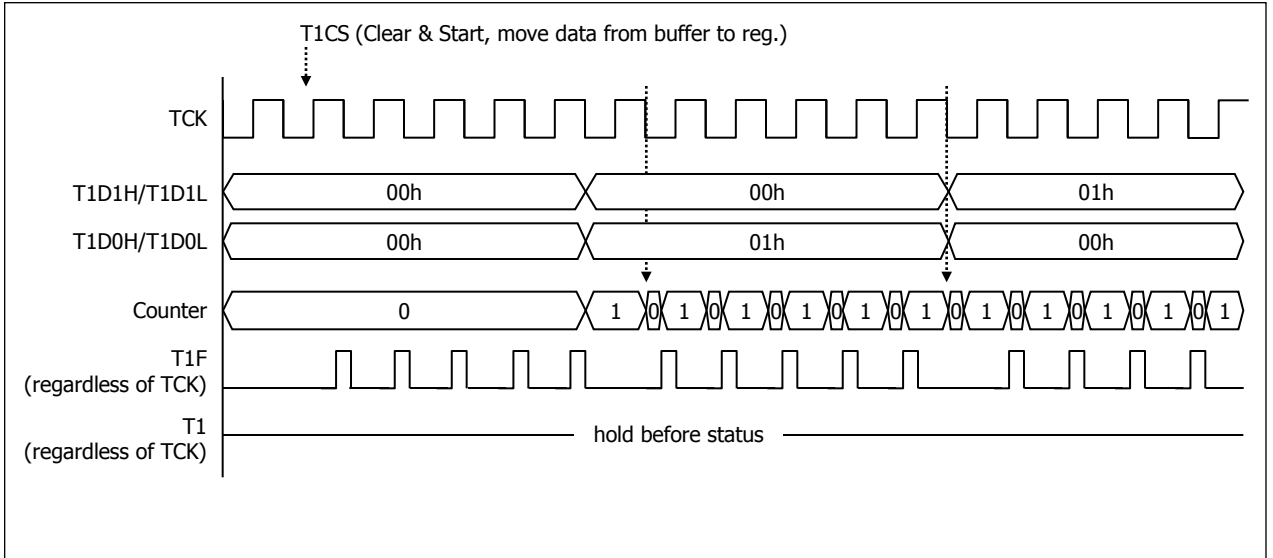
PWM1 Period (PWM1PR)
[6-bit]



6. Timer

6.3.3. Timer1 Caution

Caution : In the case of T1EG is "0",

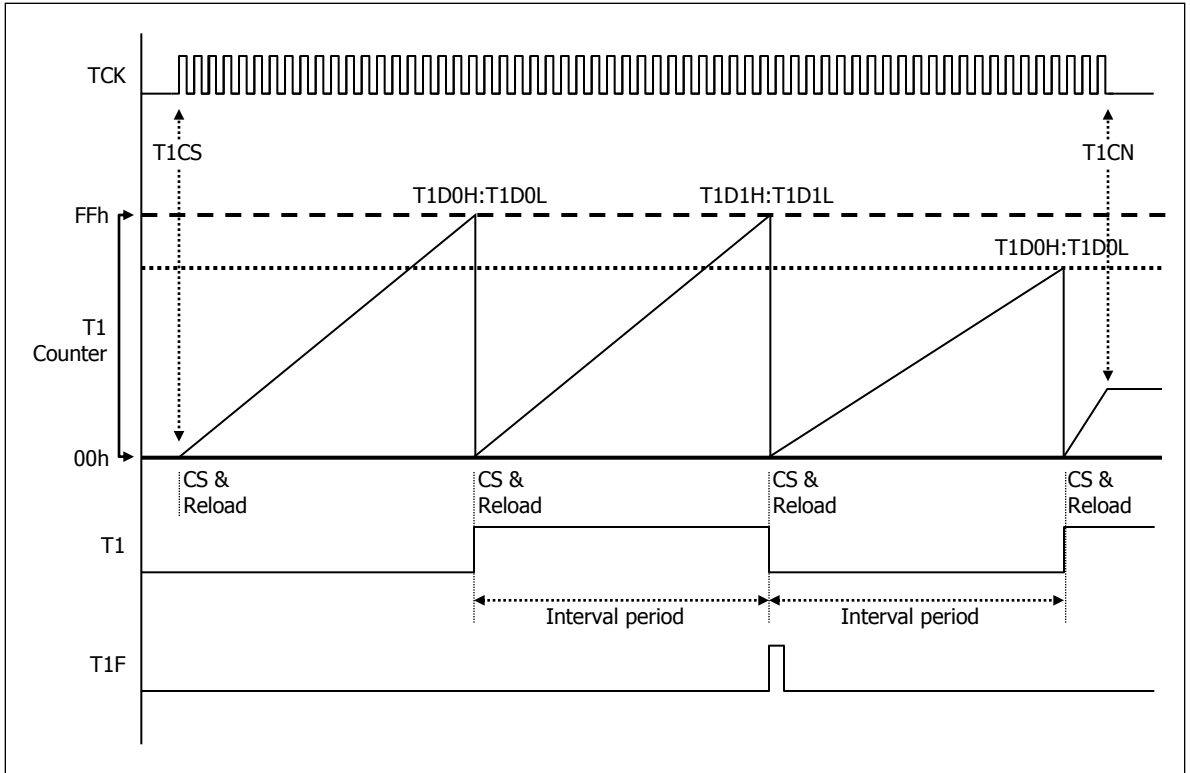


Want to count "0", set T1EG=1

6. Timer

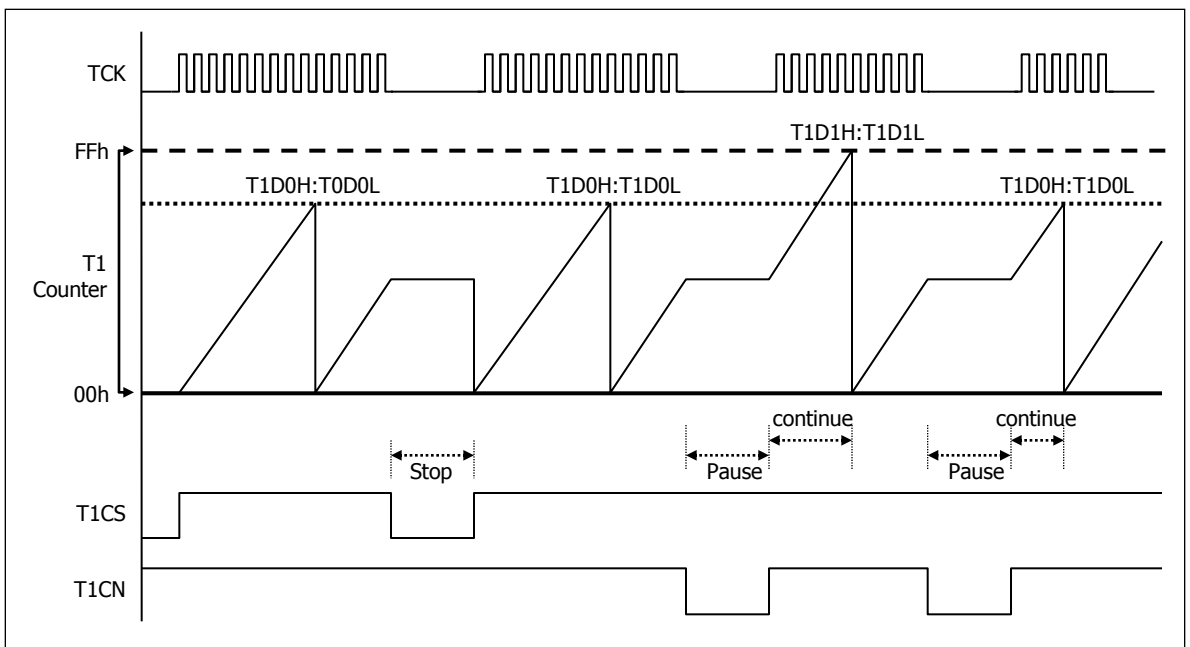
6.3.4. Timer1 Timing Diagram

* 8-bit Timer/Counter mode Timing Diagram



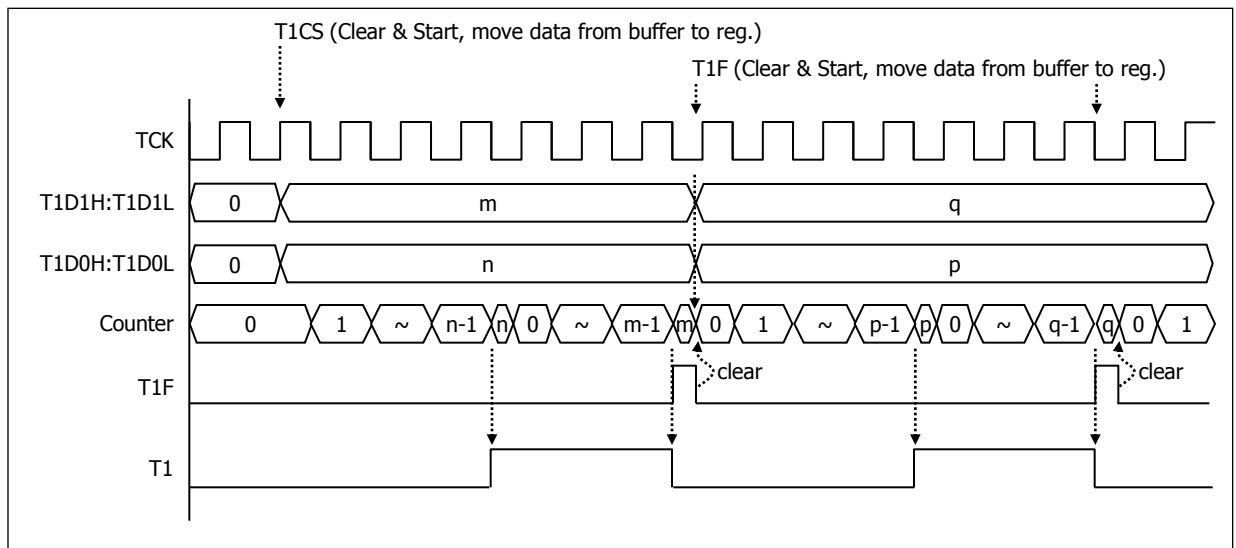
Note > CS : Timer1 Counter Clear & Start.
 Reload : Timer1 Data move from Data buffer to Data register.

* Start / Stop operation

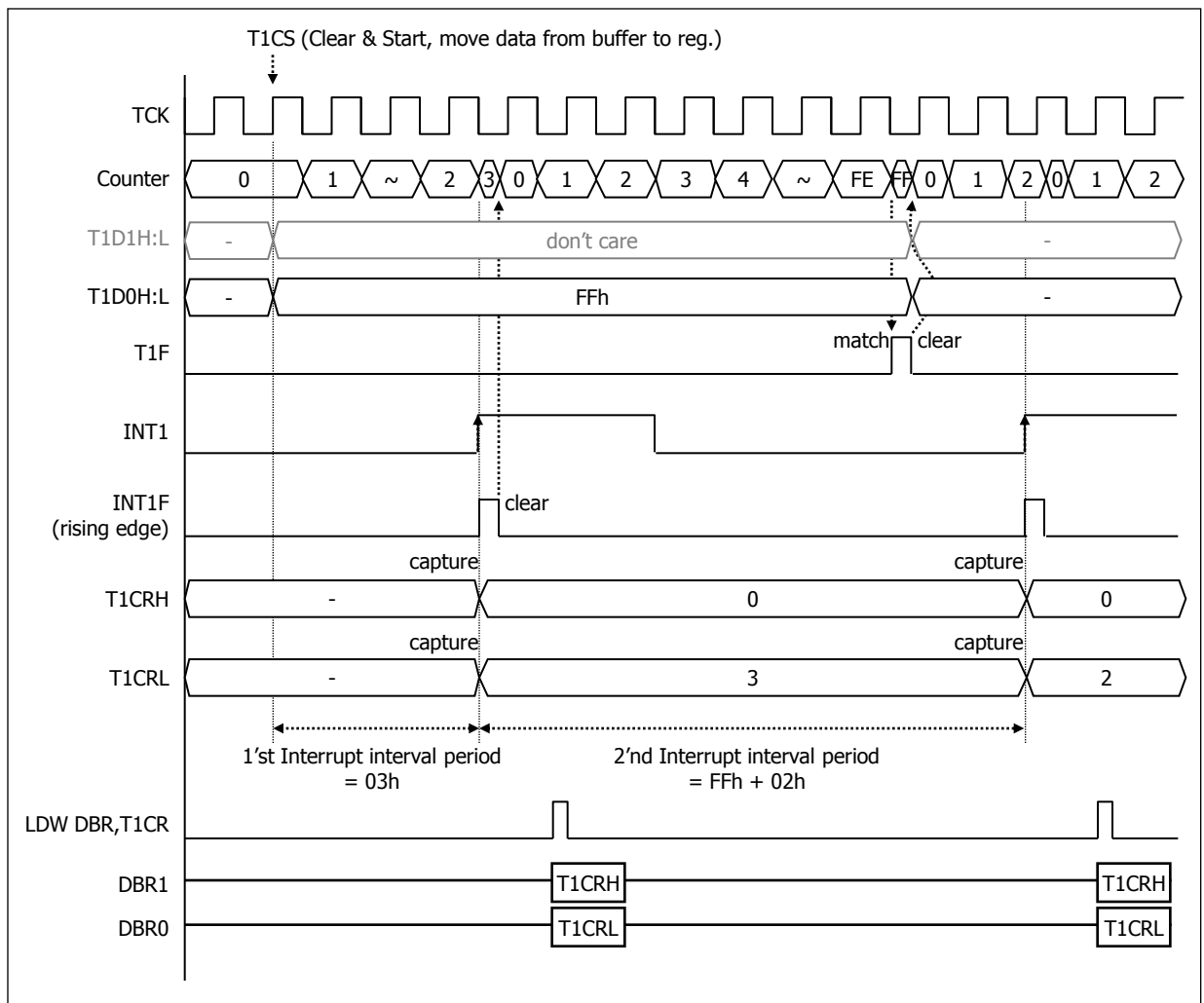


6. Timer

* 8-bit Timer/Counter mode Timing Diagram

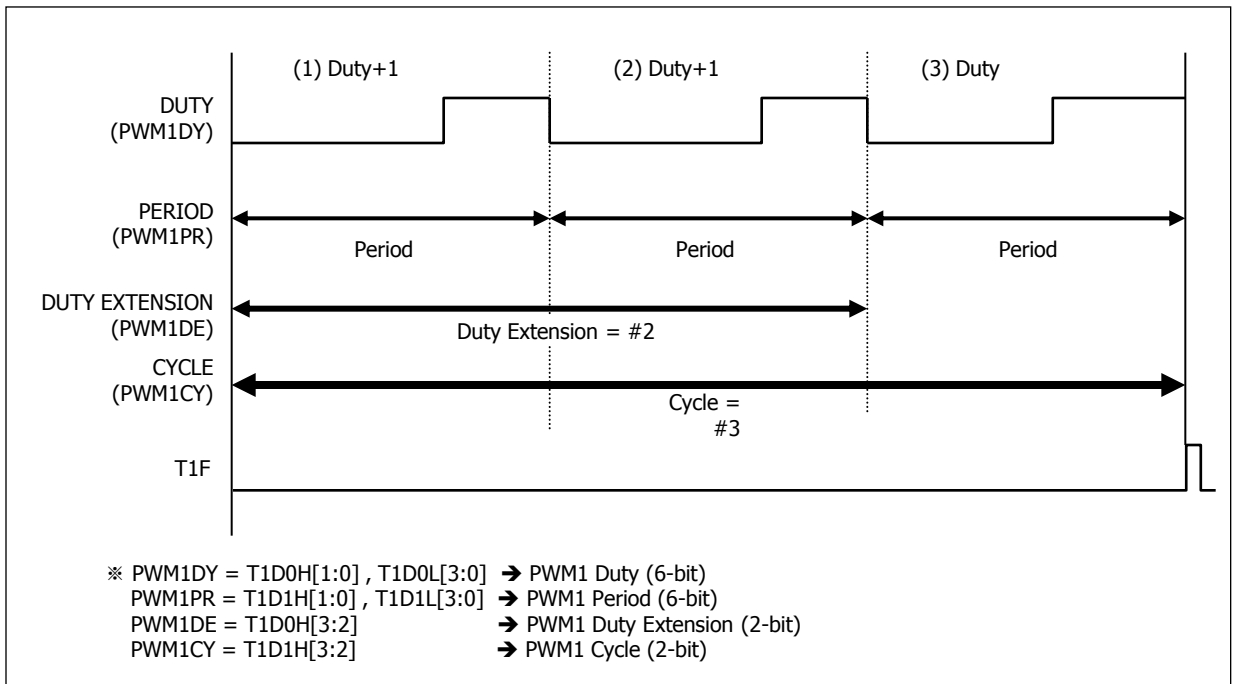


* 8-bit Capture mode Timing Diagram

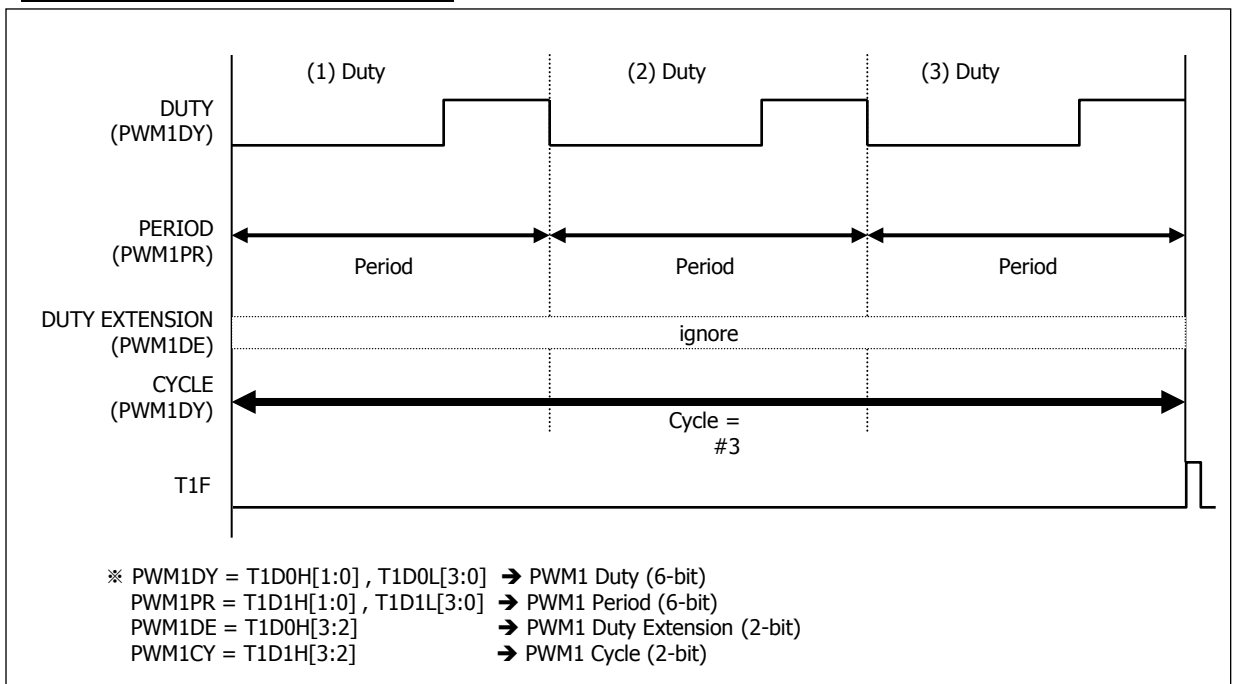


6. Timer

• PWM mode Timing Diagram : (T1EG=0)



• PWM mode Timing Diagram : (T1EG=1)

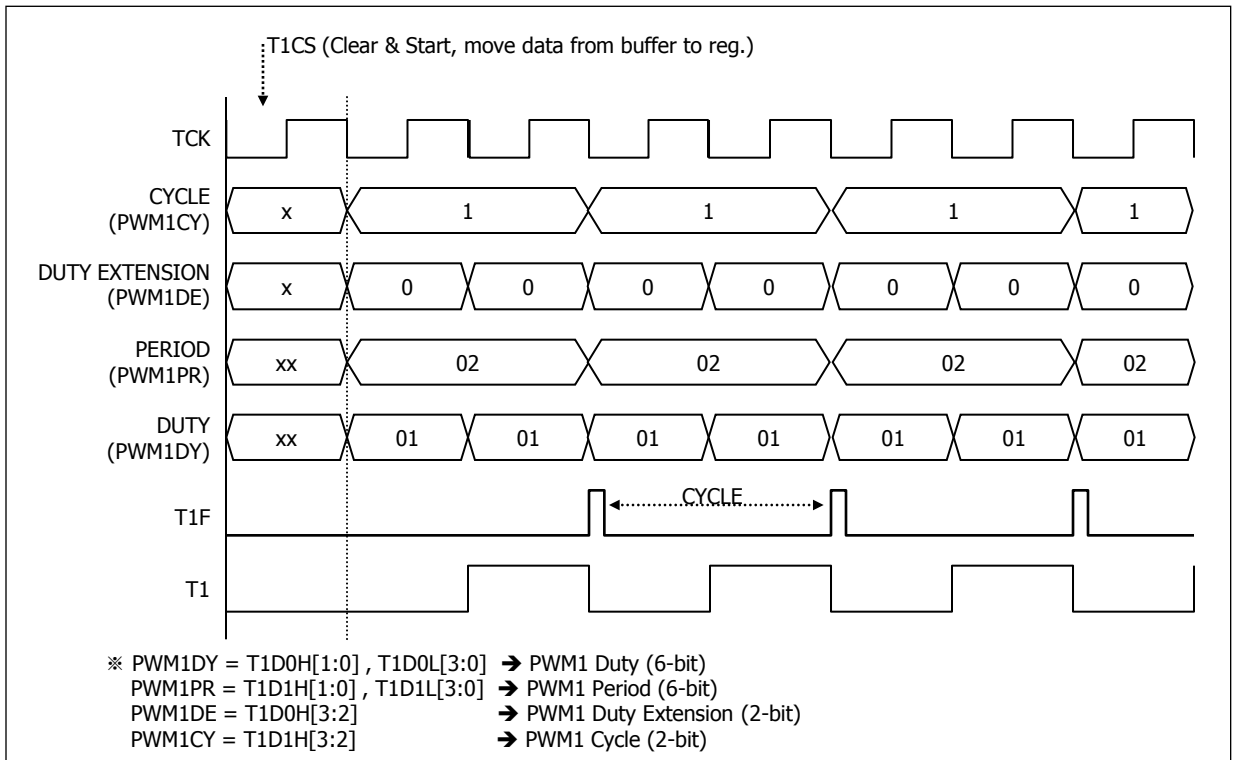


• PWM mode Condition :

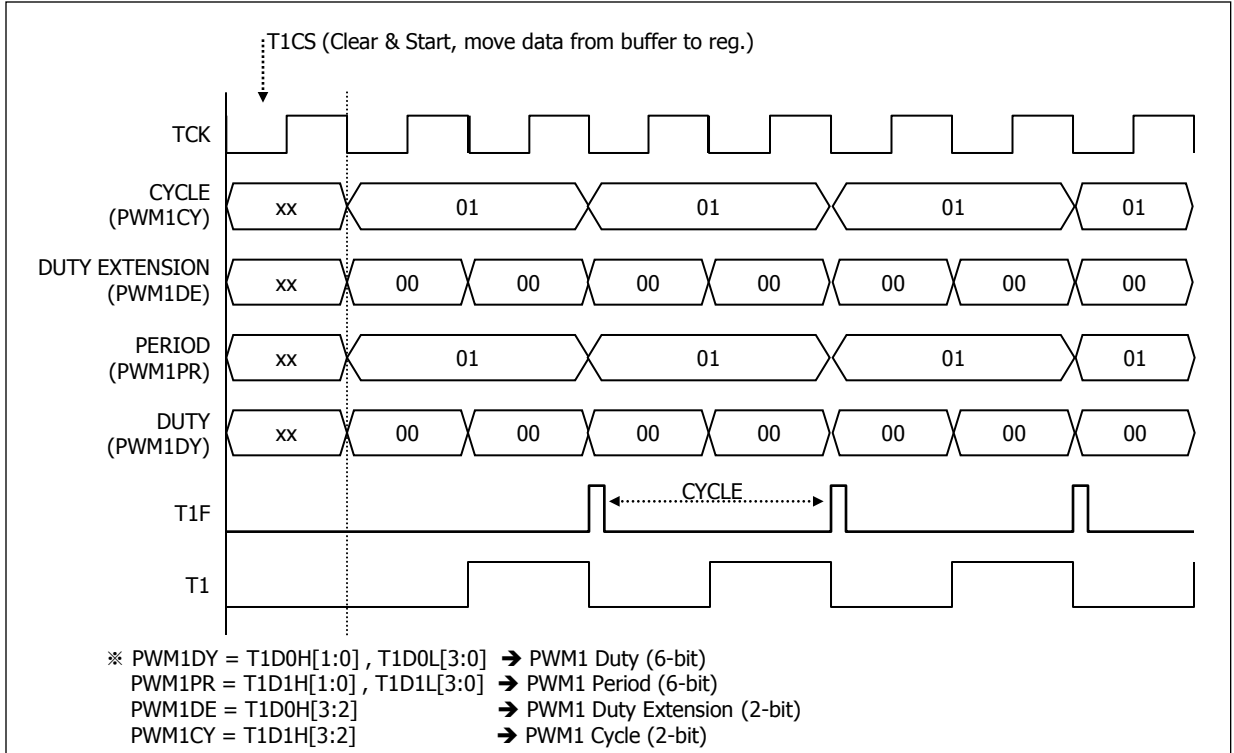
- Cycle ≠ #0
- Period ≠ #1
- Duty < Period
- Duty Extension < Cycle

6. Timer

• PWM mode Timing Diagram : (T1EG=0, DUTY EXTENSION=0)



• PWM mode Timing Diagram : (T1EG=1, DUTY EXTENSION=0)

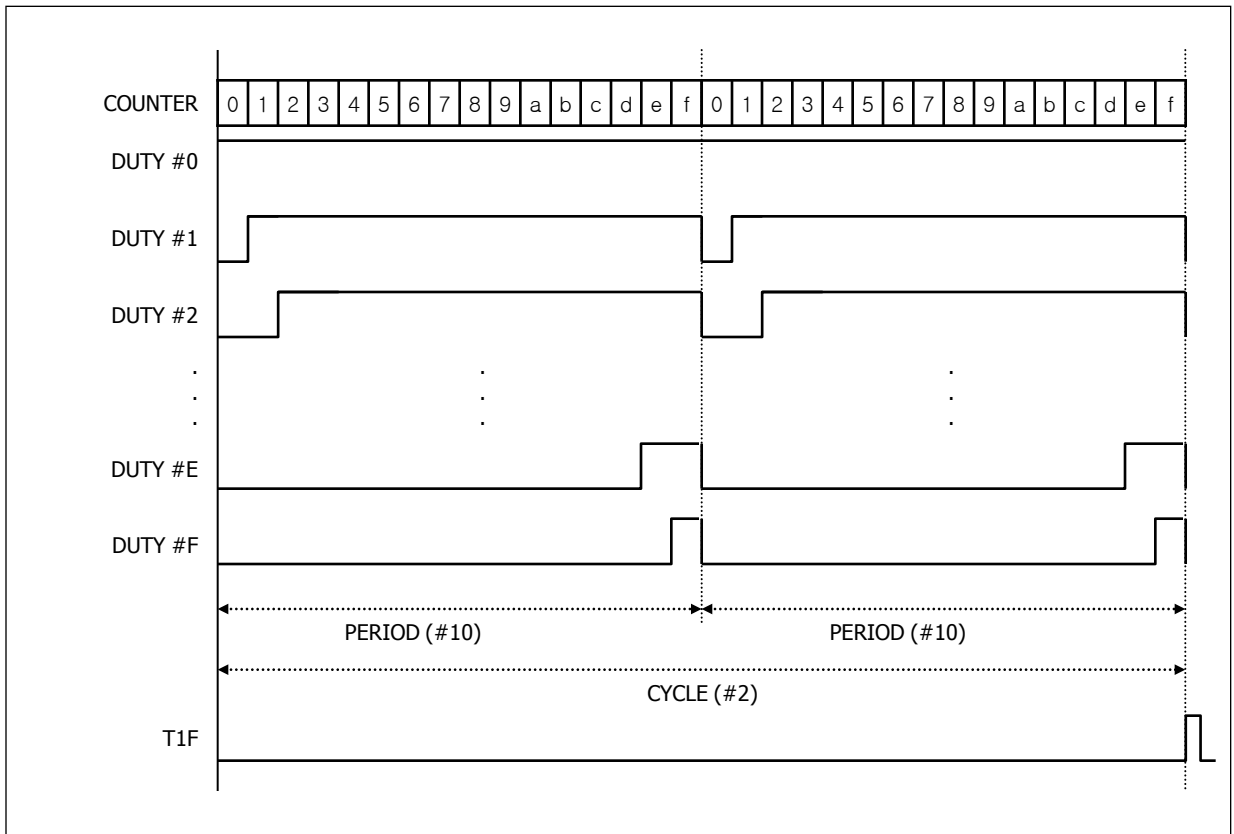


• PWM mode Condition :

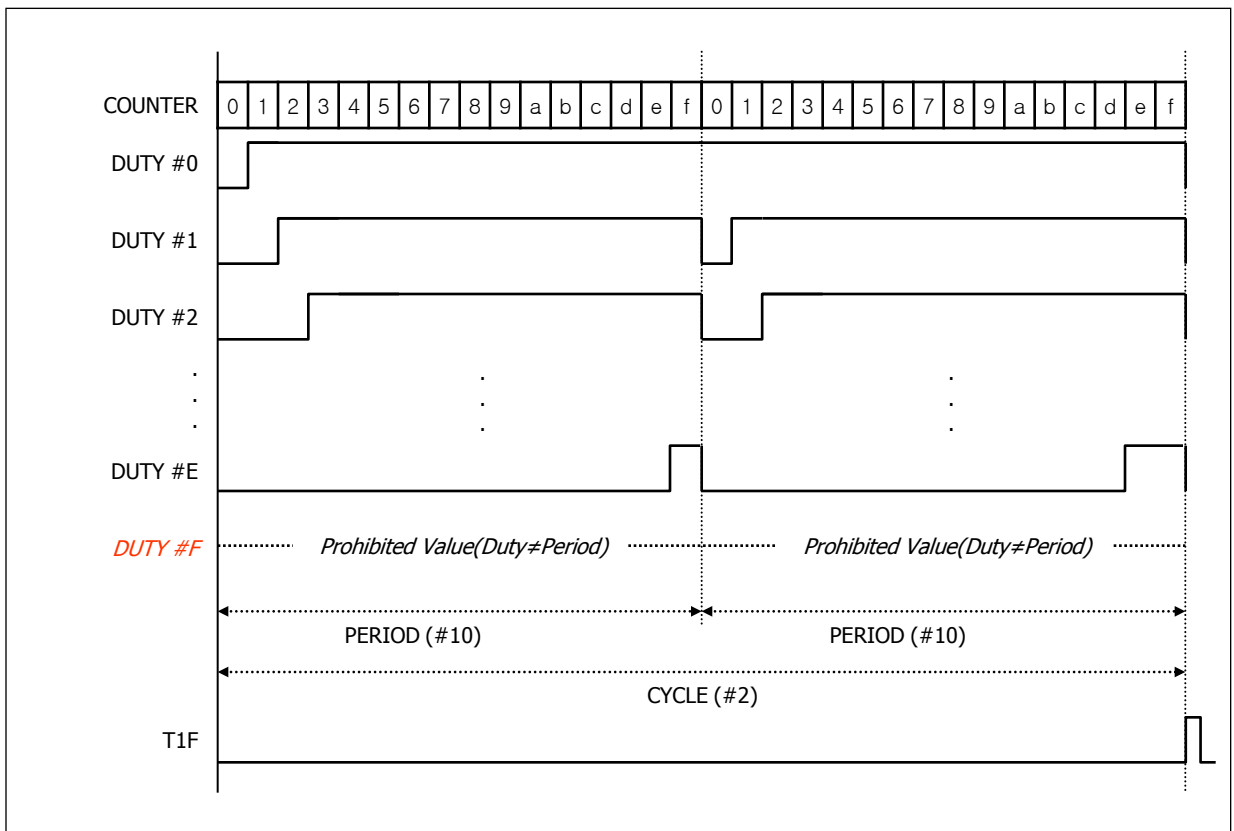
- Cycle ≠ #0
- Period ≠ #1
- Duty < Period
- Duty Extension < Cycle

6. Timer

- T1 OUTPUT (PWM mode) Timing Diagram : (T1EG=0, DUTY EXTENSION=0)



- T1 OUTPUT (PWM mode) Timing Diagram : (T1EG=0, DUTY EXTENSION=1)



7. Interrupt

The ADAM45P52XX contains 7 interrupt sources; 2 externals and 5 internals. Nested interrupt services with priority control is also possible.

- ▶ 7 interrupt source (2Ext, 2Timer, 1 A/D, 1VDI, 1WDT)
- ▶ 7 interrupt vector
- ▶ 8 level nested interrupt control is possible.
- ▶ Read of interrupt request flag are possible.
- ▶ In interrupt accept, request flag is automatically cleared.

Interrupt Enable Register (IENR0, IENR1), Interrupt Request Register (IRQ0, IRQ1) and priority circuit.

Interrupt function block diagram is shown in Fig.7.1

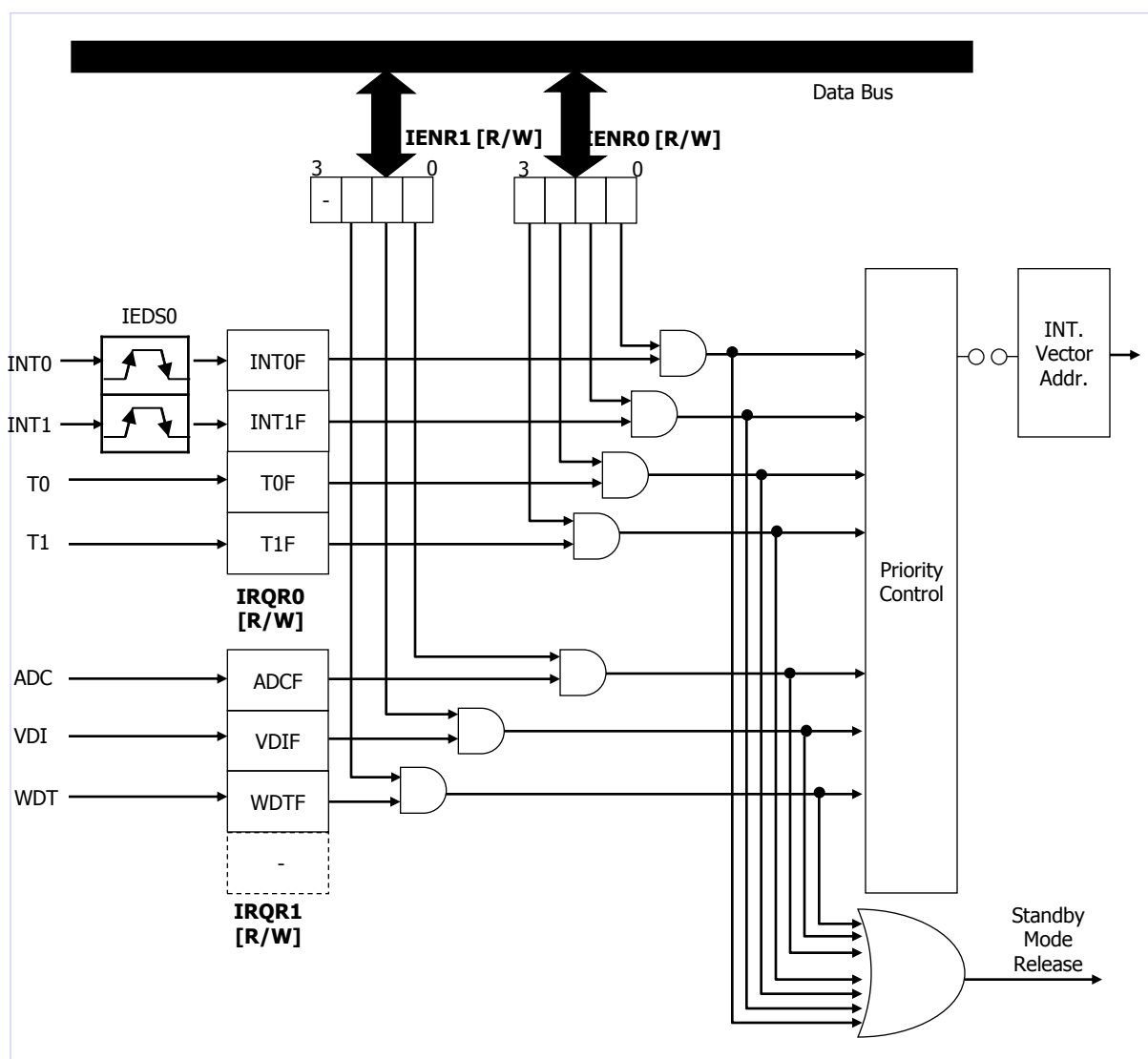


Fig.7.1 Interrupt Source

7. Interrupt

7.1. Interrupt Source

Each interrupt vector is independent and has its own priority.

	Mask	Priority	Interrupt Source	INT Vector Addr.
Hardware Interrupt	Non-maskable	–	RESET	0000h
	maskable	1	INT0 (External Interrupt 0)	0002h
		2	INT1 (External Interrupt 1)	0004h
		3	T0 (Timer0)	0006h
		4	T1 (Timer1)	0008h
		5	ADC (Analog Digital Converter)	000Ah
		6	VDI (Voltage Detection Indicator)	000Ch
		7	WDT (Watch-Dog Timer)	000Eh

Table 7.1 Interrupt Source

7.2. Interrupt Control Register

I flag of SFR is a interrupt mask enable flag. When I flag = ``0``, all interrupts become disable. When I flag = ``1``, interrupts can be selectively enabled and disabled by contents of corresponding Interrupt Enable Register(IENR0, IENR1).

When interrupt is occurred, interrupt request flag is set, and Interrupt request is detected at the edge of interrupt signal. The accepted interrupt request flag is automatically cleared during interrupt cycle process. The interrupt request flag maintains ``1`` until the interrupt is accepted or is cleared in program. In reset state, interrupt request flag register (IRQR0,IRQR1) is cleared to ``0``.

It is possible to read the state of interrupt register and to manipulate the contents of register.

• External Interrupt Edge selection Register 0 (IEDS0)

	3	2	1	0	
IEDS0	IED1H	IED1L	IED0H	IED0L	1Ah
initial value	0	0	0	0	
R/W	W	W	W	W	

Bit Name	Selection Mode		Remarks
IED1H IED1L	00	–	INT1
	01	Falling Edge Selection (1-to-0 transition)	
	10	Rising Edge Selection (0-to-1 transition)	
	11	Both Edge Selection (Falling & Rising)	
IED0H IED0L	00	–	INT0
	01	Falling Edge Selection (1-to-0 transition)	
	10	Rising Edge Selection (0-to-1 transition)	
	11	Both Edge Selection (Falling & Rising)	

7. Interrupt

• Interrupt Enable Register 0 (IENR0)

	3	2	1	0	
IENR0	T1E	T0E	INT1E	INT0E	1Eh
initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of IENR0

Bit Name	Selection Mode		Remarks
T1E	1	Timer1 Interrupt enable	
T0E	1	Timer0 Interrupt enable	
INT1E	1	External Interrupt 1 enable	
INT0E	1	External Interrupt 0 enable	

• Interrupt Enable Register 1 (IENR1)

	3	2	1	0	
IENR1	-	WDTE	VDIE	ADCE	1Fh
initial value	0	0	0	0	
R/W	-	R/W	R/W	R/W	

Selection Mode of IENR1

Bit Name	Selection Mode		Remarks
-	-	-	
WDTE	1	WDT Timer overflow Interrupt enable	
VDIE	1	Voltage Detection Interrupt enable	
ADCE	1	ADC Interrupt enable	

7. Interrupt

• Interrupt Request Flag Register (IRQR0)

	3	2	1	0	
IRQR0	T1F	T0F	INT1F	INT0F	1Ch
initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of IRQR0

Bit Name	Selection Mode		Remarks
T1F	1	Timer1 Interrupt Request Flag enable	
T0F	1	Timer0 Interrupt Request Flag enable	
INT1F	1	External Interrupt 1 Request Flag enable	
INT0F	1	External Interrupt 0 Request Flag enable	

• Interrupt Request Flag Register (IRQR1)

	3	2	1	0	
IRQR1	-	WDTF	VDIF	ADCF	1Dh
initial value	0	0	0	0	
R/W	-	R/W	R/W	R/W	

Selection Mode of IRQR1

Bit Name	Selection Mode		Remarks
-	-	-	
WDTF	1	WDT Timer overflow Interrupt Flag enable	
VDIF	1	Voltage Detection Interrupt Flag enable	
ADCF	1	ADC Interrupt Flag enable	

7. Interrupt

7.3. Interrupt Timing

Interrupt Request Sampling Time :

- Maximum 2 machine cycle (When execute LDW @ABR Instruction)
- Minimum 0 machine cycle

Interrupt preprocess step is 1 machine cycle

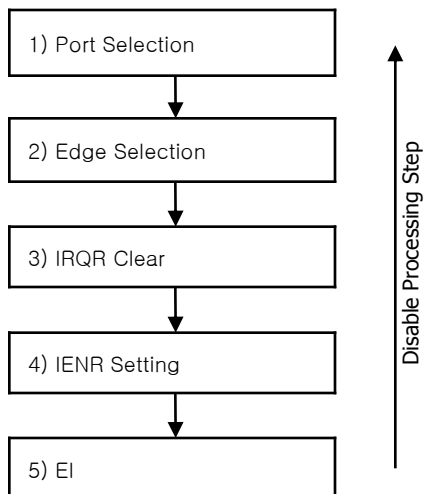
7.4. The valid timing after executing Interrupt control instructions

I flag is valid just after executing of EI/DI on the contrary.

7.5. Multiple Interrupt

If there is an interrupt, Interrupt Mask Enable Flag is automatically cleared before entering the Interrupt Service Routine. After then, no interrupt is accepted. If EI instruction is executed, interrupt mask enable bit becomes "1", and each enable bit can accept interrupt request. When two or more interrupts are generated simultaneously, the highest priority interrupt is accepted.

Key-Scan or External Interrupt Enable Processing Step



7. Interrupt

7.6. Interrupt Processing Sequence

When an interrupt is accepted, the on-going process is stopped and the interrupt service routine is executed. After the interrupt service routine is completed it is necessary to restore everything to the state before the interrupt occurred.

As soon as an interrupt is accepted, the content of the program counter is saved in the stack register which is 8 level stack area, and the contents of status flag register (SFR) is saved on the interrupt stack register (INTSK) which is 8 level stack area.

At the same time, the content of the vector address corresponding to the accepted interrupt, which is in the interrupt vector table, enters into the program counter and interrupt service is executed. In order to execute the interrupt service routine, it is necessary to write the jump addresses in the vector table corresponding to each interrupt.

Interrupt Processing Step

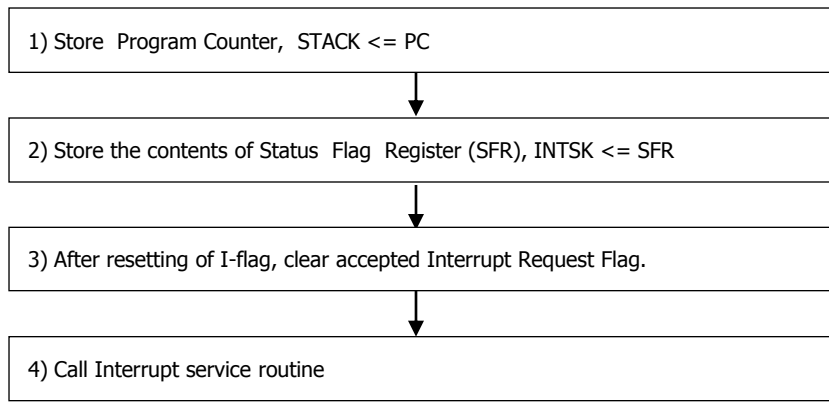
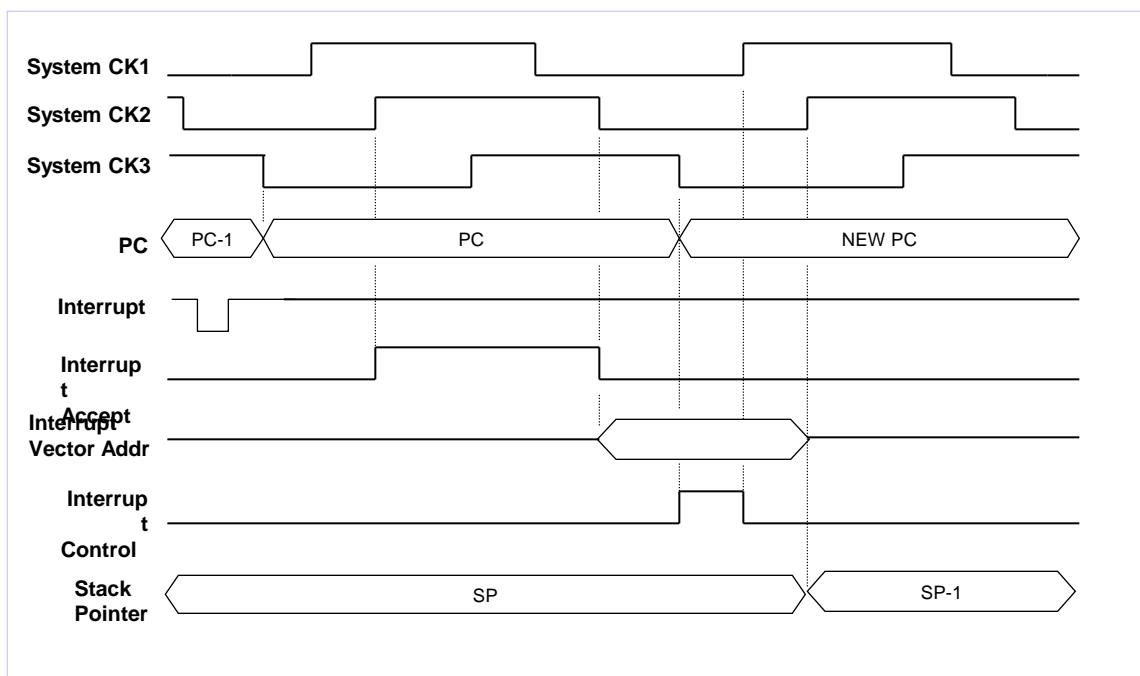


Fig.7.2 Interrupt Processing Step Timing



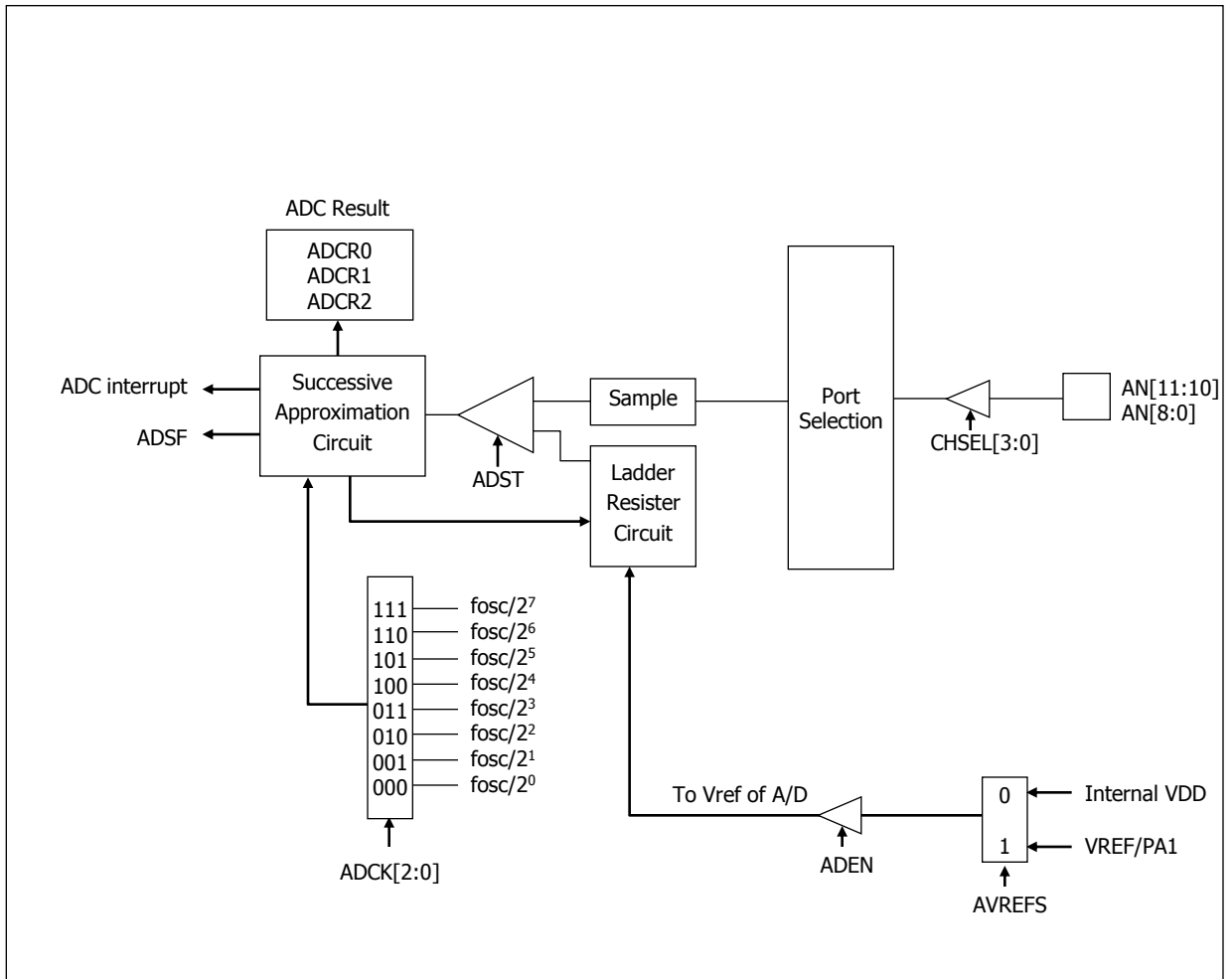
8. Analog to Digital Converter

The analog-to-digital (A/D) converter allows conversion of an analog input signal to a corresponding digital number. The A/D module has 11 selectable analog inputs. The output of sample is the input into converter, which generates the result via successive approximation.

The A/D module has four registers. These registers are

- A/D CONVERTER MODE REG 0.(ADCM0)
- A/D CONVERTER MODE REG 1.(ADCM1)
- A/D CONVERTER INPUT SELECTION REG 2.(ADCIS)
- A/D CONVERTER DATA REG 0.(ADCR0)
- A/D CONVERTER DATA REG 1.(ADCR1)
- A/D CONVERTER DATA REG 2.(ADCR2)

Fig.8.1 A/D Converter Block Diagram



8. Analog to Digital Converter

8.1. A/D Converter Control Registers

- A/D Converter Mode Register (ADCM0)

	3	2	1	0	
ADCM0	-	ADEN	ADST	ADSF	34h
initial value	0	0	0	1	
R/W	-	R/W	R/W	R	

Selection Mode of ADCM0

Bit Name	Selection Mode		Remarks
ADEN	0	ADC Disable	if (STOP) ADEN go to "L"
	1	ADC Enable	
ADST	0	A/D Conversion is Stop	
	1	A/D Conversion is Start. and cleared to "L" after 1 cycle	
ADSF	0	A/D Conversion is Processing	
	1	A/D Conversion is Completed	

- A/D Converter Mode Register (ADCM1)

	3	2	1	0	
ADCM1	ADCK2	ADCK1	ADCK0	AVREFS	35h
initial value	0	0	0	0	
R/W	W	W	W	W	

Selection Mode of ADCM1

Bit Name	Selection Mode		Remarks
ADCK[2:0]	000	PS0 ($2^0/f_{OSC}$)	
	001	PS1 ($2^1/f_{OSC}$)	
	010	PS2 ($2^2/f_{OSC}$)	
	011	PS3 ($2^3/f_{OSC}$)	
	100	PS4 ($2^4/f_{OSC}$)	
	101	PS5 ($2^5/f_{OSC}$)	
	110	PS6 ($2^6/f_{OSC}$)	
	111	PS7 ($2^7/f_{OSC}$)	
AVREFS	0	Internal VDD for ADC power	
	1	VREF(/PA1) for ADC power	

8. Analog to Digital Converter

• A/D Converter Input Selection Register (ADCIS)

	3	2	1	0	
ADCIS	CHSEL3	CHSEL2	CHSEL1	CHSEL0	36h
initial value	0	0	0	0	
R/W	W	W	W	W	

Selection Mode of ADCIS

Bit Name	Selection Mode		Remarks
CHSEL[3:0]	0000	Channel 0 Selection	if analog port selected
	0001	Channel 1 Selection	
	0010	Channel 2 Selection	
	0011	Channel 3 Selection	
	0100	Channel 4 Selection	
	0101	Channel 5 Selection	
	0110	Channel 6 Selection	
	0111	Channel 7 Selection	
	1000	Channel 8 Selection	
	1001	<i>Prohibit</i>	
	1010	Channel 10 Selection	
	1011	Channel 11 Selection	
	1100	<i>Prohibit</i>	
	1101	<i>Prohibit</i>	
	1110	<i>Prohibit</i>	
	1111	<i>Prohibit</i>	

• A/D Converter Data Register 0 (ADCR0)

	3	2	1	0	
ADCR0	ADCR03	ADCR02	ADCR01	ADCR00	35h
initial value	-	-	-	-	
R/W	R	R	R	R	

• A/D Converter Data Register 1 (ADCR1)

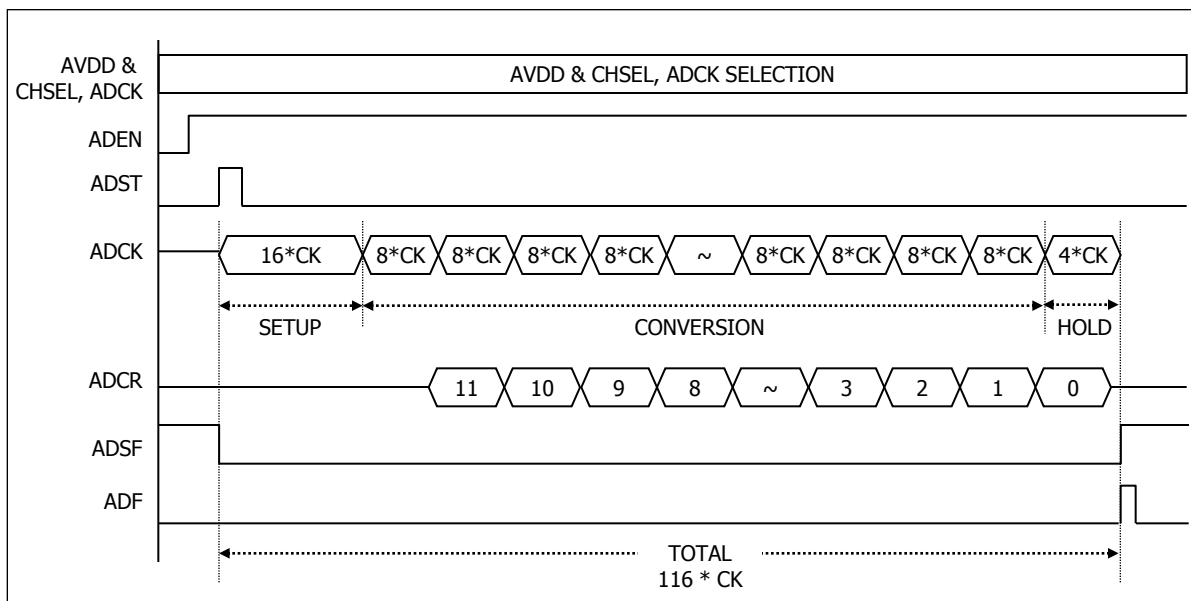
	3	2	1	0	
ADCR1	ADCR07	ADCR06	ADCR05	ADCR04	36h
initial value	-	-	-	-	
R/W	R	R	R	R	

• A/D Converter Data Register 2 (ADCR2)

	3	2	1	0	
ADCR2	ADCR11	ADCR10	ADCR09	ADCR08	37h
initial value	-	-	-	-	
R/W	R	R	R	R	

8. Analog to Digital Converter

ADC Timing Diagram



- Total Conversion Time is

$$(16 + 8*12 + 4) * ADCK$$

freq = 4MHz

Bit Name	Selection Mode			Remarks
ADCK	000	Conversion Source Clock ($1/f_{osc}$)	$116 * 250ns = 29us$	
	010	Conversion Source Clock ($2^2/f_{osc}$)	$116 * 1us = 116us$	

8. Analog to Digital Converter

8.2. A/D Converter Caution

8.2.1. Noise Countermeasures of AN[11:10], AN[8:0]

It is recommend that a capacitor be connected externally as shown Fig.8.2 in order to reduce noise.

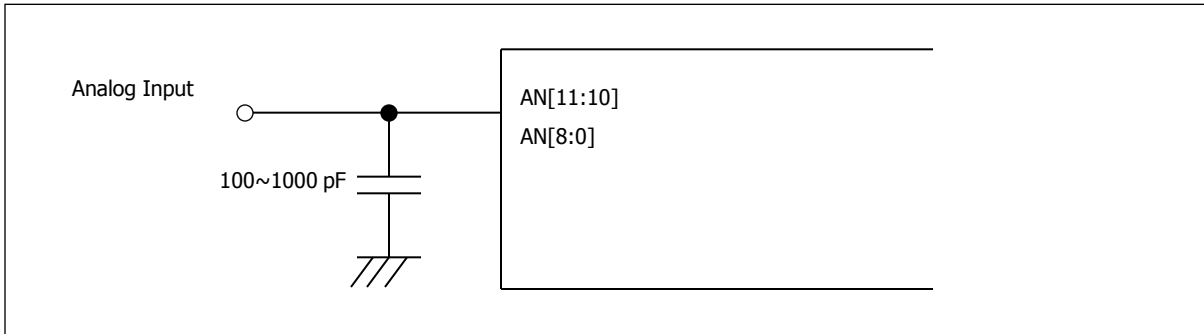


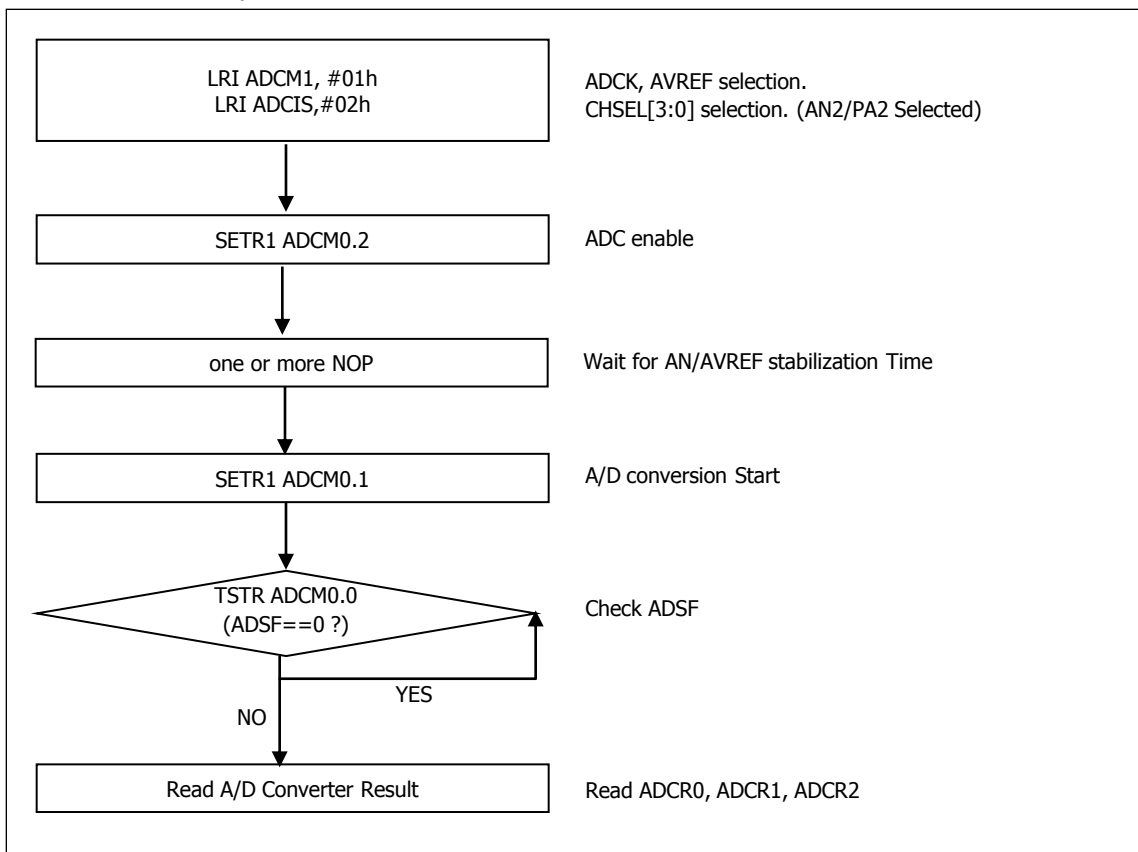
Fig.8.2 Analog input pin Connecting capacitor

8.2.2. VREF pin input impedance

A series resistor string of approximately 100kΩ~150kΩ is connected between VREF pin and VSS.

If the output impedance of VREF is high, it will result in parallel connection to the series resistor between VREF pin and GND, and there will be a large reference voltage error.

8.3. A/D Converter Operation Flow



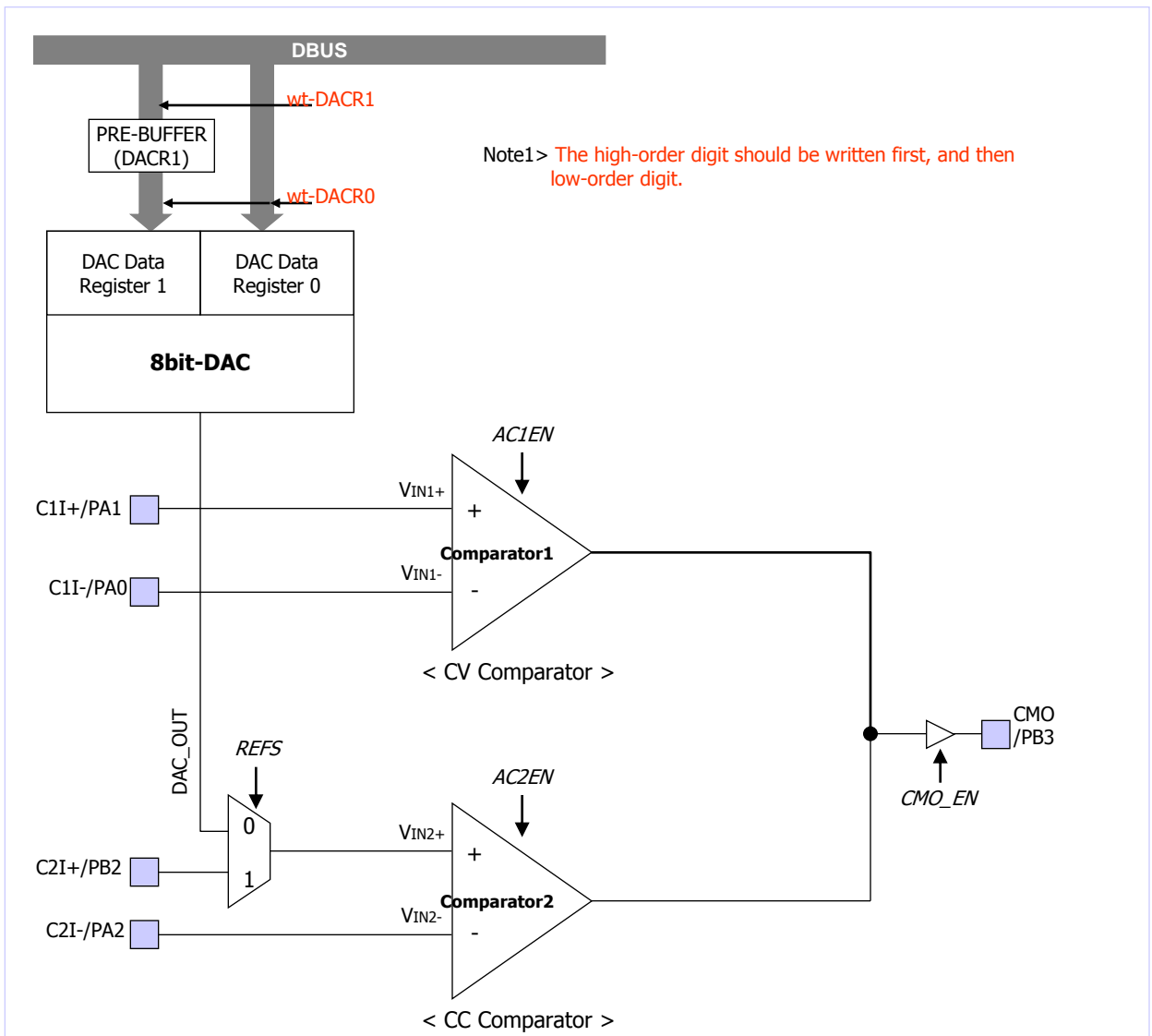
9. Analog Comparator

Analog comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. The analog comparators have 2 external analog inputs. Additionally, the analog comparator-2 has a programmable reference input with a 8-bit D/A comparator output. Two Analog comparators have one multiplexed output externally which has an open drain NMOS output.

The Analog Comparators has four registers. These registers are

- Analog Comparator MODE REG 1.(ACMR1)
- Analog Comparator MODE REG 2.(ACMR2)
- D/A CONVERTER DATA REG 0.(DACR0)
- D/A CONVERTER DATA REG 1.(DACR1)

Fig.9.1 Analog Comparator Block Diagram



* Output Status vs. Input Conditions

Input Condition	CMO
$V_{IN1-} > V_{IN1+}, V_{IN2-} > V_{IN2+}$	0
$V_{IN1-} > V_{IN1+}, V_{IN2-} < V_{IN2+}$	0
$V_{IN1-} < V_{IN1+}, V_{IN2-} > V_{IN2+}$	0
$V_{IN1-} < V_{IN1+}, V_{IN2-} < V_{IN2+}$	1

9. Analog Comparator

9.1. Analog Comparator Mode Registers

- Analog Comparator Mode Register-1 (ACMR1)

	3	2	1	0	
ACMR1	AC2EN	AC1EN	REFS	CMOEN	16h
initial value	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of ACMR1

Bit Name	Selection Mode		Remarks
AC2EN	0	Analog Comparator-2 Disable	
	1	Analog Comparator-2 Enable	
AC1EN	0	Analog Comparator-1 Disable	
	1	Analog Comparator-1 Enable	
REFS	0	Internal Reference with DAC output for the reference of Analog Comparator-2.	
	1	External Reference(C2I+) for the reference of Analog Comparator-2.	
CMOEN	0	Analog Comparator output Disable	
	1	Analog Comparator output Enable	

- Analog Comparator Mode Register-2 (ACMR2)

	3	2	1	0	
ACMR2	DACEN	-	AC2F	AC1F	17h
initial value	0	0	0	0	
R/W	R/W	-	R	R	

Selection Mode of ACMR2

Bit Name	Selection Mode		Remarks
DACEN	0	DAC Disable	
	1	DAC Enable	
-	0	-	
	1	-	
AC2F	0	if CIN2- < CIN2+	
	1	if CIN2- > CIN2+	
AC1F	0	if CIN1- < CIN1+	
	1	if CIN1- > CIN1+	

9. Analog Comparator

9.2. DAC Data Registers

- D/A Converter Data Register-1 (DACR1)

	3	2	1	0	
DACR1	DACR07	DACR06	DACR05	DACR04	19h
initial value	-	-	-	-	
R/W	W	W	W	W	

- D/A Converter Data Register-0 (DACR0)

	3	2	1	0	
DACR0	DACR03	DACR02	DACR01	DACR00	18h
initial value	-	-	-	-	
R/W	W	W	W	W	

10. Power-Down Function

In power-down mode, power consumption is reduced considerably that in battery operation battery life time can be extended a lot. For applications where power consumption is a critical factor, ADAM45P52XX provides two kinds of power-down functions, STOP mode and SLEEP mode. In this 2 Modes, program processing is stopped.

10.1. Stop Mode

STOP mode can be entered by STOP instruction during program.

In STOP mode, oscillator is stopped to make all clocks stop, which leads to less power consumption. All registers and RAM data are preserved.

"NOP" instruction should be follows STOP instruction for pre-charge time of Data Bus line.

ex) STOP : STOP instruction execution
NOP : NOP instruction

10.1.1. Stop Mode Release

Release of STOP mode is executed by Power on reset , Key input Port(one of PA, PB) which is selected by PAST and PBST register for stop release is Low, external interrupt and Low voltage detection (LVD) mode release.

When there is a release signal of STOP mode, if the Bit1(SROPT) of SCTLR is "1", the instruction execution starts after no waiting time. But if the Bit1(SROPT) of SCTLR is "0",the instruction execution after stabilization oscillation time($2^{14} \times 4/f_{OSC} = 16.384\text{ms}$ at $f_{OSC} = 4.0\text{MHz}$). The Bit1(SROPT) is default "0".

Release Factor	Release Method	Release Time
Power on Reset	By Power on reset, Stop mode is release and system is initialized.	$7.2\text{ms} + 57 \times 2^{10} \times 4/f_{OSC} = 65.5\text{ms}$ at $f_{OSC} = 4.0\text{MHz}$
Release from LVD detection	Stop mode is release when release from LVD detection.	(Option read time : about 7.2ms)
External Key Input (PA, PB port)	Stop mode is released by Low input at the selected pin by PAST and PBST register.	1) if SROPT=0 (default) : $4/f_{osc} = 1\mu\text{s}$ 2) if SROPT=1 : $2^{14} \times 4/f_{osc} = 16.384\text{ms}$ at $f_{osc} = 4.0\text{MHz}$
External interrupt	Stop mode is release external interrupt input.	
External Reset	Stop mode is release external RESETB pin.	

• System Control Register (SCTLR)

	3	2	1	0	
SCTLR	LVDOFF	CDDN	SROPT	NFOPT	1Bh
initial value	0	0	0	0	
R/W	W	W	W	W	

Selection Mode of SCTLR

Bit Name	Selection Mode		Remarks
LVDOFF	0	LVD Enable	
	1	LVD Disable	
CDDN	0	Port Current Drive Normal	
	1	Port Current Drivability decrease	
SROPT	0	STOP Release Time is Short. ($4/f_{osc}$)	
	1	STOP Release Time is Long for oscillation stabilization. ($2^{14} \times 4/f_{osc}$)	
NFOPT	0	Oscillation Clock Input Noise Filtering time is short for High Frequency operation. ($f_{osc} > 12\text{MHz}$)	
	1	Oscillation Clock Input Noise Filtering time is long for Low Frequency operation. ($f_{osc} < 12\text{MHz}$)	

10. Power-Down Function

10.2. Sleep Mode

SLEEP mode can be entered by SLEEP instruction during program.
 In SLEEP mode, basically CPU and ROM halts while oscillation and peripherals are operate.
 "NOP" instruction should be follows SLEEP instruction for pre-charge time of Data Bus line.

ex) SLEEP : SLEEP instruction execution
 NOP : NOP instruction

10.2.1 Sleep Mode Release

Release of SLEEP mode is executed by Power on reset , all interrupts and Low voltage detection (LVD) mode release. To be release by interrupt, interrupt should be enabled before SLEEP mode.
 This mode don't need the stabilization oscillation time.

Release Factor	Release Method	Release Time
Power on Reset	By Power on reset, Sleep mode is release and system is initialized.	$7.2\text{ms} + 57 \times 2^{10} \times 4 / f_{\text{OSC}} = 96.6\text{ms}$ at $f_{\text{OSC}} = 4.0\text{MHz}$
Release from LVD detection	Sleep mode is release when release from LVD detection.	(Option read time : about 7.2ms)
All Interrupts	Sleep mode is released by all Interrupts.	$4 / f_{\text{OSC}} = 1\mu\text{s}$ at $f_{\text{OSC}} = 4.0\text{MHz}$
External Reset	Sleep mode is release external RESETB pin.	Ext. reset pulse width. (longer than $2 \times T_{\text{sys}}$)

10.3. Operation States in Stop/Sleep Mode

Internal Circuit	STOP Mode	SLEEP Mode
Oscillator	Stop	Operates continuously
Internal CPU clock	Stop	Stop
Address Bus Data Bus	Retained	Retained
Registers	Retained	Retained
RAM	Retained	Retained
I/O port, Output port	Retained	Retained
Timer	Stop (Counter clear)	Operates continuously
Watch dog Timer	Stop	Stop
ADC	Stop	Stop
VDI	Operates continuously	Operates continuously
Comparators, DAC	Operates continuously	Operates continuously
Release Method	RESETB, Power-on-reset, Release from LVD, Ext. Interrupt, Key-input Low, VDI	RESETB, Power-on-reset, Release from LVD, All Interrupts (except ADC)

Table 10.1 Operation States in Stop Mode and Sleep Mode

11. RESET Function

11.1. Power On RESET

Power On Reset circuit automatically detects the rise of power voltage (the rising time should be within 50ms). Until the power voltage reaches a certain voltage level, internal reset signal is maintained at "L" Level until oscillator is stable. After power applies, this reset state is maintained for the configuration option reading time (about 7.2ms at VDD=5.0V) and the oscillation stabilization time. ($4/f_{osc} \times 57 \times 2^{10}$ = about 58.368ms at 4MHz).

Fig.11.1 Block Diagram of Power On Reset Circuit

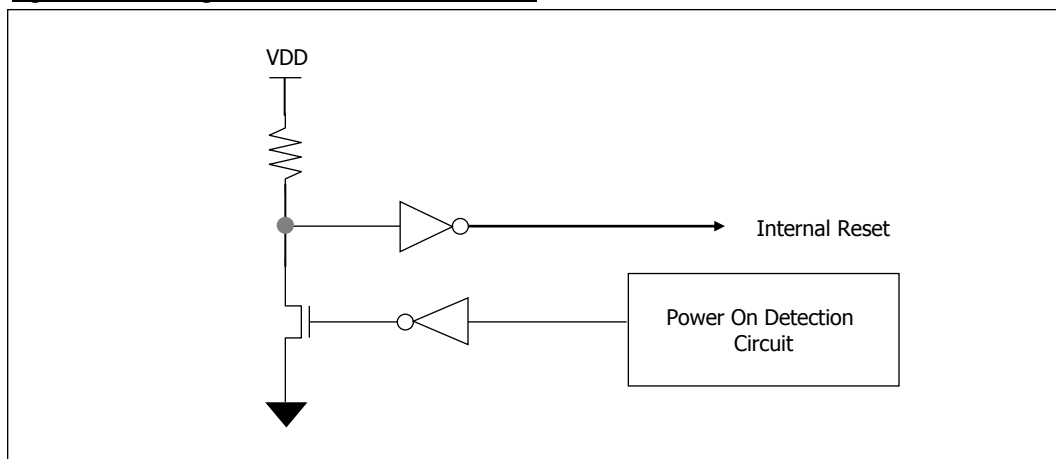
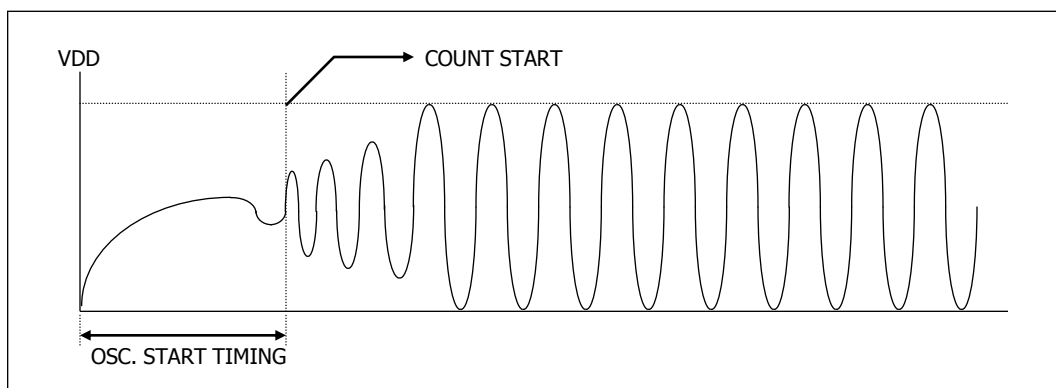


Fig.11.2 Oscillator stabilization diagram



Notice. When Power On Reset, oscillator stabilization time doesn't include OSC. Start time.

12. Low Voltage Detection Mode

12.1. Low Voltage Detection Condition

An on board voltage comparator checks that V_{DD} is at the required level to ensure correct operation of the device.

If V_{DD} is below a certain level, Low voltage detector forces the device into low voltage detection mode.

12.2. Low Voltage Detection Mode

There is no power consumption except stop current.

1. STOP mode release function is disabled.
2. I/O port is configured as input mode (without pull-up resistor).
3. Data memory is retained until voltage through external capacitor is worn out.
4. Interrupt disabled.
5. Oscillator is stop.

12.3. Release of Low Voltage Detection Mode

Reset signal result from new battery or any other power (normally 3V/5V) wakes the low voltage detection mode and come into normal reset state. It depends on user whether to execute RAM clear routine or not.

12.4. Low Voltage Detection voltage selection (option)

User can select the voltage of Low Voltage detection voltage level by OTP Configuration Bits (LVDS). One is high voltage version (typ. 2.3V, if LVDS is "0"), another is low voltage version (typ. 1.8V, if LVDS is "1").

13. Voltage Detection Indicator Mode

13.1. Voltage Detection Indicator Register

Voltage Detection indicator (VDI) are controlled by two registers. It is useful to display the consumption of Batteries.

If VDD power level is low and higher than low voltage detection (LVD) level (refer to Fig.14.1), the bit of VDIR register could be set according to the VDD level sequentially.

The VDD detection levels for Indication are three, that is, VDIR2 (Typ. 4.0V), VDIR1 (Typ. 3.0V) and VDIR0 (Typ. 2.5V) of VDIR register.

13.1.1. Voltage Detection Indicator Enable Register (VDIER)

bit	3	2	1	0	
VDIER	VDIM	VDIER2	VDIER1	VDIER0	33h
Initial value	0	0	0	0	
R/W	W	W	W	W	

VDIER0	detection level 0 (typ. 2.5V) selection	0	disable
		1	enable
VDIER1	detection level 1 (typ. 3.0V) selection	0	disable
		1	enable
VDIER2	detection level 2 (typ. 4.0V) selection	0	disable
		1	enable
VDIM	VDI Mode Selection	0	System Reset Selection
		1	Interrupt Selection

Voltage Detection Indicator Enable Register (VDIER) is 4-bit register, and can assign Indicator is enable or not.

If VDIR2 ~ VDIR0 is selected as "0", Voltage detection for Indication function is disabled and if selected as "1", it is enable. If VDIM is selected as "0" and enable one of VDIR2~VDIR0, when the corresponding voltage detection for Indication is occurred, it makes the system reset. If LVIM is selected as "1", it makes the VDI interrupt.

VDIER is write-only register and initialized as ``0h`` in reset state.

In the in-circuit emulator, VDI function is not implemented and user can not experiment with it.

Therefore after final development of user program, this function may be experimented or evaluated.

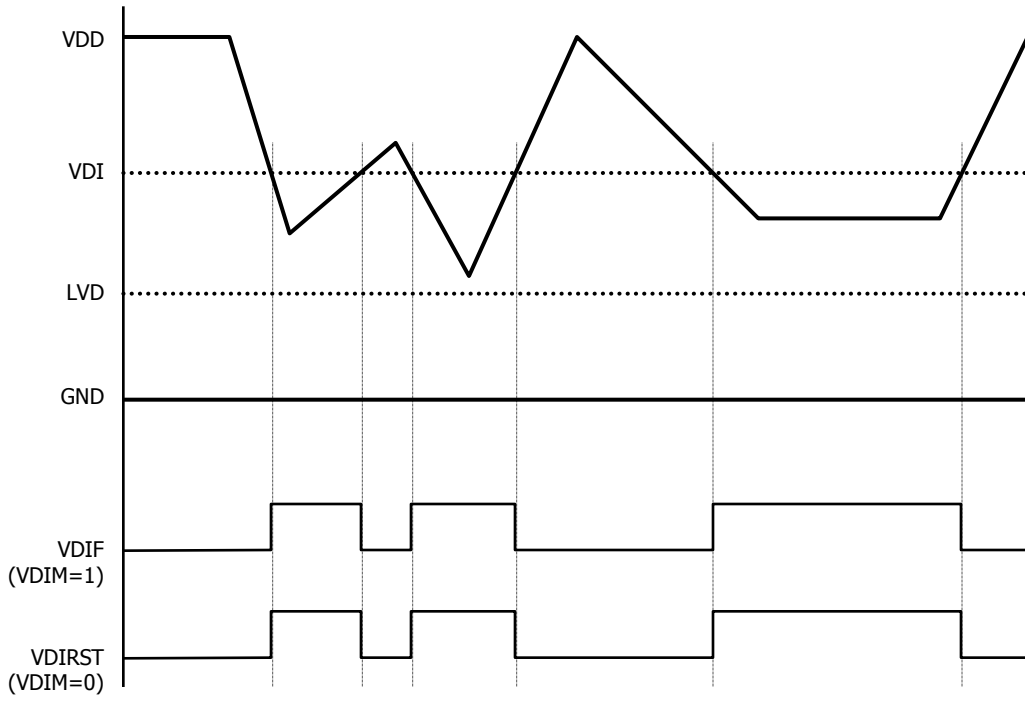
13.1.2. Voltage Detection Indicator Data Register (VDIR)

bit	3	2	1	0	
VDIR	-	VDIR2	VDIR1	VDIR0	33h
Initial value	0	0	0	0	
R/W	R	R	R	R	

Voltage Detection Indicator Data Register (VDIR) is 3-bit register to store data of low voltage level. VDIR is read only register and initialized as "0h" in reset state.

13. Voltage Detection Indicator Mode

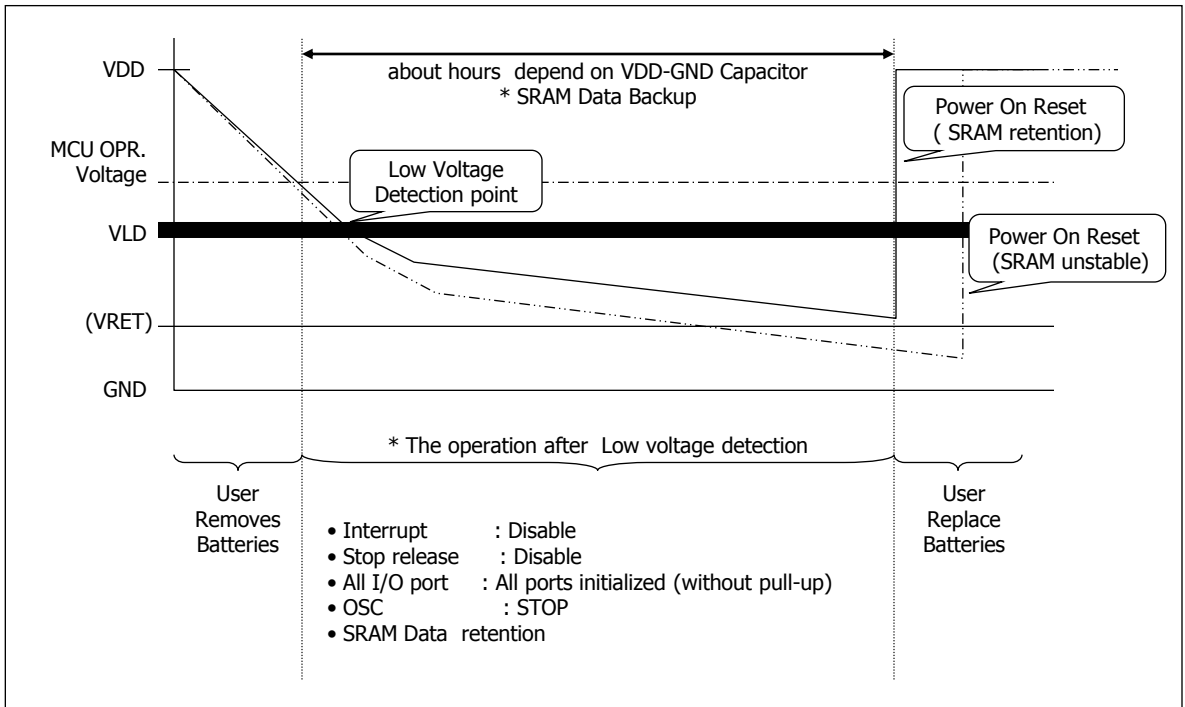
13.2. Timing Diagram



14. SRAM Data Back-Up

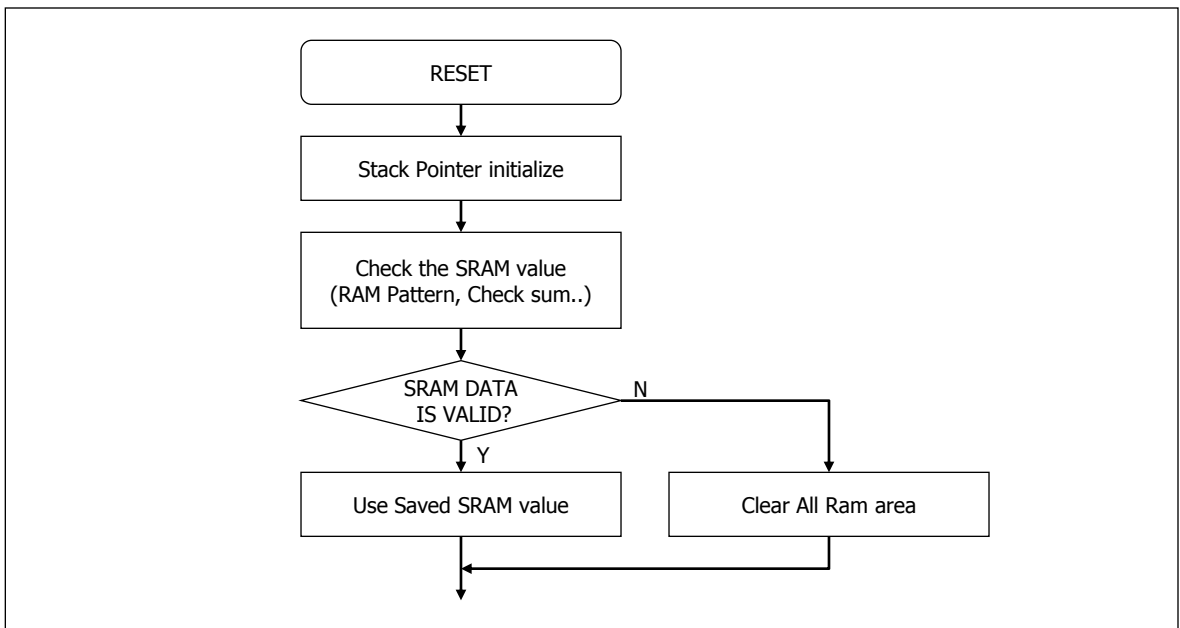
14.1 SRAM DATA BACK-UP after Low Voltage Detection

Fig.14.1 Low Voltage Detection and Protection



14.2 S/W flow chart example after Reset using SRAM DATA Back-up

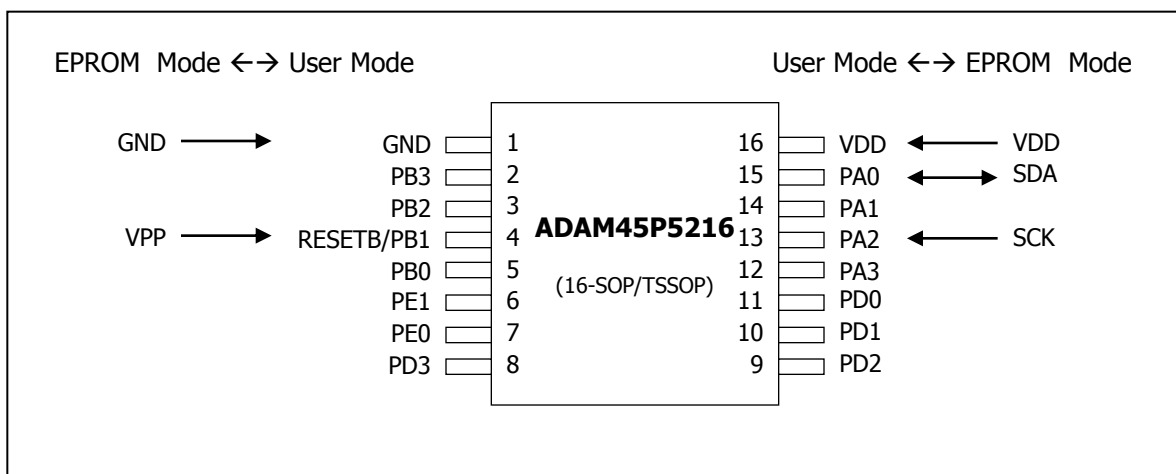
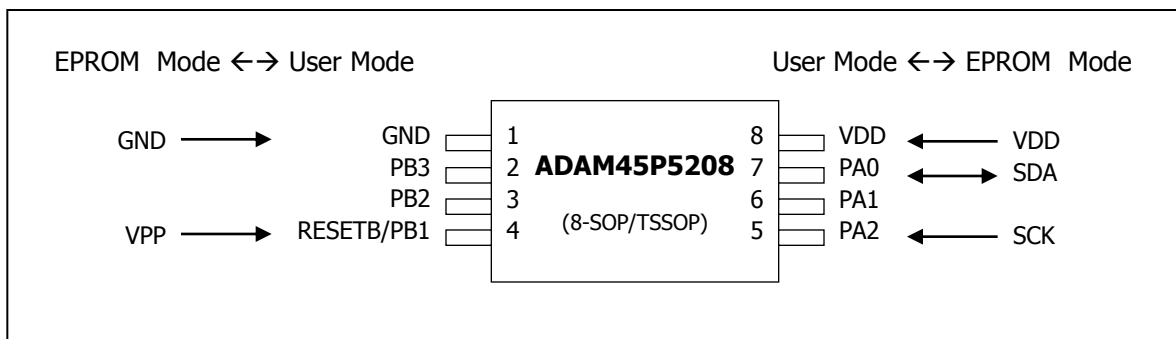
Fig.14.2 S/W Flow Chart Example for SRAM Back-up



15. MTP Programming

15.1. MTP Writing Pin Assignments

SYMBOL	User Mode	EPROM Mode
VDD	Power	VDD Power (typ. 5V)
GND	Ground	Ground (0V)
VPP	PB1	Program/Verify Power (typ. 11.5V)
SCK	PA2	Serial Clock Input
SDA	PA0	Serial Data Input/Output (Open-Drain Output)



15. MTP Programming

15.2. Configuration Option Bit Description

pgm/vfy Address : 8000h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPTION0	LOCK[3:0]				SIZE[3:0]				RSTS	OSCS[1:0]		LVDS	--			
Initial	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	OTP Code Option Description	Option Value	Remarks
15	LOCK	LOCK Definition (disable or enable reading user code)	Refer to Programming Specification	It's set automatically by our MTP Writer (ADAM OTP Programmer)
14				
13				
12				
11	SIZE	ROM SIZE Definition -. 4k x 16bit -. 2k x 16bit -. 1k x 16bit	Refer to Programming Specification	
10				
9				
8				
7	RSTS	RESETB/PB1 Selection	1	RESETB
			0	PB1
6:5	OSCS	Oscillator Type Selection	OSCS[1:0]	
		Internal RC 4MHz	11	
		Internal RC 8MHz	10	
		Internal RC 16MHz	01	
		Internal RC 1MHz	00	
4	LVDS	LVD Level Selection	1	LVD=1.8V
			0	LVD=2.3V
3:0	--	<i>Not used</i>	--	--

16. Instruction Set

16.1. Legend

A :	accumulator(4bit)
r :	peripheral address register(6bit)
[r] :	data addressed by peripheral address register (4bit)
Y :	Y register(4bit)
X :	X register(4bit)
ABR :	address buffer register(15bit)
ABRn :	address buffer register #0~3(4bit)
[@ABR] :	data addressed by ABR(16bit)
DBR :	data buffer register(16bit)
DBRn :	data buffer register #0~3(4bit)
T0CR :	Timer 0 count register(8bit)
T1CR :	Timer 1 count register(8bit)
#n4 :	0~Fh
#n2 :	0~3
#n1 :	0~1
dp :	data address point(8bit)
dp+X+Y :	data address point indexed by X-register and Y-register (8bit)
PG :	page address(1bit)
ADS :	address stack register
labs :	address

16. Instruction Set

16.2. Instruction Set Table

NO	INSTRUCTION GROUP	MNEMONIC	USAGE	OPERATION	S	CY	
1	Arithmetic & Logic	ADDC	ADDC m(dp),#n4	$A = m(dp) + \#n4 + CY$ $A = m(dp + X + Y) + \#n4 + CY$ at D flag of SFR is set. "S" set if overflow.	C	O	
2			ADDC A,#n4	$A = A + \#n4 + CY$, "S" set if overflow	C	O	
3			ADDC m(dp), A	$A = m(dp) + A + CY$, $A = m(dp + X + Y) + A + CY$ at D flag of SFR is set. "S" set if overflow	C	O	
4			ADDC ABRn,#n4	$ABRn = ABRn + \#n4 + CY$, "S" set if overflow	C	O	
5			ADDC ABRn,A	$ABRn = ABRn + A + CY$, "S" set if overflow	C	O	
6			ADDC ABRn,Y	$ABRn = ABRn + Y + CY$, "S" set if overflow	C	O	
7			ADDC DBRn,#n4	$DBRn = DBRn + \#n4 + CY$, "S" set if overflow	C	O	
8			ADDC DBRn,A	$DBRn = DBRn + A + CY$, "S" set if overflow	C	O	
9			ADDC DBRn,Y	$DBRn = DBRn + Y + CY$, "S" set if overflow	C	O	
10			ADDC Y,#n4	$Y = Y + \#n4 + CY$, "S" set if overflow	C	O	
11			ADDC X,#n4	$X = X + \#n4 + CY$, "S" set if overflow	C	O	
12		SUBC	SUBC m(dp),#n4	$A = m(dp) - \#n4 - CY$, $A = m(dp + X + Y) - \#n4 - CY$ at D flag of SFR is set. "S" clear if underflow	B	W	
13				SUBC A,#n4	$A = A - \#n4 - CY$, "S" clear if underflow	B	W
14			SUBC m(dp), A	$A = m(dp) - A - CY$, $A = m(dp + X + Y) - A - CY$ at D flag of SFR is set. "S" clear if underflow	B	W	
15			SUBC ABRn, #n4	$ABRn = ABRn - \#n4 - CY$, "S" clear if underflow	B	W	
16			SUBC ABRn, A	$ABRn = ABRn - A - CY$, "S" clear if underflow	B	W	
17			SUBC ABRn, Y	$ABRn = ABRn - Y - CY$, "S" clear if underflow	B	W	
18			SUBC DBRn, #n4	$DBRn = DBRn - \#n4 - CY$, "S" clear if underflow	B	W	
19			SUBC DBRn, A	$DBRn = DBRn - A - CY$, "S" clear if underflow	B	W	
20			SUBC DBRn, Y	$DBRn = DBRn - Y - CY$, "S" clear if underflow	B	W	
21			SUBC Y, #n4	$Y = Y - \#n4 - CY$, "S" clear if underflow	B	W	
22			SUBC X, #n4	$X = X - \#n4 - CY$, "S" clear if underflow	B	W	
23			ARRC	ARRC	$A = A$ rotate right with CY	T	R
24			ARLC	ARLC	$A = A$ rotate left with CY	T	R
25			CMPL	CMPL	$A = A + 1$	Z	.
26			XOR	XOR m(dp)	$A = A \oplus m(dp)$, $A = A \oplus m(dp + X + Y)$ at D flag of SFR is set	S	.
27			AND	AND m(dp)	$A = A \wedge m(dp)$, $A = A \wedge m(dp + X + Y)$ at D flag of SFR is set	S	.
28			OR	OR m(dp)	$A = A \vee m(dp)$, $A = A \vee m(dp + X + Y)$ at D flag of SFR is set	S	.

16. Instruction Set

NO	INSTRUCTION GROUP	MNEMONIC	USAGE	OPERATION	S	CY
29	Compare	CALE	CALE #n4	"S" set if $A \leq \#n4$	E	.
30			CALE m(dp)	"S" set if $A \leq m(dp)$, "S" set if $A \leq m(dp+X+Y)$ at D flag of SFR is set.	E	.
31		CAGE	CAGE #n4	"S" set if $A \geq \#n4$	E	.
32		CANE	CANE #n4	"S" set if $A \neq \#n4$	N	.
33			CANE m(dp)	"S" set if $A \neq m(dp)$, "S" set if $A \neq m(dp+X+Y)$ at D flag of SFR is set.	N	.
34		CMLE	CMLE m(dp),#n4	"S" set if $m(dp) \leq \#n4$, "S" set if $m(dp+X+Y) \leq \#n4$ at D flag of SFR is set.	E	.
35		CMNE	CMNE m(dp),#n4	"S" set if $m(dp) \neq \#n4$, "S" set if $m(dp+X+Y) \neq \#n4$ at D flag of SFR is set.	N	.
36		CYGE	CYGE #n4	"S" set if $Y \geq \#n4$	E	.
37		CYNE	CYNE #n4	"S" set if $Y \neq \#n4$	N	.
38			CYNE A	"S" set if $Y \neq A$	N	.
39		CXGE	CXGE #n4	"S" set if $X \geq \#n4$	E	.
40		CXNE	CXNE #n4	"S" set if $X \neq \#n4$	N	.
41	Bit Manipulation	SET1	SET1 m(dp).#n2	Set bit m(dp).#n2, Set bit m(dp+X+Y).#n2 at D flag of SFR is set.	S	.
42		CLR1	CLR1 m(dp).#n2	Clear bit m(dp).#n2, Clear bit m(dp+X+Y).#n2 at D flag of SFR is set.	S	.
43		TM	TM m(dp).#n2	"S" set if m(dp) Bit = 1 "S" set if m(dp+X+Y) Bit = 1 at D flag of SFR is set.	E	.
44		SETR1	SETR1 r.#n2	Set bit [r].#n2	S	.
45		CLRR1	CLRR1 r.#n2	Clear bit [r].#n2	S	.
46		TSTR	TSTR r.#n2	"S" set if [r].#n2 Bit = 1	E	.
47		NOTA1	NOTA1 #n2	$A.\#n2 \leftarrow \sim(A.\#n2)$	S	.
48	Carry Manipulation	CLRC	CLRC	Carry Bit of SFR is clear.	S	0
49		SETC	SETC	Carry Bit of SFR is set.	S	1
50		TSTC	TSTC	"S" set if Carry Test = 1.	E	.
51		LDC	LDC r.#n2	$CY \leftarrow [r].\#n2$	S	.
52		STC	STC r.#n2	$[r].\#n2 \leftarrow CY$	S	.
53	DATA Transfer	LDM	LDM m(dp),#n4	$m(dp) = \#n4$ $m(dp+X+Y) = \#n4$ at D flag of SFR is set.	S	.
54			LDM m(dp), A	$m(dp) \leftarrow A$ $m(dp+X+Y) \leftarrow A$ at D flag of SFR is set.	S	.
55		LDA	LDA #n4	$A = \#n4$	S	.
56			LDA m(dp)	$A \leftarrow m(dp)$ $A \leftarrow m(dp+X+Y)$ at D flag of SFR is set.	S	.

16. Instruction Set

NO	INSTRUCTION GROUP	MNEMONIC	USAGE	OPERATION	S	CY
57	DATA Transfer	LDA	LDA X	$A \leftarrow X$	S	.
58			LDA Y	$A \leftarrow Y$	S	.
59		LDY	LDY #n4	$Y = \#n4$	S	.
60			LDY A	$Y \leftarrow A$	S	.
61		LDX	LDX #n4	$X = \#n4$	S	.
62			LDX A	$X \leftarrow A$	S	.
63		XMA	XMA m(dp)	$A \leftrightarrow m(dp)$ $A \leftrightarrow m(dp+X+Y)$ at D flag of SFR is set.	S	.
64		LDW	LDW @ABR	$DBR \leftarrow (@ABR)$ **[Note]	S	.
65			LDW DBR,ABR	$DBR \leftarrow ABR$	S	.
66			LDW ABR,DBR	$ABR \leftarrow DBR$	S	.
67			LDW DBR,T0CR	$DBR1,DBR0 \leftarrow T0CR$	S	.
68			LDW DBR,T1CR	$DBR3,DBR2 \leftarrow T1CR$	S	.
69		LPG	LPG #n1	$PG = \#n1$	S	.
70		LRA	LRA r	$[r] \leftarrow A$	S	.
71	LAR	LAR r	$A \leftarrow [r]$	S	.	
72	LRI	LRI r,#n4	$[r] = \#n4$	S	.	
73	Increment	INC	INC ABR	$ABR++$	-	.
74	Branch	BR	BR !abs	If S bit of SFR =1 , Absolute branch, $PC \leftarrow !abs$	S	.
75			BR @ABR	If S bit of SFR =1 , Indirect branch $PG+PC \leftarrow ABR$	S	.
76	Subroutine	CALL	CALL !abs	If S bit of SFR =1 , $ADS \leftarrow PG + PC, SP \leftarrow SP - 1, PC \leftarrow !abs$	S	.
77			CALL @ABR	If S bit of SFR =1 , $ADS \leftarrow PG + PC, SP \leftarrow SP - 1, PG+PC \leftarrow ABR$	S	.
78		RET	RET	$SP \leftarrow SP + 1, PG+PC \leftarrow ADS$	S	.
79		RETI	RETI	$SPSFR \leftarrow SPSFR + 1, SFR \leftarrow M(SPSFR)$ $SP \leftarrow SP + 1, PG+PC \leftarrow ADS$	S	.
80	Etc	NOP	NOP		S	.
81		STOP	STOP		S	.
82		SLEEP	SLEEP		S	.
83		WDTC	WDTC	Watchdog Timer Clear	S	.
84		SPC	SPC	Stack Pointer Clear	S	.
85		EIX	EIX	Index bit of SFR is set	S	.
86		DIX	DIX	Index bit of SFR is clear	S	.
87		EI	EI	Interrupt bit of SFR is set	S	.
88		DI	DI	Interrupt bit of SFR is clear	S	.

****[Note]** The Instruction "LDW @ABR" execution time is 2cycle and execution process is as follow.
 $SP = SP - 1, ADS \leftarrow PG + PC,$
 $PG + PC \leftarrow ABR, DBR \leftarrow (PG + PC), PG + PC \leftarrow ADS, SP = SP + 1$

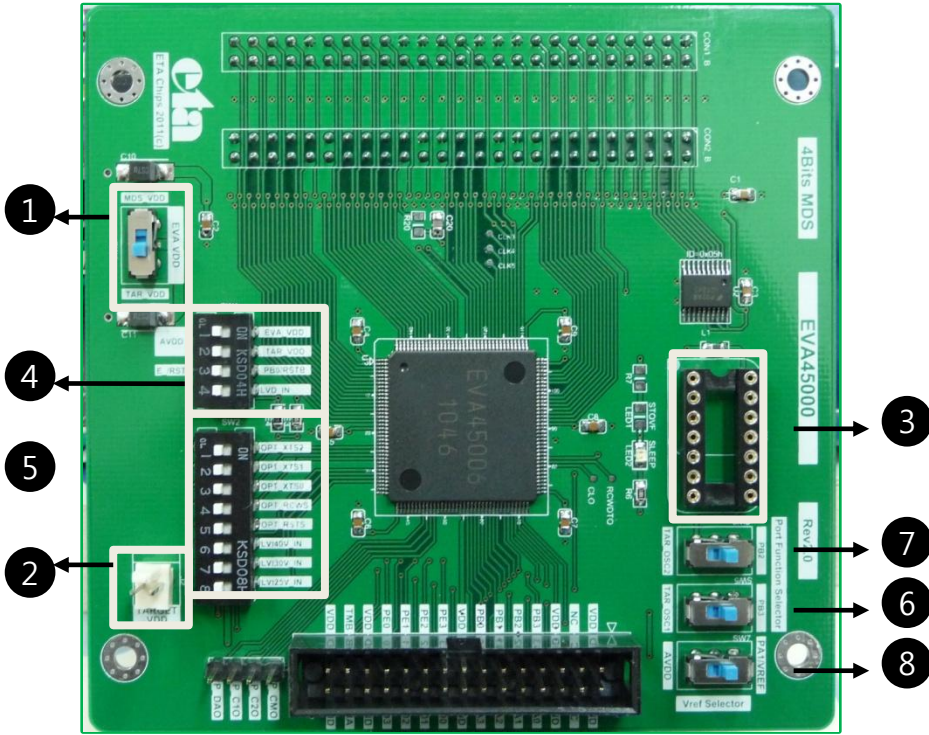
**** CARRY BIT(CY)** hold previous value before execution CLRC/SETC instruction .
 Symbols have meaning as follows.
 { O : Carry bit is only set when overflow has occurred in operation.
 W : Carry bit is only set when borrow has occurred in operation.
 R : Carry bit is only set or reset according to shift bit.

**** STATUS BIT(S)** indicates conditions for changing status. Symbols have meaning as follows.
 { S : On executing an instruction, status bit is unconditionally set.
 C : Status bit is only set when overflow has occurred in operation.
 B : Status bit is only set when underflow has not occurred in operation.
 E : Status bit is only set when equality is found in comparison.
 N : Status bit is only set when equality is not found in comparison.
 Z : Status bit only set when the result is zero.
 T : Status bit only set when the carry has occurred in operation.

A. EVA 45000 Board Manual



A.1. EMULATOR EVA45000 BOARD SETTING



J1	
1	VDD
3	N.C
5	VDD
7	PB3
9	PB2
11	PB1
13	PB0
15	VDD
17	PE3
19	PE2
21	PE1
23	PE0
25	VDD
27	TMB
29	VDD
2	GND
4	N.C
6	GND
8	PA0
10	PA1
12	PA2
14	PA3
16	GND
18	PD0
20	PD1
22	PD2
24	PD3
26	GND
28	TMA
30	GND

A.2. DIP and Slide switch setting

"1" : Switch on, "0" : Switch off, "Up" : upper side, "Dn" : lower side

DIP S/W		Description	ON/OFF Setting
① SW4	EVA VDD	- EVA Chip VDD	"Up" : MDS VDD (EVA B/D_VDD) "Dn" : Target VDD(Target system)
② J2	Target VDD Connector	- 1, 2 Pin = VDD	EVA Chip VDD ← Target VDD * EVA_VDD switch (SW4) = Target VDD
③ XE1	EXT. OSC	This is External oscillation socket	This is for External Clock (OSC Module Type.)
④ SW1	1 2	AVDD - AVDD(Analog ADC power)	"01" : AVDD ← MDS VDD (EVA B/D VDD) "10" : AVDD ← Target VDD(Target system) ADC(Analog digital converter Power)
	3	PB0/RSTB - MDS Reset input.	MDS RESETB ← PB0(RESETB) : Target reset.
	4	LVD_IN - LVD signal input pin. LVD_IN	Low voltage detector activation. (In OTP, it occurs when VDD<LVD voltage)
⑤ SW2	2 3	OPT_XTS1 OPT_XTS0 Oscillator type selection pins. (From EVA type where is selected is not used with system clock, PORT function and to CLO pin outputs being reflected)	"11" : Internal RC 4MHz "10" : Internal RC 8MHz "01" : Internal RC 16MHz "00" : internal RC 1MHz From EVA type where is selected is not used with system clock,
	4	OPT_BUFS - P-DAO2 output enable pin.	"1" : Default "0" : Enable with analog buffer
	5	OPT_RSTS - PB1/RESETB selection pin.	"1" : RESETB "0" : PB1
	6 7 8	LVI40V_IN LVI30V_IN LVI25V_IN VDI signal input pin.	In OTP, it occurs when VDD < selected VDI voltage. (from EVA, active being used respectively voltage detection indicator (VDI))
6 SW6	- PB3/OSC1	- Port function selector PB3/OSC1	"Up" : PB3 "Dn" : Xin(OSC2)
7 SW5	- PB2/OSC2	- Port function selector PB2/OSC2	"Up" : PB2 "Dn" : Xout(OSC2)
8 SW7	PA1/VREF	- Port function selector	"Up" : VREF (EVA Chip) "Dn" : AVDD (EVA Board)

B. ADAM Single Writer Manual

B.1. ADAM Single Writer

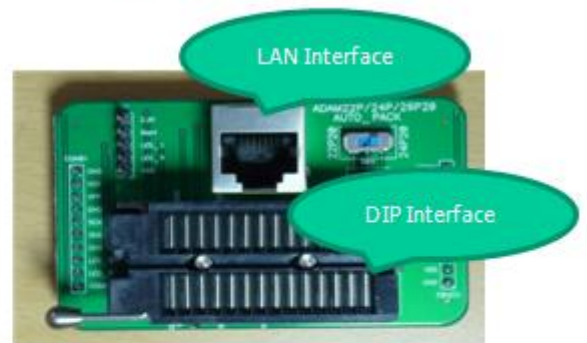
ADAM Single Writer support for all device of ETA Chips MCU family.
It can work stand alone and also work with PC via USB interface.

B.2. H/W Configuration

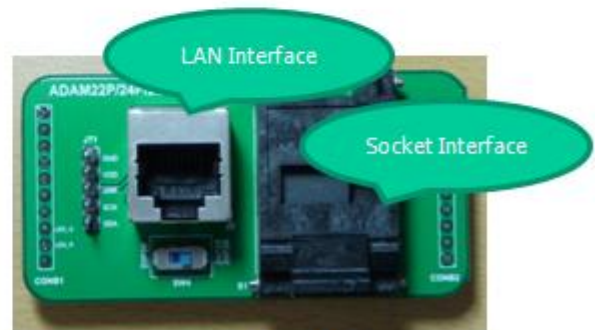
< Single Writer Body >



< Pack Board >



DIP Board



Socket Board