CMOS single-chip 8-bit MCU with 12-bit A/D converter and CEC Controller

Main features

- **8-bit Microcontroller With High Speed 8051 CPU**
- **Basic MCU Function**
  - 64KB Flash Code Memory
  - 4,352 bytes SRAM
  - 2KB Data EEPROM
- **Built-in Analog Function**
  - Power-On Reset and Low Voltage Detect Reset
  - Internal 16MHz RC Oscillator (±1.5%, T_A = 0 ~ +50°C)
  - Watchdog Timer RC Oscillator (256kHz)
- **Peripheral Features**
  - 12-bit Analog to Digital Converter (10 inputs)
  - USART 8-bit x 2-ch
  - SPI 8-bit x 2-ch
  - I2C 8-bit x 2-ch
  - Hardware CEC Controller
  - Hardware IR Receiver
- **I/O and Packages**
  - Up to 46 programmable I/O lines with 48-LQFP
  - 48-LQFP
- **Operating Conditions**
  - 2.7V to 5.5V Wide Voltage Range
  - -40°C to 85°C Temperature Range
- **Application**
  - Home Appliance

A97C450

Data Sheet

V 1.02

Revised 31 Jan, 2018

Revision History

Version	Date	Revision list
1.00	2017.08.11	The First Edition.
1.01	2017.10.26	Maximum value of IDD6 (STOP2) is added in “Table 7.9 DC Characteristics”. The content of flowchart is changed in “Figure 11.64 Procedure for Reading RTC”. Note about the writing to I2CSR is added in “11.12.11”
1.02	2018.01.31	Add Device Nomenclature. Awake-up interrupt from power down mode is removed in 11.14. Fix 11.17.9 RTC Register description (YEAR Register bit (Address 0x8FBA)).

Version 1.02

Published by AE team

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1 Overview

1.1. Description

The A97C450 is advanced CMOS 8-bit microcontroller with FLASH (64KB) and EEPROM (2KB). This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This provides the following features : 64KB of FLASH, 2KB of Data EEPROM, 256 bytes of SRAM, 4,096 bytes of XRAM, general purpose I/O, 8/16-bit timer/counter, watchdog timer, watch timer, RTC with calendar, SPI, USART, I2C, on-chip POR and LVI, 12-bit A/D converter, analog comparator, buzzer driving port, 8/16-bit PWM output, on-chip oscillator, CEC, IR receiver and clock circuitry. The A97C450 also supports power saving modes to reduce power consumption.

1.2 Ordering information

Device Name	Flash	XRAM	IRAM	EEPROM	ADC	I/O PORT	Package
A97C450CLN	64KB	4,096 bytes	256 bytes	2KB	10 inputs	46	48-LQFP

Table 1.1 Ordering Information of A97C450

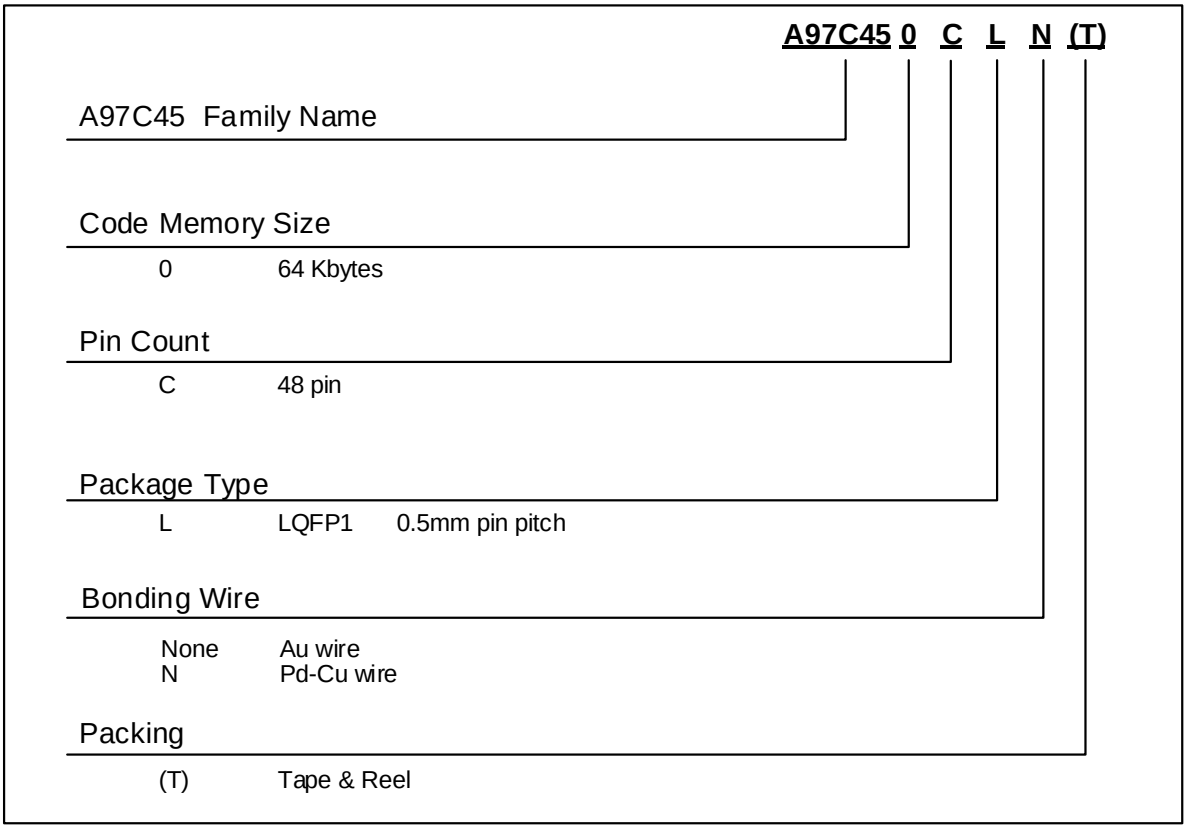


Figure 1.1 Device Nomenclature

1.3 Features

- **CPU**
  - 8-bit CISC core (M8051, 2 clocks per cycle)
- **ROM (FLASH) Capacity**
  - 64KB Flash with self-read and write capability
  - In-System Programming(ISP)
  - Endurance : 10,000 times
  - Retention : 10 years
- **2KB On-chip EEPROM**
  - Endurance : 300,000 times
  - Retention : 10 years
- **256 bytes IRAM / 4,096 bytes XRAM**
- **General Purpose I/O (GPIO)**
  - Normal I/O : 46 Ports (P0, P1, P2, P3, P4, P5[5:0])
- **Boot Loader Protection with Boot Swap**
- **External stack with stack overflow interrupt**
- **Hardware CEC**
- **Hardware IR Receiver with Noise Filter**
- **Timer/Counter**
  - Basic Interval Timer (BIT) 8-bit × 1-ch
  - Watch Dog Timer (WDT) 8-bit × 1-ch
    256kHz internal RC oscillator for WDT
  - 8-bit × 2-ch (T0/T1)
  - 16-bit × 5-ch (T2/T3/T4/T5/T6)
- **Programmable Pulse Generation**
  - Pulse generation (by T2/T3/T4/T5/T6)
  - 8-bit PWM (by T0/T1)
- **Watch Timer (WT)**
  - 3.91ms/0.25s/0.5s/1s /1min interval at 32.768kHz
- **RTC with 100 Year Calendar**
- **Buzzer**
  - 8-bit × 1-ch
- **SPI**
  - 8-bit × 2-ch
- **USART**
  - 8-bit USART × 2-ch
- **I2C**
  - I2C × 2-ch
- **12-bit A/D Converter**
  - 10 Input channels
- **Analog Comparator**
  - 2 Internal Comparator
- **Power On Reset**
  - Reset release level (1.4V)
- **Low Voltage Reset**
  - 1.6V
- **Low Voltage Indicator**
  - 3 levels detect (2.4V / 2.8V / 3.5V)
- **Interrupt Sources**
  - External Interrupts
    (EINT0, EINT1, EINT2~4, EINT5~7) (4)
  - Timer(0/1/2/3/4~6) (5)
  - CEC (1)
  - IR (1)
  - USART (4), SPI (2), I2C (2)
  - WDT (1)
  - WT (1)
  - RTC (1)
  - BIT (1)
  - ADC (1)
  - EEPROM (1)
  - LVI (1)
  - Analog comparator (1)
  - CRC (1)
  - Stack OVF (1)
- **Internal RC Oscillator**
  - Internal RC frequency: 16MHz ±1.5% (T_A= 0 ~ +50°C)
- **Power Down Mode**
  - STOP1/2, SLEEP1/2, IDLE mode
- **Operating Voltage and Frequency**
  - 2.7V~ 5.5V (@ 32 ~ 38kHz with Sub Crystal)
  - 2.7V~ 5.5V (@ 0.4 ~ 12.0MHz with Crystal)
  - 2.7V~ 5.5V (@ 1.0 ~ 16.0MHz with Internal RC)
  - Voltage dropout converter included for core
- **Minimum Instruction Execution Time**
  - 125ns (@16MHz clock)
- **Operating Temperature**
  - –40 ~ +85℃
- **Oscillator Type**
  - 0.4 - 12MHz Crystal or Ceramic for main clock
  - 32.768kHz Crystal for sub clock
- **Package Type**
  - 48-LQFP

1.4 Development tools

1.4.1 Compiler

ABOV Semiconductor does not provide compiler. It is recommended that you consult a compiler provider.

The A97C450 core is Mentor 8051 and the ROM size is smaller than 64KB. Therefore, developer can use the standard 8051 compiler from other providers.

1.4.2 OCD(On-chip debugger) emulator and debugger

The OCD (On Chip Debug) emulator supports ABOV Semiconductor's 8051 series MCU emulation. The OCD interface uses two-wire connection between PC and MCU which is attached to user's system. The OCD can read or change the value of MCU internal memory and I/O peripherals. And the OCD also controls MCU internal debugging logic, it means OCD controls emulation, step run, monitoring, etc.

The OCD debugger program works on Microsoft-Windows NT, 2000, XP, Vista (32-bit), 7, 8, 10 operating system. If you want to see more details, please refer to OCD debugger manual. You can download debugger S/W and manual from our web-site (http://www.abov.co.kr).

Connection:

- DSCL (A97C450 P36 port)
- DSDA (A97C450 P37 port)

OCD connector diagram: Connect OCD with user system

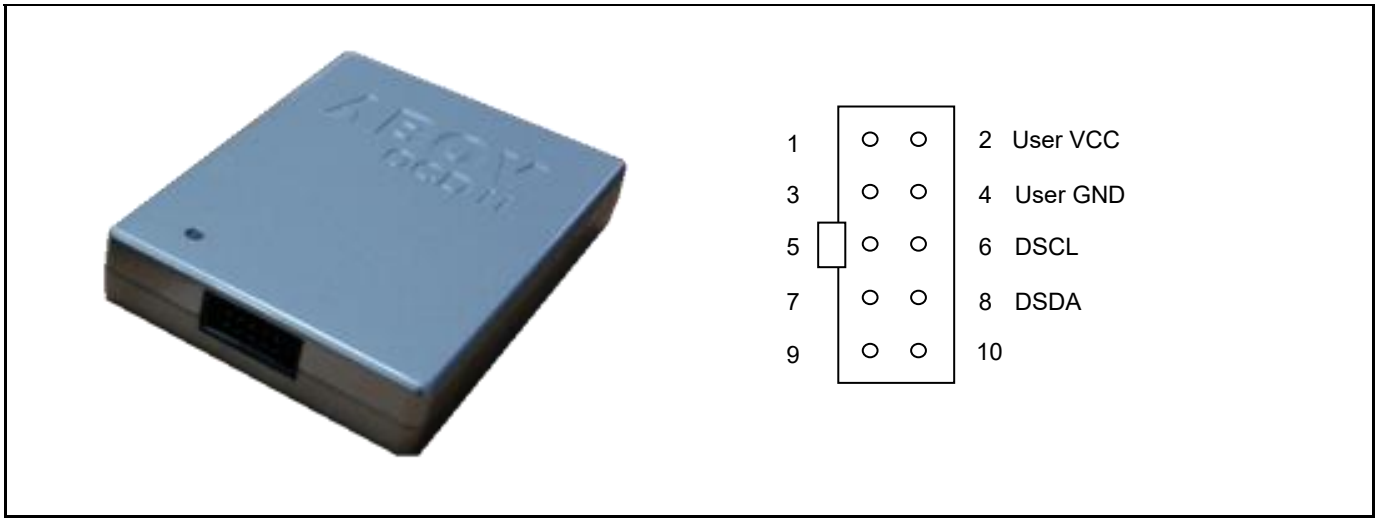


Figure 1.2 debugger and pin description

OCD2 (On Chip Debug) Emulator

- MCU emulation control via 2pin or 3pin OCD interface.
- 2pin interface : OCD2 clock & data.
- 1pin option interface
  - Support device OCD2 mode entry during user S/W is running.
  - Support exact emulation time measurement.
- Higher interface speed than OCD dongle.
- Support newly added debugging specifications.
- Compact size.
- Cost effective emulator.
- Emulation & debugging on the target system directly.
- Real time emulation.
- PC interface : USB.

Debugger

- Operates with OCD and OCD2 emulator H/W.
- Integrated Development Environment (IDE).
  Support docking windows and menus.
- Support Free run, Step run, auto step run.
- Support Symbolic debugging.
- Support Source level debugging.

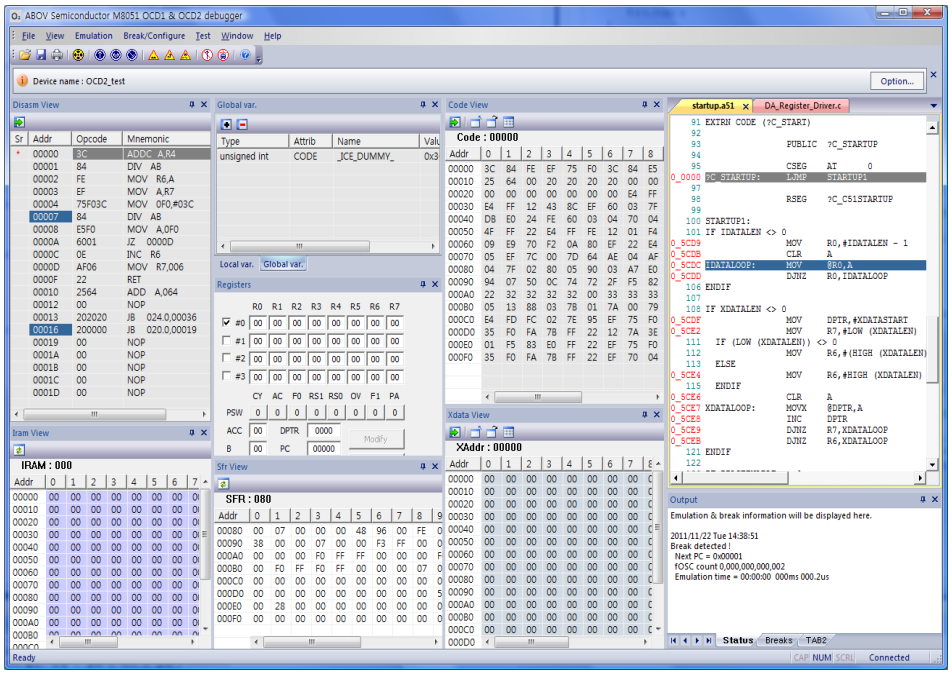


Figure 1.3 OCD Debugger

Support Devices

- MC94xxxx
- MC95xxxx
- MC96xxxx
- MC97xxxx

E-PGM +

- Support ABOV / ADAM devices
- 2~5 times faster than S-PGM+
- Main controller : 32 bit MCU @ 72MHz
- Buffer memory : 1 MByte

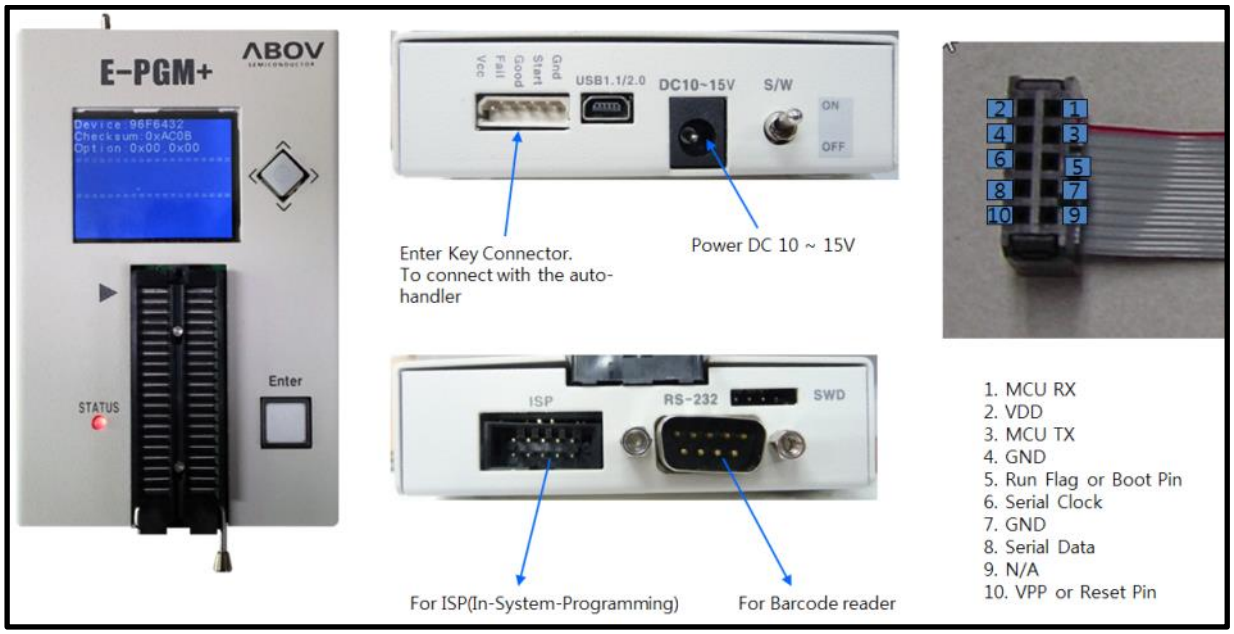


Figure 1.4 component and connector

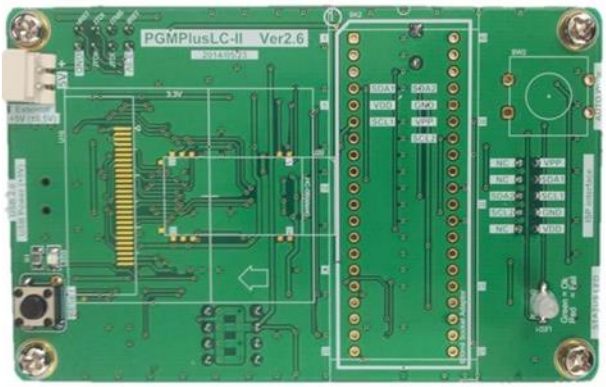
PGMPlusLC 2

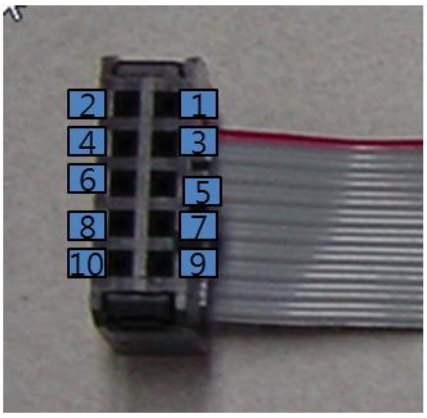
Description

PGMPlusLC2 is for ISP (In System Programming). It is used to write into the MCU Which is already mounted on target board using 10pin cable.

Features

- PGMplusLC2 is low cost writing Tool.
- USB interface is supported.
- Not need USB driver installation.
- Connect the external power adaptor (5v@2A).
- Fast 32-bit Cortex-M3 MCU is used.
- Supported high voltage Max 18V.
- PGMplusLC2 is based on PC environment.
- PGMplusLC2 is faster than PGMplusLC.
- Transmission speed is 64kbyte/s





2. Vdd
4. GND
6. Serial Clock
8. Serial Data

Figure 1.5 PGMplusLC Writer

E-PGM+ Gang4/6

- Product name : **E-PGM+ GANG 4**
- Dimension(x , y, h) : 33.5 x 22.5 x35mm
- Weight : 2.0kg
- Input Voltage : DC Adaptor 15V/2A
- Operating Temp : -10 ~ 40℃
- Storage Temp : -30 ~ 80℃
- Water Proof : No

- Product name : **E-PGM+ GANG 6**
- Dimension(x , y, h) : 148.2 x 22.5 x35mm
- Weight : 2.8kg
- Input Voltage : DC Adaptor 15V/2A
- Operating Temp : -10 ~ 40℃
- Storage Temp : -30 ~ 80℃
- Water Proof : No

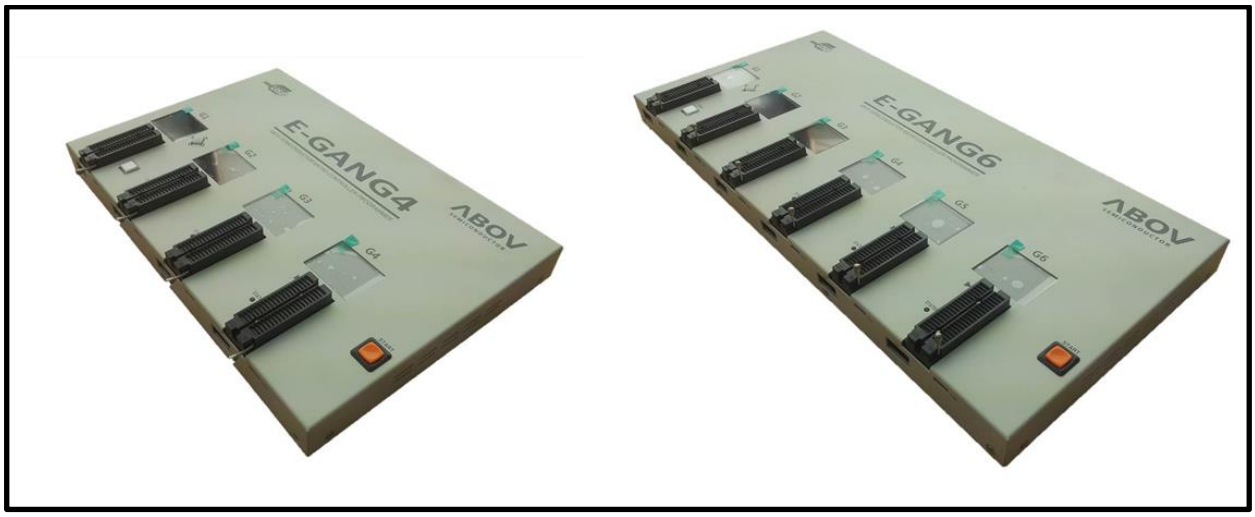


Figure 1.6 E-PGM+ Gang4/6 Programmer

1.5 MTP programming

1.5.1 Overview

The program memory of A97C450 is MTP Type. This flash is accessed by serial data format. There are four pins(DSCL, DSDA, VDD and VSS) for programming/reading the flash.

Pin name	Main chip pin name	During programming	
		I/O	Description
DSCL	P36	I	Serial clock pin. Input only pin.
DSDA	P37	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	-	Logic power supply pin.

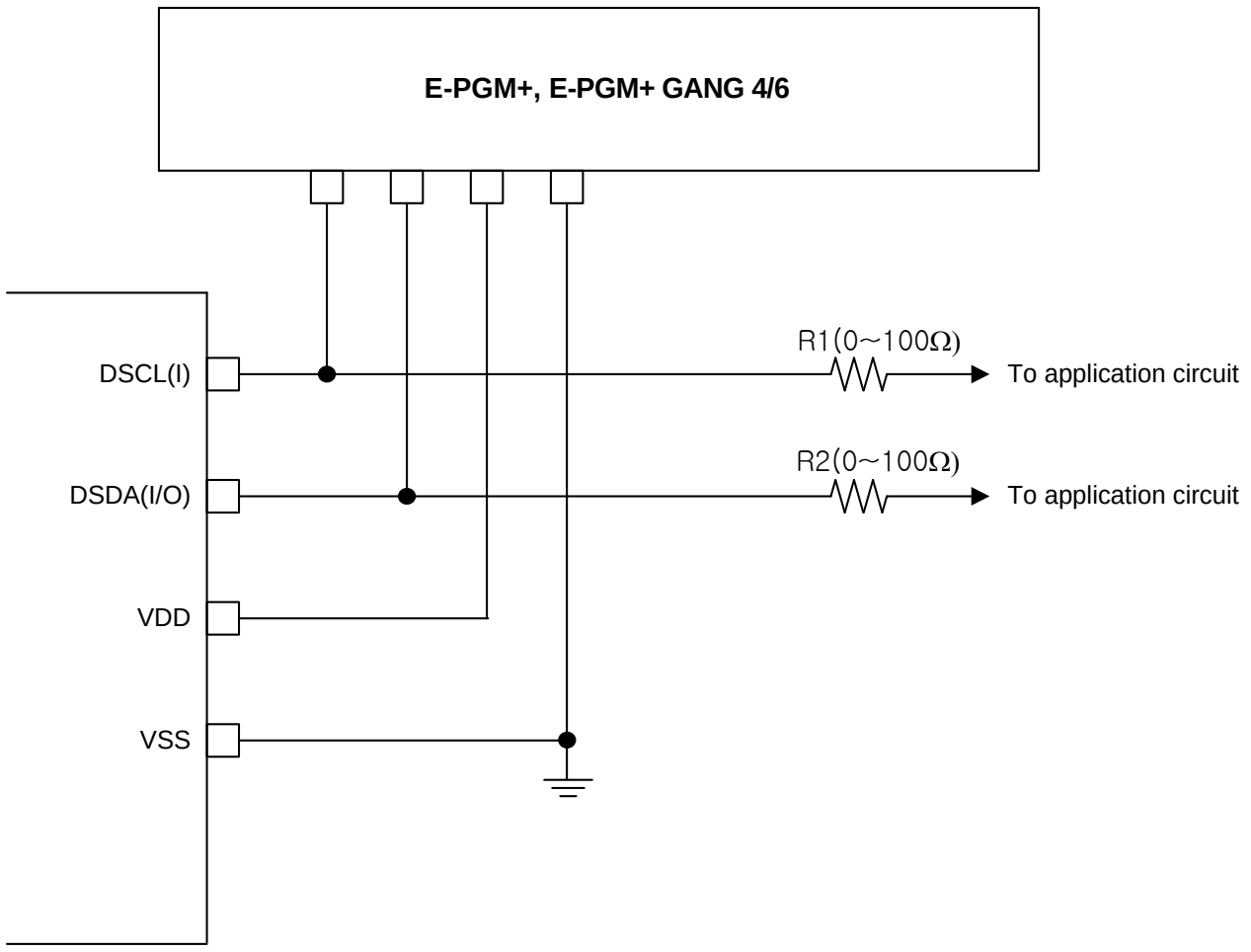
Table 1.2 Descriptions of pins which are used to programming/reading the Flash

1.5.2 On-Board programming

The A97C450 needs only four signal lines including VDD and VSS pins for programming FLASH with serial communication protocol. Therefore the on-board programming is possible if the programming signal lines are ready at the PCB of application board is designed.

1.5.2.1 Circuit Design Guide

At the FLASH programming, the programming tool needs 4 signal lines that are DSCL, DSDA, VDD and VSS. When you design the PCB circuits, you should consider the usage of these signal lines for the on-board programming.
Please be careful to design the related circuit of these signal pins because rising/falling timing of DSCL and DSDA is very important for proper programming.



NOTE)

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.

The value of R1 and R2 is recommended value and it varies with circuit of system.

Figure 1.7 PCB design guide for on board programming

2 Block diagram

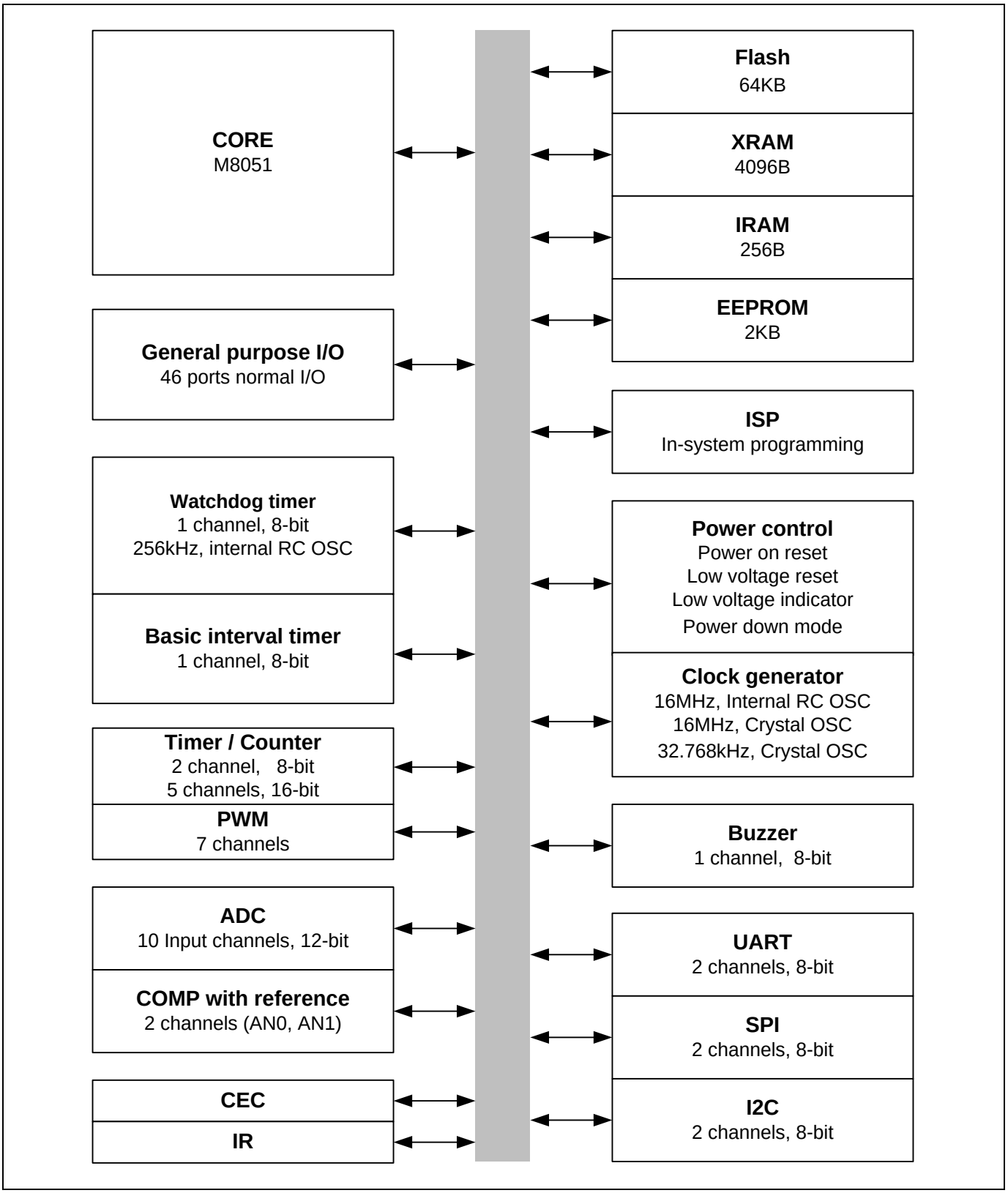
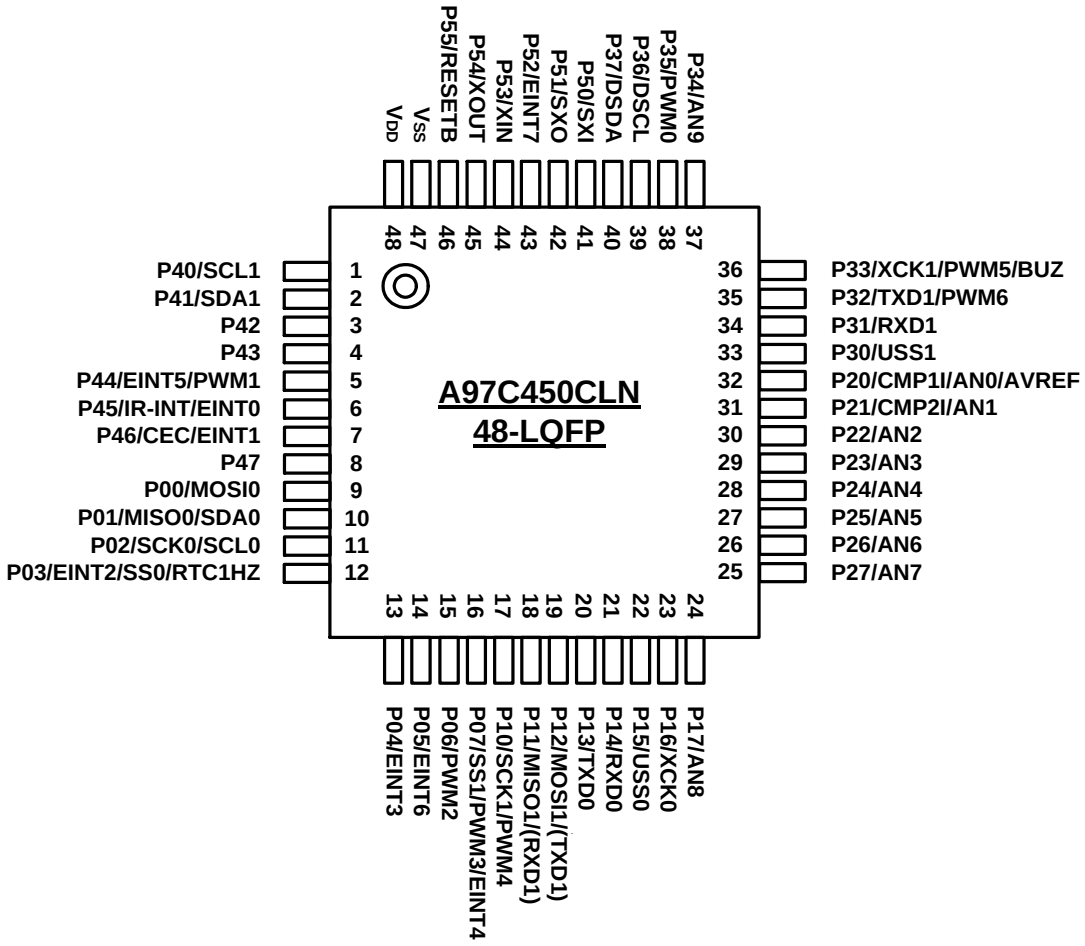


Figure 2.1 Block diagram of A97C450

3 Pin assignment



NOTE)

1. The programmer (E-PGM+, E-PGM+ GANG 4/6) uses P36, P37 pin as DSCL, DSDA.

Figure 3.1 A97C450CLN 48-LQFP pin assignment

4 Package Diagram

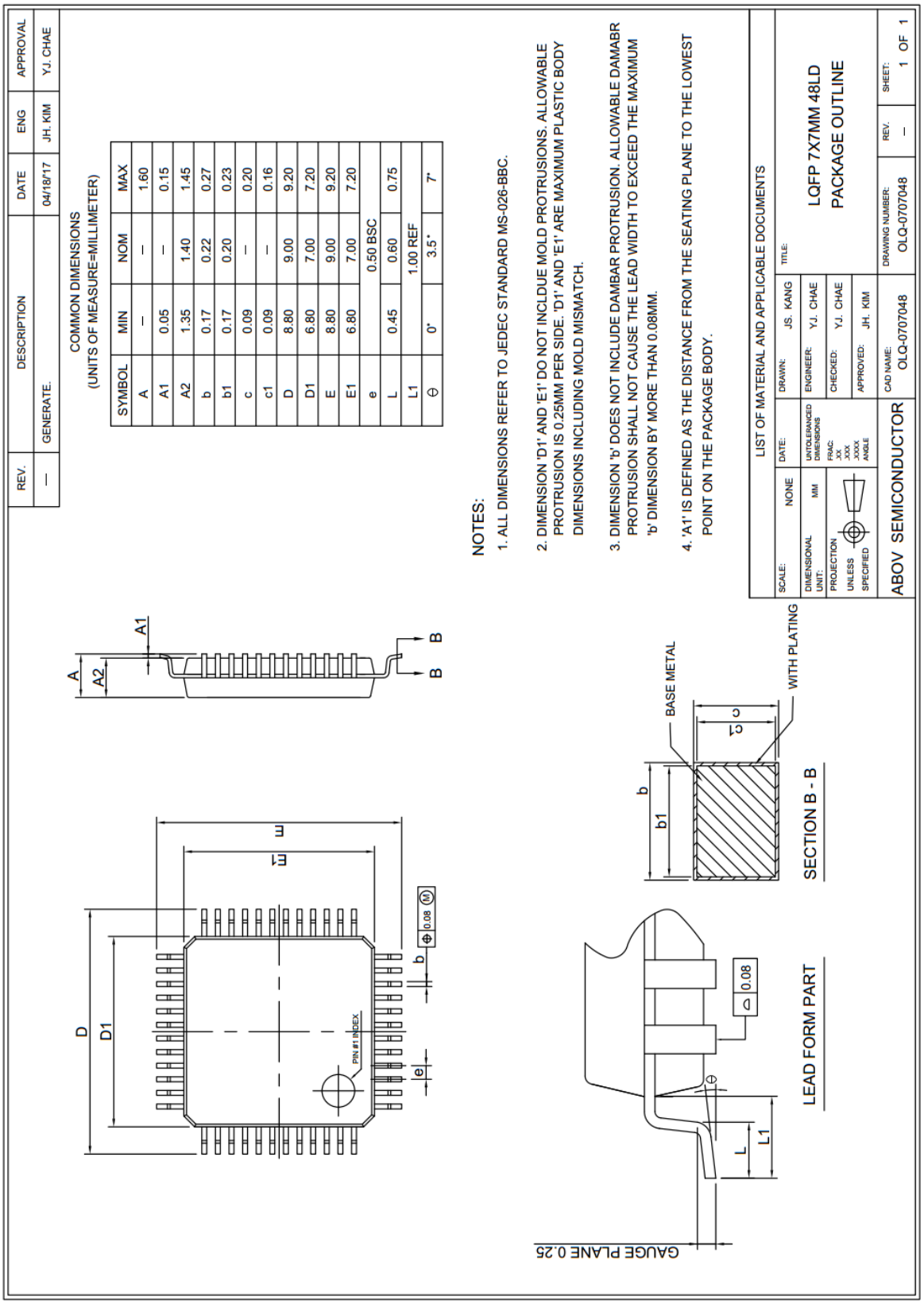


Figure 4.1 48 pin LQFP package

5 Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	Port 0 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	MOSI0
P01				SDA0/MISO0
P02				SCL0/SCK0
P03				EINT2/SS0/RTC1HZ
P04				EINT3
P05				EINT6
P06				PWM2
P07				SS1/PWM3/EINT4
P10	I/O	Port 1 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	SCK1/PWM4
P11				MISO1/(RXD1)
P12				MOSI1/(TXD1)
P13				TXD0
P14				RXD0
P15				USS0
P16				XCK0
P17				AN8
P20	I/O	Port 2 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	CMP1I/AN0/AVref
P21				CMP2I/AN1
P22				AN2
P23				AN3
P24				AN4
P25				AN5
P26				AN6
P27				AN7
P30	I/O	Port 3 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	USS1
P31				RXD1
P32				TXD1/PWM6
P33				XCK1/PWM5/BUZ
P34				AN9
P35				PWM0
P36				DSCL
P37				DSDA
P40	I/O	Port 4 is a bit-programmable I/O port which can be configured as an input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	SCL1
P41				SDA1
P42				P42
P43				P43
P44				EINT5/PWM1
P45				IR-INT/EINT0
P46				CEC/EINT1
P47				

Table 5.1 Normal Pin description

PIN Name	I/O	Function	@RESET	Shared with
P50	I/O	Port 5 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit.	Input	SXI
P51				SXO
P52				EINT7
P53				XIN
P54				XOUT
P55				RESETB
VDD	–	Power input pins	–	–
VSS	–	Power input pins	–	–

Table 5.2 Normal Pin Description (Continued)

Port IO Direction Register(PxIO)	Pull_Up Register (PxPU)	Open Drain Register (PxOD)	**Port output attribute**
ON (1)	OFF (0)	OFF (0)	Push-pull
		ON (1)	Open drain
	ON (1)	OFF (0)	Push-pull
		ON (1)	Internal Pull-Up

Port IO Direction Register	Pull_Up Register	Open Drain Register	**Port Input attribute**
OFF (0)	OFF (0)	X	External condition
	ON (1)	X	Internal Pull-Up

Table 5.3 Port attribute setting (PxIO, PxPU, PxOD, x= Port number (0, 1, 2, 3, 4, 5)

6 Port Structures

6.1 General Purpose I/O Port with Analog Input

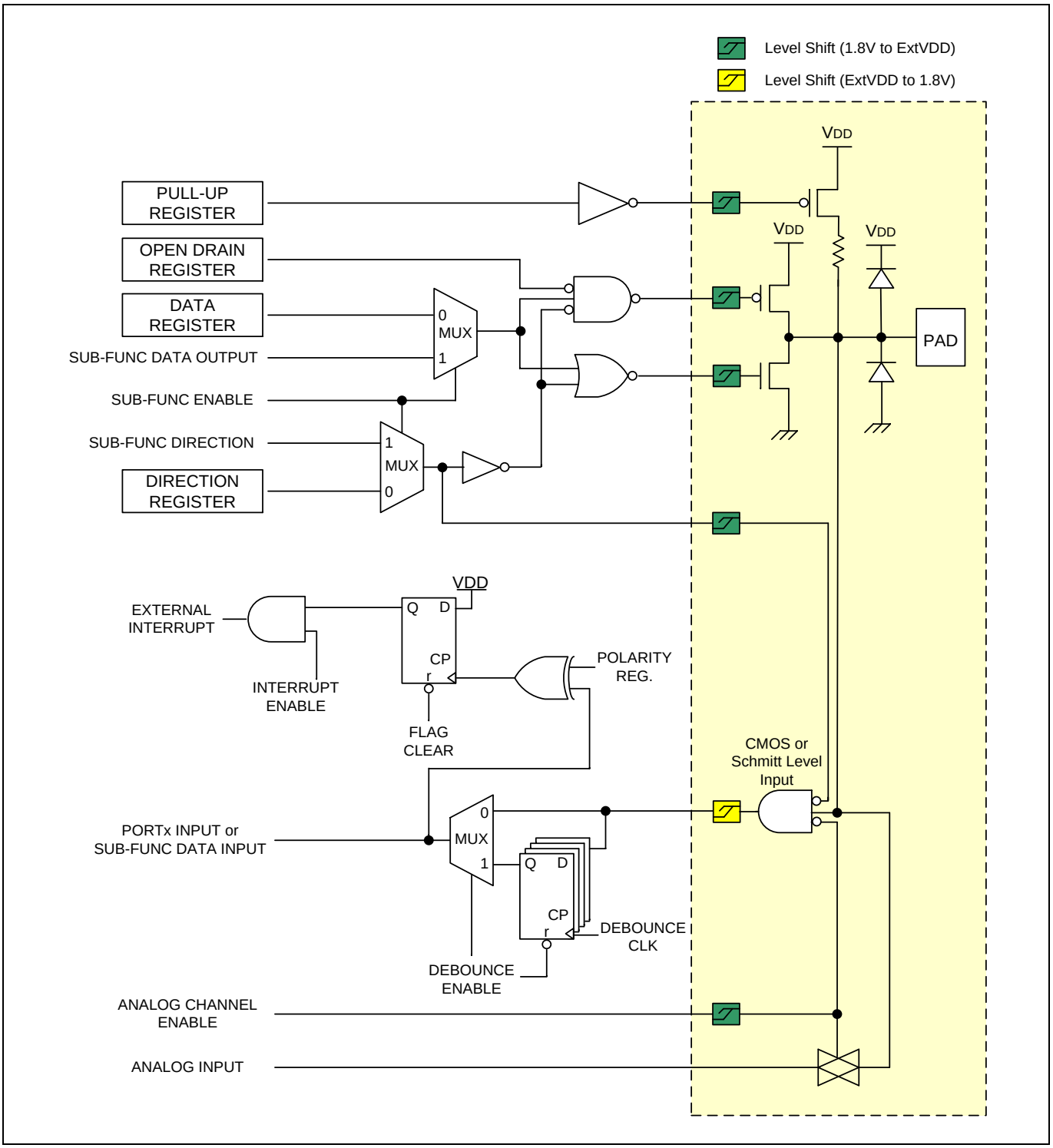


Figure 6.1 General Purpose I/O Port

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	NOTE
Supply Voltage	VDD	-0.3~+6.5	V	–
Normal Voltage Pin	V_I	-0.3~VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3~VDD+0.3	V	
	I_{OH}	-15	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	$\sum I_{OH}$	-80	mA	Maximum current ($\sum I_{OH}$)
	I_{OL}	25	mA	Maximum current sunk by (I_{OL} per I/O pin)
	$\sum I_{OL}$	160	mA	Maximum current ($\sum I_{OL}$)
Total Power Dissipation	P_T	400	mW	–
Storage Temperature	T_{STG}	-65~+150	°C	–

Table 7.1 Absolute Maximum Ratings

NOTE)

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

(T_A = -40°C ~ +85°C)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Operating Voltage	VDD	f_X= 32 ~ 38kHz	Sub Crystal	2.7	–	5.5	V
		f_X= 0.4 ~ 12MHz	Main Crystal	2.7	–	5.5	
		f_X= 1, 2, 4, 8, 16MHz	Internal RC	2.7	–	5.5	
Operating Temperature	T_{OPR}	VDD=2.7~5.5V		-40	–	85	°C

Table 7.2 Recommended Operating Conditions

7.3 A/D Converter Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.7V ~ 5.5V, VSS = 0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Resolution	–	–		–-	12	–	bit
Integral Non-Linear	INL	AVREF= 2.7V – 5.5V ADCCLK= 2MHz		–	–	±6	LSB
Differential Non-Linearity	DNL			–	–	±3	
Zero Offset Error	ZOE			–	–	±5	
Full Scale Error	FSE			–	–	±5	
Conversion Time	t_{CONV}	12-bit resolution, 2MHz		–	30	–	us
Analog Input Voltage	V_{AIN}	–		VSS	–	AVREF	V
Analog Reference Voltage	AVREF	*NOTE 3		2.2	–	VDD	
Analog Input Leakage Current	I_{AIN}	AVREF=5.12V		–	–	2	uA
ADC Operating Current	I_{ADC}	Enable	VDD=5.12V	–	1	2	mA
		Disable		–	–	0.1	uA

Table 7.3 A/D Converter Characteristics

NOTE)

1. Zero offset error is the difference between 0x000 and the converted output for zero input voltage (VSS).
2. Full scale error is the difference between 0xFFF and the converted output for full-scale input voltage (AVREF).
3. When AVREF is lower than 2.7V, the ADC resolution is worse.

7.4 Analog Comparator Characteristics

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Operating Voltage	AVDD	-	2.2	–	5.5	V
Operating Temperature	T_J	-	-40	25	125	℃
Operating Current	$IDD_{(RMS)}$	-	-	30	50	uA
STOP Current	$ISTOP_{(RMS)}$	0.7uA@105℃, 1.5uA@125℃	-	0.05	1.5	uA
Input Offset Voltage	V_{OS}	-	-50	-	+50	mV
Internal VREF stabilization time	t_{WKUP}	-	50	-	-	us
Propagation Delay(t_{PD})	t_{PHL}	@ Overdirve=50mV, AVDD=3.45V	-	0.5	1.0	us
	t_{PLH}		-	0.5	1.0	

Table 7.4 Analog Comparator Characteristics

7.5 Power-On Reset Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.7V ~ 5.5V, VSS = 0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	V_{POR}	–	–	1.4	–	V
VDD Voltage Rising Time	t_R	0.5V to 2.0V	0.05	–	30.0	V/ms
POR Current	I_{POR}	–	–	0.2	–	uA

Table 7.5 Power-on Reset Characteristics

7.6 Low Voltage Reset and Low Voltage Indicator Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.7V ~ 5.5V, VSS = 0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Detection Level	V_{LVR} V_{LVI}	The LVR level is only fixed to Typ. 1.6V but LVI level can be selected to Typ. 2.4V, 2.8V or 3.5V.		–	1.60	1.80	V
				2.20	2.40	2.60	
				2.60	2.80	3.0	
				3.30	3.50	3.70	
Hysteresis	△V	–		–	50	150	mV
Minimum Pulse Width	t_{LW}	–		100	–	–	us
LVR and LVI Current	I_{BL}	Enable	VDD= 3V, RUN Mode	–	30.0	–	uA
		Disable	VDD= 3V	–	–	0.1	

Table 7.6 LVR and LVI Characteristics

7.7 Internal RC Oscillator Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.7V ~ 5.5V, VSS = 0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Frequency	f_{IRC}	V_{DD} = 2.7 – 5.5V		15.76	16	16.24	MHz
Tolerance	–	T_A = 0°C to +50°C	With 0.1uF Bypass capacitor	–	–	±1.5	%
		T_A = -20°C to +85°C				±2.5	
		T_A = -40°C to +85°C				±3.5	
Clock Duty Ratio	T_{OD}	–		40	50	60	%
Stabilization Time	T_{HFS}	–		–	–	100	us
IRC Current	I_{IRC}	Enable		–	0.2	–	mA
		Disable		–	–	0.1	uA

Table 7.7 High Internal RC Oscillator Characteristics

NOTE)

1. A 0.1uF bypass capacitor should be connected to VDD and VSS.

7.8 Internal Watch-Dog Timer RC Oscillator Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.7V ~ 5.5V, VSS = 0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	f_{WDTRC}	–	230	256	282	kHz
Stabilization Time	t_{WDTS}	–	–	–	1	ms
WDTRC Current	I_{WDTRC}	Enable	–	5	–	uA
		Disable	–	–	0.1	

Table 7.8 Internal WDTRC Oscillator Characteristics

7.9 DC Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.7V ~ 5.5V, VSS = 0V, f_{XIN} = 8MHz)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Input High Voltage	V_{IH1}	P0, P1, P2, P3, P4, P5		0.7VDD	–	VDD	V
Input Low Voltage	V_{IL1}	P0, P1, P2, P3, P4, P5		–	–	0.3VDD	V
Output High Voltage	V_{OH1}	VDD= 3.3V, I_{OH}= -4mA, All output ports;		VDD-1.0	–	–	V
	V_{OH2}	VDD= 5.0V, I_{OH}= -10mA, All output ports;		VDD-1.0	–	–	V
Output Low Voltage	V_{OL1}	VDD=3.3V, I_{OL}= 10mA, All output ports;		–	–	1.0	V
	V_{OL2}	VDD=5.0V, I_{OL}= 20mA, All output ports;		–	–	1.0	V
Input High Leakage Current	I_{IH}	All input ports		–	–	1	uA
Input Low Leakage Current	I_{IL}	All input ports		-1	–	–	uA
Pull-Up Resistor	R_{PU1}	VI=0V, T_A= 25°C All Input ports	VDD=5.0V	25	50	100	kΩ
			VDD=3.0V	50	100	200	
OSC feedback resistor	R_{X1}	XIN= VDD, XOUT= VSS T_A= 25°C, VDD= 5V		700	1000	2500	kΩ
	R_{X2}	SXIN=VDD, SXOUT=VSS T_A= 25°C, VDD=5V		6700	13000	29000	
Supply Current	I_{DD1} (RUN)	f_{XIN}= 12MHz	VDD= 5V±10%	–	4.5	9.0	mA
		f_{XIN}= 12MHz	VDD= 3V±10%	–	3.6	6.0	
		f_{IRC}= 16MHz	VDD= 5V±10%	–	4.4	5.5	
	I_{DD2} (IDLE)	f_{XIN}= 12MHz	VDD= 5V±10%	–	2.0	4.0	mA
		f_{XIN}= 12MHz	VDD= 3V±10%	–	1.2	2.0	
		f_{IRC}= 16MHz	VDD= 5V±10%	–	1.2	3.0	
	I_{DD3} (SLP1)	SLEEP1 MODE WDTRC OSC Enable		–	-	1.0	mA
	I_{DD4} (SLP2)	SLEEP2 MODE WDTRC OSC Enable		–	-	300	uA
	I_{DD5} (STOP1)	STOP1 MODE WDTRC OSC Enable, LVR Disable		–	-	60	uA
	I_{DD6} (STOP2)	STOP2 MODE, T_A=25°C WDTRC OSC Disable, LVR Disable		–	5	10	uA

Table 7.9 DC Characteristics

NOTE)

1. Where the f_{XIN} is an external main oscillator, f_{SUB} is an external sub oscillator, the f_{IRC} is an internal RC oscillator and the fx is the selected system clock.

All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.

All supply current items include the current of the power-on reset (POR) block.

7.10 AC Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.7V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESETB Input Low Width	t_{RST}	Input, VDD= 5V	10	–	–	us
Interrupt Input High, Low Width	t_{IWH}, t_{IWL}	All interrupt, VDD= 5V	200	–	–	ns
External Counter Input High, Low Pulse Width	t_{ECWH}, t_{ECWL}	ECn, VDD = 5V (n= 0~7)	200	–	–	
External Counter Transition Time	t_{REC}, t_{FEC}	ECn, VDD = 5V (n= 0~7)	20	–	–	

Table 7.10 AC Characteristics

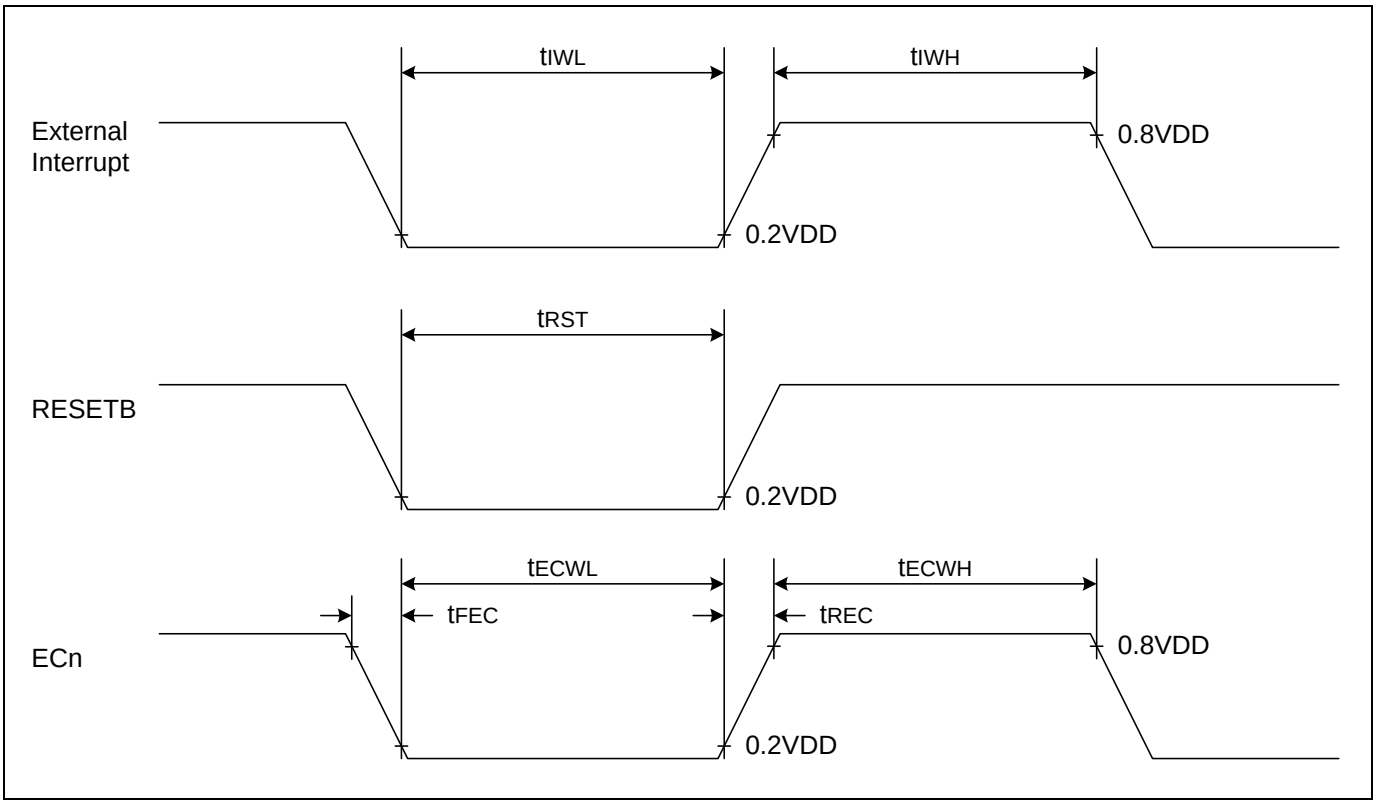


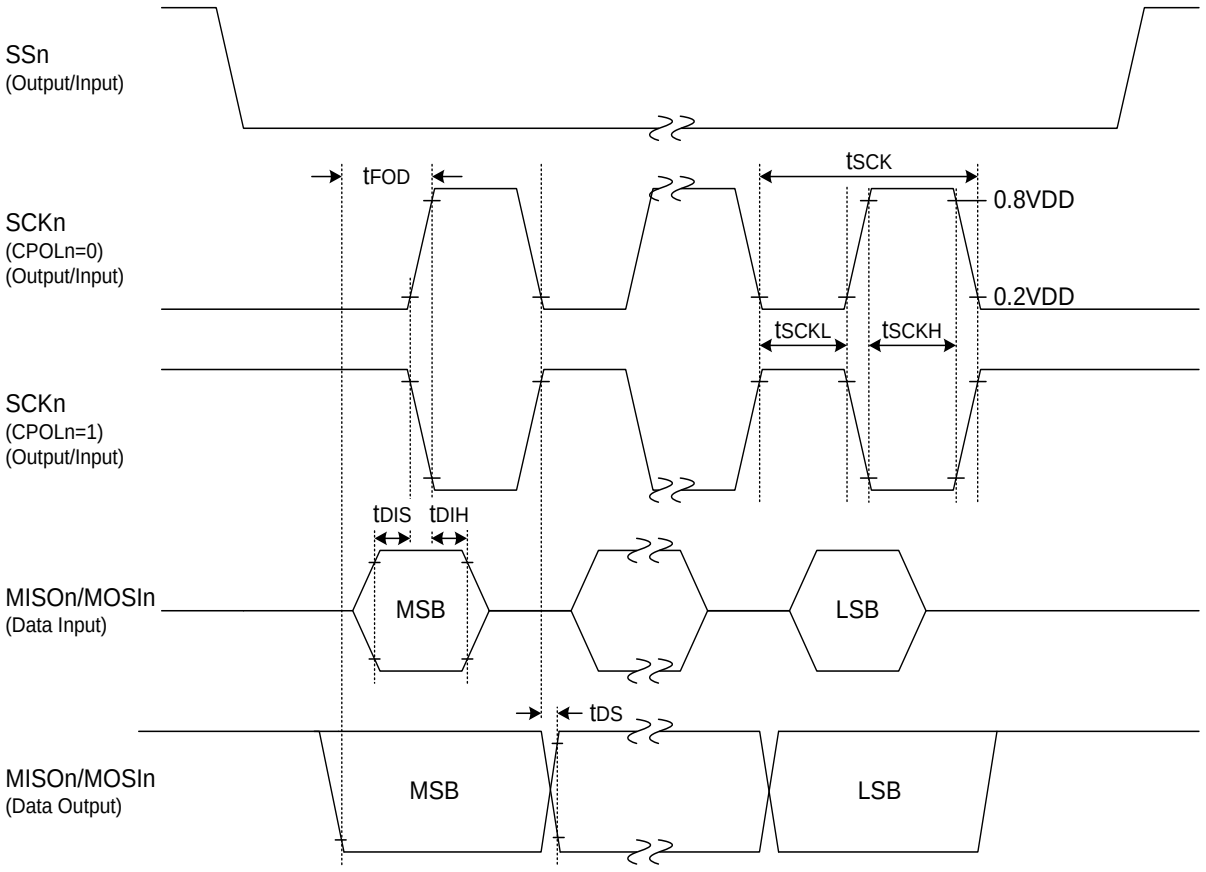
Figure 7.1 AC Timing

7.11 SPI Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.7V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Clock Pulse Period	t_{SCK}	Internal SCK source	200	–	–	ns
Input Clock Pulse Period		External SCK source	200	–	–	
Output Clock High, Low Pulse Width	t_{SCKH}, t_{SCKL}	Internal SCK source	70	–	–	
Input Clock High, Low Pulse Width		External SCK source	70	–	–	
First Output Clock Delay Time	t_{FOD}	Internal/External SCK source	100	–	–	
Output Clock Delay Time	t_{DS}	–	–	–	50	
Input Setup Time	t_{DIS}	–	100	–	–	
Input Hold Time	t_{DIH}	–	150	–	–	

Table 7.11 SPI Characteristics



NOTE)

1. n = 0 and 1

Figure 7.2 SPI Timing

7.12 USART Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.7V ~ 5.5V, f_{XIN} = 8MHz)

Parameter	Symbol	MIN	TYP	MAX	Unit
Serial port clock cycle time	t_{SCK}	1800	$t_{CPU} \times 16$	2200	ns
Output data setup to clock rising edge	t_{S1}	810	$t_{CPU} \times 13$	–	
Clock rising edge to input data valid	t_{S2}	–	–	590	
Output data hold after clock rising edge	t_{H1}	t_{CPU} – 50	t_{CPU}	–	
Input data hold after clock rising edge	t_{H2}	0	–	–	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	720	$t_{CPU} \times 8$	1280	

Table 7.12 USART Characteristics

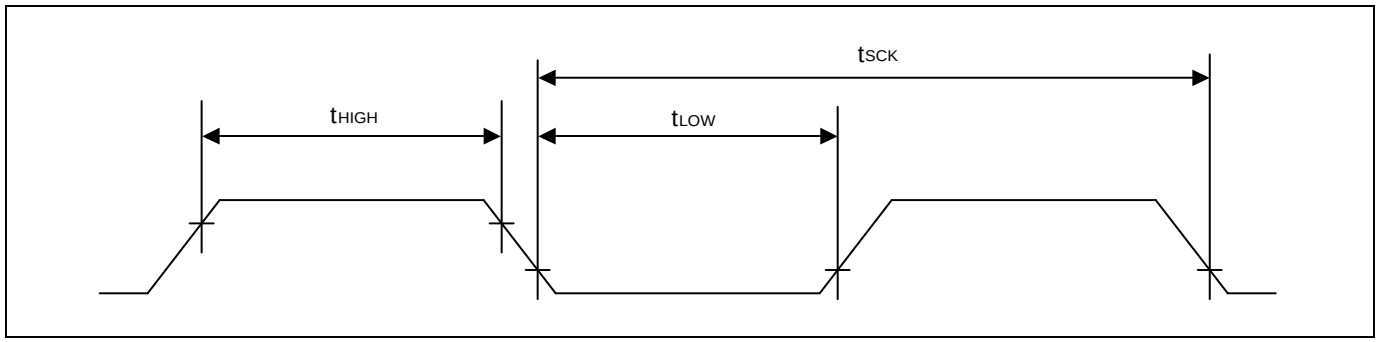


Figure 7.3 Waveform for USART Timing Characteristics

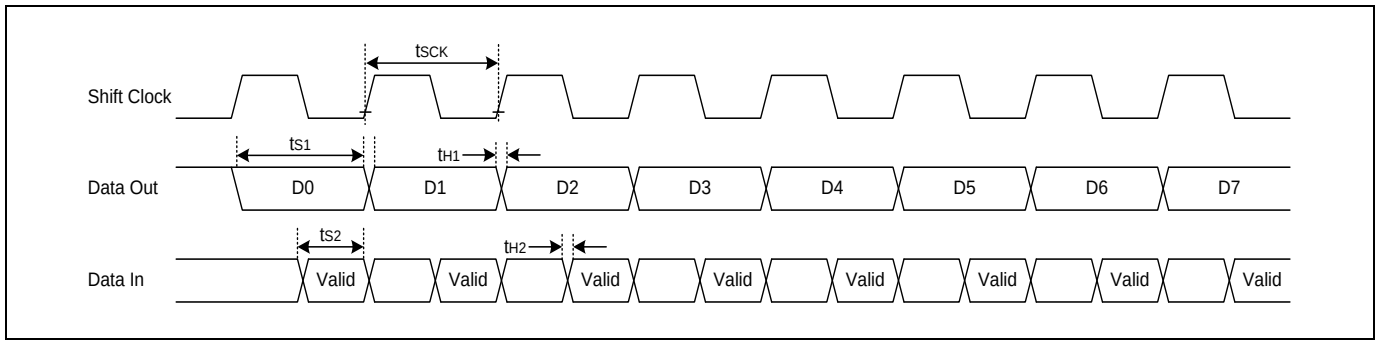


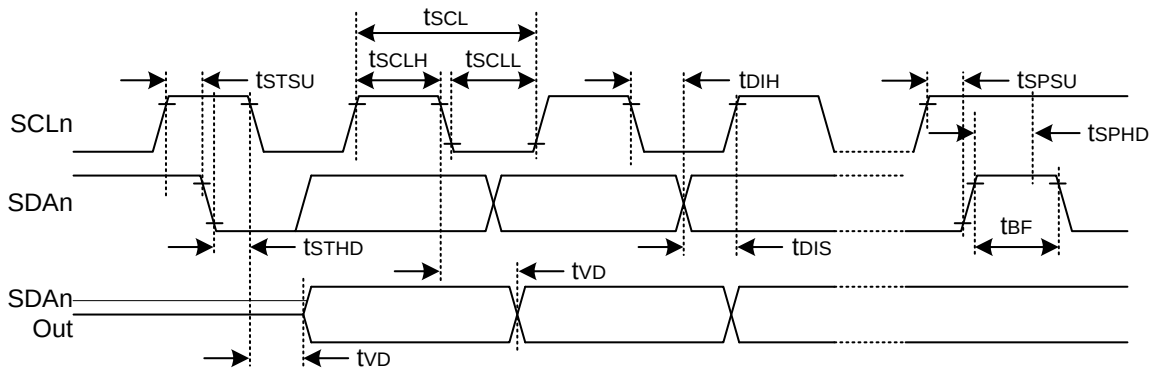
Figure 7.4 Timing Waveform for the USART Module

7.13 I2C Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.7V ~ 5.5V)

Parameter	Symbol	Standard Mode		High-Speed Mode		Unit
		MIN	MAX	MIN	MAX	
Clock frequency	t_{SCL}	0	100	0	400	kHz
Clock High Pulse Width	t_{SCLH}	4.0	–	0.6	–	us
Clock Low Pulse Width	t_{SCLL}	4.7	–	1.3	–	
Bus Free Time	t_{BF}	4.7	–	1.3	–	
Start Condition Setup Time	t_{STSU}	4.7	–	0.6	–	
Start Condition Hold Time	t_{STHD}	4.0	–	0.6	–	
Stop Condition Setup Time	t_{SPSU}	4.0	–	0.6	–	
Stop Condition Hold Time	t_{SPHD}	4.0	–	0.6	–	
Output Valid from Clock	t_{VD}	0	–	0	–	
Data Input Hold Time	t_{DIH}	0	–	0	1.0	
Data Input Setup Time	t_{DIS}	250	–	100	–	ns

Table 7.13 I2C Characteristics



NOTE)

1. n= 0 and 1

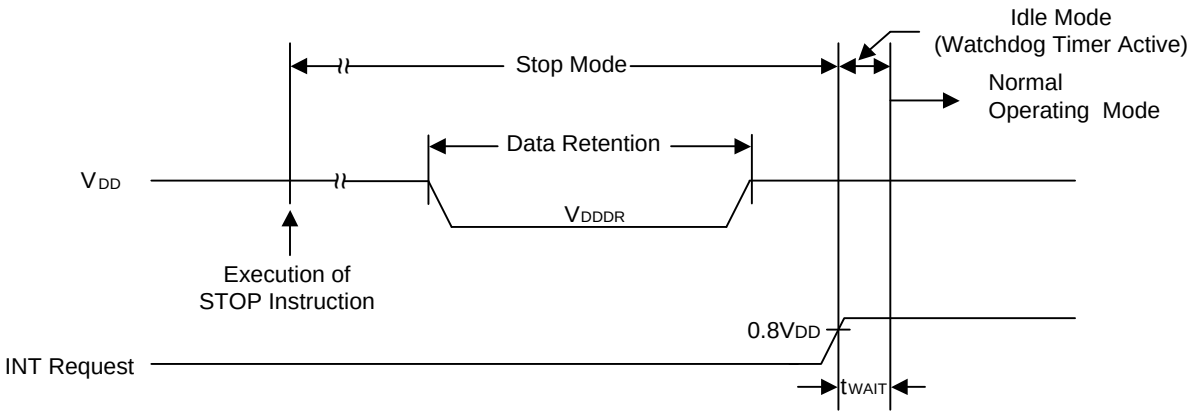
Figure 7.5 I2C Timing(DIS_SDAH=0)

7.14 Data Retention Voltage in Stop Mode

(T_A = -40°C ~ +85°C, VDD = 2.7V ~ 5.5V)

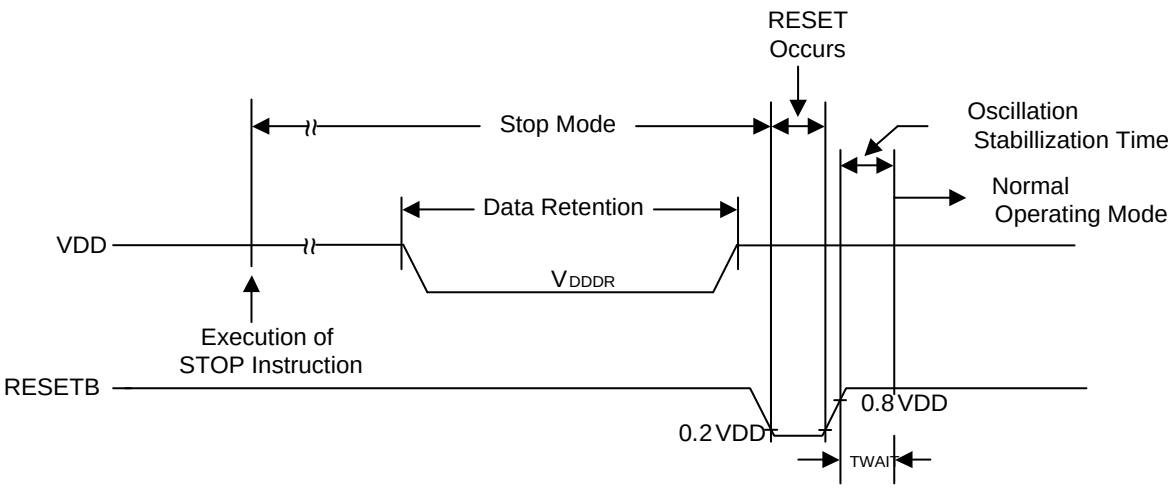
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data retention supply voltage	V_{DDDR}	–	2.7	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDR} = 2.7V(T_A = 25°C), Stop mode	–	–	1	uA

Table 7.14 Data Retention Voltage in Stop Mode



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 7.6 Stop Mode Release Timing when Initiated by an Interrupt



NOTE : tWAIT is the same as (4096 X 4 X 1/fx) (16.4ms @ 1MHz)

Figure 7.7 Stop Mode Release Timing when Initiated by RESETB

7.15 Internal Flash ROM Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.7V ~ 5.5V, VSS = 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Sector Write Time	t_{FSW}	–	–	2.5	2.7	ms
Sector Erase Time	t_{FSE}	–	–	2.5	2.7	
Code Write Protection Time	t_{FHL}	–	–	2.5	2.7	
Page Buffer Reset Time	t_{FBR}	–	–	–	5	us
Flash Programming Frequency	f_{PGM}	–	0.4	–	–	MHz
Endurance of Write/Erase	NF_{WE}	–	–	–	10,000	cycles
Flash Data Retention Time	t_{RT}	–	10			years

Table 7.15 Internal Flash Rom Characteristics

7.16 Internal EEPROM Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.7V ~ 5.5V, VSS = 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Sector/Byte Write Time	t_{FSW}	–	–	2.5	2.7	ms
Sector/Byte Erase Time	t_{FSE}	–	–	2.5	2.7	
Data Write Protection Time	t_{FHL}	–	–	2.5	2.7	
Page Buffer Reset Time	t_{FBR}	–	–	–	5	us
EEPROM Programming Frequency	f_{PGM}	–	0.4	–	–	MHz
Endurance of Write/Erase	NF_{WE}	–	–	–	300,000	cycles
EEPROM Data Retention Time	t_{RT}	–	10			years

Table 7.16 Internal Flash Rom Characteristics

7.17 Input/Output Capacitance

(T_A = -40°C ~ +85°C, VDD = 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Capacitance	C_{IN}	fx= 1MHz Unmeasured pins are connected to VSS	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

Table 7.17 Input/Output Capacitance

7.18 Main Clock Oscillator Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.7V ~ 5.5V)

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Main oscillation frequency	2.7V – 5.5V	0.4	–	12.0	MHz
Ceramic Oscillator	Main oscillation frequency	2.7V – 5.5V	0.4	–	12.0	MHz
External Clock	XIN input frequency	2.7V – 5.5V	0.4	–	12.0	MHz

Table 7.18 Main Clock Oscillator Characteristics

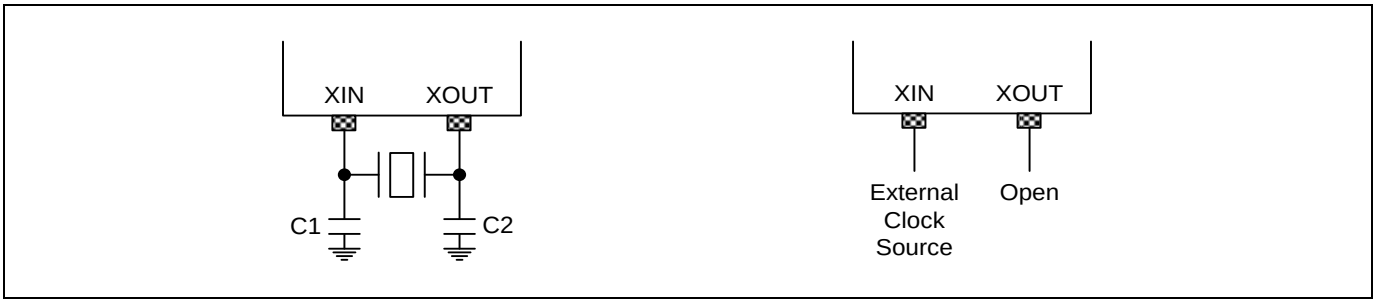


Figure 7.8 Crystal/Ceramic Oscillator & External Clock Circuit

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V)

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	fx > 4MHz, VDD = 2.7V ~ 5.5V,	–	–	15	ms
	fx > 1MHz, VDD = 2.7V, T_A=-40°C			60	
Ceramic	-	–	–	10	ms
External Clock	f_{XIN} = 0.4 to 8MHz XIN input high and low width (t_{XH}, t_{XL})	42	–	1250	ns

Table 7.19 Main Oscillation Stabilization Characteristics

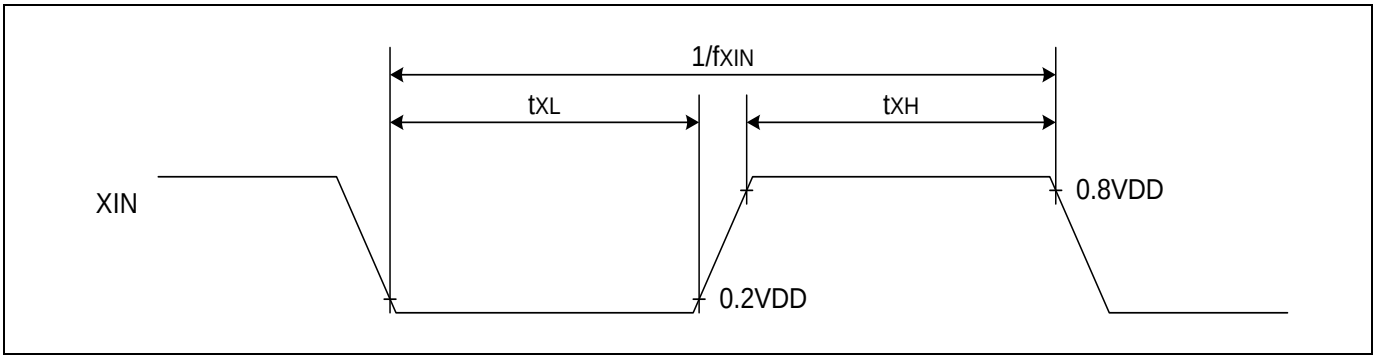


Figure 7.9 Clock Timing Measurement at XIN

7.19 Sub Clock Oscillator Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.7V ~ 5.5V)

Parameter	Symbol	MIN	TYP	MAX	Unit	Condition
Sub oscillation frequency	f_{SUB}	32	32.768	38	kHz	Crystal
SXIN input frequency	f_{SUB}	32	–	100	kHz	External Clock
Operating Current	I_{DD}		3	5	uA	-
External Load Capacitor	C_L	5	15	35	pF	-
Feedback resistance	R_{FB}	6.7	13.7	29	MΩ	
Crystal Input (Low)	V_{IL}			0.2*V_{DDINT}	V	@Max. Current Mode @V_{DDINT} = Typ. 1.85V (on-chip LDO regulator Output)
Crystal Input (High)	V_{IH}	0.8*V_{DDINT}			V	
Crystal Output (Low)	V_{OL}			0.2*V_{DDINT}	V	
Crystal Output (High)	V_{OH}	0.8*V_{DDINT}			V	
Output Clock Duty	D	45	50	55	%	-
Input Swing Level (Peak to Peak)	V_{SW}	1			V	-

Table 7.20 Sub Clock Oscillator Characteristics

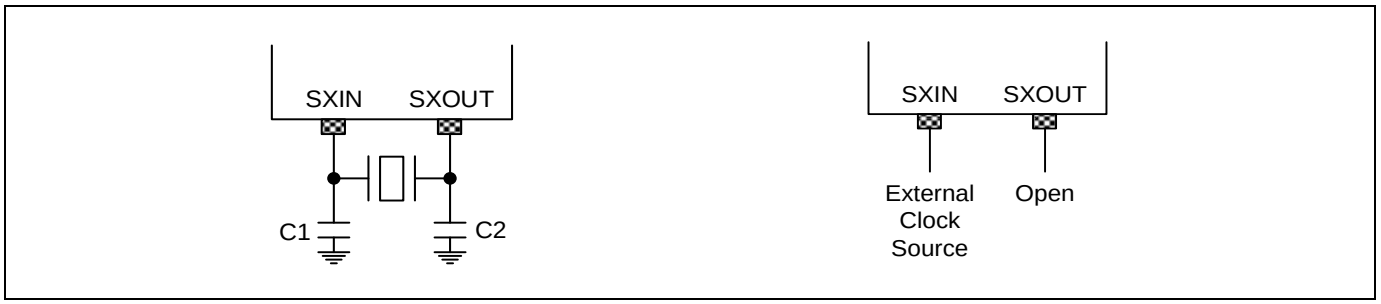


Figure 7.10 Sub Crystal Oscillator & External Clock Cuircit

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V)

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	–	–	–	10	s
External Clock	SXIN input high and low width (t_{XH}, t_{XL})	5	–	15	us

Table 7.1 Sub Oscillation Stabilization Characteristics

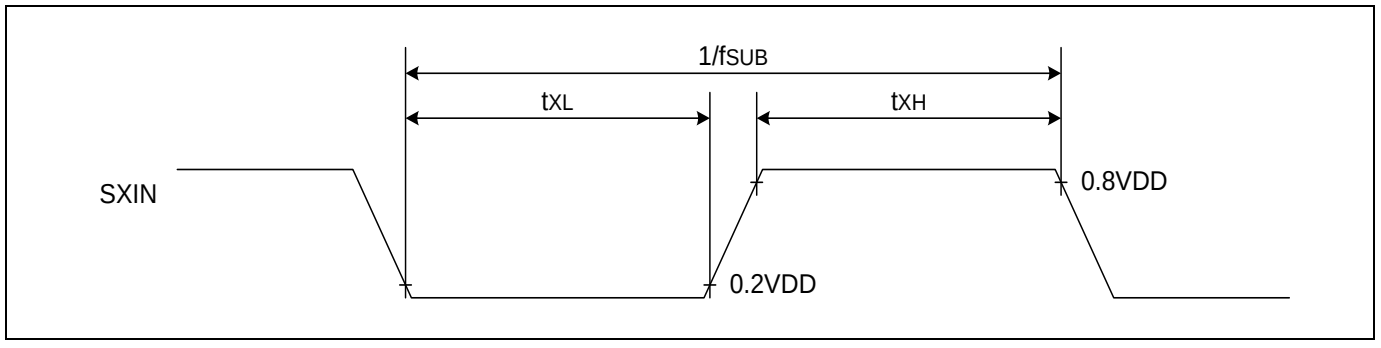


Figure 7.11 Clock Timing Measurement at SXIN

7.20 Operating Voltage Range

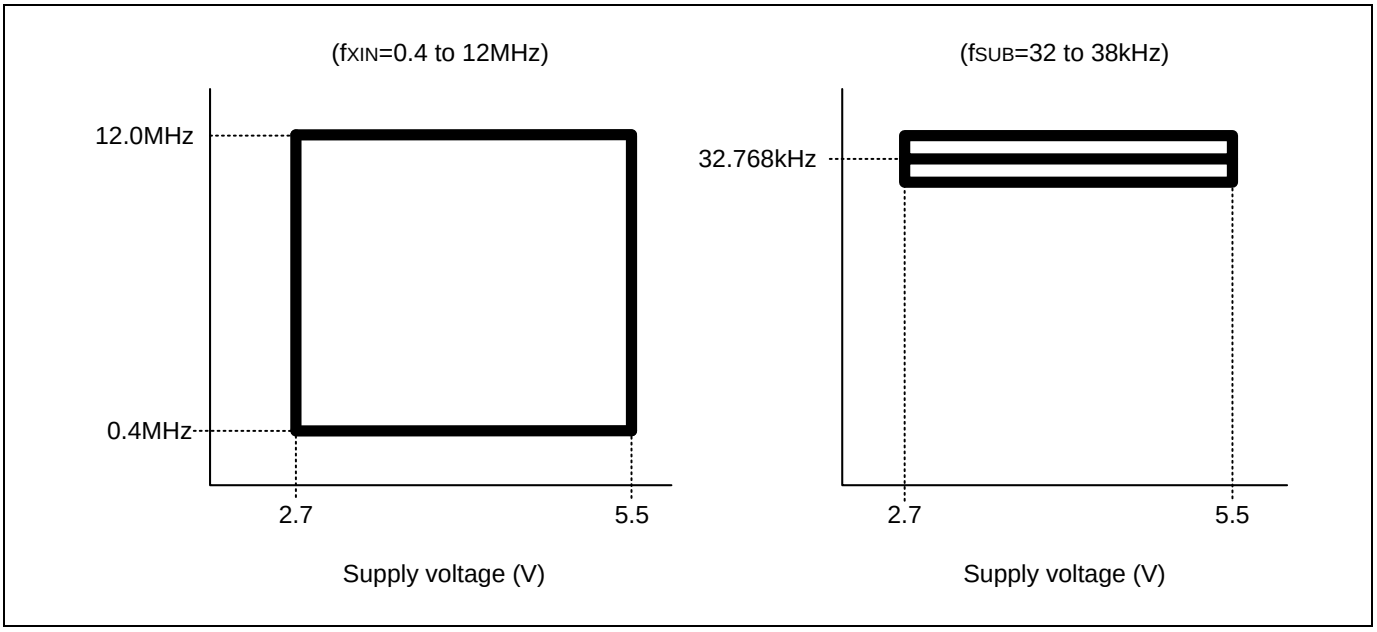


Figure 7.12 Operating Voltage Range

7.21 Recommended Circuit and Layout

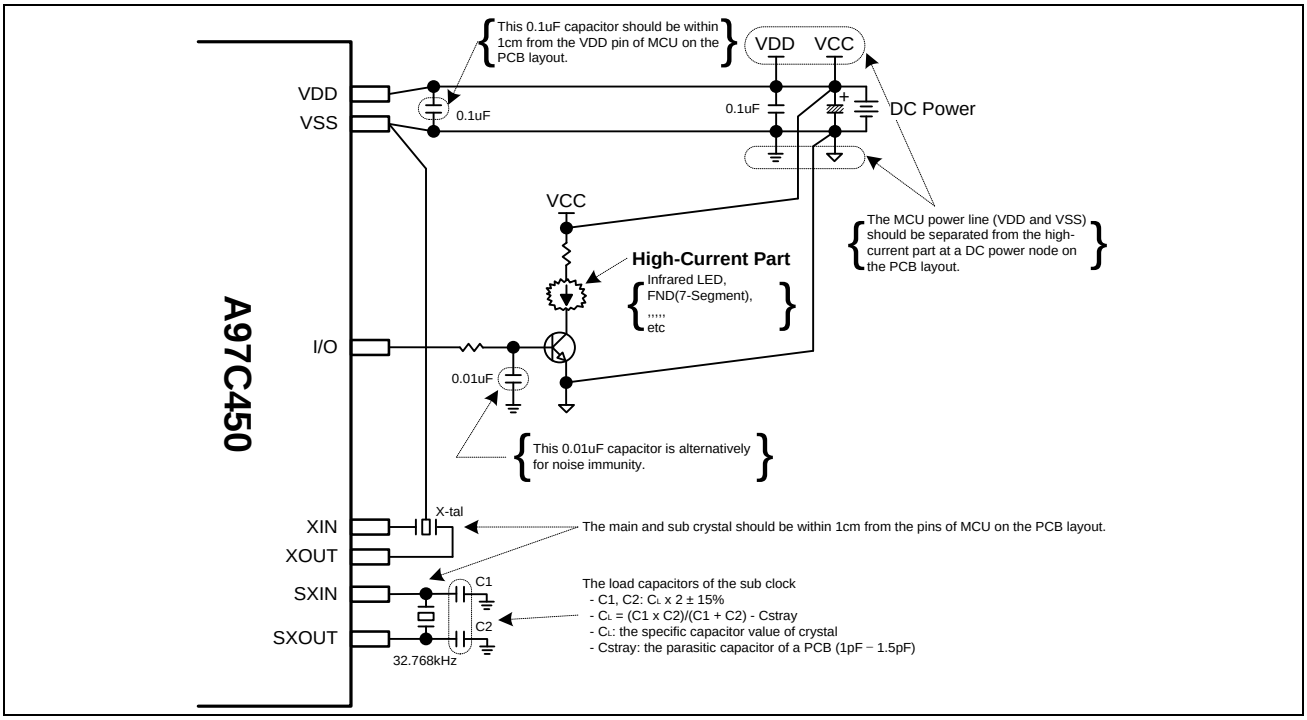
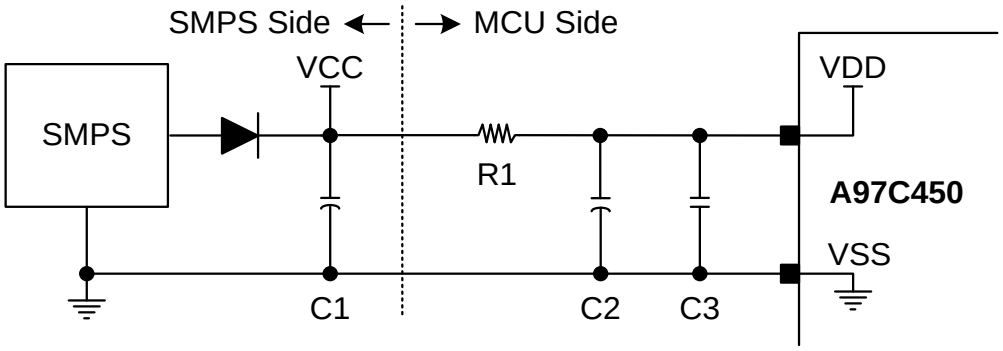


Figure 7.13 Recommended Circuit and Layout

7.22 Recommended Circuit and Layout with SMPS Power



1. The C1 capacitor is to flatten out the voltage of the SMPS power, VCC.
   √ Recommended C1: 470uF/25V more.
2. The R1 and C2 are the RC filter for VDD and suppress the ripple of VCC.
   √ Recommended R1: 10Ω - 20Ω
   √ Recommended C2: 47uF/25V more
   √ The R1 and C2 should be as close by the C3 as possible.
3. The C3 capacitor is used for temperature compensation because an electrolytic capacitor becomes worse characteristics at low temperature.
   √ Recommended C3: ceramic capacitor 2.2uF more
   √ The C3 should be within 1cm from VDD pin of MCU on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc) when the SMPS supplies the VDD of MCU.

Figure 7.14 Recommended Circuit and Layout with SMPS Power

7.23 Typical Characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

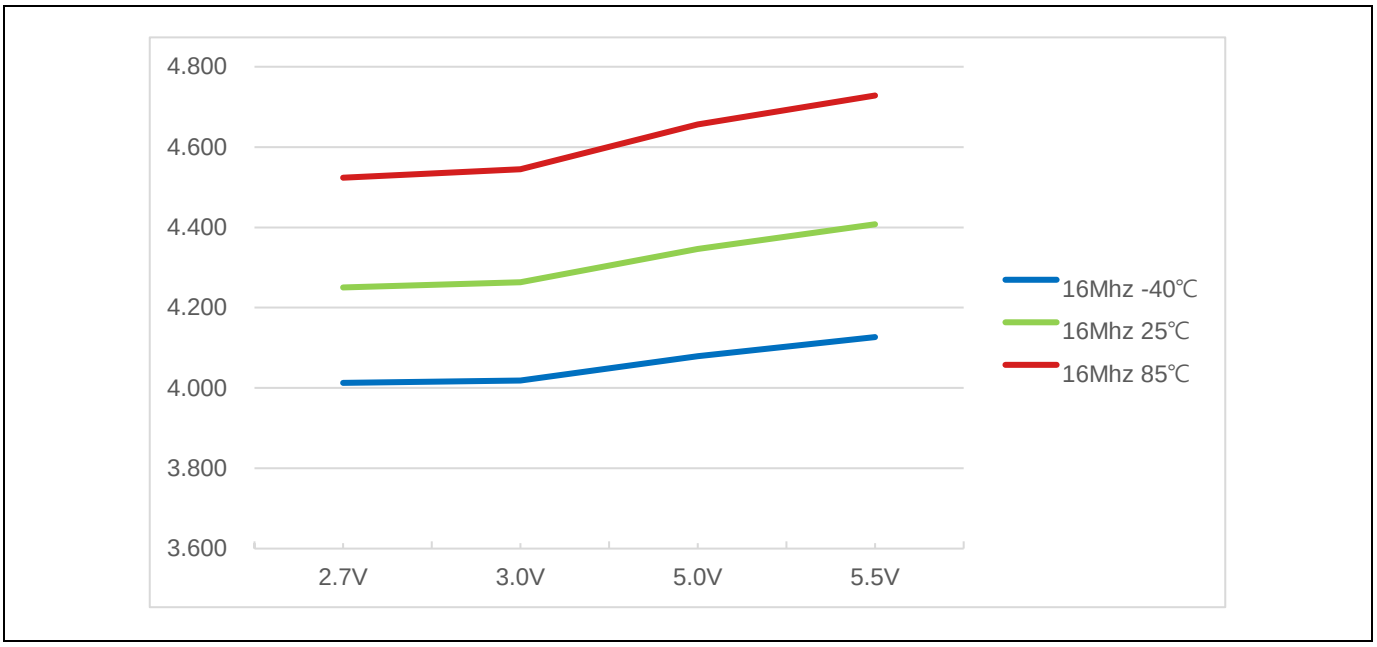


Figure 7.15 RUN (IDD1) Current

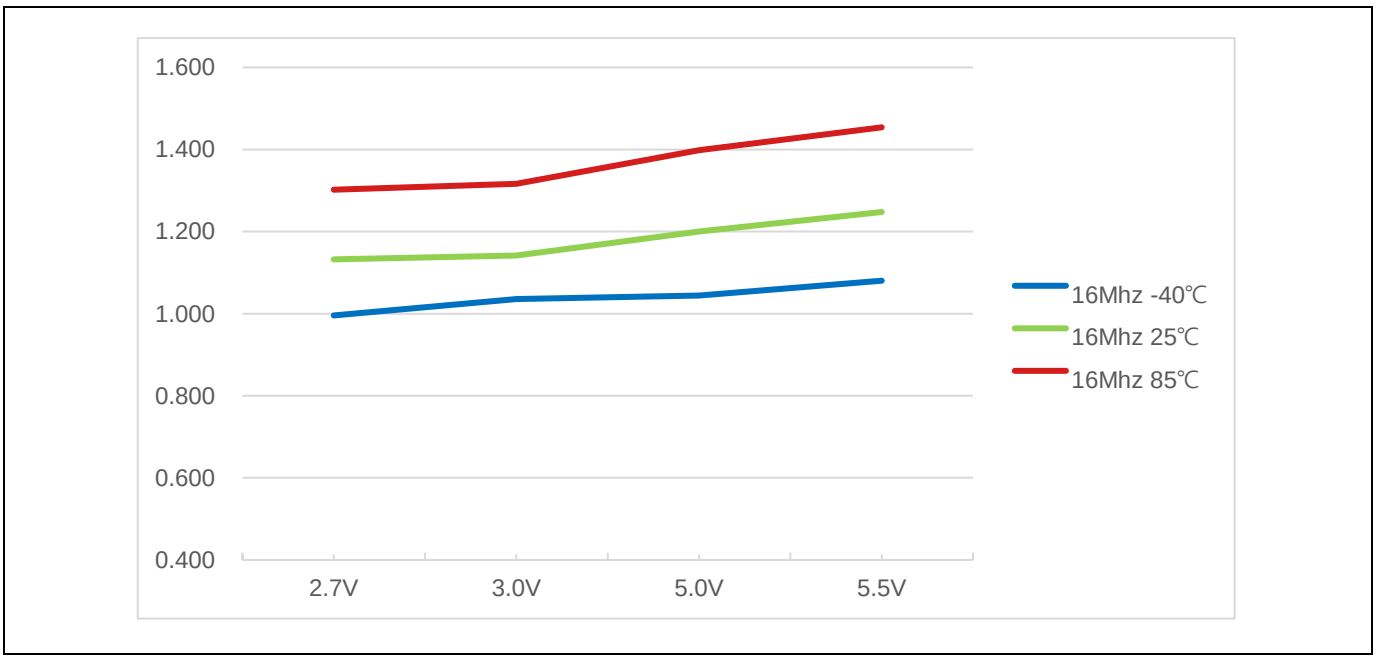


Figure 7.16 IDLE (IDD2) Current

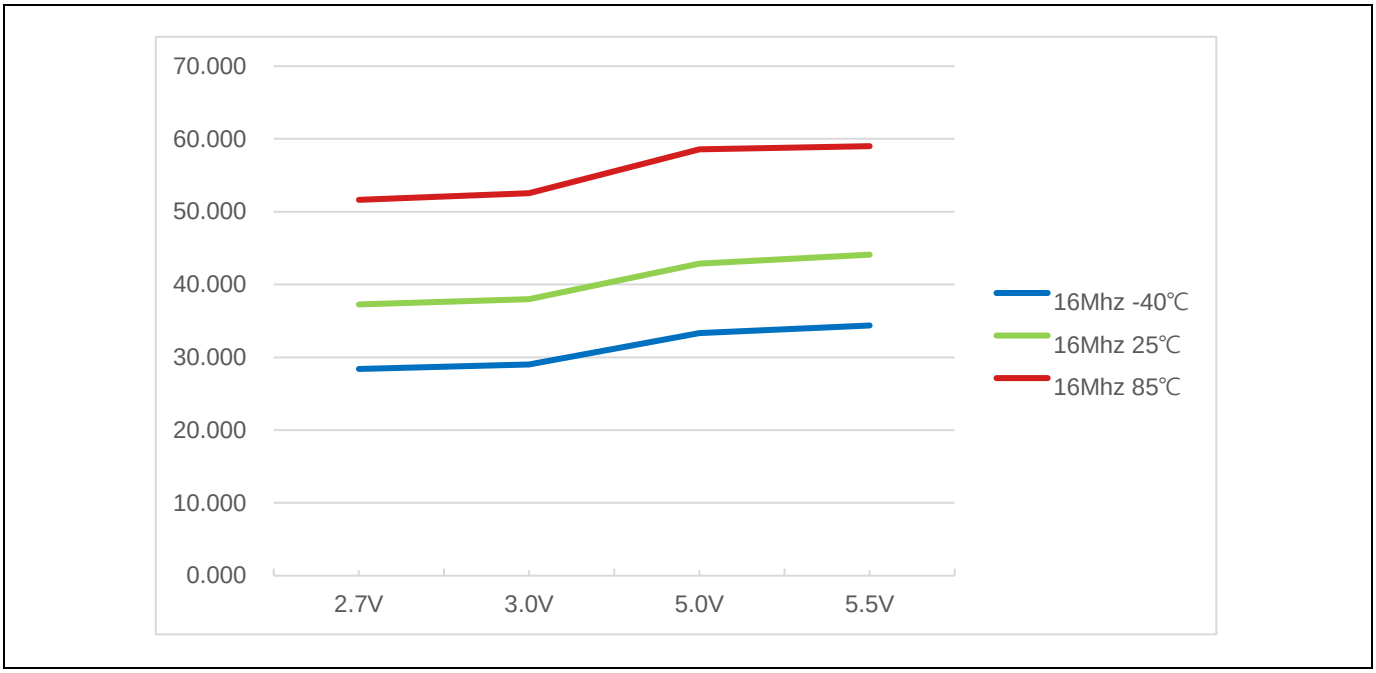


Figure 7.17 STOP1 (IDD5) Current

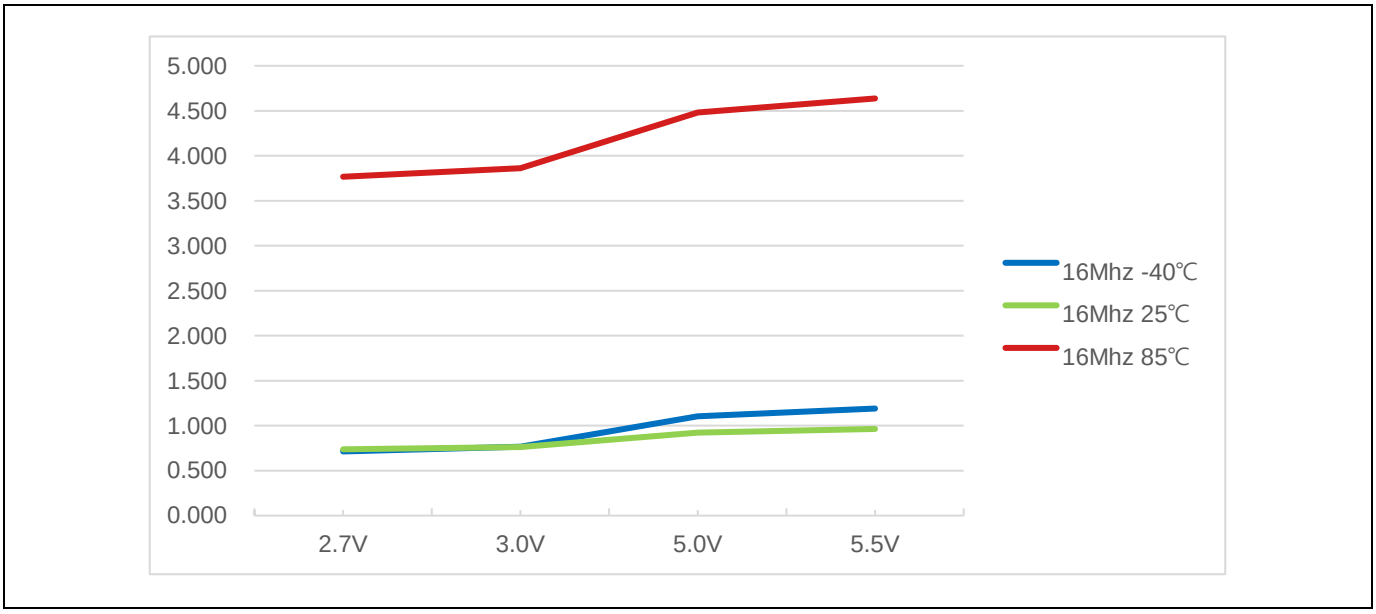


Figure 7.18 STOP2 (IDD6) Current

Table of contents