Ver 1.3

4-BIT SINGLE CHIP MICROCOMPUTERS

ADAM42X11XX

USER`S MANUAL

- ADAM42P1120
- ADAM42P1116
- ADAM42C1116
- ADAM42P1108
- ADAM42C1108

ETACHIPS Co., Ltd.

0. REVISION HISTORY

Version	Date	Description
VER 1.0	2007.06.25	-. Public Release.
VER 1.1	2008.08.11	-. Remove the PG option of the Configuration Option bit.
VER 1.2	2008.12.18	-. Add the Mask ROM Version (ADAM42C11XX) -. Add the description of using the bit access instruction for I/O data register. -. Add the caution about using two INT1 pins.
VER 1.3	2009.06.05	-. Add the package type of 20TSSOP. (ADAM42P1120T)

1. OVERVIEW

The ADAM42X11XX is the high speed and low voltage operating 4-bit single chip microcomputer. This chip contains ADAM42 core, ROM, RAM, input/output ports , two timer/counters , 12-bit A/D converter, etc.

The ADAM42P11XX is OTP Version and the ADAM42C11XX is the Masked ROM Version. But the ADAM42C1120 is not supported.

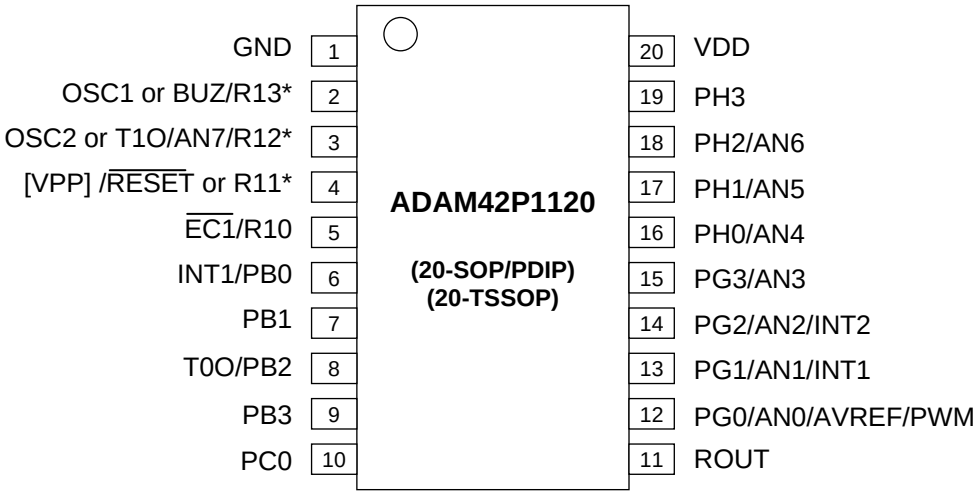
1.1. Features

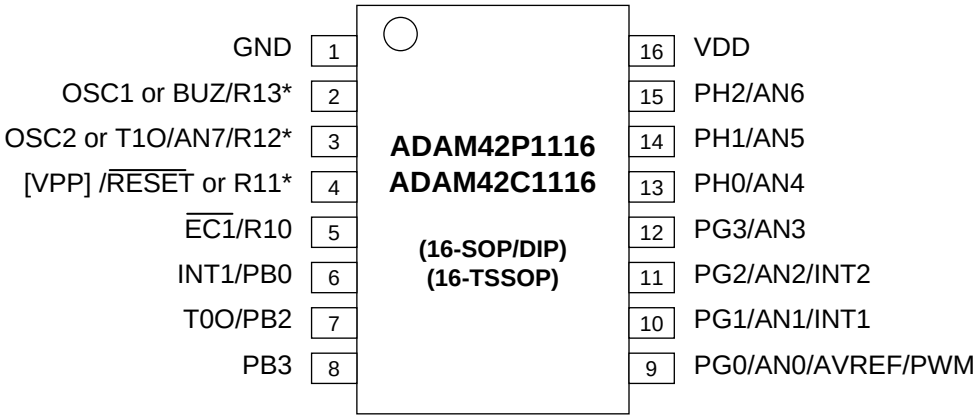
- Instruction Execution Time
  - 1us @ Xin=4MHz
- Program Memory Area (ROM)
  - 4K Bytes (2,048 x 16bit)
- Data memory(RAM)
  - 256 nibble (256 x 4bit)
- 16-Bit Table read Instruction.
- A/D Converter
  - 12Bit * 8ch ---- ADAM42P1116/ADAM42P1120/ADAM42C1116
  - 12Bit * 4ch ---- ADAM42P1108/ADAM42C1108
- Timer
  - Timer / Counter : 8Bit * 2ch (16Bit * 1ch)
  - Carrier Generator : 8Bit * 1ch
  - Watch Dog Timer : 19Bit * 1ch
- One programmable Buzzer Driving Port
- Oscillator Type
  - Crystal / Ceramic Resonator
  - External Clock Input
  - External RC Oscillator
  - Internal RC Oscillator (750kHz, 1.5MHz, 3MHz, 6MHz selectable)
- Power On Reset
- Power Saving Operation Modes
  - STOP
  - SLEEP
  - RCWDT
- 7 Interrupt Source including 2 external Interrupts.
- Operating Voltage Range
  - 2.0 ~ 5.5 V @ 4MHz
  - 2.5 ~ 5.5 V @ 8MHz
- Low Voltage Detection Reset Circuit
- Low Voltage Detection Indication Circuit (3 level)

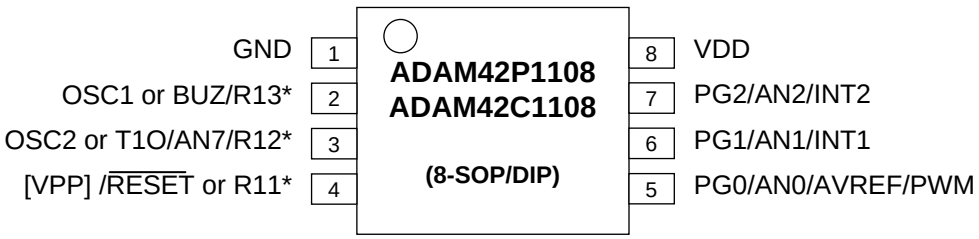
Series	**ADAM42P1120 ---**	**ADAM42P1116 ADAM42C1116**	**ADAM42P1108 ADAM42C1108**
Program memory	2,048 x 16	←	←
Data memory	256 x 4	←	←
I/O ports	16	14	6
Output ports	2	-	-
Package	20-SOP/PDIP/TSSOP	16-SOP/DIP/TSSOP	8-SOP/PDIP

Table 1.1 ADAM42X11XX series members

1.2. Pin Assignments (top view)

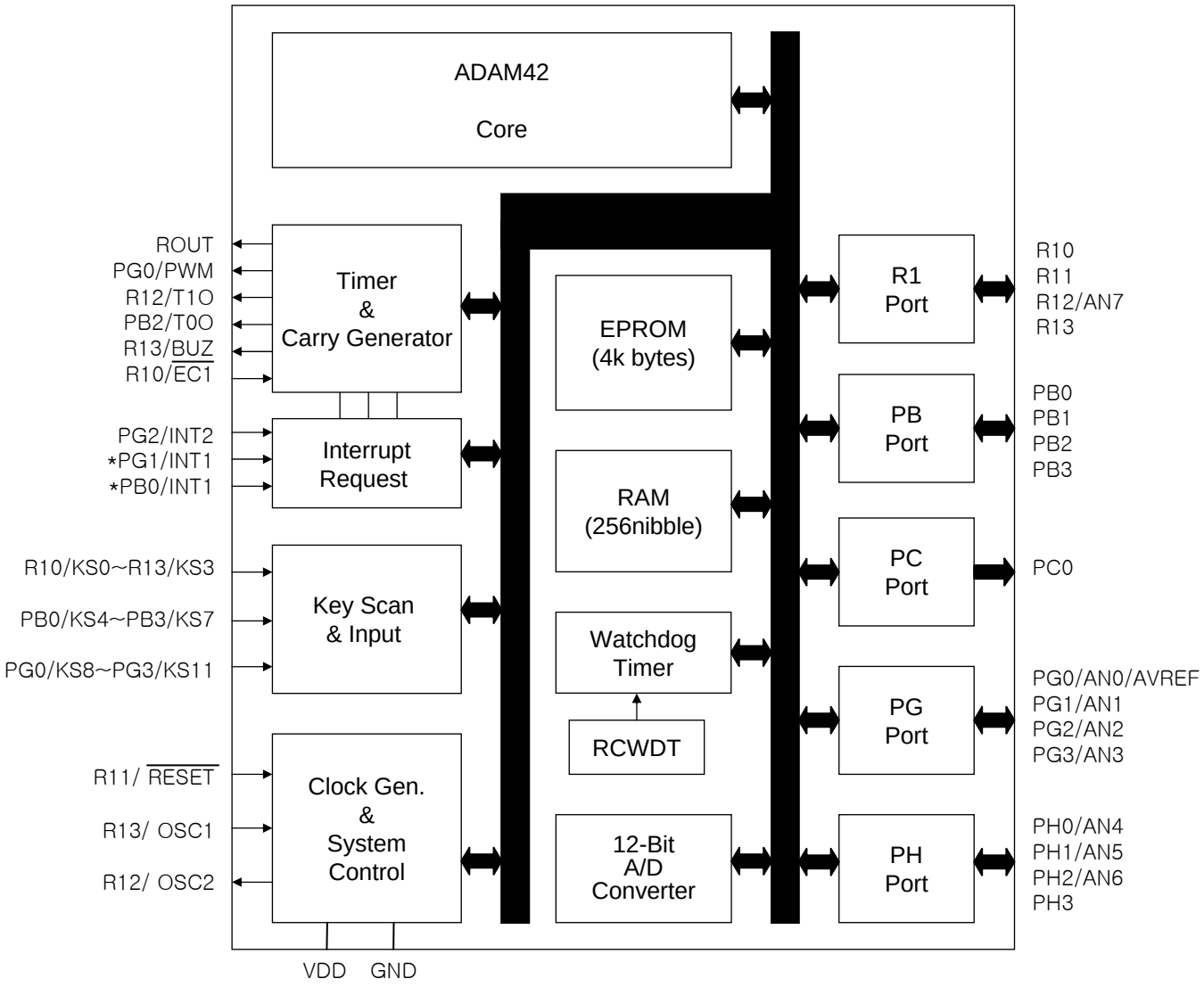






- **R11 is open drain N-MOS Output only.**
- *** means option by the Configuration Option bits.**
- **INT1/PB0 and INT1/PG1 must be used by only one pin at a application.**

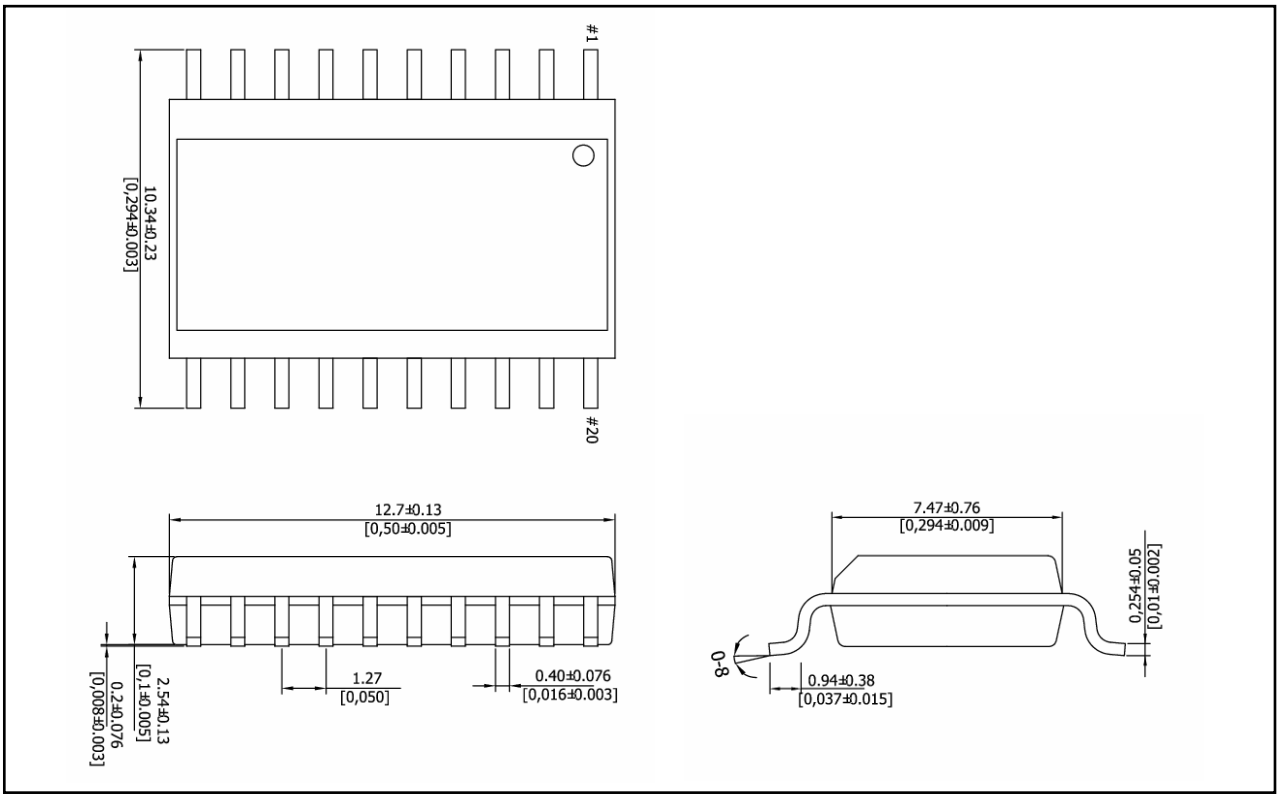
1.3. Block Diagram



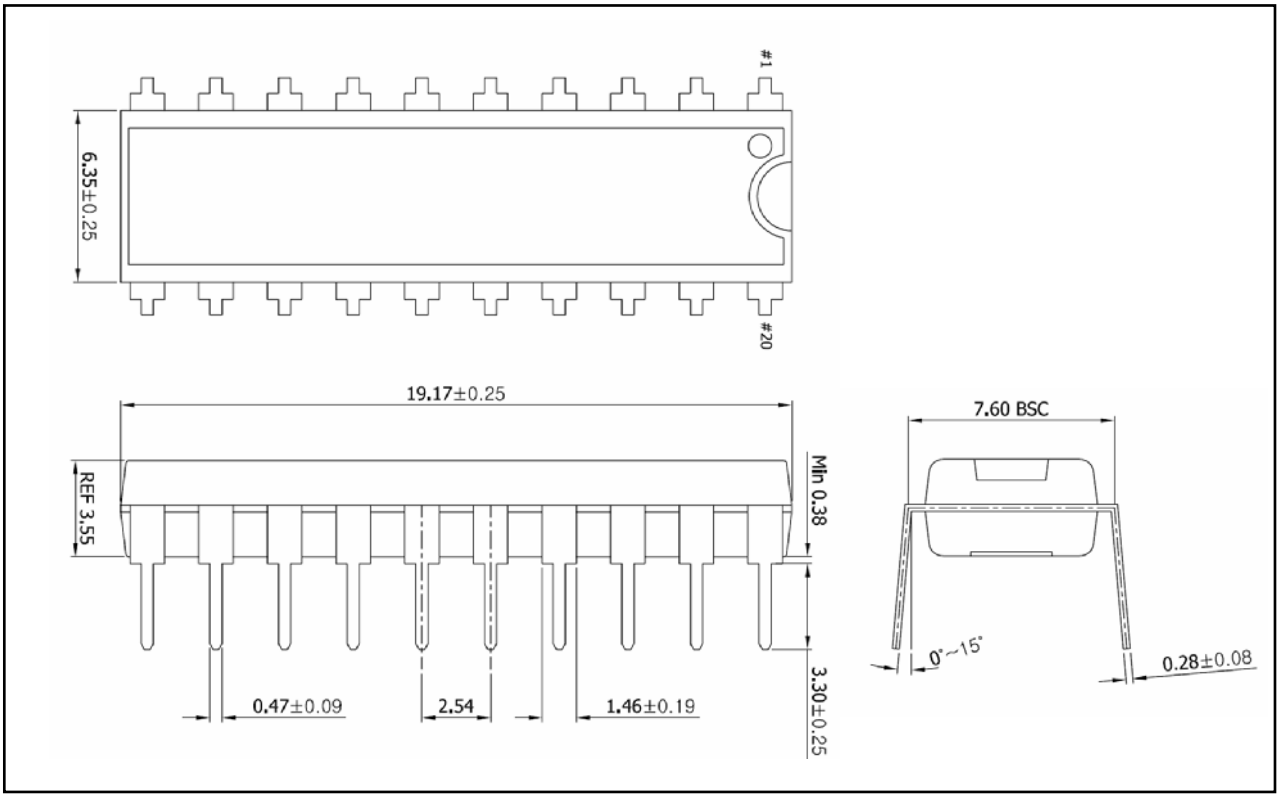
* **INT1/PB0 and INT1/PG1 must be used by only one pin at a application.**

1. OVERVIEW

1.4. PKG Dimension

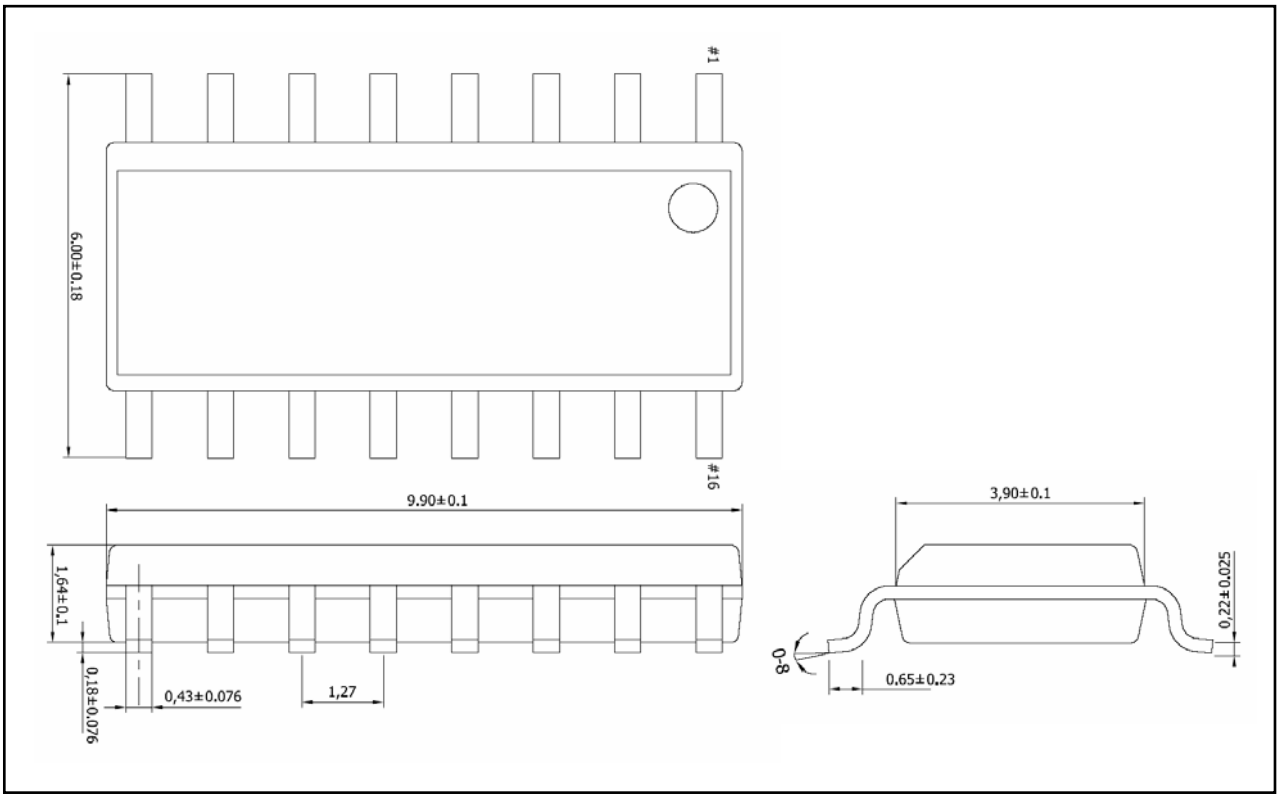


20 SOP (300Mil) Pin Dimension (dimensions in millimeters)

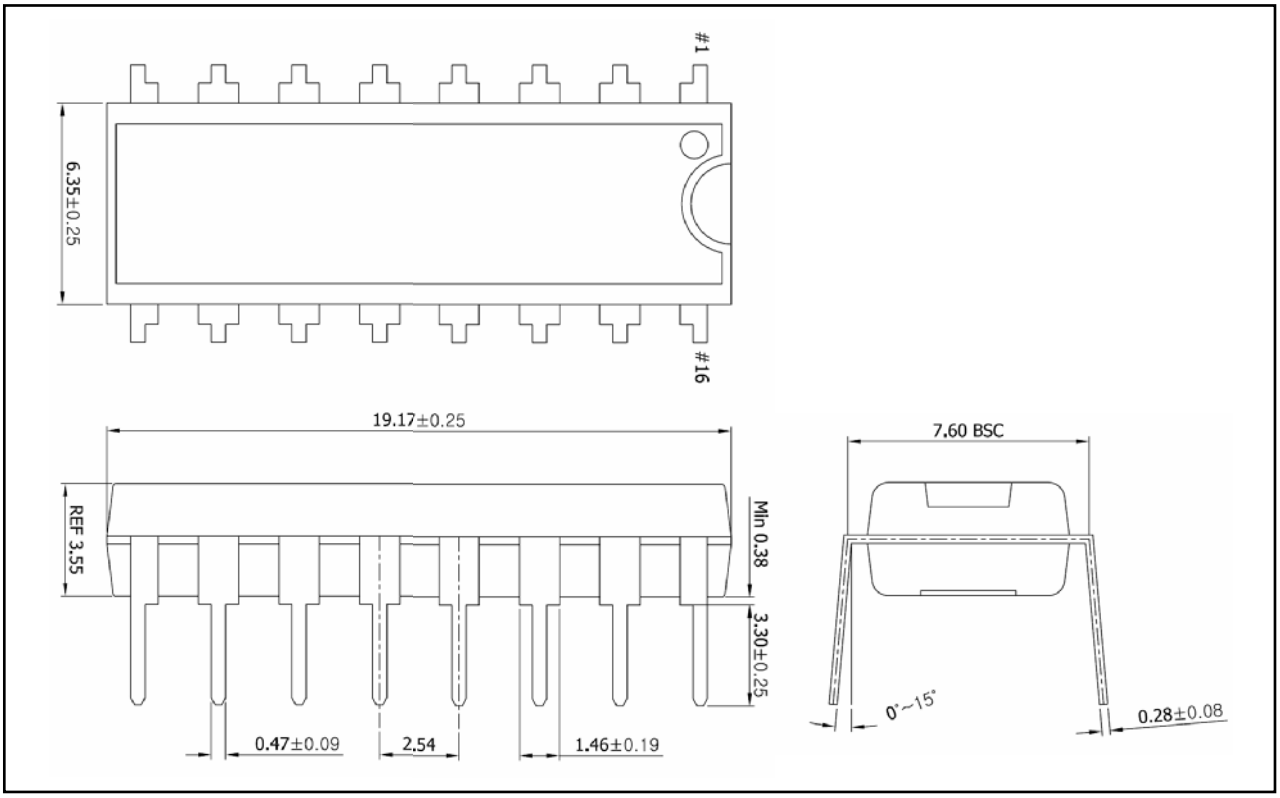


20 PDIP (300Mil) Pin Dimension (dimensions in millimeters)

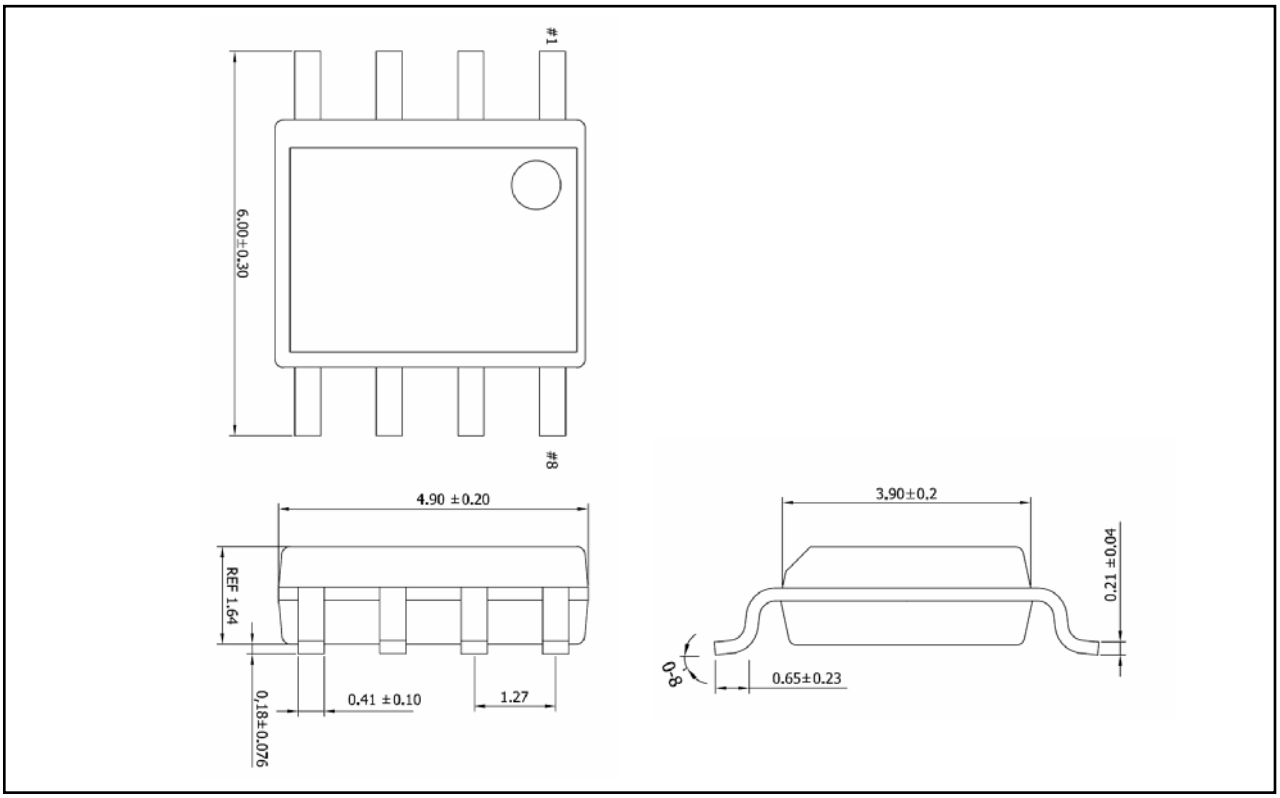
1. OVERVIEW



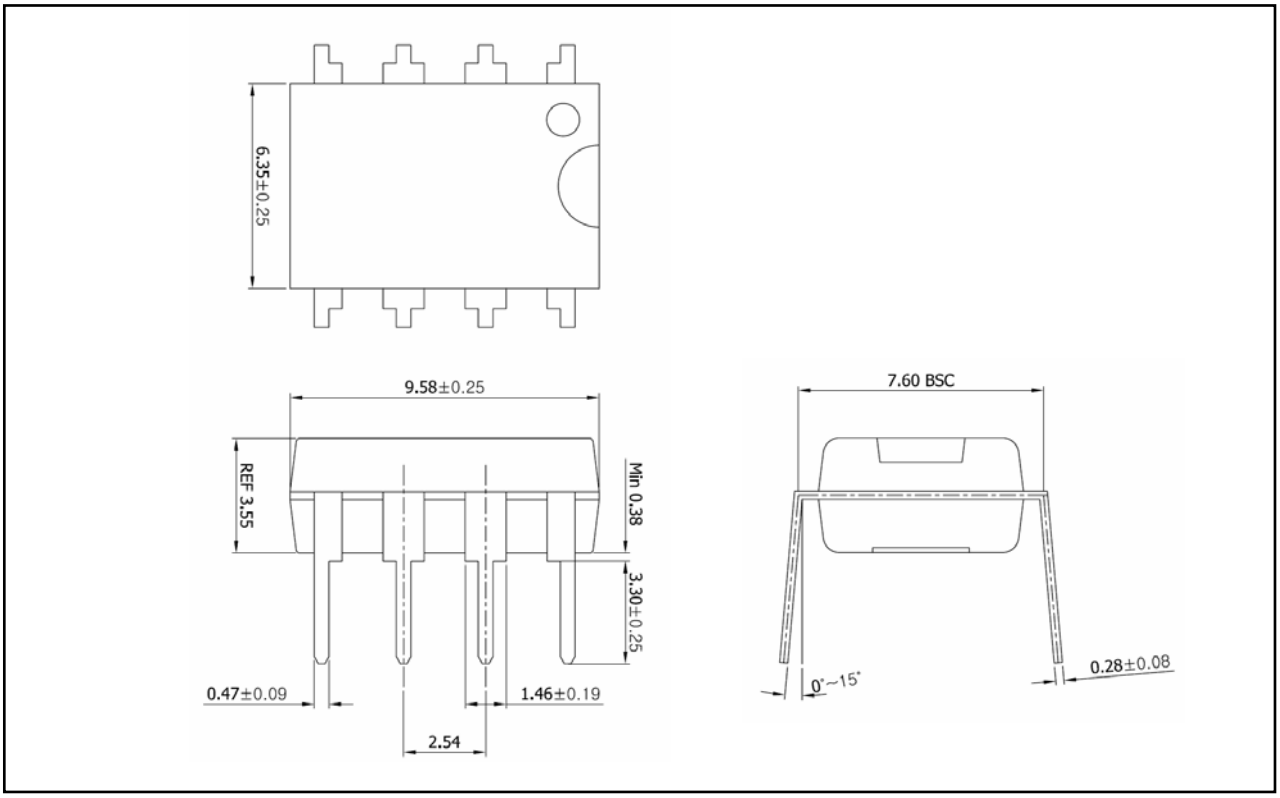
16 SOP (150Mil) Pin Dimension (dimensions in millimeters)



16 DIP (300Mil) Pin Dimension (dimensions in millimeters)

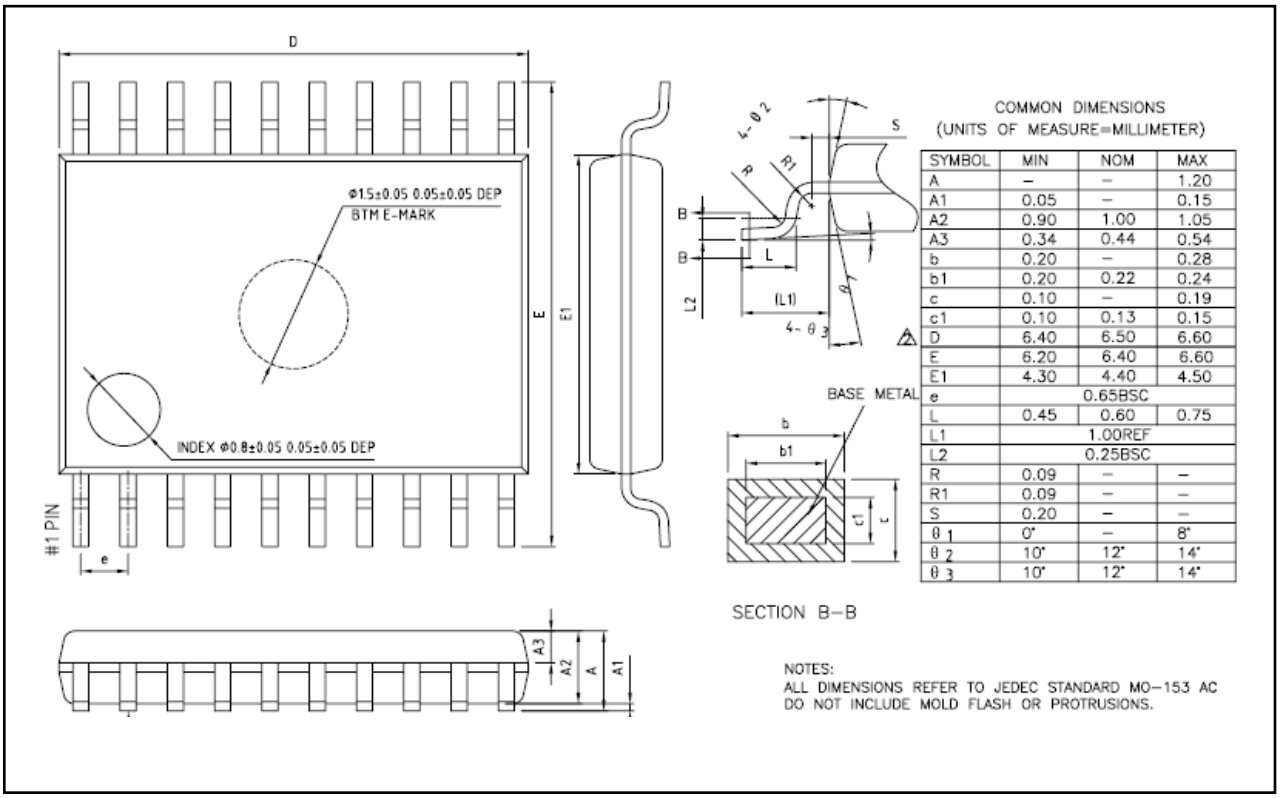


8 SOP (150Mil) Pin Dimension (dimensions in millimeters)



8 DIP (300Mil) Pin Dimension (dimensions in millimeters)

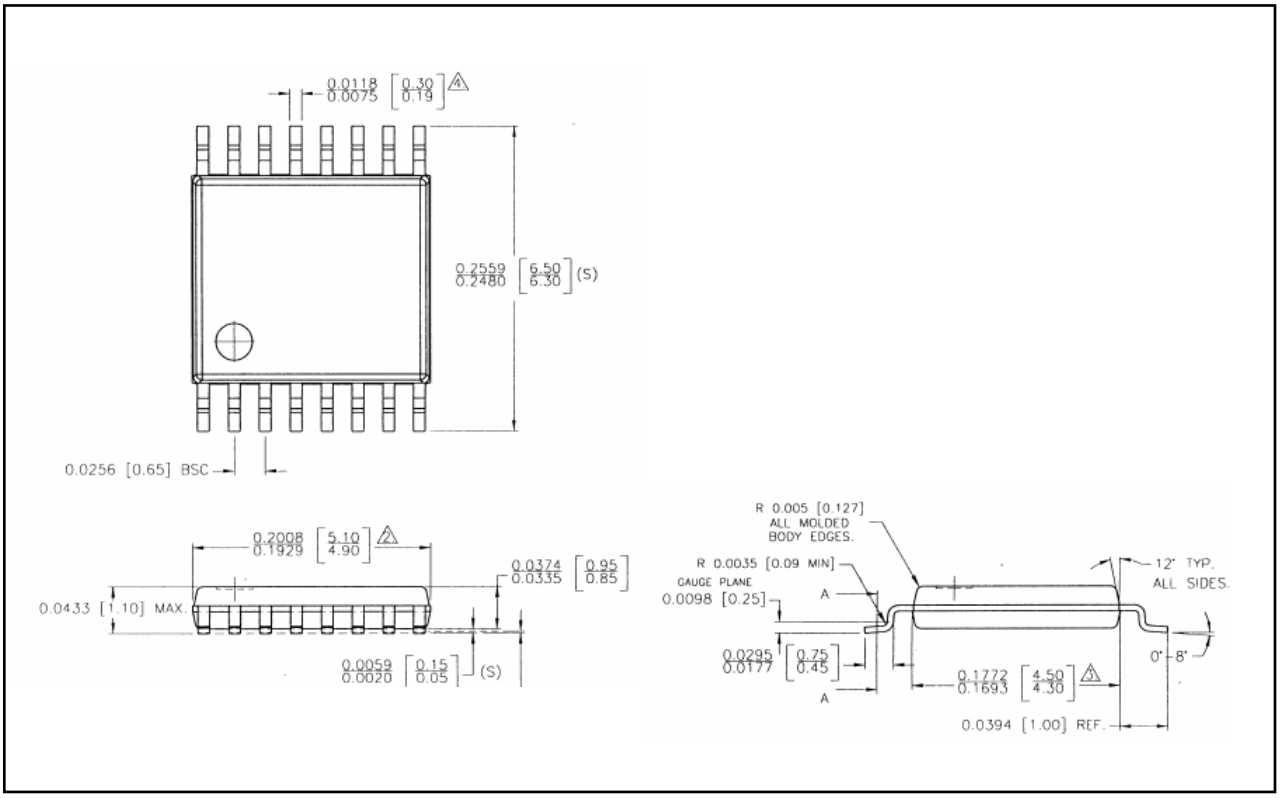
1. OVERVIEW



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	–	0.28
b1	0.20	0.22	0.24
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e		0.65BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ 1	0°	–	8°
θ 2	10°	12°	14°
θ 3	10°	12°	14°

20 TSSOP (4.4 mm) Pin Dimension (dimensions in millimeters)



16 TSSOP (4.4 mm) Pin Dimension (dimensions in inch [millimeters])

1.5. Pin Function

1.5.1. Port Pins

Pin Name	I/O	Function	@RESET	@STOP	Shared Pins
R10	I/O	- 4-bit I/O Port. - CMOS input. - Pull-ups can be connected by user program. - Can be selectable as STOP release input pin individually by user program. (It is released by “L” input at STOP mode) - N-ch open drain output. - Direct driving of LED (N-TR). - Can be programmable as Push-pull output individually. (R11 is not available) - Each pin can be set and reset by R1, PB and PG Data register value.	Input (without Pull-up)	State of before STOP	$\overline{EC1}$/KS0
R11					$\overline{RESET}$/VPP/KS1
R12					OSC2/T1O/AN7 /KS2
R13					OSC1/BUZ/KS3
PB0	I/O		Input (without Pull-up)	State of before STOP	INT1/KS4
PB1					KS5
PB2					T0O/KS6
PB3					KS7
PG0	I/O		Input (without Pull-up)	State of before STOP	PWM/AN0/AVREF /KS8
PG1					INT1/AN1/KS9
PG2					INT2/AN2/KS10
PG3					AN3/KS11
PH0	I/O	- 4-bit I/O Port. - CMOS input. - Pull-ups can be connected by user program. - N-ch open drain output. - Direct driving of LED (N-TR). - Can be programmable as Push-pull output individually. - Each pin can be set and reset by PH Data register value.	Input (without Pull-up)	State of before STOP	AN4
PH1					AN5
PH2					AN6
PH3					-
PC0	Output	- 1-bit Output Port. - N-ch open drain output. - Can be programmable as Push-pull output individually. - Direct Driving of LED(N-TR). - Each pin can be set and reset by PC Data register value.	Hi-Z	State of before STOP	-
ROUT	Output	- High Current output for IR-remote-control-signal (P-TR). - It’s output is forcibly “Low” at STOP mode.	“L” level output	“L” level output	-

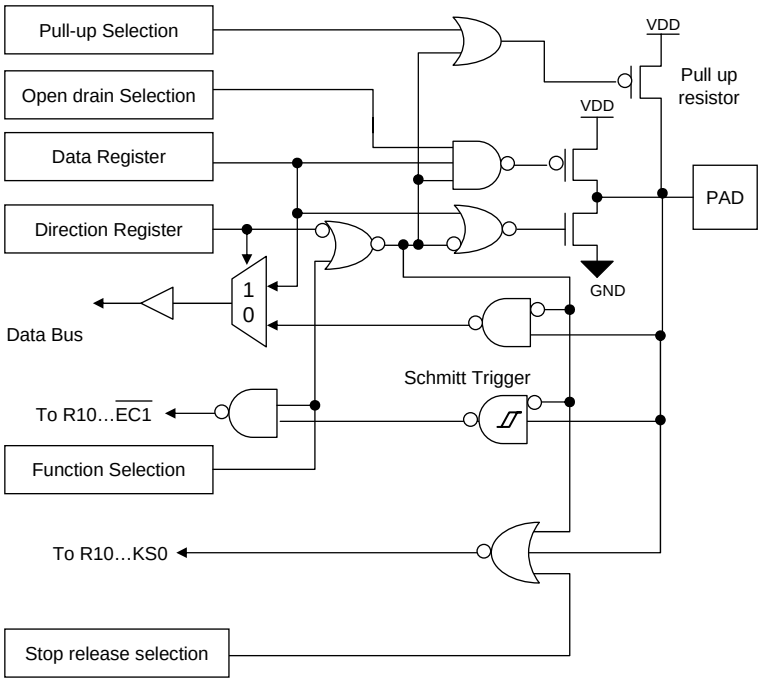
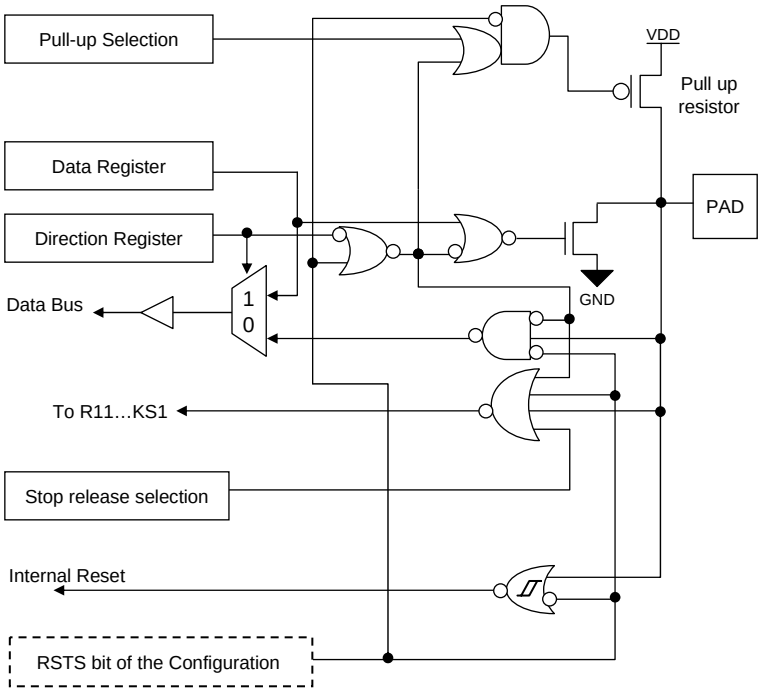
1.5.2. Non-port Pins

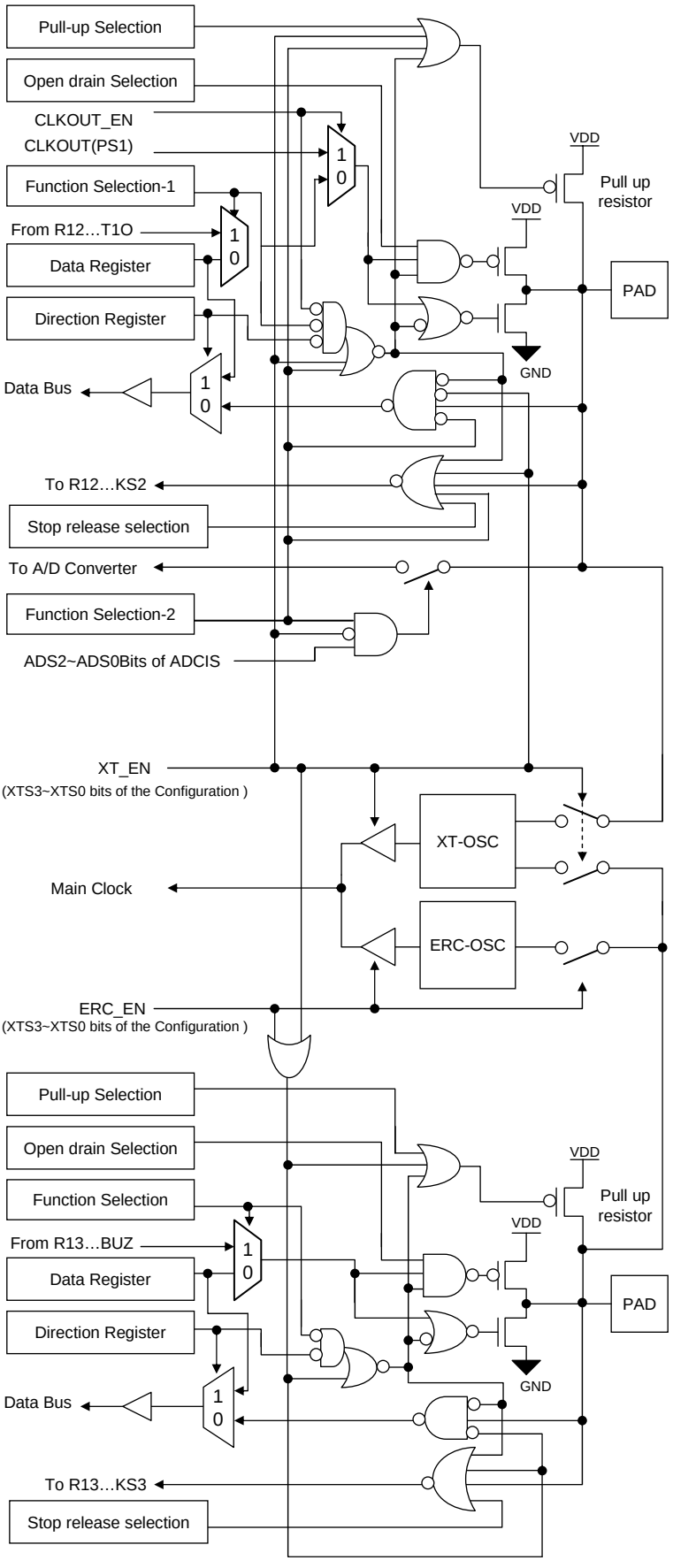
Pin Name	I/O	Function	@RESET	Shared Pins
INT1	Input	- External Interrupt input for which the valid edges (rising edge, falling edge , both rising and falling edge) can be specified.	Input (Pull-up off)	* PB0
				* PG1
INT2				PG2
$\overline{EC1}$	Input	- Timer 1 event counter input.	Input (Pull-up off)	R10
T0O	Output	- Timer 0 output.	Input (Pull-up off)	PB2
T1O	Output	- Timer 1 output.	Input (Pull-up off)	R12/OSC2
BUZ	Output	- 8bit-Buzzer output.	Input (Pull-up off)	R13/OSC1
PWM	Output	- PWM output.	Input (Pull-up off)	PG0
KS0 ~ KS3	Input	- STOP mode release input which can be selected individually by user program. - It is released by “L” input at STOP mode.	Input (Pull-up off)	R10 ~ R13
KS4 ~ KS7				PB0 ~ PB3
KS8 ~ KS11				PG0 ~ PG3
AN0 ~ AN3	Input	- Analog input for A/D Converter. - Each port’s pull-up resistor is disabled at A/D input mode.	Input (Pull-up off)	PG0 ~ PG3
AN4 ~ AN6				PH0 ~ PH2
AN7				R12/OSC2
AVREF	Input	- Analog power for A/D converter.	Input (Pull-up off)	PG0
OSC1	Input	- Oscillator input.	Input (Pull-up off)	R13
OSC2	Output	- Oscillator output.	Input (Pull-up off)	R12
$\overline{RESET}$	Input	- System reset input.	Input (Pull-up off)	R11
VDD	-	- Positive power supply.	-	-
GND	-	- Ground.	-	-

*** INT1/PB0 and INT1/PG1 must be used by only one pin at a application.**

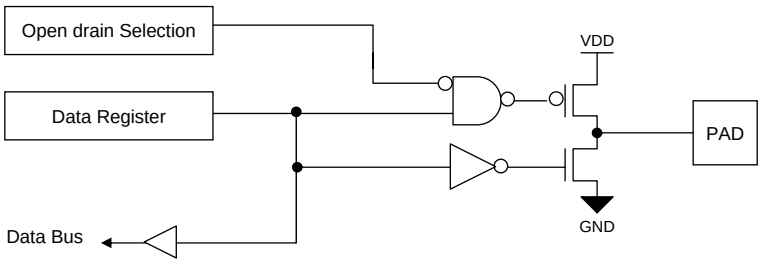
1.6. Port Structure

1.6.1. R1 Ports

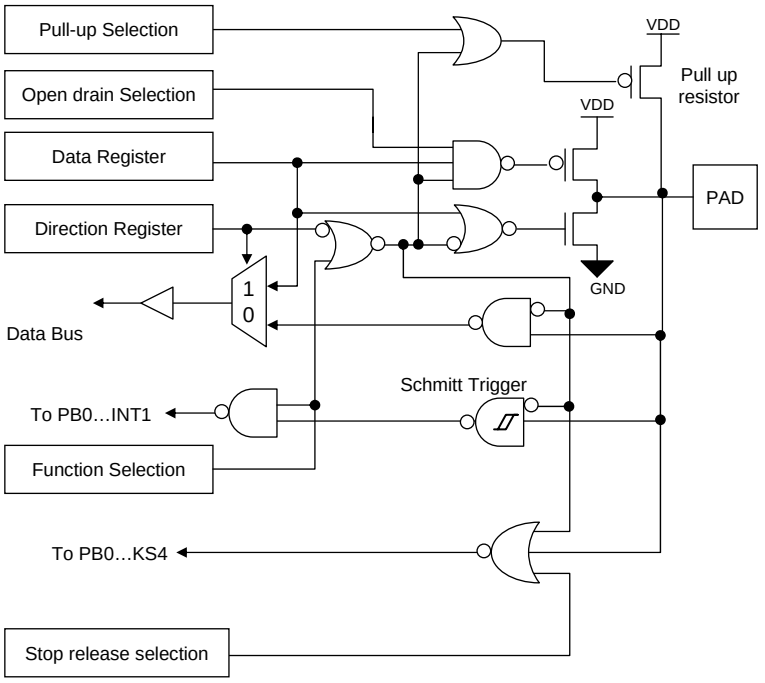
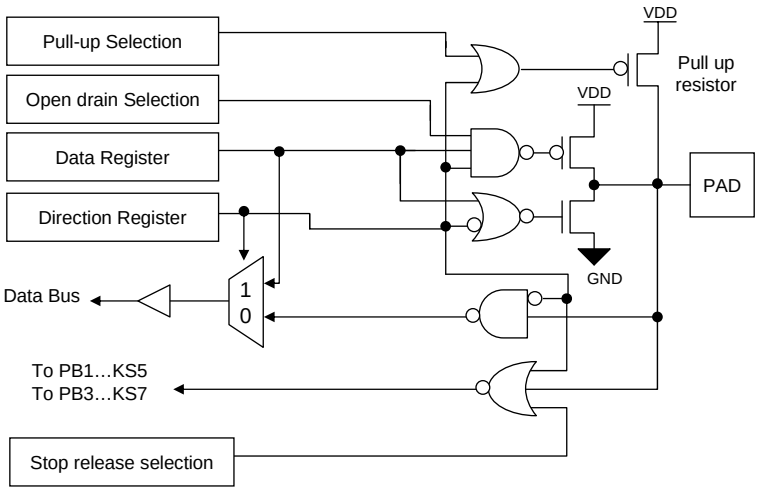
Pin Name	Circuit Type	@ RESET
R10/$\overline{EC1}$		Input (without pull-up)
R11/$\overline{RESET}$ /VPP		Input (without pull-up)

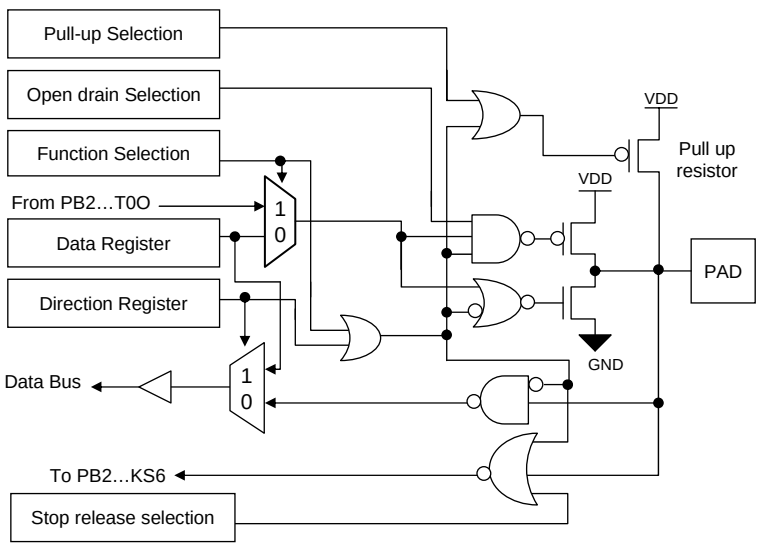
Pin Name	Circuit Type	@ RESET
R12/OSC2 /T1O/AN7		Input (without pull-up)
R13/OSC1 /BUZ		Input (without pull-up)

1.6.2. PC0 Ports

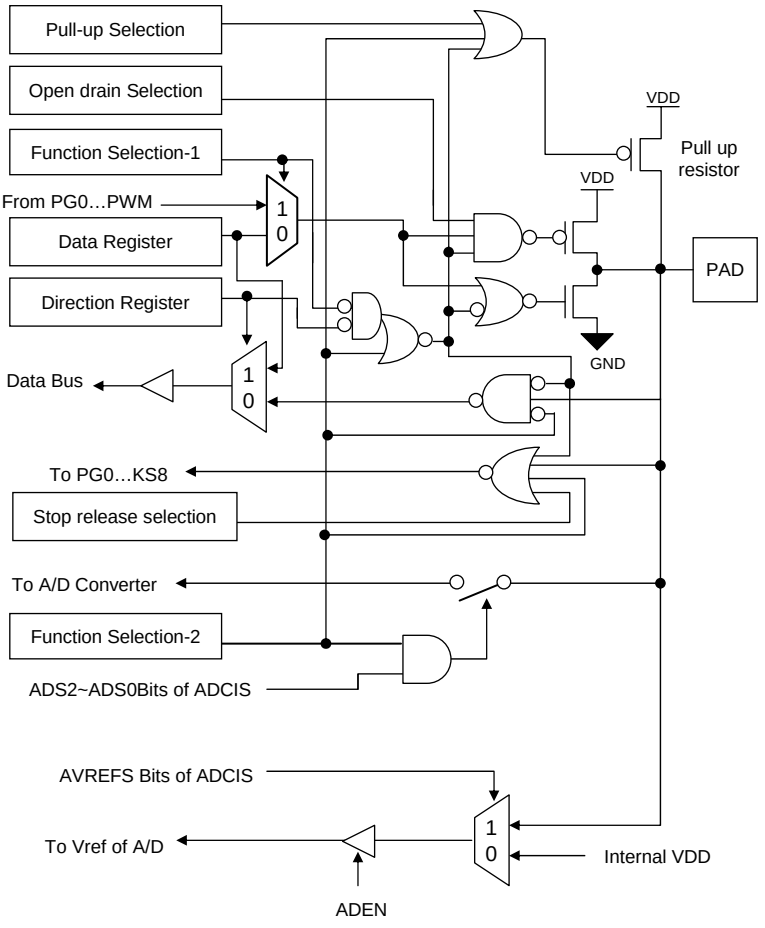
Pin Name	Circuit Type	@ RESET
PC0		Hi-Z

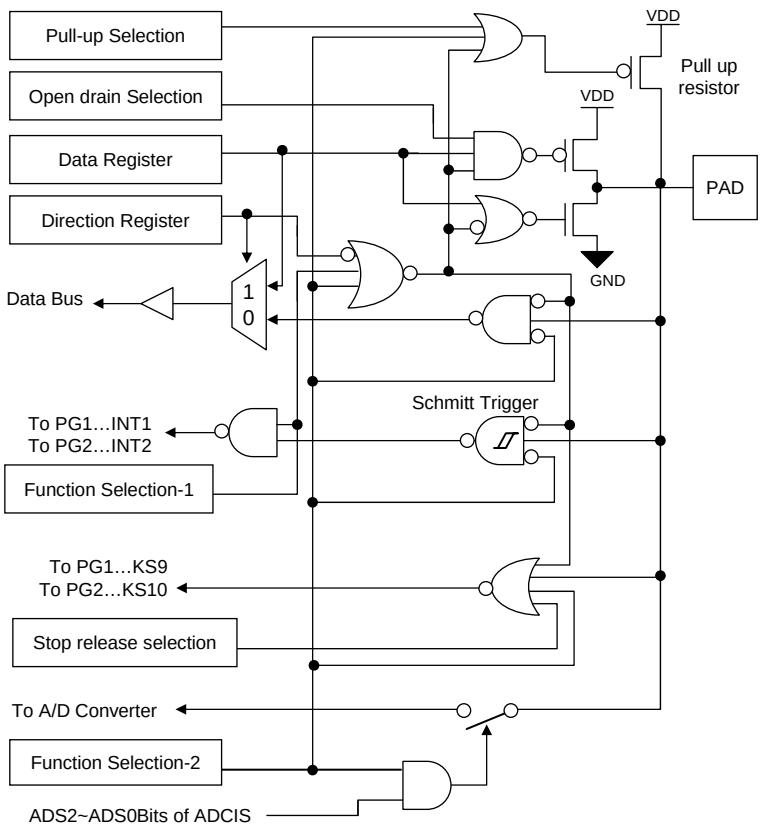
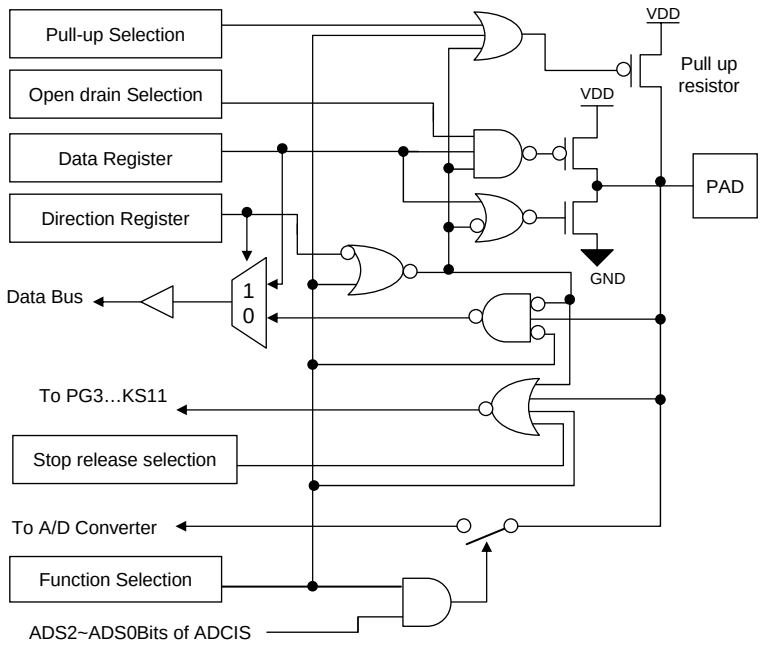
1.6.3. PB Ports

Pin Name	Circuit Type	@ RESET
PB0/INT1		Input (without pull-up)
PB1 PB3		Input (without pull-up)

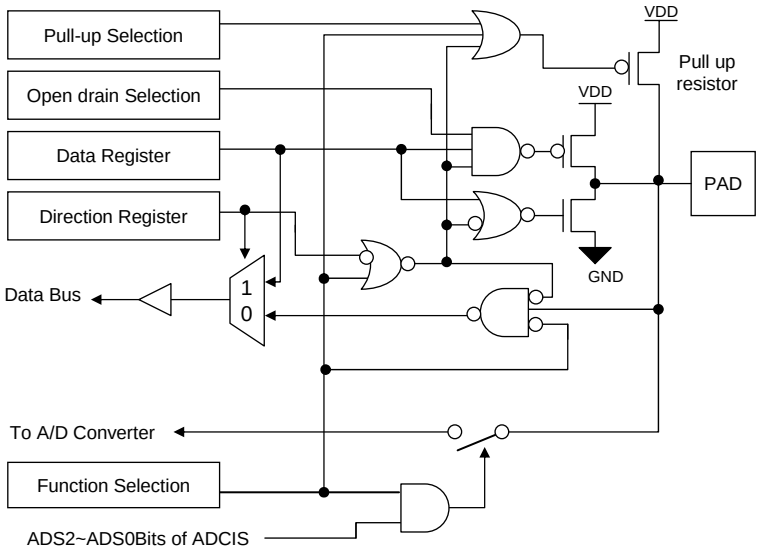
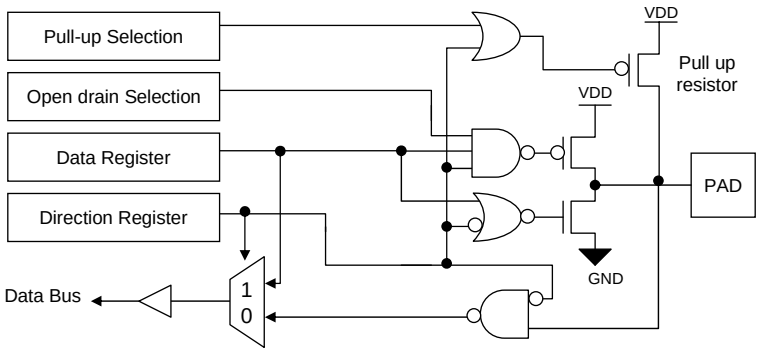
Pin Name	Circuit Type	@ RESET
PB2/T0O		Input (without pull-up)

1.6.4. PG Ports

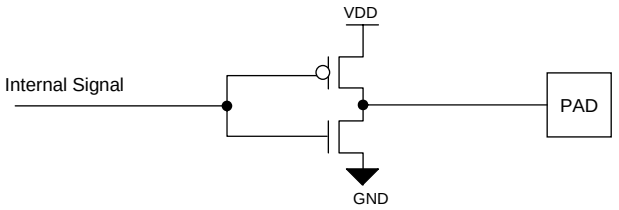
Pin Name	Circuit Type	@ RESET
PG0/PWM /AN0/AVREF		Input (without pull-up)

Pin Name	Circuit Type	@ RESET
PG1/INT1/AN1 PG2/INT2/AN2		Input (without pull-up)
PG3/AN3		Input (without pull-up)

1.6.5. PH Ports

Pin Name	Circuit Type	@ RESET
PH0/AN4 PH1/AN5 PH2/AN6		Input (without pull-up)
PH3		Input (without pull-up)

1.6.6. ROUT Port

Pin Name	Circuit Type	@ RESET
ROUT		Low Level

1. OVERVIEW

1.7. Electrical Characteristics

1.7.1. Absolute Maximum Ratings (Ta = 25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.3 ~ +6.0	V
Input Voltage	V_I	-0.3 ~ V_{DD}+0.3	V
Output Voltage	V_O	-0.3 ~ V_{DD}+0.3	
Operating Temperature	T_{OPR}	-40 ~ 85	℃
Storage Temperature	T_{STG}	-65 ~ 150	℃
Power Dissipation	P_D	700	mW

1.7.2. Recommended Operating Ranges

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}	f_{XIN} = 4MHz	2.0	-	5.5	V
		f_{XIN} = 8MHz	2.5	-	5.5	V
Oscillation Frequency	f_{XIN}	Crystal/Ceramic Resonator External Clock External RC Oscillator	1	-	8	MHz
		Internal RC Oscillator (VDD=5V, Tolerance=20%)	-	6.0	-	MHz
			-	3.0	-	
			-	1.5	-	
			-	0.75	-	
Operating Temperature	T_{OPR}		-40	-	85	℃

1.7.3. DC Characteristics (VDD = 5.5V~2.5V/2.0V, VSS = 0V, Ta = -40℃ ~ 85℃)

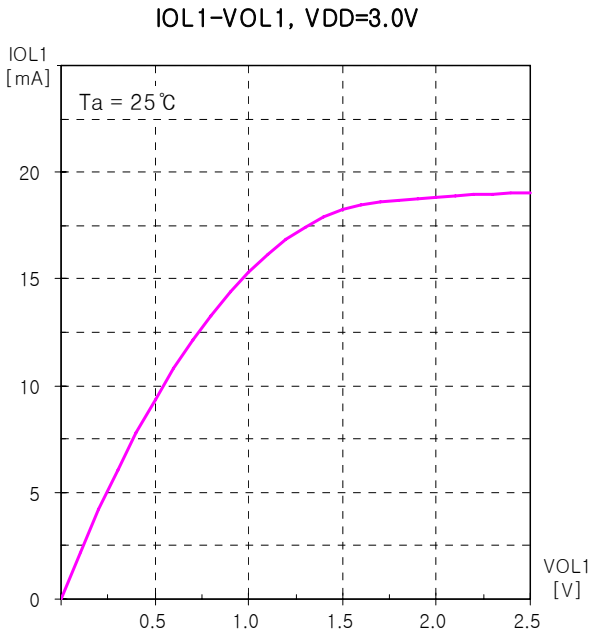
Parameter	Symbol	Condition		Specification			Unit
				min	typ	max	
high level input voltage	VIH1	INT1, INT2, $\overline{EC1}$, $\overline{RESET}$		0.8VDD		VDD	V
	VIH2	R1, PB, PG, PH		0.7VDD		VDD	V
low level input voltage	VIL1	INT1, INT2, $\overline{EC1}$, $\overline{RESET}$		0		0.2VDD	V
	VIL2	R1, PB, PG, PH		0		0.3VDD	V
high level input leakage current	IIH	All Input Pin	VIH=VDD			1	uA
low level input leakage current	IIL	All Input Pin (without Pull-up)	VIL=0V			-1	uA
high level output voltage	VOH1	R1,PB,PC0,PG,PH (Except R11)	IOH= -10mA (VDD=5.0V)	VDD-1.0			V
	VOH2	OSC2	IOH= -200uA	VDD-1.0			V
low level output voltage	VOL1	R1,PB,PC0,PG,PH	IOL= 15mA (VDD=5.0V)			1.0	V
	VOL2	OSC2	IOL= 200uA			1.0	V
high level output leakage current	IOHL	R1,PB,PC0,PG,PH	VOH=VDD			1	uA
low level output leakage current	IOLL	R1,PB,PC0,PG,PH	VOL=0V			-1	uA
high level output Current 1	IOH1	ROUT	VDD=3V VOH= 2V	-30	-12	-5	mA
low level output Current 1	IOL1	ROUT	VDD=3V VOL= 1V	0.5		3	mA
input pull-up current	IPU	All Input Port with Pull-up	VDD= 3V	-15	-30	-60	uA
power supply current	IDD	operating current	fxin=8MHz, VDD= 5.5V		8	20	mA
			fxin=4MHz, VDD= 5.5V		4	10	mA
			fxin=4MHz, VDD= 2.0V		2.4	6	mA
	ISLEEP	sleep mode current	fxin=4MHz, VDD= 5.5V		2	6	mA
			fxin=4MHz, VDD= 2.0V		1	3	mA
	ISTOP	stop mode current	oscillator stop, VDD= 5.5V		5	15	uA
			oscillator stop, VDD= 2.0V		2	8	uA
internal RC WDT Period	T_{RCWDT}	VDD=5.0V (if RCWDTCK=0)		32	64	128	uS
external RC Oscillator	F_{ERC}	VDD=4.75V to 5.25V R = 18kΩ		-	4	-	MHz
internal RC Oscillator	F_{IRC}	VDD=5.0V (Tolerance 20%)		-	3	-	MHz
RAM retention supply voltage	VRET			0.7	-	-	V

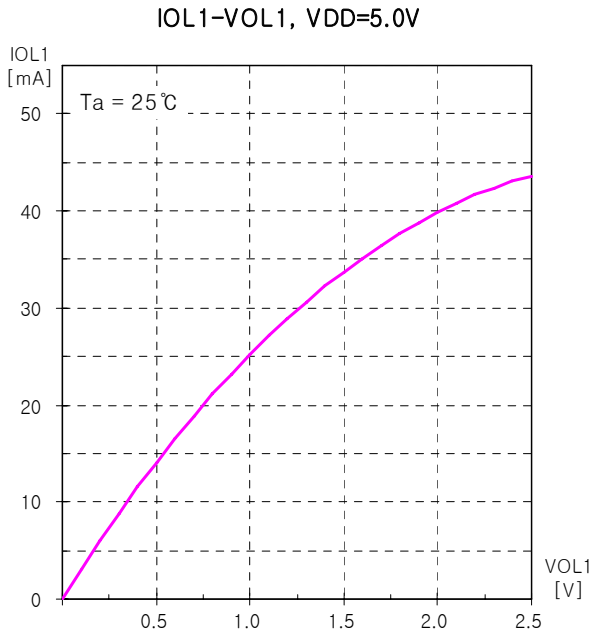
※ Typical Characteristics

This graphs provided in this section are for design guidance only and are not tested or guaranteed.

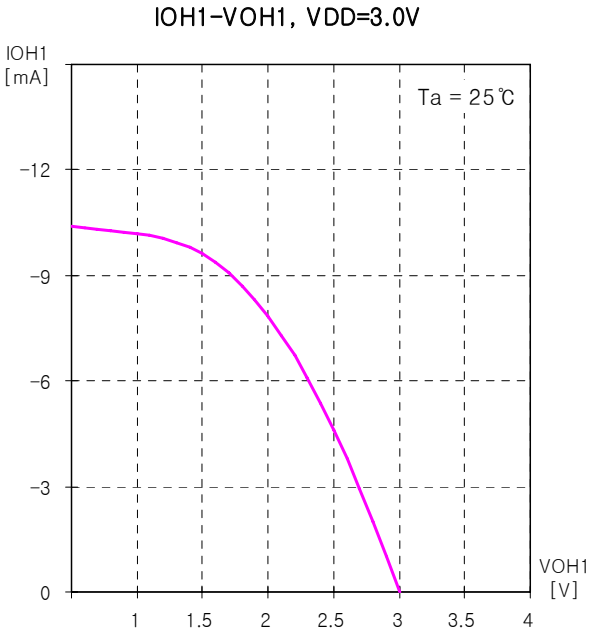
The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean – 3σ) respectively where σ is standard deviation.

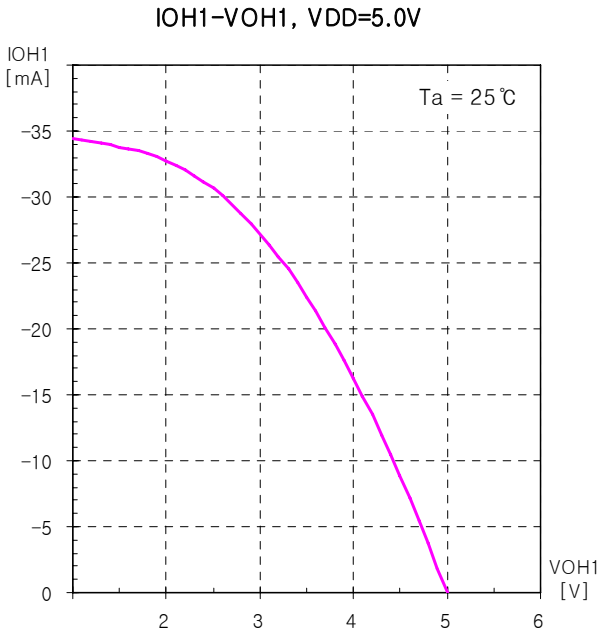
▶ IOL1 vs. VOL1 (at T=25℃)



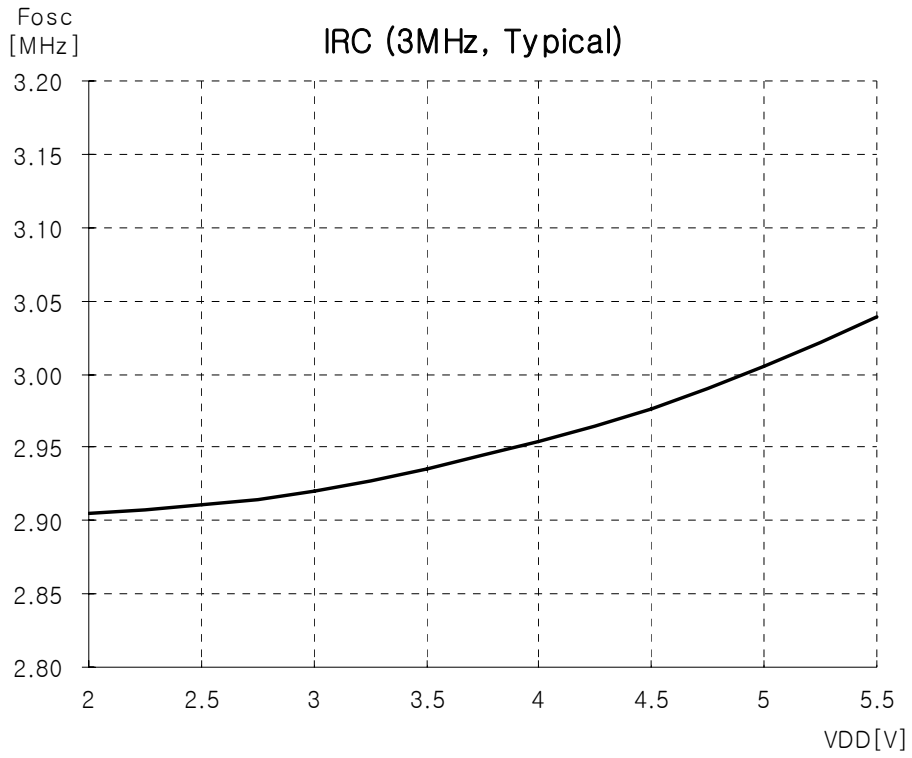


▶ IOH1 vs. VOH1 (at T=25℃)





▶ **Internal RC Oscillator (3MHz selected, at T=25℃)**

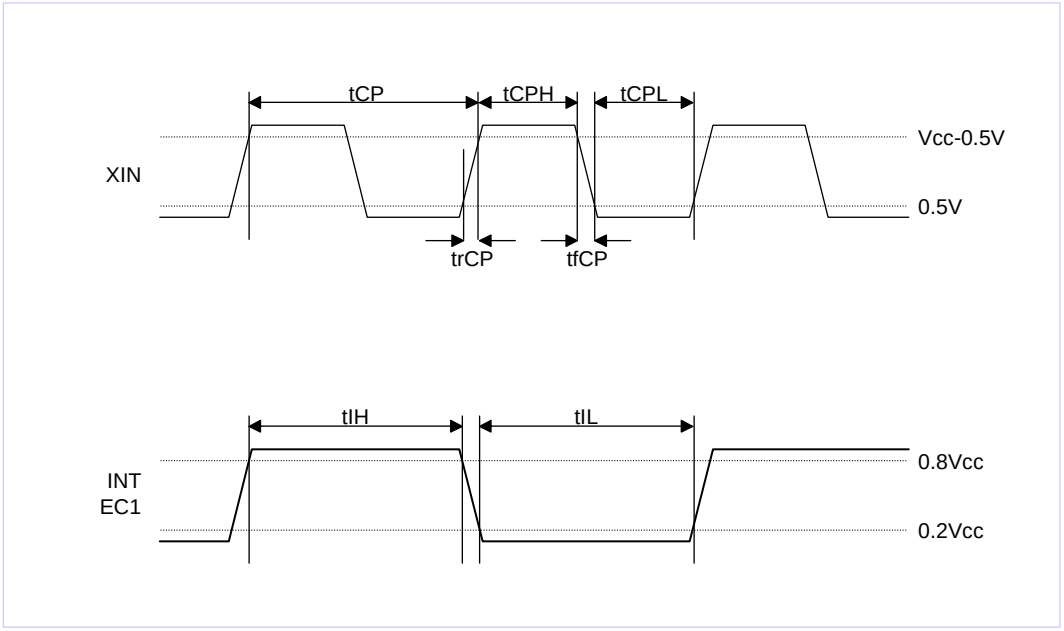


1.7.4. 12Bit A/D Conversion Characteristics (VDD = 5.5V~2.7V/2.4V@ f_{XIN} = 1~8MHz, Ta = 25℃)

Parameter	Symbol	Condition	Specification			Unit
			MIN	TYP	MAX	
Resolution	RADC			12		Bits
Analog Input Voltage Range	VAIN	AVREFS = 0	VSS	-	VDD	V
		AVREFS = 1	VSS	-	AVREF	V
Analog Input Power Supply Voltage Range	AVREF	VDD = 5.0V	2.4	-	VDD	V
		VDD = 3.0V	2.4	-	VDD	V
Overall Accuracy	EACC	VDD=4.096V, f_{XIN} = 4MHz	-	-	±4.0	LSB
Non-Linearity Error	ENE		-	-	±4.0	LSB
Differential Non-Linearity Error	EDE		-	±1.0	±2.0	LSB
Zero Offset Error	EOFF		-	±1.0	±3.0	LSB
Full Scale Error	EFE		-	±1.0	±3.0	LSB
Conversion Time	TCONV	VDD = 5.5V ~ 2.7V	29	-	-	μs
		VDD = 5.5V ~ 2.4V	58	-	-	μs
AVREF Input Current	IREF	AVREFS = 1	-	0.8	2.0	mA

1.7.5. AC Characteristics (VDD = 2.0 ~ 5.5 V, Vss = 0V, Ta = -40℃ ~ 85℃)

No.	Parameter	Symbol	Pin	Specification			Unit
				min.	typ.	max.	
1	External clock input cycle time	t_{cp}	Xin	125	250	1000	ns
2	System clock cycle time	t_{sys}		500	1000	4000	ns
3	interrupt pulse width High	t_{IH}	INT	2			t_{sys}
4	Interrupt pulse width Low	t_{IL}	INT	2			t_{sys}



Clock, Interrupt Input Timing

2. FUNCTION DESCRIPTION

2.1. Program Memory

The ADAM42X11XX can address maximum 4Kbytes (2K words × 16bits) for program memory. Program counter PC (A0~A10) is used to address the whole area of program memory having an instruction (16bits) to be next executed.

The program memory consists of 2K words.

The program memory is composed as shown below.

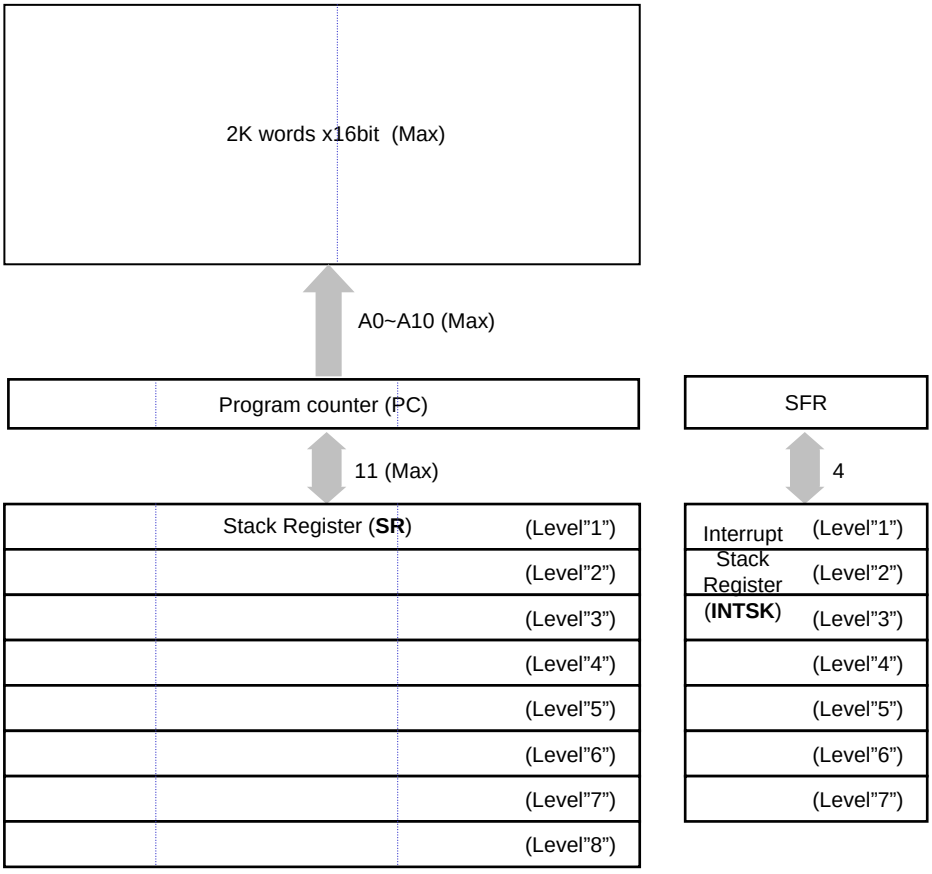


Fig 2-1 Configuration of Program Memory

2.2. Address Register

The following registers are used to address the ROM.

- **Program counter (PC) :**
  Available for addressing word on each page.
- **Stack register (SR) :**
  Stores returned-word address in the subroutine call mode.

2.2.1 Program counter :

This 11-bit binary counter increments for fetching a word to be addressed in the currently addressed page having an instruction to be next executed.

For easier programming, at turning on the power, the program counter is reset to the zero location(0000H). Then the program counter specifies the next address.

When BR, CAL or RET instructions are decoded, the switches on each step are turned off not to update the address. Then, for BR or CAL, address data are taken in from the instruction operands (A0 to A10), or for RET, and address including page address is fetched from stack register No. 1.

2.2.2. Stack register (SR)

The address stack register (ADS) stores a return address when the subroutine call instruction is executed or interrupt is acknowledged.

If subroutine or interrupts are nested to more than 8 levels, internal reset is occurred.

The interrupt stack register(INTSK) saves the contents of Status Flag Register (SFR) when an interrupt is acknowledged.

The saved contents are restored when an interrupt return(RETI) instruction is executed.

INTSK saves data each time an interrupt is acknowledged.

The programmer must keep in mind that the level of INTSK is only 7. So, if more over 7 levels of interrupt occur, the first stored data is lost. There is different result between Stack overflow and interrupt stack overflow.

When clearing SP (Stack Pointer) with using “SPC” instruction, interrupt processing must be inhibited before “SPC”.

2.3. Data Memory (RAM)

256 nibbles (256 words × 4bits) is incorporated for storing data.

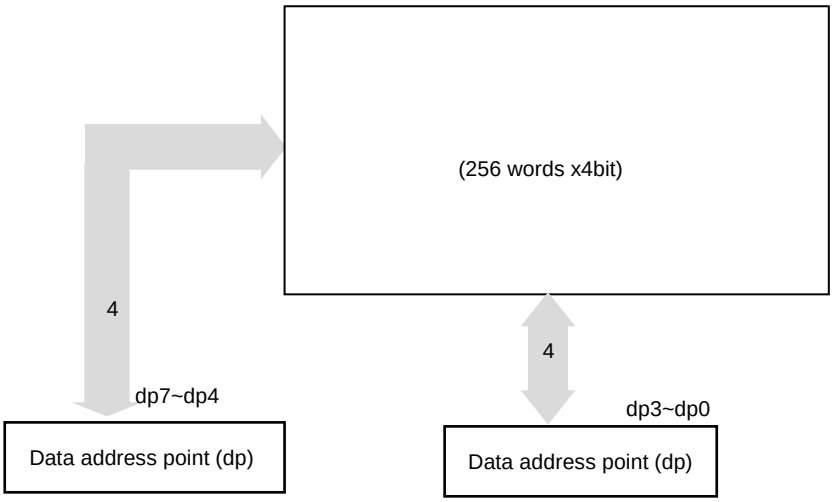
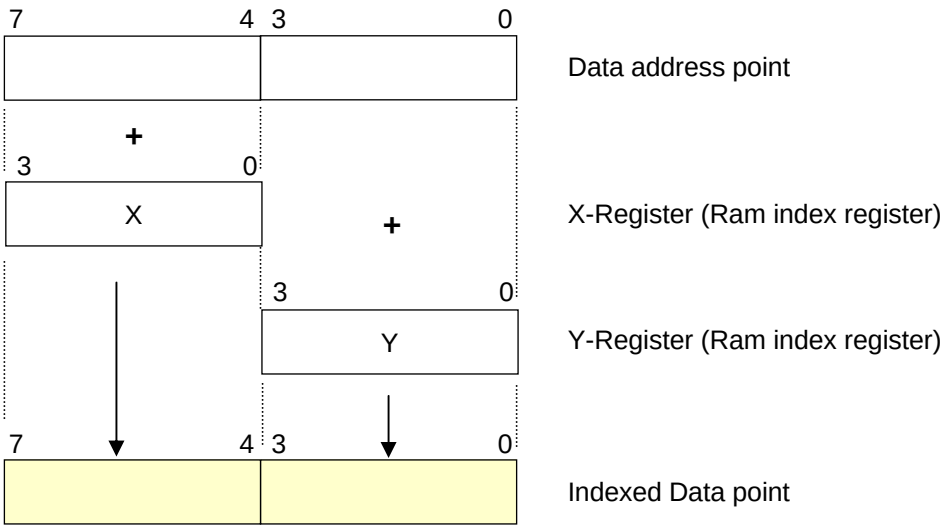


Fig 2-2 Data Memory

2.3.1. Data memory(RAM) addressing method

The whole data memory area is directly addressed by 8-bit ram data address point (dp).

Index data memory addressing is available using X-register and Y-register.
In this case, X-register is added upper 4bit of data point and Y-register is added lower 4bit of data point.



2.3.2. Data memory(RAM) data addressing example Program

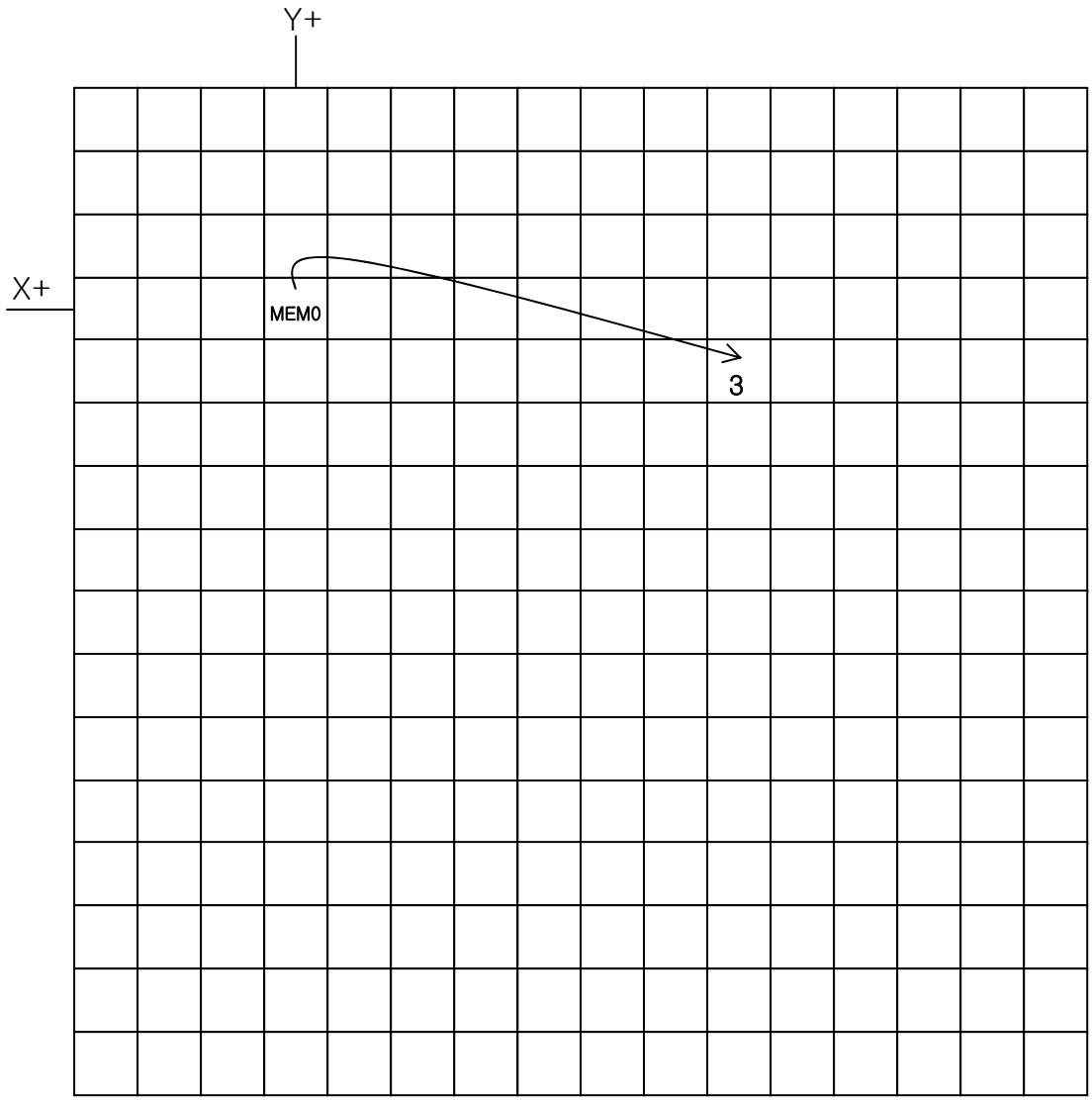


Fig 2-3 Data Memory Map

Program Example)

```
LDM     MEM0,#3h
LYI     #7
LXI     #1
LDA     MEM0
EIX
LDM     MEM0,A
DIX
```

Result after executing
; MEM0 = 3h
  MEM0 + X + Y = 3h

2.4. General Function Registers

2.4.1. X-register (X)

X-register is consist of 4bit, X-register is used for data memory indexing register.

2.4.2. Y-register (Y)

Y-register is consist of 4 bits. It can used for a general-purpose register.
Y-register also used for data memory indexing register.

2.4.3. Accumulator (ACC)

The 4-bit register for holding data and calculation results.

2.4.4. Peripheral Address Register(PAR)

The 6-bit address register for addressing peripheral registers including address buff register(ABR) , data buff register (DBR).

2.4.5. Address Buff Register (ABR)

The 16-bit register for address buffer.
The address of Address Buffer Register (ABR) is 38h ~ 3Bh on the peripheral register.
It is composed by 4 registers (ABR0, ABR1, ABR2, ABR3) and each register is 4 bit.

2.5. Buffer Registers (DBR, ABR)

Buffer registers are two types of 16 bit registers composed of 4-ninbble registers.
One is Data Buffer Register (DBR) and the other is Address Buffer Register (ABR).
The address of Data Buffer Register (DBR) is 3Ch ~ 3Fh and the address of Address Buffer Register (ABR) is 38h ~ 3Bh on the peripheral register.
These buffers are mainly used for Data transferring between ROM and buffer or peripheral registers and buffer. They are also used for general purpose register for data manipulation, data storage and intermediate buffer.

2.5.1. Function of Address Buff Register (ABR)

The most important function of ABR is ROM address pointer.
ABR must be used for reading data from ROM. The data pointed by ABR is read to DBR.
ABR value is varied through peripheral control instruction and “INC ABR”.

2.5.2. Function of Data Buff Register(DBR)

The most important function of DBR is intermediate (window) buffer for transferring data between peripheral registers and reading data from ROM.
When the data of ROM is read by “LDW @ABR”, one word of ROM is fetched to DBR.
The MSB of ROM data is written to DBR3 and LSB to DBR0.
If the data of pointed ROM is 1234h, each DBR has the data as DBR0 = 4h, DBR1 = 3h, DBR2 = 2h and DBR3 = 1h.
DBR is also used for reading some peripheral register data by 8bit unit or 16bit unit.
The peripheral registers are T0CR and T1CR.

Note) HEX. File maps the data as big endian type. Be careful to read the ROM data. When the programmer assigns the data like below, the ROM data is mapped as below.
DB 12h, 34h → ROM data = 1234h

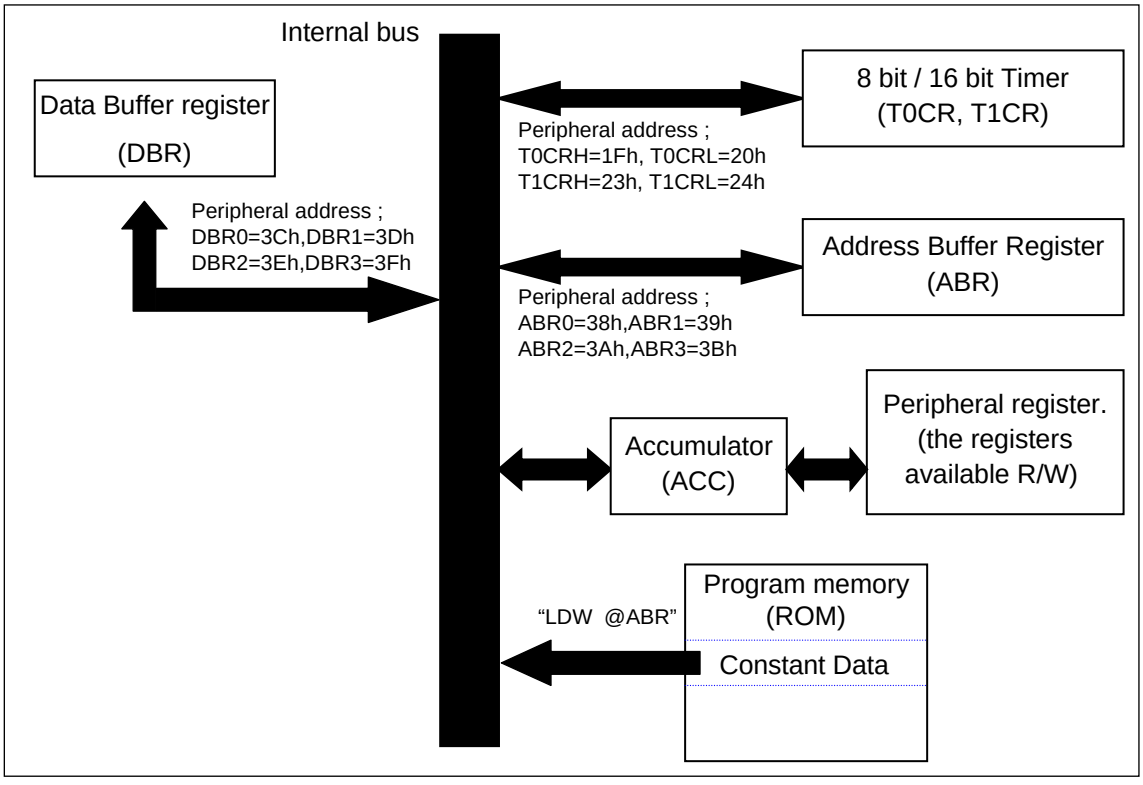


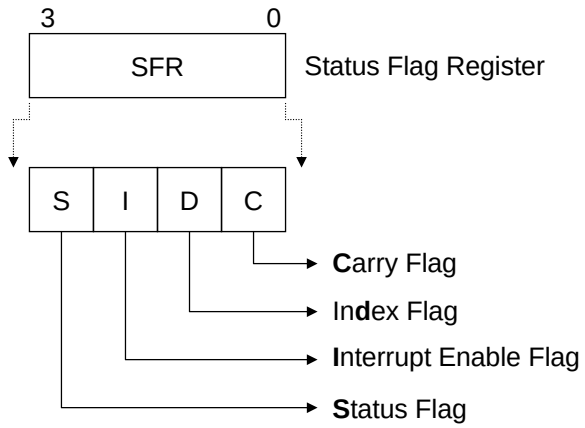
Fig 2-4 The internal Data flow among DBR, ABR, registers and ROM

2.6. Status Flag Registers (SFR)

Status Flag Register (SFR) consists of 4-bit register.

Each of the flags show the post state of operation and the flags determining the CPU operation, initialized as 0h in reset state.

When an interrupt is occurred, the value of SFR keep the value of pre-interrupt except for I flag. So, be careful to initialize the SFR status for getting reliable result in Interrupt sub-routine.



2.6.1 Carry flag (C)

- Carry flag bit is set when there is carry or borrow After executing ADDC / SUBC / ARRC/ARLC instructions.
- Set by SETC and clear by CLRC.
- Load from the assigned bit of Peripheral Registers by LDC
- Transfer to the assigned bit of Peripheral Registers by STC

2.6.2 Index flag (D)

- The control bit of ram data address point indexed or not.
- X-register and Y-register is used for index addressing.
- Set and cleared by EIX, DIX.

2.6.3 Interrupt enable flag (I)

- Master enable flag of interrupt.
- Set and cleared by EI, DI
- This Flag immediately becomes “0” when an interrupt is served.

2.6.4 Status flag (S)

- According to the condition after executing an instruction , set or clear.
- Can not be set or clear by any instruction.
- This Flag decides whether operation of BR and CALL would be done or not.

2. FUNCTION DESCRIPTION

2.7. Peripheral Registers

Peripheral Address	Function Registers	Read Write	Symbol	RESET Value			
				3	2	1	0
00 h	*Reserved*						
01 h	PORT R1 STOP RELEASE SELECTION REG.	W	R1ST	F			
02 h	PORT R1 PULL UP RESISTOR SELECTION REG.	W	R1PC	F			
03 h	PORT R1 OPEN DRAIN SELECTION REG.	W	R1OD	0			
04 h	PORT R1 DATA REG.	R/W	* R1	F			
05 h	PORT R1 DIRECTION REG.	W	R1DD	0			
06 h	TIMER OUTPUT PORT SELECTION REG.	W	TOPSR	0	0	0	0
07 h	*Reserved*						
08 h	PORT PB STOP RELEASE SELECTION REG.	W	PBST	F			
09 h	PORT PB PULL UP RESISTOR SELECTION REG.	W	PBPC	F			
0A h	PORT PB OPEN DRAIN SELECTION REG.	W	PBOD	0			
0B h	PORT PB DATA REG.	R/W	* PB	F			
0C h	EXT. INTERRUPT INPUT PORT SELECTION REG.	W	EIPSR	0	0	0	0
0D h	PORT PB DIRECTION REG.	W	PBDD	0			
0E h	PORT PC OPEN DRAIN SELECTION REG.	W	PCOD	-	-	-	0
0F h	PORT PC DATA REG.	R/W	PC	1	1	1	1
10 h	*Reserved*						
11 h	*Reserved*						
12 h	*Reserved*						
13 h	*Reserved*						
14 h	*Reserved*						
15 h	INT. REQUEST FLAG REG. 2	R/W	IRQR2	-	0	0	0
16 h	INT. ENABLE REG. 2	R/W	IENR2	-	0	0	0
17 h	EXTERNAL INT. EDGE SELECTION REG.	W	IEDS	0	0	0	0
18 h	INT. ENABLE REG.	R/W	IENR	0	0	0	0
19 h	INT. REQUEST FLAG REG.	R/W	IRQR	0	0	0	0
1A h	TIMER0 MODE REG.	R/W	T0MR	0	0	0	0
1B h	VTG. DETECTION INDICATOR ENABLE REG.	W	VDIER	0	0	0	0
	VTG. DETECTION INDICATOR DATA REG.	R	VDIR	-	0	0	0
1C h	TIMER1 MODE REG.	R/W	T1MR	0	0	0	0
1D h	ROUT CONTROL REG.	R/W	RCR	0	0	0	0
1E h	CARRY MODE REG.	R/W	CGMR	0	0	0	0
1F h	TIMER 0 DATA 0 HIGH REG.	W	T0D0H	undefined			
	TIMER0 COUNT REG. HIGH	R	T0CRH	undefined			
	TIMER 0 CAPTURE HIGH REG.	R	T0CPH	undefined			

Note1> '-' is reserved bit , it must be read to "0".
Note2> 'X' is undefined bit
Note3> * Using the bit access Instruction, bit is read-modified operation (SETR1/CLRR1/STC Instructions)

2. FUNCTION DESCRIPTION

Peripheral Address	Function Registers	Read Write	Symbol	RESET Value 3	2	1	0
20 h	TIMER 0 DATA 0 LOW REG.	W	T0D0L	undefined			
	TIMER 0 COUNT REG. LOW	R	T0CRL	undefined			
	TIMER 0 CAPTURE LOW REG.	R	T0CPL	undefined			
21 h	TIMER 0 DATA 1 HIGH REG.	W	T0D1H	undefined			
22 h	TIMER 0 DATA 1 LOW REG.	W	T0D1L	undefined			
23 h	TIMER 1 HIGH DATA REG.	W	T1HD	undefined			
	TIMER 1 COUNT REG. HIGH	R	T1CRH	undefined			
	TIMER 1 CAPTURE HIGH REG.	R	T1CPH	undefined			
24 h	TIMER 1 LOW DATA REG.	W	T1LD	undefined			
	TIMER 1 COUNT REG. LOW	R	T1CRL	undefined			
	TIMER 1 CAPTURE LOW REG.	R	T1CPL	undefined			
25 h	CARRY GENERATOR HIGH-MSB DATA REG.	W	CGHMD	undefined			
26 h	CARRY GENERATOR HIGH-LSB DATA REG.	W	CGHLD	undefined			
27 h	CARRY GENERATOR LOW-MSB DATA REG.	W	CGLMD	undefined			
28 h	CARRY GENERATOR LOW-LSB DATA REG.	W	CGLLD	undefined			
29 h	TIMER 01 MODE REG.	R/W	T01MR	0	0	0	0
2A h	PORT PG STOP RELEASE SELECTION REG.	W	PGST	F			
2B h	PORT PG OPEN DRAIN SELECTION REG.	W	PGOD	0			
2C h	PORT PG DATA REG.	R/W	* PG	F			
2D h	ADC INPUT PORT SELECTION REG. 1	W	APSR1	0	0	0	0
2E h	PORT PG DIRECTION REG.	W	PGDD	0			
2F h	PORT PH OPEN DRAIN SELECTION REG.	W	PHOD	0			
30 h	PORT PH DATA REG.	R/W	* PH	F			
31 h	ADC INPUT PORT SELECTION REG. 2	W	APSR2	0	0	0	0
32 h	PORT PH DIRECTION REG.	W	PHDD	0			
33 h	A/D CONVERTER INPUT SELECTION REG.	W	ADCIS	0	0	0	0
34 h	A/D CONVERTER MODE REG.	R/W	ADCM	0	0	0	1
35 h	A/D CONVERTER DATA REG. 1	R	ADCR1	undefined			
	PORT PG PULL UP RESISTOR SELECTION REG.	W	PGPC	F			
36 h	A/D CONVERTER DATA REG. 2	R	ADCR2	undefined			
	PORT PH PULL UP RESISTOR SELECTION REG.	W	PHPC	F			
37 h	WDT & ADC CONTROL REG.	W	WACR	0	0	0	0
	A/D CONVERTER DATA REG. 3	R	ADCR3	undefined			
38 h	ADDRESS BUFF REGISTER 0	R/W	ABR0	undefined			
39 h	ADDRESS BUFF REGISTER 1	R/W	ABR1	undefined			
3A h	ADDRESS BUFF REGISTER 2	R/W	ABR2	undefined			
3B h	ADDRESS BUFF REGISTER 3	R/W	ABR3	undefined			
3C h	DATA BUFF REGISTER 0	R/W	DBR0	undefined			
3D h	DATA BUFF REGISTER 1	R/W	DBR1	undefined			
3E h	DATA BUFF REGISTER 2	R/W	DBR2	undefined			
3F h	DATA BUFF REGISTER 3	R/W	DBR3	undefined			

Note1> '-' is reserved bit , it must be read to "0".
Note2> 'X' is undefined bit
Note3> * Using the bit access Instruction, bit is read-modified operation (SETR1/CLRR1/STC Instructions)

3. I/O PORTS

The ADAM42ADAM42X11XX has maximum 17 Input or output ports which are R1 (4 I/O), PB (4 I/O), PC0 (1 Output), PG(4 I/O), PH(4 I/O).
R1, PB and PG input Port have Stop Release selection register.
Pull-up resistor of R1, PB, PG and PH ports can be selectable by program.
R1, PB, PG and PH ports contains data direction register which controls I/O and data register which stores port data.
R1, PB, PC, PG, PH Output Ports have Open Drain selection register and Data register.

3.1. Port R1

Pin Name	Port Selection	Function Selection
R10 / $\overline{EC1}$	R10 (I/O)	Event Count($\overline{EC1}$) Input
R11	R11 (I/O)	-
R12 / AN7 / T1O	R12 (I/O)	AN7 Input / Timer-1 Output
R13 / BUZ	R13 (I/O)	Buzzer Output

3.1.1. R1 Stop Release Selection Register (R1ST)

bit	3	2	1	0	
R1ST	R1ST3	R1ST2	R1ST1	R1ST0	*01h*
Initial value	1	1	1	1	
R/W	W	W	W	W	

R1 Stop Release Selection Register (R1ST) is 4-bit register, and can assign stop release pin or not. If R1ST is selected as “0”, stop release function is enabled and if selected as “1”, it is disabled. R1ST is write-only register and initialized as “Fh” in reset state.

3.1.2. R1 Pull-up Resistor Control Register (R1PC)

bit	3	2	1	0	
R1PC	R1PC3	R1PC2	R1PC1	R1PC0	*02h*
Initial value	1	1	1	1	
R/W	W	W	W	W	

R1 pull-up resistor control register (R1PC) is 4-bit register and can control pull-up on or off each bit, if corresponding port is selected as input. If R1PC is selected as “0”, pull-up is enabled and if selected as “1”, it is disabled. R1PC is write-only register and initialized as “Fh” in reset state. The pull-up is automatically disabled, if corresponding port is selected as output.

3.1.3. R1 Open Drain Assign Register (R1OD)

bit	3	2	1	0	
R1OD	R1OD3	R1OD2	R1OD1	R1OD0	*03h*
Initial value	0	0	0	0	
R/W	W	W	W	W	

R1 Open Drain Assign Register (R1OD) is 4-bit register, and can assign R1 port as open drain output port each bit If R1OD is selected as “0”, port R1 is open drain output, and if selected as “1”, it is push-pull output. R1OD is write-only register and initialized as “0h” in reset state.

3.1.4. R1 Data Register (R1)

bit	3	2	1	0	
R1	R13	R12	R11	R10	*04h*
Initial value	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	

R1 data register (R1) is 4-bit register to store data of port R1.
When set as the output state by R1DD, and data is written in R1, data is outputted into R1 pin.
When set as the input state, input state of pin is read. The initial value of R1 is “Fh” in reset state.
Using the bit access Instruction, bit is read-modified operation (SETR1/CLRR1/STC Instructions)

3.1.5. R1 I/O Data Direction Register (R1DD)

bit	3	2	1	0	
R1DD	R1DD3	R1DD2	R1DD1	R1DD0	*05h*
Initial value	0	0	0	0	
R/W	W	W	W	W	

R1 I/O Data Direction Register (R1DD) is 4-bit register, and can assign input state or output state to each bit. If R1DD is “0”, port R1 is in the input state, and if “1”, it is in the output state. R1DD is write-only register. Since R1DD is initialized as “0h” in reset state, the whole port R1 becomes input state.

3.1.6. Timer Output Port Selection Register (TOPSR)

bit	3	2	1	0	
TOPSR	**BUZE**	**T1OE**	T0OE	PWME	*06h*
Initial value	0	0	0	0	
R/W	W	W	W	W	

Timer Output Port Selection Register (TOPSR) is 4-bit register, and can assign the Function mode for each bit. When set as “0”, corresponding bit of TOPSR acts as normal I/O port selection mode, and when set as “1”, it becomes function selection mode.

Selection Mode of TOPSR

Bit Name	Value	Selection Mode	Remarks
BUZE	0	**R13** Select (I/O)	-
	1	Buzzer output select (output)	-
T1OE	0	**R12** Select (I/O)	**AN7** can be selected by setting the bit3 of APSR2 reg.
	1	Timer-1 output select (output)	
T0OE	0	PB2 Select (I/O)	-
	1	Timer-0 output select (output)	-
PWME	0	PG0 Select (I/O)	AN0 can be selected by setting the bit0 of APSR1 reg.
	1	PWM output select (output)	

TOPSR is write-only register and initialized as “0h” in reset state. Therefore, becomes I/O Port mode.

3.1.7. External Interrupt Input Port Selection Register (EIPSR)

bit	3	2	1	0	
EIPSR	**EC1E**	INT2E	INT1E1	INT1E0	*0Ch*
Initial value	0	0	0	0	
R/W	W	W	W	W	

External Interrupt Input Port selection Register (EIPSR) is 4-bit register, and can assign the Function mode for each bit. When set as “0”, corresponding bit of EIPSR acts as normal I/O port selection mode, and when set as “1”, it becomes function selection mode.

Selection Mode of EIPSR

Bit Name	Value	Selection Mode	Remarks
EC1E	0	**R10** I/O Select (I/O)	-
	1	Event Count Input select (Input)	-
INT2E	0	PG2 I/O Select (I/O)	AN2 can be selected by setting the bit2 of APSR1 reg.
	1	External Interrupt 2 Input select (Input)	
INT1E1	0	PG1 I/O Select (I/O)	AN1 can be selected by setting the bit1 of APSR1 reg.
	1	External Interrupt 1 Input select (Input)	
INT1E0	0	PB0 I/O Select (I/O)	-
	1	External Interrupt 1 Input select (Input)	-

EIPSR is write-only register and initialized as “0h” in reset state. Therefore, becomes I/O Port mode.
Only one bit of INT1E1 and INT1E0 must be used at one application.

3.1.8. ADC Input Port Selection Register 2 (APSR2)

bit	3	2	1	0	
APSR2	**ANSEL7**	ANSEL6	ANSEL5	ANSEL4	*31h*
Initial value	0	0	0	0	
R/W	W	W	W	W	

ADC Input Port selection Register-2 (APSR2) is 4-bit register, and can assign the Function mode for each bit. When set as “0”, corresponding bit of APSR2 acts as normal I/O port selection mode, and when set as “1”, it becomes function selection mode.

Selection Mode of APSR2

Bit Name	Value	Selection Mode	Remarks
ANSEL7	0	**R12** Select (I/O)	**T1O** can be selected by setting the bit2 of TOPSR reg.
	1	Analog Input 7 select (Input)	
ANSEL6	0	PH2 Select (I/O)	-
	1	Analog Input 6 select (Input)	-
ANSEL5	0	PH1 Select (I/O)	-
	1	Analog Input 5 select (Input)	-
ANSEL4	0	PH0 Select (I/O)	-
	1	Analog Input 4 select (Input)	-

APSR2 is write-only register and initialized as “0h” in reset state. Therefore, becomes I/O Port mode.

3.2. Port PB

Pin Name	Port Selection	Function Selection
PB0 / INT1	PB0 (I/O)	INT1 Input
PB1	PB1 (I/O)	-
PB2 / T0O	PB2 (I/O)	Timer-0 Output
PB3	PB3 (I/O)	-

3.2.1. PB Stop Release Selection Register (PBST)

bit	3	2	1	0	
PBST	PBST3	PBST2	PBST1	PBST0	*08h*
Initial value	1	1	1	1	
R/W	W	W	W	W	

PB Stop Release Selection Register (PBST) is 4-bit register, and can assign stop release pin or not. If PBST is selected as ``0``, stop release function is enabled and if selected as ``1``, it is disabled. PBST is write-only register and initialized as ``F h`` in reset state.

3.2.2. PB Pull-up Resistor Control Register (PBPC)

bit	3	2	1	0	
PBPC	PBPC3	PBPC2	PBPC1	PBPC0	*09h*
Initial value	1	1	1	1	
R/W	W	W	W	W	

PB pull-up resistor control register (PBPC) is 4-bit register and can control pull-up on or off each bit, if corresponding port is selected as input. If PBPC is selected as ``0``, pull-up is enabled and if selected as ``1``, it is disabled. PBPC is write-only register and initialized as “Fh” in reset state. The pull-up is automatically disabled, if corresponding port is selected as output.

3.2.3. PB Open Drain Assign Register (PBOD)

bit	3	2	1	0	
PBOD	PBOD3	PBOD2	PBOD1	PBOD0	*0Ah*
Initial value	0	0	0	0	
R/W	W	W	W	W	

PB Open Drain Assign Register (PBOD) is 4-bit register, and can assign PB port as open drain output port each bit If PBOD is selected as “0”, port PB is open drain output, and if selected as “1”, it is push-pull output. PBOD is write-only register and initialized as “0h” in reset state.

3.2.4. PB Data Register (PB)

bit	3	2	1	0	
PB	PB3	PB2	PB1	PB0	*0Bh*
Initial value	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	

PB data register (PB) is 4-bit register to store data of port PB. The initial value of PB is “Fh” in reset state. Using the bit access Instruction, bit is read-modified operation (SETR1/CLRR1/STC Instructions)

3.2.5. Timer Output Port Selection Register (TOPSR)

bit	3	2	1	0	
TOPSR	BUZE	T1OE	**T0OE**	PWME	*06h*
Initial value	0	0	0	0	
R/W	W	W	W	W	

Timer Output Port selection Register (TOPSR) is 4-bit register, and can assign the Function mode for each bit. When set as “0”, corresponding bit of TOPSR acts as normal I/O port selection mode, and when set as “1”, it becomes function selection mode.

Selection Mode of TOPSR

Bit Name	Value	Selection Mode	Remarks
BUZE	0	R13 Select (I/O)	-
	1	Buzzer output select (output)	-
T1OE	0	R12 Select (I/O)	AN7 can be selected by setting the bit3 of APSR2 reg.
	1	Timer-1 output select (output)	
T0OE	0	**PB2** Select (I/O)	-
	1	Timer-0 output select (output)	-
PWME	0	PG0 Select (I/O)	AN0 can be selected by setting the bit0 of APSR1 reg.
	1	PWM output select (output)	

TOPSR is write-only register and initialized as “0h” in reset state. Therefore, becomes I/O Port mode.

3.2.6. External Interrupt Input Port Selection Register (EIPSR)

bit	3	2	1	0	
EIPSR	EC1E	INT2E	INT1E1	**INT1E0**	*0Ch*
Initial value	0	0	0	0	
R/W	W	W	W	W	

External Interrupt Input Port selection Register (EIPSR) is 4-bit register, and can assign the Function mode for each bit. When set as “0”, corresponding bit of EIPSR acts as normal I/O port selection mode, and when set as “1”, it becomes function selection mode.

Selection Mode of EIPSR

Bit Name	Value	Selection Mode	Remarks
EC1E	0	R10 I/O Select (I/O)	-
	1	Event Count Input select (Input)	-
INT2E	0	PG2 I/O Select (I/O)	AN2 can be selected by setting the bit2 of APSR1 reg.
	1	External Interrupt 2 Input select (Input)	
INT1E1	0	PG1 I/O Select (I/O)	AN1 can be selected by setting the bit1 of APSR1 reg.
	1	External Interrupt 1 Input select (Input)	
INT1E0	0	**PB0** I/O Select (I/O)	-
	1	External Interrupt 1 Input select (Input)	-

EIPSR is write-only register and initialized as “0h” in reset state. Therefore, becomes I/O Port mode.
Only one bit of INT1E1 and INT1E0 must be used at one application.

3.2.7. PB I/O Data Direction Register (PBDD)

bit	3	2	1	0	
PBDD	PBDD3	PBDD2	PBDD1	PBDD0	*0Dh*
Initial value	0	0	0	0	
R/W	W	W	W	W	

PB I/O Data Direction Register (PBDD) is 4-bit register, and can assign input state or output state to each bit. If PBDD is ``0``, port PB is in the input state, and if ``1``, it is in the output state. PBDD is write-only register. Since PBDD is initialized as ``0 h`` in reset state, the whole port PB becomes input state.

3.3. Port PC

3.3.1. PC Open Drain Assign Register (PCOD)

bit	3	2	1	0	
PCOD	-	-	-	PCOD0	*0Eh*
Initial value	-	-	-	0	
R/W	-	-	-	W	

PC Open Drain Assign Register (PCOD) is 1-bit register, and can assign PC port as open drain output port each bit If PCOD is selected as ``0``, port PC is open drain output, and if selected as ``1``, it is push-pull output. PCOD is write-only register and initialized as ``0 h`` in reset state.

3.3.2. PC Data Register (PC)

bit	3	2	1	0	
PC	-	-	-	PC0	*0Fh*
Initial value	1	1	1	1	
R/W	R	R	R	R/W	

PC data register (PC) is 1-bit register to store data of port PC.
The initial value of PC is “Fh” in reset state.

3.4. Port PG

Pin Name	Port Selection	Function Selection
PG0 /AN0/AVREF/PWM	PG0 (I/O)	AN0 or AVREF Input / PWM Output
PG1 /AN1/INT1	PG1 (I/O)	AN1 Input / INT1 Input
PG2 /AN2/INT2	PG2 (I/O)	AN2 Input / INT2 Input
PG3 /AN3	PG3 (I/O)	AN3 Input

3.4.1. PG Stop Release Selection Register (PGST)

bit	3	2	1	0	
PGST	PGST3	PGST2	PGST1	PGST0	*2Ah*
Initial value	1	1	1	1	
R/W	W	W	W	W	

PG Stop Release Selection Register (PGST) is 4-bit register, and can assign stop release pin or not. If PGST is selected as “0”, stop release function is enabled and if selected as “1”, it is disabled. PGST is write-only register and initialized as “Fh” in reset state.

3.4.2. PG Open Drain Assign Register (PGOD)

bit	3	2	1	0	
PGOD	PGOD3	PGOD2	PGOD1	PGOD0	*2Bh*
Initial value	0	0	0	0	
R/W	W	W	W	W	

PG Open Drain Assign Register (PGOD) is 4-bit register, and can assign PG port as open drain output port each bit If PGOD is selected as ``0``, port PG is open drain output, and if selected as ``1``, it is push-pull output. PGOD is write-only register and initialized as ``0 h`` in reset state.

3.4.3. PG Data Register (PG)

bit	3	2	1	0	
PG	PG3	PG2	PG1	PG0	*2Ch*
Initial value	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	

PG data register (PG) is 4-bit register to store data of port PG.
The initial value of PG is “Fh” in reset state.
Using the bit access Instruction, bit is read-modified operation (SETR1/CLRR1/STC Instructions)

3.4.4. Timer Output Port Selection Register (TOPSR)

bit	3	2	1	0	
TOPSR	BUZE	T1OE	T0OE	**PWME**	*06h*
Initial value	0	0	0	0	
R/W	W	W	W	W	

Timer Output Port selection Register (TOPSR) is 4-bit register, and can assign the Function mode for each bit. When set as “0”, corresponding bit of TOPSR acts as normal I/O port selection mode, and when set as “1”, it becomes function selection mode.

Selection Mode of TOPSR

Bit Name	Value	Selection Mode	Remarks
BUZE	0	R13 Select (I/O)	-
	1	Buzzer output select (output)	-
T1OE	0	R12 Select (I/O)	AN7 can be selected by setting the bit3 of APSR2 reg.
	1	Timer-1 output select (output)	
T0OE	0	PB2 Select (I/O)	-
	1	Timer-0 output select (output)	-
PWME	0	**PG0** Select (I/O)	**AN0** can be selected by setting the bit0 of APSR1 reg.
	1	PWM output select (output)	

TOPSR is write-only register and initialized as “0h” in reset state. Therefore, becomes I/O Port mode.

3.4.5. External Interrupt Input Port Selection Register (EIPSR)

bit	3	2	1	0	
EIPSR	EC1E	**INT2E**	**INT1E1**	INT1E0	*0Ch*
Initial value	0	0	0	0	
R/W	W	W	W	W	

External Interrupt Input Port selection Register (EIPSR) is 4-bit register, and can assign the Function mode for each bit. When set as “0”, corresponding bit of EIPSR acts as normal I/O port selection mode, and when set as “1”, it becomes function selection mode.

Selection Mode of EIPSR

Bit Name	Value	Selection Mode	Remarks
EC1E	0	R10 I/O Select (I/O)	-
	1	Event Count Input select (Input)	-
INT2E	0	**PG2** I/O Select (I/O)	**AN2** can be selected by setting the bit2 of APSR1 reg.
	1	External Interrupt 2 Input select (Input)	
INT1E1	0	**PG1** I/O Select (I/O)	**AN1** can be selected by setting the bit1 of APSR1 reg.
	1	External Interrupt 1 Input select (Input)	
INT1E0	0	PB0 I/O Select (I/O)	-
	1	External Interrupt 1 Input select (Input)	-

EIPSR is write-only register and initialized as “0h” in reset state. Therefore, becomes I/O Port mode.
Only one bit of INT1E1 and INT1E0 must be used at one application.

3.4.6. ADC Input Port Selection Register 1 (APSR1)

bit	3	2	1	0	
APSR1	**ANSEL3**	**ANSEL2**	**ANSEL1**	**ANSEL0**	*2Dh*
Initial value	0	0	0	0	
R/W	W	W	W	W	

ADC Input Port selection Register-1 (APSR1) is 4-bit register, and can assign the Function mode for each bit. When set as “0”, corresponding bit of APSR1 acts as normal I/O port selection mode, and when set as “1”, it becomes function selection mode.

Selection Mode of APSR1

Bit Name	Value	Selection Mode	Remarks
ANSEL3	0	**PG3** Select (I/O)	-
	1	Analog Input 3 select (Input)	-
ANSEL2	0	**PG2** Select (I/O)	**INT2** can be selected by setting the bit2 of EIPSR reg.
	1	Analog Input 2 select (Input)	
ANSEL1	0	**PG1** Select (I/O)	**INT1** can be selected by setting the bit1 of EIPSR reg.
	1	Analog Input 1 select (Input)	
ANSEL0	0	**PG0** Select (I/O)	**PWM** can be selected by setting the bit0 of TOPSR reg.
	1	Analog Input 0 select (Input), or AVREF Input select (Input)	

APSR1 is write-only register and initialized as “0h” in reset state. Therefore, becomes I/O Port mode.

3.4.7. PG I/O Data Direction Register (PGDD)

bit	3	2	1	0	
PGDD	PGDD3	PGDD2	PGDD1	PGDD0	*2Eh*
Initial value	0	0	0	0	
R/W	W	W	W	W	

PG I/O Data Direction Register (PGDD) is 4-bit register, and can assign input state or output state to each bit. If PGDD is ``0``, port PG is in the input state, and if ``1``, it is in the output state. PGDD is write-only register. Since PGDD is initialized as ``0 h`` in reset state, the whole port PG becomes input state.

3.4.8. PG Pull-up Resistor Control Register (PGPC)

bit	3	2	1	0	
PGPC	PGPC3	PGPC2	PGPC1	PGPC0	*35h*
Initial value	1	1	1	1	
R/W	W	W	W	W	

PG pull-up resistor control register (PGPC) is 4-bit register and can control pull-up on or off each bit, if corresponding port is selected as input. If PGPC is selected as ``0``, pull-up is enabled and if selected as ``1``, it is disabled. PGPC is write-only register and initialized as “Fh” in reset state. The pull-up is automatically disabled, if corresponding port is selected as output.

3.5. Port PH

Pin Name	Port Selection	Function Selection
PH0 /AN4	PH0 (I/O)	AN4 Input
PH1 /AN5	PH1 (I/O)	AN5 Input
PH2 /AN6	PH2 (I/O)	AN6 Input
PH3	PH3 (I/O)	-

3.5.1. PH Open Drain Assign Register (PHOD)

bit	3	2	1	0	
PHOD	PHOD3	PHOD2	PHOD1	PHOD0	*2Fh*
Initial value	0	0	0	0	
R/W	W	W	W	W	

PH Open Drain Assign Register (PHOD) is 4-bit register, and can assign PH port as open drain output port each bit If PHOD is selected as ``0``, port PH is open drain output, and if selected as ``1``, it is push-pull output. PHOD is write-only register and initialized as ``0 h`` in reset state.

3.5.2. PH Data Register (PH)

bit	3	2	1	0	
PH	PH3	PH2	PH1	PH0	*30h*
Initial value	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	

PH data register (PH) is 4-bit register to store data of port PH.
The initial value of PH is “Fh” in reset state.
Using the bit access Instruction, bit is read-modified operation (SETR1/CLRR1/STC Instructions)

3.5.3. ADC Input Port Selection Register 2 (APSR2)

bit	3	2	1	0	
APSR2	ANSEL7	**ANSEL6**	**ANSEL5**	**ANSEL4**	*31h*
Initial value	0	0	0	0	
R/W	W	W	W	W	

ADC Input Port selection Register-2 (APSR2) is 4-bit register, and can assign the Function mode for each bit. When set as “0”, corresponding bit of APSR2 acts as normal I/O port selection mode, and when set as “1”, it becomes function selection mode.

Selection Mode of APSR2

Bit Name	Value	Selection Mode	Remarks
ANSEL7	0	R12 Select (I/O)	T1O can be selected by setting the bit2 of TOPSR reg.
	1	Analog Input 7 select (Input)	
ANSEL6	0	**PH2** Select (I/O)	-
	1	Analog Input 6 select (Input)	-
ANSEL5	0	**PH1** Select (I/O)	-
	1	Analog Input 5 select (Input)	-
ANSEL4	0	**PH0** Select (I/O)	-
	1	Analog Input 4 select (Input)	-

APSR2 is write-only register and initialized as “0h” in reset state. Therefore, becomes I/O Port mode.

3.5.4. PH I/O Data Direction Register (PHDD)

bit	3	2	1	0	
PHDD	PHDD3	PHDD2	PHDD1	PHDD0	*32h*
Initial value	0	0	0	0	
R/W	W	W	W	W	

PH I/O Data Direction Register (PHDD) is 4-bit register, and can assign input state or output state to each bit. If PHDD is ``0``, port PH is in the input state, and if ``1``, it is in the output state. PHDD is write-only register. Since PHDD is initialized as ``0 h`` in reset state, the whole port PH becomes input state.

3.5.5. PH Pull-up Resistor Control Register (PHPC)

bit	3	2	1	0	
PHPC	PHPC3	PHPC2	PHPC1	PHPC0	*36h*
Initial value	1	1	1	1	
R/W	W	W	W	W	

PH pull-up resistor control register (PHPC) is 4-bit register and can control pull-up on or off each bit, if corresponding port is selected as input. If PGPC is selected as ``0``, pull-up is enabled and if selected as ``1``, it is disabled. PHPC is write-only register and initialized as “Fh” in reset state. The pull-up is automatically disabled, if corresponding port is selected as output.

※ ***Ports Status in RESET, STOP, SLEEP and LVD Mode***

Pin Name	I/O	Shared Pins	@RESET	@STOP	@SLEEP	@LVD
R10	I/O	EC1/KS0	Input (without Pull-up)	State of before STOP	State of before SLEEP	Input (without Pull-up)
R11		RESET/KS1				
R12		OSC2/T1O/AN7 /KS2				
R13		OSC1/BUZ/KS3				
PB0	I/O	INT1/KS4	↑	↑	↑	↑
PB1		KS5				
PB2		T0O/KS6				
PB3		KS7				
PG0	I/O	PWM/AN0/AVREF /KS8	↑	↑	↑	↑
PG1		INT1/AN1/KS9				
PG2		INT2/AN2/KS10				
PG3		AN3/KS11				
PH0	I/O	AN4	↑	↑	↑	↑
PH1		AN5				
PH2		AN6				
PH3		-				
PC0	O	-	Hi-Z	↑	↑	Hi-Z
ROUT	O	-	`L` level output	`L` level output	↑	`L` level output

4. PERIPHERAL HARDWARE

4.1. Oscillation Circuit

Oscillation circuit is designed to be used either with a ceramic or crystal oscillator.
Clock from oscillation circuit makes CPU clock via clock pulse generator, and then provide peripheral hardware clock.

There are 4 types of Oscillation circuit and they can be divided in 13 different oscillator option modes. The user can used the Configuration Option Bits (XTS3 through XTS0) to select one of these 4 types. Refer to Table 4.1.

- XT : Crystal (Ceramic) Oscillator
- ERC : External RC Oscillator (2 modes)
- ECKIN : External Clock Input (2 modes)
- IRC : Internal RC Oscillator (8 modes)

First type is Crystal (Ceramic) oscillator circuit. OSC1 and OSC2 are the input and output, respectively, a inverting amplifier which can be set for use as an on-chip oscillator. It is designed to be used either with a ceramic resonator or crystal oscillator. In the STOP mode, oscillation stop, OSC2 state goes to “High”, OSC1 state goes to “Low”, and built-in feedback resistor is disabled.

Second type is External clock input circuit. Through the OSC1, external clock is driven. Minimum and maximum high and low times specified on the data sheet must be observed. OSC2/R12 is selectable the normal I/O port R12 or clock output (fosc/2). In STOP mode, OSC1 state does not go to “Low”, and external clock does not affect to Internal.

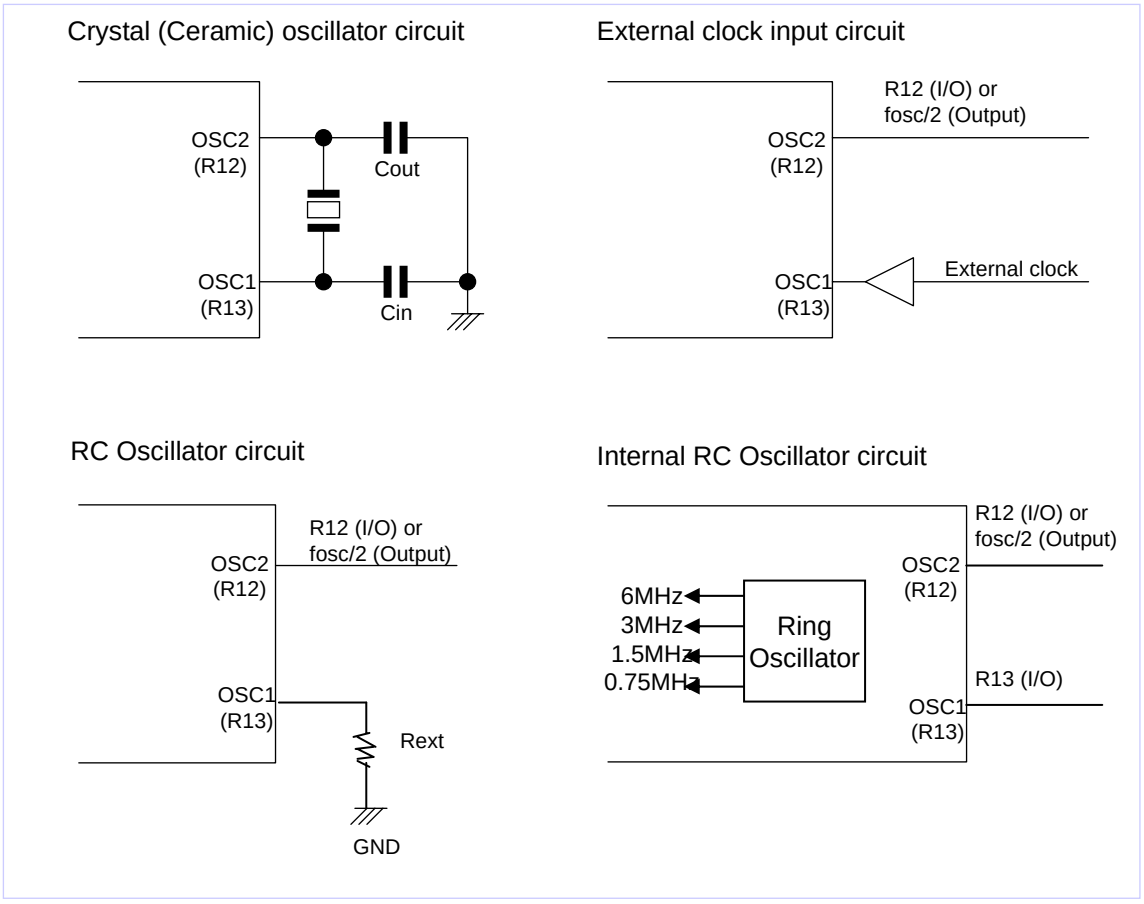


Fig. 4.1 Oscillator configurations

Another type is RC oscillation circuits. It can be constructed by connecting a resistor between OSC1 and GND. It offers additional cost savings for timing insensitive applications. The RC oscillator frequency is a function of the supply voltage, the external resistor (Rext) value, and the operating temperature. The user needs to take into account variation due to tolerance of external R components used. In STOP mode, OSC1 state goes to “Low”.

The other type is Internal RC Oscillator circuit. In this type, OSC1/R13 is used the normal I/O port R13, OSC2/R12 is selectable the normal I/O port R12 or clock output (fosc/2). The oscillator frequency, divided by 2, is output from the OSC2 pin, can be used for test purpose or to synchronize other logic. Because the Internal Oscillator is calibrated in Factory, don’t needed . In STOP mode, Internal RC oscillator is stopped.

Below table shows the selection of the oscillator type by the Configuration Option Bits (Address 8000h, XTS3 ~ XTS0). (Refer to 11.4.2. Configuration Option Bit Description)

Table. 4.1 Oscillator Type and Modes Selection

XTS3	XTS2	XTS1	XTS0	Oscillator Modes	OSC1	OSC2
1	1	1	1	Internal RC 3MHz	R13 (I/O)	R12 (I/O)
1	1	1	0	Internal RC 3MHz / PS1 Output	R13 (I/O)	1.5MHz (O)
1	1	0	1	Internal RC 1.5MHz	R13 (I/O)	R12 (I/O)
1	1	0	0	Internal RC 1.5MHz / PS1 Output	R13 (I/O)	0.75MHz (O)
1	0	1	1	Internal RC 0.75MHz	R13 (I/O)	R12 (I/O)
1	0	1	0	Internal RC 0.75MHz / PS1 Output	R13 (I/O)	0.375MHz (O)
1	0	0	1	Internal RC 6MHz	R13 (I/O)	R12 (I/O)
1	0	0	0	Internal RC 6MHz / PS1 Output	R13 (I/O)	3MHz (O)
0	1	1	1	External RC Oscillator	OSC1 (I)	R12 (I/O)
0	1	1	0	External RC Oscillator / PS1 Output	OSC1 (I)	PS1* (O)
0	1	0	1	XT Oscillator	OSC1 (I)	OSC2 (O)
0	1	0	0			
0	0	1	1	External Clock Input	OSC1 (I)	R12 (I/O)
0	0	1	0	External Clock Input / PS1 Output	OSC1 (I)	PS1* (O)
0	0	0	1	prohibited	-	-
0	0	0	0	prohibited	-	-

*** PS1 is divide by 2 of the oscillation frequency.**

4.2 Watch Dog Timer (WDT)

Watch dog timer is organized binary of 19 steps. The signal of $f_{OSC}/4$ cycle comes in the first step of WDT after WDT reset. If this counter was overflowed, reset signal automatically come out so that internal circuit is initialized. The overflow time is $2^{18} \times 4/f_{OSC}$ (262.144ms at f_{OSC} = 4.0MHz) Normally, the binary counter must be reset before the overflow by using reset instruction (WDTC), Power-on reset pulse or Low VDD detection pulse. It is constantly reset in STOP and SLEEP mode. When STOP and SLEEP are released, counting is restarted.
If it's executed the STOP instruction after setting the bit RCWDTEN of WACR to "1", the Internal RC-Ring Oscillated Watch-dog Timer (RCWDT) mode is activated.

4.2.1. WDT & ADC Control Register

bit	3	2	1	0	
WACR	**WDTRST**	**RWDTEN**	**RWDTCK**	ADCK2	*37h*
Initial value	0	0	0	0	
R/W	W	W	W	W	

WDTRST	0	WDT interrupt enable, when WDT Overflow is occurred in RCWDT Mode. (default)
	1	System Reset enable, when WDT Overflow is occurred in RCWDT Mode.
RWDTEN	0	RCWDT mode disable
	1	RCWDT Oscillator Enable & RCWDT mode enable
RWDTCK	0	WDT Input Clock selects 64us (typ. : VDD=5.0V, T=25℃)
	1	WDT Input Clock selects 16us (typ. : VDD=5.0V, T=25℃)
ADCK2 & ADCK	00	ADC Source Clock is PS0 (= 1/fXIN)
	01	ADC Source Clock is PS2 (= 4/fXIN)
	10	ADC Source Clock is PS1 (= 2/fXIN)
	11	ADC Source Clock is PS3 (= 8/fXIN)

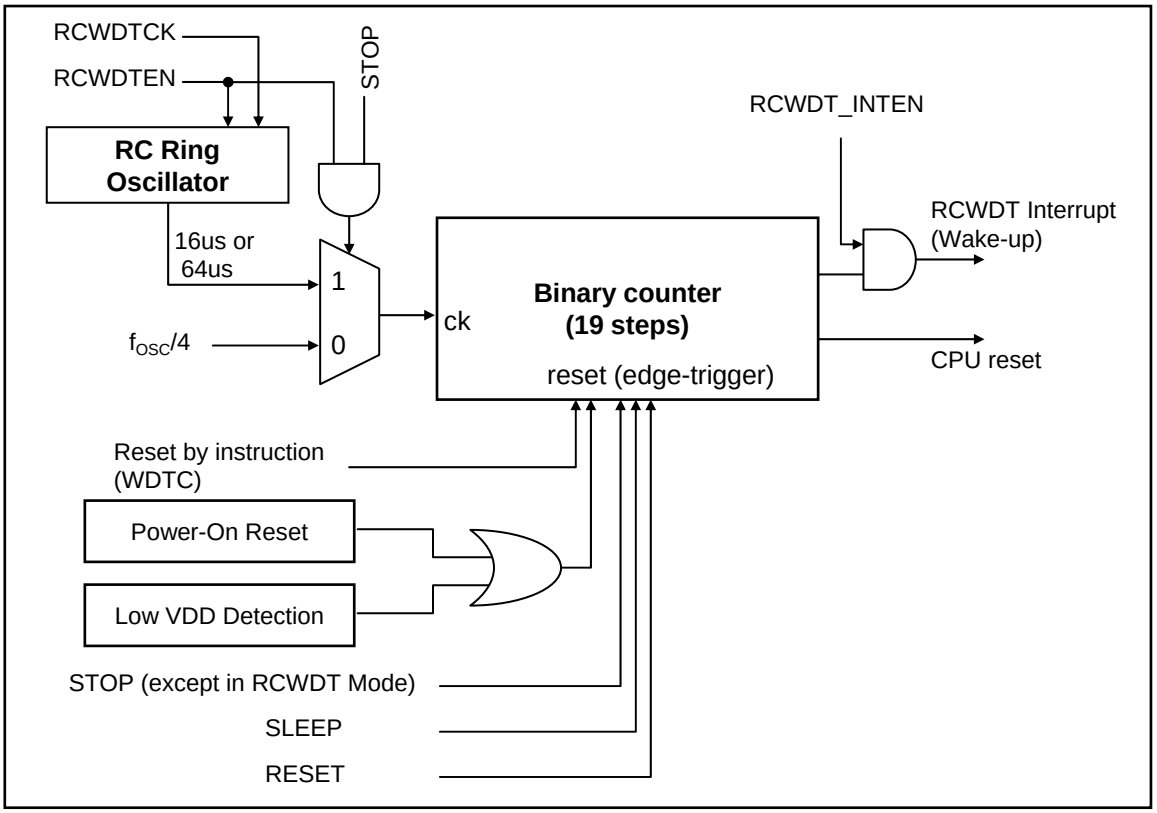


Fig 4-2 Block Diagram of Watch-dog Timer

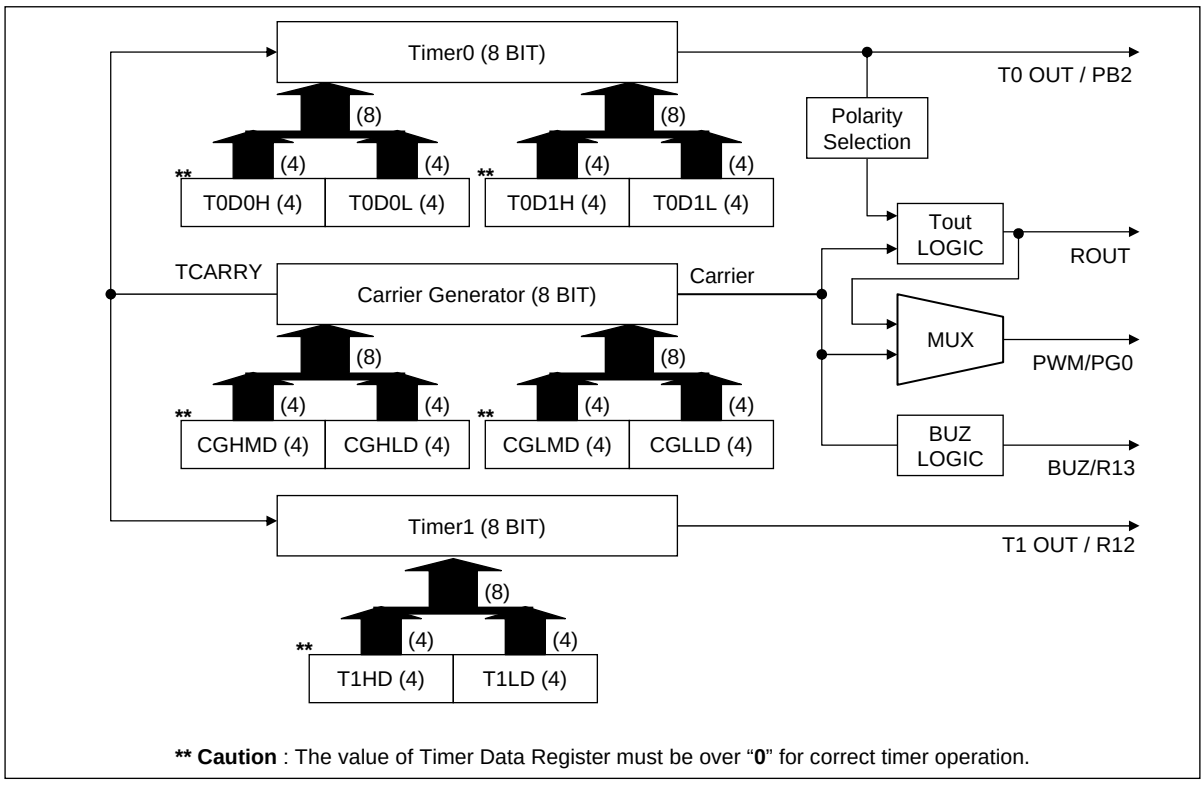
4.3. Timer

4.3.1. Timer operation mode

Timer is basically made of Timer Data Register, Timer Mode Register and control circuit. The types of Timer are 8bit binary counter Timer0 (T0), 8bit binary counter Timer1 (T1), Carrier Generator (CG) and 16-bit binary counter(Timer1 + Timer0).

Timer0 Data Register consists of Timer0 Data 0 High Register (T0D0H), Timer0 Data 0 Low Register (T0D0L), Timer0 Data 1 High Register (T0D1H) and Timer0 Data 1 Low Register (T0D1L).
Timer1 Data Register consists of Timer1 Low Data Register (T1LD), Timer1 High Data Register (T1HD).
Carrier Generator consists of Carrier Generator High MSB Data Register (CGHMD), Carrier Generator High LSB Data Register (CGHLD), Carrier Generator Low MSB Data Register (CGLMD) and Carrier Generator Low LSB Data Register (CGLLD).

Timer0	-. 8-bit Interval Timer -. 8-bit Capture Timer -. 8-bit rectangular-wave output	-. 16-bit Interval Timer -. 16-bit Event Counter -. 16-bit Capture Timer -. 16-bit rectangular-wave output
Timer1	-. 8-bit Interval Timer -. 8-bit Event Counter -. 8-bit Capture Timer -. 8-bit rectangular-wave output	
Carry Generator	-. 8-bit Interval Timer -. 8-bit rectangular-wave output	



**** Caution** : The value of Timer Data Register must be over "**0**" for correct timer operation.

Fig. 4.3 8-bit Timer / Counter Block diagram

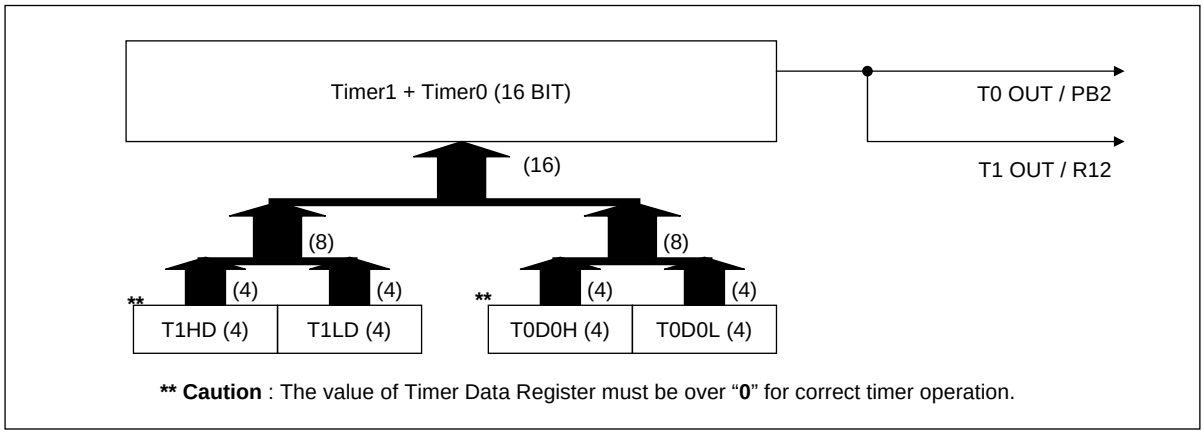


Fig. 4.4 16-bit Timer / Counter Block diagram

4.3.1.1. Timer01 Mode Register

bit	3	2	1	0	
T01MR	16BIT	CAP1E	CAP0E	PWMS	*29h*
Initial Value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

PWMS	PWM Output selection	0	ROUT selection
		1	TCARRY selection (output of Carrier Generator)
CAP0E	Timer0 Capture Mode selection	0	Timer/Counter Mode
		1	Capture Mode
CAP1E	Timer1 Capture Mode selection	0	Timer/Counter Mode
		1	Capture Mode
16BIT	16-bit Timer Mode selection	0	8-bit Timer Mode
		1	16-bit Timer Mode

• Timer 0 only counts with 'T0D0H+T0D0L' and can occur the interrupt in every counter overflow, if timer0 operates at 16-bit Timer mode or 8/16-bit Capture mode.

4.3.1.2. Timer0 Mode Register

bit	3	2	1	0	
T0MR	T0CS	T0CN	T0CK1	T0CK0	*1Ah*
Initial Value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

T0CK1 & T0CK0	Input clock selection	00	TCK1 (500ns)
		01	TCK2 (1us)
		10	TCK3 (2us)
		11	TCARRY (output of Carrier Generator)
T0CN	Timer0 Pause / Continue Control	0	Timer0 Pause
		1	Timer0 Continue
T0CS	Timer0 Stop / Start Control	0	Timer0 Stop
		1	Timer0 Clear and Start

• Timer 0 counts with 'T0D0H+T0D0L' first, after overflowed counts with 'T0D1H+T0D1L'.
• Be sure to use Timer0 Control (T0CN, T0CS, CAP0E) at 16-bit Timer Mode.

4.3.1.3. Timer1 Mode Register

bit	3	2	1	0	
T1MR	T1CS	T1CN	T1CK1	T1CK0	*1Ch*
Initial Value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

T1CK1 & T1CK0	Input clock selection	00	EC
		01	TCK2 (1us)
		10	TCK3 (2us)
		11	TCARRY (output of Carrier Generator)
T1CN	Timer1 Pause / Continue Control	0	Timer1 Pause
		1	Timer1 Continue
T1CS	Timer1 Stop / Start Control	0	Timer1 Stop
		1	Timer1 Clear and Start

4.3.1.4. Carrier Generator Mode Register

bit	3	2	1	0	
CGMR	CGCS	CGON	CGCK1	CGCK0	*1Eh*
Initial Value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

CGCK1 & CGCK0	Input clock selection	00	TCK1 (500ns)
		01	TCK2 (1us)
		10	TCK3 (2us)
		11	TCK4 (4us)
CGON	Carrier Generator Output Control	0	Output of ROUT without Carrier Pulse
		1	Output of ROUT with Carrier Pulse
CGCS	Carrier Generator Stop / Start Control	0	Carrier Generator Stop
		1	Carrier Generator Clear and Start

• Carrier Generator don't have a function of Pause & Continue.

4.3.1.5. ROUT Control Register

bit	3	2	1	0	
RCR	PR1	PR0	PRON	REM	*1Dh*
Initial Value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

REM	Output of ROUT Bit Control (When PRON=0)	0	ROUT output Low
		1	ROUT output High
PRON	PR0 / PR1 Function Control	0	PR0 / PR1 Function Disable ('REM' bit active)
		1	PR0 / PR1 Function Enable ('REM' bit inactive)
PR0	Preset of ROUT Bit Control (When PRON=1)	0	ROUT 'L' on counting Timer0 DATA0 (T0D0H+T0D0L)
		1	ROUT 'H' on counting Timer0 DATA0 (T0D0H+T0D0L)
PR1	Preset of ROUT Bit Control (When PRON=1)	0	ROUT 'L' on counting Timer0 DATA1 (T0D1H+T0D1L)
		1	ROUT 'H' on counting Timer0 DATA1 (T0D1H+T0D1L)

• ROUT Pin is controlled by REM when PRON bit = 0.
• ROUT Pin is controlled by PR0, PR1 when PRON bit = 1.
Because Timer0 counts with Data 0 (T0D0H+T0D0L) first, ROUT pin is controlled by PR0 initially.

4.3.1.6. Timer0 DATA 0 High/Low Register

bit	3	2	1	0		bit	3	2	1	0	
T0D0H					1Fh	**T0D0L**					20h
Initial Value	-	-	-	-		Initial Value	-	-	-	-	
R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W	

Note: *The T0D0x, T0CRx(Timer0 Count Reg.) and T0CPx(Timer0 Capture Reg.) are in same address. In the capture mode, reading operation is read the T0CPx, not T0CRx because path is opened to the T0CPx, and T0D0x is only for writing operation.*

4.3.1.7. Timer0 DATA 1 High/Low Register

bit	3	2	1	0		bit	3	2	1	0	
T0D1H					21h	**T0D1L**					22h
Initial Value	-	-	-	-		Initial Value	-	-	-	-	
R/W	W	W	W	W		R/W	W	W	W	W	

4.3.1.8. Timer1 High/Low DATA Register

bit	3	2	1	0		bit	3	2	1	0	
T1HD					23h	**T1LD**					24h
Initial Value	-	-	-	-		Initial Value	-	-	-	-	
R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W	

Note: *The T1xD, T1CRx(Timer1 Count Reg.) and T1CPx(Timer1 Capture Reg.) are in same address. In the capture mode, reading operation is read the T1CPx, not T1CRx because path is opened to the T1CPx, and T1xD is only for writing operation.*

4.3.1.9. Carrier Generator High MSB/LSB Data Register

bit	3	2	1	0		bit	3	2	1	0	
CGHMD					25h	**CGHLD**					26h
Initial Value	-	-	-	-		Initial Value	-	-	-	-	
R/W	W	W	W	W		R/W	W	W	W	W	

4.3.1.10. Carrier Generator Low MSB/LSB Data Register

bit	3	2	1	0		bit	3	2	1	0	
CGLMD					27h	**CGLLD**					28h
Initial Value	-	-	-	-		Initial Value	-	-	-	-	
R/W	W	W	W	W		R/W	W	W	W	W	

4.3.2. Function of 8-bit Timer & Counter

freq = 4MHz

8bit Timer (Timer0)		8bit Timer (Timer1)		Carrier Generator (CG)	
Resolution (CK)	Max. Count	Resolution (CK)	Max. Count	Resolution (CK)	Max. Count
TCK1 : 0. 5 us	128 us	TCK1 : EC		TCK1 : 0. 5 us	128 us
TCK2 : 1 us	256 us	TCK2 : 1 us	256 us	TCK2 : 1 us	256 us
TCK3 : 2 us	512 us	TCK3 : 2 us	512 us	TCK3 : 2 us	512 us
TCARRY(*)		TCARRY(*)		TCK4 : 4 us	1024 us

(*) Resolution & Max. count of TCARRY clock is decided by output of Carrier Generator

4.3.2.1. Timer0 in 8-bit timer/counter mode

TIMER0 operates as a up-counter with two-8bit data register (T0D0H+T0D0L, T0D1H+T0D1L). When the value of the up-counter reaches the content of each Timer Data Register, the up-counter is cleared to “00 h”, but interrupt (T0IF) is occurred at the next clock after every 2’nd overflow when the value of the up-counter reaches the content of Timer Data 1 Register(T0D1H+T0D1L). Two timer data registers are loaded to compare with Timer0 counter whenever T0CS is set “1” from “0” and T0IF is occurred, therefore set to the next data before T0CS is set “1” from “0” or T0IF is occurred. Internal clock (TCK) and the output of Carrier Generator (TCARRY) is used as counter clock.

The counter execution is controlled by T0CS, T0CN of T0MR. T0CN is used to pause and continue Timer0 without clearing the counter and T0CS does to clear and start the counter. During counting-up, the value of counter can be read by instruction (***LDW DBR,T0CR***). Timer execution is stopped by the reset signal. The value of counter is cleared at STOP mode.

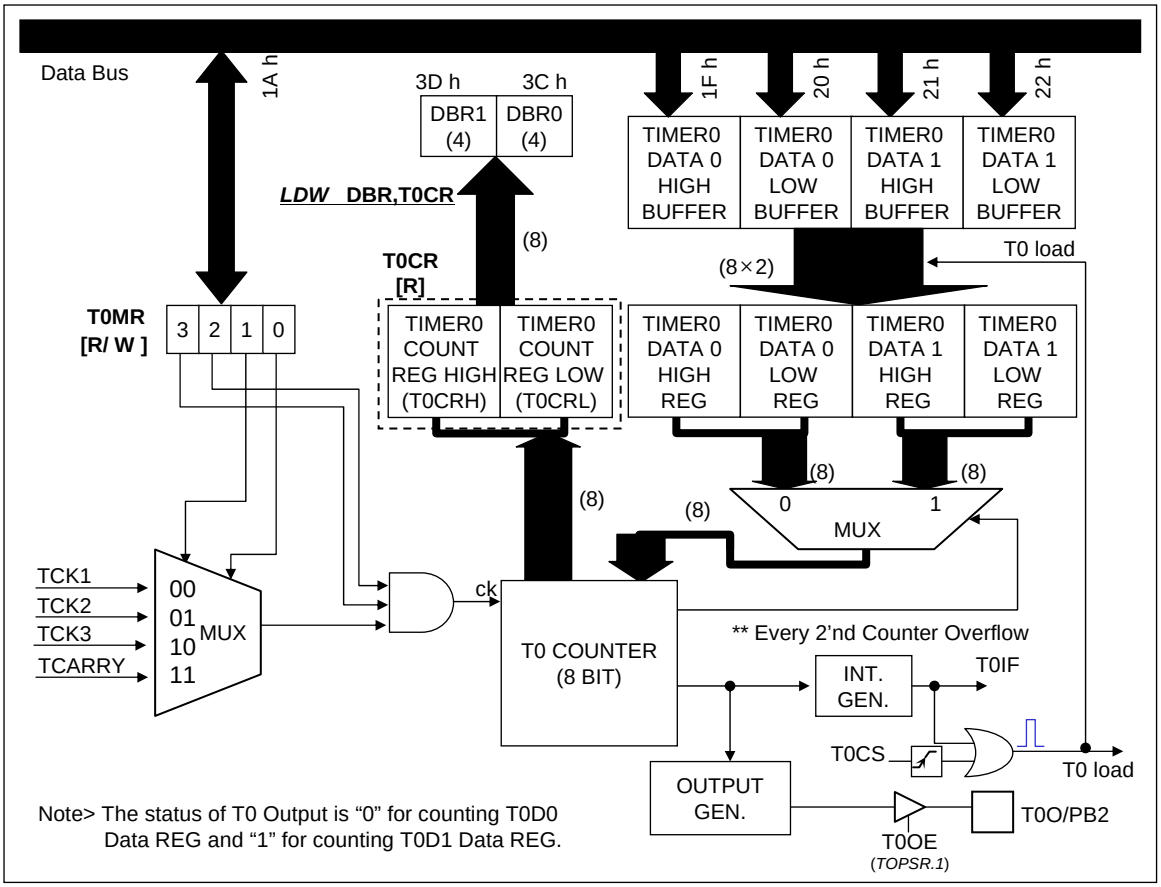


Fig. 4.5 Block Diagram of Timer0 in 8-bit timer/counter

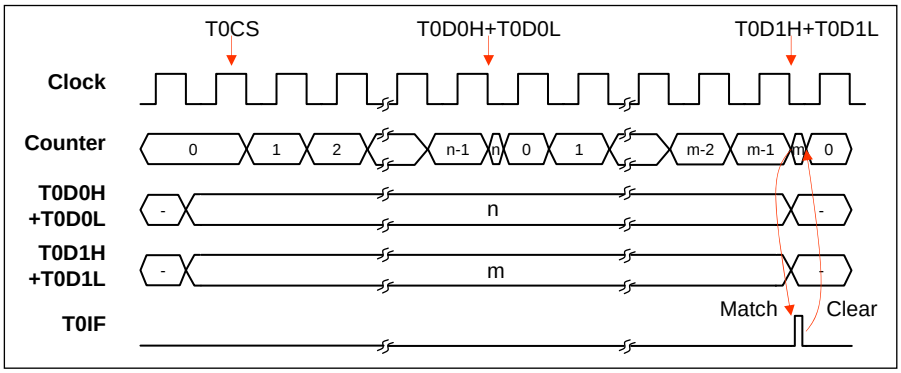


Fig. 4.6 Timing Chart of Timer0 in 8-bit timer/counter mode

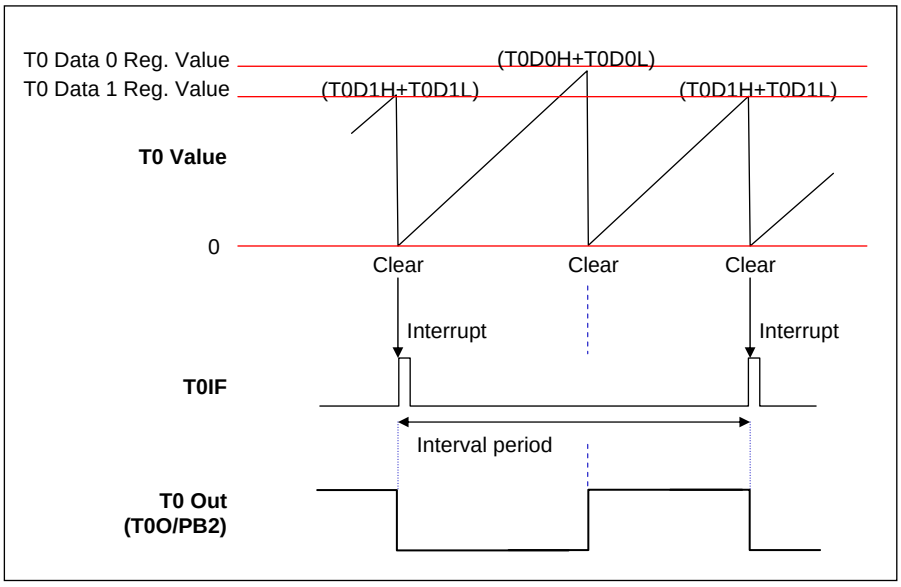


Fig. 4.7 Operation of Timer0 in 8-bit timer/counter mode

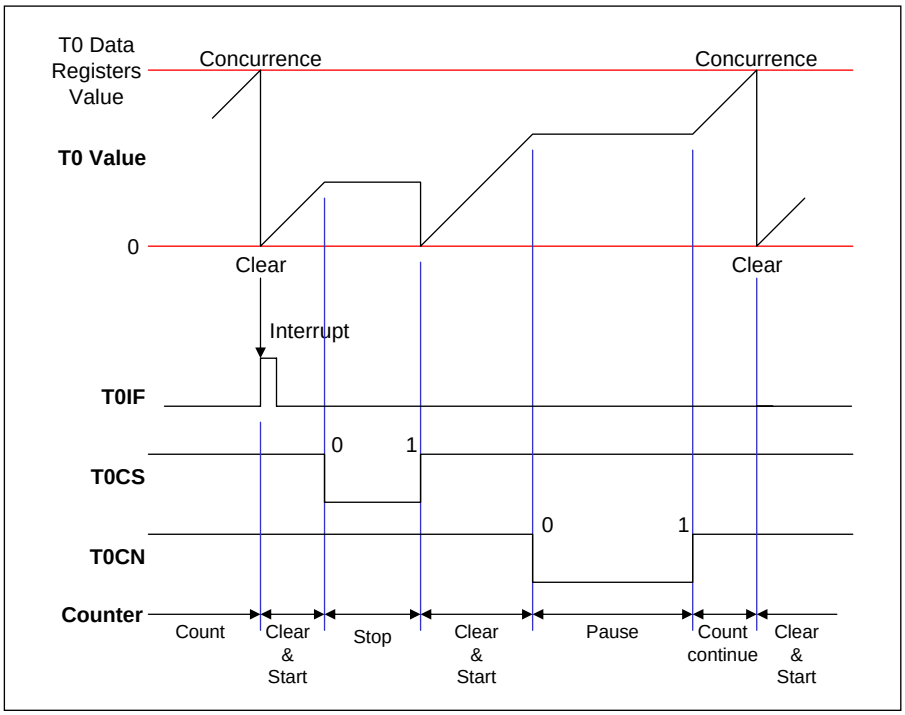


Fig. 4.8 Start / Stop operation of Timer0 in 8-bit timer/counter mode

4.3.2.2. Timer1 in 8-bit timer/counter mode

TIMER1 operates as a up-counter. Timer1 has a 8-bit data register (T1HD+T1LD).
When the value of the up-counter reaches the content of Timer Data Register, the up-counter is cleared to “00 h”, and interrupt (T1IF) is occurred at the next.
Timer data register is loaded to compare with Timer1 counter whenever T1CS is set “1” from “0” and T1IF is occurred, therefore set to the next data before T1CS is set “1” from “0” or T1IF is occurred.
External clock (EC), Internal clock (TCK) and the output of Carrier Generator (TCARRY) is used as counter clock.

The counter execution is controlled by T1CS, T1CN of T1MR.
T1CN is used to pause and continue Timer1 without clearing the counter and T1CS does to clear and start the counter. During counting-up, the value of counter can be read by instruction (***LDW DBR,T1CR***). Timer execution is stopped by the reset signal. The value of counter is cleared at STOP mode.

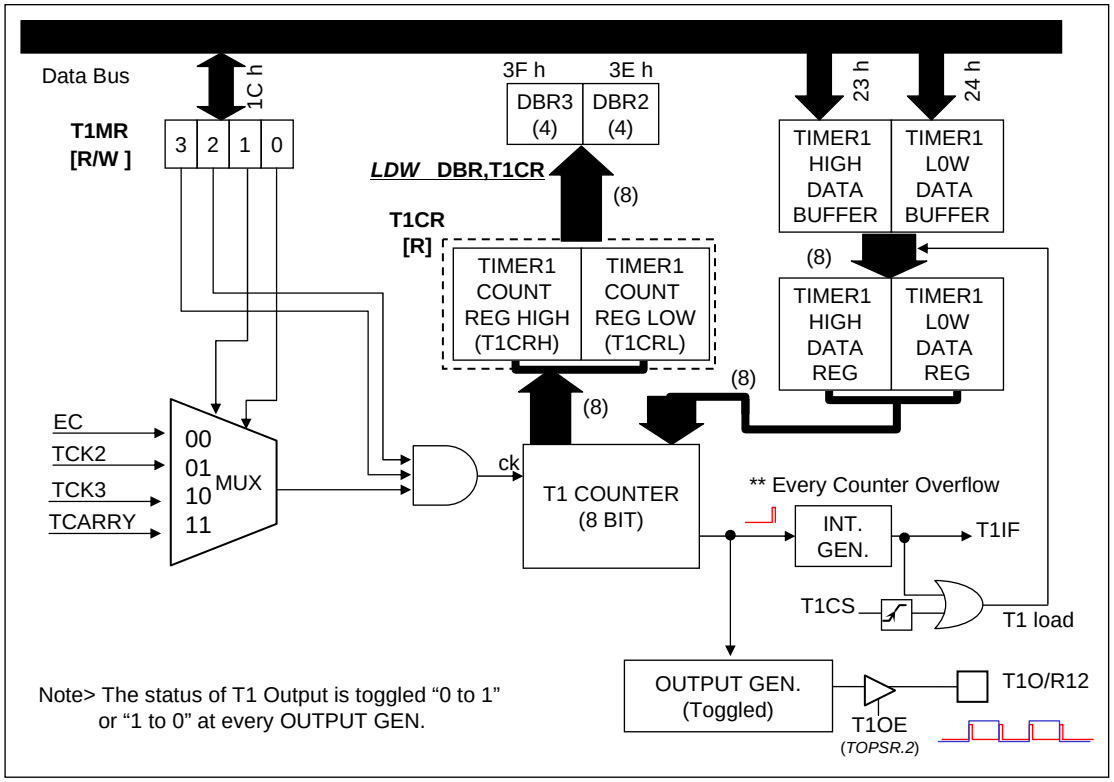


Fig. 4.9 Block Diagram of Timer1 in 8-bit timer/counter

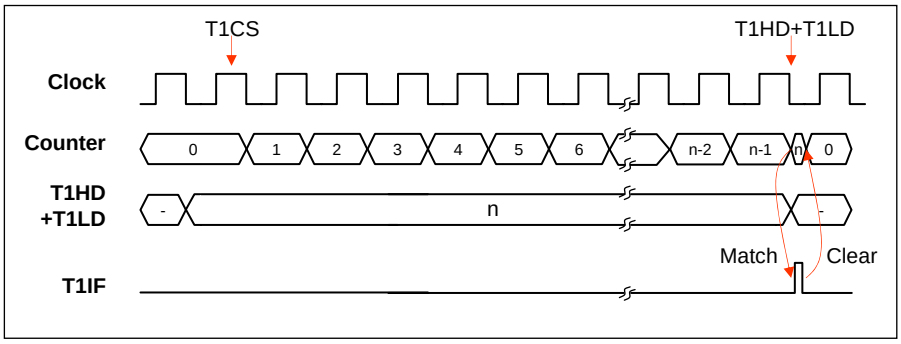


Fig. 4.10 Timing Chart of Timer1 in 8-bit timer/counter mode

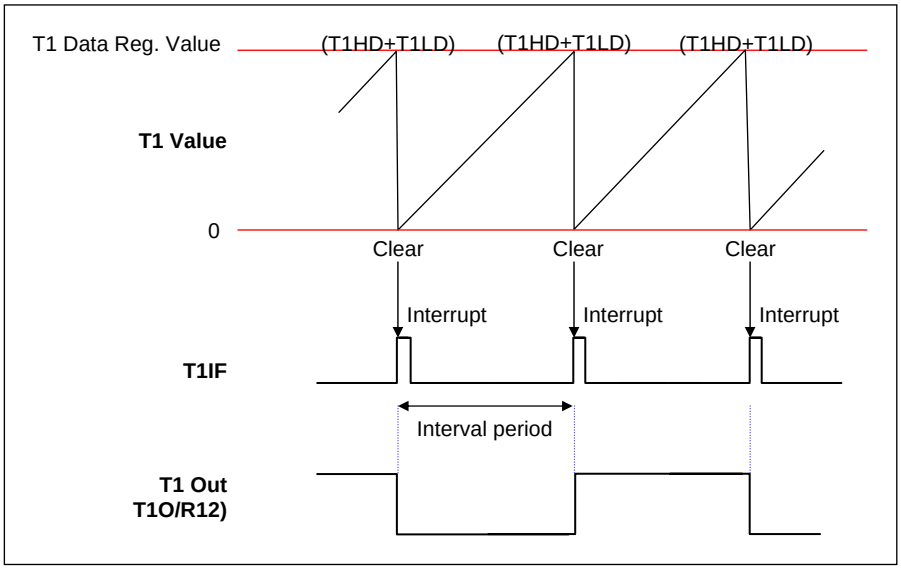


Fig. 4.11 Operation of Timer1 in 8-bit timer/counter mode

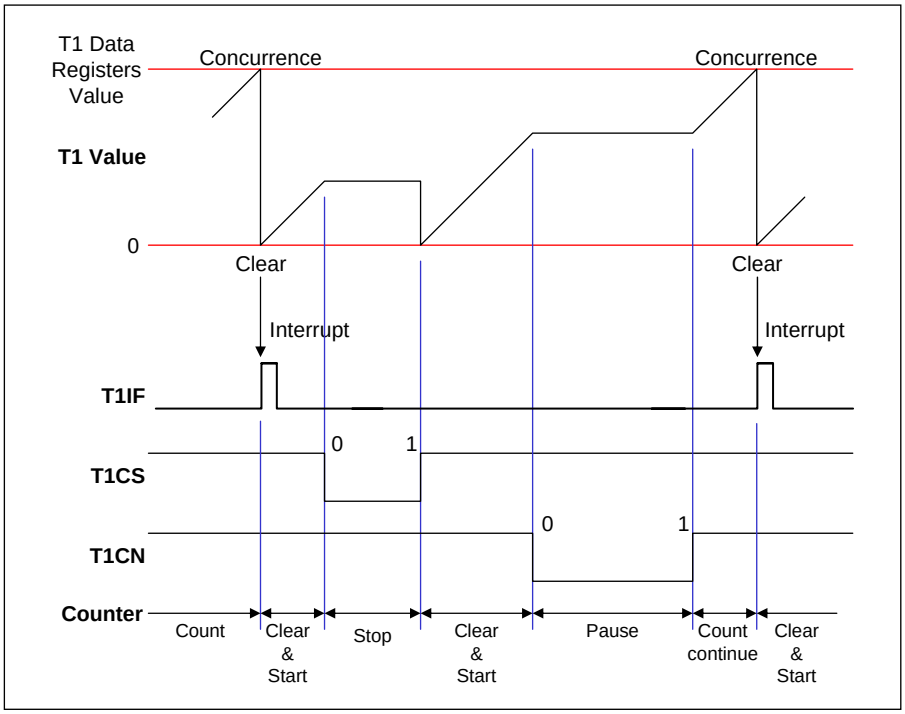


Fig. 4.12 Start / Stop operation of Timer1 in 8-bit timer/counter mode

4.3.2.3. Carrier Generator in 8-bit timer/counter mode

Carrier Generator operates as a up-counter.
Carrier Generator has two 8-bit data register (CGHMD+CGHLD, CGLMD+CGLLD).
When the value of the up-counter reaches the content of each Timer Data Register, the up-counter is cleared to “00 h”, but interrupt (CGIF) is occurred at the next clock after every 2’nd overflow when the value of the up-counter reaches the content of Timer Data 1 Register (CGHMD+CGHLD). Two timer data registers are loaded to compare with Carrier counter whenever CGCS is set “1” from “0” and CGIF is occurred, therefore set to the next data before CGCS is set “1” from “0” or CGIF is occurred.
Internal clock (TCK) is used as counter clock. It’s output (TCARRY) is used as counter clock for Timer0 and Timer1.

The counter execution is controlled by CGCS of CGMR.
When CGCS is set to “1”, count value of Carrier Generator is cleared and starts counting-up.
Carrier Generator first counts CGLMD+CGLLD and next CGHMD+CGHLD.
CGHMD+CGHLD are for the pulse of the carrier (BURST) and CGLMD+CGLLD are for the low of the carrier (PAUSE).
The value of counter can not be read. Timer execution is stopped by the reset signal. The value of counter is cleared at STOP mode.

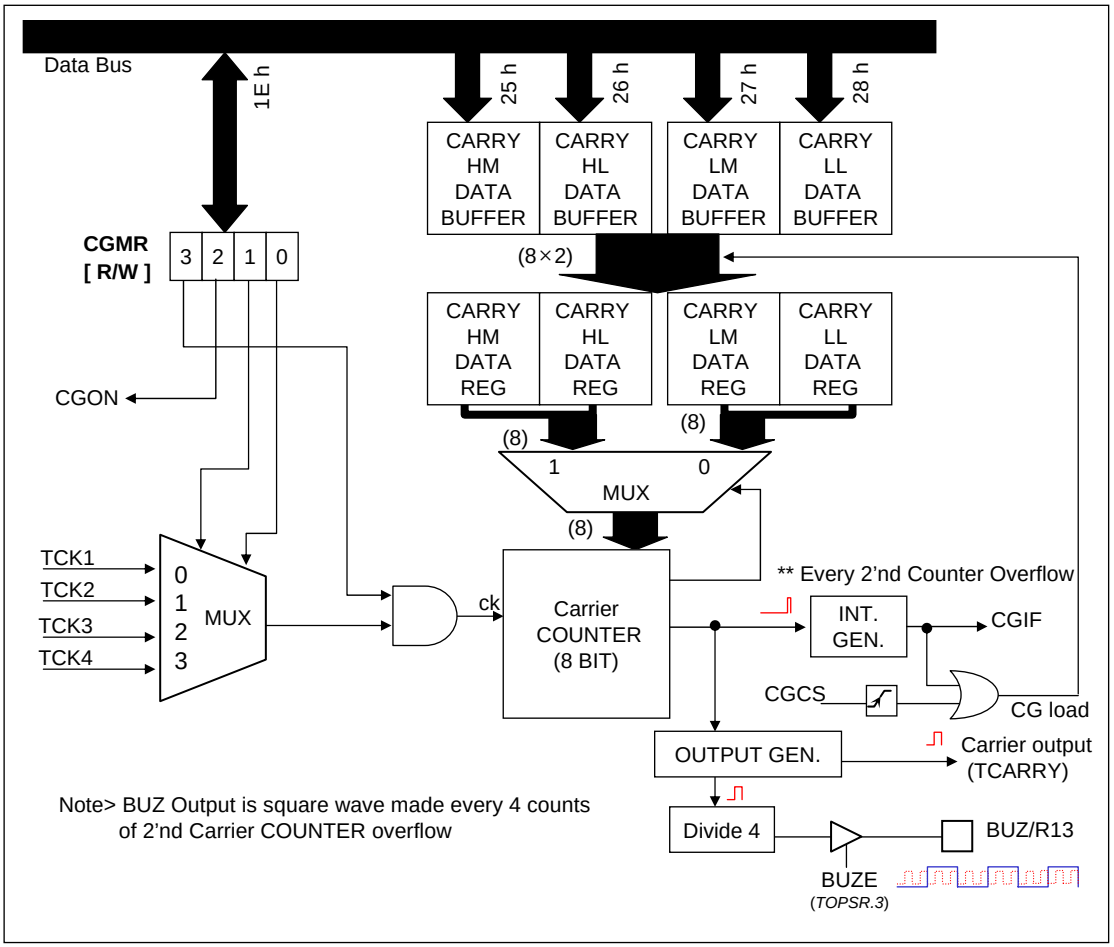


Fig. 4.13 Block Diagram of Carrier Generator

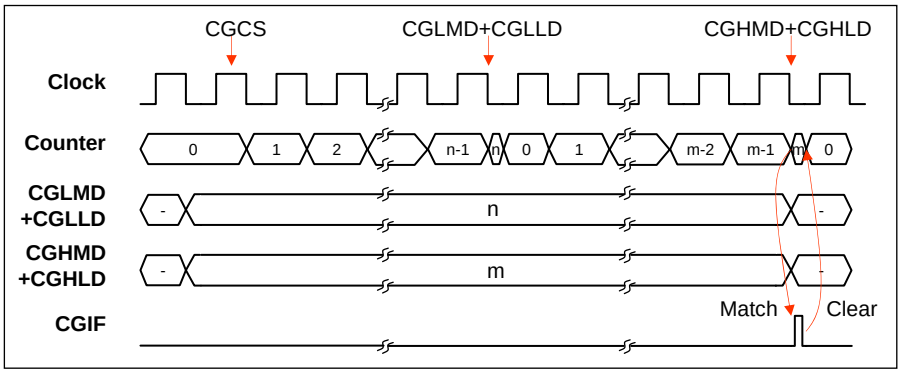


Fig. 4.14 Timing Chart of Carrier Generator

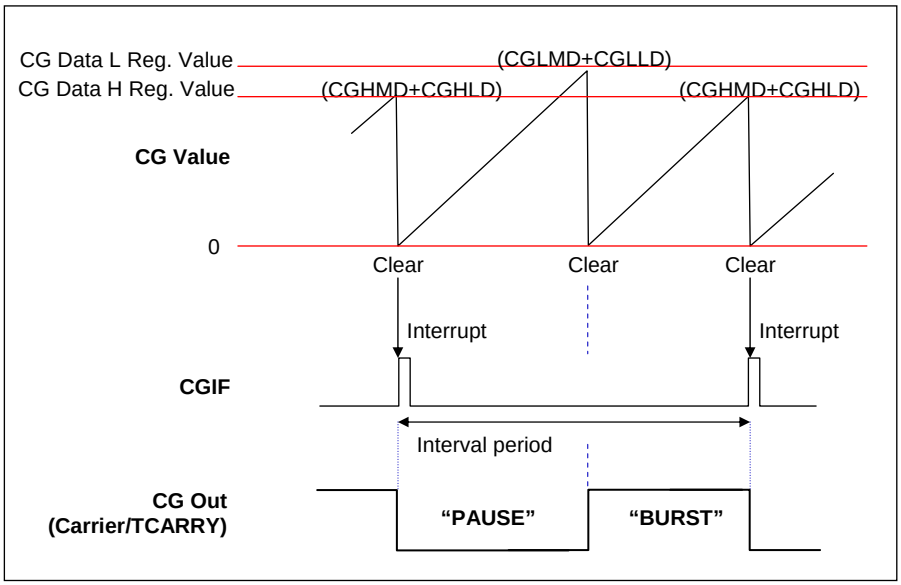


Fig. 4.15 Operation of Carrier Generator

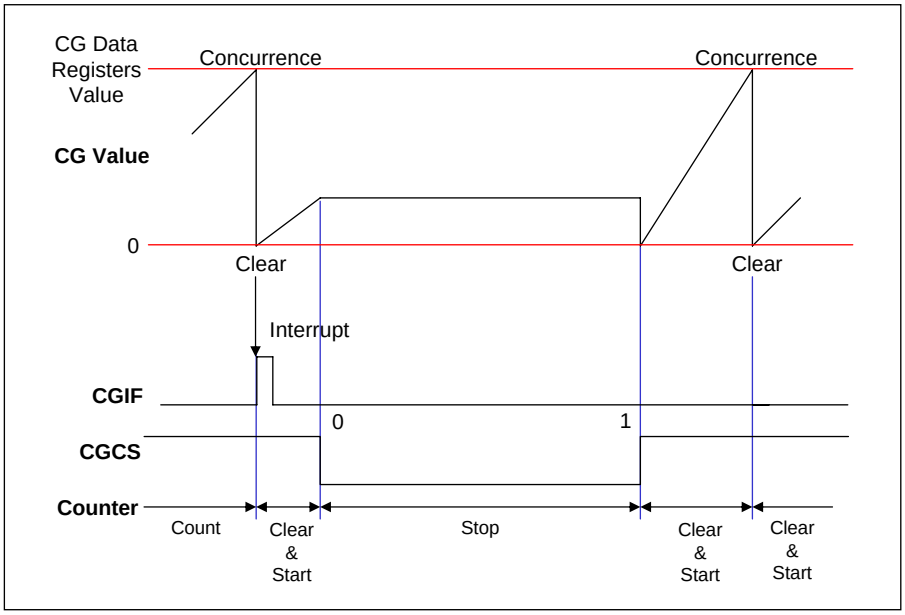


Fig. 4.16 Start / Stop operation of Carrier Generator

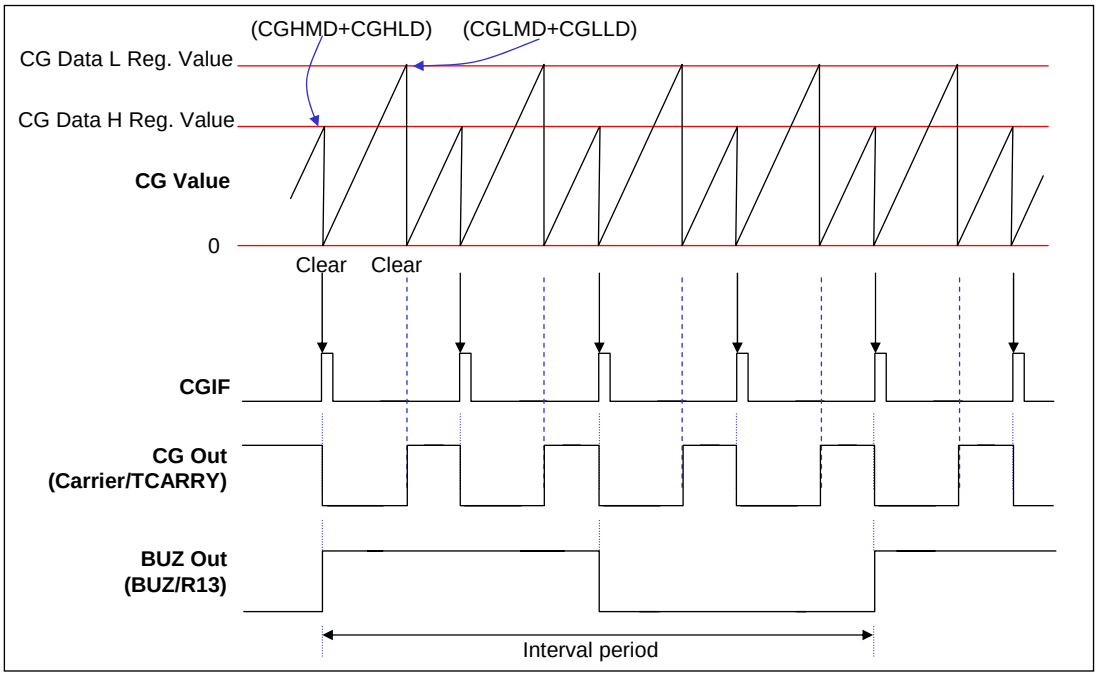


Fig. 4.17 Operation of BUZ Output

BUZ Frequency = 1 / {(CG Data L Reg. Value + CG Data H Reg. Value) x 4}

freq. = 4MHz

Source Clock	CG Data L/H Reg. Value (CGLMD+CGLLD, CGHMD+CGHLD) [unit : kHz]						
	01h/01h	01h/02h	02h/02h	02h/03h	- - -	FEh/FFh	FFh/FFh
TCK1 (00) : 0.5us	250.0	166.7	125.0	100.0	- - -	0.982	0.980
TCK2 (01) : 1.0us	125.0	83.33	62.50	50.0	- - -	0.491	0.490
TCK3 (10) : 2.0us	62.50	41.67	31.25	25.0	- - -	0.246	0.245
TCK4 (11) : 4.0us	31.25	20.83	15.63	12.50	- - -	0.123	0.123

4.3.2.4. Combinational Timer Output (ROUT, PWM)

ROUT and PWM is the output combined Timer0 Output with Carrier Generator Output (Carrier).
ROUT output is controlled by PR0, PR1, PRON, REM of RCR and CGON of CGMR.
PWM output is controlled by PWMS of T01MR.

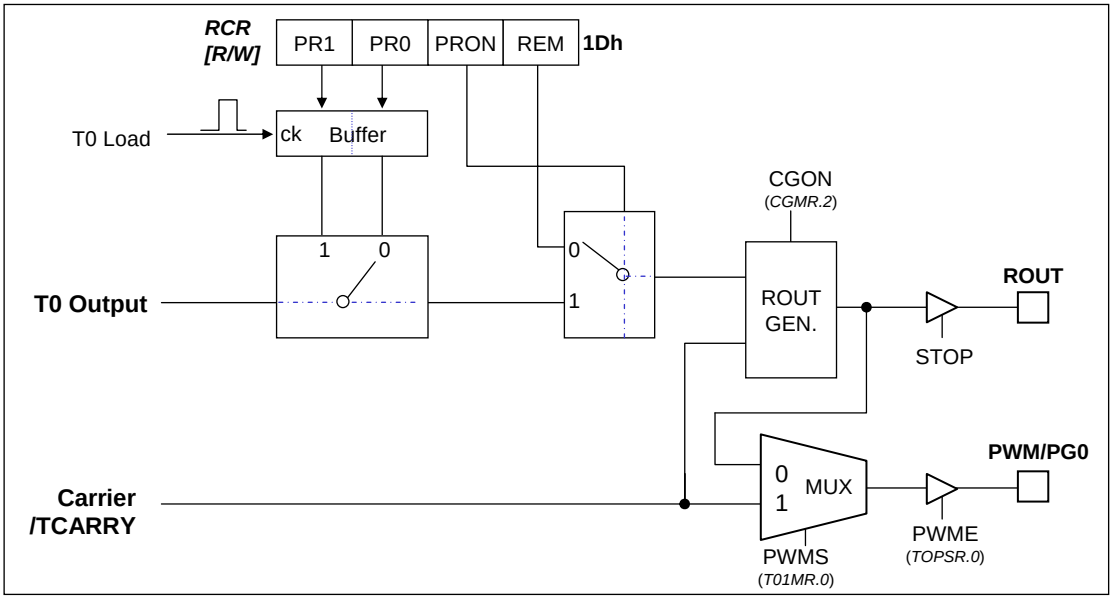
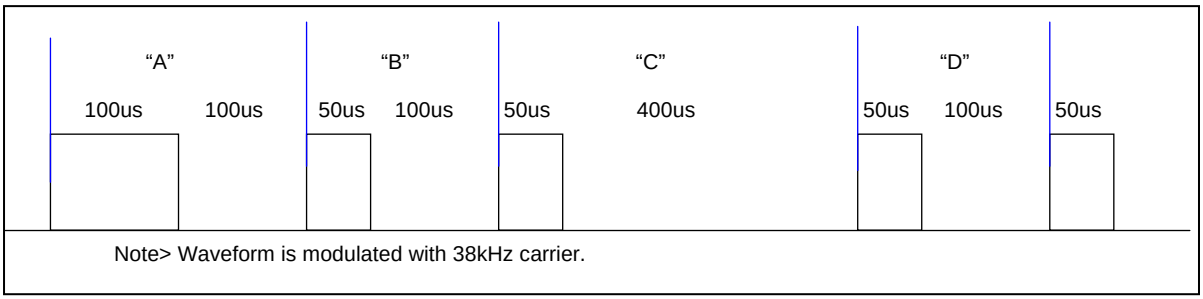
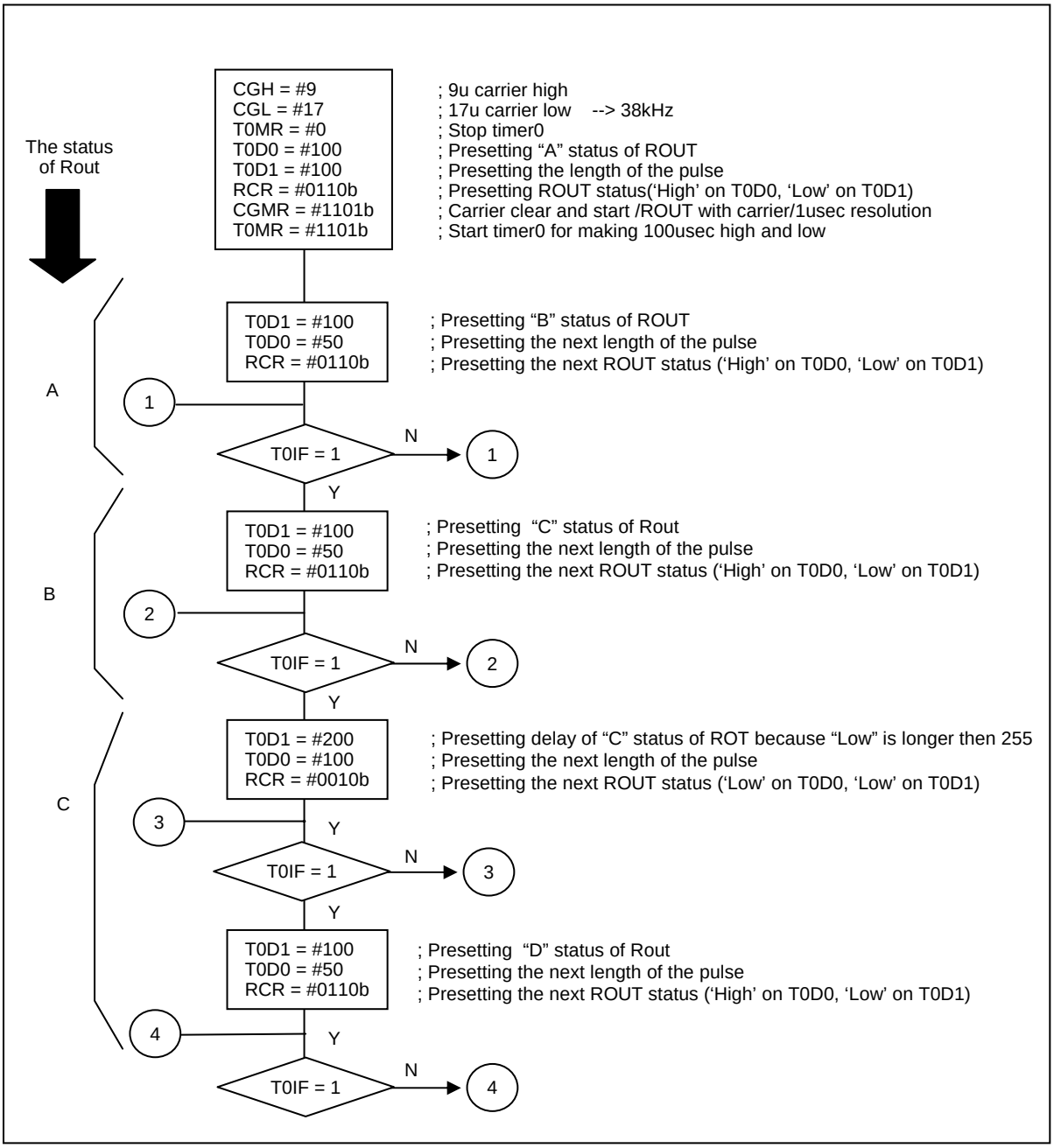


Fig. 4.18 Flow of controlling ROUT, PWM

4.3.2.4.1. Control of ROUT with using Timer0



Note> Waveform is modulated with 38kHz carrier.



4.3.3. Function of 16-bit Timer & Counter

freq = 4MHz

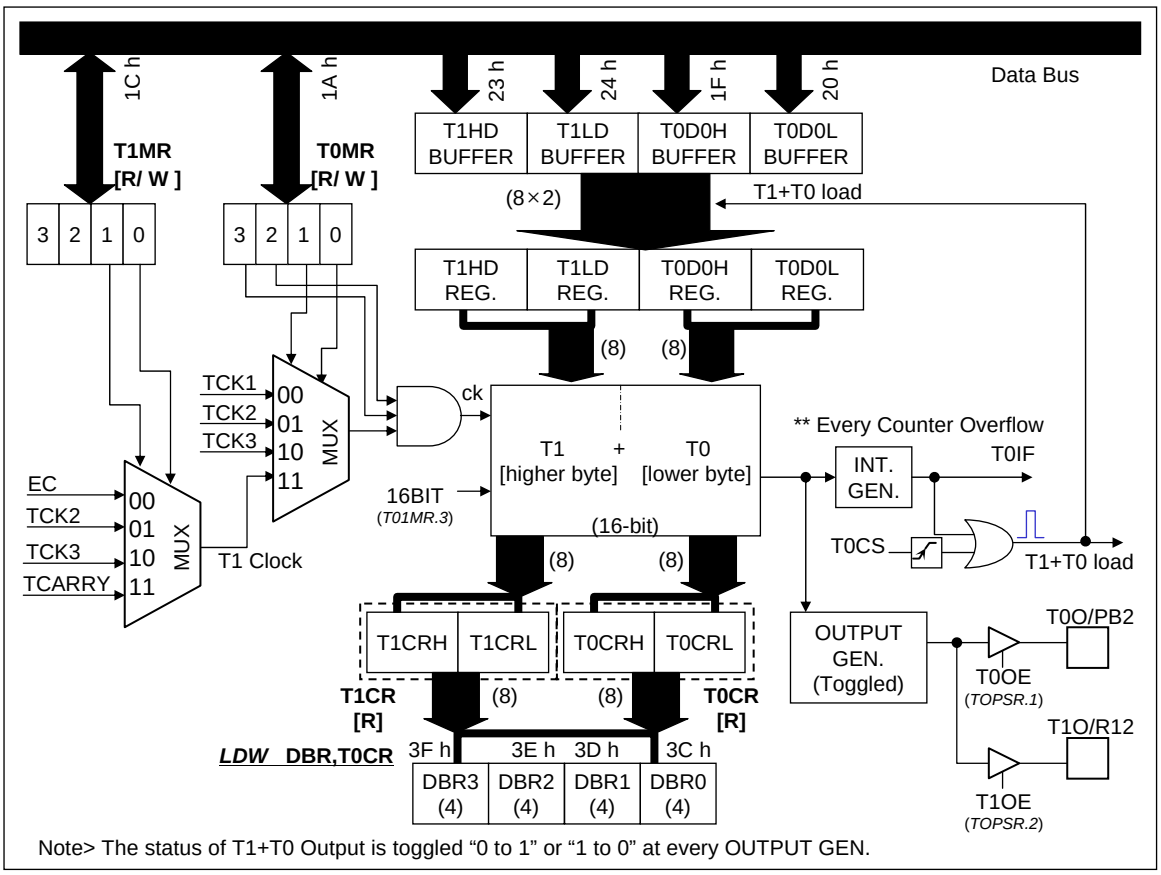
T0MR		T1MR		16bit Timer (Timer1 + Timer0)	
T0CK1	T0CK0	T1CK1	T1CK0	Resolution (CK)	Max. Count
0	0	-	-	TCK1 : 0.5 us	32768 us
0	1	-	-	TCK2 : 1 us	65536 us
1	0	-	-	TCK3 : 2 us	131072 us
1	1	0	0	EC	
		0	1	TCK2 : 1 us	65536 us
		1	0	TCK3 : 2 us	131072 us
		1	1	TCARRY (*)	

(*) Resolution & Max. count of TCARRY clock is decided by output of Carrier Generator

4.3.3.1. 16-bit timer/counter mode (Timer1 + Timer0)

If 16BIT of T01MR is set to “1”, TIMER1+TIMER0 operates as a 16-bit up-counter with 16bit data register (T1HD+T1LD+T0D0H+T0D0L). When the value of the up-counter reaches the content of Timer Data Register, the up-counter is cleared to “0000 h”, and Timer0 interrupt (T0IF) is occurred at the next clock. Timer1 interrupt (T1IF) is not occurred in 16-bit mode.
Timer data register is loaded to compare with Timer1+Timer0 counter whenever T0CS is set “1” from “0” and T0IF is occurred, therefore set to the next data before T0CS is set “1” from “0” or T0IF is occurred. External Clock (EC), Internal clock (TCK) and the output of Carrier Generator (TCARRY) is used as counter clock.

The counter execution is controlled by T0CS, T0CN of T0MR and 16BIT of T01MR. T0CN is used to pause and continue Timer1+Timer0 without clearing the counter and T0CS does to clear and start the counter. During counting-up, the value of 16-bit counter(T1 + T0) can be read by instruction (***LDW DBR, T0CR***). Timer execution is stopped by the reset signal. The value of counter is cleared at STOP mode.



Note> The status of T1+T0 Output is toggled “0 to 1” or “1 to 0” at every OUTPUT GEN.

Fig. 4.19 Block Diagram of Timer1+Timer0 in 16-bit timer/counter

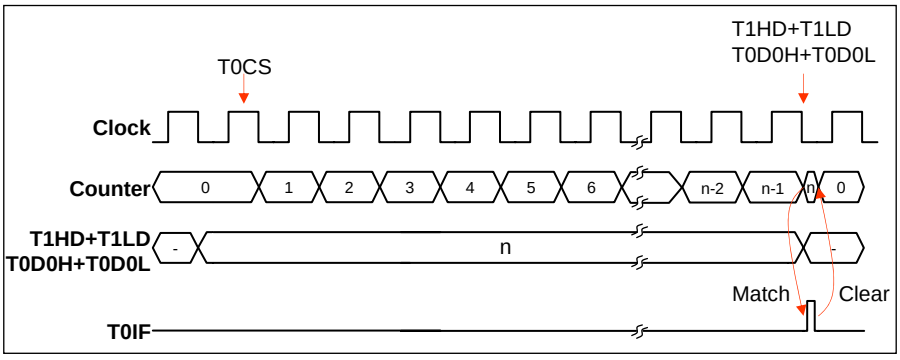


Fig. 4.20 Timing Chart of Timer1+Timer0 in 16-bit timer/counter mode

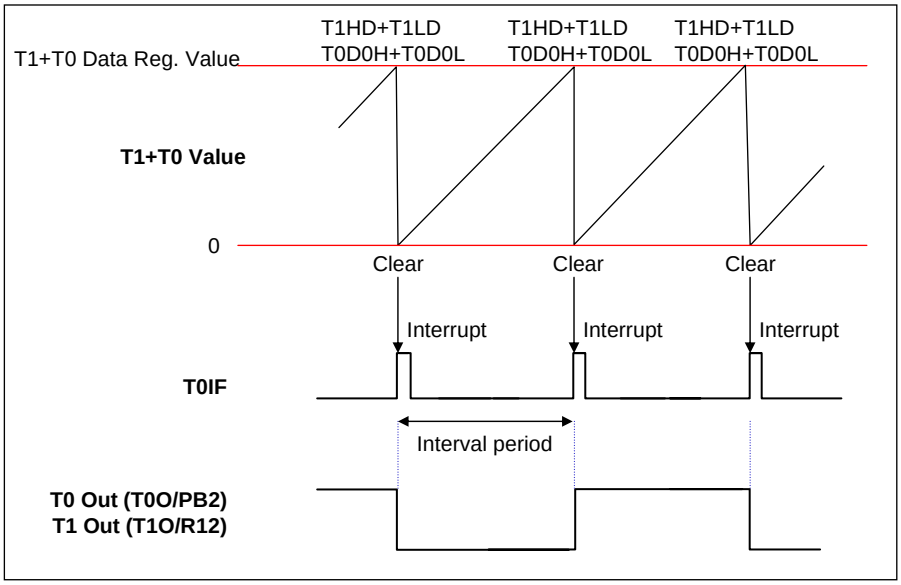


Fig. 4.21 Operation of Timer1+Timer0 in 16-bit timer/counter mode

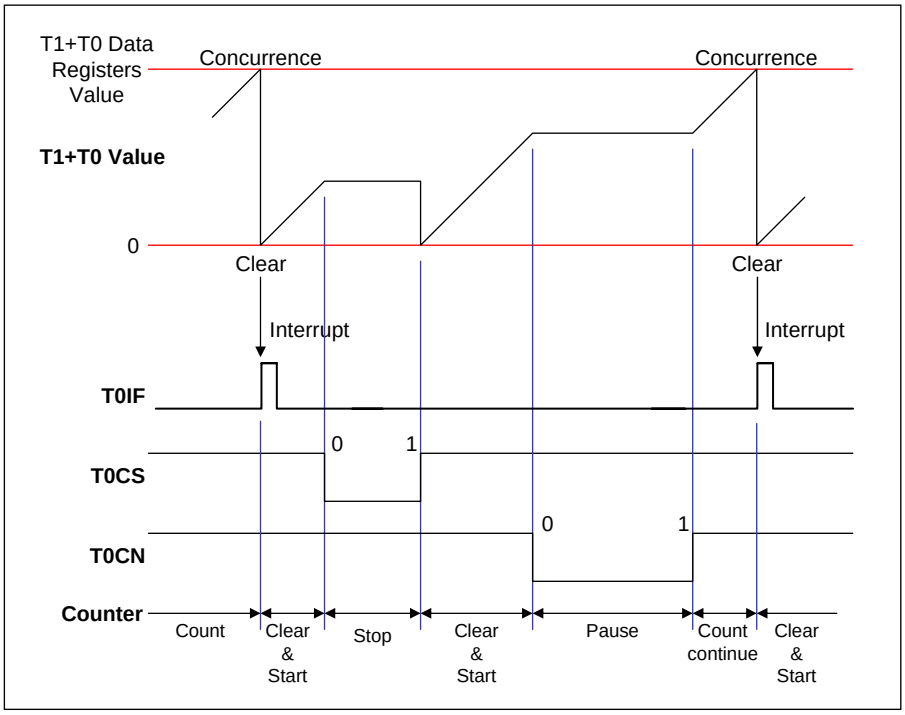


Fig. 4.22 Start / Stop operation of Timer1+Timer0 in 16-bit timer/counter mode

4.3.4. Function of 8-bit Capture Mode

freq = 4MHz

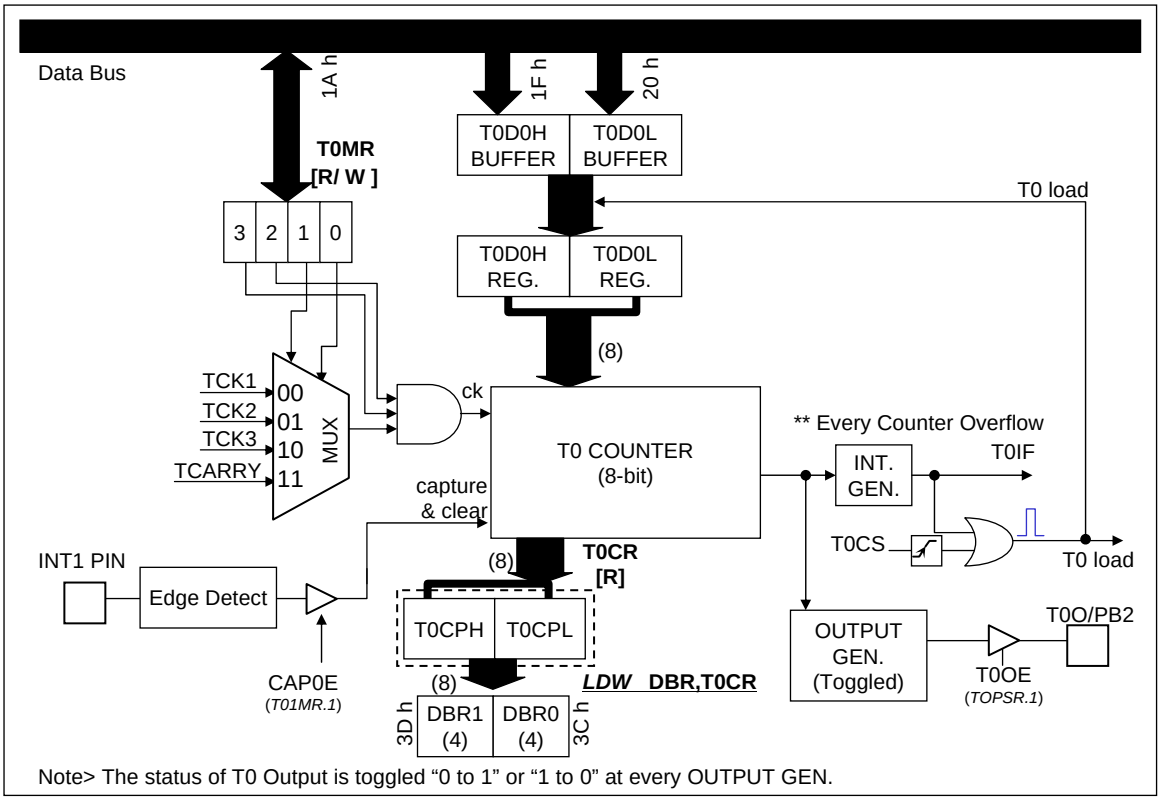
8bit Timer (Timer0)		8bit Timer (Timer1)	
Resolution (CK)	Max. Count	Resolution (CK)	Max. Count
TCK1 : 0. 5 us	128 us	TCK1 : EC	
TCK2 : 1 us	256 us	TCK2 : 1 us	256 us
TCK3 : 2 us	512 us	TCK3 : 2 us	512 us
TCARRY(*)		TCARRY(*)	

(*) Resolution & Max. count of TCARRY clock is decided by output of Carrier Generator

4.3.4.1. Timer0 in 8-bit Capture mode

If CAP0E of T01MR is set to “1”, TIMER0 operates as a 8-bit Capture Timer with 8bit data register (T0D0H+T0D0L). This counting function is same with normal 8-bit timer/counter mode except Timer0 interrupt (T0IF) is occurred at every counter overflow. This timer interrupt(T0IF) in capture is very useful when the pulse width of captured signal is more wider than the maximum period of Timer. Internal clock (TCK) and the output of Carrier Generator (TCARRY) is used as counter clock. External Interrupt 1(INT1/PB0 or PG2) is used as capture input signal. INT1 has three transition modes: “falling edge”, “rising edge”, “both edge” which are selected by interrupt edge selection register IEDS (Refer to External interrupt section.)

The counter execution is controlled by T0CS, T0CN of T0MR and CAP0E of T01MR.
In capture mode, a edge transition at external input(INT1) pin causes the current value in the Timer0 counter, to be captured into registers T0CPx(T0CPH, T0CPL). After capture, Timer0 counter is cleared and restarts by hardware. The T0CPx and T0CRx(T0 counter register; T0CRH, T0CRL) are in same address. In capture mode, reading operation is read the T0CPx, not T0CRx because path is opened to the T0CPx. The value of Capture Data can be read by instruction (***LDW DBR,T0CR***).



Note> The status of T0 Output is toggled “0 to 1” or “1 to 0” at every OUTPUT GEN.

Fig. 4.23 Block Diagram of Timer0 in 8-bit capture mode

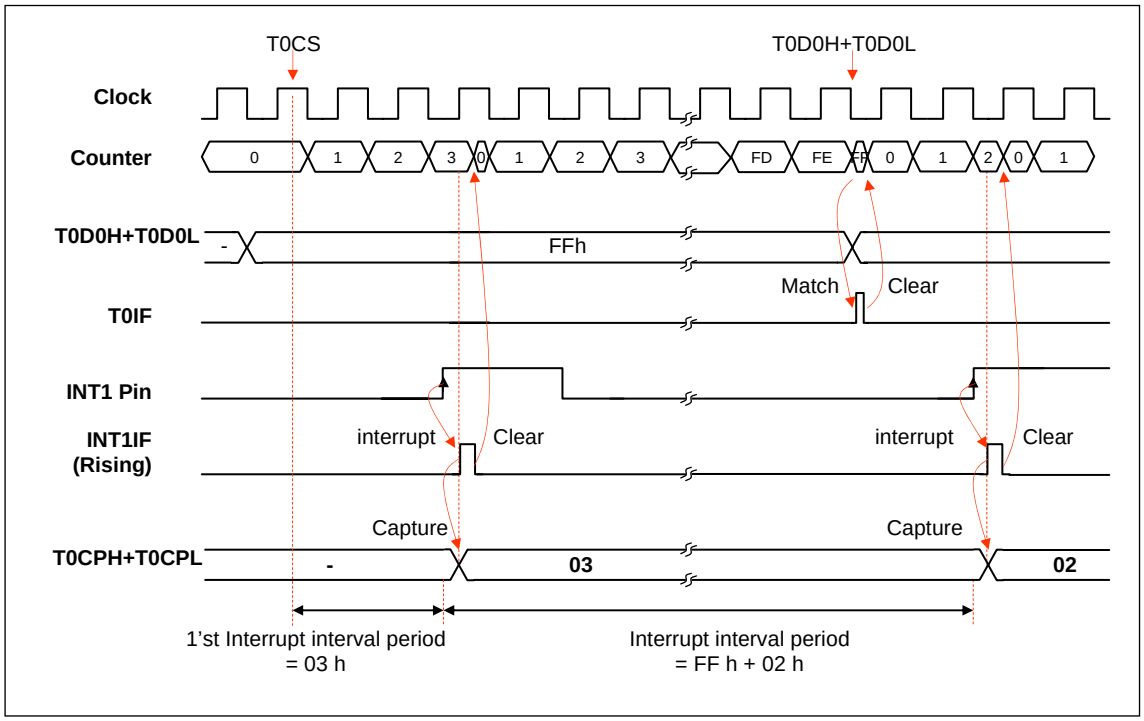


Fig. 4.24 Timing Chart of Timer0 in 8-bit capture mode

4.3.4.2. Timer1 in 8-bit Capture mode

If CAP1E of T01MR is set to "1", TIMER1 operates as a 8-bit Capture Timer with 8bit data register (T1HD+T1LD). This counting function is same with normal 8-bit timer/counter mode. This timer interrupt(T1IF) in capture is very useful when the pulse width of captured signal is more wider than the maximum period of Timer. External Clock (EC), Internal clock (TCK) and the output of Carrier Generator (TCARRY) is used as counter clock. External Interrupt 2(INT2/PG1) is used as capture input signal. INT2 has three transition modes: "falling edge", "rising edge", "both edge" which are selected by interrupt edge selection register IEDS (Refer to External interrupt section.)

The counter execution is controlled by T1CS, T1CN of T1MR and CAP1E of T01MR.
In capture mode, a edge transition at external input(INT2) pin causes the current value in the Timer1 counter, to be captured into registers T1CPx(T1CPH, T1CPL). After capture, Timer1 counter is cleared and restarts by hardware. The T1CPx and T1CRx(T1 counter register; T1CRH, T1CRL) are in same address. In capture mode, reading operation is read the T1CPx, not T1CRx because path is opened to the T1CPx. The value of Capture Data can be read by instruction (***LDW DBR,T1CR***).

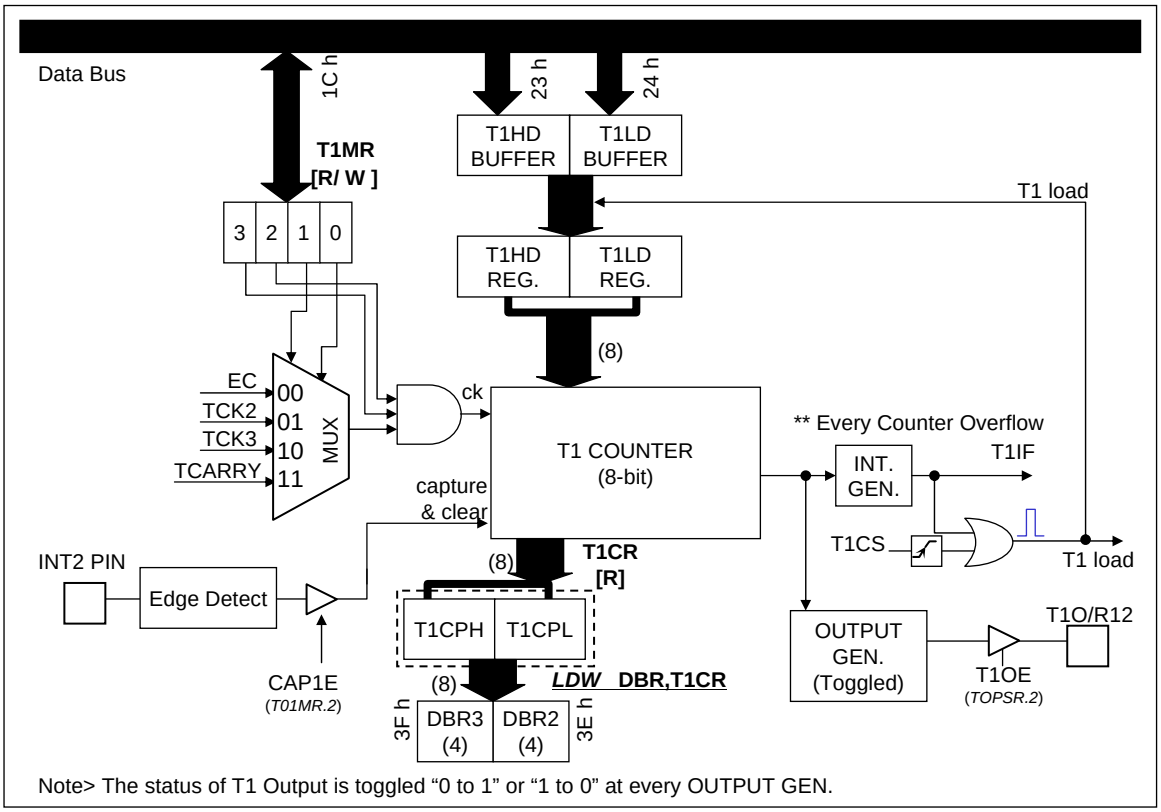


Fig. 4.25 Block Diagram of Timer1 in 8-bit capture mode

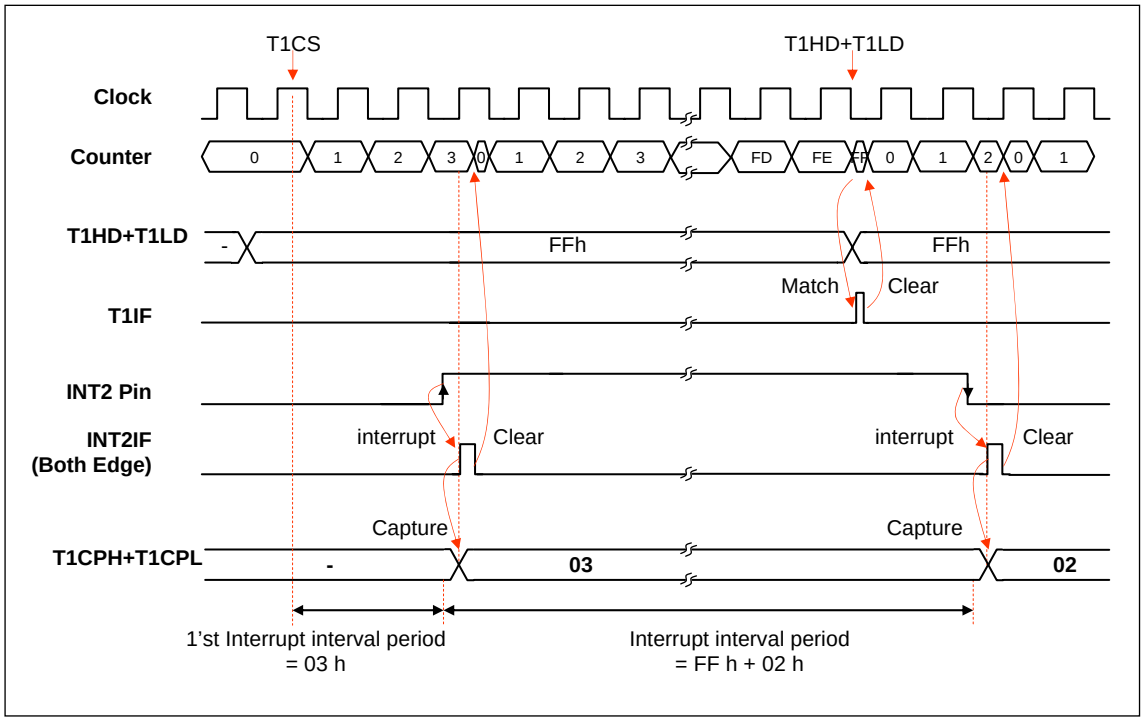
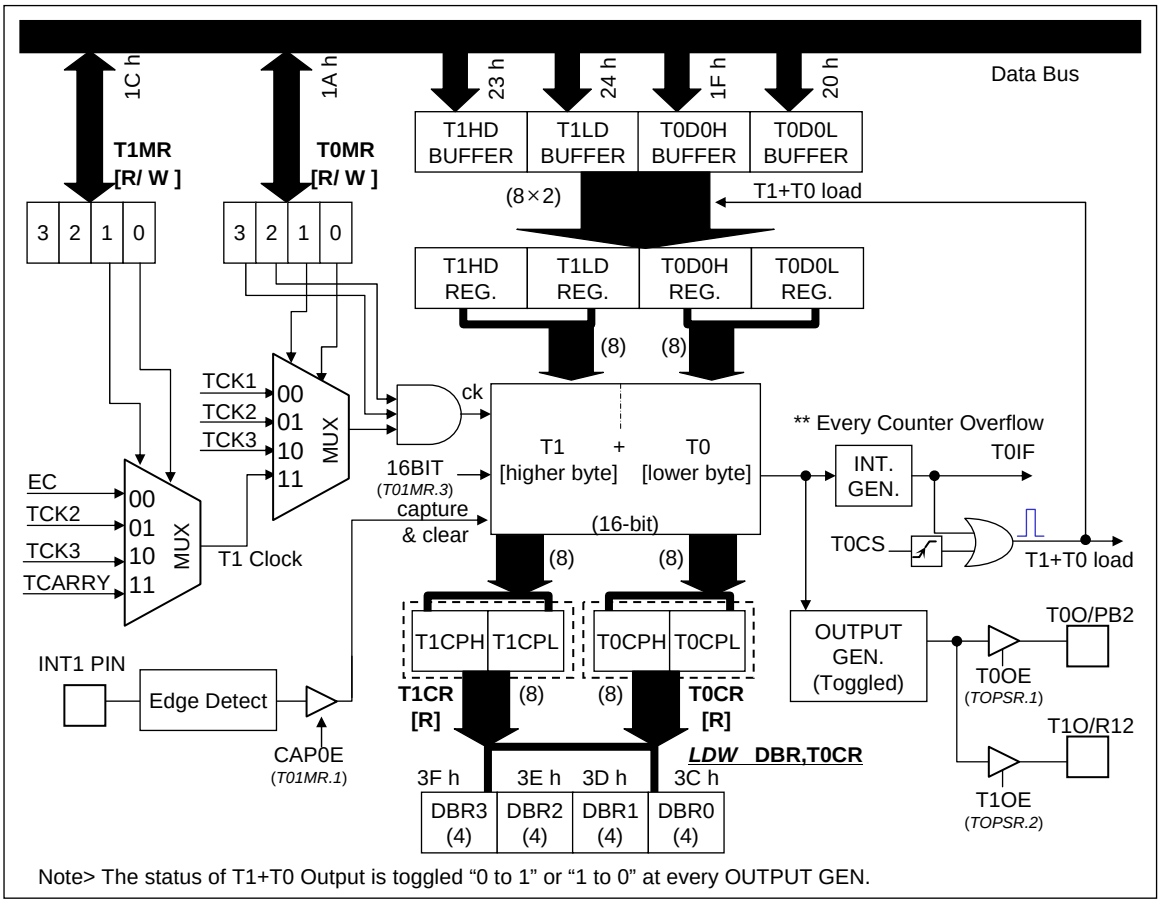


Fig. 4.26 Timing Chart of Timer1 in 8-bit capture mode

4.3.4.3. 16-bit Capture mode (Timer1+Timer0)

If CAP0E of T01MR is set to “1”, TIMER1+TIMER0 operates as a 16-bit Capture Timer with 16bit data register (T1HD+T1LD+T0D0H+T0D0L). This counting function is same with normal 16-bit timer/counter mode. This timer interrupt(T0IF) in capture is very useful when the pulse width of captured signal is more wider than the maximum period of Timer. External clock (EC), Internal clock (TCK) and the output of Carrier Generator (TCARRY) is used as counter clock. External Interrupt 1(INT1/PB0 or PG1) is used as capture input signal. INT1 has three transition modes: “falling edge”, “rising edge”, “both edge” which are selected by interrupt edge selection register IEDS (Refer to External interrupt section.)

The counter execution is controlled by T0CS, T0CN of T0MR and 16BIT, CAP0E of T01MR.
In capture mode, a edge transition at external input(INT1) pin causes the current value in the Timer0+Timer1 counter, to be captured into registers T0CPx+T1CPx. After capture, Timer1+Timer0 counter is cleared and restarts by hardware. The value of Capture Data(16-bit) can be read by instruction (***LDW DBR,T0CR***).



Note> The status of T1+T0 Output is toggled “0 to 1” or “1 to 0” at every OUTPUT GEN.

Fig. 4.27 Block Diagram of Timer1+Timer0 in 16-bit capture mode

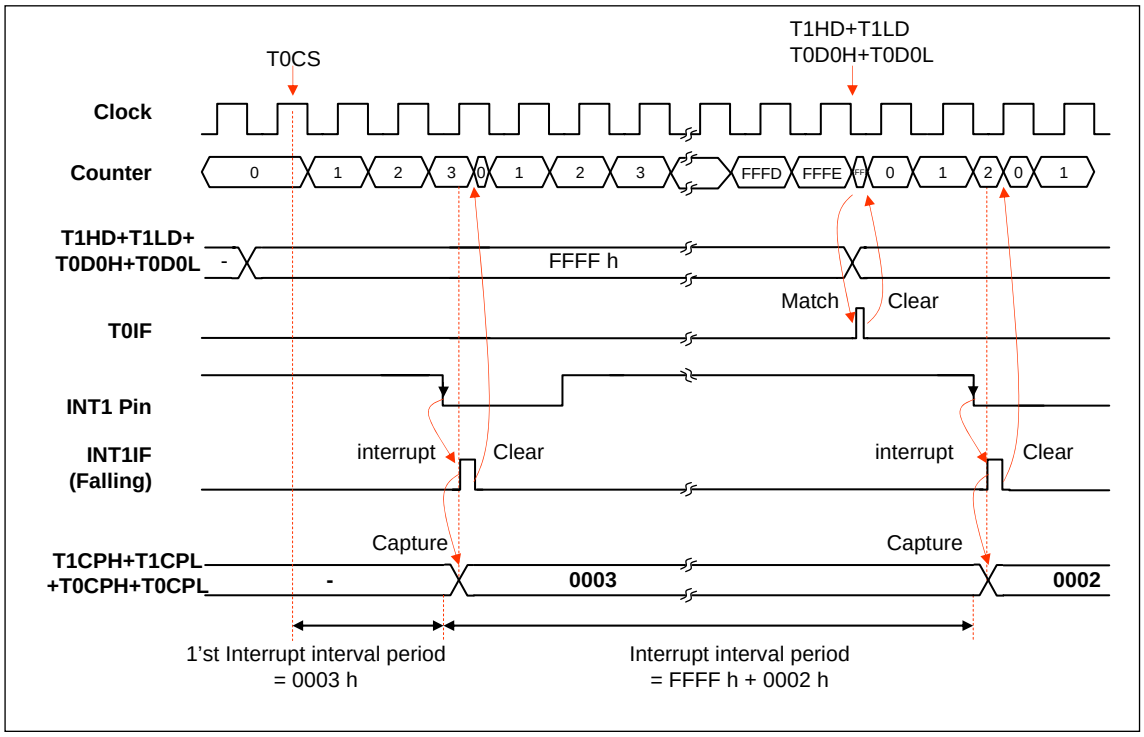


Fig. 4.28 Timing Chart of Timer1+Timer0 in 16-bit capture mode

4.3.5. Function of 8-bit PWM Mode

The ADAM42X11XX has two PWM (Pulse Width Modulation) outputs, one is Timer0 output (T0O/PB2) and the other is Carrier Generator output(PWM/PG0). Basically, Timer0 and Carrier Generator make the PWM functions without additional mode setting, because they have the Data L Registers(T0D0H+T0D0L, CGLMD+CGLLD) and the Data H Registers(T0D1H+T0D1L, CGHMD+CGHLD). The low pulse width of the PWM output determined by the Data L Registers, and the high pulse width of the PWM output determined by the Data H Registers. The period of the PWM output is the sum of the Data L Registers value and the Data H Registers value.

PWM Period = Low pulse width + High pulse width

	Timer0	Carrier Generator
Low pulse width	(T0D0H,T0D0L) x Source Clock	(CGLMD,CGLLD) x Source Clock
High pulse width	(T0D1H,T0D1L) x Source Clock	(CGHMD,CGHLD) x Source Clock

When main frequency is 4MHz, maximum PWM frequency is shown as below Table.

freq = 4MHz

Source Clock		Pulse Width Range		Duty ratio	Max. PWM Frequency
		Low	High		
Timer 0	**TCK1 (00) : 0.5us**	01h ~ FFh	01h ~ FFh	1/256 ~ 255/256	7.8125 kHz
	TCK2 (01) : 1.0us	↑	↑	↑	3.9063 kHz
	TCK3 (10) : 2.0us	↑	↑	↑	1.9531 kHz
	TCARRY (11) : 256us	↑	↑	↑	0.0153 kHz
Carrier Generator	**TCK1 (00) : 0.5us**	↑	↑	↑	7.8125 kHz
	TCK2 (01) : 1.0us	↑	↑	↑	3.9063 kHz
	TCK3 (10) : 2.0us	↑	↑	↑	1.9531 kHz
	TCK4 (11) : 4.0us	↑	↑	↑	0.9766 kHz

* TCARRY clock is decided by output of Carrier Generator

5. INTERRUPT

The ADAM42X11XX contains 7 interrupt sources; 2 externals and 5 internals.
Nested interrupt services with priority control is also possible.

- 7 interrupt source (2Ext, 3Timer, 1 A/D, 1LVI)
- 7 interrupt vector
- 7 level nested interrupt control is possible.
- Read of interrupt request flag are possible.
- In interrupt accept, request flag is automatically cleared.

Interrupt Enable Register (IENR, IENR2), Interrupt Request Register (IRQR, IRQR2) and priority circuit.
Interrupt function block diagram is shown in Fig. 5.1

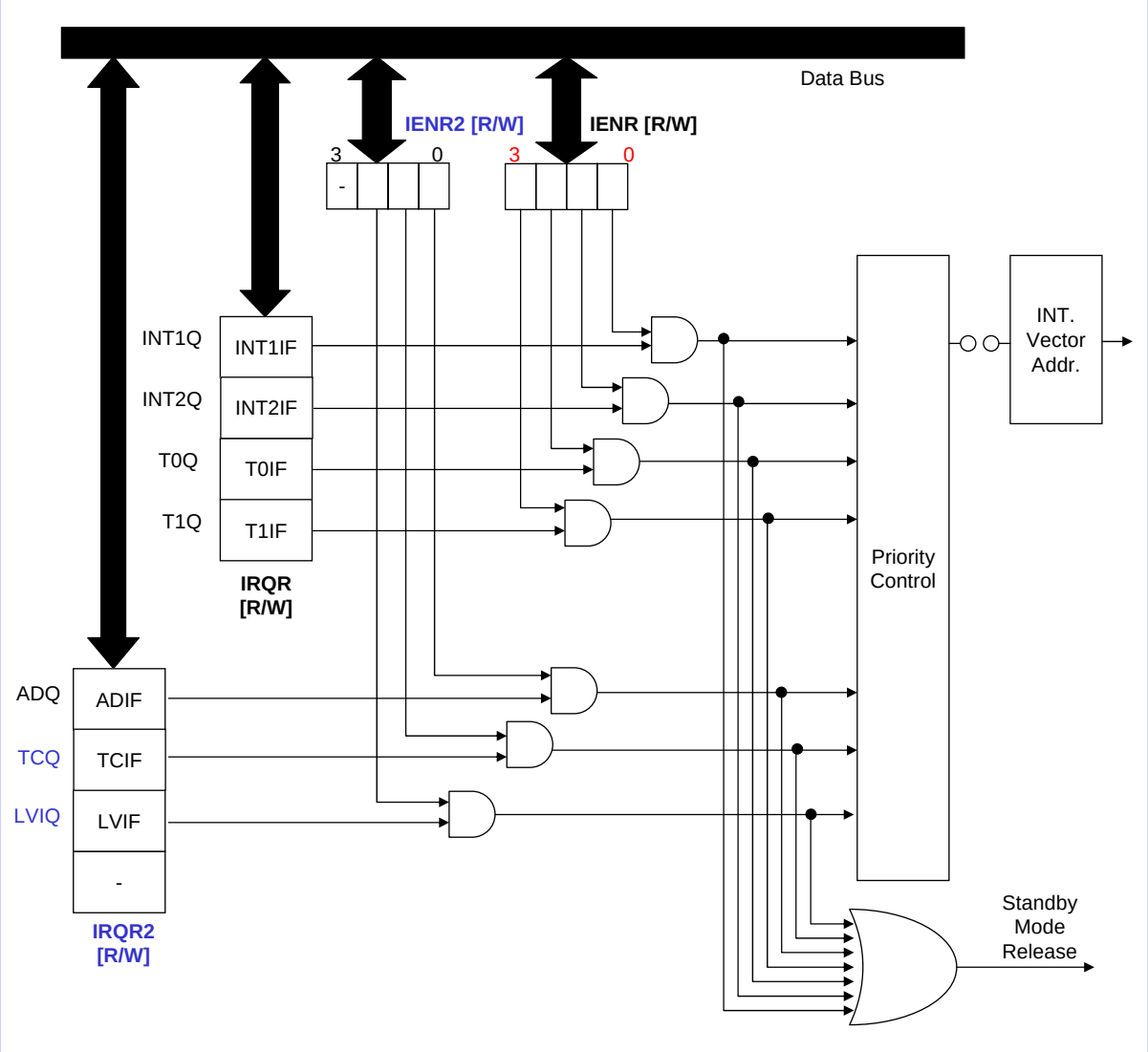


Fig. 5.1 Interrupt Source

5. INTERRUPT

5.1. Interrupt Source

Each interrupt vector is independent and has its own priority.

	Mask	Priority	Interrupt Source	INT Vector Addr.
Hardware Interrupt	Non-maskable	-	Reset	0000H
	maskable	1	INT1Q (External Interrupt1)	0002H
		2	INT2Q (External Interrupt2)	0004H
		3	T0Q (Timer0)	0006H
		4	T1Q (Timer1)	0008H
		5	ADQ (A/D)	000AH
		6	TCQ (Carrier Generator)	000CH
		7	LVIQ (Low Voltage Indicator)	000EH

Table 5.1 Interrupt Source

5.2. Interrupt Control Register

I flag of SFR is a interrupt mask enable flag. When I flag = ``0``, all interrupts become disable. When I flag = ``1``, interrupts can be selectively enabled and disabled by contents of corresponding Interrupt Enable Register(IENR).
When interrupt is occurred, interrupt request flag is set,and Interrupt request is detected at the edge of interrupt signal. The accepted interrupt request flag is automatically cleared during interrupt cycle process. The interrupt request flag maintains ``1`` until the interrupt is accepted or is cleared in program. In reset state, interrupt request flag register (IRQR) is cleared to ``0``. It is possible to read the state of interrupt register and to manipulate the contents of register.

External Interrupt Edge selection Register [IEDS]

bit	3	2	1	0	
IEDS	IED2H	IED2L	IED1H	IED1L	*17h*
Initial value	0	0	0	0	
R/W	W	W	W	W	
	INT2		INT1		

IEDH & IEDL	00	-
	01	Falling Edge Selection (1-to-0 transition)
	10	Rising Edge Selection (0-to-1 transition)
	11	Both Edge Selection (Falling & Rising)

5. INTERRUPT

Interrupt Enable Register

bit	3	2	1	0	
IENR	T1E	T0E	INT2E	INT1E	*18h*
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

T1E	Timer1 interrupt Enable bit
T0E	Timer0 interrupt Enable bit
INT2E	Ext. Interrupt-2 Enable bit
INT1E	Ext. Interrupt-1 Enable bit

Interrupt Enable Register 2

bit	3	2	1	0	
IENR2	-	LVIE	TCE	ADE	*16 h*
Initial value	0	0	0	0	
R/W	R	R/W	R/W	R/W	

-	-
LVIE	LVI Interrupt Enable bit
TCE	Carrier Generator Interrupt Enable bit
ADE	A/D Interrupt Enable bit

Interrupt Request Flag Register

bit	3	2	1	0	
IRQR	T1IF	T0IF	INT2IF	INT1IF	*19h*
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

T1IF	Timer1 interrupt Request Flag bit
T0IF	Timer0 interrupt Request Flag bit
INT2IF	Ext. Interrupt-2 Request Flag bit
INT1IF	Ext. Interrupt-1 Request Flag bit

Interrupt Request Flag Register 2

bit	3	2	1	0	
IRQR2	-	LVIF	TCIF	ADIF	*15 h*
Initial value	0	0	0	0	
R/W	R	R/W	R/W	R/W	

-	-
LVIIF	LVI Interrupt Request Flag bit
TCIF	Carrier Generator Interrupt Request Flag bit
ADIF	A/D Interrupt Request Flag bit

5.2.1. Interrupt Timing

Interrupt Request Sampling Time

Maximum 2 machine cycle (When execute LDW @ABR Instruction)
Minimum 0 machine cycle

Interrupt preprocess step is 1 machine cycle

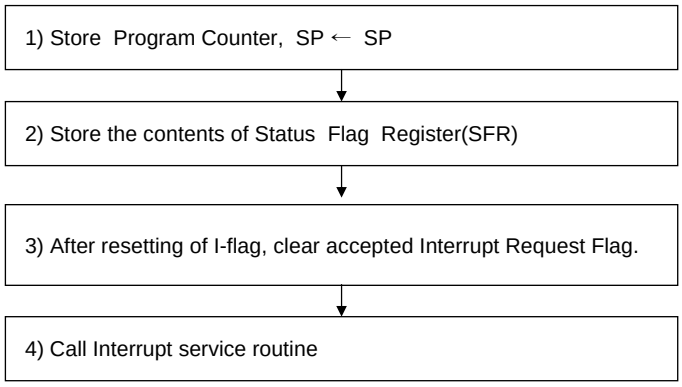
5.2.2. The valid timing after executing Interrupt control instructions

I flag is valid just after executing of EI/DI on the contrary.

5.3. Interrupt Processing Sequence

When an interrupt is accepted, the on-going process is stopped and the interrupt service routine is executed. After the interrupt service routine is completed it is necessary to restore everything to the state before the interrupt occurred.
As soon as an interrupt is accepted, the content of the program counter is saves in the stack register and the contents of status flag register (SFR) is saved on the interrupt stack register (INTSK) which is 7 level stack area.
At the same time, the content of the vector address corresponding to the accepted interrupt, which is in the interrupt vector table, enters into the program counter and interrupt service is executed. In order to execute the interrupt service routine, it is necessary to write the jump addresses in the vector table (0002 h ~ 000E h) corresponding to each interrupt.

Interrupt Processing Step



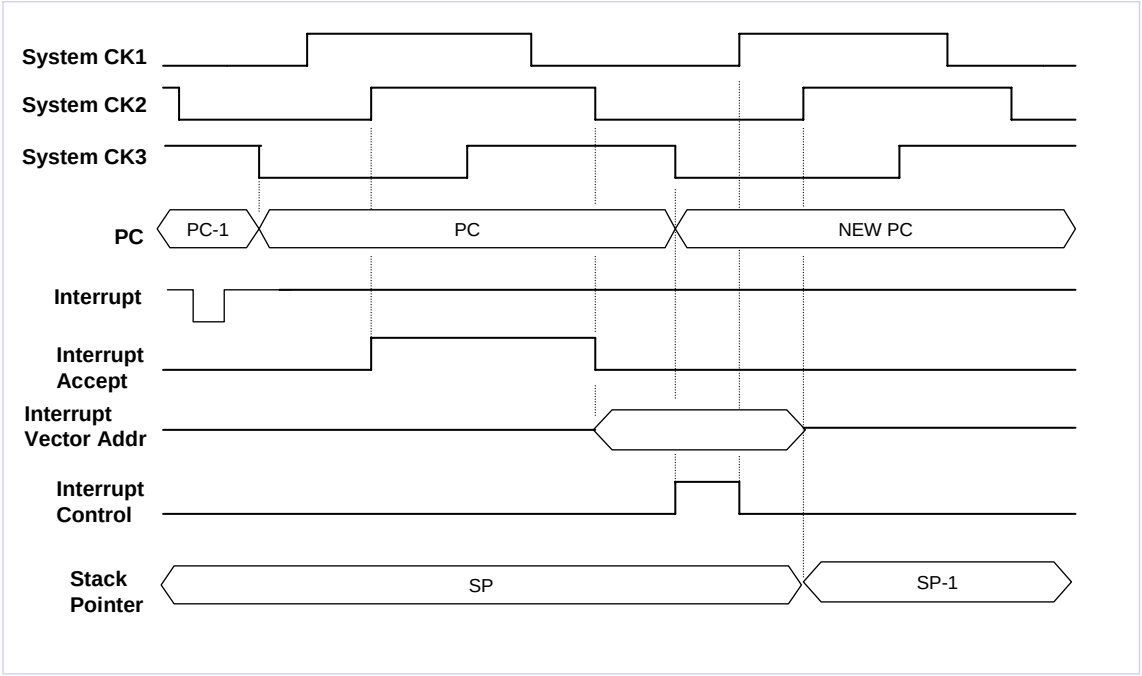


Fig. 5.2. Interrupt Processing Step Timing

5.4. Multiple Interrupt

If there is an interrupt, Interrupt Mask Enable Flag is automatically cleared before entering the Interrupt Service Routine. After then, no interrupt is accepted. If EI instruction is executed, interrupt mask enable bit becomes ``1``, and each enable bit can accept interrupt request.
When two or more interrupts are generated simultaneously, the highest priority interrupt is accepted.

6. ANALOG TO DIGITAL CONVERTER

The analog-to-digital (A/D) converter module has eight inputs.
The analog-to-digital (A/D) converter allows conversion of an analog input signal to a corresponding 12-bit digital number.The A/D module has 8 analog inputs, which are multiplexed into one sample.
The output of sample is the input into converter , which generates the result via successive approximation.
The analog reference voltages are software selectable to VDD or AVREF by setting AVREFS bit of ADCIS register.

The A/D module has six register. These registers are
- A/D CONTROL MODE REG.(ADCM)
- A/D CONVERTER INPUT SELECTION REG.(ADCIS)
- A/D CONVERTER DATA REG1.(ADCR1)
- A/D CONVERTER DATA REG2.(ADCR2)
- A/D CONVERTER DATA REG3.(ADCR3)
- WDT & ADC CONTROL REG.(WACR)

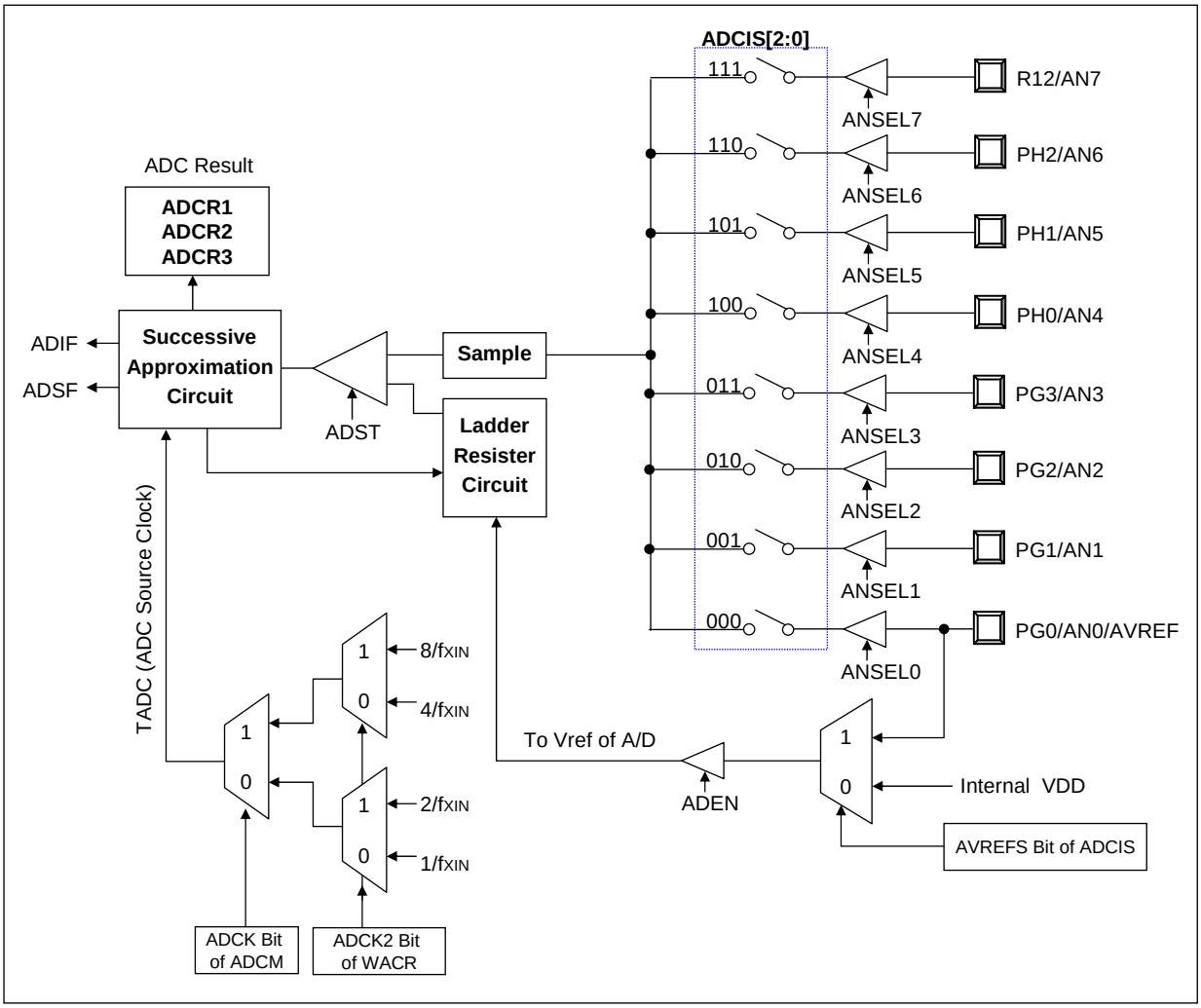


Fig. 6.1 12Bit-A/D Converter Block Diagram

6. ANALOG TO DIGITAL CONVERTER

6.1. A/D Converter Registers

6.1.1. A/D Converter Input Selection

bit	3	2	1	0	
ADCIS	AVREFS	ADS2	ADS1	ADS0	*33h*
Initial value	0	0	0	0	
R/W	W	W	W	W	

AVREFS	0	VDD for A/D
	1	AVREF for A/D
ADS2 & ADS0	000	Channel 0 (PG0/AN0)
	001	Channel 1 (PG1/AN1)
	010	Channel 2 (PG2/AN2)
	011	Channel 3 (PG3/AN3)
	100	Channel 4 (PH0/AN4)
	101	Channel 5 (PH1/AN5)
	110	Channel 6 (PH2/AN6)
	111	Channel 7 (R12/AN7)

6.1.2. A/D Converter Mode Register

bit	3	2	1	0	
ADCM	ADCK	ADEN	ADST	ADSF	*34h*
Initial value	0	0	0	1	
R/W	R/W	R/W	R/W	R	

ADCK2 & **ADCK**	0**0**	ADC Source Clock is PS0 (TADC= 1/fXIN)
	0**1**	ADC Source Clock is PS2 (TADC= 4/fXIN)
	1**0**	ADC Source Clock is PS1 (TADC= 2/fXIN)
	1**1**	ADC Source Clock is PS3 (TADC= 8/fXIN)
ADEN	0	A/D Conversion is Disable
	1	A/D Conversion is Processing
ADST	0	-
	1	A/D Conversion is Started and cleared to “0” after 1 Cycle
ADSF	0	A/D Conversion is Processing
	1	A/D Conversion is completed

** ADCK2 is bit0 of WDT & ADC Control Reg.(WACR[37h])*

6.1.3. A/D Converter Result Data Register 1, 2, 3

bit	3	2	1	0	
ADCR1	ADCRB3	ADCRB2	ADCRB1	ADCRB0	*35h*
Initial value	x	x	x	x	
R/W	R	R	R	R	

bit	3	2	1	0	
ADCR2	ADCRB7	ADCRB6	ADCRB5	ADCRB4	*36h*
Initial value	x	x	x	x	
R/W	R	R	R	R	

bit	3	2	1	0	
ADCR3	ADCRB11	ADCRB10	ADCRB9	ADCRB8	*37h*
Initial value	x	x	x	x	
R/W	R	R	R	R	

6.1.4. WDT & ADC Control Register

bit	3	2	1	0	
WACR	WDTRST	RWDTEN	RWDTCK	**ADCK2**	*37h*
Initial value	0	0	0	0	
R/W	W	W	W	W	

WDTRST	0	WDT interrupt enable, when WDT Overflow is occurred in RCWDT Mode. (default)
	1	System Reset enable, when WDT Overflow is occurred in RCWDT Mode.
RWDTEN	0	RCWDT mode disable
	1	RCWDT Oscillator Enable & RCWDT mode enable
RWDTCK	0	WDT Input Clock selects 64us (typ. : VDD=5.0V, T=25℃)
	1	WDT Input Clock selects 16us (typ. : VDD=5.0V, T=25℃)
ADCK2 & ADCK	**0**0	ADC Source Clock is PS0 (TADC= 1/fXIN)
	01	ADC Source Clock is PS2 (TADC= 4/fXIN)
	10	ADC Source Clock is PS1 (TADC= 2/fXIN)
	11	ADC Source Clock is PS3 (TADC= 8/fXIN)

6.2. A/D Converter Caution

6.2.1. Noise Countermeasures of AN0~AN7

It is recommend that a capacitor be connected externally as shown Fig 6.2 in order to reduce noise.

Because the ADC does not use sample-and-hold circuitry, it is important that any fluctuations in the analog level at the AN0 to AN7 input pins during a conversion procedure be kept to an absolute minimum. Any change in the input level, perhaps due to circuit noise, will invalidate the result.

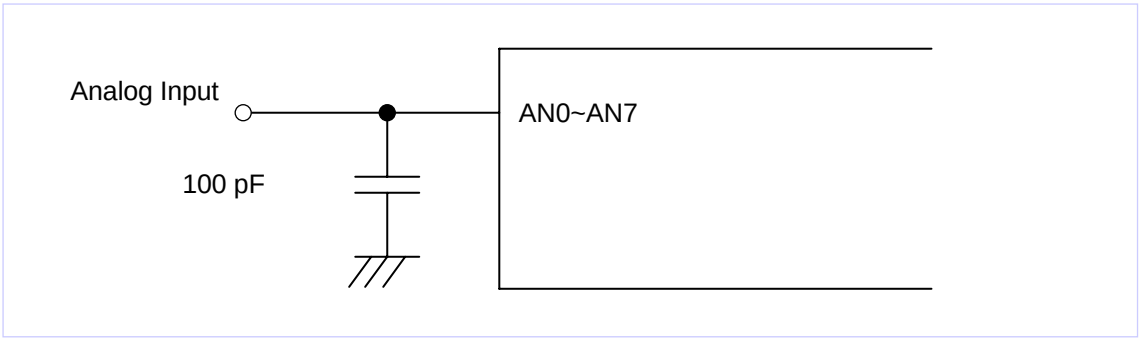


Fig. 6.2. Analog input pin Connecting capacitor

6.2.2. AVREF pin input impedance

A series resistor string of approximately 100kΩ~150kΩ is connected between AVREF pin and GND.

If the output impedance of AVREF is high, it will result in parallel connection to the series resistor between AVREF pin and GND, and there will be a large reference voltage error.

6.3. A/D Converter Operation

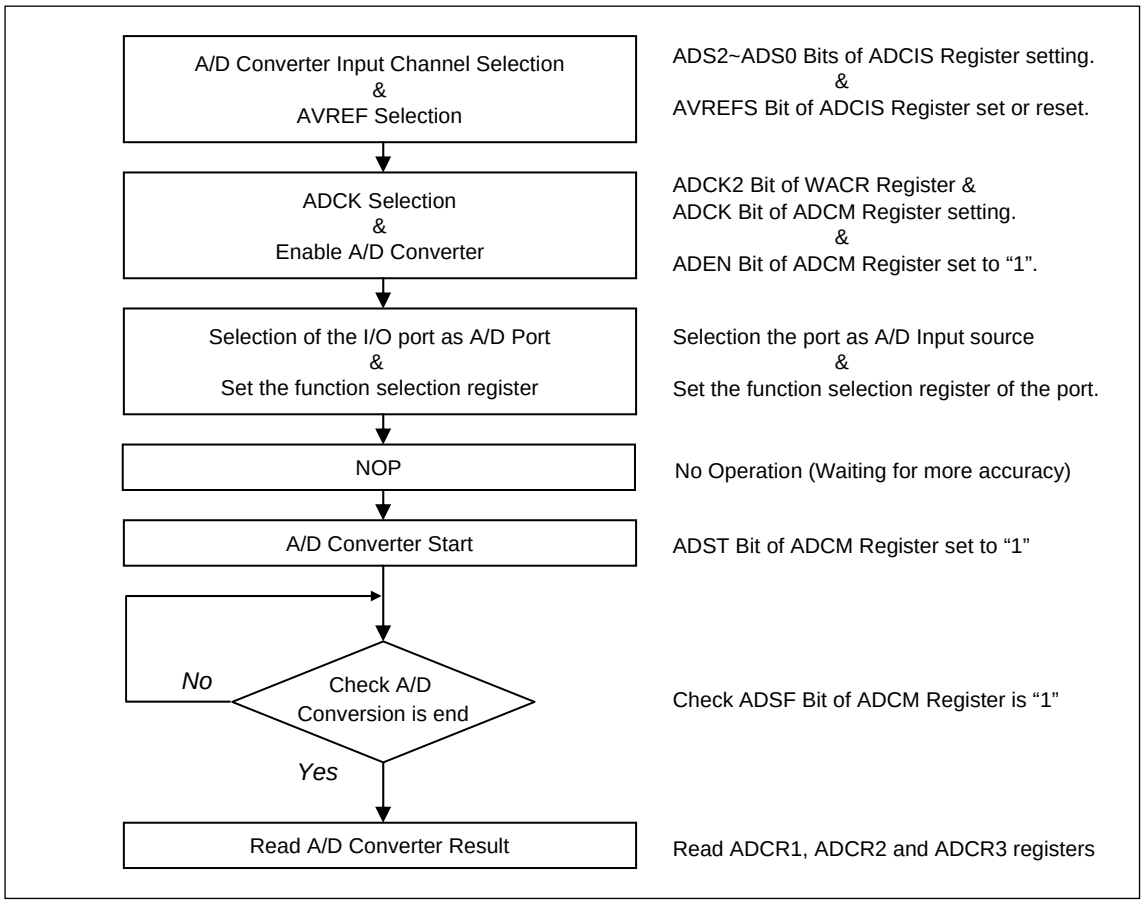


Fig. 6.3. A/D Converter Operation Flow

Remember to read the contents of ADCR1, ADCR2 and ADCR3 before another conversion starts. Otherwise, the previous result will be overwritten by the next conversion result.
The A/D conversion process requires total 116 TADC(ADC Source Clock).

▶ Setup time (= 16 TADC) + Conversion time (=12 bits x 8 TADC = 96 TADC) + Hold time (= 4 TADC)

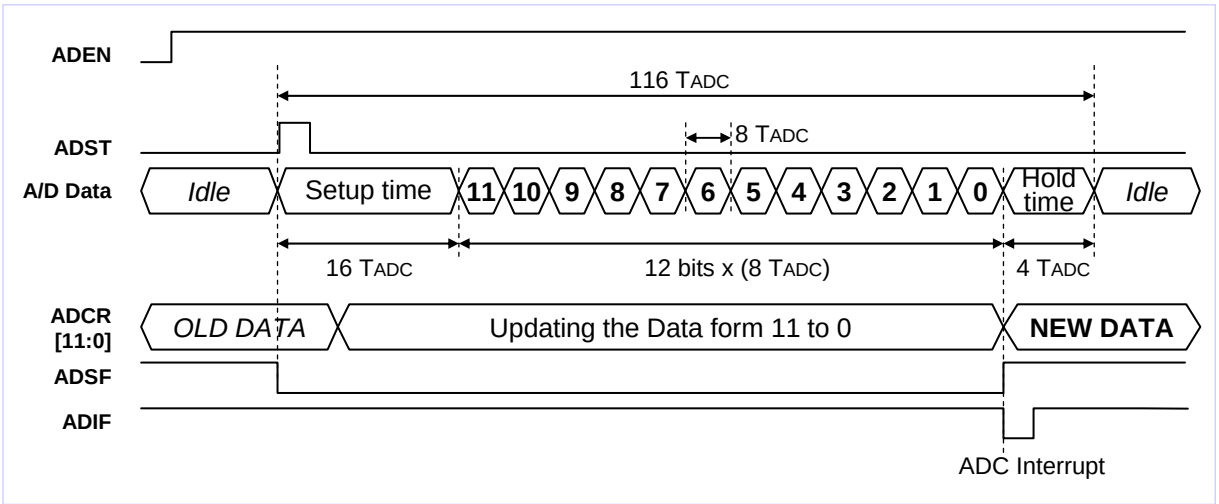


Fig. 6.4. ADC Conversion Timing

For minimum power dissipation, after the Hold time, conversion clock is stopped and ADC is in idle, but conversion data hold.
Be careful not to do restarting the ADC for the Hold time(=4 TADC). Otherwise, ADC operates abnormally.

7. POWER-DOWN FUNCTION

In power-down mode, power consumption is reduced considerably that in battery operation battery life time can be extended a lot. For applications where power consumption is a critical factor, ADAM42X11XX provides two kinds of power-down functions, STOP mode and SLEEP mode. In this 2 Modes, program processing is stopped.

7.1. Stop Mode

STOP mode can be entered by STOP instruction during program.
In STOP mode, oscillator is stopped to make all clocks stop, which leads to less power consumption. All registers and RAM data are preserved.
˝NOP˝ instruction should be follows STOP instruction for pre-charge time of Data Bus line.

ex) STOP : STOP instruction execution
NOP : NOP instruction

Additionally, if it's executed the STOP instruction after setting the bit RCWDTEN of WACR to "1", the Internal RC-Oscillated Watchdog Timer mode is activated. In the Internal RC-Oscillated Watchdog Timer mode, STOP mode is also released by occurring of WDT Time-out. (Ring-OSC period * 2^{18})

The Ring-OSC oscillation period is vary with temperature, VDD and process variations from part to part. According to the bit RCWDTCK of WACR, the RCWDT oscillated watchdog timer time-out is shown below.

The bit RCWDTCK of WACR	WDT Time-out (Typ.)
0	16.8s
1	4.2s

˝ NOP˝ instruction should be follows STOP instruction for pre-charge time of Data Bus line.

```
ex)   LRI    WACR, #0100b   : set the bit of RCWDTEN
      WDTC                  : WDT clear
      STOP                  : STOP instruction execution
      NOP                   : NOP instruction
```

7.1.1. Stop Mode Release

Release of STOP mode is executed by Power on reset , Key input Port(one of R1, PB, PG) which is selected by R1ST, PBST and PGST register for stop release is Low , external interrupt and Low voltage detection (LVD) mode release .
When there is a release signal of STOP mode, the instruction execution starts after stabilization oscillation time.($2^{14} \times 4/f_{OSC}$ = 16.384ms at f_{OSC} = 4.0MHz)

Release Factor	Release Method	Release Time
Power on Reset	By Power on reset, Stop mode is release and system is initialized.	38ms + $57 \times 2^{10} \times 4/f_{OSC}$ = 96.6ms at f_{OSC} = 4.0MHz (Option read time : about 38ms)
Release from LVD detection	Stop mode is release when release from LVD detection.	
R1, PB, PG Port (key input)	Stop mode is released by Low input of selected pin by R1ST, PBST and PGST register.	$2^{14} \times 4/f_{OSC}$ = 16.384ms at f_{OSC} = 4.0MHz
External interrupt	Stop mode is release external interrupt input.	
WDT Overflow	Stop mode is release by reset or interrupt of WDT. (in RCWDT Mode only)	
External Reset	Stop mode is release external $\overline{\text{RESET}}$ pin.	Ext. reset pulse width. (longer than 100us)

7. POWER-DOWN FUNCTION

7.2. Sleep Mode

SLEEP mode can be entered by SLEEP instruction during program.
In SLEEP mode, basically CPU and ROM halts while oscillation and peripherals are operate.
˝NOP˝ instruction should be follows SLEEP instruction for pre-charge time of Data Bus line.

ex) SLEEP : SLEEP instruction execution
NOP : NOP instruction

7.2.1 Sleep Mode Release

Release of SLEEP mode is executed by Power on reset , all interrupts and Low voltage detection (LVD) mode release. To be release by interrupt, interrupt should be enabled before SLEEP mode. This mode don't need the stabilization oscillation time.

Release Factor	Release Method	Release Time
Power on Reset	By Power on reset, Sleep mode is release and system is initialized.	38ms + 57×2^{10}×4/fosc = 96.6ms at fosc = 4.0MHz (Option read time : about 38ms)
Release from LVD detection	Sleep mode is release when release from LVD detection.	
All Interrupts	Sleep mode is released by all Interrupts.	2^5×4/fosc = 32us at fosc = 4.0MHz
External Reset	Sleep mode is release external $\overline{\text{RESET}}$ pin.	Ext. reset pulse width. (longer than 2xTsys)

7.3. Operation States in Stop/Sleep Mode

Internal Circuit	STOP Mode	SLEEP Mode
Oscillator	Stop	Operates continuously
Internal CPU clock	Stop	Stop
Address Bus Data Bus	Retained	Retained
Registers	Retained	Retained
RAM	Retained	Retained
I/O port, Output port	Retained	Retained
ROUT	Stop	Operates continuously
Timer	Stop (Counter clear)	Operates continuously
Watch dog Timer	Stop (only operate in RCWDT mode)	Stop
ADC	Stop	Stop
BUZ	Stop	Operates continuously
RCWDT	Operate continuously (only operate in RCWDT mode)	not operate
LVI	Stop	Operates continuously
Release Method	$\overline{\text{RESET}}$, Power-on-reset, Release from LVD, WDT(RCWDT), Ext. Interrupt, Key-input interrupt.	$\overline{\text{RESET}}$, Power-on-reset, Release from LVD, All Interrupts (except ADC)

Table 7.1 Operation States in Stop Mode and Sleep Mode

8. RESET FUNCTION

8.1. Power on RESET

Power On Reset circuit automatically detects the rise of power voltage
(the rising time should be within 50ms). Until the power voltage reaches a certain voltage level, internal reset signal is maintained at ˝L˝ Level until oscillator is stable.
After power applies, this reset state is maintained for the configuration option reading time (about 38ms at VDD=5.0V) and the oscillation stabilization time. ($4/f_{OSC} \times 57 \times 2^{10}$ = about 58.368ms at 4MHz).

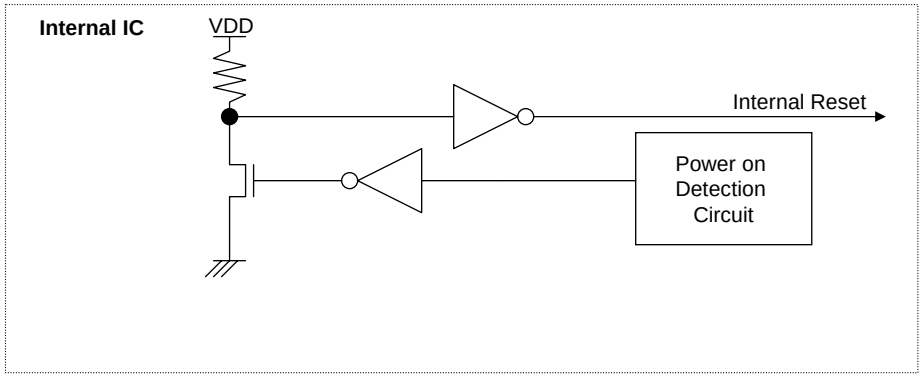


Fig.8.1 Block Diagram of Power On Reset Circuit

* Notice ; When Power On Reset, oscillator stabilization time doesn't include OSC. Start time.

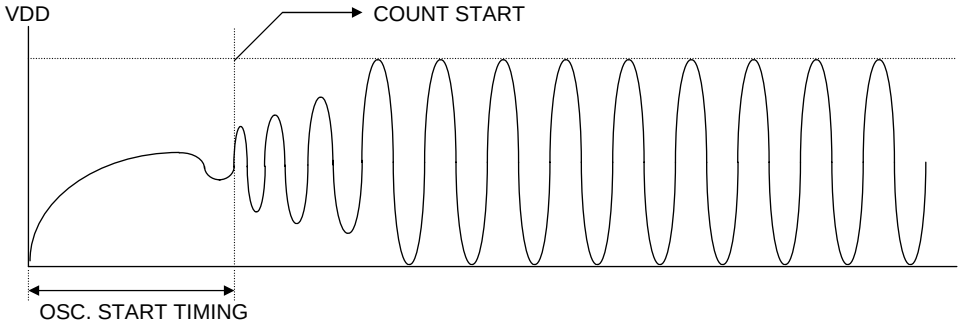


Fig.8.2 Oscillator stabilization diagram

9. LOW VOLTAGE DETECTION MODE

9.1. Low Voltage Detection Condition

An on board voltage comparator checks that V_{DD} is at the required level to ensure correct operation of the device. If V_{DD} is below a certain level,
Low voltage detector forces the device into low voltage detection mode.

9.2. Low Voltage Detection Mode

There is no power consumption except stop current, stop mode release function is disabled.
All I/O ports(R1,PB,PG,PH) are configured as input mode (without pull-up resistor) and Data memory is retained until Voltage through external capacitor is worn out.
But R11 is configured as input mode with pull-up resistor in LVD Mode, when R11 pin is used to RESET function by the Configuration Bits (RSTS).
In this mode, output only port (PC0) is configured open drain “H” output.

9.3. Release of Low Voltage Detection Mode

Reset signal result from new battery (normally 3V) wakes the low voltage detection mode and come into normal reset state. It depends on user whether to execute RAM clear routine or not.

9.4. Low Voltage Detection voltage selection (option)

User can select the voltage of Low Voltage detection voltage level by the Configuration Bits (LVDS). One is high voltage version (typ. 2.2V, if LVDS is “0”),
another is low voltage version (typ. 1.7V, if LVDS is “1”).

9. LOW VOLTAGE DETECTION MODE

9.5. Low Voltage Detection Indicator Register

Low Voltage indication (LVI) are controlled by two registers. It is useful to display the consumption of Batteries.

If VDD power level is low and higher than low voltage detection (LVD) level (refer to Fig 10.1), the bit of VDIR register could be set according to the VDD level sequentially.

The VDD detection levels for Indication are three , that is , VDIR2 (Typ. 2.7V) , VDIR1(Typ. 2.4V) and VDIR0 (Typ. 2.1V) of VDIR register.

9.5.1. Voltage Detection Indicator Enable Register (VDIER)

bit	3	2	1	0	
VDIER	LVIM	VDIER2	VDIER1	VDIER0	*1Bh*
Initial value	0	0	0	0	
R/W	W	W	W	W	

VDIER0	detection level 0 (typ. 2.1V) selection	0	disable
		1	enable
VDIER1	detection level 1 (typ. 2.4V) selection	0	disable
		1	enable
VDIER2	detection level 2 (typ. 2.7V) selection	0	disable
		1	enable
LVIM	LVI Mode Selection	0	System Reset Selection
		1	Interrupt Selection

Voltage Detection Indicator Enable Register (VDIER) is 4-bit register, and can assign Indicator is enable or not.

If VDIER2 ~ VDIER0 is selected as “0”, Voltage detection for Indication function is disabled and if selected as “1”, it is enable. If LVIM is selected as “0” and enable one of VDIER2~VDIER0, when the corresponding voltage detection for Indication is occurred, it makes the system reset. If LVIM is selected as “1”, it makes the LVI interrupt.

VDIER is write-only register and initialized as ``0 h`` in reset state.

In the in-circuit emulator, LVI function is not implemented and user can not experiment with it. Therefore after final development of user program, this function may be experimented or evaluated.

9.5.2. Voltage Detection Indicator Data Register (VDIR)

bit	3	2	1	0	
VDIR	-	VDIR2	VDIR1	VDIR0	*1Bh*
Initial value	0	0	0	0	
R/W	R	R	R	R	

Voltage Detection Indicator Data Register (VDIR) is 3-bit register to store data of low voltage level. VDIR is read only register and initialized as “0h” in reset state.

10. SRAM DATA BACK-UP FUNCTION

10.1. SRAM DATA BACK-UP after Low Voltage Detection

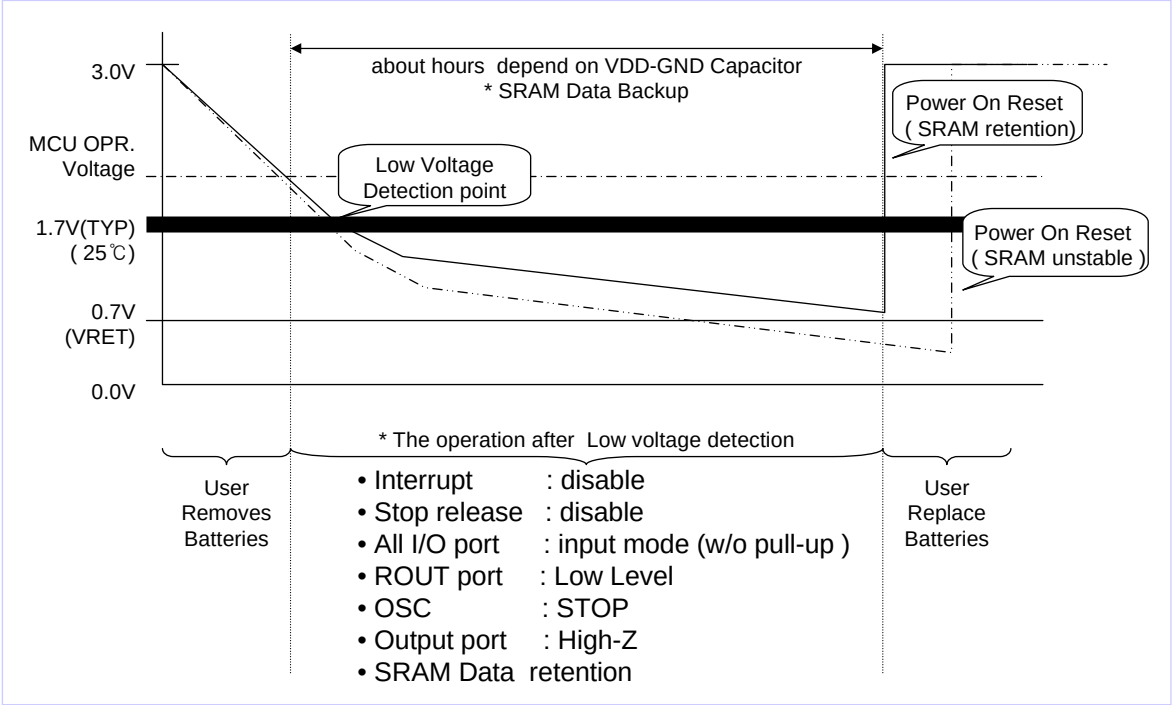


Fig 10.1 Low Voltage Detection and Protection

10.2. S/W flow chart example after Reset using SRAM DATA Back-up

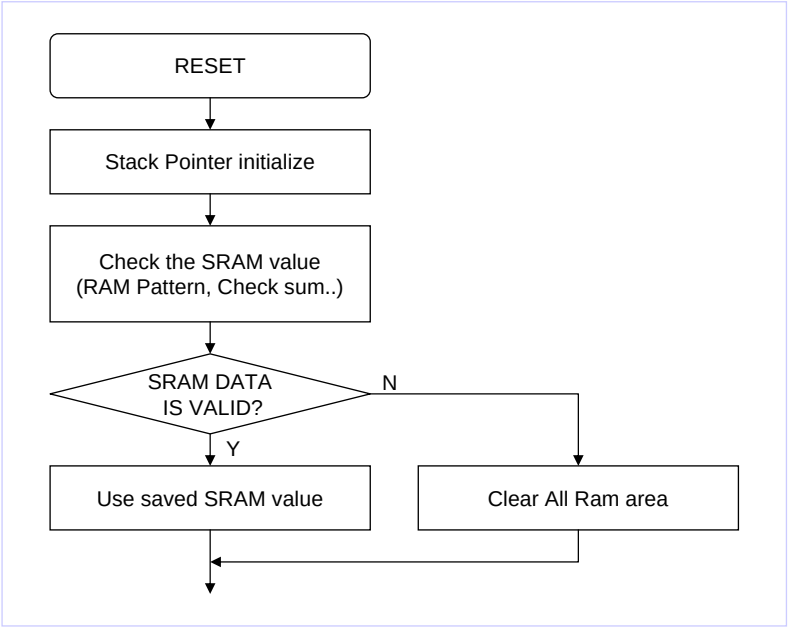
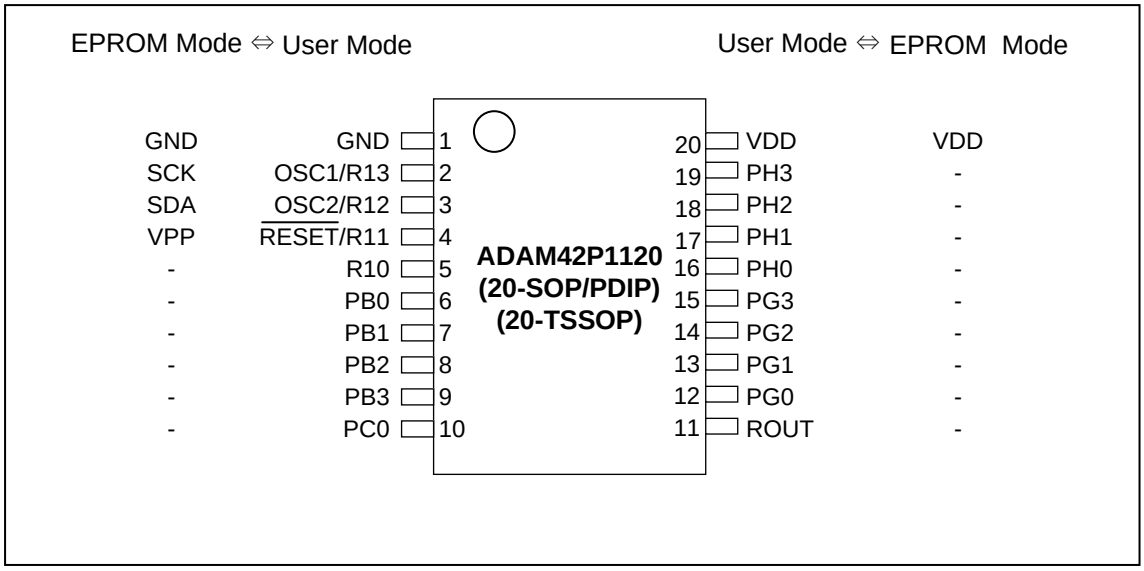


Fig 10.2 S/W Flow Chart Example for SRAM Back-up

11. OTP PROGRAMMING

11.1. ADAM42P1120

11.1.1. PIN Assignment



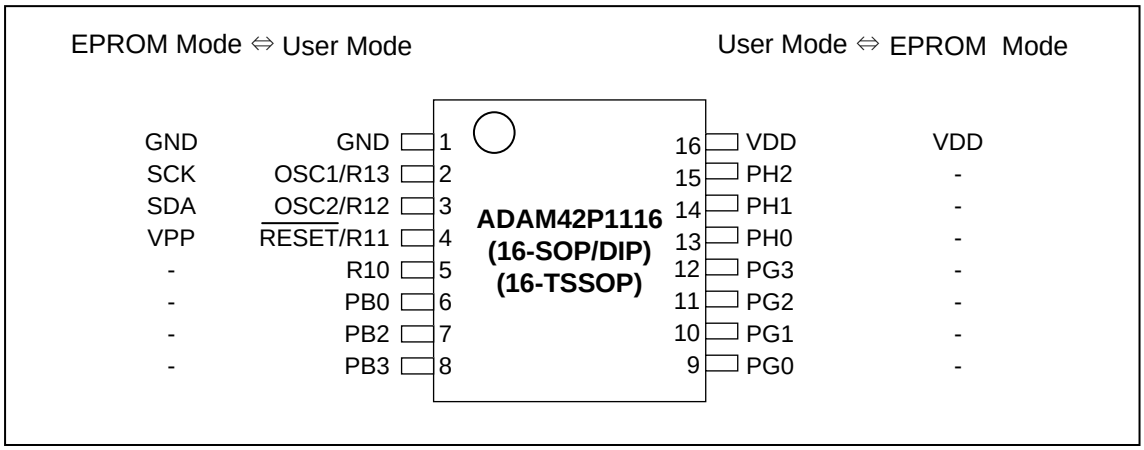
11.1.2. PIN Function

Pin No.	Port Name	User Mode	EPROM Mode
1, 20	GND, VDD	Power	Power
2	OSC1/R13	Clock (Input) or R13(I/O)	SCK (Input)
3	OSC2/R12	Clock (Output) or R12(I/O)	SDA (I/O)
4	$\overline{\text{RESET}}$/R11	$\overline{\text{RESET}}$(Input) or R11 (I/O)	VPP(11.5V)
5	R10	R10 (I/O)	-
6	PB0	PB0 (I/O)	-
7	PB1	PB1 (I/O)	-
8	PB2	PB2 (I/O)	-
9	PB3	PB3 (I/O)	-
10	PC0	PC0 (Output)	-
11	ROUT	ROUT (Output)	-
12	PG0	PG0 (I/O)	-
13	PG1	PG1 (I/O)	-
14	PG2	PG2 (I/O)	-
15	PG3	PG3 (I/O)	-
16	PH0	PH0 (I/O)	-
17	PH1	PH1 (I/O)	-
18	PH2	PH2 (I/O)	-
19	PH3	PH3 (I/O)	-

11. OTP PROGRAMMING

11.2. ADAM42P1116

11.2.1. PIN Assignment



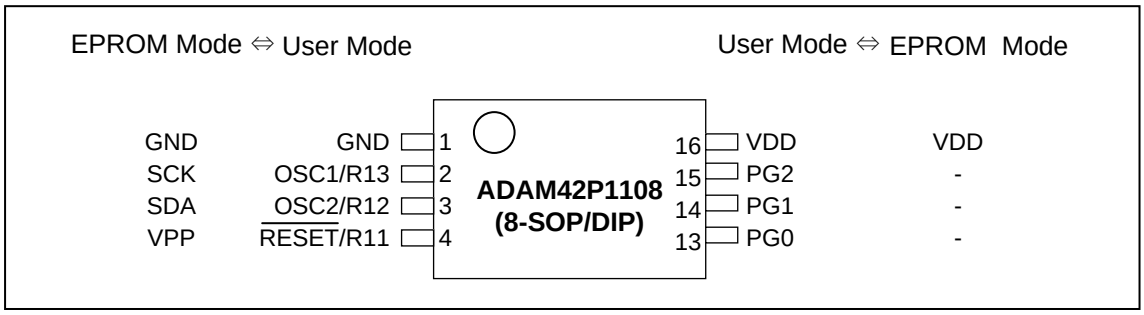
11.2.2. PIN Function

Pin No.	Port Name	User Mode	EPROM Mode
1, 16	GND, VDD	Power	Power
2	OSC1/R13	Clock (Input) or R13(I/O)	SCK (Input)
3	OSC2/R12	Clock (Output) or R12(I/O)	SDA (I/O)
4	$\overline{\text{RESET}}$/R11	$\overline{\text{RESET}}$(Input) or R11 (I/O)	VPP(11.5V)
5	R10	R10 (I/O)	-
6	PB0	PB0 (I/O)	-
7	PB2	PB2 (I/O)	-
8	PB3	PB3 (I/O)	-
9	PG0	PG0 (I/O)	-
10	PG1	PG1 (I/O)	-
11	PG2	PG2 (I/O)	-
12	PG3	PG3 (I/O)	-
13	PH0	PH0 (I/O)	-
14	PH1	PH1 (I/O)	-
15	PH2	PH2 (I/O)	-

11. OTP PROGRAMMING

11.3. ADAM42P1108

11.3.1. PIN Assignment



11.3.2. PIN Function

Pin No.	Port Name	User Mode	EPROM Mode
1, 8	GND, VDD	Power	Power
2	OSC1/R13	Clock (Input) or R13(I/O)	SCK (Input)
3	OSC2/R12	Clock (Output) or R12(I/O)	SDA (I/O)
4	$\overline{\text{RESET}}$/R11	$\overline{\text{RESET}}$(Input) or R11 (I/O)	VPP(11.5V)
5	PG0	PG0 (I/O)	-
6	PG1	PG1 (I/O)	-
7	PG2	PG2 (I/O)	-

11. OTP PROGRAMMING

11.4. AC / DC Timing for OTP Program Write / Read MODE (Ta = 25 ℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Programming Supply Current	I_{VPP}	-	-	50	mA
Supply Current in EPROM Mode	I_{VDDP}	-	-	20	mA
VPP Level during Programming	V_{IHP}	11.0	11.5	12.0	V
VDD Level in Program Mode	V_{DD1H}	4.75	5.0	5.25	V
VDD Level in Read Mode	V_{DD2H}	-	2.3 / 5.0	-	V
SCK/SDA Input High Level in EPROM Mode	V_{IHC}	V_{DD}*0.8	-	-	V
SCK/SDA Input Low Level in EPROM Mode	V_{ILC}	-	-	V_{DD}*0.2	V
Mode Latch Time	T_{MODI}	50	-	-	μs
Mode Setup Time	T_{MODS}	10	-	-	μs
Mode Hold Time	T_{MODH}	10	-	-	μs
Mode Clock Pulse Period	T_{MCK}	2	-	-	μs
VPP Setup Time	T_{VPPS}	1	15	30	ms
VPP Rise Time	T_{VPPR}	1	-	-	ms
SCK Pulse Width High	T_{PWH1}	2	-	-	μs
SCK Pulse Width Low	T_{PWL1}	2	-	-	μs
SDA Input Setup to SCK High	T_{SET1}	1	-	-	μs
SDA Input Hold after SCK Low	T_{HLD1}	1	-	-	μs
SCK High to SDA Output Valid	T_{HLD2}	-	-	T_{PWH}	μs
SCK Pulse Width High in Program Mode	T_{PWH2}	-	**50±10%**	-	μs

11. OTP PROGRAMMING

11.5. Configuration Option Bit Description

11.5.1. Optional Features

- 16 Bit for Option bit are available.
- The reserved bit(bit15) never write “0” data at program mode.
- Lock bit is available. (LOCK)
- RESET function selection (RSTS)
- LVD level selection (LVDS)
- Oscillator Type selection (XTS3 ~ XTS0)
- The reserved bits(bit7 ~ bit0) don’t care at verify mode and never write “0” data at program mode.

11.5.2. Configuration Option Bit mapping List [Address : 8000h]

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	-	LOCK	RSTS	LVDS	XTS3	XTS2	XTS1	XTS0	-	-	-	-	-	-	-	-	*8000h*
Initial value	1	1	1	1	1	1	1	1	x	x	x	x	x	x	x	x	

Bit Name	Option Description	Initial Value	Code Write Value	Option Result		
-	-	1 (No Writing =default)	-	-		
LOCK	LOCK disable or enable reading User Code	1 (No Writing =default)	0	Disable reading User Code. (But Device ID is readable)		
			1	Enable reading User Code.		
RSTS	RESET function Selection in R11/RESET port	1 (No Writing =default)	0	Use to R11 function in R11/RESET port.		
			1	Use to RESET function in P11/RESET port.		
LVDS	Low Voltage Detection Level Selection	1 (No Writing =default)	0	Low Voltage Detection Level high (typ. 2.2V)		
			1	Low Voltage Detection Level low (typ. 1.7V)		
XTS3 XTS2 XTS1 XTS0	Oscillator Type Selection	1 (No Writing =default)	**XTS[3:0]**	**Oscillator Modes (Type)**	**OSC1**	**OSC2**
			1111	Internal RC 3MHz	R13 (I/O)	R12 (I/O)
			1110	Internal RC 3MHz / PS1 Output	R13 (I/O)	1.5MHz (O)
			1101	Internal RC 1.5MHz	R13 (I/O)	R12 (I/O)
			1100	Internal RC 1.5MHz / PS1 Output	R13 (I/O)	0.75MHz (O)
			1011	Internal RC 750kHz	R13 (I/O)	R12 (I/O)
			1010	Internal RC 750kHz / PS1 Output	R13 (I/O)	0.375MHz (O)
			1001	Internal RC 6MHz	R13 (I/O)	R12 (I/O)
			1000	Internal RC 6MHz / PS1 Output	R13 (I/O)	3MHz (O)
			0111	External RC Oscillator	OSC1 (I)	R12 (I/O)
			0110	External RC Oscillator / PS1 Output	OSC1 (I)	PS1***** (O)
			0101	XT Oscillator	OSC1 (I)	OSC2 (O)
			0100			
			0011	External Clock Input	OSC1 (I)	R12 (I/O)
			0010	External Clock Input / PS1 Output	OSC1 (I)	PS1***** (O)
			0001	prohibited	-	-
			0000	prohibited	-	-

*** PS1 is divide by 2 of the oscillation frequency.**

12. INSTRUCTION SET

12.1. Legend

A : accumulator(4bit)

r : peripheral address register(6bit)

[r] : data addressed by peripheral address register (4bit)

Y : Y register(4bit)

X : X register(4bit)

ABR : address buffer register(15bit)

ABRn : address buffer register #0~3(4bit)

[@ABR] : data addressed by ABR(16bit)

DBR : data buffer register(16bit)

DBRn : data buffer register #0~3(4bit)

T0CR : Timer 0 count register(8bit)

T1CR : Timer 1 count register(8bit)

#n4 : 0~Fh

#n2 : 0~3

#n1 : 0~1

dp : data address point(8bit)

dp+X+Y : data address point indexed by X-register and Y-register (8bit)

PG : page address(1bit)

ADS : address stack register

!abs : address

12. INSTRUCTION SET

12.2. INSTRUCTION SET TABLE

NO	INSTRUCTION GROUP	MNEMONIC	USAGE	OPERATION	S	CY
1	Arithmetic & Logic	ADDC	ADDC m(dp),#n4	A = m(dp)+#n4+CY A = m(dp+X+Y)+#n4+CY at D flag of SFR is set. "S" set if overflow.	C	O
2			ADDC A,#n4	A = A+#n4+CY, "S" set if overflow	C	O
3			ADDC m(dp), A	A = m(dp) +A+CY, A = m(dp+X+Y) +A+CY at D flag of SFR is set. "S" set if overflow	C	O
4			ADDC ABRn,#n4	ABRn = ABRn + #n4+CY, "S" set if overflow	C	O
5			ADDC ABRn,A	ABRn = ABRn + A+CY, "S" set if overflow	C	O
6			ADDC ABRn,Y	ABRn = ABRn + Y+CY, "S" set if overflow	C	O
7			ADDC DBRn,#n4	DBRn = DBRn + #n4+CY, "S" set if overflow	C	O
8			ADDC DBRn,A	DBRn = DBRn + A+CY, "S" set if overflow	C	O
9			ADDC DBRn,Y	DBRn = DBRn + Y+CY, "S" set if overflow	C	O
10			ADDC Y,#n4	Y = Y + #n4 + CY, "S" set if overflow	C	O
11			ADDC X,#n4	X = X + #n4 + CY, "S" set if overflow	C	O

12		SUBC	SUBC m(dp),#n4	A = m(dp) - #n4-CY,
				A = m(dp+X+Y)- #n4-CY at D flag of SFR is set.
				"S" clear if underflow
					B	W

13			SUBC A,#n4	A = A - #n4-CY, "S" clear if underflow	B	W
14			SUBC m(dp), A	A = m(dp) – A-CY, A = m(dp+X+Y)- A-CY at D flag of SFR is set. "S" clear if underflow	B	W
15			SUBC ABRn, #n4	ABRn = ABRn - #n4-CY, "S" clear if underflow	B	W
16			SUBC ABRn, A	ABRn = ABRn – A-CY, "S" clear if underflow	B	W
17			SUBC ABRn, Y	ABRn = ABRn – Y-CY, "S" clear if underflow	B	W
18			SUBC DBRn, #n4	DBRn = DBRn - #n4-CY, "S" clear if underflow	B	W
19			SUBC DBRn, A	DBRn = DBRn - A-CY, "S" clear if underflow	B	W
20			SUBC DBRn, Y	DBRn = DBRn - Y-CY, "S" clear if underflow	B	W
21			SUBC Y, #n4	Y = Y- #n4-CY, "S" clear if underflow	B	W
22			SUBC X, #n4	X = X- #n4-CY, "S" clear if underflow	B	W
23		ARRC	ARRC	A = A rotate right with CY	T	R
24		ARLC	ARLC	A = A rotate left with CY	T	R
25		CMPL	CMPL	A = $\overline{A}$ + 1	Z	.
26		XOR	XOR m(dp)	A = A $\oplus$ m(dp) , A = A $\oplus$ m(dp+X+Y) at D flag of SFR is set	S	.
27		AND	AND m(dp)	A = A ^ m(dp) , A = A ^ m(dp+X+Y) at D flag of SFR is set	S	.
28		OR	OR m(dp)	A = A v m(dp) , A = A v m(dp+X+Y) at D flag of SFR is set	S	.

12. INSTRUCTION SET

NO	INSTRUCTION GROUP	MNEMONIC	USAGE	OPERATION	S	CY
29	Compare	CALE	CALE #n4	“S” set if A <= #n4	E	.
30			CALE m(dp)	“S” set if A <= m(dp), “S” set if A <= m(dp+X+Y) at D flag of SFR is set.	E	.
31		CAGE	CAGE #n4	“S” set if A >= #n4	E	.
32		CANE	CANE #n4	“S” set if A != #n4	N	.
33			CANE m(dp)	“S” set if A != m(dp), “S” set if A != m(dp+X+Y) at D flag of SFR is set.	N	.
34		CMLE	CMLE m(dp),#n4	“S” set if m(dp) <= #n4, “S” set if m(dp+X+Y) <= #n4 at D flag of SFR is set.	E	.
35		CMNE	CMNE m(dp),#n4	“S” set if m(dp) != #n4, “S” set if m(dp+X+Y) = #n4 at D flag of SFR is set.	N	.
36		CYGE	CYGE #n4	“S” set if Y >= #n4	E	.
37		CYNE	CYNE #n4	“S” set if Y != #n4	N	.
38			CYNE A	“S” set if Y != A	N	.
39		CXGE	CXGE #n4	“S” set if X >= #n4	E	.
40		CXNE	CXNE #n4	“S” set if X != #n4	N	.
41	Bit Manipulation	SET1	SET1 m(dp).#n2	Set bit m(dp).#n2, Set bit m(dp+X+Y).#n2 at D flag of SFR is set.	S	.
42		CLR1	CLR1 m(dp).#n2	Clear bit m(dp).#n2, Clear bit m(dp+X+Y).#n2 at D flag of SFR is set.	S	.
43		TM	TM m(dp).#n2	“S” set if m(dp) Bit = 1 “S” set if m(dp+X+Y) Bit = 1 at D flag of SFR is set.	E	.
44		SETR1	SETR1 r. #n2	Set bit [r]. #n2	S	.
45		CLRR1	CLRR1 r. #n2	Clear bit [r]. #n2	S	.
46		TSTR	TSTR r. #n2	“S” set if [r]. #n2 Bit = 1	E	.
47		NOTA1	NOTA1 #n2	A.#n2 ← ~ (A.#n2)	S	.
48	Carry Manipulation	CLRC	CLRC	Carry Bit of SFR is clear.	S	0
49		SETC	SETC	Carry Bit of SFR is set.	S	1
50		TSTC	TSTC	“S” set if Carry Test = 1.	E	.
51		LDC	LDC r.#n2	CY ← [r].#n2	S	.
52		STC	STC r.#n2	[r].#n2 ← CY	S	.
53	DATA Transfer	LDM	LDM m(dp),#n4	m(dp) = #n4 m(dp+X+Y) = #n4 at D flag of SFR is set.	S	.
54			LDM m(dp), A	m(dp) ← A m(dp+X+Y) ← A at D flag of SFR is set.	S	.
55		LDA	LDA #n4	A = #n4	S	.
56			LDA m(dp)	A ← m(dp) A ← m(dp+X+Y) at D flag of SFR is set.	S	.

12. INSTRUCTION SET

NO	INSTRUCTION GROUP	MNEMONIC	USAGE	OPERATION	S	CY
57	DATA Transfer	LDA	LDA X	A ← X	S	.
58			LDA Y	A ← Y	S	.
59		LDY	LDY #n4	Y = #n4	S	.
60			LDY A	Y ← A	S	.
61		LDX	LDX #n4	X = #n4	S	.
62			LDX A	X ← A	S	.
63		XMA	XMA m(dp)	A <=> m(dp) A <=> m (dp+X+Y) at D flag of SFR is set.	S	.
64		LDW	LDW @ABR	DBR ← (@ABR) **[Note]	S	.
65			LDW DBR,ABR	DBR ← ABR	S	.
66			LDW ABR,DBR	ABR ← DBR	S	.
67			LDW DBR,T0CR	DBR1,DBR0 ← T0CR	S	.
68			LDW DBR,T1CR	DBR3,DBR2 ← T1CR	S	.
69		LPG	LPG #n1	PG = #n1	S	.
70		LRA	LRA r	[r] ← A	S	.
71		LAR	LAR r	A ← [r]	S	.
72		LRI	LRI r,#n4	[r] = #n4	S	.
73	Increment	INC	INC ABR	ABR++	-	.
74	Branch	BR	BR !abs	If S bit of SFR =1 , Absolute branch, PC ← !abs	S	.
75			BR @ABR	If S bit of SFR =1 , Indirect branch PG+PC ← ABR	S	.
76	Subroutine	CALL	CALL !abs	If S bit of SFR =1 , ADS ← PG + PC, SP ← SP – 1 , PC ← !abs	S	.
77			CALL @ABR	If S bit of SFR =1 , ADS ← PG + PC, SP ← SP – 1 , PG+PC ← ABR	S	.
78		RET	RET	SP ← SP +1, PG+PC ← ADS	S	.
79		RETI	RETI	SPSFR ← SPSFR +1, SFR ← M(SPSFR) SP ← SP +1, PG+PC ← ADS	S	.
80	Etc	NOP	NOP		S	.
81		STOP	STOP		S	.
82		SLEEP	SLEEP		S	.
83		WDTC	WDTC	Watchdog Timer Clear	S	.
84		SPC	SPC	Stack Pointer Clear	S	.
85		EIX	EIX	Index bit of SFR is set	S	.
86		DIX	DIX	Index bit of SFR is clear	S	.
87		EI	EI	Interrupt bit of SFR is set	S	.
88		DI	DI	Interrupt bit of SFR is clear	S	.

**[Note] The Instruction “LDW @ABR” execution time is 2cycle and execution process is as follow.
SP = SP-1 , ADS← PG+PC ,
PG+PC ← ABR , DBR ← (PG+PC) , PG+PC ← ADS , SP = SP+1
.

** CARRY BIT(CY) hold previous value before execution CLRC/SETC instruction .
Symbols have meaning as follows.
- O : Carry bit is only set when overflow has occurred in operation.
- W : Carry bit is only set when borrow has occurred in operation.
- R : Carry bit is only set or reset according to shift bit.

** STATUS BIT(S) indicates conditions for changing status. Symbols have meaning as follows.
- S : On executing an instruction, status bit is unconditionally set.
- C : Status bit is only set when overflow has occurred in operation.
- B : Status bit is only set when underflow has not occurred in operation.
- E : Status bit is only set when equality is found in comparison.
- N : Status bit is only set when equality is not found in comparison.
- Z : Status bit only set when the result is zero.
- T : Status bit only set when the carry has occurred in operation.

12.3. INSTRUCTION SET

▶ ADDC (Add with Carry)

Add the contents of General Function Register to the contents of assigned memory address or the direct data value and Add carry bit value to the result. Store the result in general function register.

(Function) GFR = GFR + M + C

MNEMONIC	OPERAND	SFR			
		S	I	D	C
ADDC	m(dp), #n4	C	.	.	O
	A, #n4	C	.	.	O
	m(dp), A	C	.	.	O
	ABRn, #n4	C	.	.	O
	ABRn, A	C	.	.	O
	ABRn, Y	C	.	.	O
	DBRn, #n4	C	.	.	O
	DBRn, A	C	.	.	O
	DBRn, Y	C	.	.	O
	Y, #n4	C	.	.	O
	X, #n4	C	.	.	O

▶ SUBC (Subtract with Carry)

Subtract the contents of General Function Register to the contents of the assigned memory address or the direct data value and subtract carry bit value to the result. Store the result in general function register.

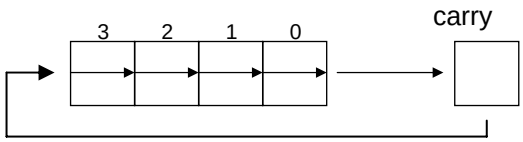
(Function) GFR ← GFR - M - C

MNEMONIC	OPERAND	SFR			
		S	I	D	C
SUBC	m(dp), #n4	B	.	.	W
	A, #n4	B	.	.	W
	m(dp), A	B	.	.	W
	ABRn, #n4	B	.	.	W
	ABRn, A	B	.	.	W
	ABRn, Y	B	.	.	W
	DBRn, #n4	B	.	.	W
	DBRn, A	B	.	.	W
	DBRn, Y	B	.	.	W
	Y, #n4	B	.	.	W
	X, #n4	B	.	.	W

▶ ARRC(Accumulator rotate right with carry)

The contents of A location to the right by 1 bit. Move bit0 to Carry flag, and carry into bit3.

(Function)

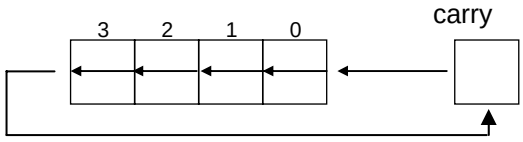


MNEMONIC	OPERAND	SFR			
		S	I	D	C
ARRC	-	T	.	.	R

▶ ARLC(Accumulator rotate left with carry)

The contents of A location to the left by 1 bit. Move bit3 to Carry flag, and carry into bit0.

(Function)



MNEMONIC	OPERAND	SFR			
		S	I	D	C
ARLC	-	T	.	.	R

▶ CMPL (Complement Accumulator)

Add the 1's complement contents of A to 1.
Store the result in A.

(Function) $A \leftarrow \overline{A} + 1$

MNEMONIC	OPERAND	SFR			
		S	I	D	C
CMPL	-	Z	.	.	.

▶ XOR (Logical Exclusive OR)

Exclusive OR operation of the contents of A with the contents of assigned memory address.
Store the result in A.

(Function) A ← A XOR M

MNEMONIC	OPERAND	SFR			
		S	I	D	C
XOR	m(dp)	S	.	.	.

▶ AND (Logical AND)

AND operation of the contents of A with the contents of assigned memory address. Store the result in A.

(Function) A ← A AND M

MNEMONIC	OPERAND	SFR			
		S	I	D	C
AND	m(dp)	S	.	.	.

▶ OR (Logical OR)

OR operation of the contents of A with the contents of assigned memory address. Store the result in A.

(Function) A ← A OR M

MNEMONIC	OPERAND	SFR			
		S	I	D	C
OR	m(dp)	S	.	.	.

▶ CALE (Compare to Accumulator)

Check the contents of A is less or equal compare to the contents of assigned memory address or the direct data value.

(Function) compare A <= #n4 , A <= m(dp) , A <= m(dp+X+Y)

MNEMONIC	OPERAND	SFR			
		S	I	D	C
CALE	#n4	E	.	.	.
	m(dp)	E	.	.	.

▶ CAGE (Compare to Accumulator)

Check the contents of A is greater or equal compare to the contents of the direct data value.

(Function) compare A >= #n4

MNEMONIC	OPERAND	SFR			
		S	I	D	C
CAGE	#n4	E	.	.	.

▶ CANE (Compare to Accumulator)

Check the contents of A is not equal with the contents of assigned memory address or the direct data value.

(Function) compare A != #n4 , A != m(dp) , A != m(dp+X+Y)

MNEMONIC	OPERAND	SFR			
		S	I	D	C
CANE	#n4	N	.	.	.
	m(dp)	N	.	.	.

▶ CMLE (Compare to memory)

Check the contents of assigned memory address is less or equal with the direct data value.

(Function) compare m(dp) <= #n4 , m(dp+X+Y) >= #n4

MNEMONIC	OPERAND	SFR			
		S	I	D	C
CMLE	m(dp), #n4	E	.	.	.

▶ CMNE (Compare to memory)

Check the contents of assigned memory address is not equal with the direct data value.

(Function) compare m(dp) != #n4 , m(dp+X+Y) != #n4

MNEMONIC	OPERAND	SFR			
		S	I	D	C
CMNE	m(dp), #n4	N	.	.	.

▶ CYGE (Compare to Y-register)

Check the contents of Y-register is greater or equal with the direct data value.

(Function) compare Y >= #n4

MNEMONIC	OPERAND	SFR			
		S	I	D	C
CYGE	#n4	E	.	.	.

▶ CYNE (Compare to Y-register)

Check the contents of Y-register is not equal with the contents of A or the direct data value.

(Function) compare Y != #n4 , Y != A

MNEMONIC	OPERAND	SFR			
		S	I	D	C
CYNE	#n4	N	.	.	.
	A	N	.	.	.

▶ CXGE(Compare to X-register)

Check the contents of X-register is greater or equal with the direct data value.

(Function) compare X >= #n4

MNEMONIC	OPERAND	SFR			
		S	I	D	C
CXGE	#n4	E	.	.	.

▶ CXNE(Compare to X-register)

Check the contents of X-register is not equal with the direct data value.

(Function) compare X != #n4

MNEMONIC	OPERAND	SFR			
		S	I	D	C
CXNE	#n4	N	.	.	.

▶ SET1 (Clear bit)

Set the bit of assigned memory address

(Function) m(dp).bit ← 1 , m(dp+X+Y).bit ← 1

MNEMONIC	OPERAND	SFR			
		S	I	D	C
SET1	m(dp).#n2	S	.	.	.

▶ CLR1 (Clear bit)

Clear the bit of assigned memory address

(Function) m(dp).bit ← 0 , m(dp+X+Y).bit ← 0

MNEMONIC	OPERAND	SFR			
		S	I	D	C
CLR1	m(dp).#n2	S	.	.	.

▶ TM

Check the bit of assigned memory address is 1.

(Function) m(dp).bit = 1 ? , m(dp+X+Y).bit = 1 ?

MNEMONIC	OPERAND	SFR			
		S	I	D	C
TM	m(dp).#n2	E	.	.	.

▶ SETR1 (Clear register data bit)

Set the bit of assigned register data.

(Function) [r].bit ← 1

MNEMONIC	OPERAND	SFR			
		S	I	D	C
SETR1	[r].#n2	S	.	.	.

▶ CLRR1 (Clear register data bit)

Clear the bit of assigned register data.

(Function) [r].bit ← 0

MNEMONIC	OPERAND	SFR			
		S	I	D	C
CLRR1	[r].#n2	S	.	.	.

▶ TSTR (Test register data bit)

Check the bit of assigned register data is 1.

(Function) [r].bit = 1 ?

MNEMONIC	OPERAND	SFR			
		S	I	D	C
TSTR	[r].#n2	E	.	.	.

▶ NOTA1 (Bit Complement of Accumulator)

Complement the bit of Accumulator.

(Function) A.bit = ~(A.bit)

MNEMONIC	OPERAND	SFR			
		S	I	D	C
NOTA1	#n2	S	.	.	.

▶ CLRC (Clear Carry Flag)

Clear the carry bit

(Function) CY ← 0

MNEMONIC	OPERAND	SFR			
		S	I	D	C
CLRC	-	S	.	.	0

▶ SETC (Set Carry flag)

Set the carry bit

(Function) CY ← 1

MNEMONIC	OPERAND	SFR			
		S	I	D	C
SETC	-	S	.	.	1

▶ TSTC (Test Carry Flag)

Check the content of carry bit is 1.

(Function) CY = 1?

MNEMONIC	OPERAND	SFR			
		S	I	D	C
TSTC	-	E	.	.	.

▶ LDC (Load Carry Flag)

Load the bit of assigned register data on the carry bit.

(Function) CY ← [r].#n2

MNEMONIC	OPERAND	SFR			
		S	I	D	C
LDC	[r].#n2	S	.	.	.

▶ STC (Store Carry Flag)

Store the carry bit into the bit of assigned register.

(Function) [r].#n2 ← CY

MNEMONIC	OPERAND	SFR			
		S	I	D	C
STC	[r].#n2	S	.	.	.

▶ LDM (Load memory)

Load the contents of A or the direct data value on assigned memory.

(Function) m(dp) ← #n4 , m(dp+X+Y) ← #n4, m(dp) ← A , m(dp+X+Y) ← A

MNEMONIC	OPERAND	SFR			
		S	I	D	C
LDM	m(dp), #n4	S	.	.	.
	m(dp), A	S			

▶ LDA (Load accumulator)

Load the contents of memory address or the direct data value , X-register's ,Y-register's on A .

(Function) A ← #n4 , m(dp) , m(dp+X+Y) , X-register , Y-register

MNEMONIC	OPERAND	SFR			
		S	I	D	C
LDA	#n4	S			
	m(dp)	S	.	.	.
	X	S			
	Y	S			

▶ LDY (Load register Y)

Load the contents of the A or the direct data value on Y register.

(Function) Y ← #n4 , A

MNEMONIC	OPERAND	SFR			
		S	I	D	C
LDY	#n4	S			
	A	S			

▶ LDX (Load register X)

Load the contents of the A or the direct data value on X- register.

(Function) X ← #n4 , A

MNEMONIC	OPERAND	SFR			
		S	I	D	C
LDX	#n4	S			
	A	S			

▶ XMA (Exchange Accumulator and Memory)

Exchange the contents of A and the contents of assigned memory.

(Function) A ↔ m(dp)

MNEMONIC	OPERAND	SFR			
		S	I	D	C
XMA	m(dp)	S			

▶ LDW (Load word)

Data transfer from function register to function register or from timer count register to function register.

(Function) DBR = @ ABR , DBR ← ABR , ABR ← DBR ,
DBR1+DBR0←T0CR , DBR3+DBR2←T1CR

MNEMONIC	OPERAND	SFR			
		S	I	D	C
LDW	@ABR	S	.	.	.
	DBR, ABR	S	.	.	.
	ABR, DBR	S	.	.	.
	DBR, T0CR	S	.	.	.
	DBR, T1CR	S	.	.	.

**[Note] The Instruction "LDW @ABR" execution time is 2cycle and execution process is as follow.

SP = SP-1 , ADS ← PG+PC ,

PG+PC ← ABR , DBR ← (PG+PC) , PG+PC ← ADS , SP = SP+1

▶ LPG (Load Rom page register)

Load 0 or 1 on 1-bit page register.

(Function) PG ← 0 or 1

MNEMONIC	OPERAND	SFR			
		S	I	D	C
LPG	#n1	S	.	.	.

▶ LRA (Load register from A)

Load the contents of A on the register assigned by peripheral address register(PAR).

(Function) [r] ← A

MNEMONIC	OPERAND	SFR			
		S	I	D	C
LRA	r	S	.	.	.

▶ LAR (Load A from register)

Load the contents of the assigned by peripheral address register(PAR) on A .

(Function) A ← [r]

MNEMONIC	OPERAND	SFR			
		S	I	D	C
LAR	r	S	.	.	.

▶ LRI (Load register immediate)

Load the direct data value on the register assigned by peripheral address register(PAR).

(Function) [r] ← #n4

MNEMONIC	OPERAND	SFR			
		S	I	D	C
LRI	r, #n4	S	.	.	.

▶ INC (Increment ABR)

Incrementing the address buffer register(ABR) by 1 .

(Function) ABR++

MNEMONIC	OPERAND	SFR			
		S	I	D	C
INC	ABR	.	.	.	.

▶ BR (Branch to address)

Branch to the assigned memory address.

(Function) If S bit of SFR =1 , PC ← !abs
PG+PC ← ABR

MNEMONIC	OPERAND	SFR			
		S	I	D	C
BR	!abs	S	.	.	.
	@ABR	S	.	.	.

▶ CALL (Subroutine Call)

Call the assigned memory address.

(Function) If S bit of SFR =1 , ADS ← PG + PC, SP ← SP – 1 , PC ← !abs
ADS ← PG + PC, SP ← SP – 1 , PG+PC ← ABR

MNEMONIC	OPERAND	SFR			
		S	I	D	C
CALL	!abs	S	.	.	.
	@ABR	S	.	.	.

▶ RET (Return from Subroutine)

By CALL instruction, return to the address pushed onto stack.

(Function) SP ← SP +1, PG+PC ← ADS

MNEMONIC	OPERAND	SFR			
		S	I	D	C
RET	-	S	.	.	.

▶ RETI (Return from Interrupt)

Right after finishing the interrupt processing routine, execute from the next to instruction, which is executed before interrupt occur and use always this instruction in the last stage of interrupt processing routine.

(Function) SPSFR ← SPSFR +1, SFR ← M(SPSFR)
SP ← SP +1, PG+PC ← ADS

MNEMONIC	OPERAND	SFR			
		S	I	D	C
RETI	-	S	.	.	.

▶ NOP (No Operation)

No operation

MNEMONIC	OPERAND	SFR			
		S	I	D	C
NOP	-	S	.	.	.

▶ STOP (Stop mode)

(Function) Oscillation Stop

MNEMONIC	OPERAND	SFR			
		S	I	D	C
STOP	-	S	.	.	.

▶ SLEEP (Sleep mode)

(Function) Sleep the system clock

MNEMONIC	OPERAND	SFR			
		S	I	D	C
SLEEP	-	S	.	.	.

▶ WDTC (Watchdog timer clear)

Watchdog timer clear

MNEMONIC	OPERAND	SFR			
		S	I	D	C
WDTC	-	S	.	.	.

▶ SPC (Stack Pointer clear)

Stack Pointer clear

MNEMONIC	OPERAND	SFR			
		S	I	D	C
SPC	-	S	.	.	.

▶ EIX (Set index flag bit)

Set the index flag bit of SFR.

(Function) IX ← 1

MNEMONIC	OPERAND	SFR			
		S	I	D	C
EIX	-	S	.	1	.

▶ DIX (Disable index flag bit)

Clear the index flag bit of SFR.

(Function) IX ← 0

MNEMONIC	OPERAND	SFR			
		S	I	D	C
DIX	-	S	.	0	.

▶ EI (Set interrupt flag bit)

Set the interrupt flag bit of SFR.

(Function) I ← 1

MNEMONIC	OPERAND	SFR			
		S	I	D	C
EI	-	S	1	.	.

▶ DI (Disable interrupt flag bit)

Clear the interrupt flag bit of SFR.

(Function) I ← 0

MNEMONIC	OPERAND	SFR			
		S	I	D	C
DI	-	S	0	.	.