December 3, 2015 Ver 0.6

4-BIT SINGLE CHIP MICROCOMPUTERS

ADAM43P1108

USER`S MANUAL

ABOV SEMICONDUCTOR

0. Revision History

Version	Date	Description
VER 0.0	2008.11.25	1'st Release.
VER 0.1	2009.6.23	remove "T1" of the Timer-0 Source clock.
VER 0.2	2009.7.09	added the section of MTP Programming and Instruction Set.
VER 0.3	2010.9.28	added the description of PS0~PS11 for Timer Clock Source. changed the specification of sleep mode current.
VER 0.4	2010.12.14	correct the error in page 73. (14.2. Configuration Option Bit Description) added the characteristic graph and specification of the Internal RC Oscillator.
VER 0.5	2013.4.4	correct the error in page 30, 57, 58.
VER 0.6	2015.12.3	Add the chapter '1.7.3 POR Electrical Characteristics'. (12 page) Add the electrical specification of LVD & Temperature characteristics. (13, 15 page)

1. Overview

The ADAM43P1108 is the High Speed and Low Voltage operating 4-bit single chip microcomputer. This chip contains ADAM43 CPU, EPROM, RAM, Timer/PWM, Interrupt, Watch Dog Timer, 12-bit ADC, Input/Output Ports and Oscillation Circuit.

1.1. Features

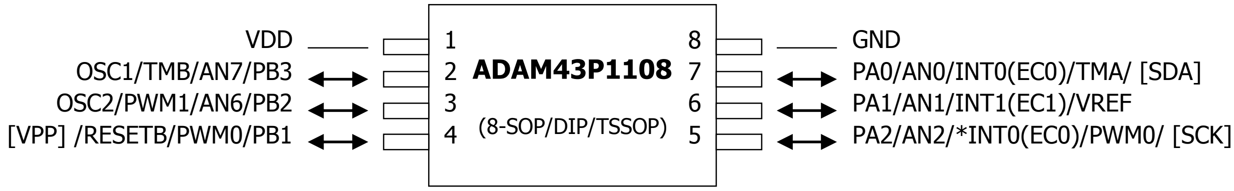
- Instruction Execution Time
  - 500ns @ f_{OSC}=8MHz
- Program Memory Area (MTP)
  - 4K Bytes (2,048 x 16bit)
  - Multi-programmable by 2K Bytes(1,024 x 16bit)
- Data memory (RAM)
  - 128 nibble (128 x 4bit)
- 16-Bit Table read Instruction.
- A/D Converter
  - 12Bit x 5ch
- Timer (Timer/Counter/Capture/PWM)
  - 12Bit x 1ch [PWM0 : (8+4)bit x 1ch]
  - 8Bit x 1ch [PWM1 : (6+2)bit x 1ch]
- Watch-Dog Timer (with RCWDT=64kHz)
  - 19Bit x 1ch
- Oscillator Type
  - Calibrated Internal RCOSC : typ. 16/8/4/1MHz(±2%) selectable
  - External R-OSC : 400k~16MHz
  - External Clock Input : 400k ~ 16MHz
  - Crystal/Resonator : 400k ~ 16MHz, 32.768kHz
- Power On Reset
- Power Saving Operation Modes
  - STOP
  - SLEEP
  - RCWDT
- Interrupt Sources
  - External : 3ch (KSCN, INT0, INT1)
  - Internal : 5ch (T0, T1, ADC, WDT, VDI)
- Low Voltage Detection Reset Circuit
- 3-level Voltage Detection Indicator (4.0V/3.0V/2.5V)
- Operating Voltage Range
  - 2.0 ~ 5.5 V @ 30kHz ~ 4MHz
  - 2.7 ~ 5.5 V @ 4MHz ~ 16MHz
- Operating Temperature Range
  - -40 ~ 85 ℃

☑ ADAM43P1108 Device Summary

Series	ADAM43P1108
Program memory	2,048 x 16
Data memory	128 x 4
I/O ports	6
Package	8-SOP/DIP/TSSOP

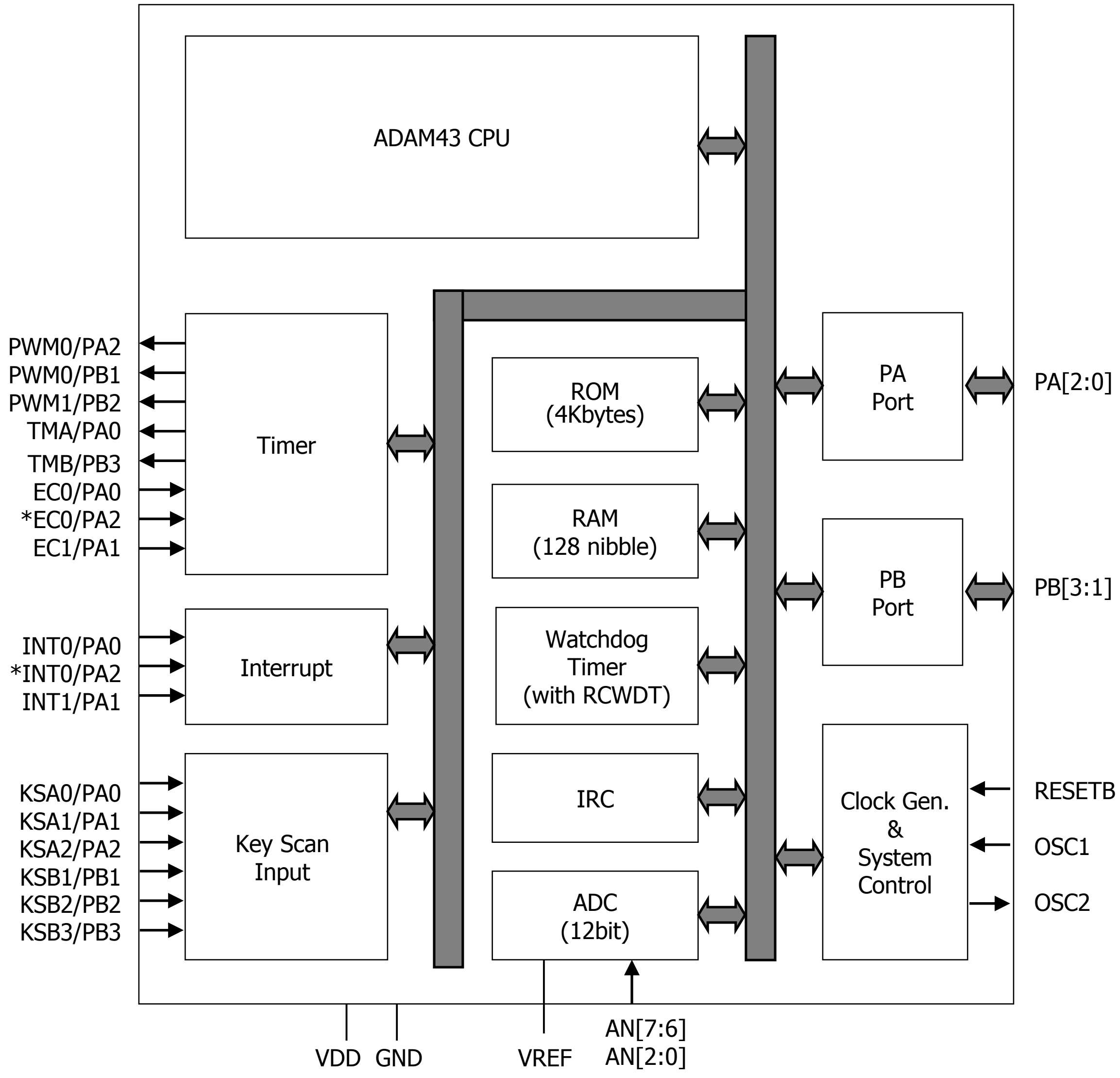
1. Overview

1.2. Pin Assignments



*※ INT0(EC0) and *INT0(EC0) must be used by only one pin at a application.*
※ OSC1, OSC2, RESETB is selected by setting the OTP Configuration Bit.

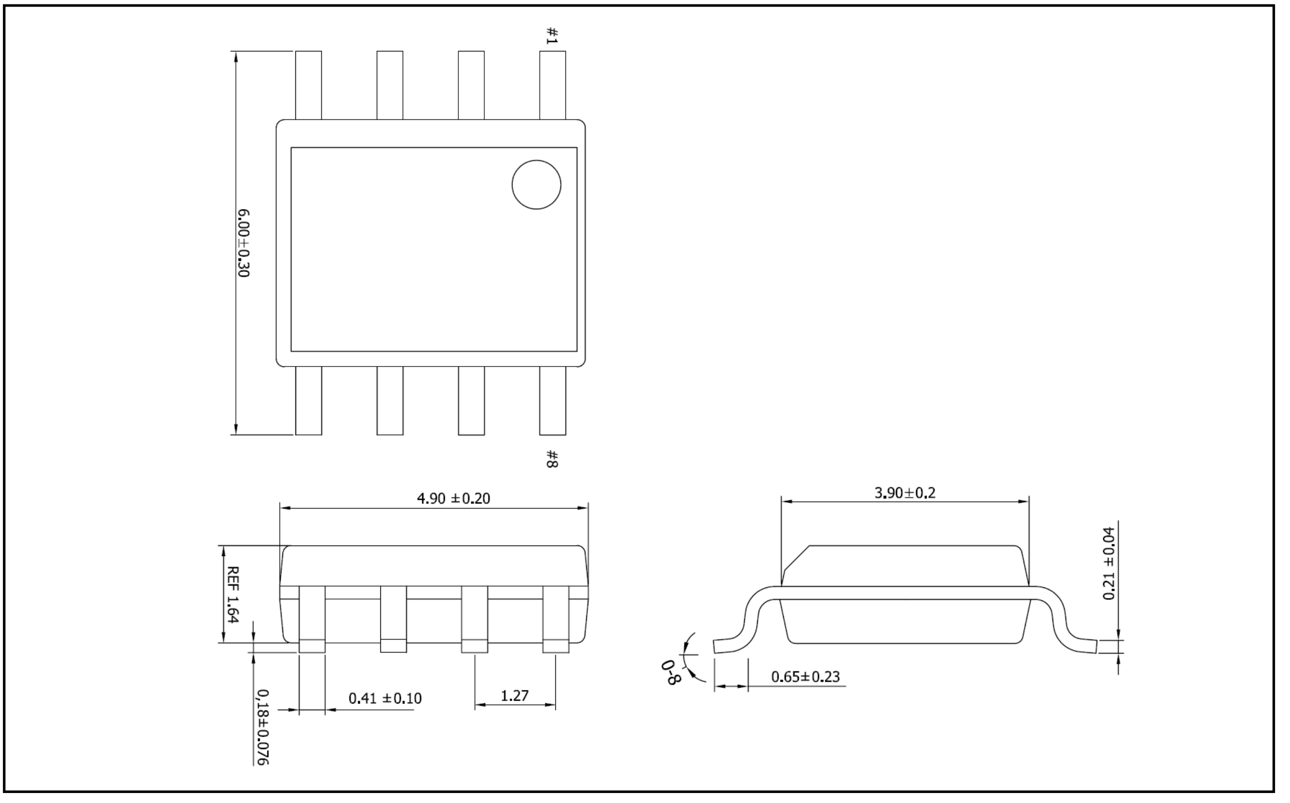
1.3. Block Diagram



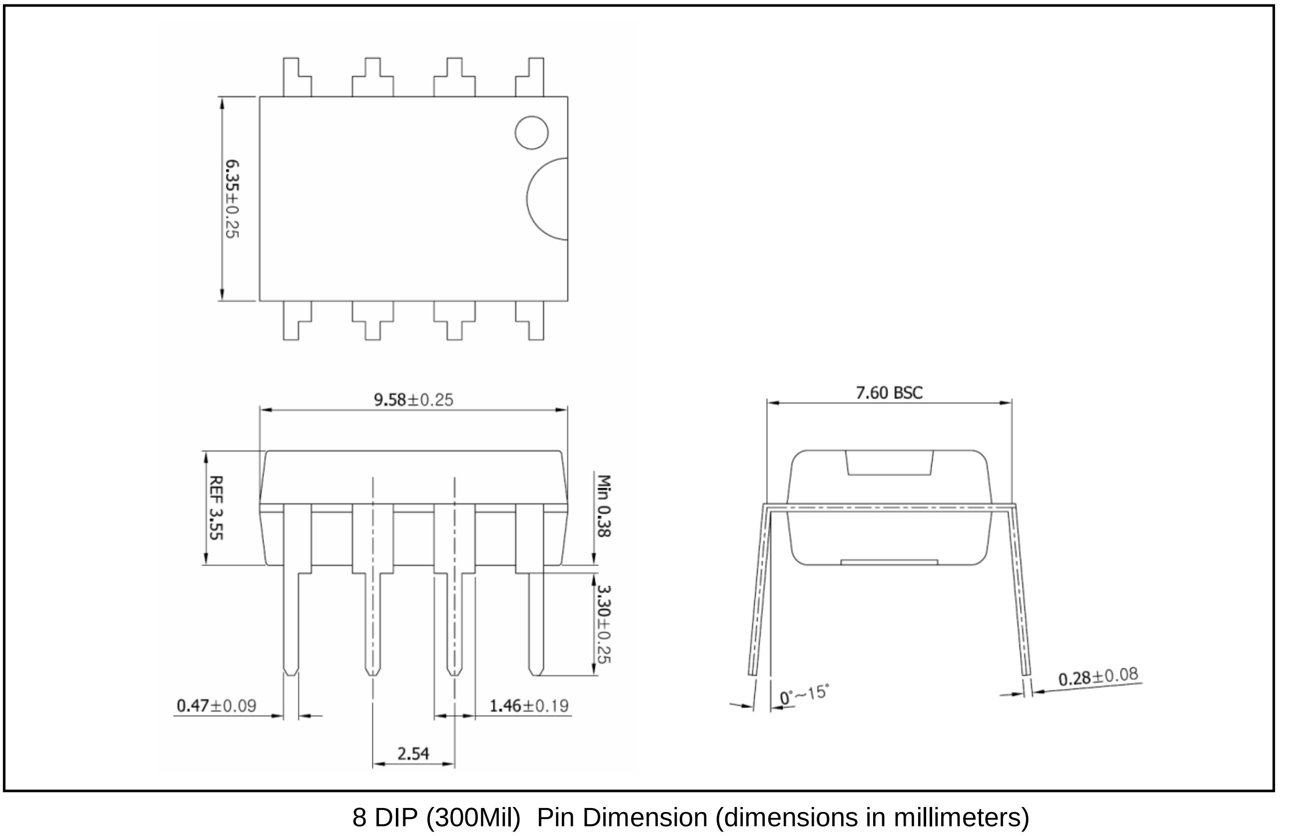
*※ INT0(EC0) and *INT0(EC0) must be used by only one pin at a application.*
※ OSC1, OSC2, RESETB is selected by setting the OTP Configuration Bit.

1. Overview

1.4. Package Dimension

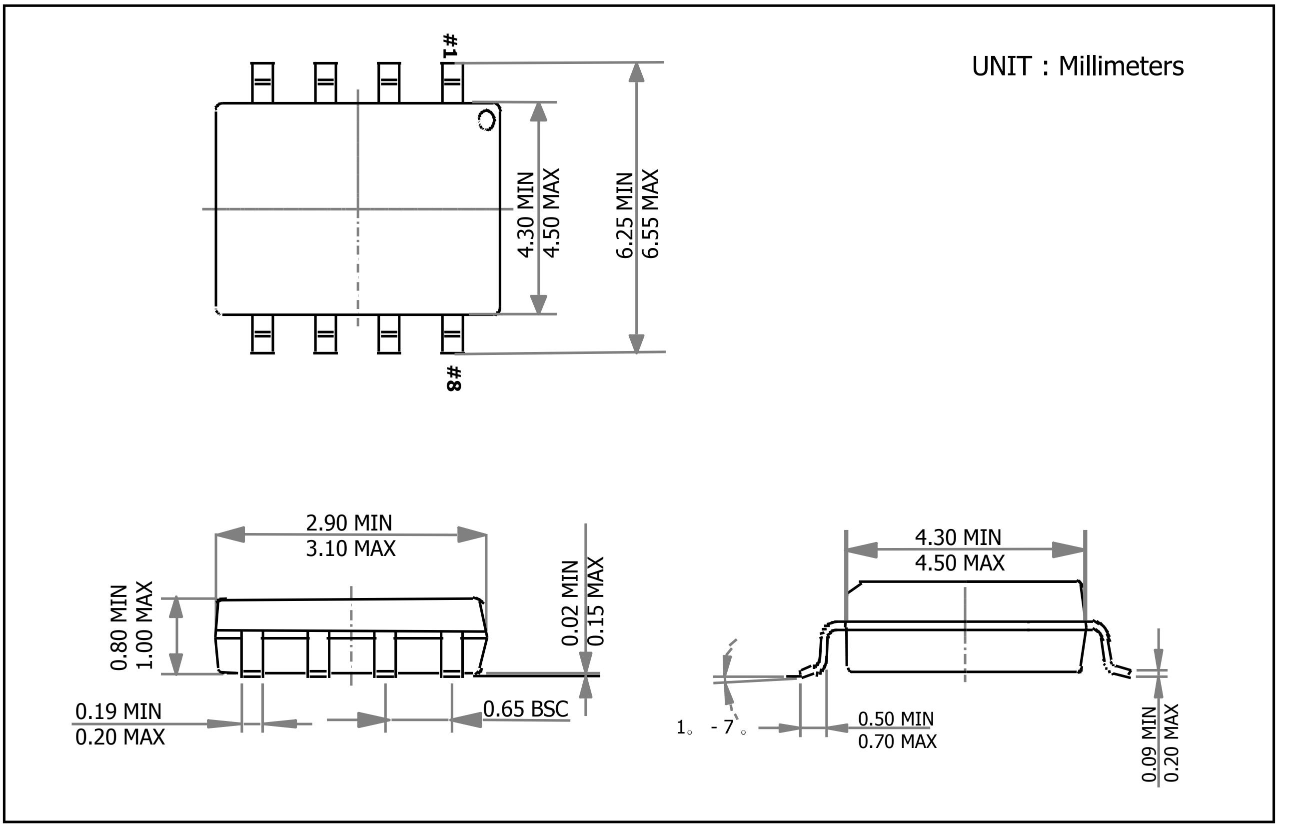


8 SOP (150Mil) Pin Dimension (dimensions in millimeters)



8 DIP (300Mil) Pin Dimension (dimensions in millimeters)

1. Overview



8 TSSOP (4.4 mm) Pin Dimension (dimensions in inch [millimeters])

1. Overview

1.5. Pin Function

1.5.1. Port Pins

Pin Name	I/O	Function	@RESET	@STOP	Shared Pins
PA0	I/O	- 3-bit I/O Port. - CMOS input. - Push-pull output. - Each pin can be set and reset by Data register value. - Can be programmable as Pull-up/N-ch open drain/ KSCN/AN/INT(EC)/TIMER output/VREF individually. - Direct driving of LED (N-TR).	Input (without Pull-up)	State of before STOP	TMA/INT0(EC0) /AN0/KSA0
PA1					VREF/INT1(EC1) /AN1/KSA1
PA2					PWM0/*INT0(EC0) /AN2/KSA2
PB1	I/O	- 3-bit I/O Port. - CMOS input. - Push-pull output (except PB1). - Each pin can be set and reset by Data register value. - Can be programmable as Pull-up/N-ch open drain /KSCN/AN/TIMER output individually. - Direct driving of LED (N-TR). - PB1 is N-ch Open drain output only at output mode. - PB2 and PB3 can be selected Pull-down individually.	Input (without Pull-up)	State of before STOP	RESETB/PWM0 /KSB1
PB2					OSC2/PWM1 /AN6/KSB2
PB3					OSC1/TMB /AN7/KSB3

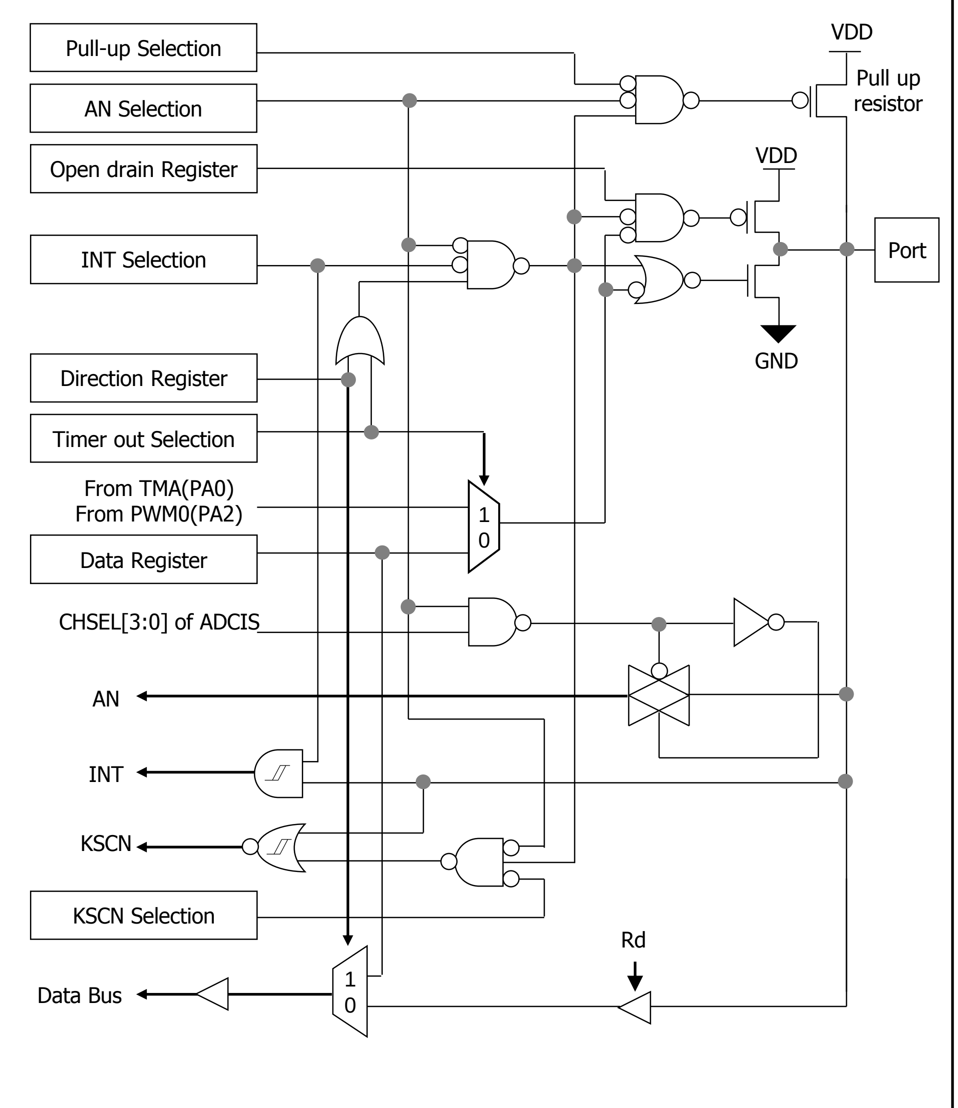
1.5.2. Non-port Pins

Pin Name	I/O	Function	@RESET	Shared Pins
INT0	I	- External Interrupt input for which the valid edges (rising edge, falling edge , both rising and falling edge) can be specified. - Timer0, Timer1 capture input.	Input (Pull-up off)	PA0
				PA2
INT1				PA1
EC0	I	- Timer0, Timer1 event counter input.	Input (Pull-up off)	PA0
				PA2
EC1				PA1
PWM0	O	- 12-bit PWM (shared with Timer0) output.	Input (Pull-up off)	PA2
				PB1
PWM1	O	- 8-bit PWM (shared with Timer1) output.	Input (Pull-up off)	PB2/OSC2
TMA	O	- Timer0, Timer1 logic output.	Input (Pull-up off)	PA0
TMB				PB3/OSC1
KSA0 ~ KSA2	I	- Key Scan Interrupt input and STOP mode release input which the valid edges (rising edge, falling edge, both rising and the falling edge) can be specified.	Input (Pull-up off)	PA0 ~ PA2
KSB1 ~ KSB3				PB1 ~ PB3
AN0 ~ AN2	I	- Analog input for A/D Converter. - Each port's pull-up resistor is disabled at A/D input mode.	Input (Pull-up off)	PA0 ~ PA2
AN6 ~ AN7				PB2 ~ PB3
VREF	P	- Analog power for A/D converter.	Input (Pull-up off)	PA1
OSC1	I	- Oscillator input.	Input (Pull-up off)	PB3
OSC2	O	- Oscillator output.	Input (Pull-up off)	PB2
RESETB	I	- External RESETB Input by Code/Register Option.	Input (Pull-up off)	PB1
VDD	P	- Positive power supply.	-	-
GND	P	- Ground.	-	-

1.5.3. OTP Programming Pin Description (OTP Program Mode)

Pin No.	Pin Name	I/O	Function	Shared Pins
#1	VDD	P	- Programming Power supply (+ 5.0V)	VDD
#4	VPP	P	- Programming high voltage Power supply (+11.5V)	PB1/PWM0/RESETB
#8	GND	P	- Ground	GND
#5	SCK	I	- Programming Clock input pin	PA2/AN2/*INT0(EC0)/PWM0
#7	SDA	I/O	- Programming Data Input/Output pin	PA0/AN0/INT0(EC0)/TMA

1.6. Port Structure

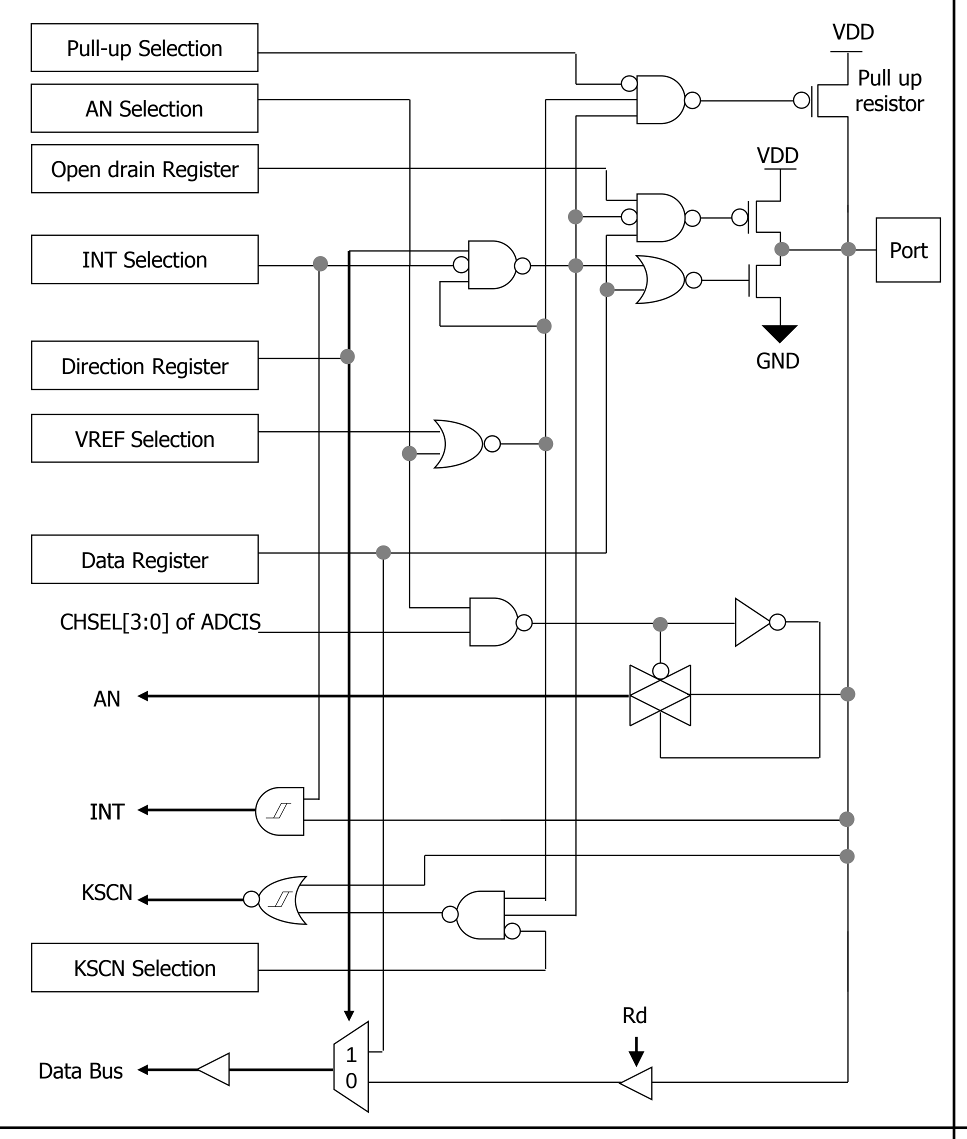
Pin Name	Circuit Type	RESET
PA0 **PA2**		Input (without Pull-up)
Shared Function	KSCN/AN/INT(EC)/TIMER	

Assignment	Direction	Pull-Up	Port Read		Port	Remarks	RESET
			Dir. Input	Dir. Output			
KSCN	**	**	Port	Data	KSA0 KSA2	Schmitt input	Disable
AN	Input	Off	unknown	Data	AN0 AN2		
INT	Input	**	Port	Data	INT0(EC0) *INT0(EC0)	Schmitt input	
TIMER	Output	Off	Port	Data	TMA PWM0		

** : It is depend on user definition.

1. Overview

1.6. Port Structure

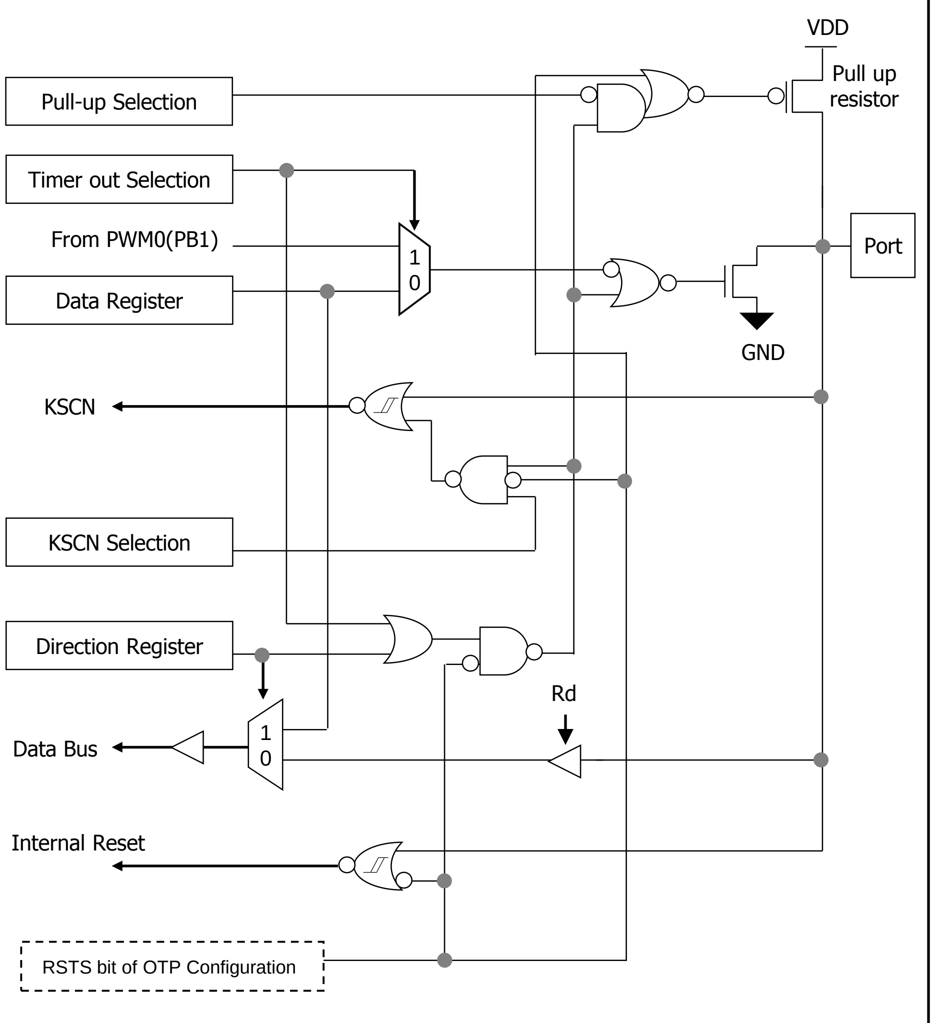
Pin Name	Circuit Type	RESET
PA1		Input (without Pull-up)
Shared Function	KSCN/AN/INT(EC)/VREF	

Assignment	Direction	Pull-Up	Port Read		Port	Remarks	RESET
			Dir. Input	Dir. Output			
KSCN	*	*	Port	Data	KSA1	Schmitt input	Disable
AN	Input	Off	unknown	Data	AN1		
INT	Input	*	Port	Data	INT1 (EC1)	Schmitt input	
VREF	Input	Off	Unknown	Data	VREF	ADC power	

* : It is depend on user definition.

1. Overview

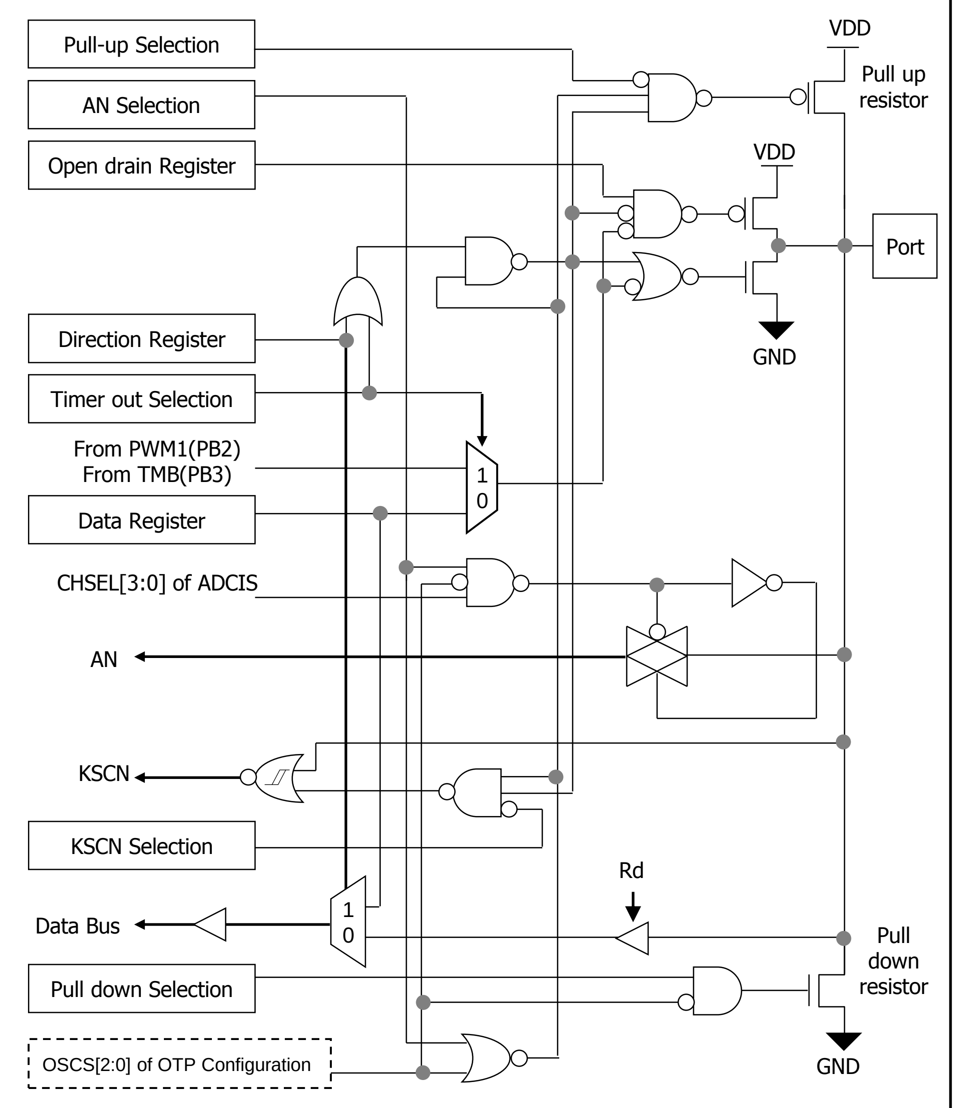
1.6. Port Structure

Pin Name	Circuit Type	RESET
PB1		Input
Shared Function	KSCN/TIMER/RESETB	

Assignment	Direction	Pull-Up	Port Read		Port	Remarks	RESET
			Dir. Input	Dir. Output			
KSCN	*	*	Port	Data	KSB1	Schmitt input	Disable
TIMER	Output	Off	Port	Data	PWM0		
RESETB	Input	On	Port	Data	RESETB	Schmitt input with pull-up	RESETB

* : It is depend on user definition.

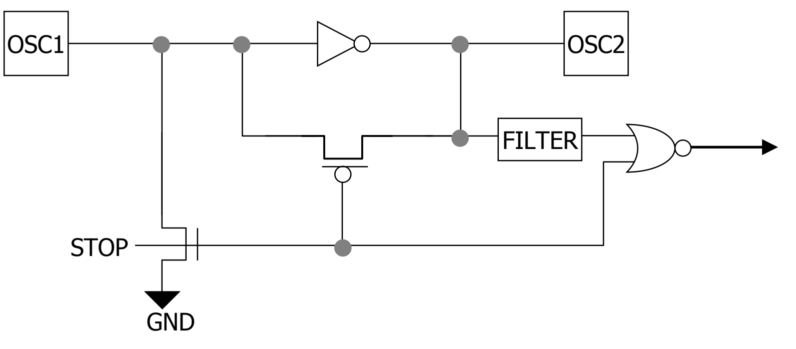
1.6. Port Structure

<table>
<tr><th>Pin Name</th><th>Circuit Type</th><th>RESET</th></tr>
<tr><td>PB2
PB3</td><td>
</td><td>Input
(without
Pull-up)</td></tr>
<tr><td>Shared
Function</td><td>KSCN/AN/TIMER/Pull-Down</td><td></td></tr>
</table>

Assignment	Direction	Pull-Up	Pull -Down	Port Read		Port	Remarks	RESET
				Dir. Input	Dir. Output			
KSCN	*	*	*	Port	Data	KSB2 KSB3	Schmitt input	Disable
AN	Input	Off	Off	unknown	Data	AN6 AN7		
TIMER	Output	Off	Off	Port	Data	PWM1 TMB	Schmitt input	
Pull-Down	*	*	On	Port	Data	*	Pull-down	
OSC1	Input	Off	Off	unknown	Data	OSC1	XT,LP,ERC	
OSC2	Input	Off	Off	unknown	Data	OSC2	XT,LP	

* : It is depend on user definition.

1.6. Port Structure (OSC1/OSC2 mode)

Pin Name	Circuit Type	RESET
OSC1 OSC2	(XT, LP Mode) 	Oscillation

1.7. Electrical Characteristics

1.7.1. Absolute Maximum Ratings (Ta = 25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.3 ~ +6.0	V
Input Voltage	V_I	-0.3 ~ VDD + 0.3	V
Output Voltage	V_O	-0.3 ~ VDD + 0.3	V
Storage Temperature	T_{STG}	-65 ~ 150	°C
Power Dissipation	P_D	700	mW

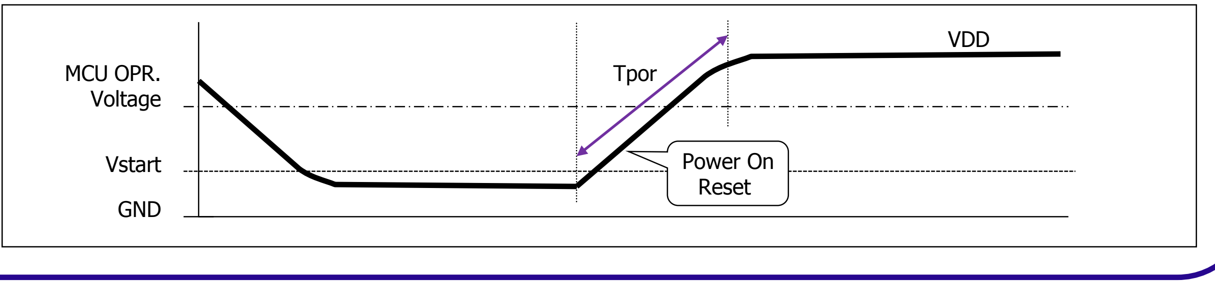
1.7.2. Recommended Operating Ranges

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX	UNIT
Supply Voltage	V_{DD}	f_{OSC} = 4MHz	2.0	-	5.5	V
		f_{OSC} = 16MHz	2.7	-	5.5	V
Oscillation Frequency	f_{OSC}	Crystal/Ceramic Resonator External Clock External RC Oscillator	0.4	4	16	MHz
		Crystal Resonator	-	32.768	-	kHz
		Calibrated Internal RC Oscillator (Ta=-20 ~ 70℃)	15.68	16.00	16.32	MHz
			7.84	8.00	8.16	
			3.92	4.00	4.08	
			0.98	1.00	1.02	
			(-2%)	-	(+2%)	
		Calibrated Internal RC Oscillator (Ta=-40~85℃)	15.52	16.00	16.48	
			7.76	8.00	8.24	
			3.88	4.00	4.12	
			0.97	1.00	1.03	
			(-3%)	-	(+3%)	
Operating Temperature	T_{OPR}		-40		85	°C

1.7.3. POR(Power on Reset) Electrical Characteristics (VDD=5.5V~2.0V, VSS=0V, Ta = −40℃~85℃)

Parameter	**Symbol**	**Condition**	**Specification**			Unit
			MIN	TYP	MAX	
POR Start voltage	Vstart*	Tpor > 0.35V/ms	VSS	-	0.2	V
		Tpor > 0.05V/ms	-	-	VSS	V
VDD Voltage Rising Time	Tpor*		0.05	-	-	V/ms

*) These parameters are presented for design guidance only and not tested or guaranteed.



1.7.4. DC Characteristics (Ta = 25℃)

PARAMETER	Symbol	Condition			Specification MIN.	TYP.	MAX.	UNIT
High level input voltage	V_{IHX}	OSC1			0.9VDD		VDD	V
	V_{IH1}	RESETB, KSCN, INT0/EC0, INT1/EC1			0.8VDD		VDD	V
	V_{IH2}	PA, PB			0.7VDD		VDD	V
Low level input voltage	V_{ILX}	OSC1			0		0.1VDD	V
	V_{IL1}	RESETB, KSCN, INT0/EC0, INT1/EC1			0		0.2VDD	V
	V_{IL2}	PA, PB			0		0.3VDD	V
High level input leakage current	I_{IH}	PA, PB		VIH = VDD			1	uA
Low level input leakage current	I_{IL}	PA, PB		VIL = 0V			-1	uA
High level output voltage	V_{OH1}	PA, PB (Except PB1)	VDD = 5V	IOH = -10mA	VDD-1.0			V
	V_{OHX}	OSC2	VDD = 5V	IOH = -0.2mA	VDD-1.0			V
Low level output voltage	V_{OL1}	PA, PB	VDD = 5V	IOL = 15mA			1.0	V
	V_{OL2}	PA, PB (Reg. selectable)	VDD = 5V	IOL = 25mA			1.0	V
	V_{OLX}	OSC2	VDD = 5V	IOL = 0.2mA			1.0	V
High level output leakage current	I_{OHL}	PA, PB		VOH = VDD			1	uA
Low level output leakage current	I_{OLL}	PA, PB		VOL = 0V			-1	uA
Input Pull-up current	I_{PU}	PA, PB	VDD = 5V		-25	-50	-100	uA
Input Pull-down current	I_{PD}	PB2, PB3	VDD = 5V		25	50	100	uA
Power supply current	I_{DD}	Operating current	VDD = 5V	fXIN = 10MHz		2	2.5	mA
			VDD = 5V	fXIN = 4MHz		1	1.5	mA
	I_{SLEEP}	Sleep mode current	VDD = 5V	fXIN = 10MHz		1	2	mA
			VDD = 5V	fXIN = 4MHz		0.6	1.2	mA
	I_{STOP}	Stop mode current (Oscillator Stop)	VDD = 5V	RCWDT On		10	20	uA
			VDD = 5V	LVD On		2	5	uA
			VDD = 5V	LVD Off		-	1	uA
RCWDT Frequency	F_{RCWDT}	RCWDT	VDD = 5V		32	64	128	KHz
RAM retention supply voltage	V_{RET}				0.7			V
Low Voltage Detection	LVD	LVDS=1 (in the Configuration Bits), Ta=25℃			1.5	1.7	2.0	V
		LVDS=0 (in the Configuration Bits), Ta=25℃			2.0	2.2	2.5	V

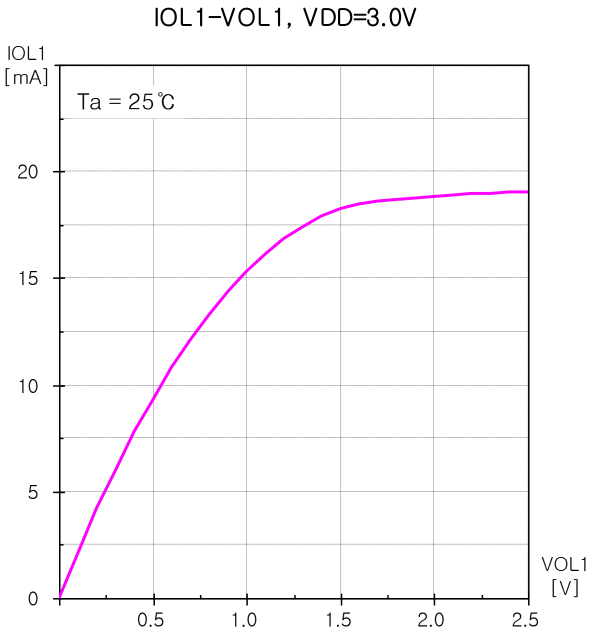
1. Overview

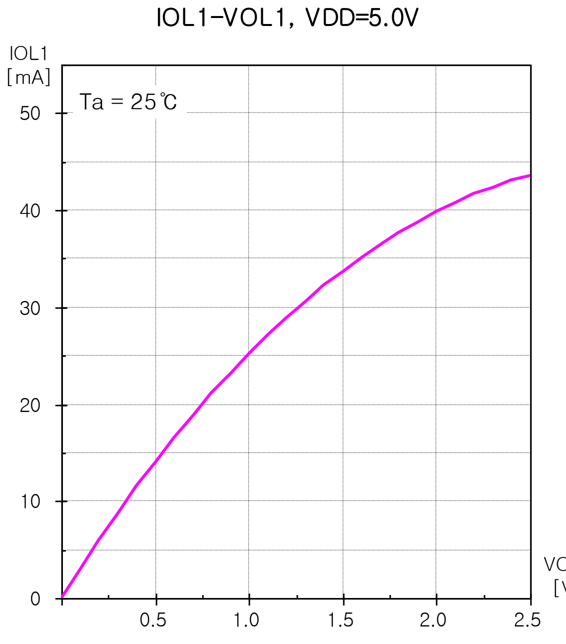
※ Typical Characteristics

This graphs provided in this section are for design guidance only and are not tested or guaranteed.

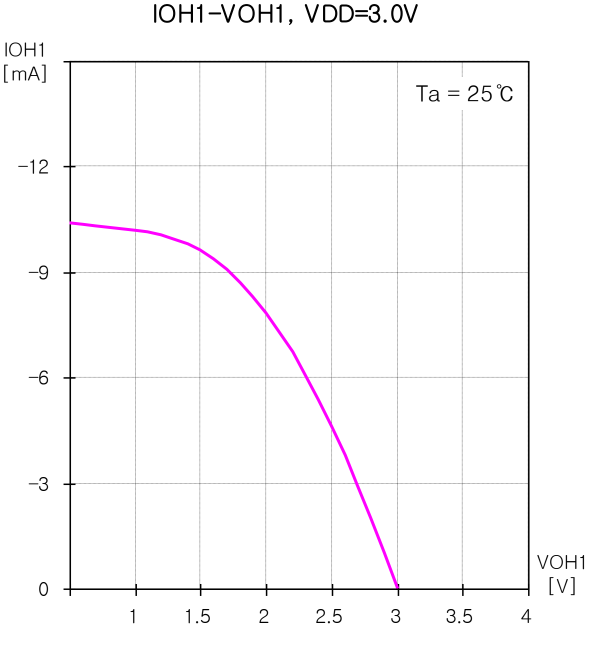
The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean – 3σ) respectively where σ is standard deviation.

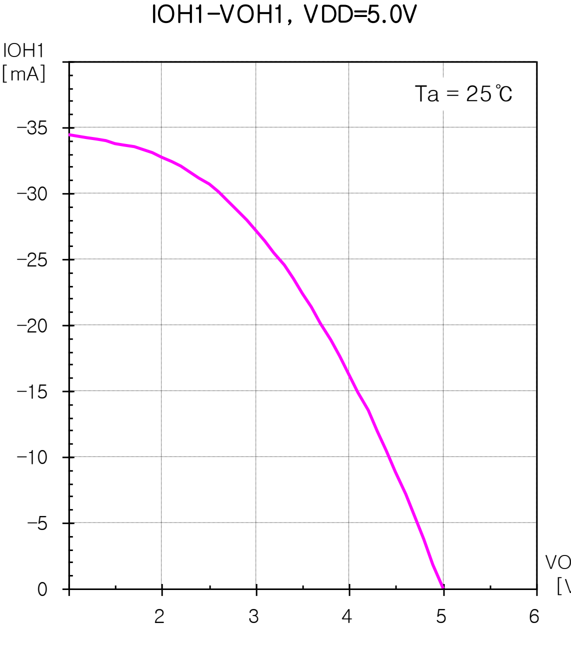
▶ **IOL1 vs. VOL1 (at T=25℃)**





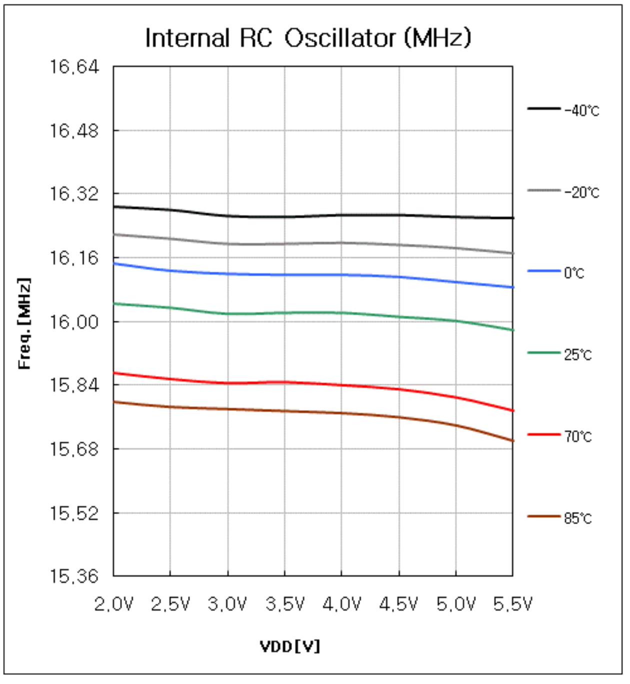
▶ **IOH1 vs. VOH1 (at T=25℃)**

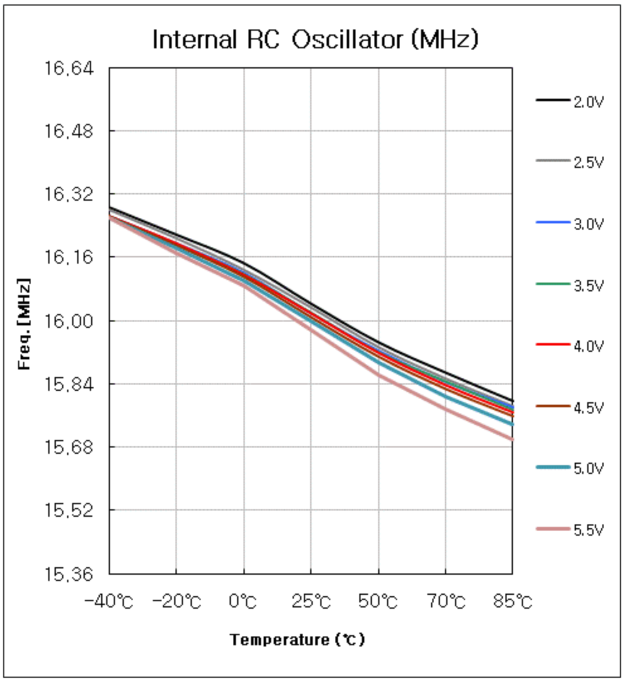




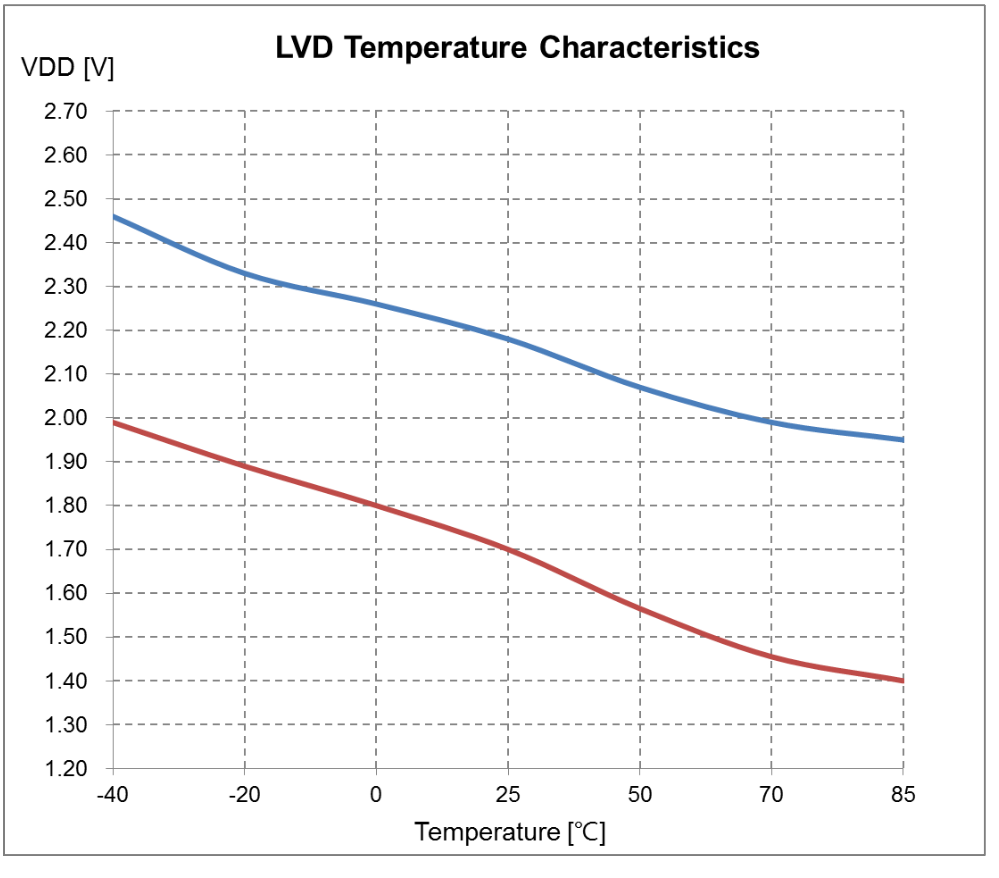
1. Overview

▶ Internal RC Oscillator Characteristics





▶ Low Voltage Detection (Temperature Characteristics)



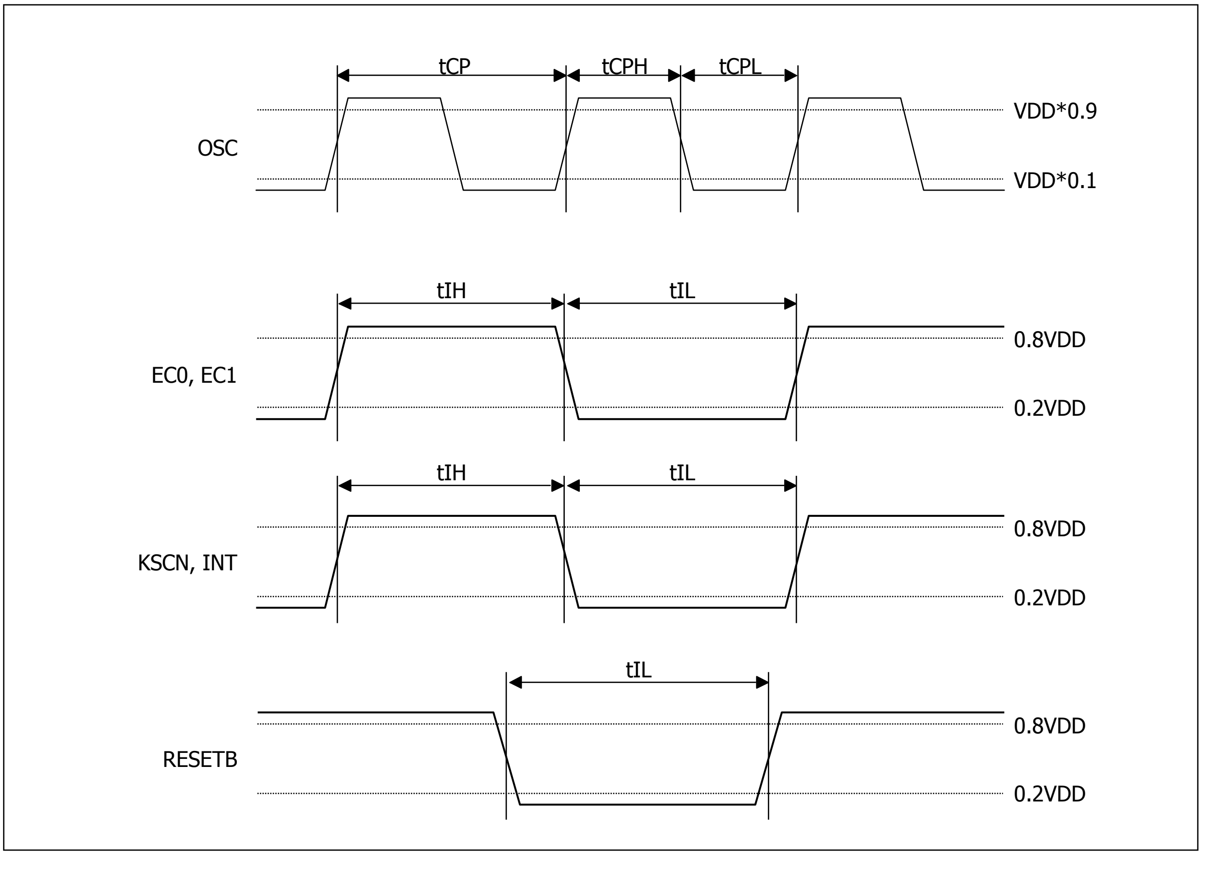
1.7.5. 12Bit A/D Conversion Characteristics (VDD=5.5 ~ 2.7V @f_{XIN}=30kHz~16MHz, Ta=25℃)

Parameter	**Symbol**	**Condition**	**Specification**			Unit
			MIN	TYP	MAX	
Resolution	RADC			12		Bits
Analog Input Voltage Range	VAIN	AVREFS = 0	VSS	-	VDD	V
		AVREFS = 1	VSS	-	AVREF	V
Analog Input Power Supply Voltage Range	AVREF	VDD = 5.0V	2.4	-	VDD	V
		VDD = 3.0V	2.4	-	VDD	V
Overall Accuracy	EACC	VDD=4.096V, f_{XIN} = 4MHz	-	-	±4.0	LSB
Non-Linearity Error	ENE		-	-	±4.0	LSB
Differential Non-Linearity Error	EDE		-	±1.0	±2.0	LSB
Zero Offset Error	EOFF		-	±1.0	±3.0	LSB
Full Scale Error	EFE		-	±1.0	±3.0	LSB
Conversion Time	TCONV	VDD = 5.5V ~ 2.7V	29	-	-	㎲
AVREF Input Current	IREF	AVREFS = 1	-	0.8	2.0	㎃

1.7.6. AC Characteristics (Ta = 25℃)

Parameter	Symbol	Pin	Specification			Unit
			min.	typ.	max.	
External clock input cycle time	tCP	OSC	62.5	250	2500	ns
External clock input High	tCPH	OSC		0.5		tCP
External clock input Low	tCPL	OSC		0.5		tCP
System clock cycle time	tSYS	–		4		tCP
External pulse width High	tIH	EC0, EC1	1			tCP
External pulse width Low	tIL	EC0, EC1	1			tCP
Externa pulse width Low	tIL	RESETB	8			tSYS
Interrupt pulse width High	tIH	RESETB, KSCN, INT	2			tSYS
Interrupt pulse width Low	tIL	RESETB, KSCN, INT	2			tSYS

Minimum pulse width



2. Function Description

2.1. Program Memory

The ADAM43P1108 can address maximum 4Kbytes (2K words × 16bits) for program memory. Program counter PC (A0~A10) is used to address the whole area of program memory having an instruction (16bits) to be next executed.

The program memory consists of 2K words.

The program memory is composed as shown below.

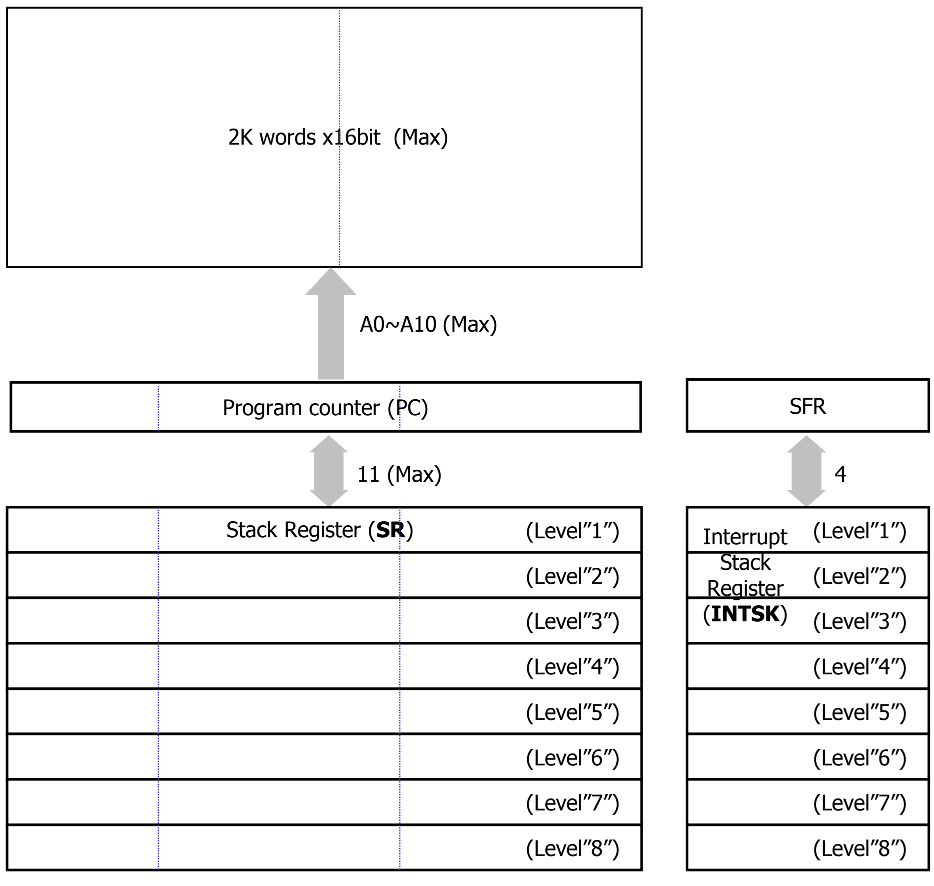


Fig.2.1 Configuration of Program Memory

2.2. Address Register

The following registers are used to address the ROM.

- **Program counter (PC) :**
  Available for addressing word on each page.
- **Stack register (SR) :**
  Stores returned-word address in the subroutine call mode.

2.2.1 Program counter :

This 11-bit binary counter increments for fetching a word to be addressed in the currently addressed page having an instruction to be next executed.
For easier programming, at turning on the power, the program counter is reset to the zero location(0000H). Then the program counter specifies the next address.
When BR, CAL or RET instructions are decoded, the switches on each step are turned off not to update the address. Then, for BR or CAL, address data are taken in from the instruction operands (A0 to A10), or for RET, and address including page address is fetched from stack register No. 1.

2.2.2. Stack register (SR)

The address stack register (ADS) stores a return address when the subroutine call instruction is executed or interrupt is acknowledged.
If subroutine or interrupts are nested to more than 8 levels, internal reset is occurred.
The interrupt stack register(INTSK) saves the contents of Status Flag Register (SFR) when an interrupt is acknowledged.
The saved contents are restored when an interrupt return(RETI) instruction is executed.
INTSK saves data each time an interrupt is acknowledged.
The programmer must keep in mind that the level of INTSK is 8. So, if more over 8 levels of interrupt occur, the first stored data is lost. There is different result between Stack overflow and interrupt stack overflow.
When clearing SP (Stack Pointer) with using “SPC” instruction, interrupt processing must be inhibited before “SPC”.

2.3. Data Memory (RAM)

128 nibbles (128 words × 4bits) is incorporated for storing data.

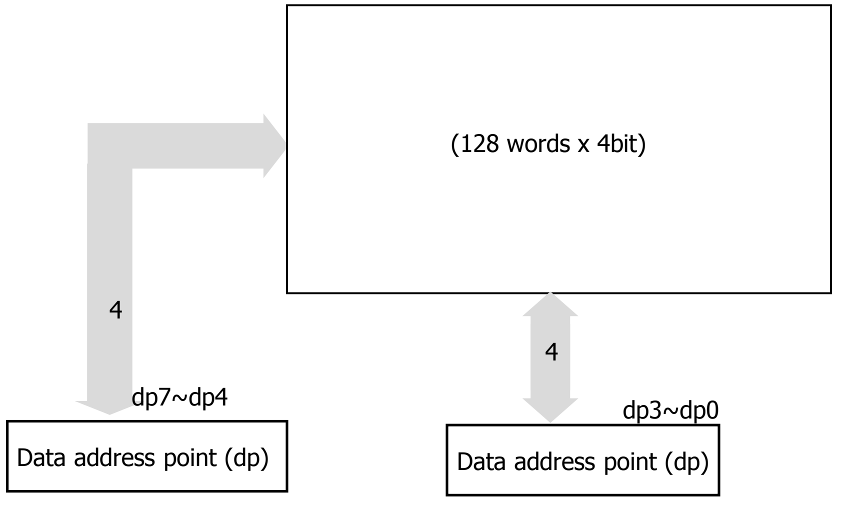
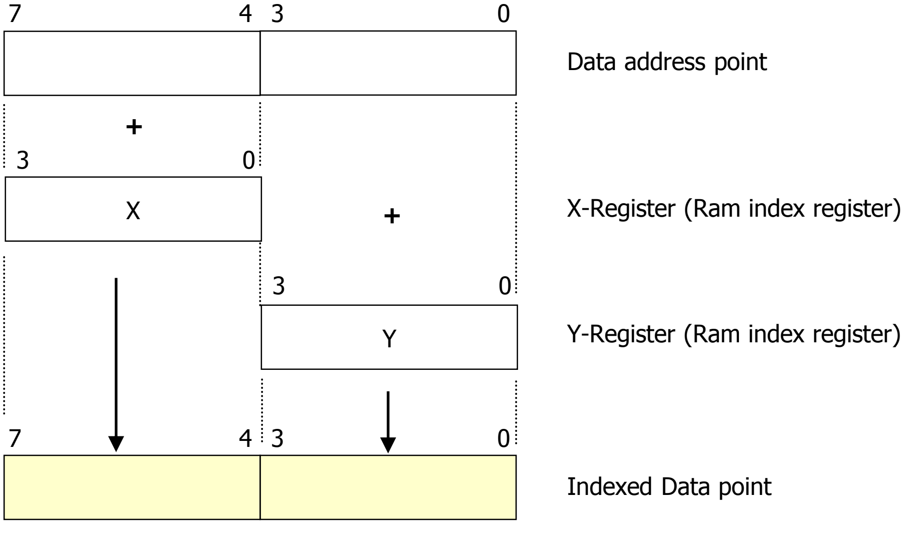


Fig.2.2 Data Memory

2.3.1. Data memory(RAM) addressing method

The whole data memory area is directly addressed by 8-bit ram data address point (dp).

Index data memory addressing is available using X-register and Y-register.
In this case, X-register is added upper 4bit of data point and Y-register is added lower 4bit of data point.



2.3.2. Data memory(RAM) data addressing example Program

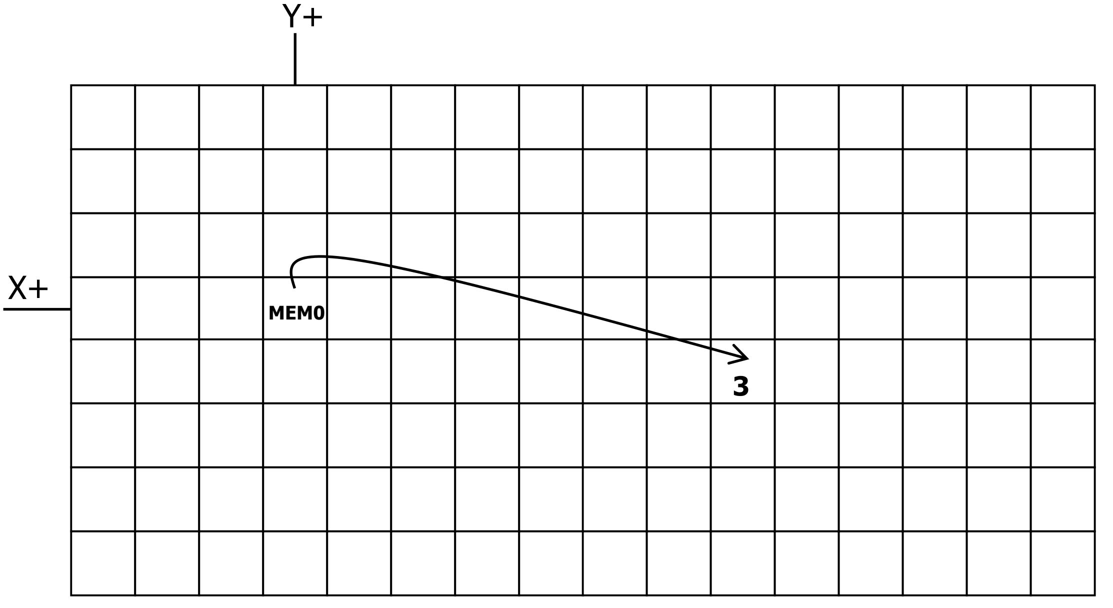


Fig.2.3 Data Memory Map

Program Example)

```
LDM     MEM0,#3h
LYI      #7
LXI      #1
LDA      MEM0
EIX
LDM     MEM0,A
DIX
```

Result after executing
; MEM0 = 3h
  MEM0 + X + Y = 3h

2.4. General Function Registers

2.4.1. X-register (X)

X-register is consist of 4bit, X-register is used for data memory indexing register.

2.4.2. Y-register (Y)

Y-register is consist of 4 bits. It can used for a general-purpose register.
Y-register also used for data memory indexing register.

2.4.3. Accumulator (ACC)

The 4-bit register for holding data and calculation results.

2.4.4. Peripheral Address Register(PAR)

The 6-bit address register for addressing peripheral registers including
address buff register(ABR) , data buff register (DBR).

2.4.5. Address Buff Register (ABR)

The 16-bit register for address buffer.
The address of Address Buffer Register (ABR) is 38h ~ 3Bh on the peripheral register.
It is composed by 4 registers (ABR0, ABR1, ABR2, ABR3) and each register is 4 bit.

2.5. Buffer Registers (DBR, ABR)

Buffer registers are two types of 16 bit registers composed of 4-ninbble registers.
One is Data Buffer Register (DBR) and the other is Address Buffer Register (ABR).
The address of Data Buffer Register (DBR) is 3Ch ~ 3Fh and the address of Address Buffer Register (ABR) is 38h ~ 3Bh on the peripheral register.
These buffers are mainly used for Data transferring between ROM and buffer or peripheral registers and buffer. They are also used for general purpose register for data manipulation, data storage and intermediate buffer.

2.5.1. Function of Address Buff Register (ABR)

The most important function of ABR is ROM address pointer.
ABR must be used for reading data from ROM. The data pointed by ABR is read to DBR.
ABR value is varied through peripheral control instruction and "INC ABR".

2.5.2. Function of Data Buff Register(DBR)

The most important function of DBR is intermediate (window) buffer for transferring data between peripheral registers and reading data from ROM.
When the data of ROM is read by "LDW @ABR", one word of ROM is fetched to DBR.
The MSB of ROM data is written to DBR3 and LSB to DBR0.
If the data of pointed ROM is 1234h, each DBR has the data as DBR0 = 4h, DBR1 = 3h, DBR2 = 2h and DBR3 = 1h.
DBR is also used for reading some peripheral register data by 12bit unit or 8bit unit.
The peripheral registers are T0CR and T1CR.

Note) HEX. File maps the data as big endian type. Be careful to read the ROM data.
When the programmer assigns the data like below, the ROM data is mapped as below.
DB 12h, 34h → ROM data = 1234h

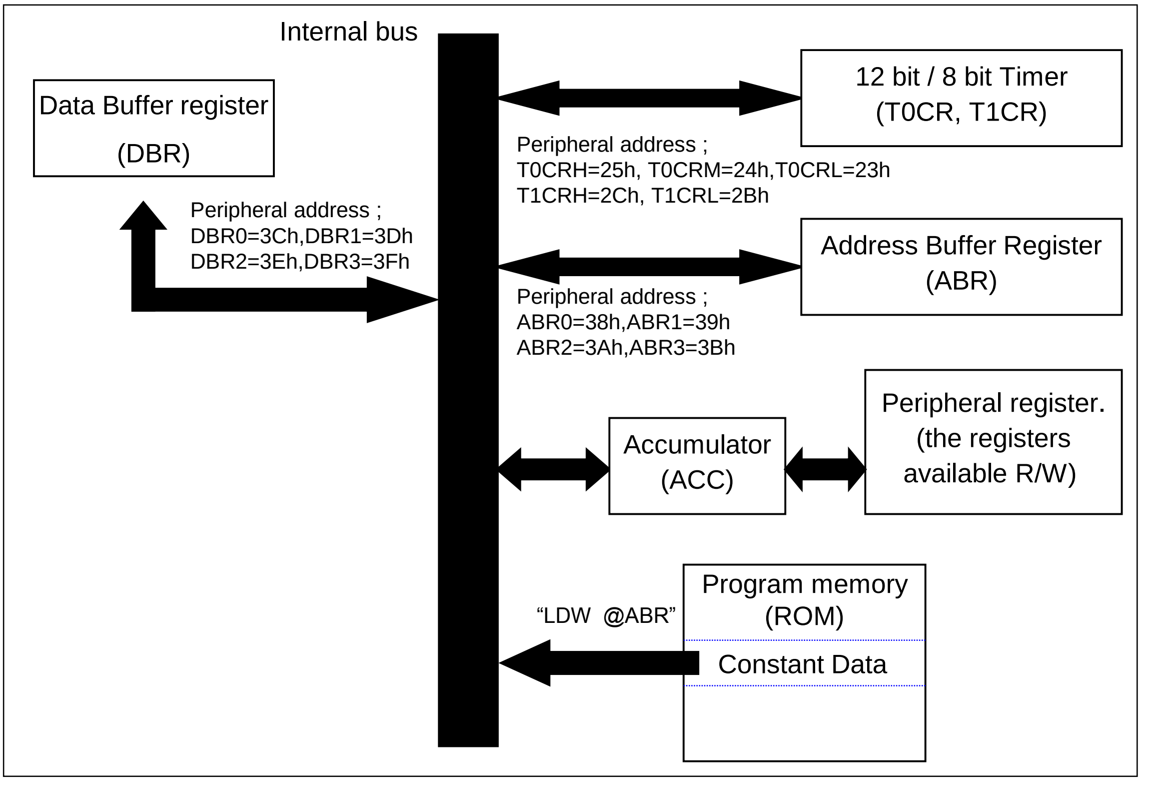


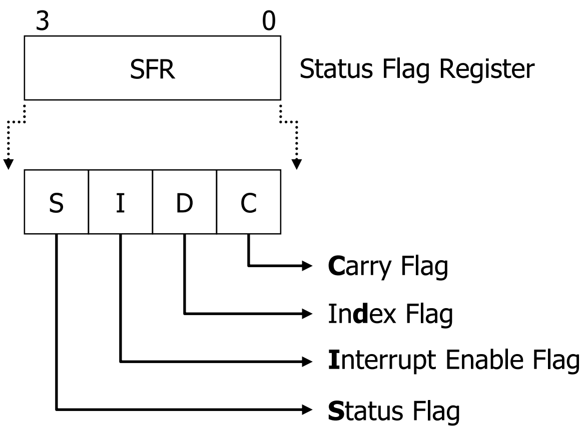
Fig.2.4 The internal Data flow among DBR, ABR registers and ROM

2.6. Status Flag Registers (SFR)

Status Flag Register (SFR) consists of 4-bit register.

Each of the flags show the post state of operation and the flags determining the CPU operation, initialized as 0h in reset state.

When an interrupt is occurred, the value of SFR keep the value of pre-interrupt except for I flag.
So, be careful to initialize the SFR status for getting reliable result in Interrupt sub-routine.



2.6.1 Carry flag (C)

- Carry flag bit is set when there is carry or borrow After executing ADDC / SUBC / ARRC/ARLC instructions.
- Set by SETC and clear by CLRC.
- Load from the assigned bit of Peripheral Registers by LDC
- Transfer to the assigned bit of Peripheral Registers by STC

2.6.2 Index flag (D)

- The control bit of ram data address point indexed or not.
- X-register and Y-register is used for index addressing.
- Set and cleared by EIX, DIX.

2.6.3 Interrupt enable flag (I)

- Master enable flag of interrupt.
- Set and cleared by EI, DI
- This Flag immediately becomes "0" when an interrupt is served.

2.6.4 Status flag (S)

- According to the condition after executing an instruction , set or clear.
- Can not be set or clear by any instruction.
- This Flag decides whether operation of BR and CALL would be done or not.

2.7. Peripheral Registers

Peripheral Address	Function Registers	Read Write	Symbol	RESET Value
				3 2 1 0
00 h	PORT PA DATA REG.	R/W	* PADR	F
01 h	PORT PA PULL-UP SELECTION REG.	W	PAPU	F
02 h	PORT PA OPEN DRAIN SELECTION REG.	W	PAOD	F
03 h	PORT PA DIRECTION REG.	R/W	PADD	0
04 h	PORT PA STOP RELEASE SELECTION REG.	W	PAST	F
05 h	PORT PA FUNCTION SELECTION REG. LOW	R/W	PAFL	0
06 h	PORT PA FUNCTION SELECTION REG. HIGH	R/W	PAFH	0
07 h	PORT PA CURRENT DRIVING CONTROL REG.	W	PACD	0
08 h	PORT PB DATA REG.	R/W	* PBDR	F
09 h	PORT PB PULL-UP SELECTION REG.	W	PBPU	F
0A h	PORT PB OPEN DRAIN SELECTION REG.	W	PBOD	F
0B h	PORT PB DIRECTION REG.	R/W	PBDD	0
0C h	PORT PB STOP RELEASE SELECTION REG.	W	PBST	F
0D h	PORT PB FUNCTION SELECTION REG. LOW	R/W	PBFL	0
0E h	PORT PB FUNCTION SELECTION REG. HIGH	R/W	PBFH	0
0F h	PORT PB CURRENT DRIVING CONTROL REG.	W	PBCD	0
10 h	*Reserved*			
11 h	*Reserved*			
12 h	*Reserved*			
13 h	*Reserved*			
14 h	*Reserved*			
15 h	*Reserved*			
16 h	*Reserved*			
17 h	*Reserved*			
18 h	*Reserved*			
19 h	*Reserved*			
1A h	EXT. INTERRUPT EDGE SELECTION REG.	W	IEDS0	0
1B h	KEY SCAN INTERRUPT EDGE SELECTION REG.	W	IEDS1	0
1C h	INTERRUPT REQUEST FLAG REG. 0	R/W	IRQR0	0
1D h	INTERRUPT REQUEST FLAG REG. 1	R/W	IRQR1	0
1E h	INTERRUPT ENABLE REG. 0	R/W	IENR0	0
1F h	INTERRUPT ENABLE REG. 1	R/W	IENR1	0

Note1> * Using the bit access Instruction, bit is read-modified operation (SETR1/CLRR1/STC Instructions)

2. Function Description

Peripheral Address	Function Registers	Read Write	Symbol	RESET Value 3 2 1 0
20 h	TIMER 0 MODE REG. 0	R/W	T0MR0	0
21 h	TIMER 0 MODE REG. 1	R/W	T0MR1	0
22 h	TIMER 0 MODE REG. 2	R/W	T0MR2	0
23 h	TIMER 0 DATA 0 LOW REG.(PWM0 DUTY LSB)	W	T0D0L	undefined
	TIMER 0 COUNT REG. LOW	R	T0CRL	undefined
24 h	TIMER 0 DATA 0 MIDDLE REG.(PWM0 DUTY MSB)	W	T0D0M	undefined
	TIMER 0 COUNT REG. MIDDLE	R	T0CRM	undefined
25 h	TIMER 0 DATA 0 HIGH REG.(PWM0 DUTY EXTENSION)	W	T0D0H	undefined
	TIMER 0 COUNT REG. HIGH	R	T0CRH	undefined
26 h	TIMER 0 DATA 1 LOW REG.(PWM0 PERIOD LSB)	W	T0D1L	undefined
27 h	TIMER 0 DATA 1 MIDDLE REG.(PWM0 PERIOD MSB)	W	T0D1M	undefined
28 h	TIMER 0 DATA 1 HIGH REG.(PWM0 CYCLE)	W	T0D1H	undefined
29 h	TIMER 1 MODE REG. 0	R/W	T1MR0	0
2A h	TIMER 1 MODE REG. 1	R/W	T1MR1	0
2B h	TIMER 1 DATA 0 LOW REG.(PWM1 DUTY)	W	T1D0L	undefined
	TIMER 1 COUNT REG. LOW	R	T1CRL	undefined
2C h	TIMER 1 DATA 0 HIGH REG.(PWM1 DUTY EXTENSION)	W	T1D0H	undefined
	TIMER 1 COUNT REG. HIGH	R	T1CRH	undefined
2D h	TIMER 1 DATA 1 LOW REG.(PWM1 PERIOD)	W	T1D1L	undefined
2E h	TIMER 1 DATA 1 HIGH REG.(PWM1 CYCLE)	W	T1D1H	undefined
2F h	TIMER MODULATION CONTROL REG.	W	TMCR	F
30 h	*Reserved*			
31 h	*Reserved*			
32 h	WATCH-DOG TIMER CONTROL REG.	W	WDTCR	1 0 0 0
33 h	VTG. DETECTION INDICATOR ENABLE REG.	W	VDIER	0
	VTG DETECTION INDICATOR FLAG REG.	R	VDIR	- 0 0 0
34 h	A/D CONVERTER MODE REG. 0	R/W	ADCM0	0 0 0 1
35 h	A/D CONVERTER MODE REG. 1	W	ADCM1	0
	A/D CONVERTER DATA REG. 0	R	ADCR0	undefined
36 h	A/D CONVERTER INPUT SELECTION REG.	W	ADCIS	0
	A/D CONVERTER DATA REG. 1	R	ADCR1	undefined
37 h	A/D CONVERTER DATA REG. 2	R	ADCR2	undefined
38 h	ADDRESS BUFF REGISTER 0	R/W	ABR0	undefined
39 h	ADDRESS BUFF REGISTER 1	R/W	ABR1	undefined
3A h	ADDRESS BUFF REGISTER 2	R/W	ABR2	undefined
3B h	ADDRESS BUFF REGISTER 3	R/W	ABR3	undefined
3C h	DATA BUFF REGISTER 0	R/W	DBR0	undefined
3D h	DATA BUFF REGISTER 1	R/W	DBR1	undefined
3E h	DATA BUFF REGISTER 2	R/W	DBR2	undefined
3F h	DATA BUFF REGISTER 3	R/W	DBR3	undefined

Note1> '-' is reserved bit , it must be read to "0".

3. I/O Ports

The ADAM43 has 6 I/O ports which are PA (3 I/O), PB (3 I/O).
PA and PB Port have Stop Release selection register.
Pull-up resistor of PA and PB ports can be selectable by program.
Pull-down resistor of PB2 and PB3 ports can be selectable by program.
PA and PB ports contains data direction register which controls I/O and data register which stores port data.
PA, PB2 and PB3 Ports have Open Drain selection register and Data register.

PB1 is Open Drain output only.

I/O Ports Registers

Port	Data Reg.	Pull-up Reg.	Open-Drain Reg.	Direction Reg.	Stop Release Reg.
port PA	PA	PAPU	PAOD	PADD	PAST
port PB	PB	PBPU	PBOD	PBDD	PBST

R/W	R/W	W	W	R/W	W
Initial value	1111	-111	-111	0000	-111
default	fh	disable	disable	input	disable

Port	Function Reg.	Current Driving Reg.
port PA	PAFH/PAFL	PACD
port PB	PBFH/PBFL	PBCD

R/W	R/W	W
Initial value	0000	-000
default	disable	disable

3. I/O Ports

3.1. Port PA

Pin Name	Port Selection	Function Selection
PA0/AN0/EC0 INT0/TMA/KSA0	PA0 (I/O)	AN0 Input / Event Count-0 input / INT0 Input / Timer0/1 Logic Output / KSA0 Input
PA1/AN1/EC1/INT1/KSA1	PA1 (I/O)	AN1 Input / Event Count-1 input / INT1 Input / KSA1 Input
PA2/AN2/*EC0/*INT0/PWM0/KSA2	PA2 (I/O)	AN2 Input / Event Count-2 input / INT0 Input / PWM0 Output / KSA2 Input

3.1.1. PA Data Register (PA)

bit	3	2	1	0	
PA	-	PA2	PA1	PA0	00h
Initial value	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	

PA data register (PA) is 4-bit register to store data of port PA.
When set as the output state by PA, and data is written in PA, data is outputted into PA pin.
When set as the input state, input state of pin is read. The initial value of PA is "Fh" in reset state.
At output state, if port PA is read, PA Data Register is read instead of port PA.

3.1.2. PA Pull-up Resistor Control Register (PAPU)

bit	3	2	1	0	
PAPU	-	PAPU2	PAPU1	PAPU0	01h
Initial value	-	1	1	1	
R/W	W	W	W	W	

PA pull-up resistor control register (PAPU) is 4-bit register and can control pull-up on or off each bit, if corresponding port is selected as input. If PAPU is selected as "0", pull-up is enabled and if selected as "1", it is disabled. PAPC is write-only register and initialized as "Fh" in reset state. The pull-up is automatically disabled, if corresponding port is selected as output.

3.1.3. PA Open Drain Assign Register (PAOD)

bit	3	2	1	0	
PAOD	-	PAOD2	PAOD1	PAOD0	02h
Initial value	-	1	1	1	
R/W	W	W	W	W	

PA Open Drain Assign Register (PAOD) is 4-bit register, and can assign PA port as open drain output port each bit If PAOD is selected as "0", port PA is open drain output, and if selected as "1", it is push-pull output. PAOD is write-only register and initialized as "Fh" in reset state.

3.1.4. PA I/O Data Direction Register (PADD)

bit	3	2	1	0	
PADD	-	PADD2	PADD1	PADD0	03h
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

PA I/O Data Direction Register (PADD) is 4-bit register, and can assign input state or output state to each bit. If PADD is "0", port PA is in the input state, and if "1", it is in the output state. Since PADD is initialized as "0h" in reset state, the whole port PA becomes input state.

3.1.5. PA Stop Release Selection Register (PAST)

bit	3	2	1	0	
PAST	-	PAST2	PAST1	PAST0	04h
Initial value	-	1	1	1	
R/W	W	W	W	W	

PA Stop Release Selection Register (PAST) is 4-bit register, and can assign stop release pin or not. If PAST is selected as "0", stop release function is enabled and if selected as "1", it is disabled. PAST is write-only register and initialized as "Fh" in reset state.

3.1.6. PA Function Selection Register (PAFL)

bit	3	2	1	0	
PAFL	PA1		PA0		05h
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

3.1.7. PA Function Selection Register (PAFH)

bit	3	2	1	0	
PAFH	-		PA2		06h
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of PAFL

Bit Name	Selection Mode		Remarks
PA1	00	I/O	
	01	ADC selection	AN1
	10	Interrupt selection	INT1(EC1)
	11	AVREF selection	VREF
PA0	00	I/O	
	01	ADC selection	AN0
	10	Interrupt selection	INT0(EC0)
	11	Tout selection	TMA

Selection Mode of PAFH

Bit Name	Selection Mode		Remarks
–	00	–	
	01	–	
	10	–	
	11	–	
PA2	00	I/O	
	01	ADC selection	AN2
	10	Interrupt selection	*INT0(EC0)
	11	Tout selection	PWM0

3.1.8. PA Current Driving Control Register (PACD)

bit	3	2	1	0	
PACD	-	PACD2	PACD1	PACD0	07h
Initial value	-	0	0	0	
R/W	W	W	W	W	

PA Current Driving Control Register (PACD) is 4-bit register, and can enhance current drive capacity. If PACD is selected as "1", current driving control function is enabled and if selected as "0", it is disabled. PACD is write-only register and initialized as "0h" in reset state.

3.2. Port PB

Pin Name	Port Selection	Function Selection
PB1/PWM0/RESETB/KSB1	PB1 (I/O)	PWM0 Output / RESETB Input / KSB1 Input
PB2/AN6/PWM1/KSB2	PB2 (I/O)	AN6 Input / PWM1 Output / KSB2 Input
PB3/AN7/TMB/KSB3	PB3 (I/O)	AN7 Input / Timer0/1 Logic Output / KSB3 Input

3.2.1. PB Data Register (PB)

bit	3	2	1	0	
PB	PB3	PB2	PB1	-	08h
Initial value	1	1	1	1	
R/W	R/W	R/W	R/W	R/W	

PB data register (PB) is 4-bit register to store data of port PB.
When set as the output state by PB, and data is written in PB, data is outputted into PB pin.
When set as the input state, input state of pin is read. The initial value of PB is "Fh" in reset state.
At output state, if port PB is read, PB Data Register is read instead of port PB.

3.2.2. PB Pull-up Resistor Control Register (PBPU)

bit	3	2	1	0	
PBPU	PBPU3	PBPU2	PBPU1	-	09h
Initial value	1	1	1	-	
R/W	W	W	W	W	

PB pull-up resistor control register (PBPU) is 4-bit register and can control pull-up on or off each bit, if corresponding port is selected as input. If PBPC is selected as "0", pull-up is enabled and if selected as "1", it is disabled. PBPU is write-only register and initialized as "Fh" in reset state. The pull-up is automatically disabled, if corresponding port is selected as output.

3.2.3. PB Open Drain Assign Register (PBOD)

bit	3	2	1	0	
PBOD	PBOD3	PBOD2	PBOD1	-	0Ah
Initial value	1	1	1	-	
R/W	W	W	W	W	

PB Open Drain Assign Register (PBOD) is 4-bit register, and can assign PB port as open drain output port each bit If PBOD is selected as "0", port PB is open drain output, and if selected as "1", it is push-pull output. PBOD is write-only register and initialized as "Fh" in reset state.

3.2.4. PB I/O Data Direction Register (PBDD)

bit	3	2	1	0	
PBDD	PBDD3	PBDD2	PBDD1	-	0Bh
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

PB I/O Data Direction Register (PBDD) is 4-bit register, and can assign input state or output state to each bit. If PBDD is "0", port PB is in the input state, and if "1", it is in the output state. Since PBDD is initialized as "0h" in reset state, the whole port PB becomes input state.

3.2.5. PB Stop Release Selection Register (PBST)

bit	3	2	1	0	
PBST	PBST3	PBST2	PBST1	-	0Ch
Initial value	1	1	1	-	
R/W	W	W	W	W	

PB Stop Release Selection Register (PBST) is 4-bit register, and can assign stop release pin or not. If PBST is selected as "0", stop release function is enabled and if selected as "1", it is disabled. PBST is write-only register and initialized as "Fh" in reset state.

3.2.6. PB Function Selection Register (PBFL)

bit	3	2	1	0	
PBFL	PB1		-		0Dh
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

3.2.7. PB Function Selection Register (PBFH)

bit	3	2	1	0	
PBFH	PB3		PB2		0Eh
Initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of PBFL

Bit Name	Selection Mode		Remarks
PB1	00	I/O	
	01		
	10		
	11	Tout selection	PWM0
–	00	–	
	01	–	
	10	–	
	11	–	

Selection Mode of PBFH

Bit Name	Selection Mode		Remarks
PB3	00	I/O	
	01	ADC selection	AN7
	10	Pull–down selection	
	11	Tout selection	TMB
PB2	00	I/O	
	01	ADC selection	AN6
	10	Pull–down selection	
	11	Tout selection	PWM1

3.2.8. PB Current Driving Control Register (PBCD)

bit	3	2	1	0	
PBCD	PBCD3	PBCD2	PBCD1	-	0Fh
Initial value	0	0	0	-	
R/W	W	W	W	W	

PB Current Driving Control Register (PBCD) is 4-bit register, and can enhance current drive capacity. If PBCD is selected as "1", current driving control function is enabled and if selected as "0", it is disabled. PBCD is write-only register and initialized as "0h" in reset state.

4. Oscillation Circuit

4.1. Oscillation Circuit

Oscillation circuit is designed to be used either with a ceramic or crystal oscillator.
Clock from oscillation circuit makes CPU clock via clock pulse generator, and then provide peripheral hardware clock.

There are 5 types of Oscillation circuit and they can be divided in 8 different oscillator option modes. The user can used OTP Configuration Option Bits (OSCS2 through OSCS0) to select one of these 5 types. Refer to Table 4.1.

- XT : Crystal (Ceramic) Oscillator
- LP : 32.768kHz Crystal Oscillator
- ERC : External RC Oscillator
- ECKIN : External Clock Input
- IRC : Internal RC Oscillator (4 modes)

First type is Crystal (Ceramic) oscillator circuit. OSC1 and OSC2 are the input and output, respectively, a inverting amplifier which can be set for use as an on-chip oscillator. It is designed to be used either with a ceramic resonator or crystal oscillator. In the STOP mode, oscillation stop, OSC2 state goes to "High", OSC1 state goes to "Low", and built-in feedback resistor is disabled. Second type is 32.768kHz Ceramic oscillator circuit. It operate same as the first type.

Third type is External clock input circuit. Through the OSC1, external clock is driven. Minimum and maximum high and low times specified on the data sheet must be observed. OSC2/PB2 is selectable the normal I/O port PB2. In STOP mode, OSC1 state does not go to "Low", and external clock does not affect to Internal.

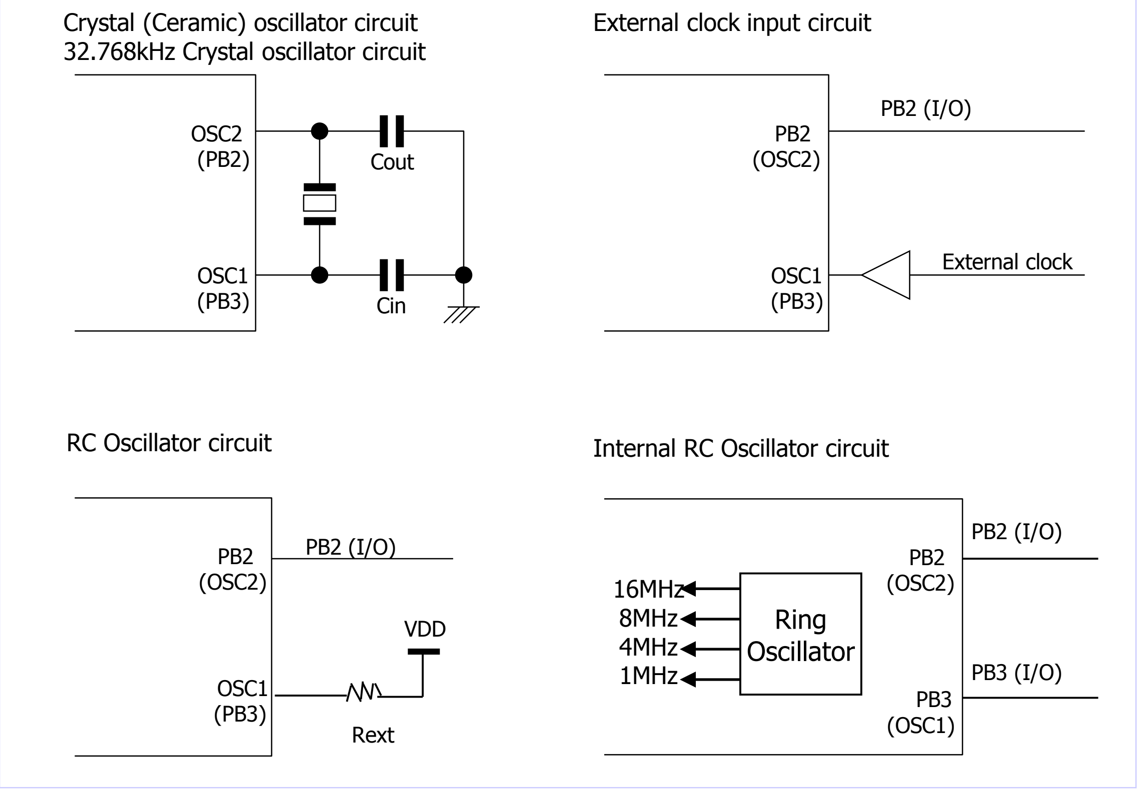


Fig.4.1 Oscillator configurations

Another type is RC oscillation circuits. It can be constructed by connecting a resistor between OSC1 and VDD. It offers additional cost savings for timing insensitive applications. The RC oscillator frequency is a function of the supply voltage, the external resistor (Rext) value, and the operating temperature. The user needs to take into account variation due to tolerance of external R components used. In STOP mode, OSC1 state goes to "Hi-Z" and RC Oscillation is stopped.

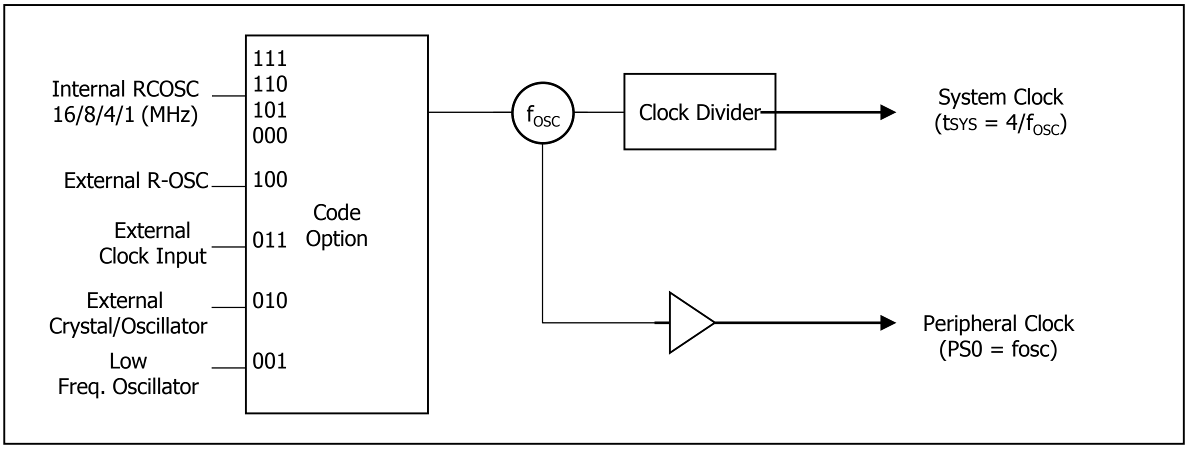
The other type is Internal RC Oscillator circuit. In this type, OSC1/PB3 is used the normal I/O port PB3, OSC2/PB2 is selectable the normal I/O port PB2. The Internal Oscillator is calibrated in Factory. In STOP mode, Internal RC oscillator is stopped.

Below table shows the selection of the oscillator type by OTP Configuration Option Bits (Address 8000h, OSCS2 ~ OSCS0). (Refer to 14.2. Configuration Option Bit Description)

Table. 4.1 Oscillator Type and Modes Selection

OSCS[2:0]			Oscillator Modes	OSC1	OSC2
OSCS[2]	OSCS[1]	OSCS[0]			
1	1	1	Internal RC 4MHz	PB3 (I/O)	PB2 (I/O)
1	1	0	Internal RC 8MHz	↑	↑
1	0	1	Internal RC 16MHz	↑	↑
1	0	0	External RC Oscillator	OSC1 (I)	PB2 (I/O)
0	1	1	External Clock Input	OSC1 (I)	PB2 (I/O)
0	1	0	XT Oscillator	OSC1 (I)	OSC2 (O)
0	0	1	Low Frequency Oscillator	OSC1 (I)	OSC2 (O)
0	0	0	Internal RC 1MHz	PB3 (I/O)	PB2 (I/O)

4.2. System Clock & Peripheral Clock Generator Block Diagram



Peripheral Clock	PS0/2	PS0	PS1	PS2	PS3	PS4	---	PS10	PS11
Frequency [MHz]	$f_{OSC} * 2$	$f_{OSC}/2^0$	$f_{OSC}/2^1$	$f_{OSC}/2^2$	$f_{OSC}/2^3$	$f_{OSC}/2^4$	---	$f_{OSC}/2^{10}$	$f_{OSC}/2^{11}$
Period [us] (at fosc=4MHz)	0.125	0.25	0.5	1.0	2.0	4.0	---	256	512

5. Watch Dog Timer

5.1. Watch Dog Timer (WDT)

Watch dog timer is organized binary of 19 steps. The signal of $f_{OSC}/4$ cycle comes in the first step of WDT after WDT reset. If this counter was overflowed, reset signal automatically come out so that internal circuit is initialized. The overflow time is initially $2^{18} \times 4/f_{OSC}$ (262.144ms at f_{OSC} = 4.0MHz), it is selectable by WDT Control Register (WDTCR). Normally, the binary counter must be reset before the overflow by using reset instruction (WDTC), Power-on reset pulse or Low VDD detection pulse. It is constantly reset in STOP and SLEEP mode. When STOP and SLEEP are released, counting is restarted.
If it's executed the STOP instruction after setting the bit RWDTEN of WDTCR to "1", the Internal RC-Ring Oscillated Watch-dog Timer (RCWDT) mode is activated.

5.1.1. WDT Control Register

bit	3	2	1	0	
WDTCR	WDTRST	RWDTEN	WDTCK1	WDTCK0	*32h*
Initial value	1	0	0	0	
R/W	W	W	W	W	

WDTRST	0	WDT interrupt enable, when WDT Overflow is occurred.
	1	System Reset enable, when WDT Overflow is occurred. (default)
RWDTEN	0	RCWDT mode disable (fosc/4 selected)
	1	RCWDT Oscillator Enable & RCWDT mode enable
WDTCK1 & WDTCK0	00	WDT Overflow Time is 2^{18} x Tck
	01	WDT Overflow Time is 2^{17} × Tck
	10	WDT Overflow Time is 2^{16} × Tck
	11	WDT Overflow Time is 2^{15} × Tck

<u>Reset or Interrupt Wakeup Time (Example)</u>

	Tck * 2^{18}	Tck * 2^{17}	Tck * 2^{16}	Tck * 2^{15}	Unit
Tck = 1us	262.144	131.072	65.536	32.768	ms
Tck = 8us	2,097.152	1,048.076	524.288	262.144	
Tck = 16us	4,194.304	2,097.152	1,048.076	524.288	

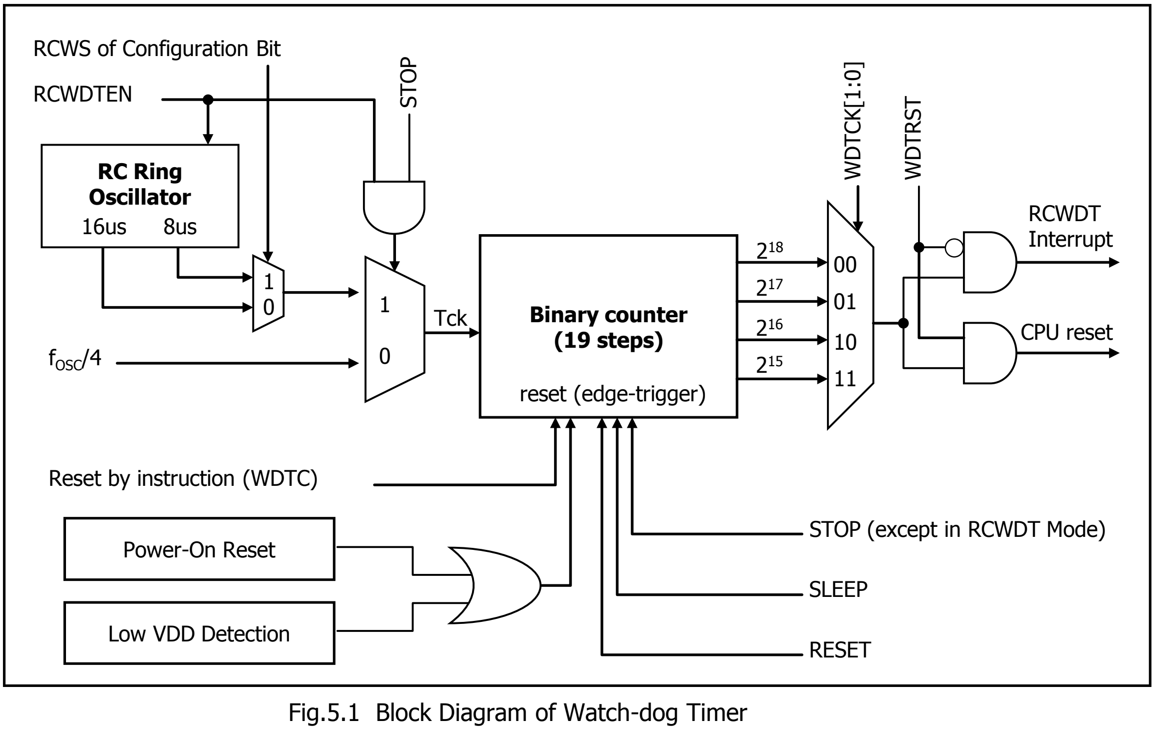


Fig.5.1 Block Diagram of Watch-dog Timer

6. Timer

6.1. Timer

6.1.1. Timer operation mode

Timer is basically made of Timer Data Register, Timer Mode Register and control circuit. The types of Timer are 12bit binary counter Timer0 (T0), 8bit binary counter Timer1 (T1).

Timer0 Data Register consists of Timer0 Data 0 High Register (T0D0H), Timer0 Data 0 Middle Register (T0D0M), Timer0 Data 0 Low Register (T0D0L), Timer0 Data 1 High Register (T0D1H), Timer0 Data 1 Middle Register (T0D1M) and Timer0 Data 1 Low Register (T0D1L).

Timer1 Data Register consists of Timer1 Data 0 High Register (T1D0H), Timer1 Data 0 Low Register (T1D0L), Timer1 Data 1 High Register (T1D1H) and Timer1 Data 1 Low Register (T1D1L).

Timer0	-. 12-bit Interval Timer -. 12-bit Event Counter -. 12-bit Capture Timer -. 12-bit rectangular-wave output -. (8 + 4) Pulse Width Modulation output
Timer1	-. 8-bit Interval Timer -. 8-bit Event Counter -. 8-bit Capture Timer -. 8-bit rectangular-wave output -. (6 + 2) Pulse Width Modulation output

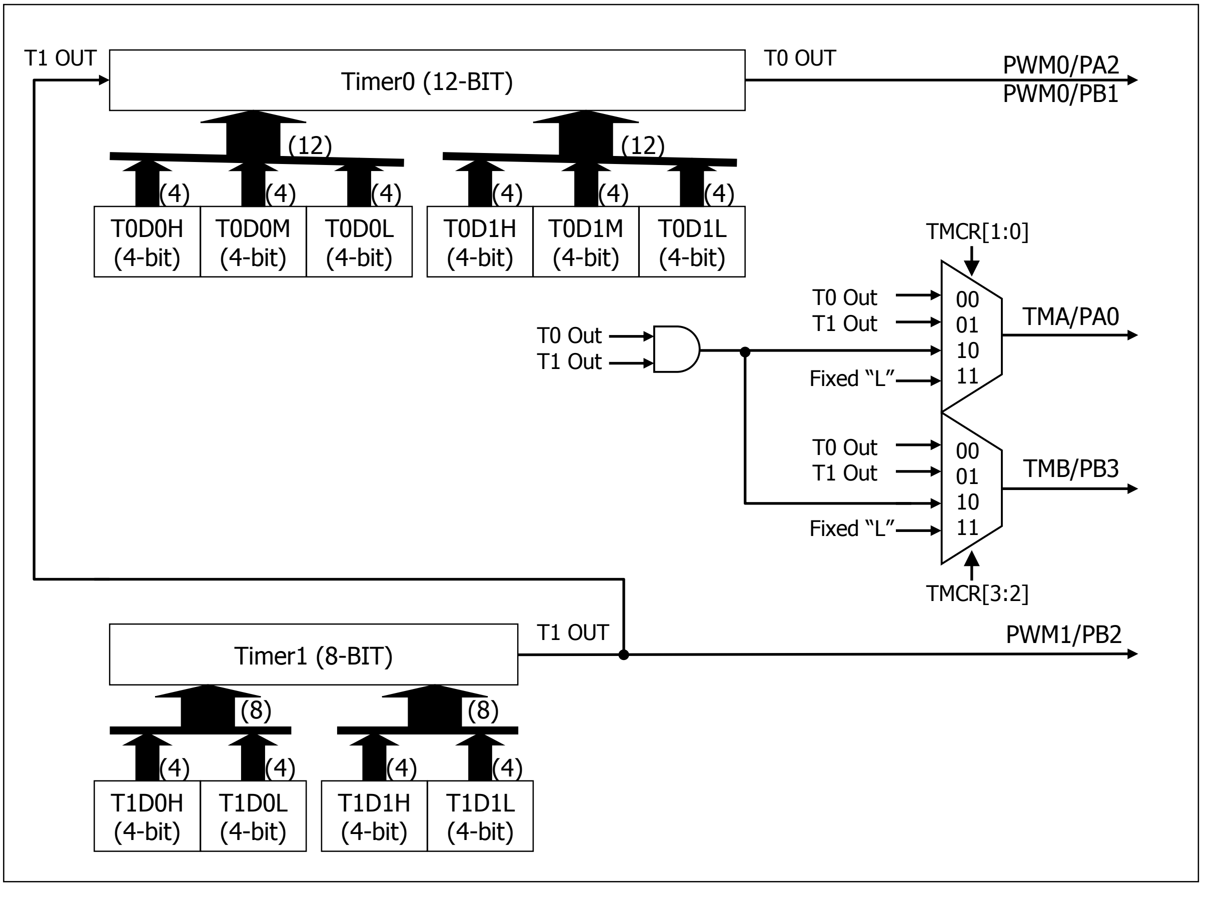
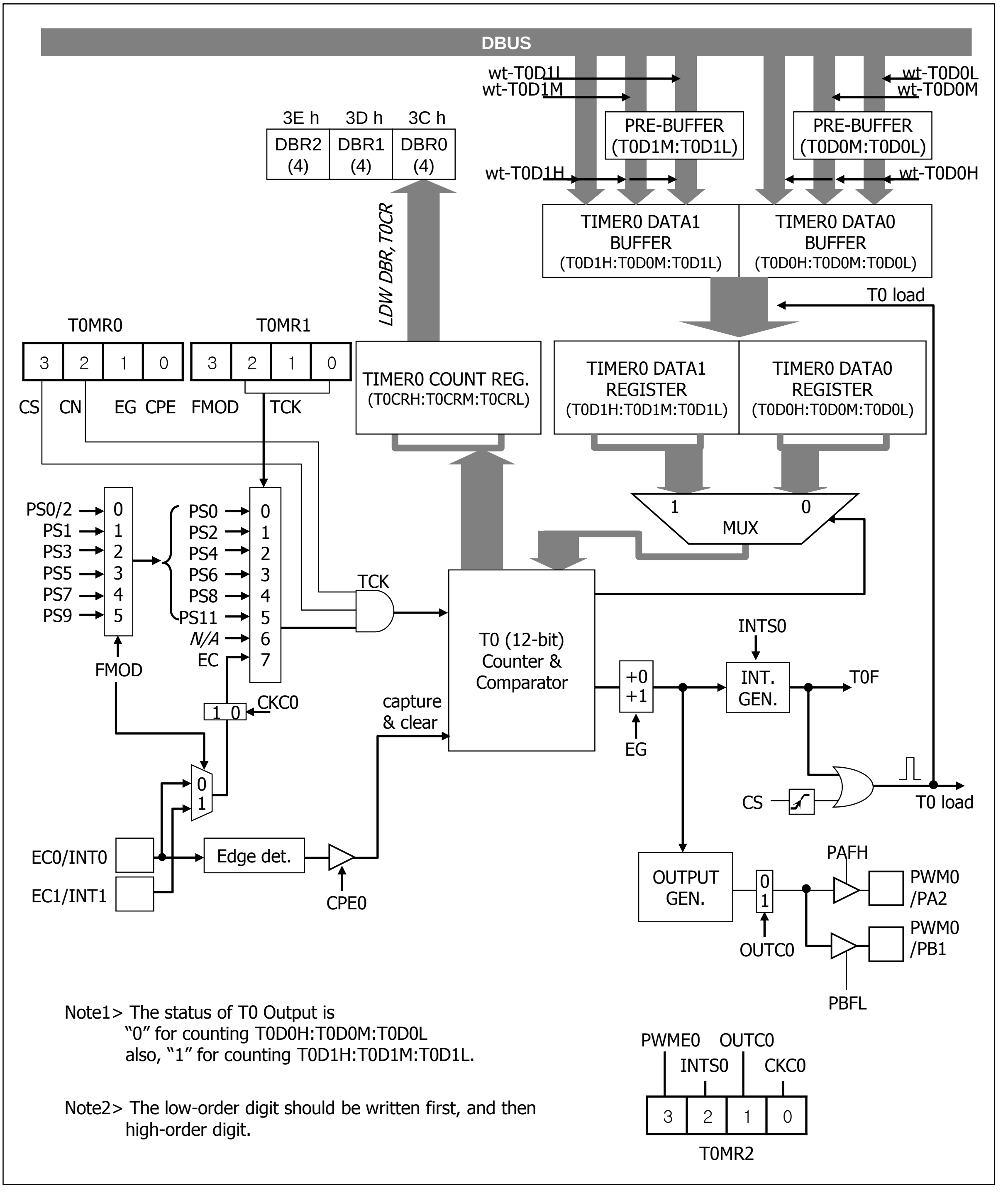


Fig.6.1 Timer/Counter Block diagram

6.2. Timer0

6.2.1. Timer0(T0) Block Diagram



6.2.2. Timer0 Control Register

• Timer0 Mode Register 0 (T0MR0)

	3	2	1	0	
T0MR0	T0CS	T0CN	T0EG	T0CPE	20h
initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of T0MR0

Bit Name			Selection Mode	Remarks
T0CS	Timer0 Clear / start Control	0	Timer0 Stop	
		1	Timer0 Clear and Start	
T0CN	Timer0 Pause / Continue Control	0	Timer0 Pause	
		1	Timer0 continue	
T0EG	Timer0 Count Control	0	Timer0 Count	
		1	Timer0 Count + 1	
T0CPE	Input capture Mode selection	0	Timer/Counter Mode	
		1	Capture Mode	

• Timer0 Mode Register 1 (T0MR1)

	3	2	1	0	
T0MR1	FMODE	T0CK2	T0CK1	T0CK0	21h
initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of T0MR1

Bit Name			Selection Mode		Remarks
FMODE	Input clock selection master bit		0	1	
T0CK2 T0CK1 T0CK0	Input clock selection	000	PS0 ($f_{OSC}/2^0$)	*PS0/2 (f_{OSC}*2)	
		001	PS2 ($f_{OSC}/2^2$)	PS1 ($f_{OSC}/2^1$)	
		010	PS4 ($f_{OSC}/2^4$)	PS3 ($f_{OSC}/2^3$)	
		011	PS6 ($f_{OSC}/2^6$)	PS5 ($f_{OSC}/2^5$)	
		100	PS8 ($f_{OSC}/2^8$)	PS7 ($f_{OSC}/2^7$)	
		101	PS11 ($f_{OSC}/2^{11}$)	PS9 ($f_{OSC}/2^9$)	
		110	*Not Available*		
		111	EC0	EC1	

Caution : PS0/2 must be used only in the case of fosc ≤ 4.0MHz

• Timer0 Mode Register 2 (T0MR2)

	3	2	1	0	
T0MR2	PWME0	INTS0	OUTC0	CKC0	22h
initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of T0MR2

Bit Name			Selection Mode	Remarks
PWME0	Timer/PWM Mode Selection	0	Timer0 Normal Mode	
		1	Timer0 PWM Mode	
INTS0	Timer0 Interrupt Overflow Control	0	Timer0 Interrupt Every 2nd Overflow	
		1	Timer0 Interrupt Every Overflow	
OUTC0	Timer0 Output Control	0	Timer0 Output Normal	
		1	Timer0 Output Reverse	
CKC0	Timer0 Event Counter Input Control	0	Timer0 Event counter Input Clock Normal	
		1	Timer0 Event counter Input Clock Reverse	

• Timer0 Data0 Register Low (T0D0L)
= PWM0 DUTY LSB

	3	2	1	0	
T0D0L	T0D0L3	T0D0L2	T0D0L1	T0D0L0	23h
initial value	–	–	–	–	
R/W	W	W	W	W	

• Timer0 Data0 Register Middle (T0D0M)
= PWM0 DUTY MSB

	3	2	1	0	
T0D0M	T0D0L3	T0D0L2	T0D0L1	T0D0L0	24h
initial value	–	–	–	–	
R/W	W	W	W	W	

• Timer0 Data0 Register High (T0D0H)
= PWM0 DUTY EXTENSION

	3	2	1	0	
T0D0H	T0D0H3	T0D0H2	T0D0H1	T0D0H0	25h
initial value	–	–	–	–	
R/W	W	W	W	W	

• Timer0 Count Register Low (T0CRL)

	3	2	1	0	
T0CRL	T0CRL3	T0CRL2	T0CRL1	T0CRL0	23h
initial value	–	–	–	–	
R/W	R	R	R	R	

• Timer0 Count Register Middle (T0CRM)

	3	2	1	0	
T0CRM	T0CRM3	T0CRM2	T0CRM1	T0CRM0	24h
initial value	–	–	–	–	
R/W	R	R	R	R	

• Timer0 Count Register High (T0CRH)

	3	2	1	0	
T0CRH	T0CRH3	T0CRH2	T0CRH1	T0CRH0	25h
initial value	–	–	–	–	
R/W	R	R	R	R	

• Timer0 Data1 Register Low (T0D1L)
= PWM0 PERIOD LSB

	3	2	1	0	
T0D1L	T0D1L3	T0D1L2	T0D1L1	T0D1L0	26h
initial value	–	–	–	–	
R/W	W	W	W	W	

• Timer0 Data1 Register Middle (T0D1M)
= PWM0 PERIOD MSB

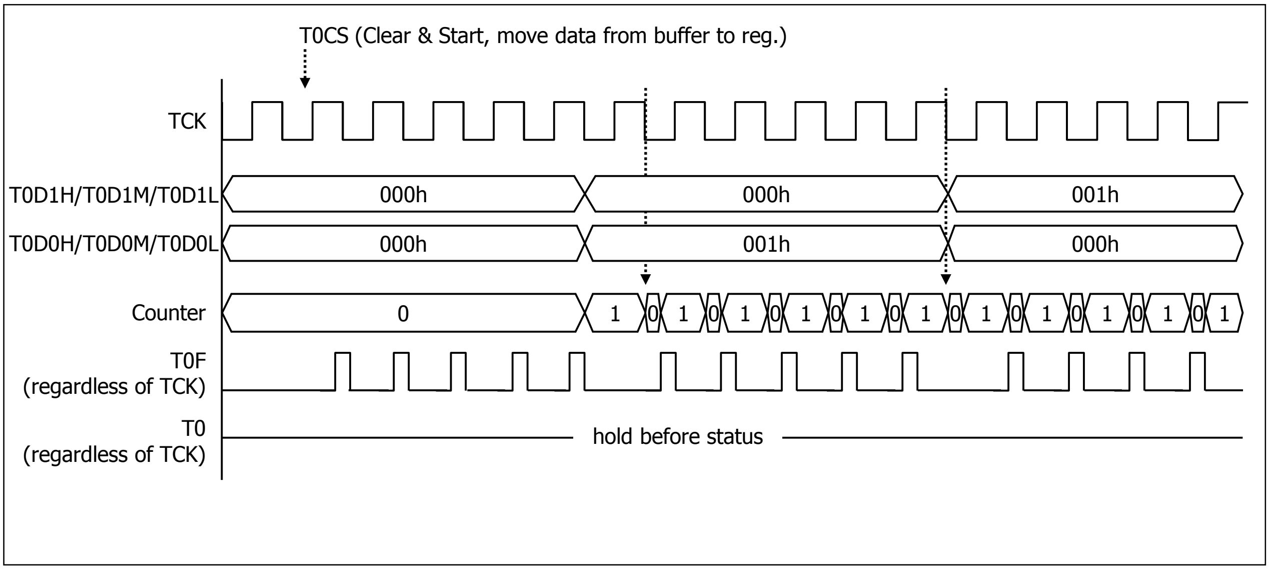
	3	2	1	0	
T0D1M	T0D1L3	T0D1L2	T0D1L1	T0D1L0	27h
initial value	–	–	–	–	
R/W	W	W	W	W	

• Timer0 Data1 Register High (T0D1H)
= PWM0 CYCLE

	3	2	1	0	
T0D1H	T0D1H3	T0D1H2	T0D1H1	T0D1H0	28h
initial value	–	–	–	–	
R/W	W	W	W	W	

6.2.3. Timer0 Caution

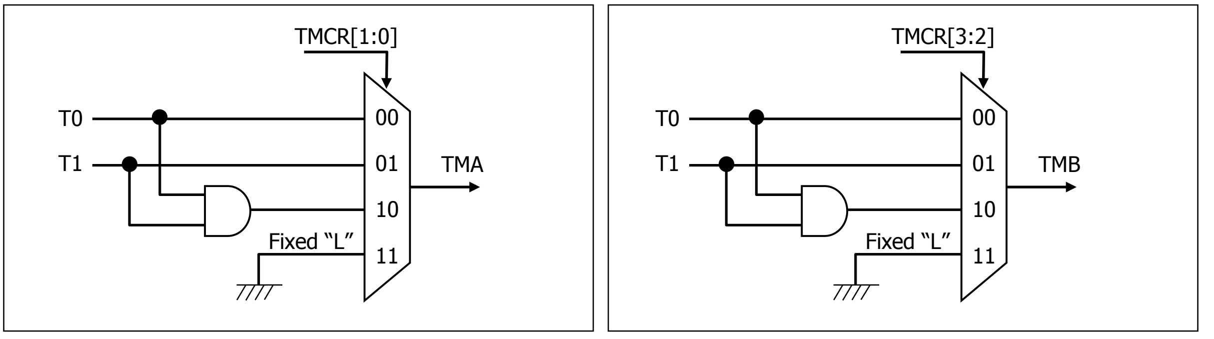
Caution : In the case of T0EG is "0",



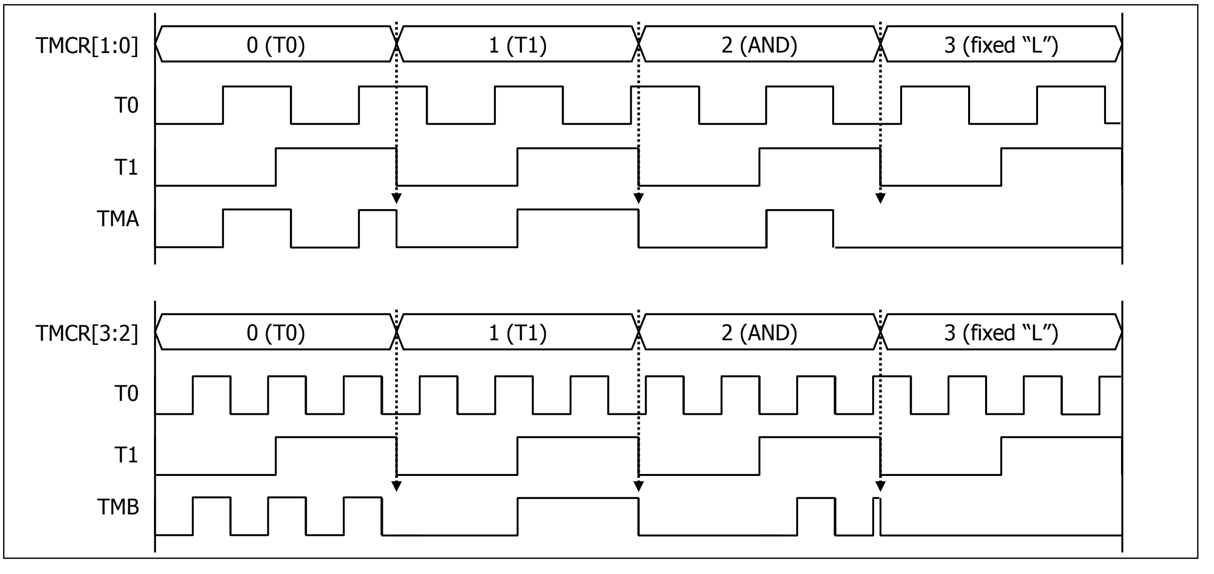
Want to count "0", set T0EG=1

6.2.4. TMA/TMB OUTPUT CONTROL

* TMA/TMB Logical Output Control



* TMA/TMB Output Timing Diagram



• TMA/TMB Output Control Register (TMCR)

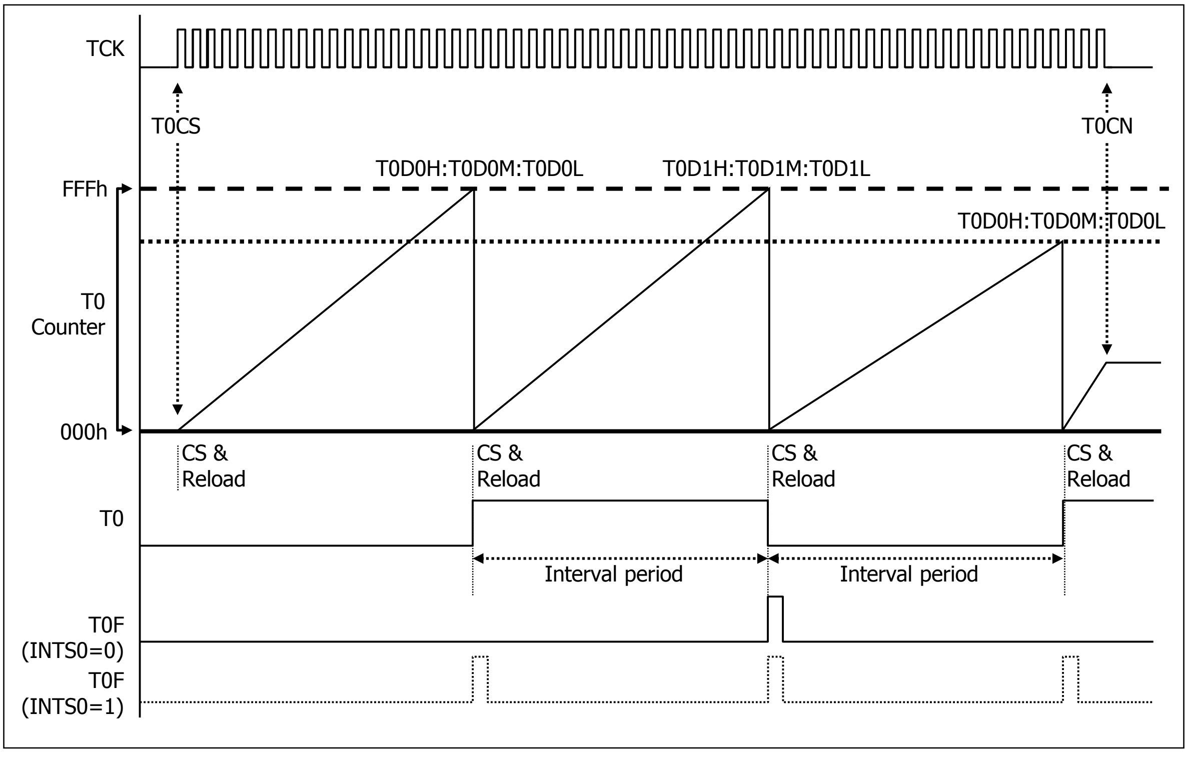
	3	2	1	0	
TMCR	TMCR3	TMCR2	TMCR1	TMCR0	2Fh
initial value	1	1	1	1	
R/W	W	W	W	W	

Selection Mode of TMCR

Bit Name			Selection Mode	Remarks
TMCR3	TMB Output Selection	00	T0 (Timer0 Output)	
		01	T1 (Timer1 Output)	
TMCR2		10	T0 and T1	
		11	fixed "L" (default)	
TMCR1	TMA Output Selection	00	T0 (Timer0 Output)	
		01	T1 (Timer1 Output)	
TMCR0		10	T0 and T1	
		11	fixed "L" (default)	

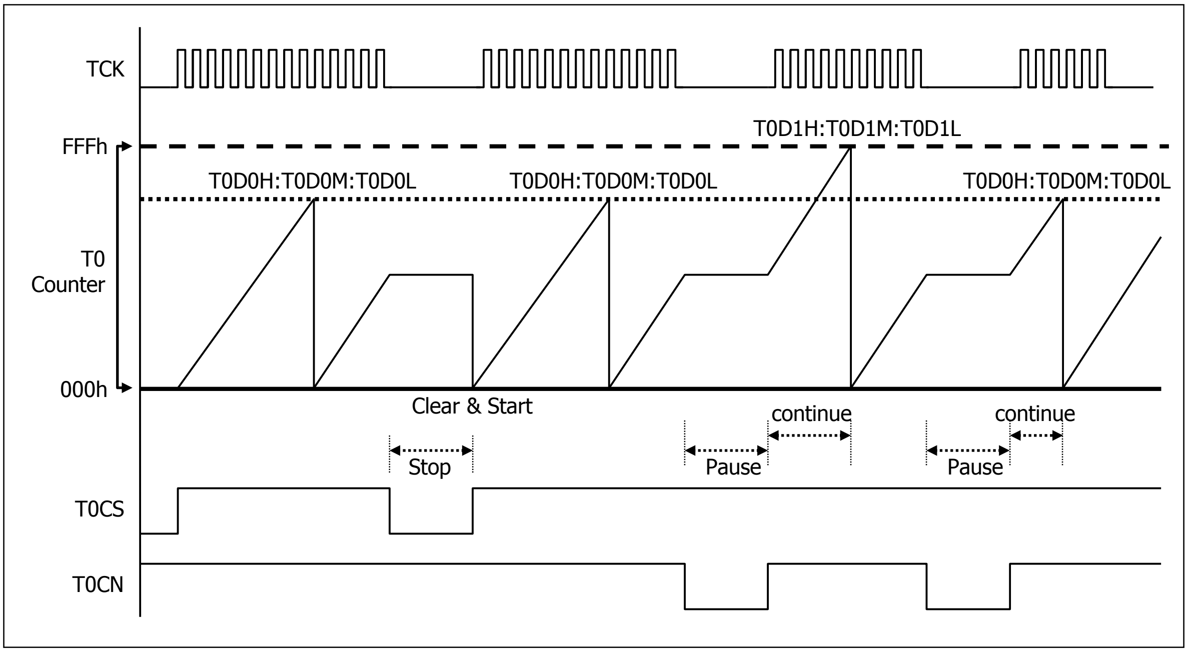
6.2.5. Timer0 Timing Diagram

* 12-bit Timer/Counter mode Timing Diagram

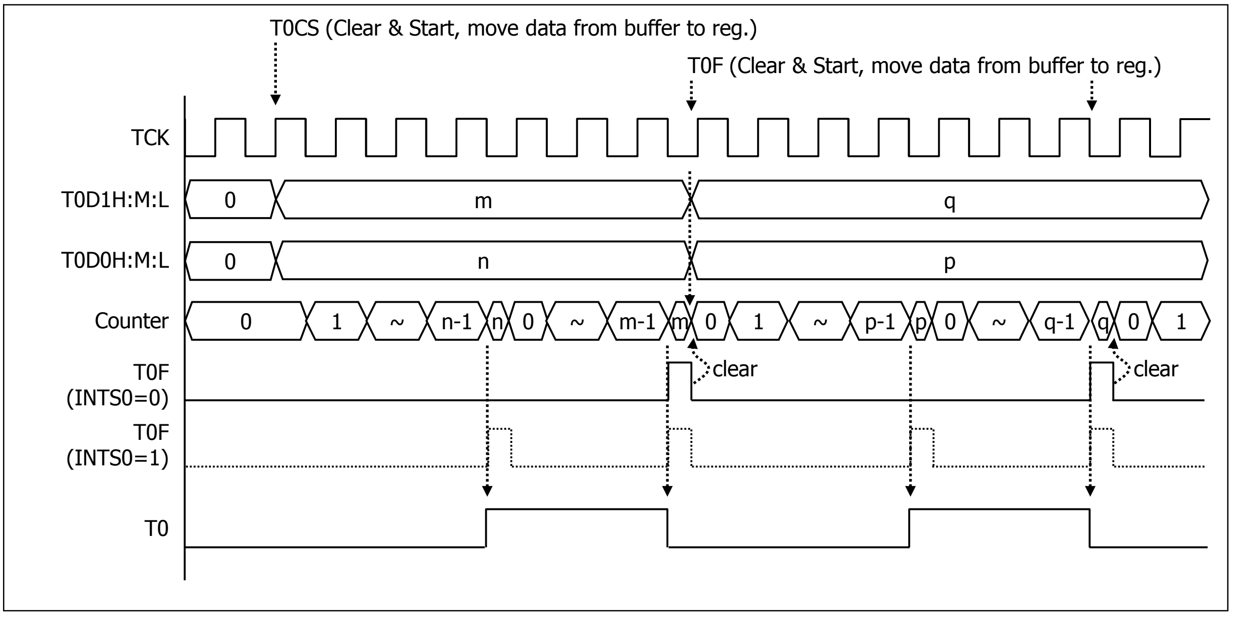


Note > CS : Timer0 Counter Clear & Start.
Reload : Timer0 Data move from Data buffer to Data register.

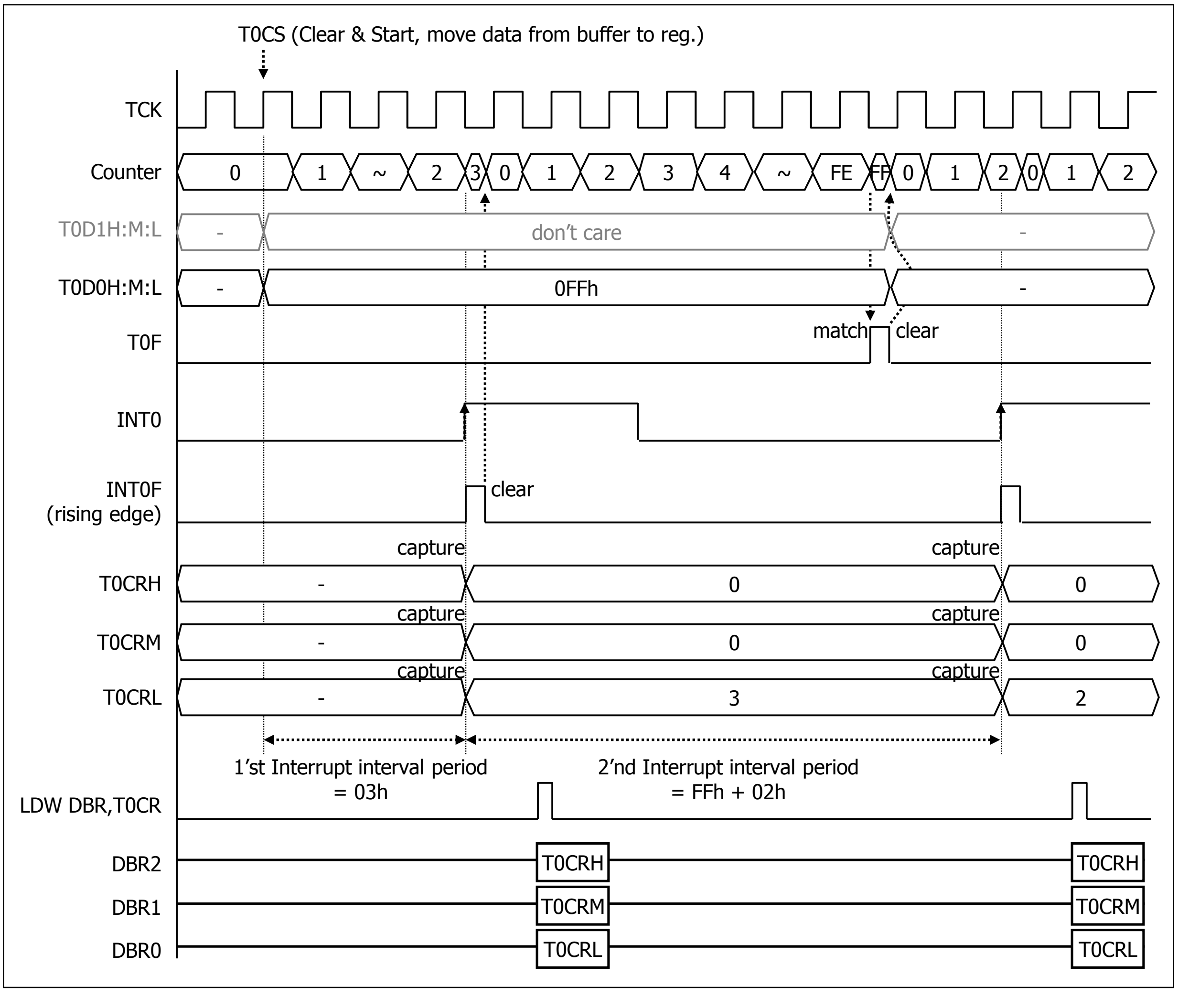
* Start / Stop operation



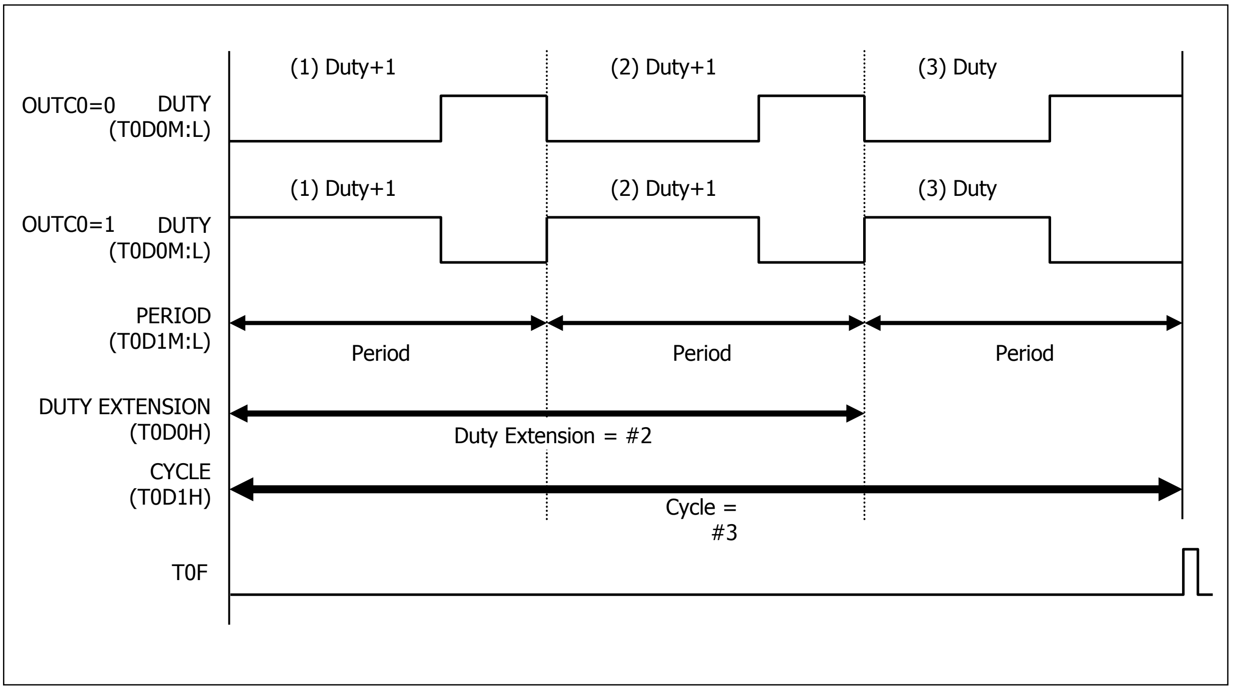
* 12-bit Timer/Counter mode Timing Diagram



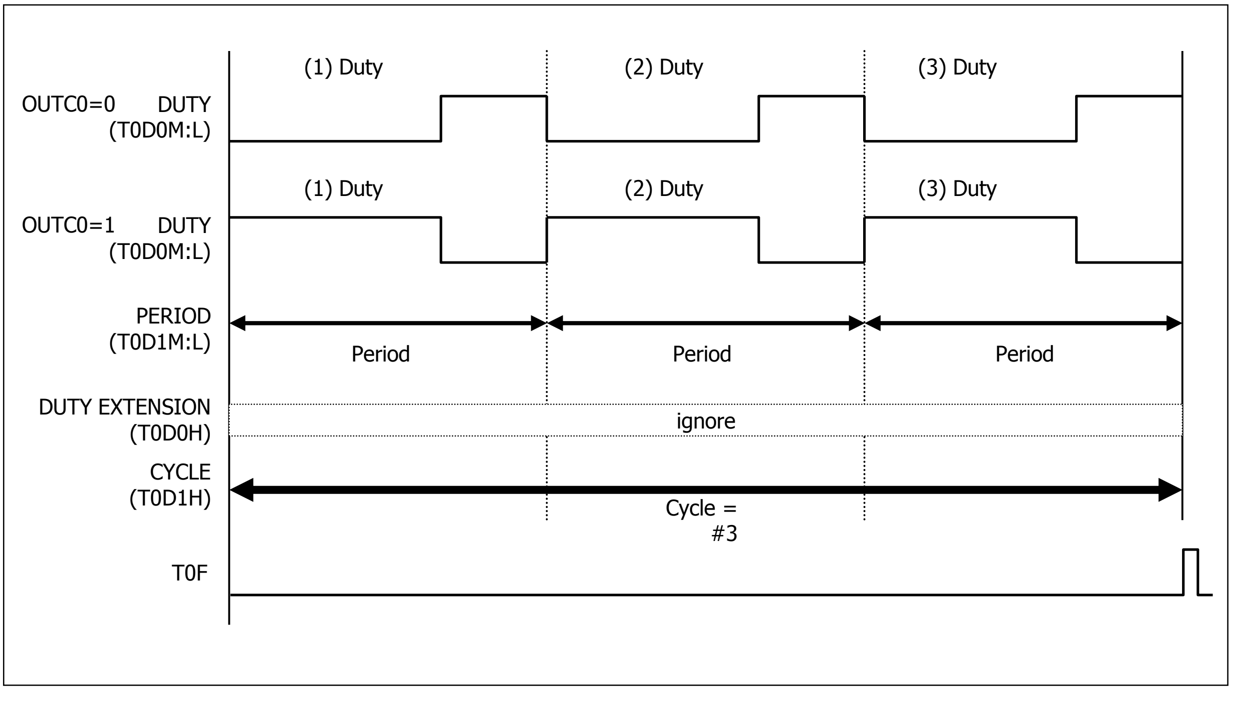
* 12-bit Capture mode Timing Diagram



• PWM mode Timing Diagram : (T0EG=0)



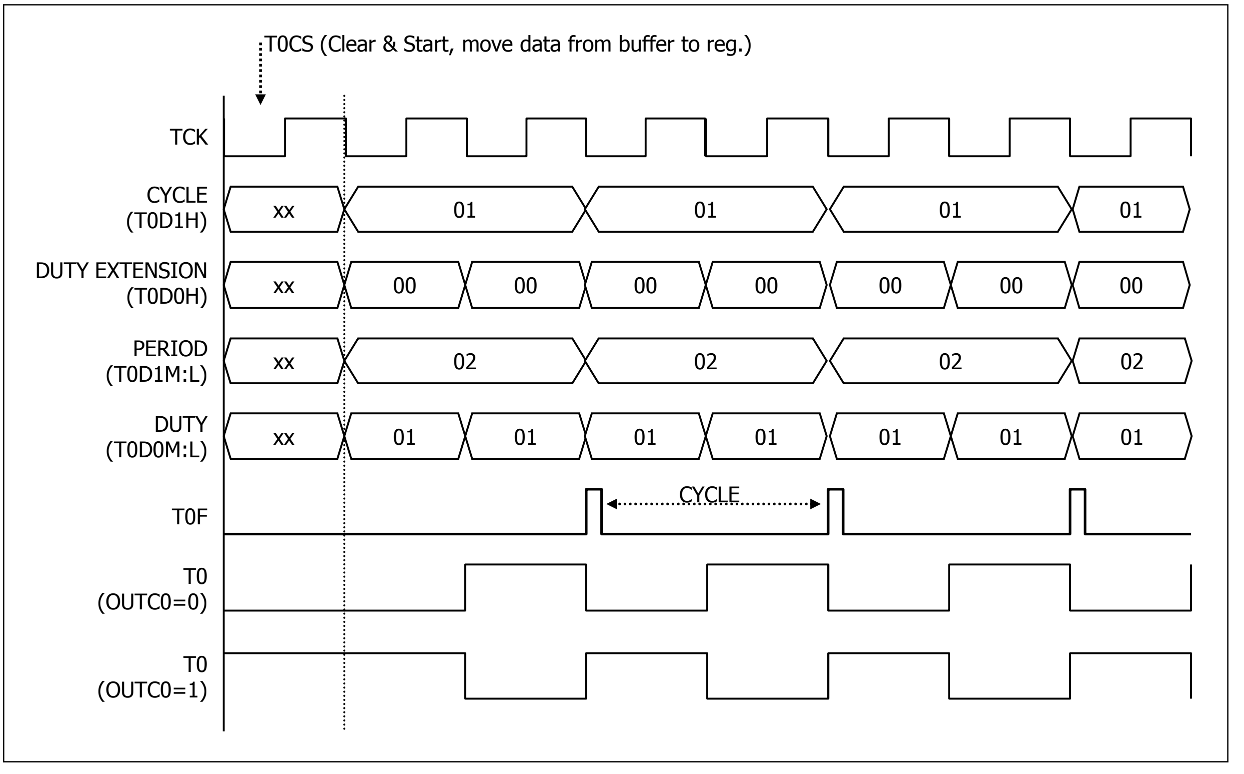
• PWM mode Timing Diagram : (T0EG=1)



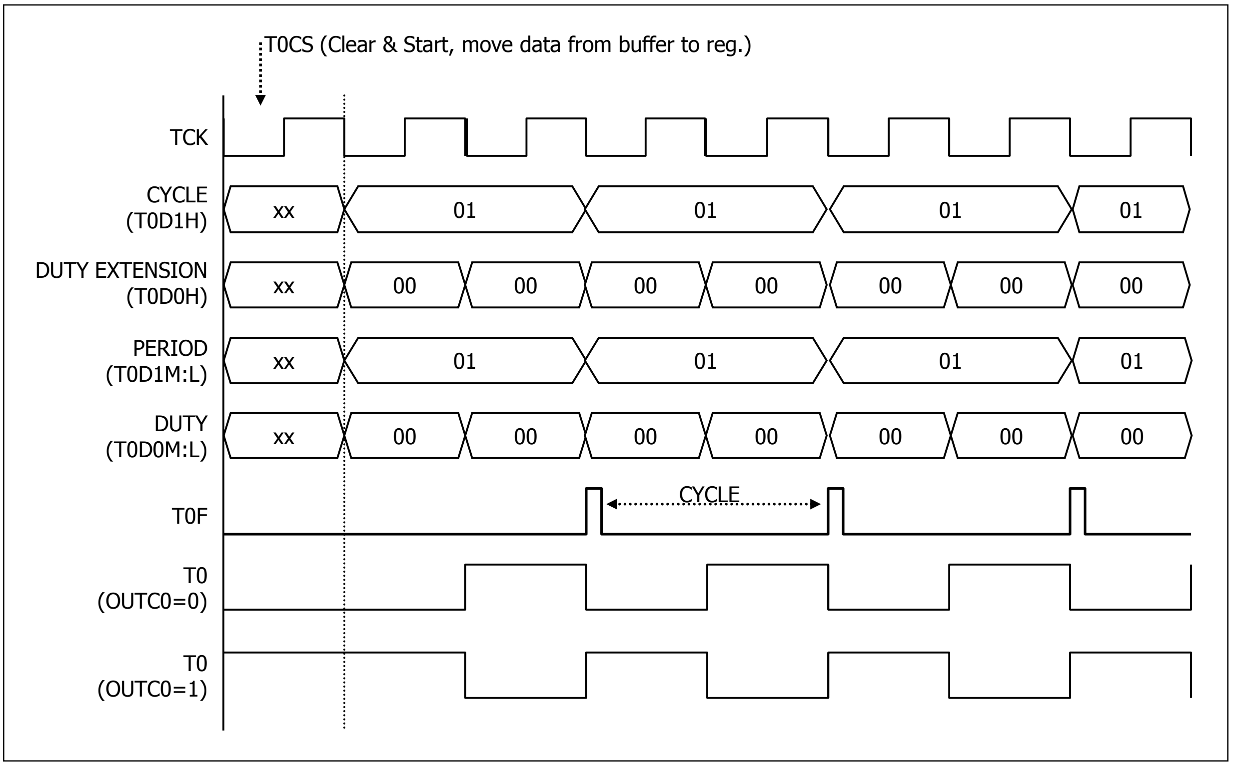
• PWM mode Condition :

Cycle ≠ #0
Period ≠ #1
Duty < Period
Duty Extension < Cycle

• PWM mode Timing Diagram : (T0EG=0, DUTY EXTENSION=0)



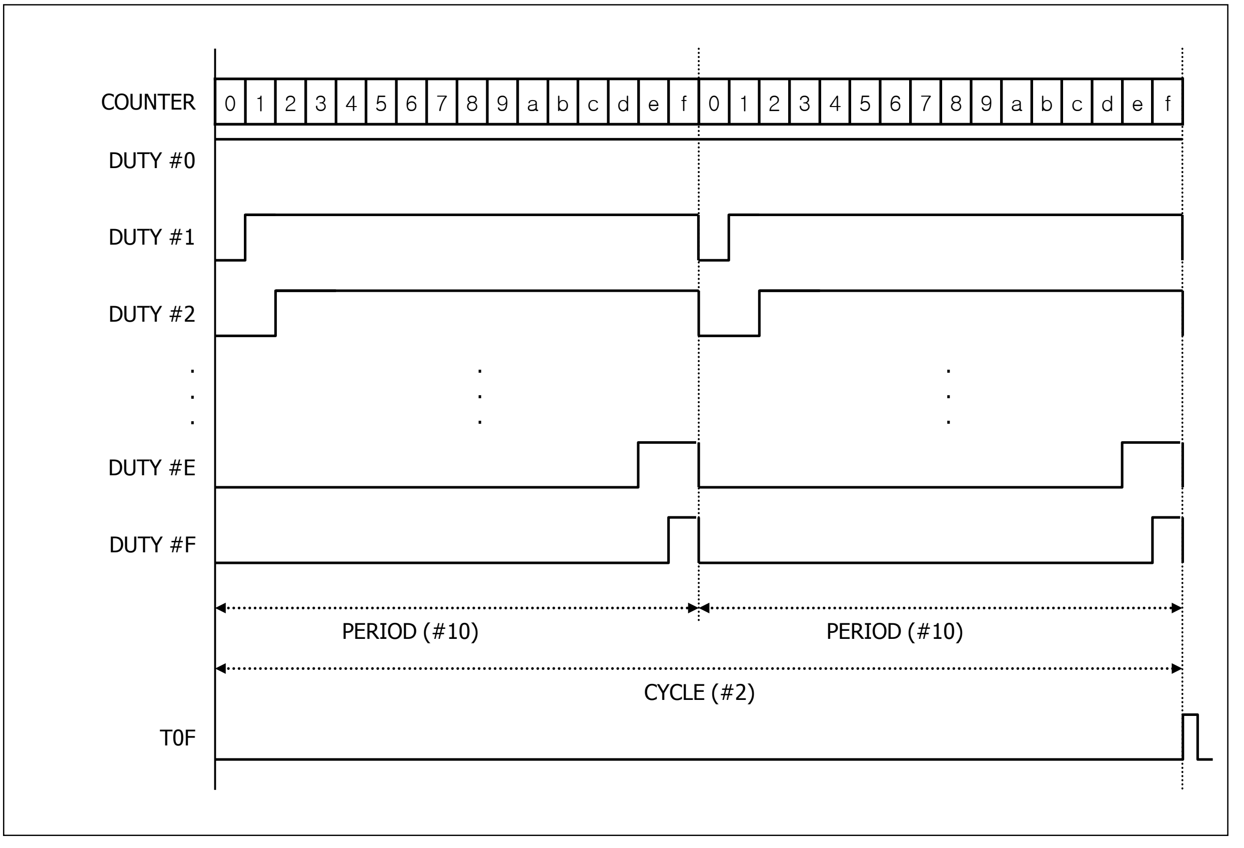
• PWM mode Timing Diagram : (T0EG=1, DUTY EXTENSION=0)



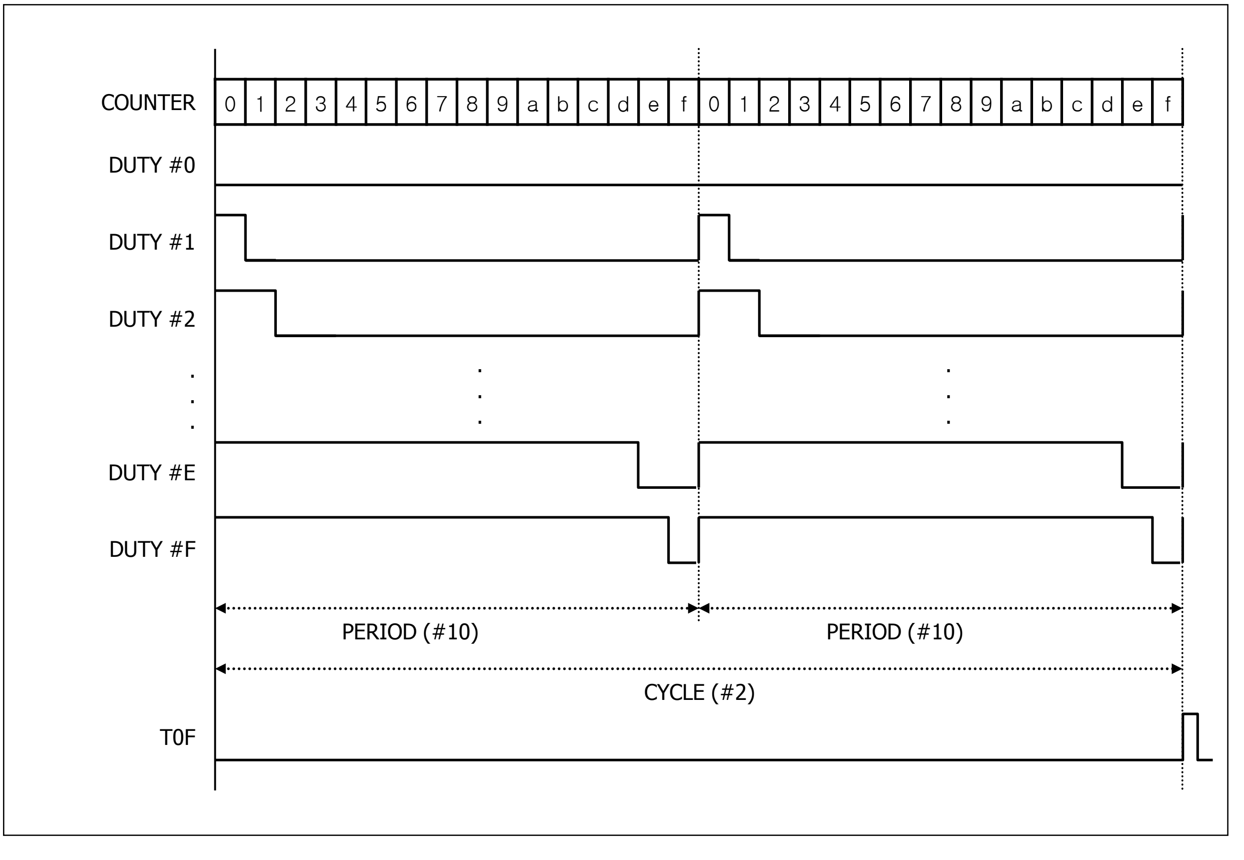
• PWM mode Condition :

Cycle ≠ #0
Period ≠ #1
Duty < Period
Duty Extension < Cycle

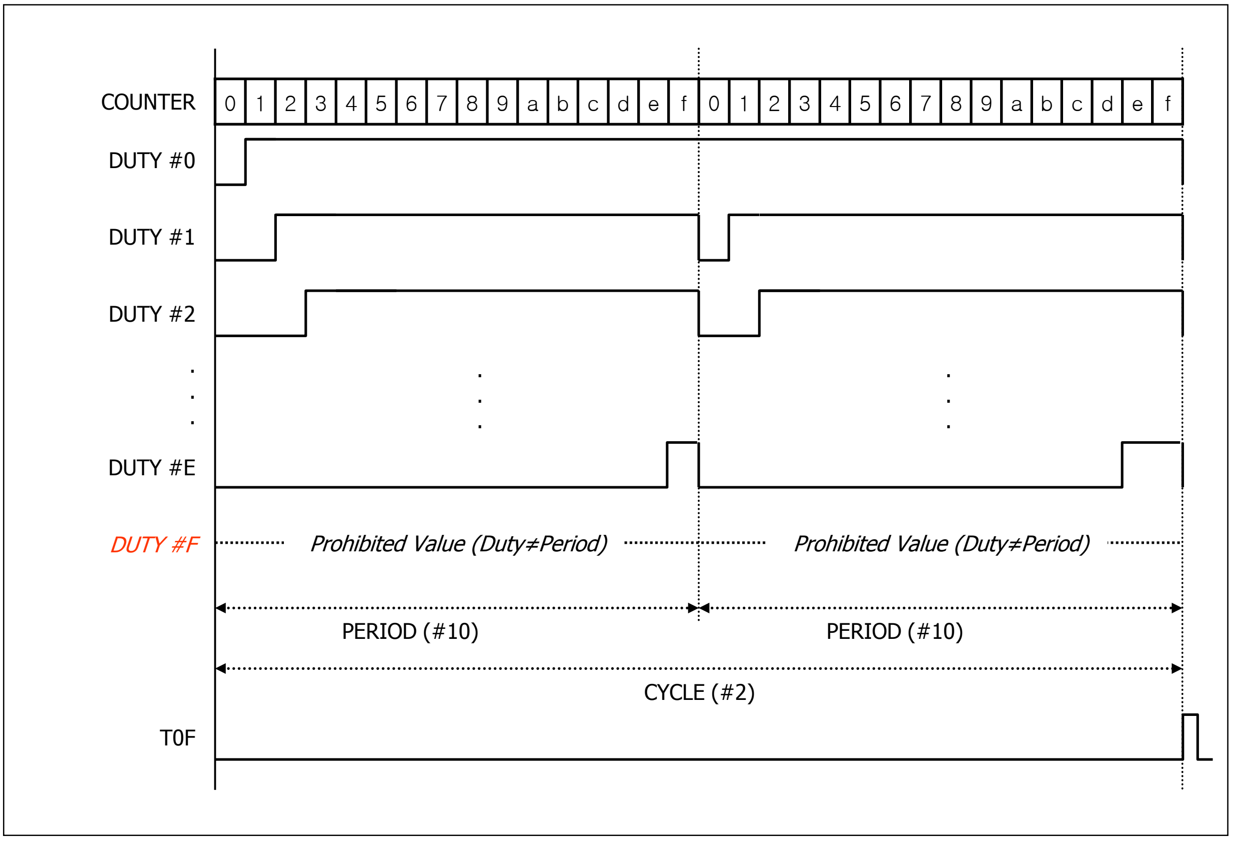
• T0 OUTPUT (PWM mode) Timing Diagram : (OUTC0=0, T0EG=0, DUTY EXTENSION=0)



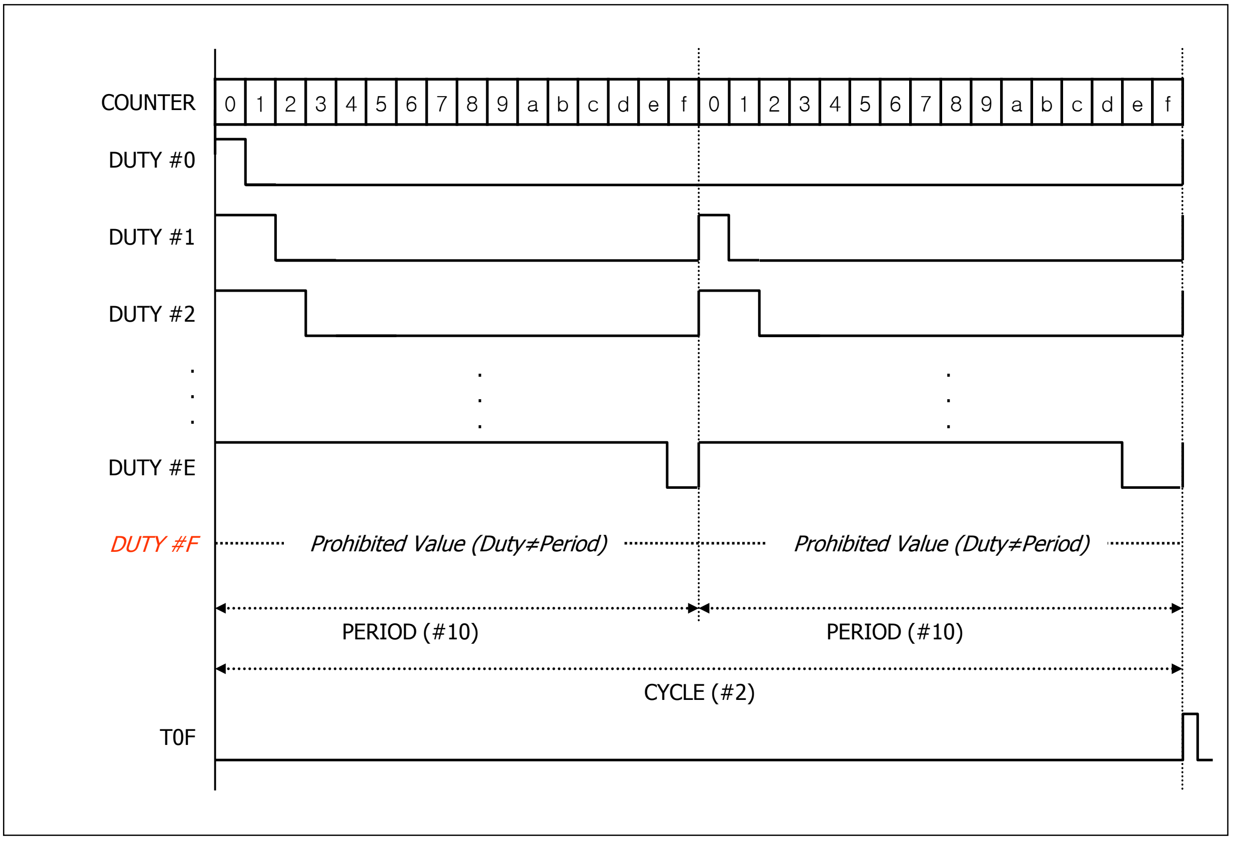
• T0 OUTPUT (PWM mode) Timing Diagram : (OUTC0=1, T0EG=0, DUTY EXTENSION=0)



• T0 OUTPUT (PWM mode) Timing Diagram : (OUTC0=0, T0EG=0, DUTY EXTENSION=1)

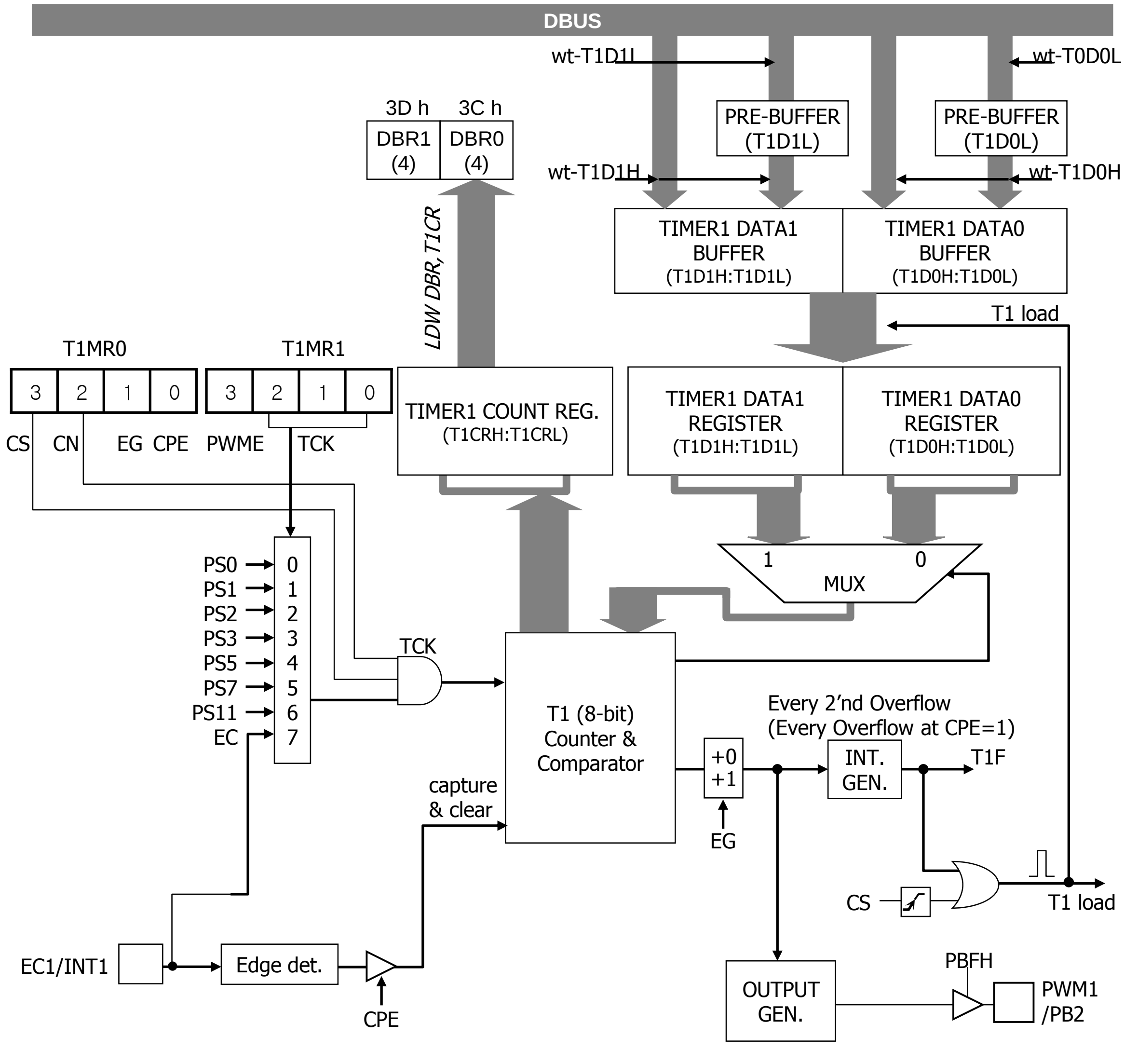


• T0 OUTPUT (PWM mode) Timing Diagram : (OUTC0=1, T0EG=0, DUTY EXTENSION=1)



6.3. Timer1

6.3.1. Timer1(T1) Block Diagram



Note1> The status of T1 Output is
"0" for counting T1D0H:T1D0L
also, "1" for counting T1D1H:T1D1L.

Note2> The low-order digit should be written first, and then high-order digit.

6.3.2. Timer1 Control Register

• Timer1 Mode Register 0 (T1MR0)

	3	2	1	0	
T1MR0	T1CS	T1CN	T1EG	T1CPE	29h
initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of T1MR0

Bit Name			Selection Mode	Remarks
T1CS	Timer0 Clear / start Control	0	Timer1 Stop	
		1	Timer1 Clear and Start	
T1CN	Timer0 Pause / Continue Control	0	Timer1 Pause	
		1	Timer1 continue	
T1EG	Timer0 Count Control	0	Timer1 Count	
		1	Timer1 Count + 1	
T1CPE	Input capture Mode selection	0	Timer/Counter Mode	
		1	Capture Mode	

• Timer1 Mode Register 1 (T1MR1)

	3	2	1	0	
T1MR1	PWME1	T1CK2	T1CK1	T1CK0	2Ah
initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of T1MR1

Bit Name			Selection Mode	Remarks
PWME1	Timer/PWM Mode Selection	0	Timer1 Normal Mode	
		1	Timer1 PWM Mode	
T1CK2 T1CK1 T1CK0	Input clock selection	000	PS0 ($f_{OSC}/2^0$)	
		001	PS1 ($f_{OSC}/2^1$)	
		010	PS2 ($f_{OSC}/2^2$)	
		011	PS3 ($f_{OSC}/2^3$)	
		100	PS5 ($f_{OSC}/2^5$)	
		101	PS7 ($f_{OSC}/2^7$)	
		110	PS11 ($f_{OSC}/2^{11}$)	
		111	EC1	

• Timer1 Data0 Register Low (T1D0L)

	3	2	1	0	
T1D0L	T1D0L3	T1D0L2	T1D0L1	T1D0L0	2Bh
initial value	–	–	–	–	
R/W	W	W	W	W	

• Timer1 Count Register Low (T1CRL)

	3	2	1	0	
T1CRL	T1CRL3	T1CRL2	T1CRL1	T1CRL0	2Bh
initial value	–	–	–	–	
R/W	R	R	R	R	

• Timer1 Data0 Register High (T1D0H)

	3	2	1	0	
T1D0H	T1D0H3	T1D0H2	T1D0H1	T1D0H0	2Ch
initial value	–	–	–	–	
R/W	W	W	W	W	

• Timer1 Count Register High (T1CRH)

	3	2	1	0	
T1CRH	T1CRH3	T1CRH2	T1CRH1	T1CRH0	2Ch
initial value	–	–	–	–	
R/W	R	R	R	R	

• Timer1 Data1 Register Low (T1D1L)

	3	2	1	0	
T1D1L	T1D1L3	T1D1L2	T1D1L1	T1D1L0	2Dh
initial value	–	–	–	–	
R/W	W	W	W	W	

• Timer1 Data1 Register High (T1D1H)

	3	2	1	0	
T1D1H	T1D1H3	T1D1H2	T1D1H1	T1D1H0	2Eh
initial value	–	–	–	–	
R/W	W	W	W	W	

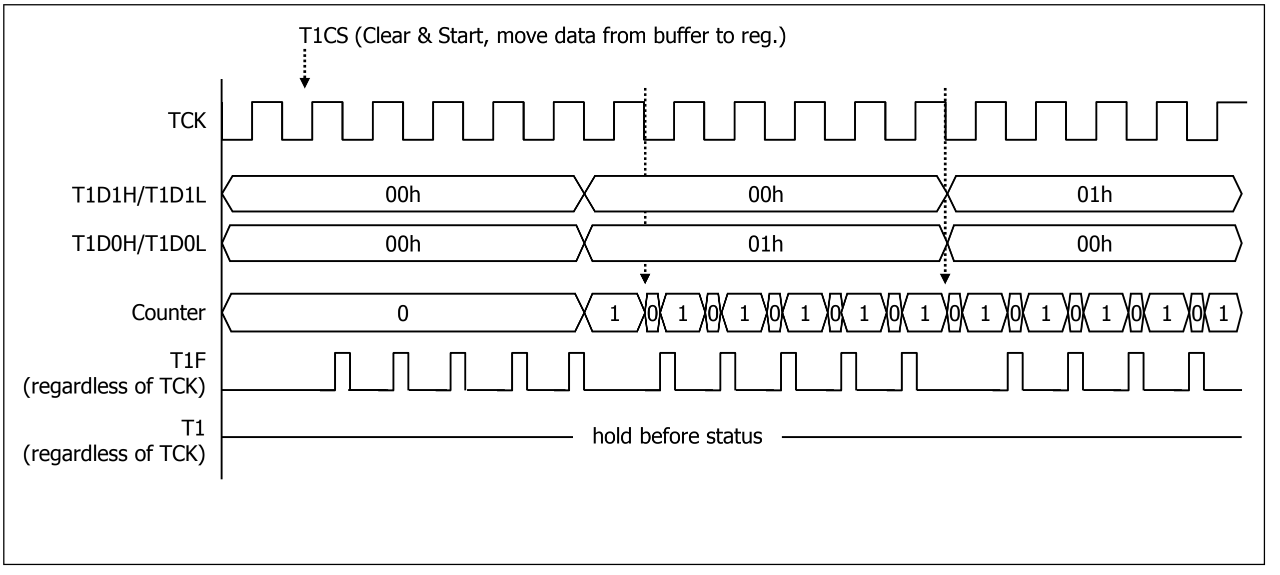
※ PWM1 Data Registers

PWM1 Duty Extension (PWM1DE) [2-bit]		PWM1 Duty (PWM1DY) [6-bit]					
3	2	1	0	3	2	1	0
T1D0H3	T1D0H2	T1D0H1	T1D0H0	T1D0L3	T1D0L2	T1D0L1	T1D0L0
T1D0H [2Ch]				T1D0L [2Bh]			

PWM1 Cycle (PWM1CY) [2-bit]		PWM1 Period (PWM1PR) [6-bit]					
3	2	1	0	3	2	1	0
T1D1H3	T1D1H2	T1D1H1	T1D1H0	T1D1L3	T1D1L2	T1D1L1	T1D1L0
T1D1H [2Eh]				T1D1L [2Dh]			

6.3.3. Timer1 Caution

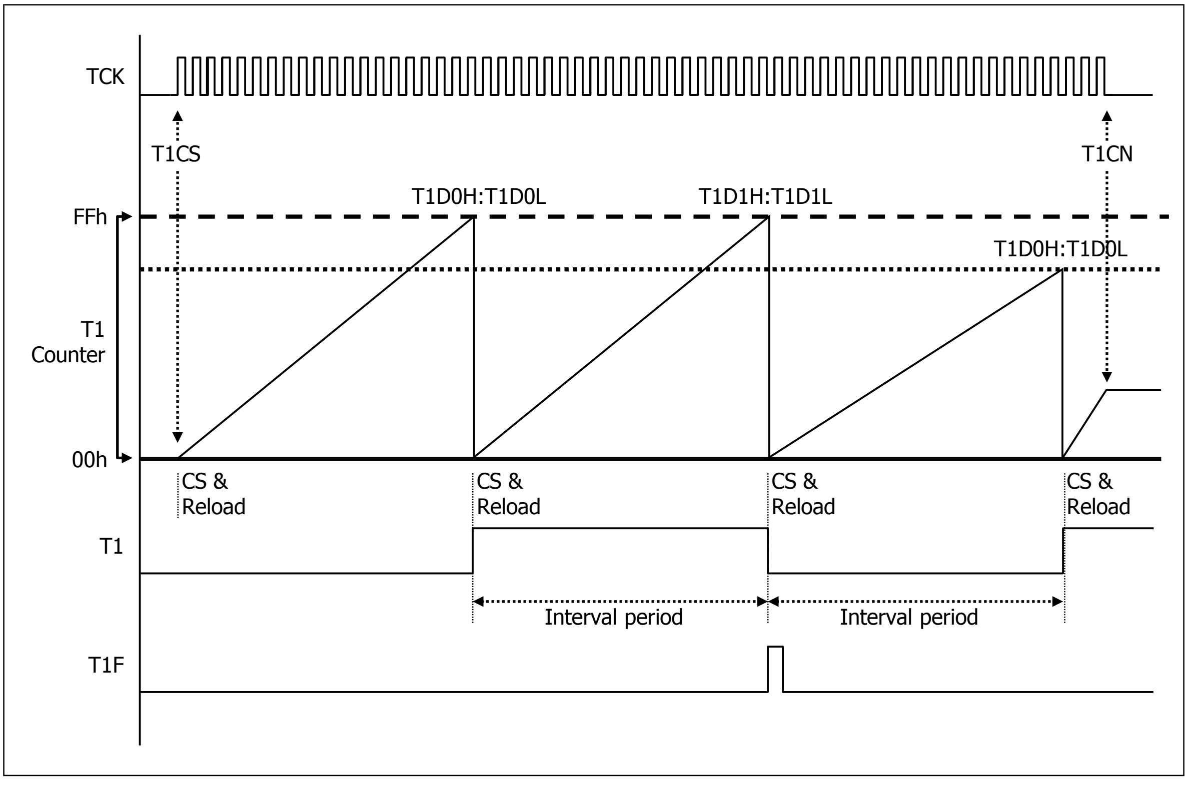
Caution : In the case of T1EG is "0",



Want to count "0", set T1EG=1

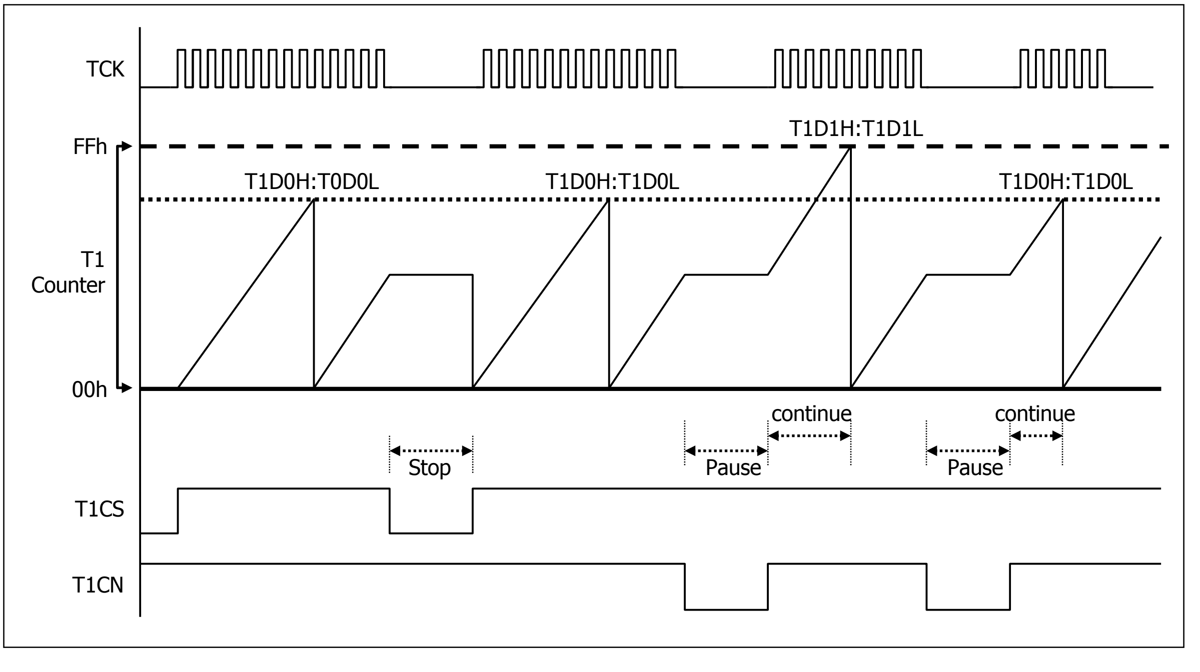
6.3.4. Timer1 Timing Diagram

* 8-bit Timer/Counter mode Timing Diagram

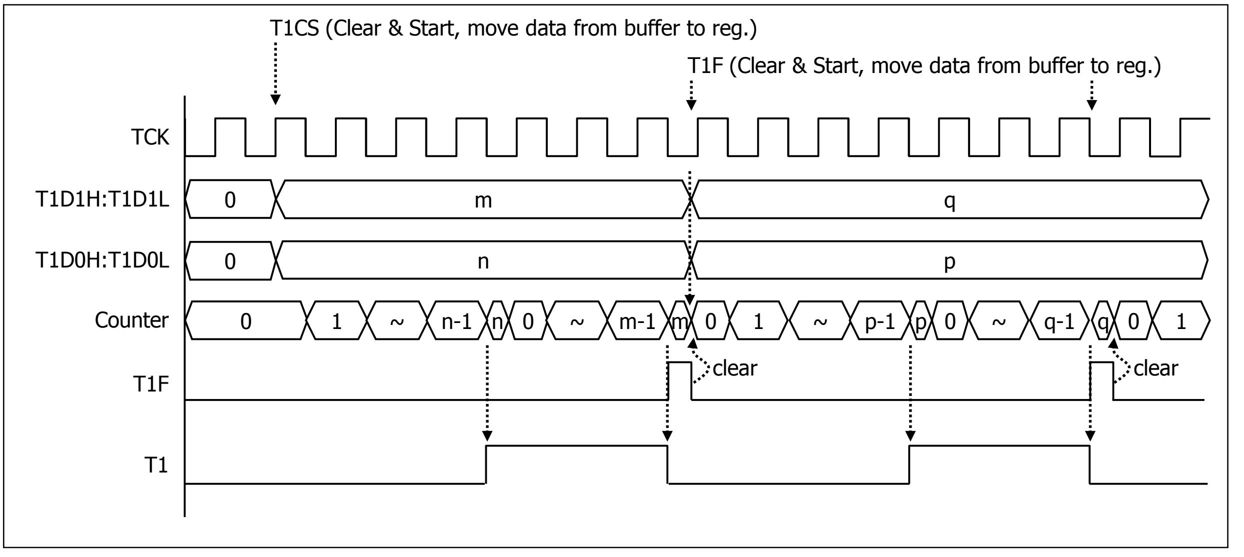


Note > CS : Timer1 Counter Clear & Start.
Reload : Timer1 Data move from Data buffer to Data register.

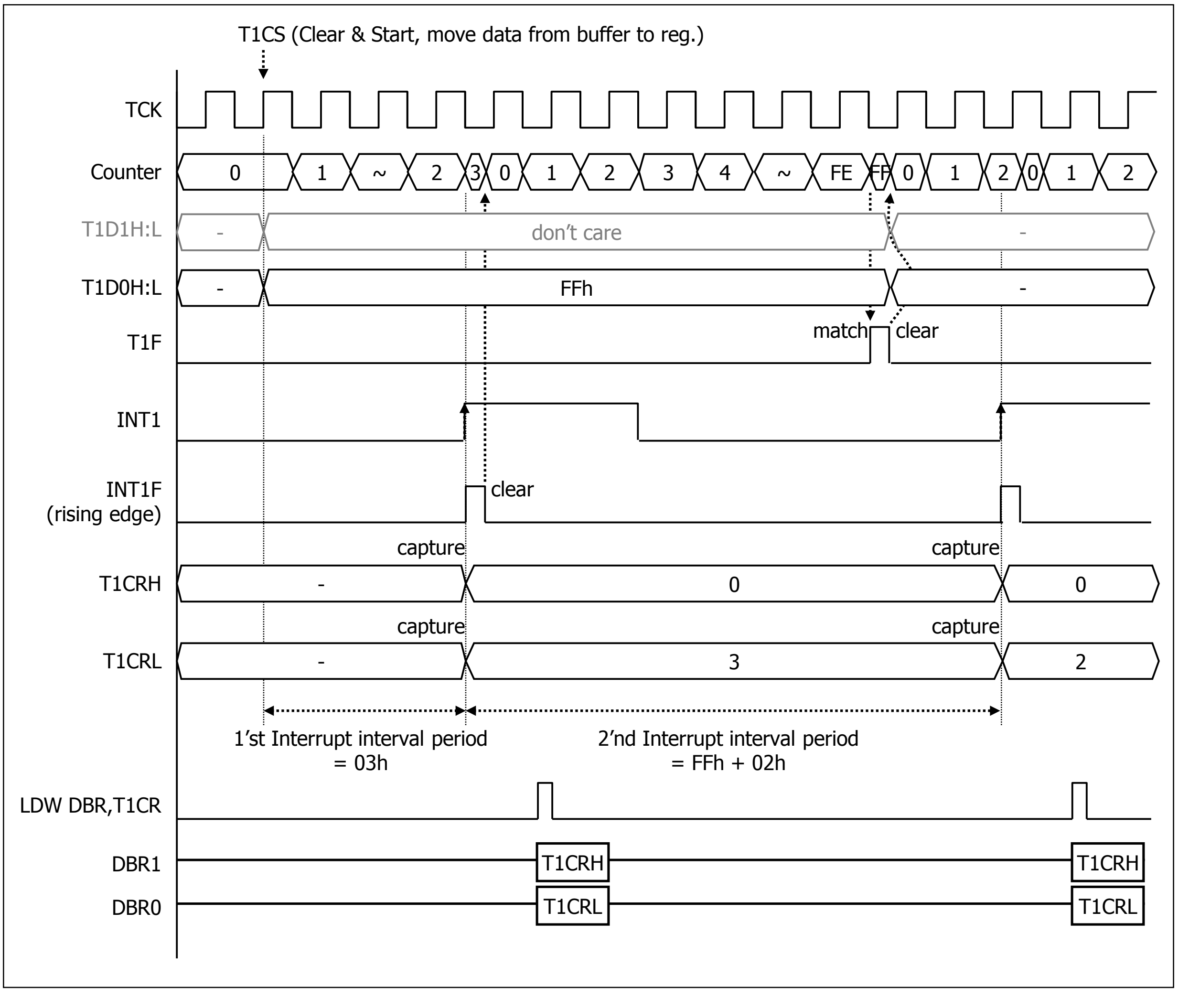
* Start / Stop operation



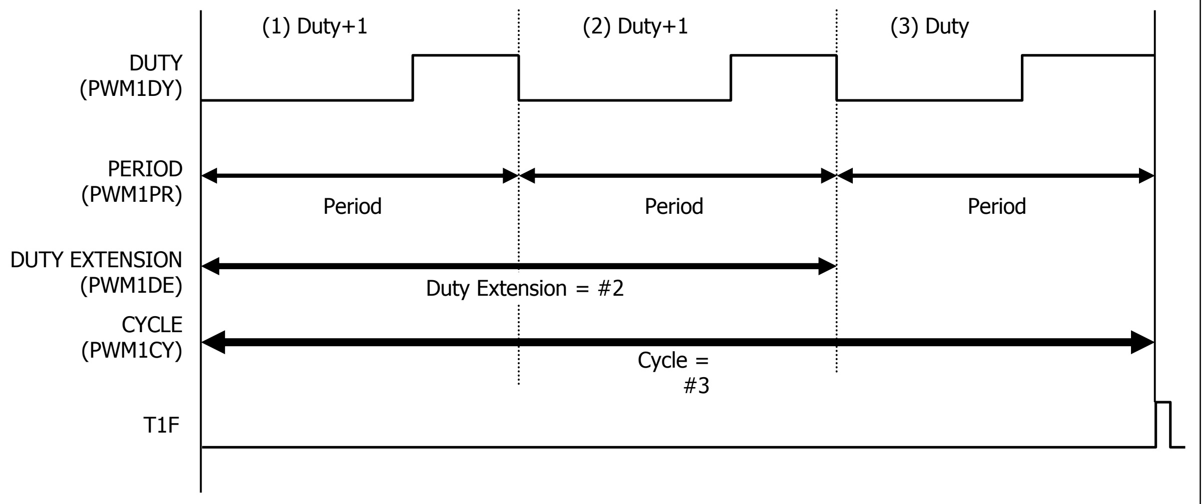
* 8-bit Timer/Counter mode Timing Diagram



* 8-bit Capture mode Timing Diagram

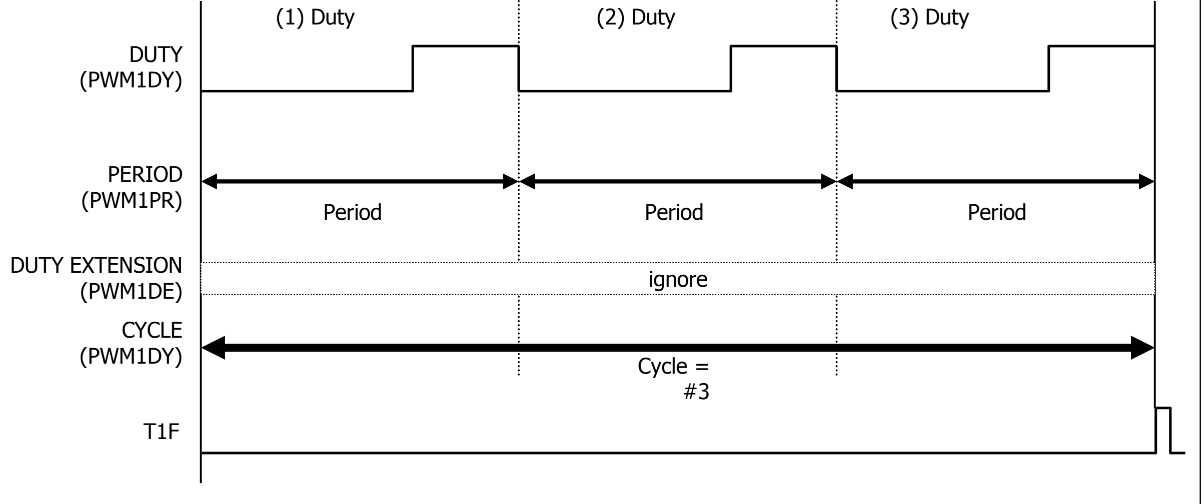


• PWM mode Timing Diagram : (T1EG=0)



※ PWM1DY = T1D0H[1:0] , T1D0L[3:0] ➔ PWM1 Duty (6-bit)
PWM1PR = T1D1H[1:0] , T1D1L[3:0] ➔ PWM1 Period (6-bit)
PWM1DE = T1D0H[3:2] ➔ PWM1 Duty Extension (2-bit)
PWM1CY = T1D1H[3:2] ➔ PWM1 Cycle (2-bit)

• PWM mode Timing Diagram : (T1EG=1)

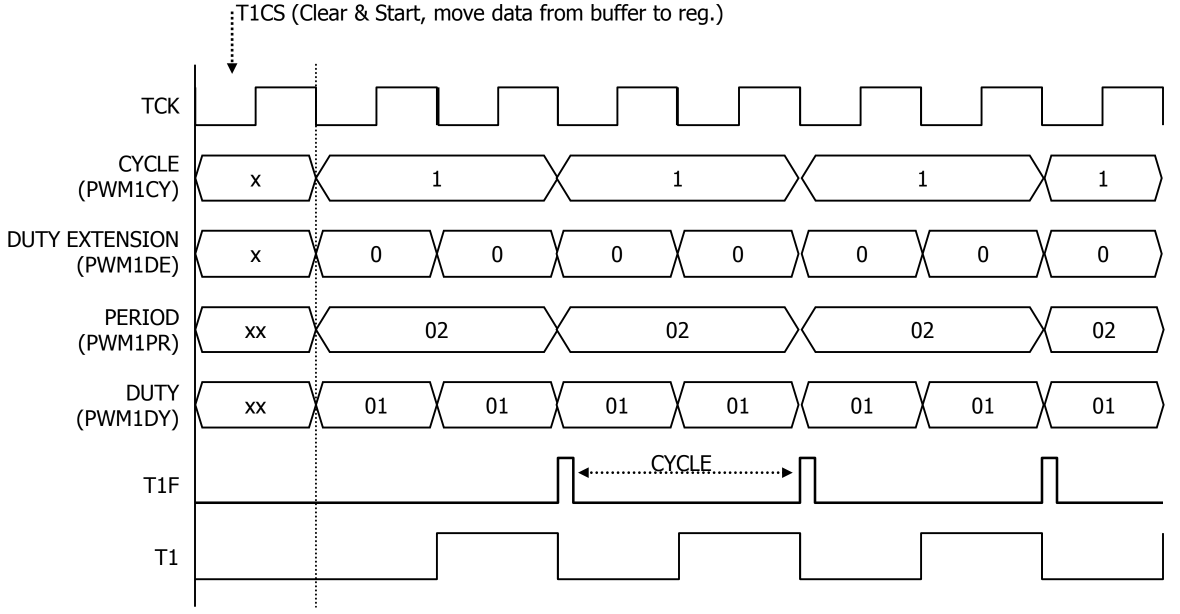


※ PWM1DY = T1D0H[1:0] , T1D0L[3:0] ➔ PWM1 Duty (6-bit)
PWM1PR = T1D1H[1:0] , T1D1L[3:0] ➔ PWM1 Period (6-bit)
PWM1DE = T1D0H[3:2] ➔ PWM1 Duty Extension (2-bit)
PWM1CY = T1D1H[3:2] ➔ PWM1 Cycle (2-bit)

• PWM mode Condition :

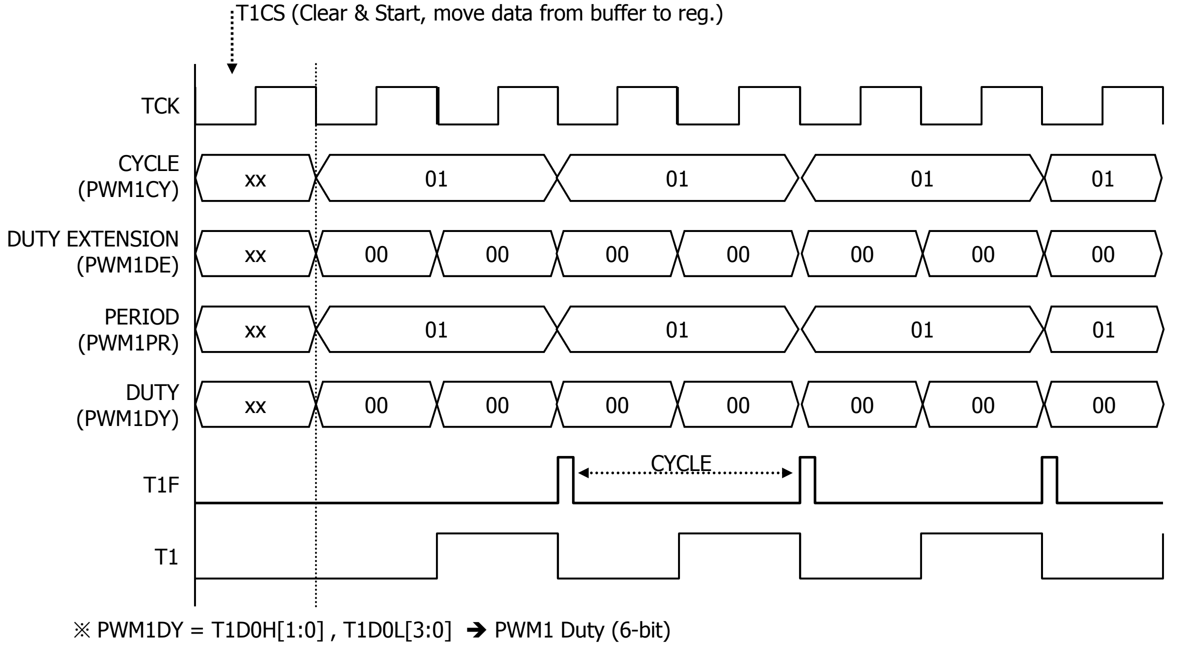
Cycle ≠ #0
Period ≠ #1
Duty < Period
Duty Extension < Cycle

• PWM mode Timing Diagram : (T1EG=0, DUTY EXTENSION=0)



※ PWM1DY = T1D0H[1:0] , T1D0L[3:0] → PWM1 Duty (6-bit)
PWM1PR = T1D1H[1:0] , T1D1L[3:0] → PWM1 Period (6-bit)
PWM1DE = T1D0H[3:2] → PWM1 Duty Extension (2-bit)
PWM1CY = T1D1H[3:2] → PWM1 Cycle (2-bit)

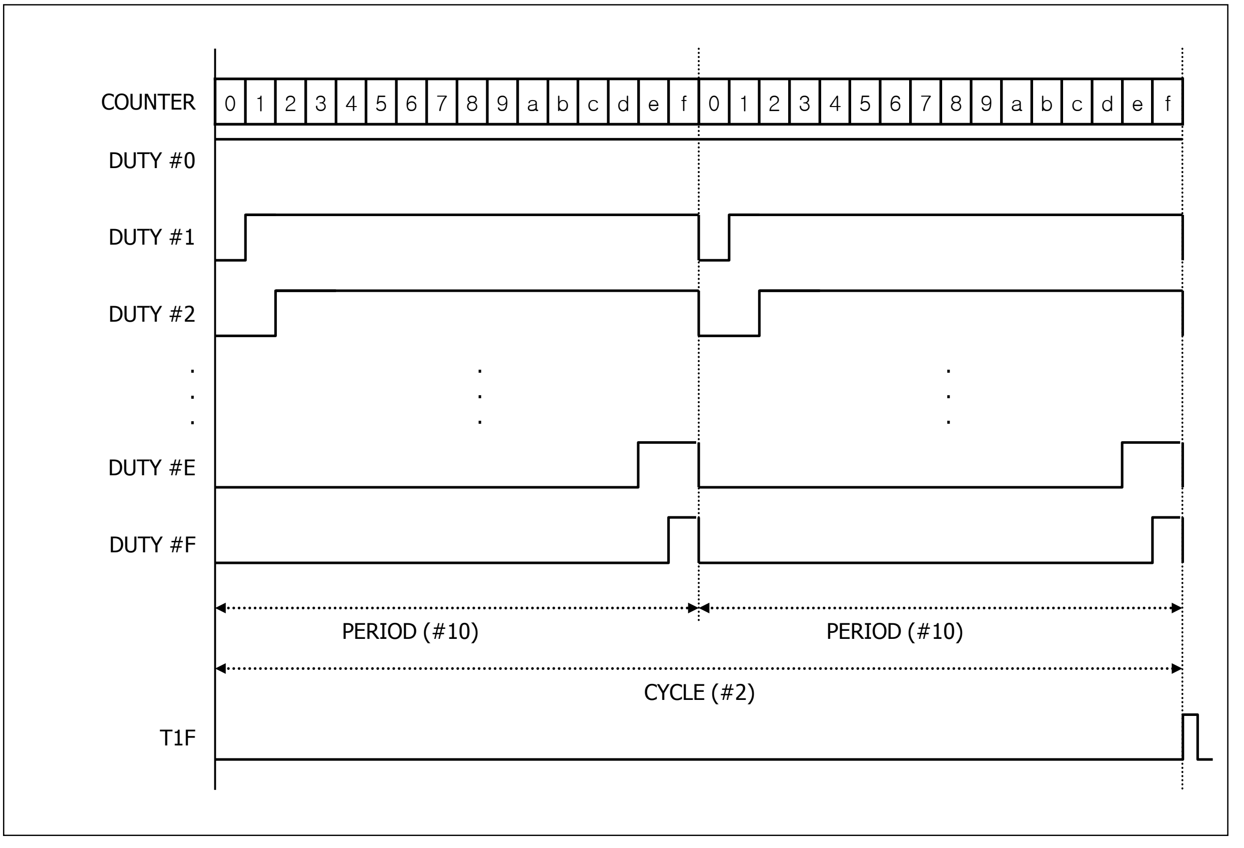
• PWM mode Timing Diagram : (T1EG=1, DUTY EXTENSION=0)



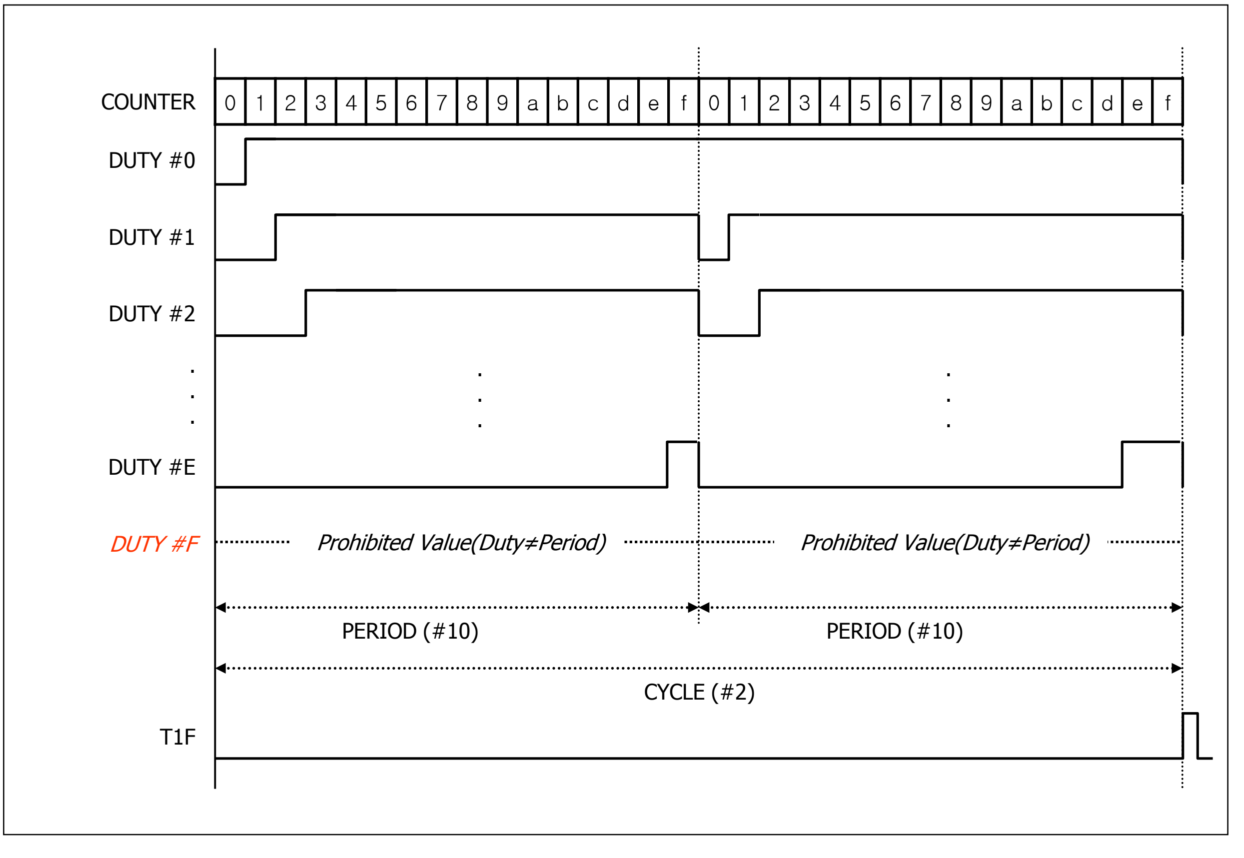
※ PWM1DY = T1D0H[1:0] , T1D0L[3:0] → PWM1 Duty (6-bit)
PWM1PR = T1D1H[1:0] , T1D1L[3:0] → PWM1 Period (6-bit)
PWM1DE = T1D0H[3:2] → PWM1 Duty Extension (2-bit)
PWM1CY = T1D1H[3:2] → PWM1 Cycle (2-bit)

• PWM mode Condition :
Cycle ≠ #0
Period ≠ #1
Duty < Period
Duty Extension < Cycle

• T1 OUTPUT (PWM mode) Timing Diagram : (T1EG=0, DUTY EXTENSION=0)



• T1 OUTPUT (PWM mode) Timing Diagram : (T1EG=0, DUTY EXTENSION=1)



The ADAM43P1108 contains 8 interrupt sources; 3 externals and 5 internals.
Nested interrupt services with priority control is also possible.

- ▶ 8 interrupt source (3Ext, 2Timer, 1 A/D, 1VDI, 1WDT)
- ▶ 8 interrupt vector
- ▶ 8 level nested interrupt control is possible.
- ▶ Read of interrupt request flag are possible.
- ▶ In interrupt accept, request flag is automatically cleared.

Interrupt Enable Register (IENR0, IENR1), Interrupt Request Register (IRQR0, IRQR1) and priority circuit.
Interrupt function block diagram is shown in Fig.7.1

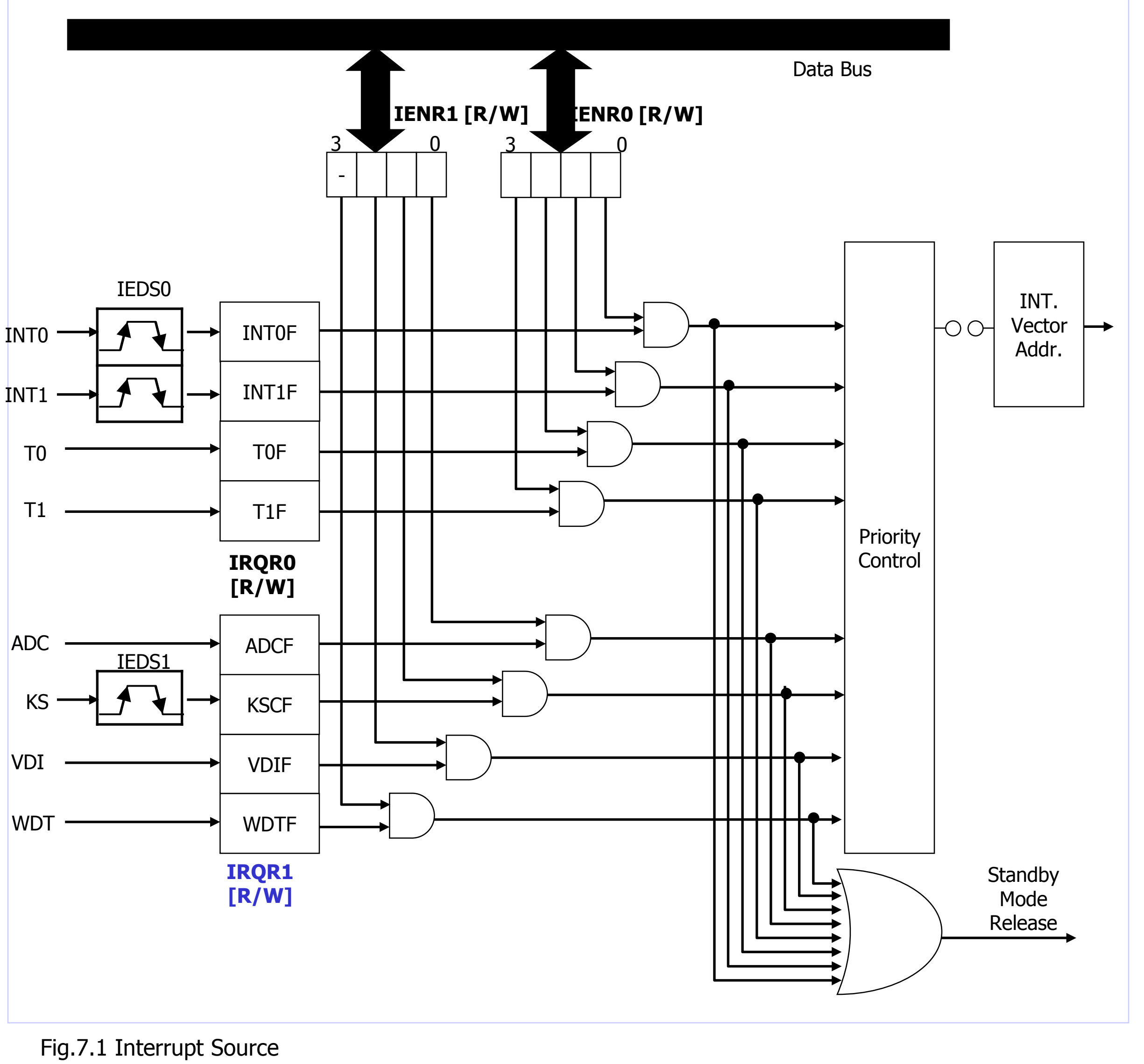


Fig.7.1 Interrupt Source

7. Interrupt

7.1. Interrupt Source

Each interrupt vector is independent and has its own priority.

	Mask	Priority	Interrupt Source	INT Vector Addr.
Hardware Interrupt	Non-maskable	-	RESET	0000h
	maskable	1	INT0 (External Interrupt 0)	0002h
		2	INT1 (External Interrupt 1)	0004h
		3	T0 (Timer0)	0006h
		4	T1 (Timer1)	0008h
		5	ADC (Analog Digital Converter)	000Ah
		6	KS (Key Scan)	000Ch
		7	VDI (Voltage Detection Indicator)	000Eh
		8	WDT (Watch-Dog Timer)	0010h

Table 7.1 Interrupt Source

7.2. Interrupt Control Register

I flag of SFR is a interrupt mask enable flag. When I flag = ``0``, all interrupts become disable. When I flag = ``1``, interrupts can be selectively enabled and disabled by contents of corresponding Interrupt Enable Register(IENR0, IENR1).
When interrupt is occurred, interrupt request flag is set,and Interrupt request is detected at the edge of interrupt signal. The accepted interrupt request flag is automatically cleared during interrupt cycle process. The interrupt request flag maintains ``1`` until the interrupt is accepted
or is cleared in program. In reset state, interrupt request flag register (IRQR0,IRQR1) is cleared to ``0``.
It is possible to read the state of interrupt register and to manipulate the contents of register.

- External Interrupt Edge selection Register 0 (IEDS0)

	3	2	1	0	
IEDS0	IED1H	IED1L	IED0H	IED0L	1Ah
initial value	0	0	0	0	
R/W	W	W	W	W	

Bit Name	Selection Mode		Remarks
IED1H IED1L	00	-	INT1
	01	Falling Edge Selection (1-to-0 transition)	
	10	Rising Edge Selection (0-to-1 transition)	
	11	Both Edge Selection (Falling & Rising)	
IED0H IED0L	00	-	INT0
	01	Falling Edge Selection (1-to-0 transition)	
	10	Rising Edge Selection (0-to-1 transition)	
	11	Both Edge Selection (Falling & Rising)	

• External Interrupt Edge selection Register 1 (IEDS1)

	3	2	1	0	
IEDS0	LVDC	VOLC	IEDKH	IEDKL	1Bh
initial value	0	0	0	0	
R/W	W	W	W	W	

Selection Mode of IEDS1

Bit Name	Selection Mode		Remarks
LVDC	0	LVD Enable	* Caution of usage
	1	LVD Disable	
VOLC	0	PA, PB port NMOS Driving Normal	* Caution of usage
	1	PA, PB port NMOS Driving Decrease	
IEDKH IEDKL	00	–	KS
	01	Falling Edge Selection (1–to–0 transition)	
	10	Rising Edge Selection (0–to–1 transition)	
	11	Both Edge Selection (Falling & Rising)	

• Interrupt Enable Register 0 (IENR0)

	3	2	1	0	
IENR0	T1E	T0E	INT1E	INT0E	1Eh
initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of IENR0

Bit Name	Selection Mode		Remarks
T1E	1	Timer1 Interrupt enable	
T0E	1	Timer0 Interrupt enable	
INT1E	1	External Interrupt 1 enable	
INT0E	1	External Interrupt 0 enable	

• Interrupt Enable Register 1 (IENR1)

	3	2	1	0	
IENR1	WDTE	VDIE	KSCE	ADCE	1Fh
initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of IENR1

Bit Name	Selection Mode		Remarks
WDTE	1	WDT Timer overflow Interrupt enable	
VDIE	1	Voltage Detection Interrupt enable	
KSCE	1	External Key Scan Interrupt enable	
ADCE	1	ADC Interrupt enable	

• Interrupt Request Flag Register (IRQR0)

	3	2	1	0	
IRQR0	T1F	T0F	INT1F	INT0F	1Ch
initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of IRQR0

Bit Name	Selection Mode		Remarks
T1F	1	Timer1 Interrupt Request Flag enable	
T0F	1	Timer0 Interrupt Request Flag enable	
INT1F	1	External Interrupt 1 Request Flag enable	
INT0F	1	External Interrupt 0 Request Flag enable	

• Interrupt Request Flag Register (IRQR1)

	3	2	1	0	
IRQR1	WDTF	VDIF	KSCF	ADCF	1Dh
initial value	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	

Selection Mode of IRQR1

Bit Name	Selection Mode		Remarks
WDTF	1	WDT Timer overflow Interrupt Flag enable	
VDIF	1	Voltage Detection Interrupt Flag enable	
KSCF	1	External Key Scan Interrupt Flag enable	
ADCF	1	ADC Interrupt Flag enable	

7.3. Interrupt Timing

Interrupt Request Sampling Time :
-. Maximum 2 machine cycle (When execute LDW @ABR Instruction)
-. Minimum 0 machine cycle

Interrupt preprocess step is 1 machine cycle

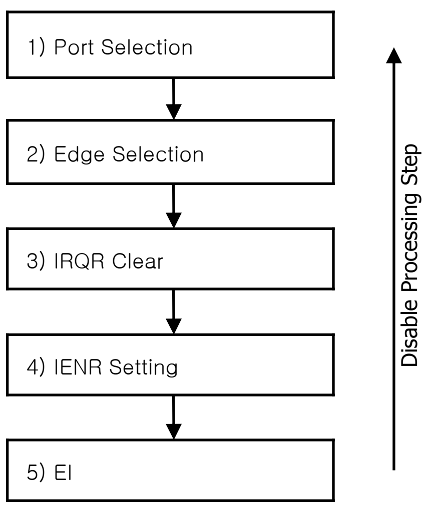
7.4. The valid timing after executing Interrupt control instructions

I flag is valid just after executing of EI/DI on the contrary.

7.5. Multiple Interrupt

If there is an interrupt, Interrupt Mask Enable Flag is automatically cleared before entering the Interrupt Service Routine. After then, no interrupt is accepted. If EI instruction is executed, interrupt mask enable bit becomes "1", and each enable bit can accept interrupt request. When two or more interrupts are generated simultaneously, the highest priority interrupt is accepted.

Key-Scan or External Interrupt Enable Processing Step



7.6. Interrupt Processing Sequence

When an interrupt is accepted, the on-going process is stopped and the interrupt service routine is executed. After the interrupt service routine is completed it is necessary to restore everything to the state before the interrupt occurred.
As soon as an interrupt is accepted, the content of the program counter is saved in the stack register which is 8 level stack area, and the contents of status flag register (SFR) is saved on the interrupt stack register (INTSK) which is 8 level stack area.
At the same time, the content of the vector address corresponding to the accepted interrupt, which is in the interrupt vector table, enters into the program counter and interrupt service is executed. In order to execute the interrupt service routine, it is necessary to write the jump addresses in the vector table corresponding to each interrupt.

Interrupt Processing Step

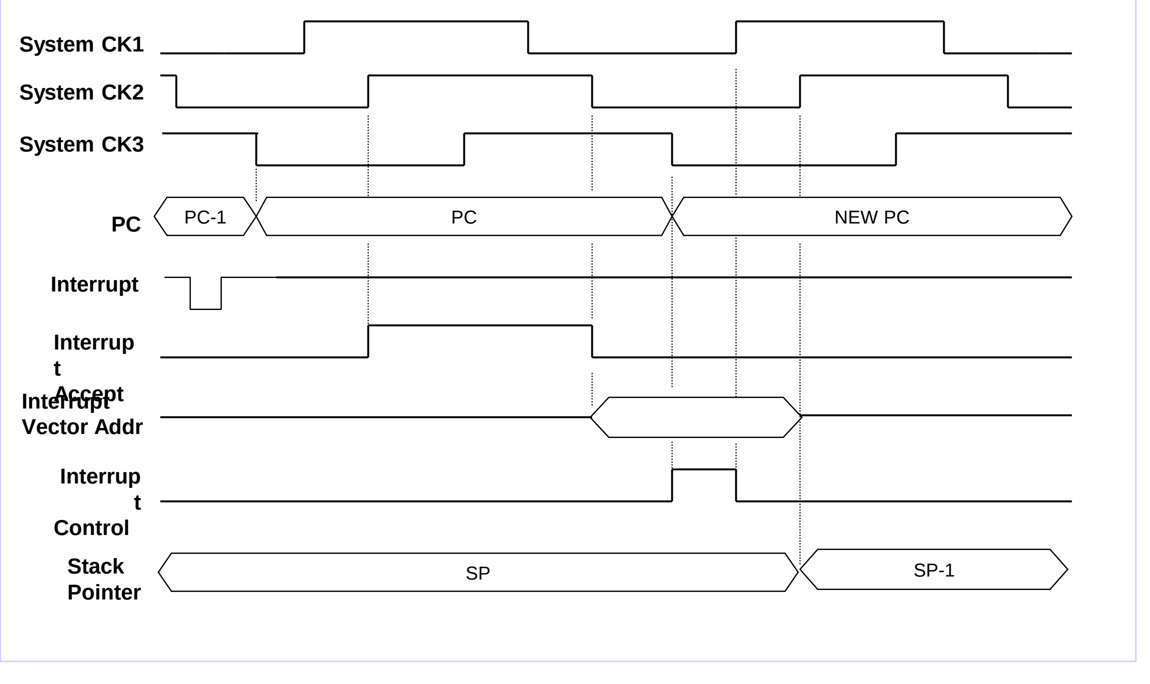
1) Store Program Counter, STACK <= PC

2) Store the contents of Status Flag Register (SFR), INTSK <= SFR

3) After resetting of I-flag, clear accepted Interrupt Request Flag.

4) Call Interrupt service routine

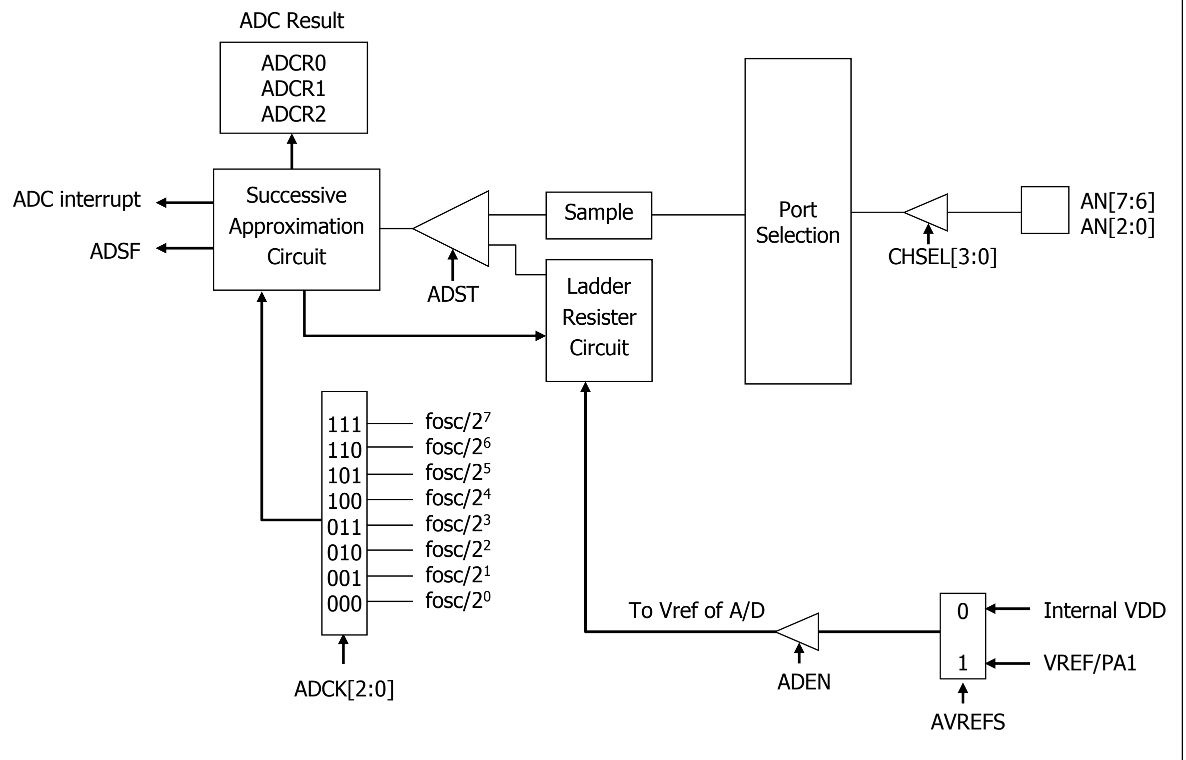
Fig.7.2 Interrupt Processing Step Timing



The analog-to-digital (A/D) converter allows conversion of an analog input signal to a corresponding digital number. The A/D module has 5 selectable analog inputs.
The output of sample is the input into converter , which generates the result via successive approximation.

The A/D module has four register. These registers are
- A/D CONVERTER MODE REG 0.(ADCM0)
- A/D CONVERTER MODE REG 1.(ADCM1)
- A/D CONVERTER INPUT SELECTION REG 2.(ADCIS)
- A/D CONVERTER DATA REG 0.(ADCR0)
- A/D CONVERTER DATA REG 1.(ADCR1)
- A/D CONVERTER DATA REG 2.(ADCR2)

Fig.8.1 A/D Converter Block Diagram



8.1. A/D Converter Control Registers

• A/D Converter Mode Register (ADCM0)

	3	2	1	0	
ADCM0	–	ADEN	ADST	ADSF	34h
initial value	0	0	0	1	
R/W	–	R/W	R/W	R	

Selection Mode of ADCM0

Bit Name	Selection Mode		Remarks
ADEN	0	ADC Disable	if (STOP) ADEN go to “L”
	1	ADC Enable	
ADST	0	A/D Conversion is Stop	
	1	A/D Conversion is Start. and cleared to “L” after 1 cycle	
ADSF	0	A/D Conversion is Processing	
	1	A/D Conversion is Completed	

• A/D Converter Mode Register (ADCM1)

	3	2	1	0	
ADCM1	ADCK2	ADCK1	ADCK0	AVREFS	35h
initial value	0	0	0	0	
R/W	W	W	W	W	

Selection Mode of ADCM1

Bit Name	Selection Mode		Remarks
ADCK[2:0]	000	PS0 ($f_{OSC}/2^0$)	
	001	PS1 ($f_{OSC}/2^1$)	
	010	PS2 ($f_{OSC}/2^2$)	
	011	PS3 ($f_{OSC}/2^3$)	
	100	PS4 ($f_{OSC}/2^4$)	
	101	PS5 ($f_{OSC}/2^5$)	
	110	PS6 ($f_{OSC}/2^6$)	
	111	PS7 ($f_{OSC}/2^7$)	
AVREFS	0	Internal VDD for ADC power	
	1	VREF(/PA1) for ADC power	

- A/D Converter Input Selection Register (ADCIS)

	3	2	1	0	
ADCIS	CHSEL3	CHSEL2	CHSEL1	CHSEL0	36h
initial value	0	0	0	0	
R/W	W	W	W	W	

Selection Mode of ADCIS

Bit Name	Selection Mode		Remarks
CHSEL[3:0]	0000	Channel 0 Selection	if analog port selected
	0001	Channel 1 Selection	
	0010	Channel 2 Selection	
	0011	*Prohibit*	
	0100	*Prohibit*	
	0101	*Prohibit*	
	0110	Channel 6 Selection	
	0111	Channel 7 Selection	
	1000	*Prohibit*	
	1001	*Prohibit*	
	1010	*Prohibit*	
	1011	*Prohibit*	
	1100	*Prohibit*	
	1101	*Prohibit*	
	1110	*Prohibit*	
	1111	*Prohibit*	

- A/D Converter Data Register 0 (ADCR0)

	3	2	1	0	
ADCR0	ADCR03	ADCR02	ADCR01	ADCR00	35h
initial value	–	–	–	–	
R/W	R	R	R	R	

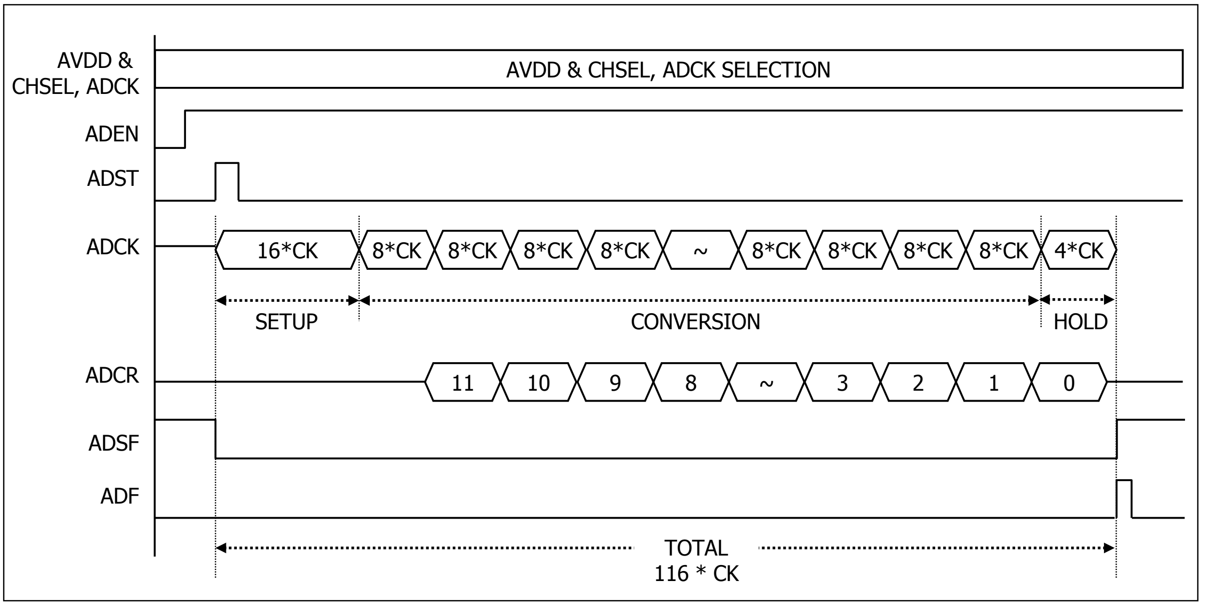
- A/D Converter Data Register 1 (ADCR1)

	3	2	1	0	
ADCR1	ADCR07	ADCR06	ADCR05	ADCR04	36h
initial value	–	–	–	–	
R/W	R	R	R	R	

- A/D Converter Data Register 2 (ADCR2)

	3	2	1	0	
ADCR2	ADCR11	ADCR10	ADCR09	ADCR08	37h
initial value	–	–	–	–	
R/W	R	R	R	R	

ADC Timing Diagram



- Total Conversion Time is

  (16 + 8*12 + 4) * ADCK

freq = 4MHz

Bit Name	Selection Mode			Remarks
ADCK	000	Conversion Source Clock ($1/f_{OSC}$)	116 * 250ns = 29us	
	010	Conversion Source Clock ($2^2/f_{OSC}$)	116 * 1us = 116us	

8.2. A/D Converter Caution

8.2.1. Noise Countermeasures of AN[7:6], AN[2:0]

It is recommend that a capacitor be connected externally as shown Fig.8.2 in order to reduce noise.

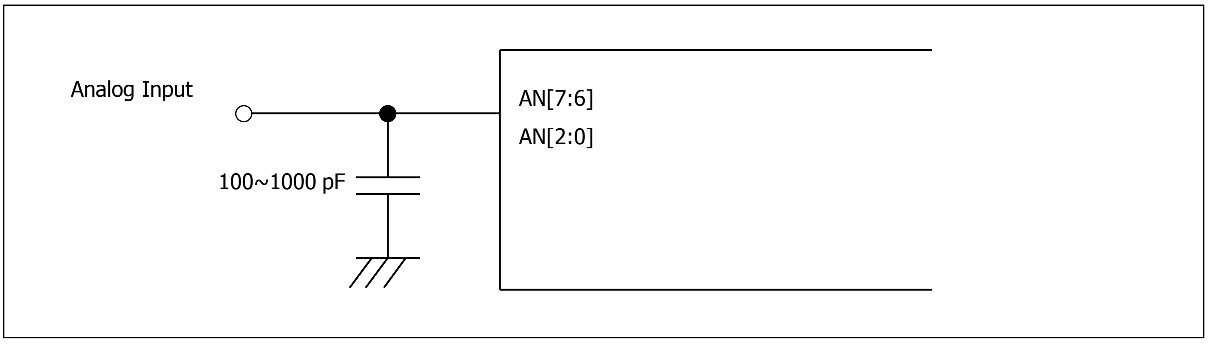


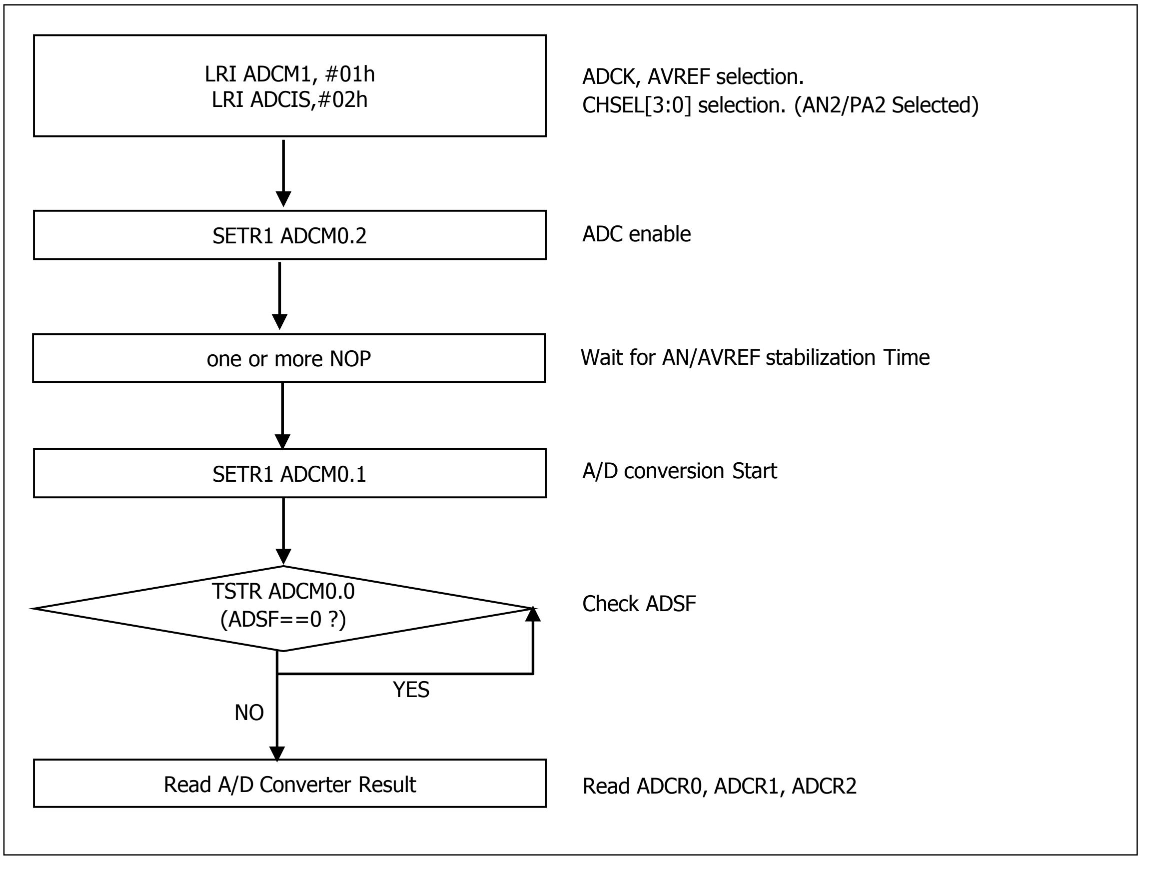
Fig.8.2 Analog input pin Connecting capacitor

8.2.2. VREF pin input impedance

A series resistor string of approximately 100kΩ~150kΩ is connected between VREF pin and VSS.

If the output impedance of VREF is high, it will result in parallel connection to the series resistor between VREF pin and GND, and there will be a large reference voltage error.

8.3. A/D Converter Operation Flow



9. Power-Down Function

In power-down mode, power consumption is reduced considerably that in battery operation battery life time can be extended a lot. For applications where power consumption is a critical factor, ADAM43P1108 provides two kinds of power-down functions, STOP mode and SLEEP mode. In this 2 Modes, program processing is stopped.

9.1. Stop Mode

STOP mode can be entered by STOP instruction during program.
In STOP mode, oscillator is stopped to make all clocks stop, which leads to less power consumption. All registers and RAM data are preserved.
"NOP" instruction should be follows STOP instruction for pre-charge time of Data Bus line.

```
ex)  STOP : STOP instruction execution
     NOP  : NOP instruction
```

Additionally, if it's executed the STOP instruction after setting the bit RCWDTEN of WDTCR to "1", the Internal RC-Oscillated Watchdog Timer mode is activated. In the Internal RC-Oscillated Watchdog Timer mode, STOP mode is also released by occurring of WDT Time-out selected by WDTCK[1:0].

The Ring-OSC oscillation period is vary with temperature, VDD and process variations from part to part. According to the bit RCWDTCK of WDTCR, the RCWDT oscillated watchdog timer time-out is shown at Chapter 5. Watch Dog Timer.

"NOP" instruction should be follows STOP instruction for pre-charge time of Data Bus line.

```
ex)  LRI   WDTCR, #0100b  : set the bit of RCWDTEN
     WDTC                 : WDT clear
     STOP                 : STOP instruction execution
     NOP                  : NOP instruction
```

9.1.1. Stop Mode Release

Release of STOP mode is executed by Power on reset , Key input Port(one of PA, PB) which is selected by PAST and PBST register for stop release makes the edge selected by IEDS1[1:0], external interrupt and Low voltage detection (LVD) mode release .
When there is a release signal of STOP mode, the instruction execution starts after stabilization oscillation time.($2^{14} \times 4/fOSC$ = 16.384ms at fOSC = 4.0MHz)

Release Factor	Release Method	Release Time
Power on Reset	By Power on reset, Stop mode is release and system is initialized.	7.2ms + $57 \times 2^{10} \times 4/fOSC$ = 65.5ms at fOSC = 4.0MHz (Option read time : about 7.2ms)
Release from LVD detection	Stop mode is release when release from LVD detection.	
External Key-scan Interrupt (PA, PB port)	Stop mode is released by the transition of input at the selected pin by PAST and PBST register.	$2^{14} \times 4/fOSC$ = 16.384ms at fOSC = 4.0MHz
External interrupt	Stop mode is release external interrupt input.	
WDT Overflow	Stop mode is release by reset or interrupt of WDT. (in RCWDT Mode only)	
External Reset	Stop mode is release external RESETB pin.	

9.2. Sleep Mode

SLEEP mode can be entered by SLEEP instruction during program.
In SLEEP mode, basically CPU and ROM halts while oscillation and peripherals are operate.
"NOP" instruction should be follows SLEEP instruction for pre-charge time of Data Bus line.

ex) SLEEP : SLEEP instruction execution
NOP : NOP instruction

9.2.1 Sleep Mode Release

Release of SLEEP mode is executed by Power on reset , all interrupts and Low voltage detection (LVD) mode release. To be release by interrupt, interrupt should be enabled before SLEEP mode.
This mode don't need the stabilization oscillation time.

Release Factor	Release Method	Release Time
Power on Reset	By Power on reset, Sleep mode is release and system is initialized.	$7.2ms + 57 \times 2^{10} \times 4/fOSC$ = 96.6ms at fOSC = 4.0MHz (Option read time : about 7.2ms)
Release from LVD detection	Sleep mode is release when release from LVD detection.	
All Interrupts	Sleep mode is released by all Interrupts.	$2^5 \times 4/fOSC$ = 32us at fOSC = 4.0MHz
External Reset	Sleep mode is release external RESETB pin.	Ext. reset pulse width. (longer than 2xTsys)

9.3. Operation States in Stop/Sleep Mode

Internal Circuit	STOP Mode	SLEEP Mode
Oscillator	Stop	Operates continuously
Internal CPU clock	Stop	Stop
Address Bus Data Bus	Retained	Retained
Registers	Retained	Retained
RAM	Retained	Retained
I/O port, Output port	Retained	Retained
Timer	Stop (Counter clear)	Operates continuously
Watch dog Timer	Stop (only operate in RCWDT mode)	Stop
ADC	Stop	Stop
RCWDT	Operate continuously (only operate in RCWDT mode)	not operate
VDI	Operates continuously	Operates continuously
Release Method	RESETB, Power-on-reset, Release from LVD, WDT(RCWDT), Ext. Interrupt, Key-input interrupt, VDI	RESETB, Power-on-reset, Release from LVD, All Interrupts (except ADC)

Table 9.1 Operation States in Stop Mode and Sleep Mode

10. RESET Function

10.1. Power On RESET

Power On Reset circuit automatically detects the rise of power voltage (the rising time should be within 50ms). Until the power voltage reaches a certain voltage level, internal reset signal is maintained at "L" Level until oscillator is stable.
After power applies, this reset state is maintained for the configuration option reading time (about 7.2ms at VDD=5.0V) and the oscillation stabilization time. ($4/f_{OSC} \times 57 \times 2^{10}$ = about 58.368ms at 4MHz).

Fig.10.1 Block Diagram of Power On Reset Circuit

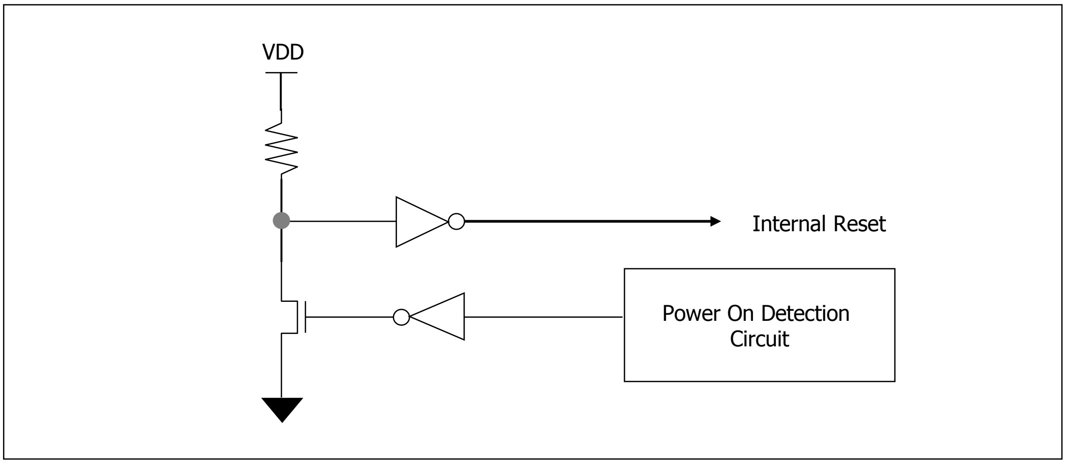
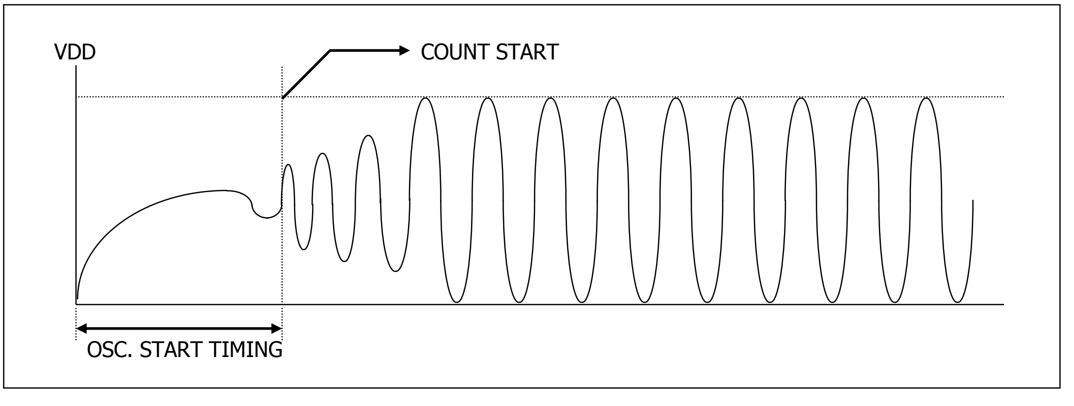


Fig.10.2 Oscillator stabilization diagram



Notice. When Power On Reset, oscillator stabilization time doesn't include OSC. Start time.

11. Low Voltage Detection Mode

11.1. Low Voltage Detection Condition

An on board voltage comparator checks that V_{DD} is at the required level to ensure correct operation of the device.
If V_{DD} is below a certain level, Low voltage detector forces the device into low voltage detection mode.

11.2. Low Voltage Detection Mode

There is no power consumption except stop current.
1. STOP mode release function is disabled.
2. I/O port is configured as input mode (without pull-up resistor).
3. Data memory is retained until voltage through external capacitor is worn out.
4. Interrupt disabled.
5. Oscillator is stop.

11.3. Release of Low Voltage Detection Mode

Reset signal result from new battery or any other power (normally 3V/5V) wakes the low voltage detection mode and come into normal reset state. It depends on user whether to execute RAM clear routine or not.

11.4. Low Voltage Detection voltage selection (option)

User can select the voltage of Low Voltage detection voltage level by OTP Configuration Bits (LVDS). One is high voltage version (typ. 2.2V, if LVDS is “0”),
another is low voltage version (typ. 1.7V, if LVDS is “1”).

12. Voltage Detection Indicator Mode

12.1. Voltage Detection Indicator Register

Voltage Detection indicator (VDI) are controlled by two registers. It is useful to display the consumption of Batteries.
If VDD power level is low and higher than low voltage detection (LVD) level (refer to Fig.13.1), the bit of VDIR register could be set according to the VDD level sequentially.
The VDD detection levels for Indication are three , that is , VDIR2 (Typ. 4.0V) , VDIR1(Typ. 3.0V) and VDIR0 (Typ. 2.5V) of VDIR register.

12.1.1. Voltage Detection Indicator Enable Register (VDIER)

bit	3	2	1	0	
VDIER	VDIM	VDIER2	VDIER1	VDIER0	*33h*
Initial value	0	0	0	0	
R/W	W	W	W	W	

VDIER0	detection level 0 (typ. 2.5V) selection	0	disable
		1	enable
VDIER1	detection level 1 (typ. 3.0V) selection	0	disable
		1	enable
VDIER2	detection level 2 (typ. 4.0V) selection	0	disable
		1	enable
VDIM	VDI Mode Selection	0	System Reset Selection
		1	Interrupt Selection

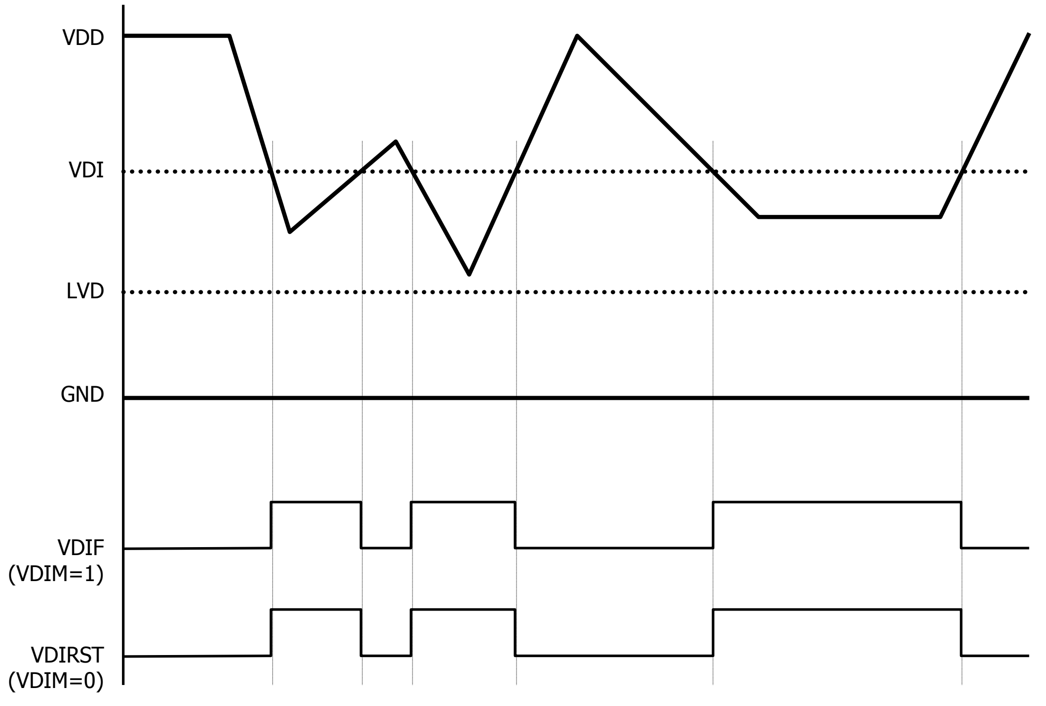
Voltage Detection Indicator Enable Register (VDIER) is 4-bit register, and can assign Indicator is enable or not.
If VDIER2 ~ VDIER0 is selected as "0", Voltage detection for Indication function is disabled and if selected as "1", it is enable. If VDIM is selected as "0" and enable one of VDIER2~VDIER0, when the corresponding voltage detection for Indication is occurred, it makes the system reset. If LVIM is selected as "1", it makes the VDI interrupt.
VDIER is write-only register and initialized as ``0 h`` in reset state.
In the in-circuit emulator, VDI function is not implemented and user can not experiment with it. Therefore after final development of user program, this function may be experimented or evaluated.

12.1.2. Voltage Detection Indicator Data Register (VDIR)

bit	3	2	1	0	
VDIR	-	VDIR2	VDIR1	VDIR0	*33h*
Initial value	0	0	0	0	
R/W	R	R	R	R	

Voltage Detection Indicator Data Register (VDIR) is 3-bit register to store data of low voltage level. VDIR is read only register and initialized as "0h" in reset state.

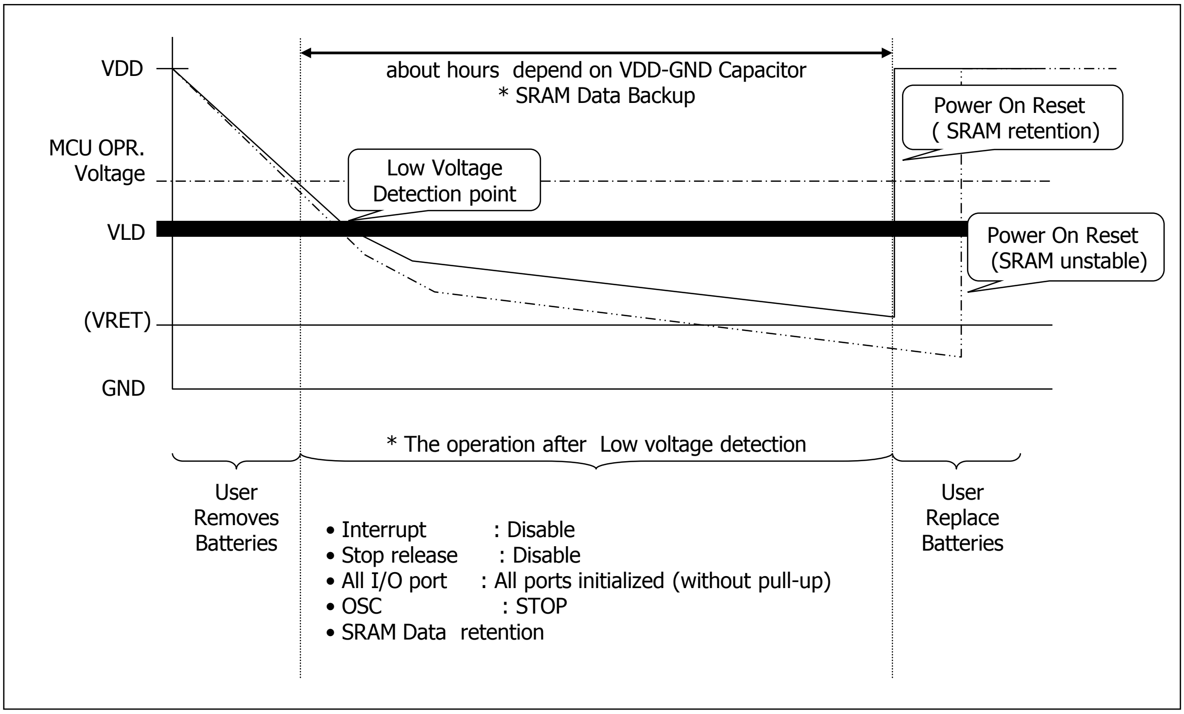
12.2. Timming Diagram



13. SRAM Data Back-Up

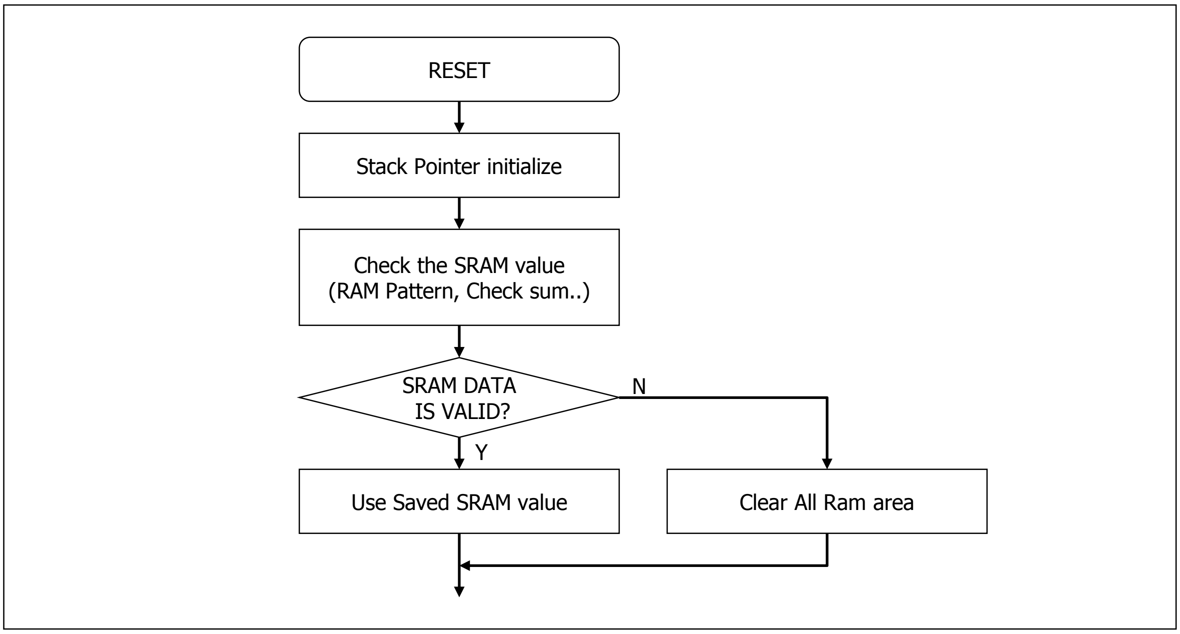
13.1 SRAM DATA BACK-UP after Low Voltage Detection

Fig.13.1 Low Voltage Detection and Protection



13.2. S/W flow chart example after Reset using SRAM DATA Back-up

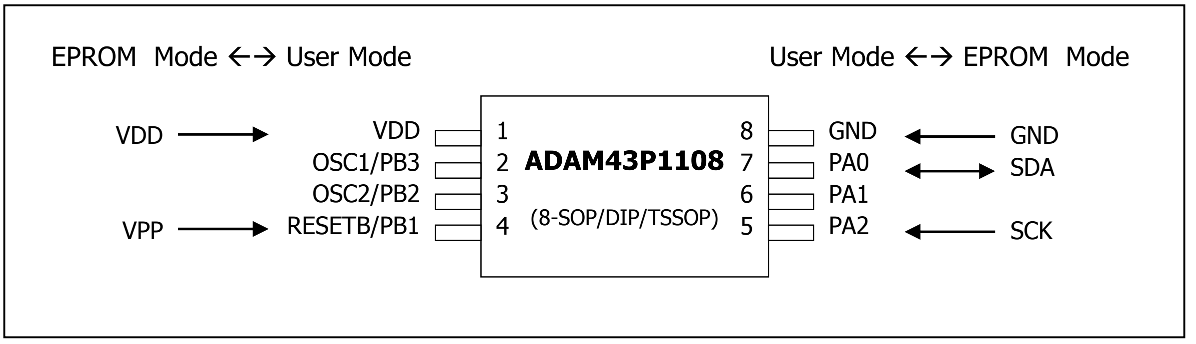
Fig.13.2 S/W Flow Chart Example for SRAM Back-up



14. MTP Programming

14.1. MTP Writing Pin Assignments

SYMBOL	User Mode	EPROM Mode
VDD	Power	VDD Power (typ. 5V)
GND	Ground	Ground (0V)
VPP	PB1	Program/Verify Power (typ. 11.5V)
SCK	PA2	Serial Clock Input
SDA	PA0	Serial Data Input/Output (Open-Drain Output)



14.2. Configuration Option Bit Description

pgm/vfy Address : 8000h

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPTION	LOCK		SIZE		RSTS	OSCS[2:0]			LVDS	RCWS	---					
Initial	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Name	OTP Code Option Description	Option Value	Remarks	
15 14	LOCK	LOCK Definition (disable or enable reading user code)	Refer to Programming Specification	It's set automatically by our MTP Writer (ADAM OTP Programmer)	
13 12	SIZE	ROM SIZE Definition (2k x 16bit or 1k x 16bit selectable)	Refer to Programming Specification		
11	RSTS	RESETB/PB1 Selection	1	RESETB	
			0	PB1	
10:8	OSCS	Oscillator Type Selection	OSCS[2:0]	PB3/OSC1	PB2/OSC2
		Internal RC 4MHz	111	PB3(I/O)	PB2(I/O)
		Internal RC 8MHz	110	↑	↑
		Internal RC 16MHz	101	↑	↑
		External RC Oscillator	100	OSC1(I)	PB2(I/O)
		External Clock Input	011	↑	↑
		XT Oscillator	010	OSC1(I)	OSC2(O)
		LP Oscillator	001	↑	↑
		Internal RC 1MHz	000	PB3(I/O)	PB2(I/O)
7	LVDS	LVD Level Selection	1	LVD=1.7V	
			0	LVD=2.2V	
6	RCWS	RCWDT Source Clock Selection	1	T_{RCWDT} = 16us	
			0	T_{RCWDT} = 8us	

15. Instruction Set

15.1. Legend

A : accumulator(4bit)

r : peripheral address register(6bit)

[r] : data addressed by peripheral address register (4bit)

Y : Y register(4bit)

X : X register(4bit)

ABR : address buffer register(15bit)

ABRn : address buffer register #0~3(4bit)

[@ABR] : data addressed by ABR(16bit)

DBR : data buffer register(16bit)

DBRn : data buffer register #0~3(4bit)

T0CR : Timer 0 count register(8bit)

T1CR : Timer 1 count register(8bit)

#n4 : 0~Fh

#n2 : 0~3

#n1 : 0~1

dp : data address point(8bit)

dp+X+Y : data address point indexed by X-register and Y-register (8bit)

PG : page address(1bit)

ADS : address stack register

!abs : address

15.2. Instruction Set Table

NO	INSTRUCTION GROUP	MNEMONIC	USAGE	OPERATION	S	CY
1	Arithmetic & Logic	ADDC	ADDC m(dp),#n4	A = m(dp)+#n4+CY A = m(dp+X+Y)+#n4+CY at D flag of SFR is set. "S" set if overflow.	C	O
2			ADDC A,#n4	A = A+#n4+CY, "S" set if overflow	C	O
3			ADDC m(dp), A	A = m(dp) +A+CY, A = m(dp+X+Y) +A+CY at D flag of SFR is set. "S" set if overflow	C	O
4			ADDC ABRn,#n4	ABRn = ABRn + #n4+CY, "S" set if overflow	C	O
5			ADDC ABRn,A	ABRn = ABRn + A+CY, "S" set if overflow	C	O
6			ADDC ABRn,Y	ABRn = ABRn + Y+CY, "S" set if overflow	C	O
7			ADDC DBRn,#n4	DBRn = DBRn + #n4+CY, "S" set if overflow	C	O
8			ADDC DBRn,A	DBRn = DBRn + A+CY, "S" set if overflow	C	O
9			ADDC DBRn,Y	DBRn = DBRn + Y+CY, "S" set if overflow	C	O
10			ADDC Y,#n4	Y = Y + #n4 + CY, "S" set if overflow	C	O
11			ADDC X,#n4	X = X + #n4 + CY, "S" set if overflow	C	O

12		SUBC	SUBC m(dp),#n4	A = m(dp) - #n4-CY,
				A = m(dp+X+Y)- #n4-CY at D flag of SFR is set.
				"S" clear if underflow
					B	W

13			SUBC A,#n4	A = A - #n4-CY, "S" clear if underflow	B	W
14			SUBC m(dp), A	A = m(dp) – A-CY, A = m(dp+X+Y)- A-CY at D flag of SFR is set. "S" clear if underflow	B	W
15			SUBC ABRn, #n4	ABRn = ABRn - #n4-CY, "S" clear if underflow	B	W
16			SUBC ABRn, A	ABRn = ABRn – A-CY, "S" clear if underflow	B	W
17			SUBC ABRn, Y	ABRn = ABRn – Y-CY, "S" clear if underflow	B	W
18			SUBC DBRn, #n4	DBRn = DBRn - #n4-CY, "S" clear if underflow	B	W
19			SUBC DBRn, A	DBRn = DBRn - A-CY, "S" clear if underflow	B	W
20			SUBC DBRn, Y	DBRn = DBRn - Y-CY, "S" clear if underflow	B	W
21			SUBC Y, #n4	Y = Y- #n4-CY, "S" clear if underflow	B	W
22			SUBC X, #n4	X = X- #n4-CY, "S" clear if underflow	B	W
23		ARRC	ARRC	A = A rotate right with CY	T	R
24		ARLC	ARLC	A = A rotate left with CY	T	R
25		CMPL	CMPL	A = $\overline{A}$ + 1	Z	.
26		XOR	XOR m(dp)	A = A $\oplus$ m(dp) , A = A $\oplus$ m(dp+X+Y) at D flag of SFR is set	S	.
27		AND	AND m(dp)	A = A ^ m(dp) , A = A ^ m(dp+X+Y) at D flag of SFR is set	S	.
28		OR	OR m(dp)	A = A v m(dp) , A = A v m(dp+X+Y) at D flag of SFR is set	S	.

NO	INSTRUCTION GROUP	MNEMONIC	USAGE	OPERATION	S	CY
29	Compare	CALE	CALE #n4	"S" set if A <= #n4	E	.
30			CALE m(dp)	"S" set if A <= m(dp), "S" set if A <= m(dp+X+Y) at D flag of SFR is set.	E	.
31		CAGE	CAGE #n4	"S" set if A >= #n4	E	.
32		CANE	CANE #n4	"S" set if A != #n4	N	.
33			CANE m(dp)	"S" set if A != m(dp), "S" set if A != m(dp+X+Y) at D flag of SFR is set.	N	.
34		CMLE	CMLE m(dp),#n4	"S" set if m(dp) <= #n4, "S" set if m(dp+X+Y) <= #n4 at D flag of SFR is set.	E	.
35		CMNE	CMNE m(dp),#n4	"S" set if m(dp) != #n4, "S" set if m(dp+X+Y) = #n4 at D flag of SFR is set.	N	.
36		CYGE	CYGE #n4	"S" set if Y >= #n4	E	.
37		CYNE	CYNE #n4	"S" set if Y != #n4	N	.
38			CYNE A	"S" set if Y != A	N	.
39		CXGE	CXGE #n4	"S" set if X >= #n4	E	.
40		CXNE	CXNE #n4	"S" set if X != #n4	N	.
41	Bit Manipulation	SET1	SET1 m(dp).#n2	Set bit m(dp).#n2, Set bit m(dp+X+Y).#n2 at D flag of SFR is set.	S	.
42		CLR1	CLR1 m(dp).#n2	Clear bit m(dp).#n2, Clear bit m(dp+X+Y).#n2 at D flag of SFR is set.	S	.
43		TM	TM m(dp).#n2	"S" set if m(dp) Bit = 1 "S" set if m(dp+X+Y) Bit = 1 at D flag of SFR is set.	E	.
44		SETR1	SETR1 r. #n2	Set bit [r]. #n2	S	.
45		CLRR1	CLRR1 r. #n2	Clear bit [r]. #n2	S	.
46		TSTR	TSTR r. #n2	"S" set if [r]. #n2 Bit = 1	E	.
47		NOTA1	NOTA1 #n2	A.#n2 ← ~ (A.#n2)	S	.
48	Carry Manipulation	CLRC	CLRC	Carry Bit of SFR is clear.	S	0
49		SETC	SETC	Carry Bit of SFR is set.	S	1
50		TSTC	TSTC	"S" set if Carry Test = 1.	E	.
51		LDC	LDC r.#n2	CY ← [r].#n2	S	.
52		STC	STC r.#n2	[r].#n2 ← CY	S	.
53	DATA Transfer	LDM	LDM m(dp),#n4	m(dp) = #n4 m(dp+X+Y) = #n4 at D flag of SFR is set.	S	.
54			LDM m(dp), A	m(dp) ← A m(dp+X+Y) ← A at D flag of SFR is set.	S	.
55		LDA	LDA #n4	A = #n4	S	.
56			LDA m(dp)	A ← m(dp) A ← m(dp+X+Y) at D flag of SFR is set.	S	.

NO	INSTRUCTION GROUP	MNEMONIC	USAGE	OPERATION	S	CY
57	DATA Transfer	LDA	LDA X	A ← X	S	.
58			LDA Y	A ← Y	S	.
59		LDY	LDY #n4	Y = #n4	S	.
60			LDY A	Y ← A	S	.
61		LDX	LDX #n4	X = #n4	S	.
62			LDX A	X ← A	S	.
63		XMA	XMA m(dp)	A <=> m(dp) A <=> m (dp+X+Y) at D flag of SFR is set.	S	.
64		LDW	LDW @ABR	DBR ← (@ABR) **[Note]	S	.
65			LDW DBR,ABR	DBR ← ABR	S	.
66			LDW ABR,DBR	ABR ← DBR	S	.
67			LDW DBR,T0CR	DBR1,DBR0 ← T0CR	S	.
68			LDW DBR,T1CR	DBR3,DBR2 ← T1CR	S	.
69		LPG	LPG #n1	PG = #n1	S	.
70		LRA	LRA r	[r] ← A	S	.
71		LAR	LAR r	A ← [r]	S	.
72		LRI	LRI r,#n4	[r] = #n4	S	.
73	Increment	INC	INC ABR	ABR++	-	.
74	Branch	BR	BR !abs	If S bit of SFR =1 , Absolute branch, PC ← !abs	S	.
75			BR @ABR	If S bit of SFR =1 , Indirect branch PG+PC ← ABR	S	.
76	Subroutine	CALL	CALL !abs	If S bit of SFR =1 , ADS ← PG + PC, SP ← SP – 1 , PC ← !abs	S	.
77			CALL @ABR	If S bit of SFR =1 , ADS ← PG + PC, SP ← SP – 1 , PG+PC ← ABR	S	.
78		RET	RET	SP ← SP +1, PG+PC ← ADS	S	.
79		RETI	RETI	SPSFR ← SPSFR +1, SFR ← M(SPSFR) SP ← SP +1, PG+PC ← ADS	S	.
80	Etc	NOP	NOP		S	.
81		STOP	STOP		S	.
82		SLEEP	SLEEP		S	.
83		WDTC	WDTC	Watchdog Timer Clear	S	.
84		SPC	SPC	Stack Pointer Clear	S	.
85		EIX	EIX	Index bit of SFR is set	S	.
86		DIX	DIX	Index bit of SFR is clear	S	.
87		EI	EI	Interrupt bit of SFR is set	S	.
88		DI	DI	Interrupt bit of SFR is clear	S	.

**[Note] The Instruction "LDW @ABR" execution time is 2cycle and execution process is as follow.
SP = SP-1 , ADS← PG+PC ,
PG+PC ← ABR , DBR ← (PG+PC) , PG+PC ← ADS , SP = SP+1
.

** CARRY BIT(CY) hold previous value before execution CLRC/SETC instruction .
Symbols have meaning as follows.
- O : Carry bit is only set when overflow has occurred in operation.
- W : Carry bit is only set when borrow has occurred in operation.
- R : Carry bit is only set or reset according to shift bit.

** STATUS BIT(S) indicates conditions for changing status. Symbols have meaning as follows.
- S : On executing an instruction, status bit is unconditionally set.
- C : Status bit is only set when overflow has occurred in operation.
- B : Status bit is only set when underflow has not occurred in operation.
- E : Status bit is only set when equality is found in comparison.
- N : Status bit is only set when equality is not found in comparison.
- Z : Status bit only set when the result is zero.
- T : Status bit only set when the carry has occurred in operation.